290-MHz LOW-DISTORTION HIGH-SPEED AMPLIFIERS

Check for Samples: THS4011, THS4012

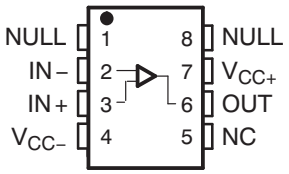
FEATURES

- **High Speed**
  - **290-MHz Bandwidth (G = 1, –3 dB)**
  - **310-V/ms Slew Rate**
  - **37-ns Settling Time (0.1%)**
- **Low Distortion**
  - **THD = –80 dBc (f = 1 MHz, R_L = 150 Ω)**
- **110-mA Output Current Drive (Typical)**
- **7.5-nV/√Hz Voltage Noise**
- **Excellent Video Performance**
  - **70-MHz Bandwidth (0.1 dB, G = 1)**
  - **0.006% Differential Gain Error**
  - **0.01° Differential Phase Error**
- **±5-V to ±15-V Supply Voltage**
- **Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Packages**
- **Evaluation Module Available**

DESCRIPTION

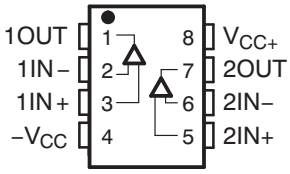
The THS4011 and THS4012 are high-speed, single/dual, voltage feedback amplifiers ideal for a wide range of applications. The devices offer good ac performance, with 290-MHz bandwidth, 310-V/μs slew rate, and 37-ns settling time (0.1%). These amplifiers have a high output drive capability of 110 mA and draw only 7.8-mA supply current per channel. For applications requiring low distortion, the THS4011/4012 operate with a total harmonic distortion (THD) of -80 dBc at f = 1 MHz. For video applications, the THS4011/4012 offer 0.1-dB gain flatness to 70 MHz, 0.006% differential gain error, and 0.01° differential phase error.

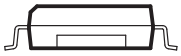
THS4011
D, DGN, OR JG PACKAGE
(TOP VIEW)



NC – No internal connection

THS4012
D OR DGN† PACKAGE
(TOP VIEW)

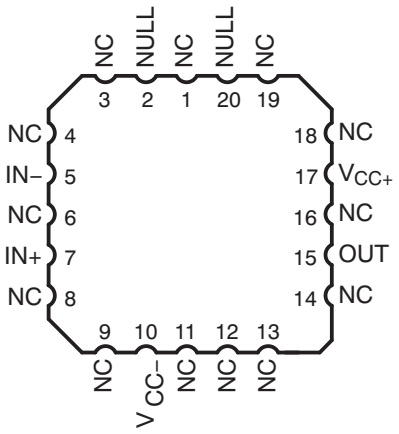




Cross-section view showing PowerPAD option (DGN)

† This package is in the Product Preview stage of development. Please contact your local TI sales of fice for availability.

THS4011
FK PACKAGE
(TOP VIEW)



RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/4012	290-MHz low-distortion high-speed amplifiers
THS4031/4032	100-MHz low-noise high-speed-amplifiers
THS4061/4062	180-MHz high-speed amplifiers

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

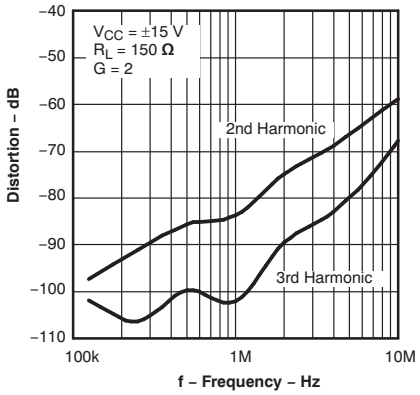
PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DISTORTION vs FREQUENCY



AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES(1)		MSOP SYMBOL	PACKAGED DEVICES		EVALUATION MODULE
		PLASTIC SMALL OUTLINE(2) (D)	PLASTIC MSOP(2) (DGN)		CERAMIC DIP (JG)	CHIP CARRIER (FK)	
0°C to 70°C	1	THS4011CD	THS4011CDGN	TIACI	—	—	THS4011EVM
	2	THS4012CD	THS4012CDGN(3)	TIABY	—	—	THS4012EVM
–40°C to 85°C	1	THS4011ID	THS4011DGN	TIACJ	—	—	—
	2	THS4012ID	THS4012IDGN(3)	TIABZ	—	—	—
–55°C to 125°C	1	—	—	—	THS4011MJG	THS4011MFK	—

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4011CDGNR).
(3) This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

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FUNCTIONAL BLOCK DIAGRAM

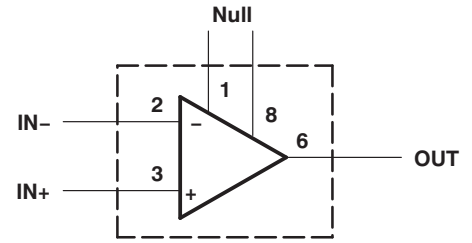


Figure 1. THS4011 – Single Channel

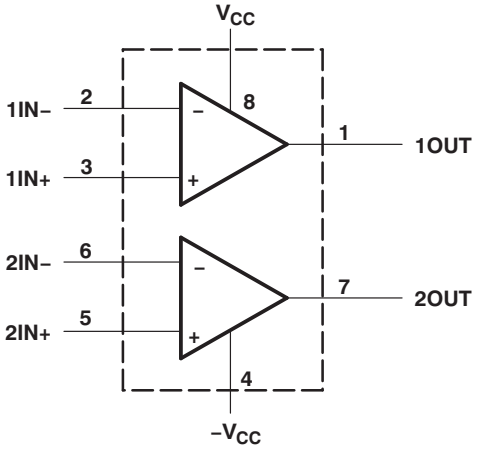


Figure 2. THS4012 – Dual Channel

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_{CC}	Supply voltage		±16.5	V
V_I	Input voltage		$\pm V_{CC}$	
I_O	Output current		175	mA
V_{ID}	Differential input voltage		±4	V
	Continuous total power dissipation		See Dissipation Rating Table	
T_J	Maximum junction temperature		150	°C
T_A	Operation free-air temperature range	THS401xC	0 to 70	°C
		THS401xI	–40 to 85	°C
		THS4011M	–55 to 125	°C
T_{stg}	Storage temperature range		–65 to 150	°C

DISSIPATION RATINGS

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167(1)	38.3	740 mW
DGN(2)	58.4	4.7	2.14 W
JG	119	28	1050 mW
FK	87.7	20	1375 mW

(1) This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC-proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at 1.32 W at T_A = 25°C.
(2) This data was taken using 2-oz trace and copper pad that is soldered directly to a 3-in × 3-in PC. For further information, refer to the Application Information section of this data sheet.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Split supply	±4.5	±16	V
		Single supply	9	32	
T_A	Operating free-air temperature	C suffix	0	70	°C
		I suffix	–40	85	
		M suffix	–55	125	

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ELECTRICAL CHARACTERISTICS

V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		THS4011C/I THS4012C/I TYP	UNIT
DYNAMIC PERFORMANCE					
BW	Unity-gain bandwidth (–3 dB)	Gain = 1	V_{CC} = ±15 V	290	MHz
			V_{CC} = ±5 V	270	
	Bandwidth for 0.1-dB flatness	Gain = 1	V_{CC} = ±15 V	70	MHz
			V_{CC} = ±5 V	35	
	Full-power bandwidth(2)	V_{CC} = ±15 V, R_L = 150 Ω	$V_{O(PP)}$ = 20 V	4.9	MHz
		V_{CC} = ±5 V, R_L = 150 Ω	$V_{O(PP)}$ = 5 V	16	MHz
SR	Slew rate	Gain = –1, R_L = 150 Ω	V_{CC} = ±15 V	310	V/μs
			V_{CC} = ±5 V	260	
t_s	Settling time to 0.1%	V_I = –2.5 V to 2.5 V, Gain = –12	V_{CC} = ±15 V	37	ns
			V_{CC} = ±5 V	35	
	Settling time to 0.01%	V_I = –2.5 V to 2.5 V, Gain = –12	V_{CC} = ±15 V	90	ns
			V_{CC} = ±5 V	70	
NOISE/DISTORTION PERFORMANCE					
THD	Total harmonic distortion	V_{CC} = ±15 V, f_c = 1 MHz,	$V_{O(PP)}$ = 2 V	–80	dBc
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz	7.5	nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz	1	pA/√Hz
	Differential gain error	. Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V	0.01%	
			V_{CC} = ±5 V	0.01%	
	Differential phase error	. Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V	0.01°	
			V_{CC} = ±5 V	0.001°	

(1) Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.
(2) Full-power bandwidth = Slew rate/2π V_O(peak)

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ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		THS4011C/I THS4012C/I			UNIT
				MIN	TYP	MAX	
DC PERFORMANCE							
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	10	25		V/mV
			T_A = Full range	8			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 250 Ω	T_A = 25°C	7	12		
			T_A = Full range	5			
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	6	mV
			T_A = Full range			8	
	Input offset voltage drift					15	µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	6	µA
			T_A = Full range			8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		25	250	nA
			T_A = Full range			400	
	Offset current drift	V_{CC} = ±5 V or ±15 V			0.3		nA/°C
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13	±14.1		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V, V_{IC} = ±12 V	T_A = 25°C	82	110		dB
			T_A = Full range	77			
		V_{CC} = ±5 V, V_{IC} = ±2.5 V	T_A = 25°C	90	95		
			T_A = Full range	83			
R_I	Input resistance				2		MΩ
C_I	Input capacitance				1.2		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.4	±3.7		
		V_{CC} = ±15 V,	R_L = 250 Ω	±12	±13		
		V_{CC} = ±5 V,	R_L = 150 Ω	±3	±3.4		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	70	110		mA
		V_{CC} = ±5 V		50	75		
I_{OS}	Short-circuit output current	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			12		Ω
POWER SUPPLY							
V_{CC}	Supply voltage	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15 V	T_A = 25°C		7.8	9.5	mA
			T_A = Full range			11	
		V_{CC} = ±5 V	T_A = 25°C		6.9	8.5	
			T_A = Full range			10	
PSRR	Power-supply rejection ratio	V_{CC} = ±5 V to ±15 V	T_A = 25°C	75	83		dB
			T_A = Full range	68			

(1) Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

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ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		THS4011M			UNIT
				MIN	TYP	MAX	
DYNAMIC PERFORMANCE							
	Unit-gain bandwidth	Closed loop, R_L = 1 kΩ,	V_{CC} = ±15 V	160[2]	200		MHz
BW	Bandwidth for 0.1-dB flatness	Gain = 1	V_{CC} = ±15 V		70		MHz
			V_{CC} = ±5 V		35		MHz
			V_{CC} = ±2.5 V		30		MHz
	Full-power bandwidth[3]	V_{CC} = ±15 V, R_L = 150 Ω,	$V_{O(PP)}$ = 20 V		2.5		MHz
		V_{CC} = ±5 V, R_L = 150 Ω,	$V_{O(PP)}$ = 20 V		8		MHz
SR	Slew rate	V_{CC} = ±15 V, R_L = 1 kΩ		300[2]	400		V/µs
t_s	Settling time to 0.1%	V_I = –2.5 to 2.5 V, Gain = –1	V_{CC} = ±15 V		37		ns
			V_{CC} = ±5 V		35		ns
	Settling time to 0.01%	V_I = –2.5 to 2.5 V, Gain = –1	V_{CC} = ±15 V		90		ns
			V_{CC} = ±5 V		70		ns
NOISE/DISTORTION PERFORMANCE							
THD	Total harmonic distortion	V_{CC} = ±15 V, f_c = 1 MHz, $V_{O(PP)}$ = 1 V			–80		dBc
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		7.5		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		1		pA/√Hz
	Differential gain error	Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V		0.006%		
			V_{CC} = ±5 V		0.001%		
	Differential phase error	Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V		0.01°		
			V_{CC} = ±5 V		0.002°		

(1) Full range = –55°C to 125°C for the M suffix
(2) This parameter is not tested.
(3) Full-power bandwidth = Slew rate/2π V_O(peak)

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ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = ±15 V, R_L = 1 kΩ, T_A = full range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		THS4011M			UNIT
				MIN	TYP	MAX	
DC PERFORMANCE							
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = Full range	6	14		V/mV
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ		5	10		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	6	mV
			T_A = Full range		2	8	
	Input offset voltage drift	V_{CC} = ±5 V or ±15 V			15		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	6	µA
			T_A = Full range		4	8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V			25	250	nA
	Offset current drift	V_{CC} = ±5 V or ±15 V	T_A = 25°C		0.3		nA/°C
INPUT CHARACTERISTICS							
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13	±14.1		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V, V_{IC} = ±12 V		75	90		dB
		V_{CC} = ±5 V, V_{IC} = ±2.5 V		84	95		
R_I	Input resistance				2		MΩ
C_I	Input capacitance				1.2		pF
OUTPUT CHARACTERISTICS							
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.4	±3.7		
		V_{CC} = ±15 V,	R_L = 250 Ω	±12	±13		
		V_{CC} = ±5 V,	R_L = 150 Ω	±3	±3.4		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	65	115		mA
		V_{CC} = ±5 V		40	75		
I_{OS}	Short-circuit output current	V_{CC} = ±15 V,	T_A = 25°C		150		mA
R_O	Output resistance	Open loop			12		Ω
POWER SUPPLY							
V_{CC}	Supply voltage	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current	V_{CC} = ±15 V	T_A = 25°C		7.8	9.5	mA
			T_A = Full range			11	
		V_{CC} = ±5 V	T_A = 25°C		6.9	8.5	
			T_A = Full range			10	
PSRR	Power-supply rejection ratio	V_{CC} = ±5 V to ±15 V	T_A = 25°C	80	86		dB
			T_A = Full range	78	83		

(1) Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

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PARAMETER MEASUREMENT INFORMATION

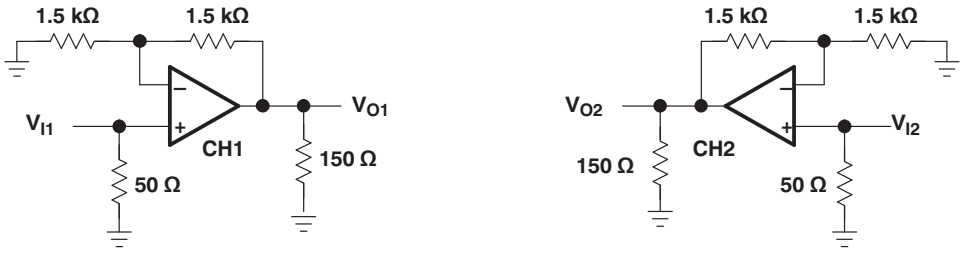


Figure 3. THS4012 Crosstalk Test Circuit

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

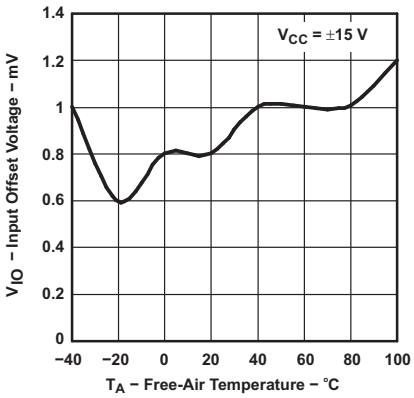


Figure 4.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

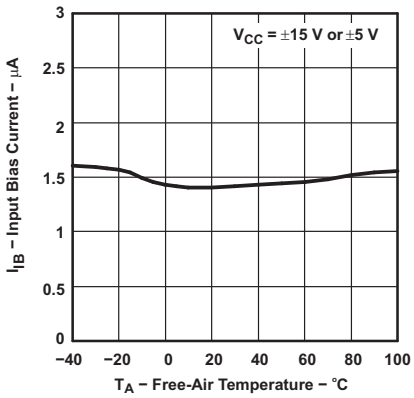


Figure 5.

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

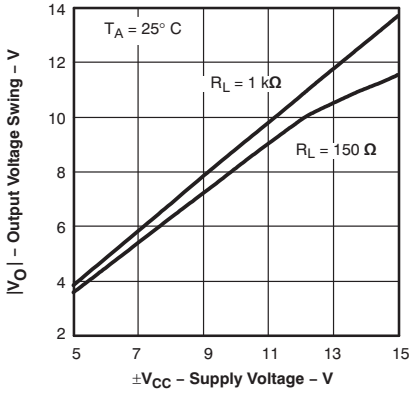


Figure 6.

MAXIMUM OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

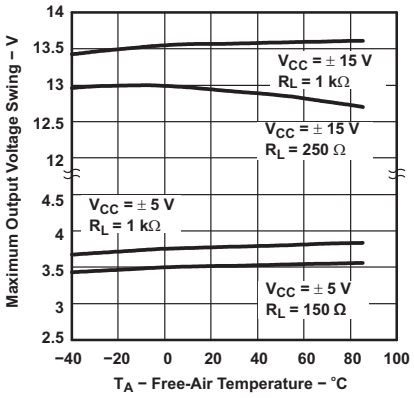


Figure 7.

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

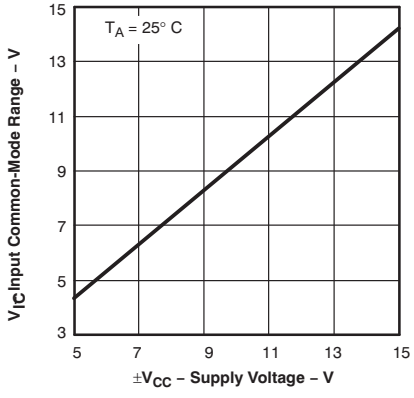


Figure 8.

PSRR vs FREQUENCY

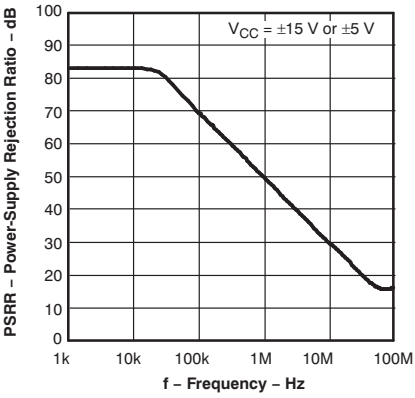


Figure 9.

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TYPICAL CHARACTERISTICS (continued)

CMRR vs FREQUENCY

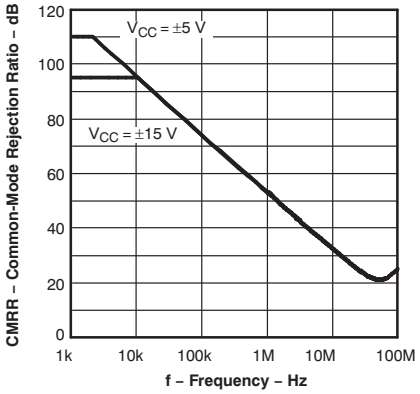


Figure 10.

CROSSTALK vs FREQUENCY

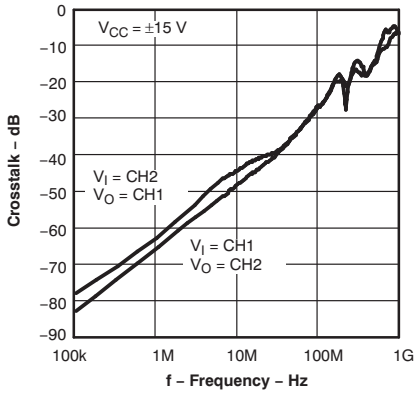


Figure 11.

OPEN-LOOP GAIN RESPONSE vs FREQUENCY

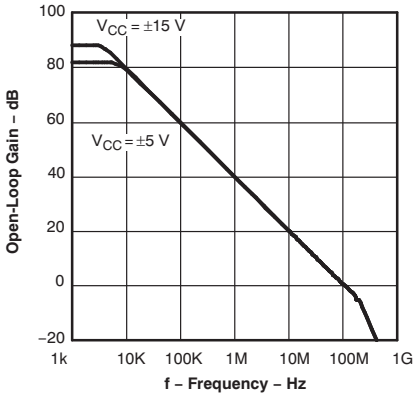


Figure 12.

DISTORTION vs FREQUENCY

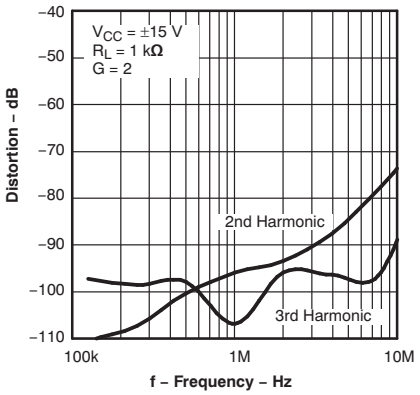


Figure 13.

DISTORTION vs FREQUENCY

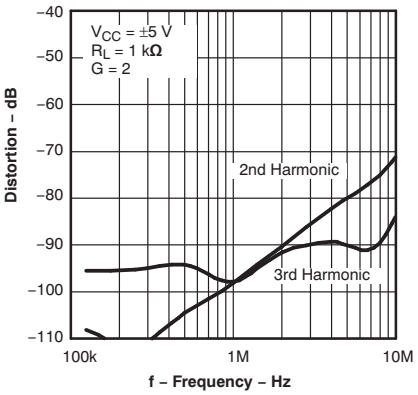


Figure 14.

DISTORTION vs FREQUENCY

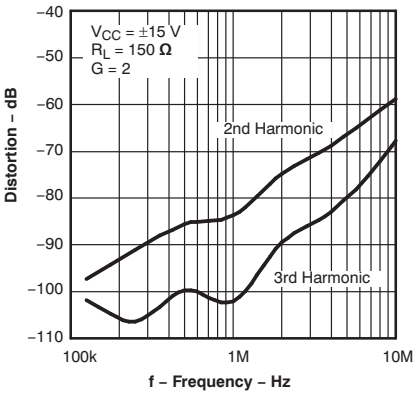


Figure 15.

DISTORTION vs FREQUENCY

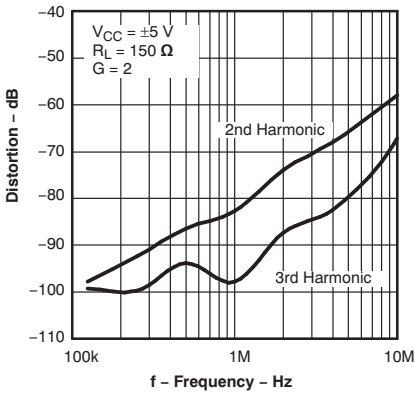


Figure 16.

OUTPUT AMPLITUDE vs FREQUENCY

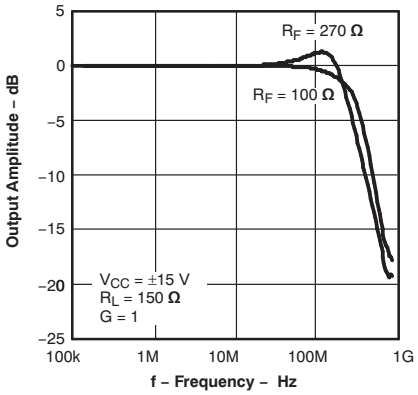


Figure 17.

OUTPUT AMPLITUDE vs FREQUENCY

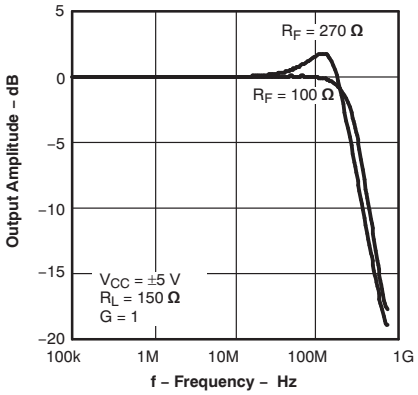


Figure 18.

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TYPICAL CHARACTERISTICS (continued)

NOISE SPECTRAL DENSITY vs FREQUENCY

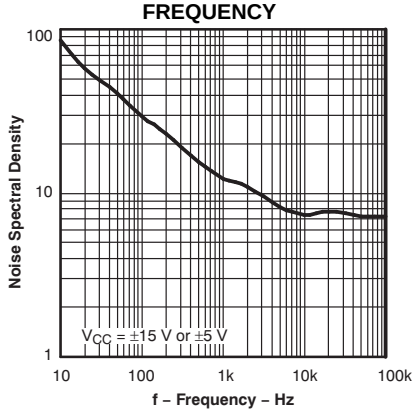


Figure 19.

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

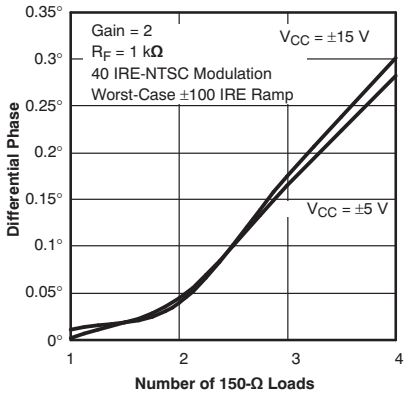


Figure 20.

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

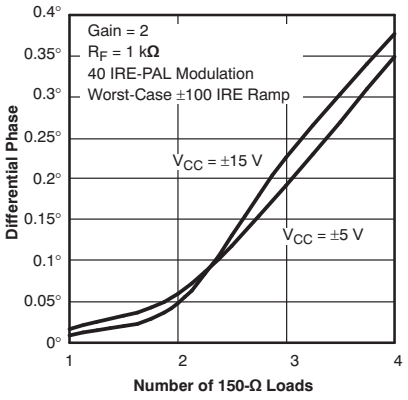


Figure 21.

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

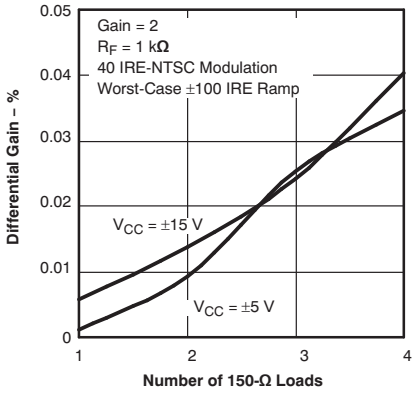


Figure 22.

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

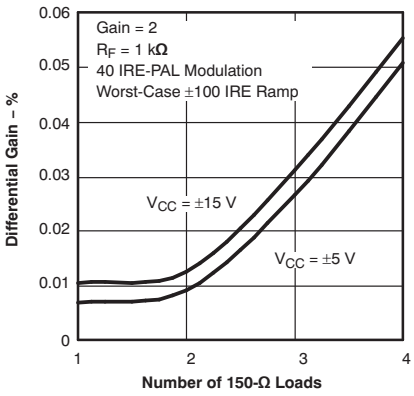
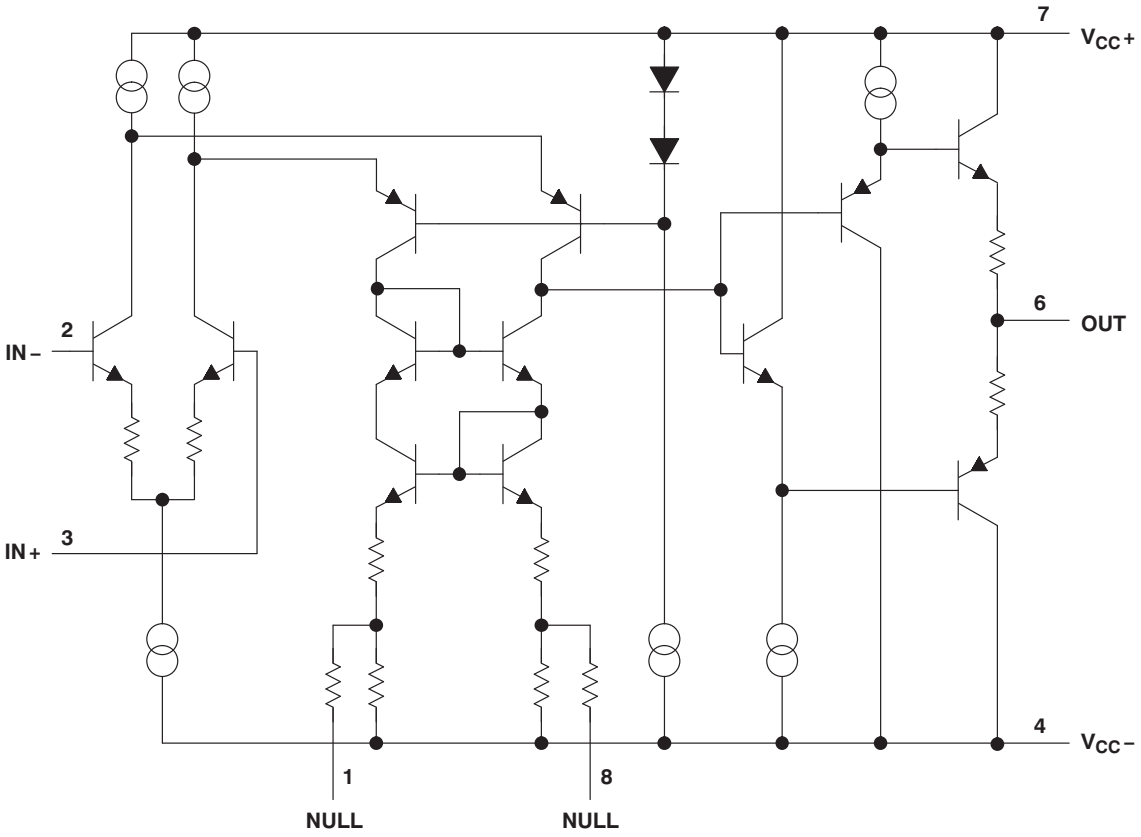


Figure 23.

APPLICATION INFORMATION

THEORY OF OPERATION

The THS401x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process, with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 24.



Pin numbers are for the D, DGN, and JG packages.

Figure 24. THS4011/4012 Simplified Schematic

Noise Calculations and Noise Figure (NF)

Noise can cause errors on very small signals. This is especially true when amplifying small signals. The noise model for the THS401x is shown in Figure 25. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

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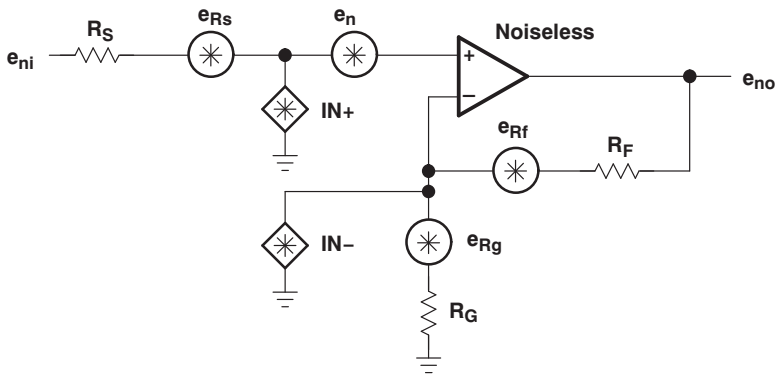


Figure 25. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 + °C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise density of the amplifier, multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V):

$$e_{no} = e_{ni} A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small-value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, refer to the *Noise Analysis* section in the *Operational Amplifier Circuits Applications Report* (SLVA043).

This brings up another noise measurement usually preferred in RF applications — the noise figure (NF). NF is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, approximate NF as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\,kTR_S}\right]$$

Figure 26 shows the NF graph for the THS401x.

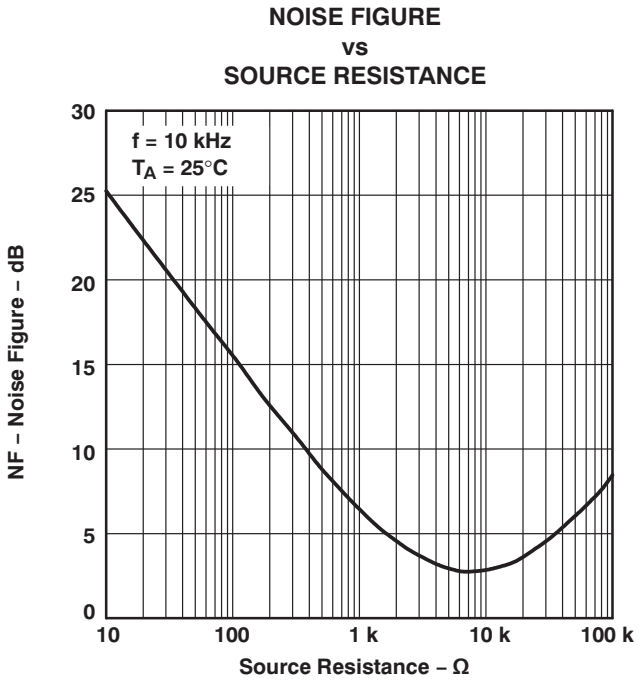


Figure 26. Noise Figure vs Source Resistance

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high performance amplifiers is not a problem, as long as certain precautions are taken. The first precaution is to note that the THS401x has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 27. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series-resistor value to 75 Ω both isolates any capacitance loading and provides the proper line-impedance matching at the source end.

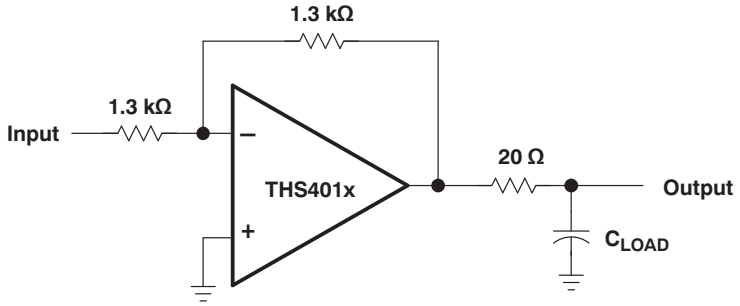


Figure 27. Driving a Capacitive Load

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OFFSET NULLING

The THS401x has low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4011/4012. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply (see Figure 28).

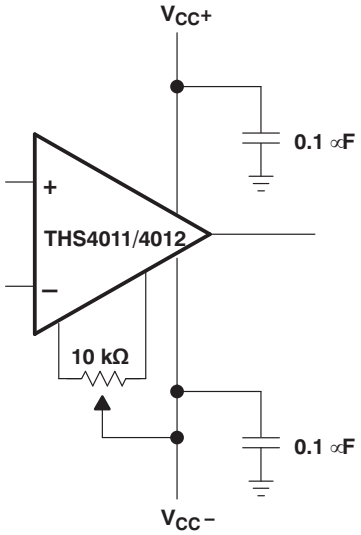
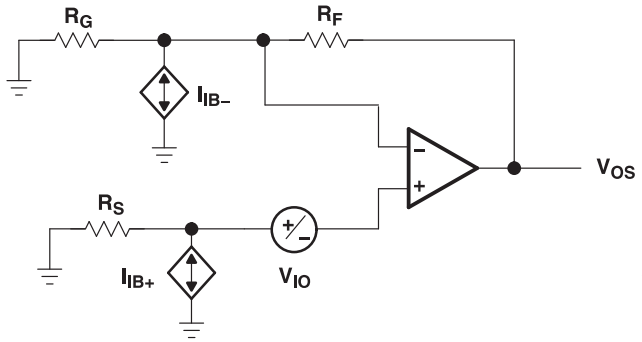


Figure 28. Offset Nulling Schematic

OFFSET VOLTAGE

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 29. Output Offset Voltage Model

OPTIMIZING UNITY GAIN RESPONSE

Internal frequency compensation of the THS401x was selected to provide very wideband performance, yet maintain stability when operating in a noninverting unity gain configuration. When amplifiers are compensated in this manner, there is usually peaking in the closed-loop response and some ringing in the step response for fast input edges, depending on the application. This is because a minimum phase margin is maintained for the G = +1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 100 Ω should be used (see Figure 30). Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

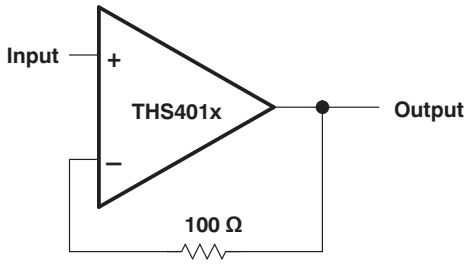
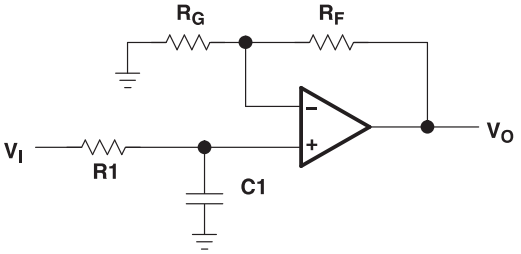


Figure 30. Noninverting Unity Gain Schematic

GENERAL CONFIGURATIONS

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 31).



$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 31. Single-Pole Low-Pass Filter

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If even more attenuation is needed, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

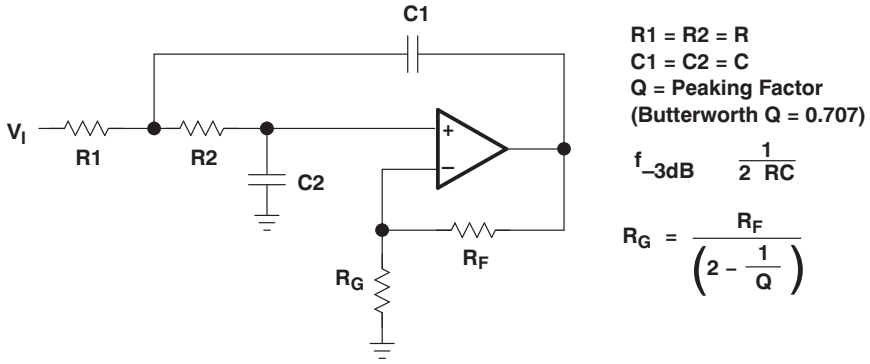


Figure 32. 2-Pole Low-Pass Sallen-Key Filter

CIRCUIT LAYOUT CONSIDERATIONS

To achieve the high-frequency performance levels of the THS401x, follow proper printed circuit board (PCB) high-frequency design techniques. A general set of guidelines is given in the following paragraphs. In addition, a THS401x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 in between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often leads to stability problems. Surface-mount packages soldered directly to the PCB are the best implementation.
- Short trace runs/compact part placements – Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This minimizes stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

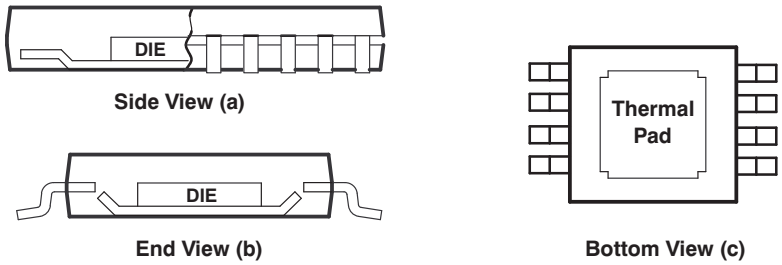
GENERAL PowerPAD™ DESIGN CONSIDERATIONS

The THS401x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 33(a) and Figure 33(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 33(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

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The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE: The thermal pad is electrically isolated from all terminals in the package.

Figure 33. Thermally-Enhanced DGN Package Views

Although there are many ways to properly heatsink this device, the following steps show the recommended approach:

1. Prepare the PCB with a top-side etch pattern as shown in Figure 34. There should be etch for the leads, as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal-pad area. This helps dissipate the heat generated by the THS401xDGN IC. These additional vias may be larger than the 13-mils diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS401xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal-pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal-pad area. This prevents solder from pulling away from the thermal-pad area during the reflow process.
7. Apply solder paste to the exposed thermal-pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS401xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

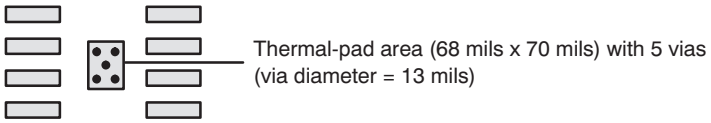


Figure 34. PowerPAD™ PCB Etch and Via Pattern

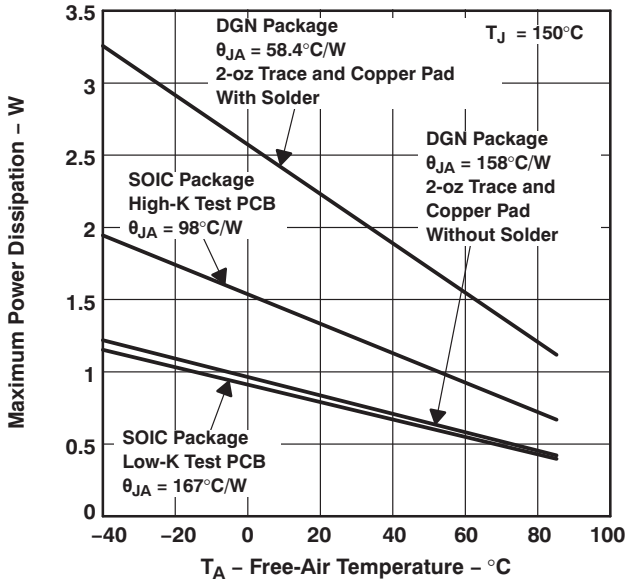
The actual thermal performance achieved with the THS401xDGN in its PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 in × 3 in, the expected thermal coefficient, θ_{JA}, is approximately 58.4°C/W. For comparison, the non-PowerPAD version of the THS401x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 35 and is calculated by the following formula:

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$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS401x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



A. Results are with no airflow and PCB size = 3 in × 3 in

Figure 35. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal-management techniques can be found in the TI technical brief, *PowerPAD™ Thermally-Enhanced Package*. This document can be found at the TI web site (www.ti.com) by searching on the keyword PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiple amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 36 to Figure 39 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. When using V_{CC} = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat-dissipation properties of the PowerPAD package. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4012), the sum of the RMS output currents and voltages should be used to choose the proper package.

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THS4011
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

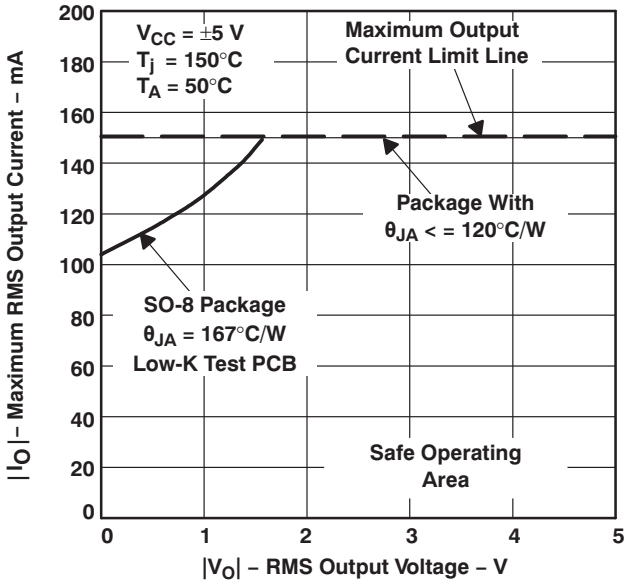


Figure 36.

THS4011
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

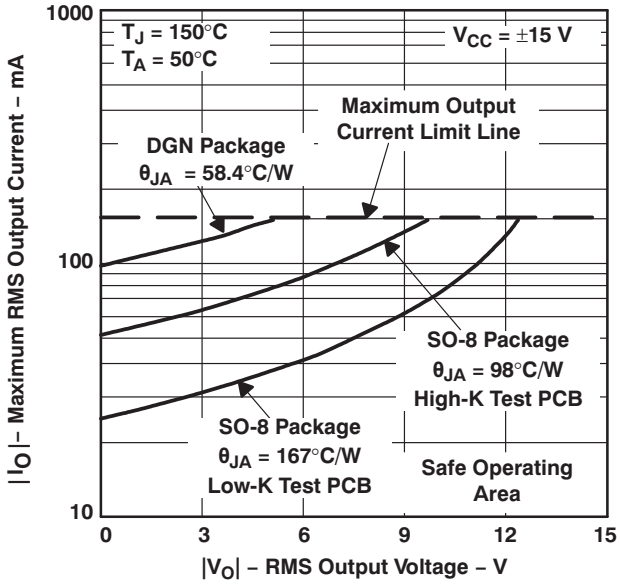


Figure 37.

THS4012
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

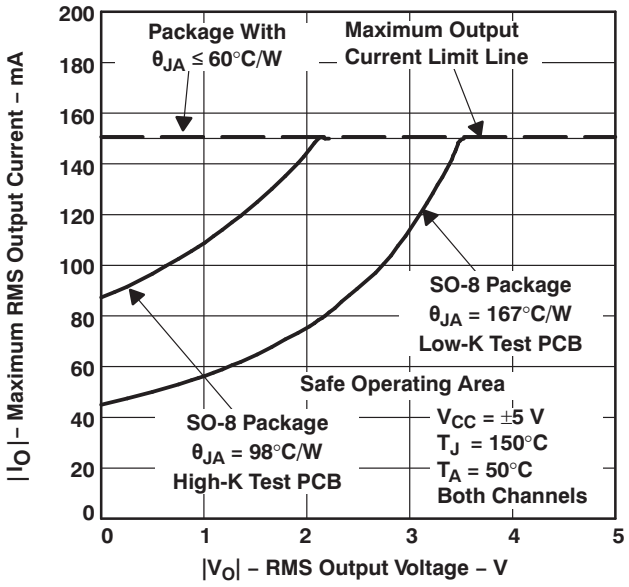


Figure 38.

THS4012
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

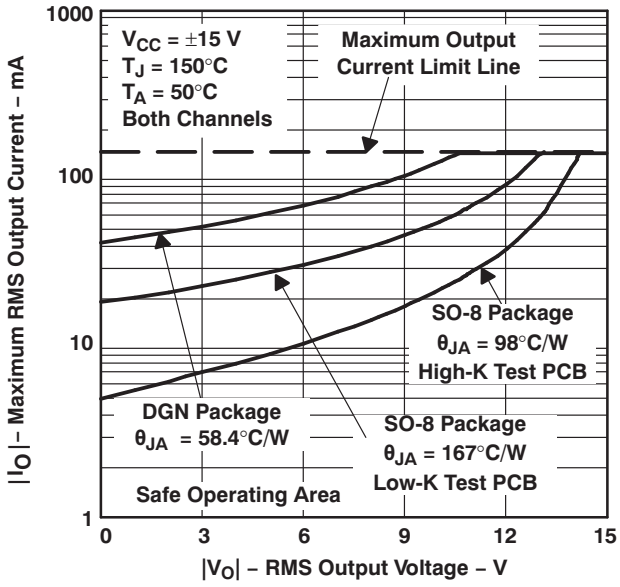


Figure 39.

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EVALUATION BOARD

An evaluation board is available for the THS4011 (literature number SLOP128) and THS4012 (literature number SLOP230). This board has been configured for low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the THS4011 evaluation board is shown in Figure 40. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, refer to the *THS4011 EVM User's Guide* (literature number SLOU028) or the *THS4012 EVM User's Guide* (literature number SLOU041) To order the evaluation board, contact your local TI sales office or distributor.

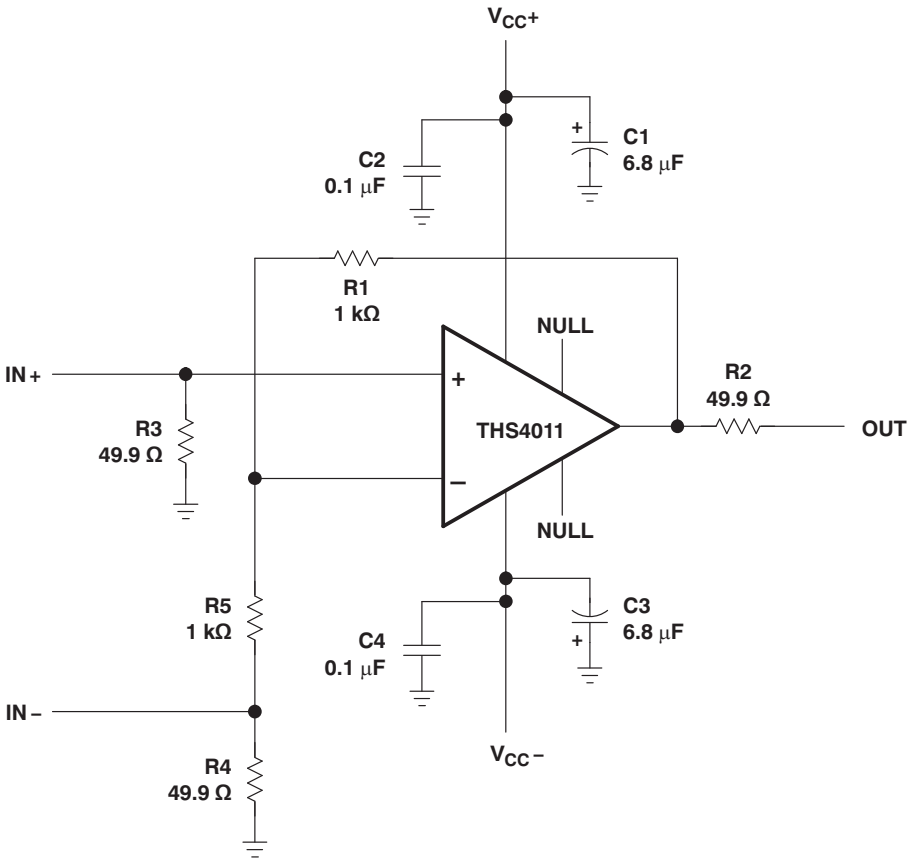


Figure 40. THS4011 Evaluation Board

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REVISION HISTORY

Changes from Original (June 1999) to Revision A — **Page**

- Changed Feature List item From: 0.006% Differential Gain Error To: 0.01% Differential Gain Error 1
- Replaced the HIGH SPEED FAMILY of DEVICES table with the RELATED DEVICES table 1
- Changed the Available Options table, THS4012ID MSOP Symbol From: TAIBG To: TIABZ 2
- Changed the ELECTRICAL CHARACTERISTIC table 5
- Changed the TYPICAL CHARACTERISTICS section 9
- Changed Figure 26, Noise Figure vs Source Resistance 14
- Changed Figure 36 through Figure 39 20
- Changed Figure 40, THS4011 Evaluation Board 21

Changes from Revision A (February 2000) to Revision B — **Page**

- Changed Feature List item From: 0.01% Differential Gain Error To: 0.006% Differential Gain Error 1
- Added THS4011M to the Abs Max table 4
- Added the ELECTRICAL CHARACTERISTICS for device number THS4011M 7

Changes from Revision B (February 2000) to Revision C — **Page**

- Changed Figure 24, THS4011/4012 Simplified Schematic 12

Changes from Revision C (May 2006) to Revision D — **Page**

- Changed Figure 29 - Output Offset Voltage Model docato-extra-info-title Output Offset Voltage Model 16

Changes from Revision D (June 2007) to Revision E — **Page**

- Deleted Lead temperature and Case temperature from the Abs Max table 4
- Changed Figure 5 label - From: Input Bias Current - A To: Input Bias Current - µA 9

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9959301Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9959301Q2A THS4011MFKB
5962-9959301QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9959301QPA THS4011M
THS4011CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4011C
THS4011CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4011C
THS4011CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ACI
THS4011CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACI
THS4011CDGNG4	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	-	Call TI	Call TI	0 to 70	
THS4011CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ACI
THS4011CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ACI
THS4011CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4011C
THS4011CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4011C
THS4011ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4011I
THS4011ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4011I
THS4011IDG4	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	-40 to 85	
THS4011IDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ACJ
THS4011IDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACJ
THS4011IDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ACJ
THS4011IDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACJ
THS4011MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9959301Q2A THS4011MFKB
THS4011MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9959301Q2A THS4011MFKB
THS4011MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	THS4011MJG
THS4011MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	THS4011MJG
THS4011MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9959301QPA THS4011M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THS4011MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9959301QPA THS4011M
THS4012CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4012C
THS4012CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4012C
THS4012CDG4	Active	Production	SOIC (D) | 8	75 | TUBE	-	Call TI	Call TI	0 to 70	
THS4012CDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ABY
THS4012CDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ABY
THS4012CDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ABY
THS4012CDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ABY
THS4012CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4012C
THS4012CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	4012C
THS4012ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4012I
THS4012ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4012I
THS4012IDGN	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABZ
THS4012IDGN.A	Active	Production	HVSSOP (DGN) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABZ
THS4012IDGNR	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABZ
THS4012IDGNR.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4011, THS4011M :

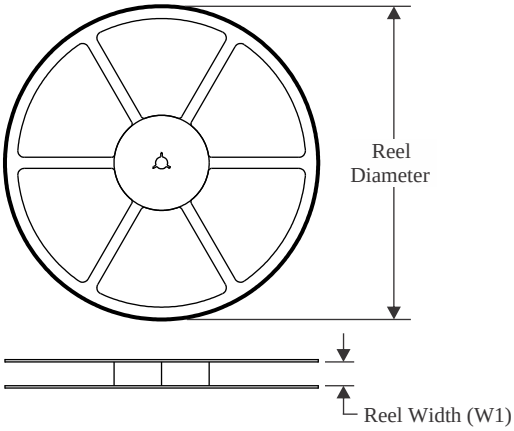
- Catalog : THS4011
- Military : THS4011M

NOTE: Qualified Version Definitions:

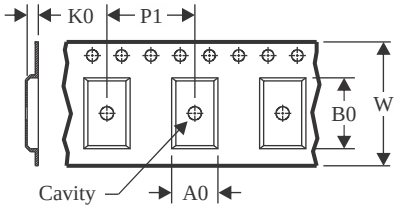
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

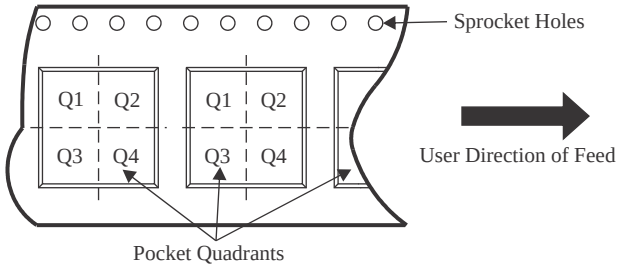


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

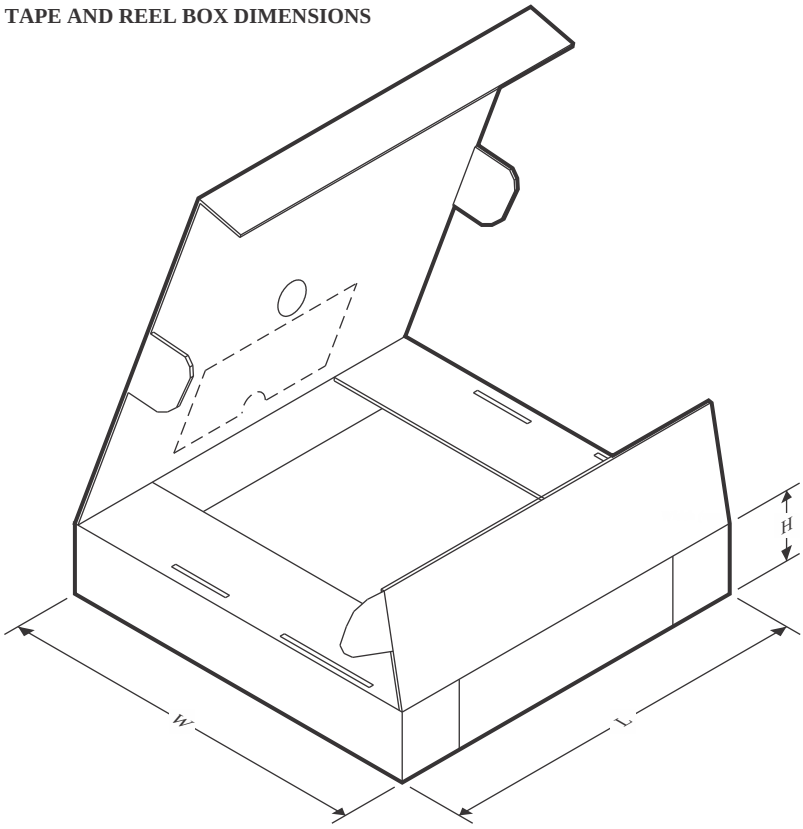
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4011CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4011CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4011CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4011IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4011IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4012CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4012CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4012IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

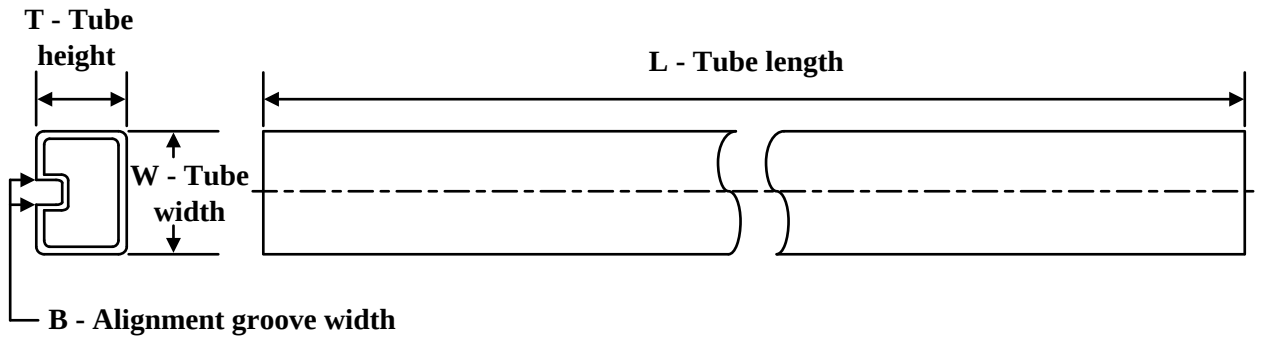
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4011CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4011CDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4011CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4011IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4011IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4012CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4012CDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4012IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0

TUBE



*All dimensions are nominal

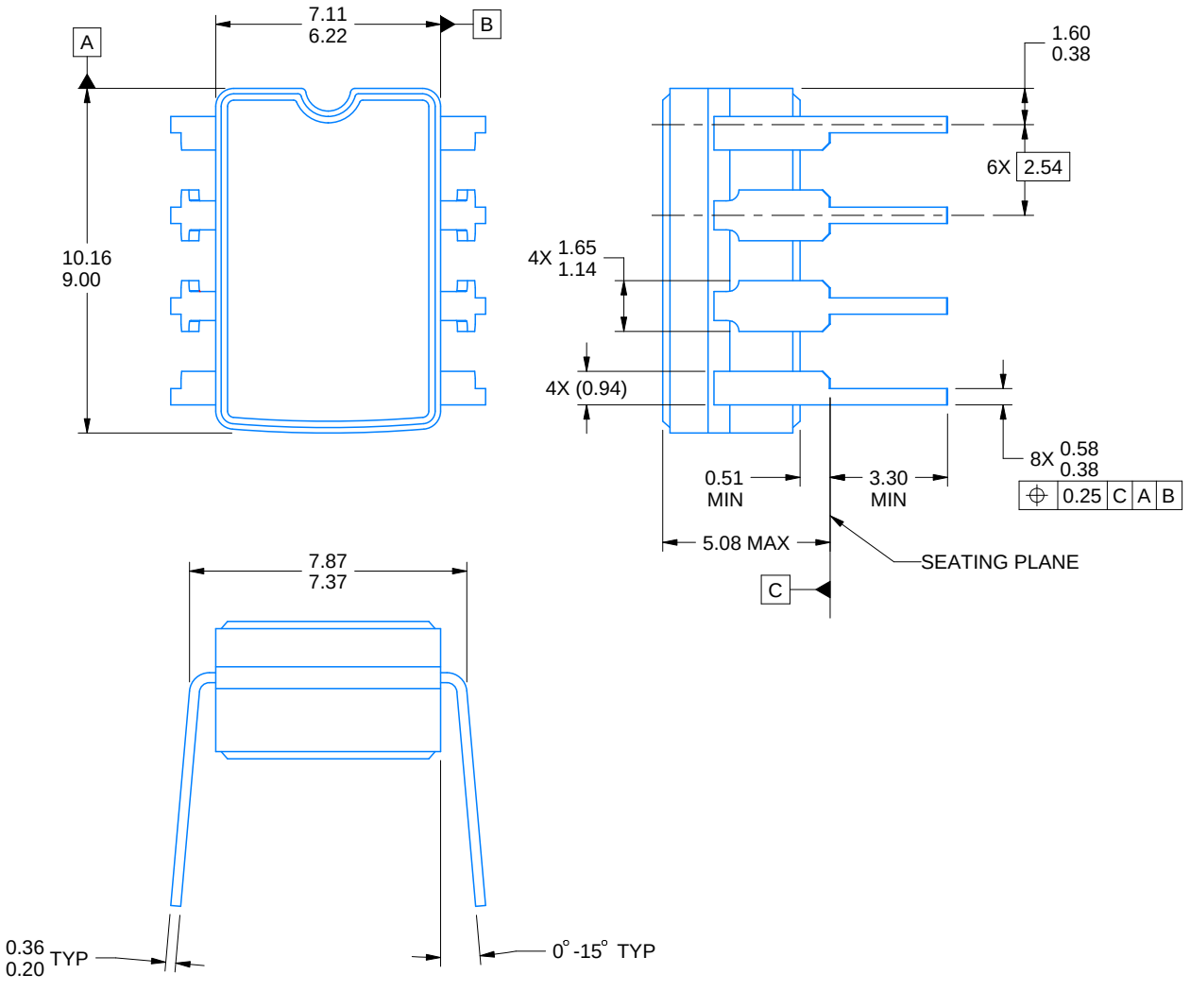
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9959301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
THS4011CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4011CD.A	D	SOIC	8	75	505.46	6.76	3810	4
THS4011CDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4011CDGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
THS4011CDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4011CDGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
THS4011ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4011ID.A	D	SOIC	8	75	505.46	6.76	3810	4
THS4011IDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4011IDGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
THS4011IDGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
THS4011IDGN.A	DGN	HVSSOP	8	80	330	6.55	500	2.88
THS4011MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
THS4011MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
THS4012CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4012CD.A	D	SOIC	8	75	505.46	6.76	3810	4
THS4012CDGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
THS4012CDGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5
THS4012ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4012ID.A	D	SOIC	8	75	505.46	6.76	3810	4
THS4012IDGN	DGN	HVSSOP	8	80	274	6.2	2540	2.5
THS4012IDGN.A	DGN	HVSSOP	8	80	274	6.2	2540	2.5

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

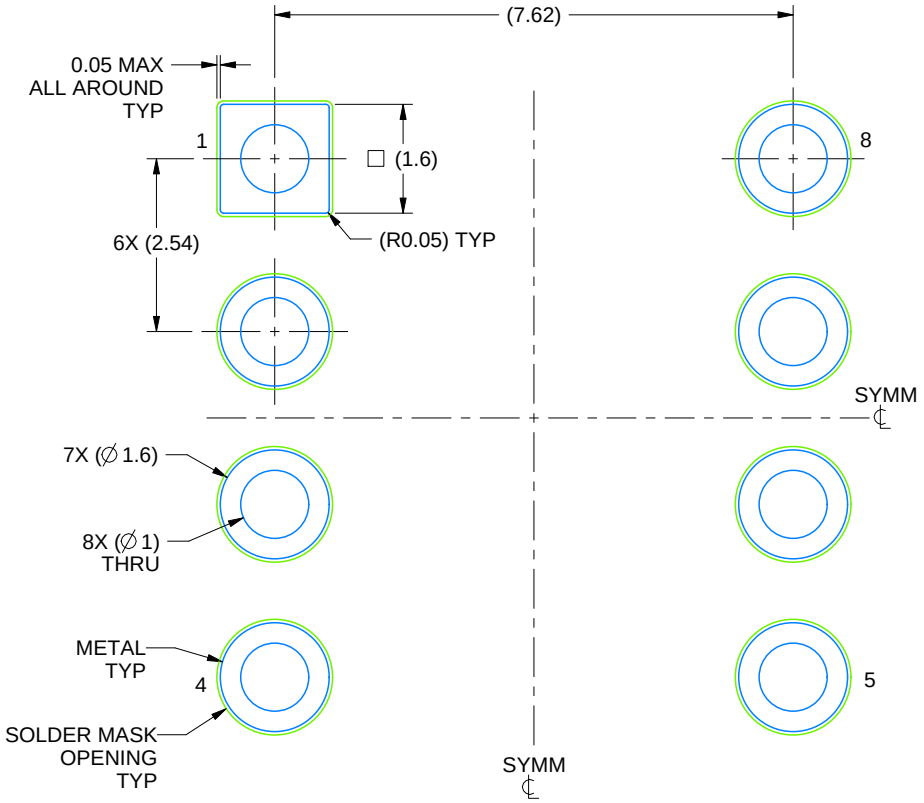
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

4230036/A 09/2023

GENERIC PACKAGE VIEW

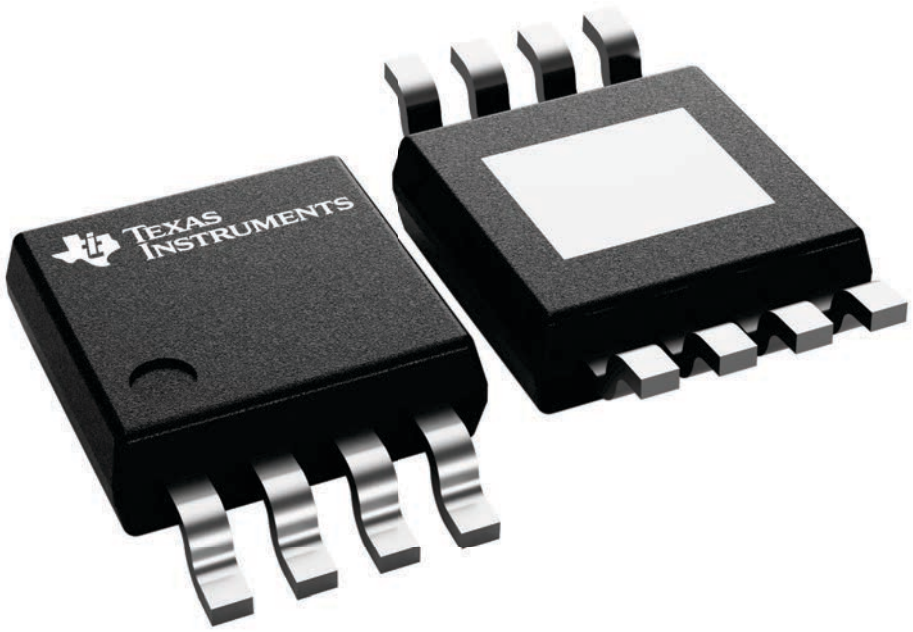
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

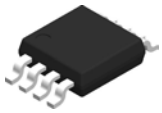
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

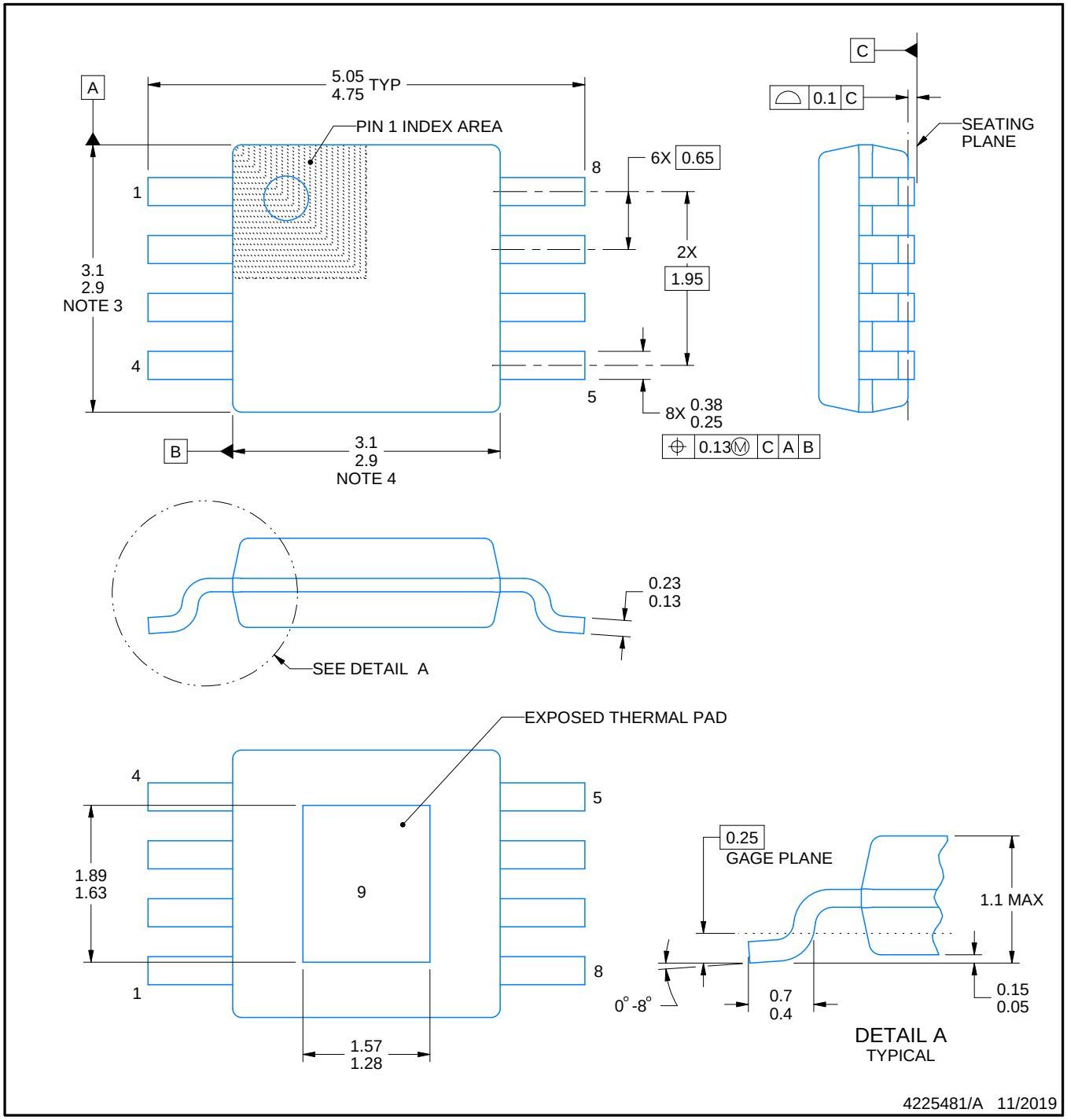
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

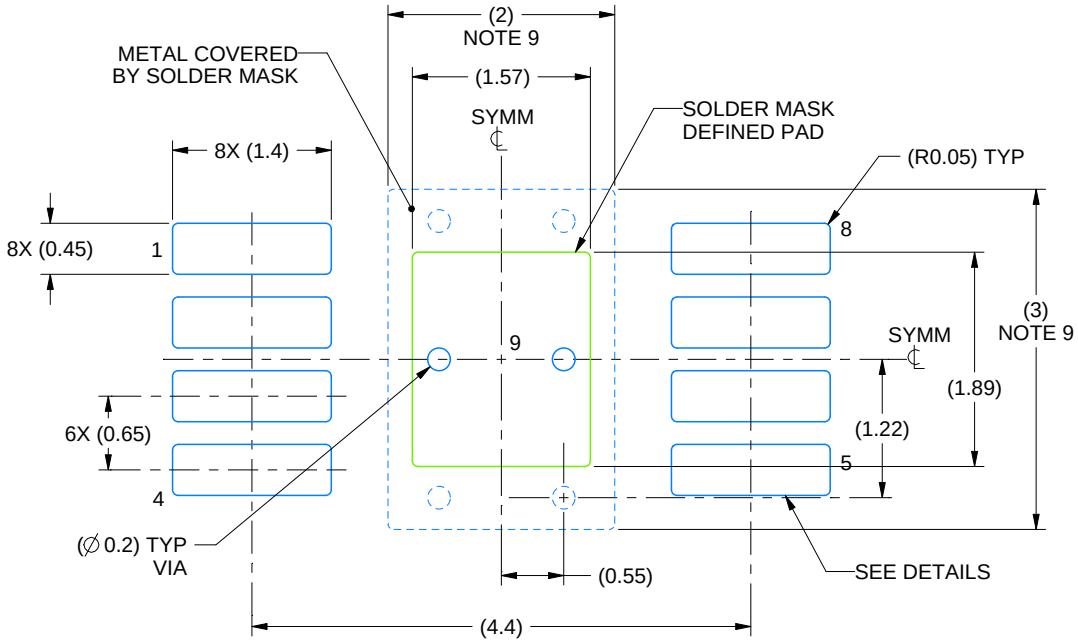
SMALL OUTLINE PACKAGE



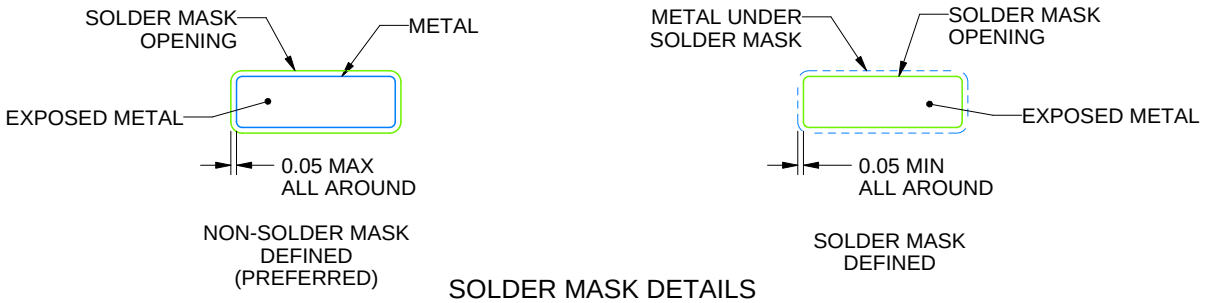
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

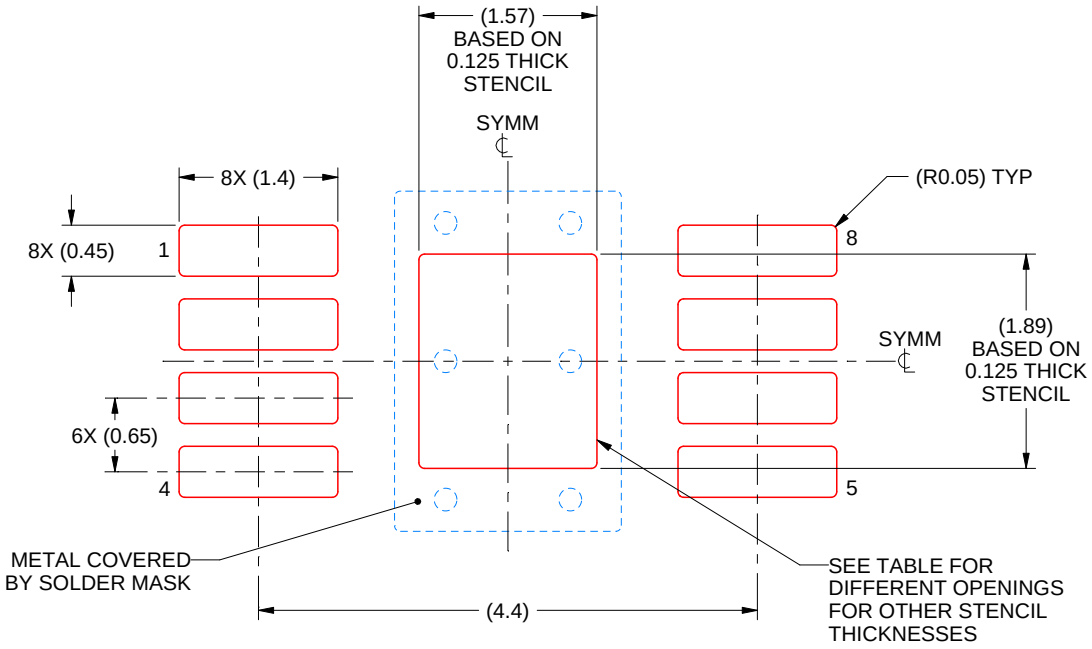


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

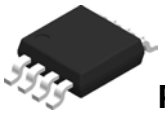
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

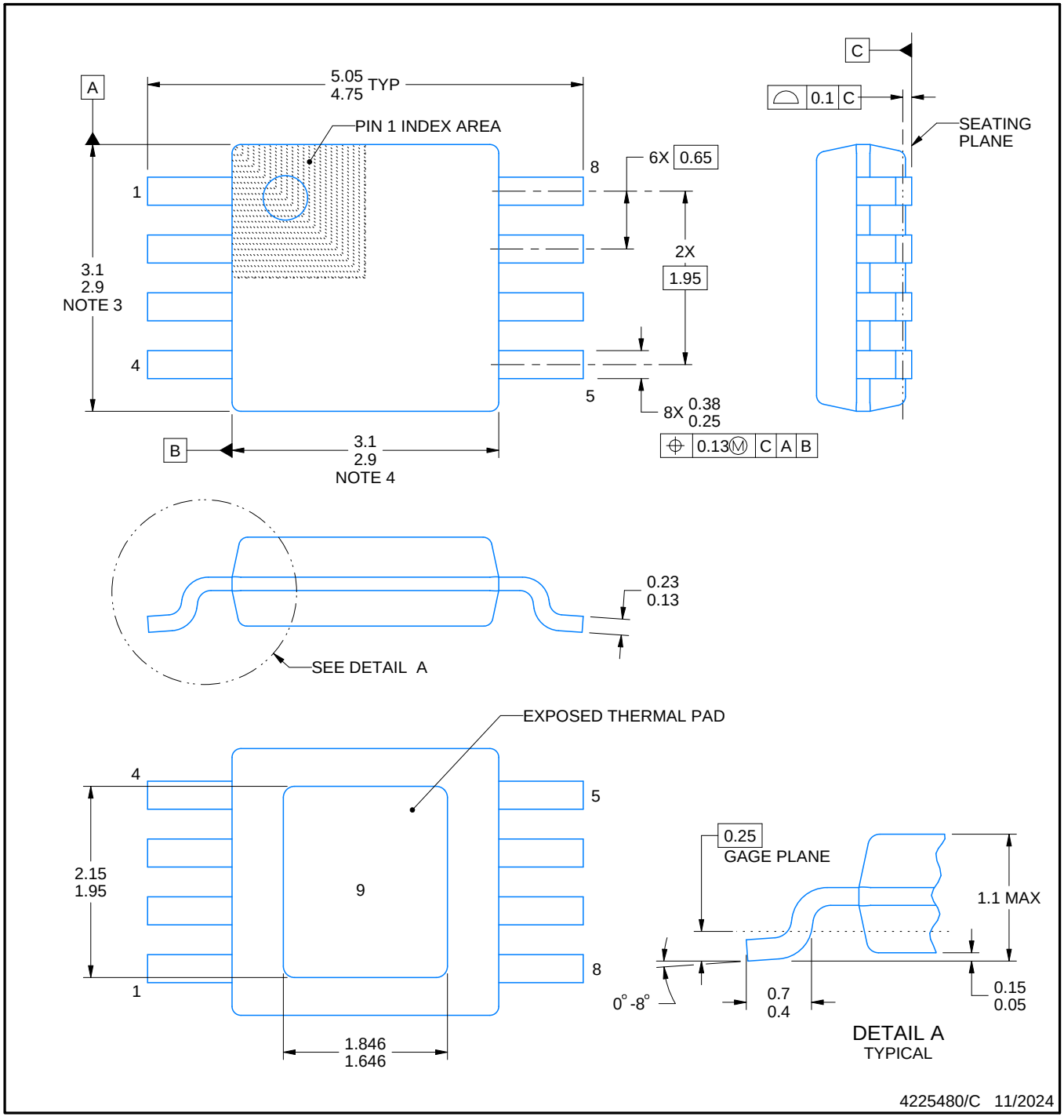
PACKAGE OUTLINE

DGN0008G



PowerPAD™ HVSSOP - 1.1 mm max height

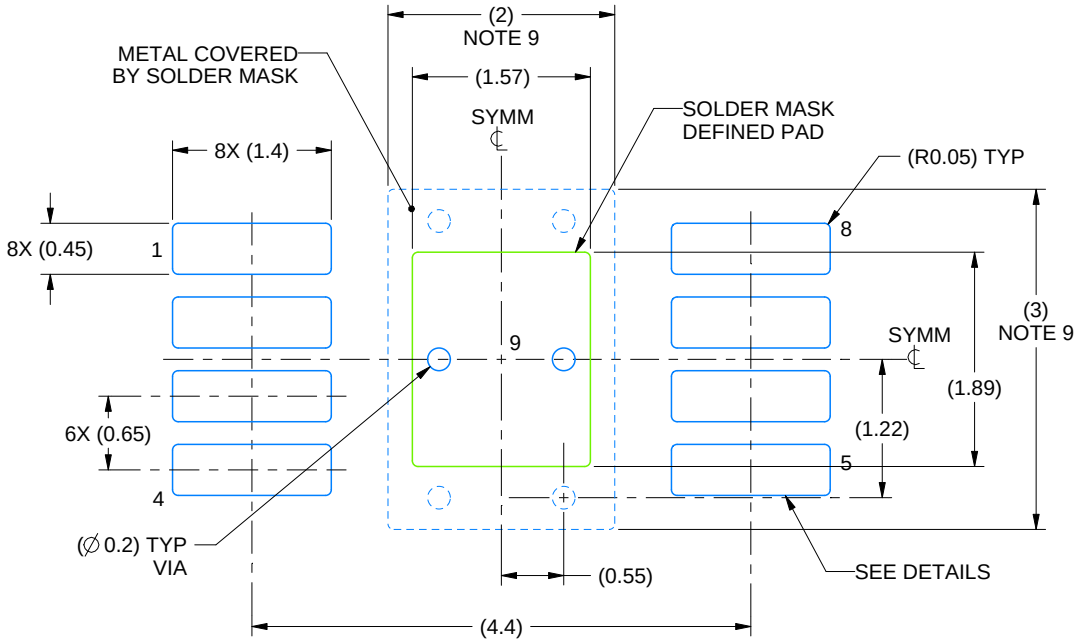
SMALL OUTLINE PACKAGE



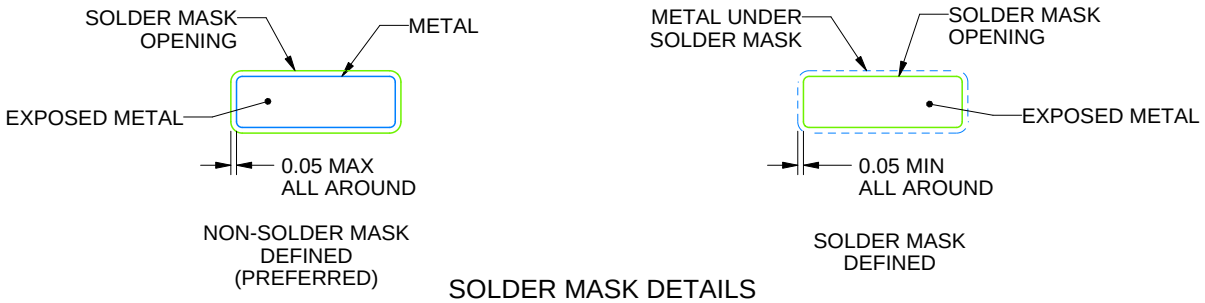
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

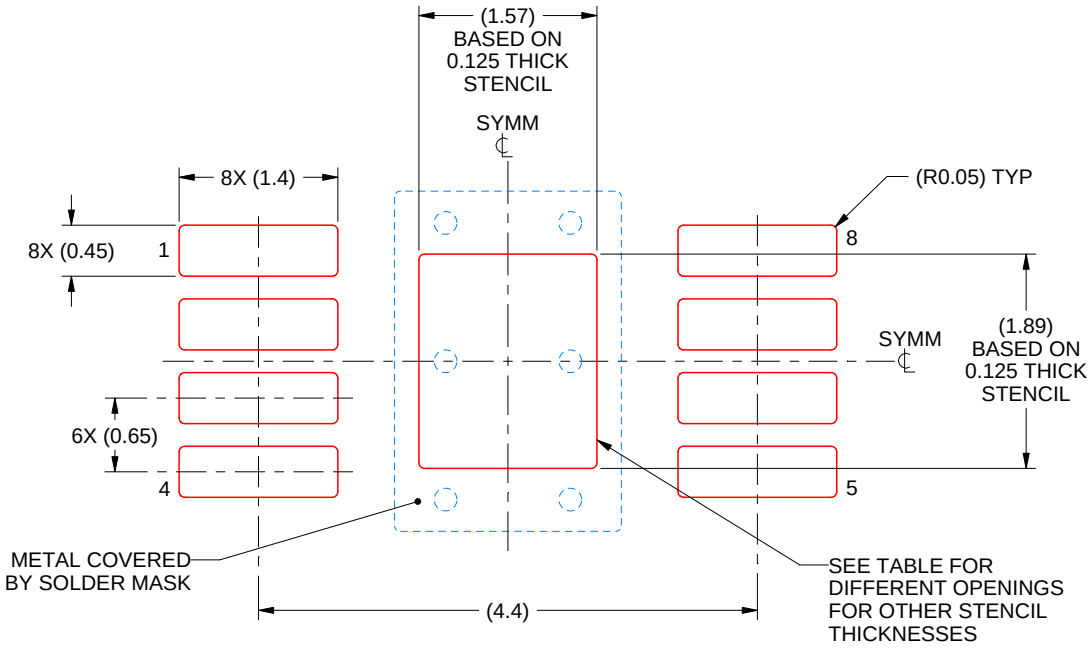


SOLDER MASK DETAILS

4225480/C 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/C 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

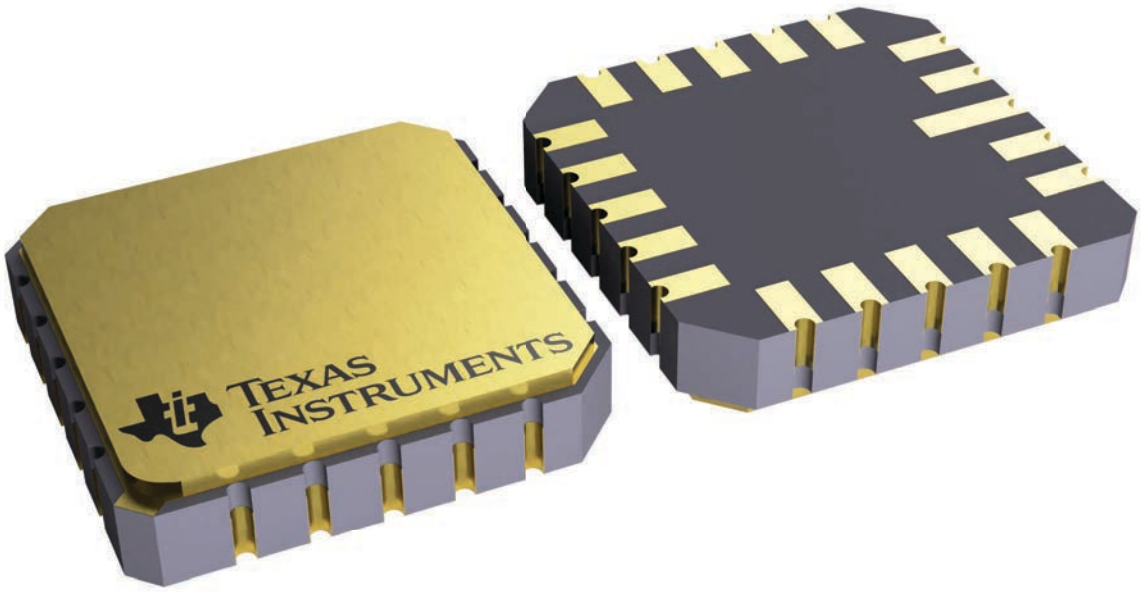
FK 20

LCCC - 2.03 mm max height

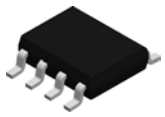
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

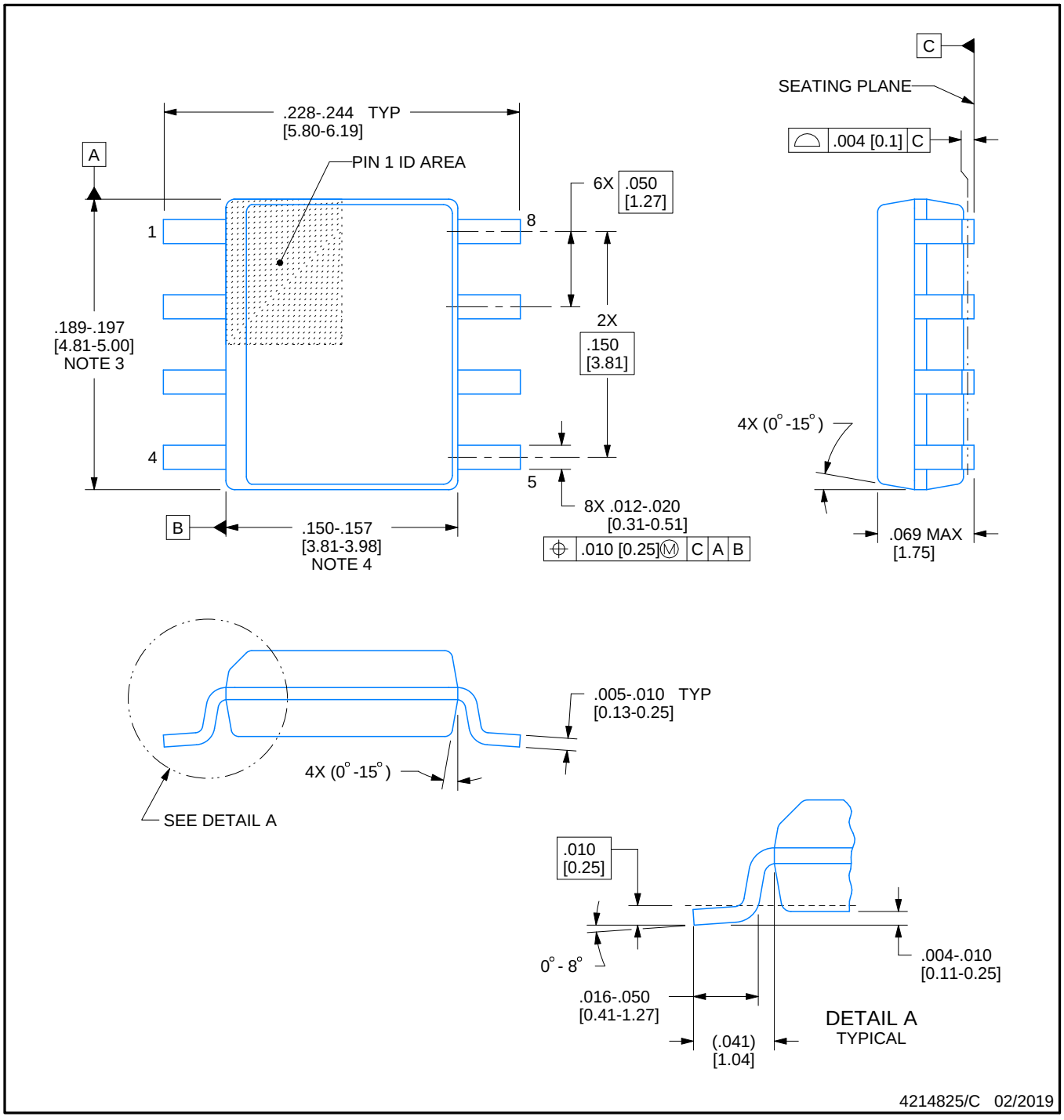


PACKAGE OUTLINE

D0008A

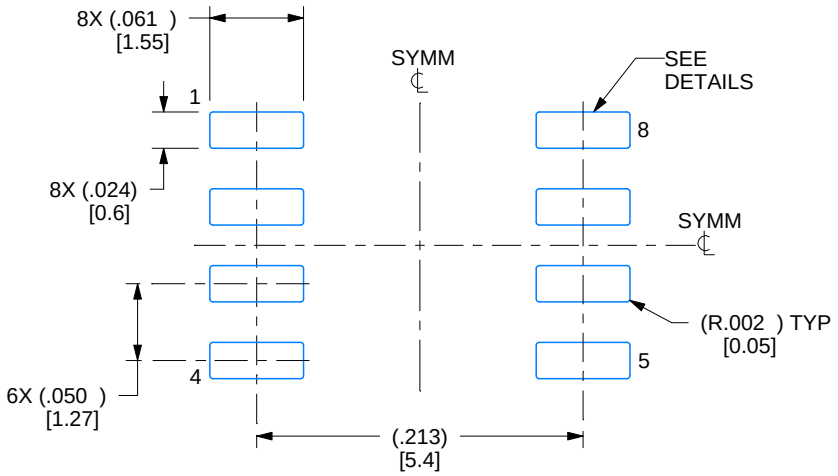
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

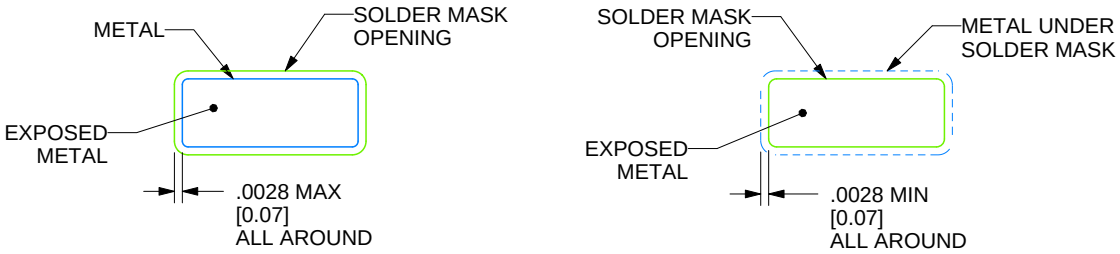


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

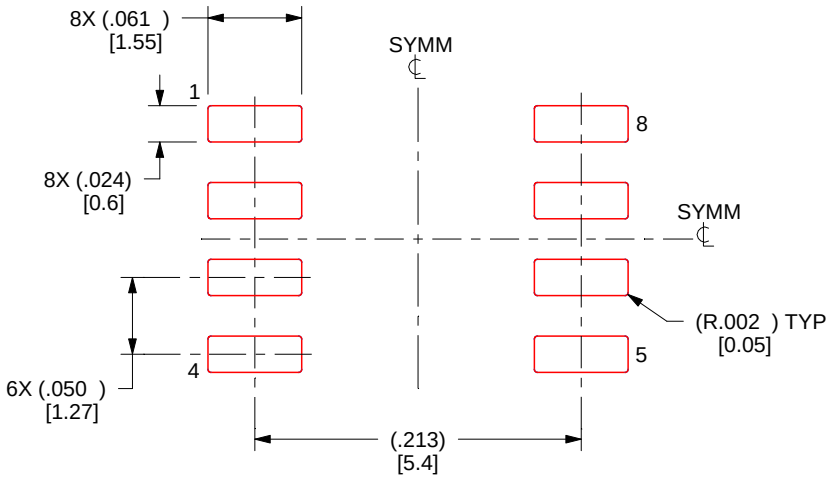
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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