THVD4411 Multiprotocol (RS-232, RS-422, RS485) Transceiver with Integrated 120Ω Switchable Termination Resistor and IEC-ESD Protection

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A and TIA/EIA-232F standards
- 1 transmitter, 1 receiver for RS-232
- 1 transmitter, 1 receiver for RS-485
- On-chip switchable 120Ω termination resistor for RS-485 mode
- Integrated charge-pump for RS-232 signaling
- 3V to 5.5V supply voltage
- 1.65V to 5.5V supply for logic data and control signals
- RS-485 differential output exceeds 2.1V for PROFIBUS compatibility with 5V supply
- Large output swing (typical ± 9V) for RS-232 mode
- SLR Pin Selectable Data Rates:
  - RS-232 3T5R mode: 250kbps and 1Mbps
  - RS-485 half-duplex and full-duplex mode: 500kbps and 20Mbps
- Bus I/O protection
  - ±16kV HBM ESD
  - ±8kV IEC 61000-4-2 contact and ±15kV air-gap discharge
  - ±4kV IEC 61000-4-4 fast transient burst
- Shutdown pin for extremely low current consumption (10µA typical) in disabled state
- Glitch-free power-up/down for hot plug-in capability
- 1/8 unit load (up to 256 bus nodes) for RS-485
- Open, short, and idle bus failsafe for RS-485 receiver
- Bus short-circuit protection, Thermal shutdown
- Extended ambient temperature range: -40°C to 125°C
- Space-saving thermally efficient 4mm x 4mm VQFN-24 package

2 Applications

- Industrial PC
- Factory automation and control
- HVAC systems
- Building automation
- Point-of-sale terminals
- Grid infrastructure
- Industrial Transport

3 Description

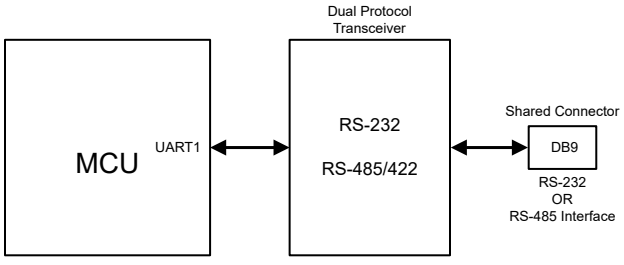
THVD4411 is a highly integrated and robust multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layers. The device has one transmitter and one receiver to enable 1T1R RS-232 port. Device also integrates one transmitter and one receiver to enable half and full duplex RS-485 port. MODE selection pins enable shared bus and logic pins for the protocols to share a common single connector. Integrated termination for RS-485 bus pins and for RS-232 receiver inputs are provided so no external components are needed to realize a fully-functional communication port. These devices have slew rate select feature that enables them to be used at two maximum speeds based on the SLR pin setting.

These devices feature integrated Level 4 IEC ESD protection, eliminating the need for external system-level protection components. In addition, the RS-485 receiver fail-safe feature drives logic high on received logic output when the bus inputs are open or shorted together or when the bus is idle. Shutdown mode consumes ultra-low current (10µA typical) in power-sensitive applications. The device needs 3V to 5.5V supply that powers the charge pump for RS-232 and the drivers and receivers for both RS-232 and RS-485. A separate logic supply V_{IO} (1.65V to 5.5V) enables interface with low level microcontrollers.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
THVD4411	VQFN (24)	4mm × 4mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



THVD4411 Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 ESD Ratings [IEC]....4
5.4 Recommended Operating Conditions....5
5.5 Thermal Information....5
5.6 Power Dissipation....6
5.7 Electrical Characteristics....7
5.8 Switching Characteristics_RS-485_500kbps....10
5.9 Switching Characteristics_RS-485_20Mbps....10
5.10 Switching Characteristics, Driver_RS232....11
5.11 Switching Characteristics, Receiver_RS232....11
5.12 Switching Characteristics_MODE switching....12
5.13 Switching Characteristics_RS-485_Termination resistor....13
5.14 Typical Characteristics....14
6 Parameter Measurement Information....17
7 Detailed Description....23
7.1 Overview....23
7.2 Functional Block Diagram....23
7.3 Feature Description....24
7.4 Device Functional Modes....27
8 Application and Implementation....32
8.1 **Application Information**....32
8.2 Typical Application....32
8.3 Power Supply Recommendations....37
8.4 Layout....37
9 Device and Documentation Support....39
9.1 Device Support....39
9.2 Receiving Notification of Documentation Updates....39
9.3 Support Resources....39
9.4 Trademarks....39
9.5 Electrostatic Discharge Caution....39
9.6 Glossary....39
10 Revision History....39
11 Mechanical, Packaging, and Orderable Information....39

Copyright © 2024 Texas Instruments Incorporated

4 Pin Configuration and Functions

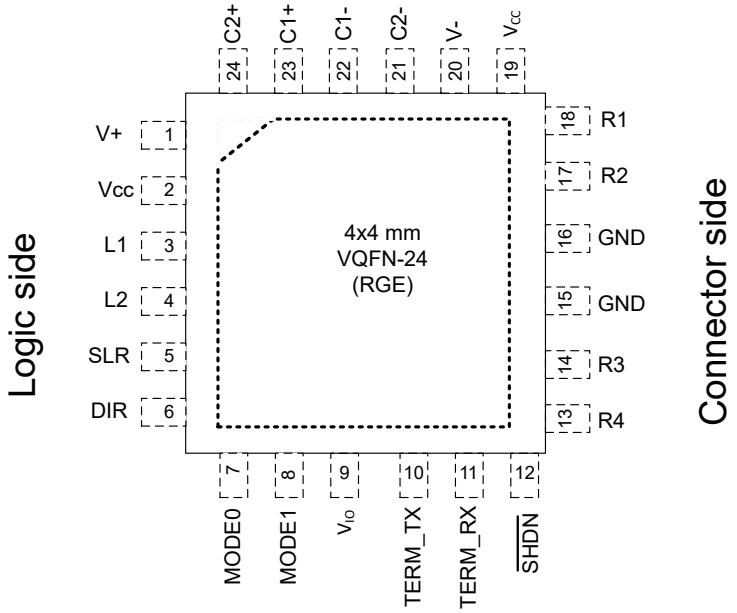


Figure 4-1. 24-Pin VQFN Package (RGE)
Top View

Table 4-1. Pin Functions

NAME	NO.	TYPE	DESCRIPTION
V+	1		Positive charge pump rail
V_{CC}	2	P	3V to 5.5V supply voltage
L1	3	O	Logic output (RS-232/RS-485)
L2	4	I	Logic input (RS-232/RS-485)
SLR	5	I	Slew rate control, internal pull-down. SLR=H enables slow speed (250kbps for RS-232, 500kbps for RS-485)
DIR	6	I	RS-485 TX/RX enable/disable. Internal pull-down
MODE0	7	I	MODE control pins
MODE1	8	I	
V_{IO}	9	P	1.65V to 5.5V logic supply voltage
TERM_TX	10	I	120Ω Termination enable/disable across R1/R2 terminals. Internal Pull down
TERM_RX	11	I	120Ω Termination enable/disable across R3/R4 terminals. Internal Pull down
$\overline{SHDN}$	12	I	Device enable/disable. Internal pull-down
R4	13	I/O	RS-485 inverting receiver input (B)
R3	14	I/O	RS-232 driver output or RS-485 non-inverting receiver input (A)
GND(1)	15, 16	G	Ground
R2	17	I/O	RS-232 receiver input or RS-485 bus pin (Y or A)
R1	18	I/O	RS-485 bus pin (Z or B)
V_{CC}	19	P	3V to 5.5V supply voltage
V-	20		Negative charge pump rail
C2-	21		Negative terminal of charge pump capacitor
C1-	22		Negative terminal of charge pump capacitor
C1+	23		Positive terminal of charge pump capacitor
C2+	24		Positive terminal of charge pump capacitor

(1) GND pins 15 and 16 must be grounded on PCB.

Copyright © 2024 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Bus supply voltage	V_{CC} to GND	–0.5	6	V
Logic supply voltage	V_{IO} to GND	–0.5	V_{CC} + 0.2	V
Charge pump positive-output supply voltage	V+ to GND	–0.3	14	V
Charge pump negative-output supply voltage	V- to GND	0.3	-14	V
Charge pump capacitor terminals	C1+ to GND	V_{CC} - 0.3	V+	V
Charge pump capacitor terminals	C2+ to GND	-0.3	V+	V
Charge pump capacitor terminals	C1- to GND	-0.3	V_{CC}	V
Charge pump capacitor terminals	C2- to GND	V-	-0.3	V
Bus voltage	Voltage at any bus pin (R1, R2, R3, R4) with respect to GND	–16	16	V
Differential bus voltage	(R1-R2) or (R2-R1), (R3-R4) or (R4-R3) with termination disbled	-22	22	V
Differential bus voltage RS485 mode	(R1-R2) or (R2-R1), (R3-R4) or (R4-R3) with termination enabled	-6	6	V
Input voltage	Range at any logic pin (L2, SLR, $\overline{SHDN}$, TERM_TX, TERM_RX, MODE0, MODE1, DIR)	–0.3	V_{IO} + 0.2	V
Receiver output current	I_O (L1)	–8	8	mA
Storage temperature	T_{stg}	–65	150	°C
Junction temperature	T_J	-40	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals (R1, R2, R3, R4) and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, Device in powered or unpowered state, In powered condition- either shutdown or RS232 or RS485 mode, on chip termination ON or OFF, loopback ON or OFF	Contact discharge, per IEC 61000-4-2	Bus terminals (R1, R2, R3, R4) and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2		±15,000	
$V_{(EFT)}$	Electrical fast transient in RS485 HD or FD mode	Per IEC 61000-4-4	Bus terminals (R1, R2, R3, R4)	±4,000	V

Copyright © 2024 Texas Instruments Incorporated

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		V_{CC}	V
$V_{I\ (RS-485)}$	Input voltage at any bus terminal (R1, R2, R3, R4) in RS-485 mode(1)		–7		12	V
V_{ID}	Differential input voltage in RS-485 mode [(R1-R2) or (R2-R1), (R3-R4) or (R4-R3)]		-12		12	V
$V_{I\ (RS-232)}$	Receiver input voltage in RS-232 mode		-15		15	V
V_{IH}	High-level input voltage (L2, SLR, $\overline{SHDN}$, TERM_TX, TERM_RX, MODE0, MODE1, DIR inputs)		0.7*V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (L2 SLR, $\overline{SHDN}$, TERM_TX, TERM_RX, MODE0, MODE1, DIR inputs)		0		0.3*V_{IO}	V
I_O	Output current, driver in RS-485 mode		–60		60	mA
I_{OR}	Output current, receiver (L1)	V_{IO} = 1.8 V or 2.5 V	–2		2	mA
I_{OR}	Output current, receiver (L1)	V_{IO} = 3.3 V or 5 V	–4		4	mA
R_L	Differential load resistance in RS-485 mode		54	60		Ω
$1/t_{UI}$	Signaling rate in RS-485 mode	SLR = V_{IO}			500	kbps
		SLR = GND or floating			20	Mbps
	Signaling rate in RS-232 mode	SLR = V_{IO}			250	kbps
		SLR = GND or floating			1	Mbps
T_A (2)	Operating ambient temperature		-40		125	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures upto 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver and receiver when the junction temperature reaches 170°C.

5.5 Thermal Information

THERMAL METRIC(1)		THVD4411 RGE (QFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

Copyright © 2024 Texas Instruments Incorporated

5.6 Power Dissipation

PARAMETER		TEST CONDITIONS			Typical	Max	UNIT
$P_{D\ (RS-485)}$	Driver outputs externally shorted to receiver inputs, MODE1, MODE0 = 11, DIR = V_{IO}, V_{IO} = V_{CC} = 5.5 V, T_A = 125 °C, L2 = square wave 50% duty	Unterminated, TERM_TX = L, TERM_RX = L	SLR = H	500 kbps	160	200	mW
			SLR = L	20Mbps	310	410	
		TERM_TX = TERM_RX = V_{IO}	SLR = H	500 kbps	430	500	mW
			SLR = L	20Mbps	485	575	
$P_{D\ (RS-232)}$	RS-232 mode with MODE1, MODE0 = 01	V_{CC} = V_{IO} = 5.5V, R3 bus line loaded with 3 kΩ, R3 load cap = 1000 pF, L2 toggling	SLR = L	1 Mbps	300	480	mW
		V_{CC} = V_{IO} = 5.5V, R3 bus line loaded with 3 kΩ, R3 load cap = 2500 pF, L2 toggling	SLR = H	250 kbps	170	200	mW

Copyright © 2024 Texas Instruments Incorporated

5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Driver_RS-485								
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V (See Figure 6-1)			1.5	2		V
		R_L = 60 Ω, –7 V ≤ V_{test} ≤ 12 V, 4.5 V ≤ V_{CC} ≤ 5.5 V (See Figure 6-1)			2.1	3		V
		R_L = 100 Ω (See Figure 6-2)			2	2.5		V
		R_L = 54 Ω, 4.5 V ≤ V_{CC} ≤ 5.5 V (See Figure 6-2)			2.1	3.3		V
		R_L = 54 Ω (See Figure 6-2)			1.5	3.3		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage	R_L = 54 Ω or 100 Ω (See Figure 6-2)			–50		50	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 6-2)				V_{CC}/2	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54 Ω or 100 Ω (See Figure 6-2)			–50		50	mV
I_{OS}	Short-circuit output current (bus terminals)	DIR = V_{IO}, -7 V ≤ (V_{R2} or V_{R1}) ≤ 12 V, or R1 shorted to R2			–250		250	mA
I_{OZD}	Driver High impedance output leakage current on R1 and R2 in Full duplex mode	MODE1, MODE0 = 11 , TERM_TX = GND, DIR = GND, V_{CC} = GND or 5.5V, V_O = -7V, +12V			-125		125	µA
		MODE1, MODE0 = 11, TERM_TX = V_{IO}, DIR = GND, V_{CC} = 5.5V, V_O = -7V, +12V			- 325		350	µA
Receiver_RS-485								
I_I	Bus input current (termination disabled)	Half and full duplex modes, DIR = 0 V, V_{CC} and V_{IO} = 0 V or 5.5 V	V_I = 12 V			75	125	µA
			V_I = –7 V		–125	–70		µA
I_{RXT}	Receiver bus input leakage current with termination enabled	Full duplex mode, V_{CC} and V_{IO} = 5.5 V, TERM_RX = V_{IO}	VI = - 7 to 12 V		-325		325	µA
V_{TH+}	Positive-going input threshold voltage(1)	Over common-mode range of - 7 V to 12 V				- 70	- 40	mV
V_{TH-}	Negative-going input threshold voltage(1)				–200	–150		mV
V_{HYS}	Input hysteresis				25	80		mV
$C_{A,B}$	Input differential capacitance	Measured between R3 and R4, f = 1 MHz				20		pF
V_{OH}	Output high voltage, L1 pin	I_{OH} = –4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V			V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage, L1 pin	I_{OL} = 4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V				0.2	0.4	V
V_{OH}	Output high voltage, L1 pin	I_{OH} = –2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V			V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage, L1 pin	I_{OL} = 2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V				0.2	0.4	V
I_{OZ}	Output high-impedance current, L1 pin	V_O = 0 V or V_{IO}, DIR = V_{IO}, MODE1, MODE0= 10 (half duplex mode)			–2		2	µA
Driver_RS-232								
V_{OH}	High-level output voltage	DOUT (R3) at R_L = 3 kΩ to GND, DIN (L2) = GND; V_{CC} = 3 V to 3.6 V			5	5.5	7	V
V_{OL}	Low-level output voltage	DOUT (R3) at R_L = 3 kΩ to GND, DIN (L2) = V_{IO} ; V_{CC} = 3 V to 3.6 V			–7.3	–5.5	-5	V
V_{OH}	High-level output voltage	DOUT (R3) at R_L = 3 kΩ to GND, DIN (L2) = GND; V_{CC} = 4.5 V to 5.5 V			7.8	9	11	V
V_{OL}	Low-level output voltage	DOUT (R3) at R_L = 3 kΩ to GND, DIN (L2) = V_{IO} ; V_{CC} = 4.5 V to 5.5 V			–11.3	–9	-7.8	V
I_{OS}	Short-circuit output current (2)	V_{CC} = 3.6 V	V_O = 0 V			±35	±60	mA
		V_{CC} = 5.5 V	V_O = 0 V					
r_o	Output resistance on R3	V_{CC} = 0 V, V_+ = 0 V, and V_- = 0 V	V_O = ±2 V		300	10M		Ω
I_{off}	Output leakage current on R3	$\overline{SHDN}$ = GND	V_O = ±12 V	V_{CC} = 3 to 3.6 V			±125	µA
			V_O = ±10 V	V_{CC} = 4.5 to 5.5 V			±125	µA
Receiver_RS-232								

Copyright © 2024 Texas Instruments Incorporated

5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage L1	I_{OH} = –4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V		V_{IO} – 0.5	V_{IO} – 0.2		V
		I_{OH} = –2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V		V_{IO} – 0.46	V_{IO} – 0.2		V
V_{OL}	Low-level output voltage L1	I_{OL} = 4 mA, V_{IO} = 3 to 3.6 V or 4.5 V to 5.5 V				0.4	V
		I_{OL} = 2 mA, V_{IO} = 1.65 to 1.95 V or 2.25 V to 2.75 V				0.4	V
V_{IT+}	Positive-going input threshold voltage on RS-232 receiver inputs (R2)	V_{CC} = 3.3 V			1.6	2.4	V
		V_{CC} = 5 V			1.9	2.4	V
$V_{IT–}$	Negative-going input threshold voltage on RS-232 receiver inputs (R2)	V_{CC} = 3.3 V		0.6	1.1		V
		V_{CC} = 5 V		0.8	1.4		V
V_{hys}	Input hysteresis on receiver inputs (V_{IT+} – $V_{IT–}$)			0.4	0.5		V
I_{off}	Output leakage current on receiver output pins L1	$\overline{SHDN}$ = 0 V			±0.05	±10	µA
r_I	Input resistance on receiver input pins	-15 V ≤ V_I ≤ 15 V		3	5	7	kΩ
Thermal Protection							
T_{SHDN}	Thermal shutdown threshold	Temperature rising		150	170		°C
T_{HYS}	Thermal shutdown hysteresis				15		°C
Supply							
$UV_{VCC (rising)}$	Rising under-voltage threshold on V_{CC}				2.5	2.7	V
$UV_{VCC (falling)}$	Falling under-voltage threshold on V_{CC}			1.9	2.1		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}			100	400		mV
$UV_{VIO (rising)}$	Rising under-voltage threshold on V_{IO}				1.5	1.6	V
$UV_{VIO (falling)}$	Falling under-voltage threshold on V_{IO}			1.2	1.4		V
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}			85	100		mV
I_{CC_SHDN}	Supply current in shutdown mode	V_{CC} = 4.5 V to 5.5 V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, T_A ≤ 125 °C			5	20	µA
		V_{CC} = 3 V to 3.6 V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, T_A ≤ 125 °C			3	15	µA
		V_{CC} = 4.5 V to 5.5 V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, T_A ≤ 105 °C			5	15	µA
		V_{CC} = 3 V to 3.6 V, $\overline{SHDN}$ = GND, All other logic input pins floating, no load on bus, T_A ≤ 105 °C			3	10	µA
I_{IO_SHDN}	Logic supply current in shutdown mode	V_{IO} = 1.65 V to 5.5 V, $\overline{SHDN}$ = GND, All other logic input pins floating				2	µA
I_{CC_485}	Supply current (quiescent), V_{CC} = 4.5 V to 5.5 V TERM_RX, TERM_TX= Floating or low, SLR = X	Driver and receiver enabled, DIR = V_{IO}, MODE1, MODE0 = 11 (Full duplex)	No load		1.7	3.4	mA
		Driver enabled, receiver disabled, DIR = V_{IO}, MODE1, MODE0 = 10 (Half duplex)	No load		1.3	2.8	mA
		Driver disabled, receiver enabled, DIR = GND, MODE1, MODE0 = 10 (Half duplex)	No load		0.8	1.5	mA
I_{CC_485}	Supply current (quiescent), V_{CC} = 3 V to 3.6 V TERM_RX, TERM_TX= Floating or low, SLR = X	Driver and receiver enabled, DIR = V_{IO}, MODE1, MODE0 = 11 (Full duplex)	No load		1.5	2.8	mA
		Driver enabled, receiver disabled, DIR = V_{IO}, MODE1, MODE0 = 10 (Half duplex)	No load		1	2.3	mA
		Driver disabled, receiver enabled, DIR = GND, MODE1, MODE0 = 10 (Half duplex)	No load		0.7	1.3	mA

Copyright © 2024 Texas Instruments Incorporated

5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{IO_485}	Logic supply current (quiescent), V_{IO} = 3 to 3.6 V TERM_RX, TERM_TX= Floating	Driver disabled, Receiver enabled, SLR = GND, DIR = GND; MODE1, MODE0 = 10 (half duplex)	No load		7	17	µA
		Driver disabled, Receiver enabled, SLR = V_{IO}; DIR = GND; MODE1, MODE0 = 10 (half duplex)	No load		8	21	µA
I_{CCDT_485}	Supply current in RS-485 driver termination mode	Driver enabled with termination ON; MODE1, MODE0 = 11 (full duplex)	DIR= V_{IO}, TERM_TX = V_{IO}		38	50	mA
I_{CCRT_485}	Supply current in RS-485 receiver termination mode	Receiver enabled with termination ON; MODE1, MODE0 = 11 (full duplex)	DIR = GND, TERM_RX = V_{IO}		1	1.5	mA
I_{CC_RS232}	Supply current in RS-232 mode	MODE1, MODE0 = 01, $\overline{SHDN}$ = V_{IO}; other logic inputs floating	No load		2.5	3.8	mA
On-Chip termination resistor_RS-485							
R_{TERM_TX}	120 Ω termination across Driver output R1/R2 terminals	MODE1, MODE0 = 11 (Full duplex) or 10 (half duplex); DIR = GND, TERM_TX = V_{IO}, V_{R2R1} = 2 V, V_{R1} = -7 V, 0 V, 10 V; See Figure 6-9		102	120	138	Ω
R_{TERM_RX}	120 Ω termination across receiver output R3/R4 terminals	MODE1, MODE0 = 11 (Full duplex); TERM_RX = V_{IO}, V_{R3R4} = 2 V, V_{R4} = -7 V, 0 V, 10 V; See Figure 6-9		102	120	138	Ω
Logic							
I_{IN}	Input current (L2, DIR, $\overline{SHDN}$, SLR, TERM_TX, TERM_RX, MODE1, MODE0)	1.65 V ≤ V_{IO} ≤ 5.5 V, 0 V ≤ V_{IN} ≤ V_{IO}		-20		5	µA
$V_{IT+(IN)}$	Rising threshold: logic inputs	1.65 V ≤ V_{IO} ≤ 5.5 V			0.6*V_{IO}	0.7*V_{IO}	V
$V_{IT-(IN)}$	Falling threshold: logic inputs			0.3*V_{IO}	0.4*V_{IO}		V
$V_{IN(HYS)}$	Input threshold: logic inputs			0.1*V_{IO}	0.2*V_{IO}		V

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-}.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Copyright © 2024 Texas Instruments Incorporated

5.8 Switching Characteristics_RS-485_500kbps

500-kbps (with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V , V_{IO} = 3.3 V, unless otherwise noted. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See Figure 6-3	V_{CC} = 3 to 3.6 V, Typical at 3.3V	210	300	600	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	250	300	600	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{CC} = 3 to 3.6 V, Typical at 3.3V		250	450	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		250	450	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		V_{CC} = 3 to 3.6 V, Typical at 3.3V		2	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		2	15	ns
t_{PHZ}, t_{PLZ}	Disable time	MODE1, MODE0 = 10 (half duplex) or 11 (full duplex)	See Figure 6-4 and Figure 6-5		80	150	ns
t_{PZH}, t_{PZL}	Enable time	MODE1, MODE0 = 11 (full duplex): receiver enabled			200	650	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See Figure 6-6		13	20	ns
t_{PHL}, t_{PLH}	Propagation delay				700	1200	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				10	50	ns
t_{PHZ}, t_{PLZ}	Disable time in half duplex mode	MODE1, MODE0 = 10, TERM_TX = V_{IO}	See Figure 6-7		30	80	ns
$t_{PZH(1)}$	Enable time in half duplex mode				60	155	ns
$t_{PZL(1)}$					450	1250	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time from shutdown with TX disabled in full duplex mode	DIR = 0 V; MODE1, MODE0 = 11	See Figure 6-8		7	16	µs

(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode

5.9 Switching Characteristics_RS-485_20Mbps

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF See Figure 6-3	V_{CC} = 3 to 3.6 V, Typical at 3.3 V	5	10	15	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V	5	10	15	ns
t_{PHL}, t_{PLH}	Propagation delay		V_{IO} = 1.65 V to 1.95V	14	25	58	ns
			V_{IO} = 3 V to 3.6 V	9	20	46	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$		V_{CC} = 3 to 3.6 V, Typical at 3.3 V		1	3.5	ns
			V_{CC} = 4.5 to 5.5 V, Typical at 5 V		1	3.5	ns
t_{PHZ}, t_{PLZ}	Disable time	MODE1, MODE0 = 10 (half duplex) or 11 (full duplex)	See Figure 6-4 and Figure 6-5		11	65	ns
t_{PZH}, t_{PZL}	Enable time	MODE1, MODE0 = 11 (full duplex): receiver enabled			8	80	ns
Receiver							
t_r, t_f	Output rise/fall time	C_L = 15 pF	See Figure 6-6		5	10	ns
t_{PHL}, t_{PLH}	Propagation delay				40	70	ns
$t_{SK(P)}$	Pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					10	ns

Copyright © 2024 Texas Instruments Incorporated

5.9 Switching Characteristics_RS-485_20Mbps (continued)

20-Mbps (SLR = GND) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V, V_{IO} = 3.3 V. (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHZ}, t_{PLZ}	Disable time in half duplex mode	MODE1, MODE0 = 10, TERM_TX = V_{IO}	See Figure 6-7		20	80	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time in half duplex mode				50	160	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time from shutdown with TX disabled in full duplex mode	DIR = 0 V; MODE1, MODE0 = 11	See Figure 6-8		4	15	µs

(1) A, B are RX input, Y/Z are driver output terminals in Full duplex mode.

5.10 Switching Characteristics, Driver_RS232

over recommended ranges of supply voltage and operating free-air temperature(unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP(2)	MAX	UNIT
250 kbps							
	Maximum data rate	R_L = 3 kΩ One DOUT switching	C_L = 2500 pF See Figure 6-14	250	500		kbps
t_{PHL}, t_{PHL}	Transmitter propagation delay	R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 2500 pF See Figure 6-14		0.8	2	µs
$t_{sk(p)}$	Transmitter Pulse skew(3)				100	600	ns
SR(tr)	Slew rate, transition region	V_{CC} = 3.3 V ± 10%, 5 V ± 10% , R_L = 3 kΩ to 7 kΩ, See Figure 6-15	C_L = 150 pF to 1000 pF	6		30	V/µs
			C_L = 150 pF to 2500 pF	4		30	
1 Mbps							
	Maximum data rate	R_L = 3 kΩ One DOUT switching, See Figure 6-14	C_L = 250 pF, V_{CC} = 3 to 3.6 V	1000			kbps
			C_L = 1000 pF, V_{CC} = 4.5 to 5.5 V	1000			kbps
t_{PLH}, t_{PHL}	Transmitter propagation delay	R_L = 3k to 7 kΩ, See Figure 6-14	C_L = 150 pF to 1000 pF		300	800	ns
$t_{sk(p)}$	Pulse skew(3)				25	150	ns
SR(tr)	Slew rate, transition region	R_L = 3k to 7 kΩ, VCC = 4.5 V to 5.5 V	C_L = 150 pF to 1000 pF; See Figure 6-15	18		150	V/µs
		R_L = 3k to 7 kΩ, VCC = 3 V to 3.6 V		15		150	V/µs

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V + 0.3 V; V_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as$|t_{PLH} - t_{PHL}|$ of each channel of the samedevice.

5.11 Switching Characteristics, Receiver_RS232

over recommended ranges of supply voltage and operating free-air temperature (unlessotherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
250 kbps						
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 6-16		150	550	ns
t_{PHL}	Propagation delay time, high- to low-level output			150	550	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF, See Figure 6-16		130	520	ns
t_{PHL}	Propagation delay time, high- to low-level output			130	520	ns
t_{R_232}, t_{F_232}	Rise/fall time (receiver buffer output), V_{IO} = 3 to 5.5 V	C_L = 150 pF, See Figure 6-16		20	50	ns
		C_L = 15 pF, See Figure 6-16		5	10	ns
	Rise/fall time (receiver buffer output), V_{IO} = 1.65 to 2.75 V	C_L = 150 pF, See Figure 6-16		40	90	ns
		C_L = 15 pF, See Figure 6-16		10	20	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 6-17		6	14	us
t_{dis}	Output disable time			100	200	ns
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF, See Figure 6-16		50	135	ns
		C_L = 15 pF, See Figure 6-16		50	135	ns

Copyright © 2024 Texas Instruments Incorporated

5.11 Switching Characteristics, Receiver_RS232 (continued)

over recommended ranges of supply voltage and operating free-air temperature (unlessotherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
1 Mbps						
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 6-16		150	550	ns
t_{PHL}	Propagation delay time, high- to low-level output			150	550	ns
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 15 pF, See Figure 6-16		130	520	ns
t_{PHL}	Propagation delay time, high- to low-level output			130	520	ns
t_{R_232}, t_{F_232}	Rise/fall time (receiver buffer output), V_{IO} = 3 to 5.5 V	C_L = 150 pF, See Figure 6-16		20	50	ns
		C_L = 15 pF, See Figure 6-16		5	10	ns
	Rise/fall time (receiver buffer output), V_{IO} = 1.65 to 2.75 V	C_L = 150 pF, See Figure 6-16		40	90	ns
		C_L = 15 pF, See Figure 6-16		10	20	ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 6-17		6	14	us
t_{dis}	Output disable time			100	200	ns
$t_{sk(p)}$	Pulse skew(3)	C_L = 150 pF, See Figure 6-16		50	125	ns
		C_L = 15 pF, See Figure 6-16		50	125	ns

(1) Test conditions are C1–C4 = 0.1 µF atV_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF atV_{CC} = 5 V ± 0.5 V.
(2) All typical values are at V_{CC} = 3.3 V orV_{CC} = 5 V, and T_A = 25°C.
(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

5.12 Switching Characteristics_MODE switching

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V , V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RDY}	Time from Shutdown to RS-232 ready	MODE1, MODE0 = 00 or floating; $\overline{SHDN}$ = GND to V_{IO}; rest of logic input pins floating, V_{CC} = 4.5 V to 5.5 V Time from 50% of rising SHDN to charge pump V-supply reaching -8 V; See Figure 6-11		0.05	0.1	ms
		MODE1, MODE0 = 00 or floating; SHDN = GND to V_{IO}; rest of logic input pins floating, V_{CC} = 3 V to 3.6 V Time from 50% of rising SHDN to charge pump V-supply reaching -5 V; See Figure 6-11		0.1	0.4	ms
t_{R2_R4}	Time to switch from RS-232 1T1R mode to RS-485 Full duplex mode	L2 = Vio, MODE1 from GND to Vio, MODE0 = Vio; $\overline{SHDN}$ = DIR = $V_{IO;}$ SLR, TERM_TX, TERM_RX= floating; Time from 50% of MODE1 rising edge to R2 reaching 2V; See Figure 6-12		0.04	0.1	µs
t_{R4_R2}	Time to switch from RS-485 full dupplex mode to RS-232 3T5R mode	L2 = Vio, MODE1 from Vio to GND, MODE0 = Vio; $\overline{SHDN}$ = DIR = $V_{IO;}$ SLR, TERM_TX, TERM_RX= floating; Time from 50% of MODE1 falling edge to R2 reaching 300 mV; See Figure 6-12		2	2.1	µs
t_{FHD_RS485}	Time to switch from RS-485 full duplex to half duplex mode	DIR= V_{IO}, MODE1 = V_{IO}; MODE0 from V_{IO} to GND ; $\overline{SHDN}$ = V_{IO} , SLR, TERM_TX, TERM_RX= floating; L2= GND, 10k pull down resistor on L1, Time from 50% of MODE0 falling edge to 50% falling edge on L1; See Figure 6-13		0.5	1	µs
t_{HFD_RS485}	Time to switch from RS-485 half duplex to full duplex mode	DIR= V_{IO}, MODE1 = V_{IO}; MODE0 from GND to V_{IO} ; $\overline{SHDN}$ = V_{IO} , SLR, TERM_TX, TERM_RX= floating; L2= GND, 10k pull down resistor on L1, Time from 50% of MODE0 rising edge to 50% rising edge on L1; See Figure 6-13		0.5	1	µs

Copyright © 2024 Texas Instruments Incorporated

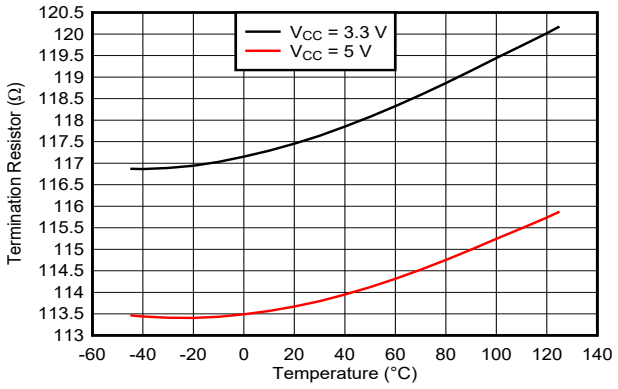
5.13 Switching Characteristics_RS-485_Termination resistor

Parameters over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5 V , V_{IO} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DTEN}	Driver terminal Termination resistor turn-on time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, DIR = GND, V_{R2R1} = 2 V, V_{R1} = 0 V; See Figure 6-10		1000	2200	ns
t_{DTZ}	Driver terminal Termination resistor turn-off time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, DIR = GND, V_{R2R1} = 2 V, V_{R1} = 0 V; See Figure 6-10		2000	7200	ns
t_{RTEN}	Receiver terminal Termination resistor turn-on time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, V_{R3R4} = 2 V, V_{R4} = 0 V; See Figure 6-10		1000	2200	ns
t_{RTZ}	Receiver terminal Termination resistor turn-off time	MODE1, MODE0 = 11; V_{IO} = 3 to 3.6 V, V_{R3R4} = 2 V, V_{R4} = 0 V; See Figure 6-10		2000	7200	ns

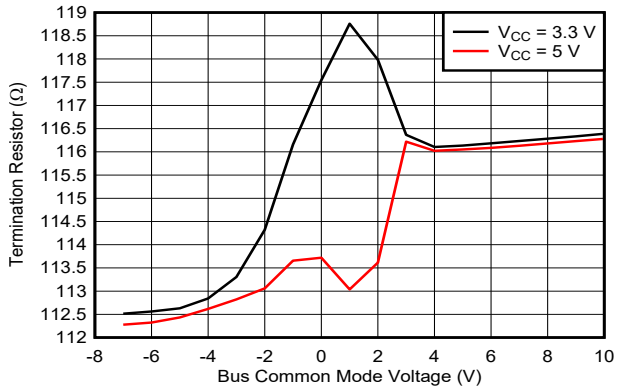
Copyright © 2024 Texas Instruments Incorporated

5.14 Typical Characteristics



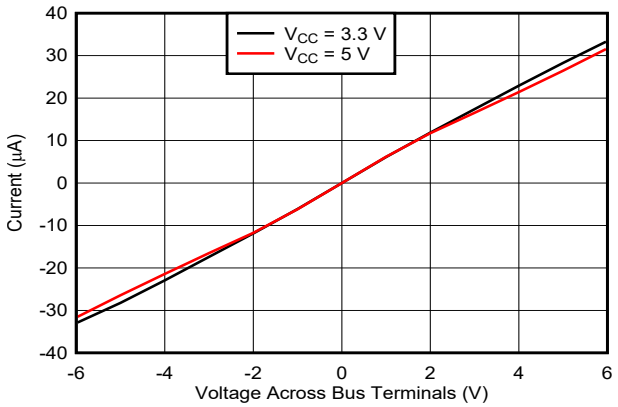
RS-485 Full Duplex mode V(R3-R4) = 2V

Figure 5-1. RS-485 Termination Resistor vs Temperature



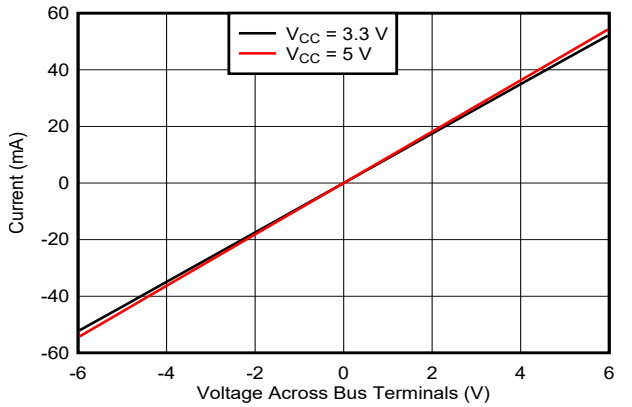
RS-485 Full Duplex mode V(R3-R4) = 2V

Figure 5-2. Termination Resistor vs Bus Common Mode Voltage



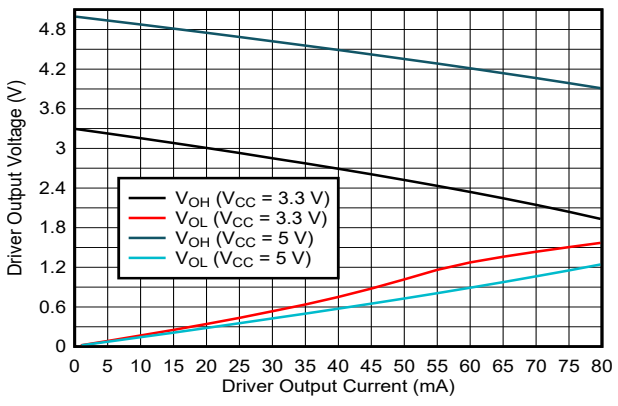
TERM_TX = GND DIR = GND T_A = 25°C

Figure 5-3. Voltage vs Current across R2-R1 Bus Pins with Termination OFF



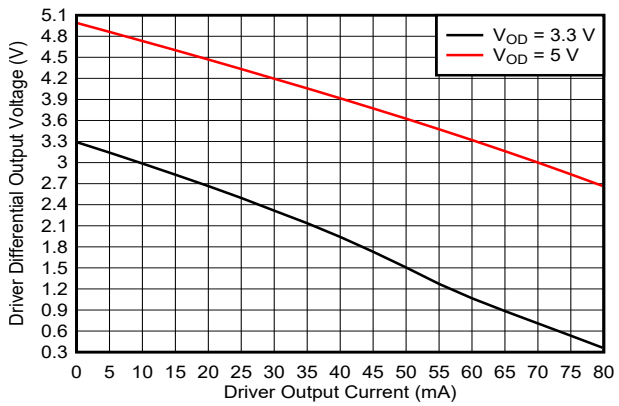
TERM_TX = V_{IO} DIR = GND T_A = 25°C

Figure 5-4. Voltage vs Current across R2-R1 Bus Pins with Termination ON



DIR = V_{IO} T_A = 25°C

Figure 5-5. RS-485 Driver Output Voltage vs Driver Output Current

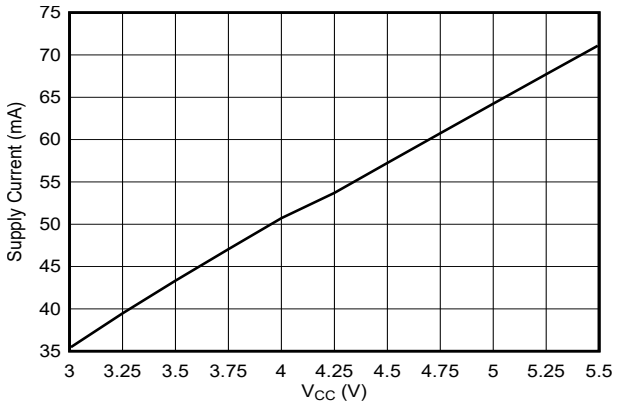


DIR = V_{IO} T_A = 25°C

Figure 5-6. RS-485 Driver Differential Output Voltage vs Driver Output Current

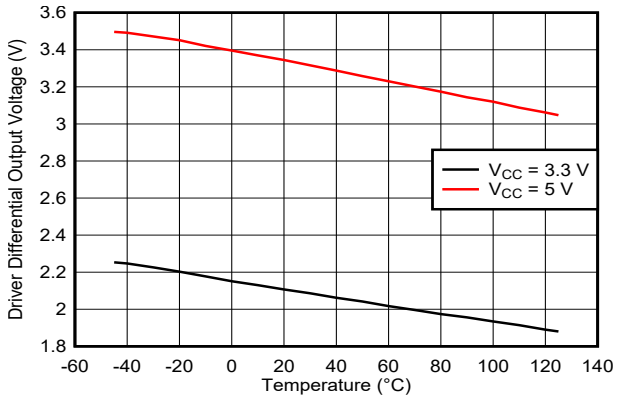
Copyright © 2024 Texas Instruments Incorporated

5.14 Typical Characteristics (continued)



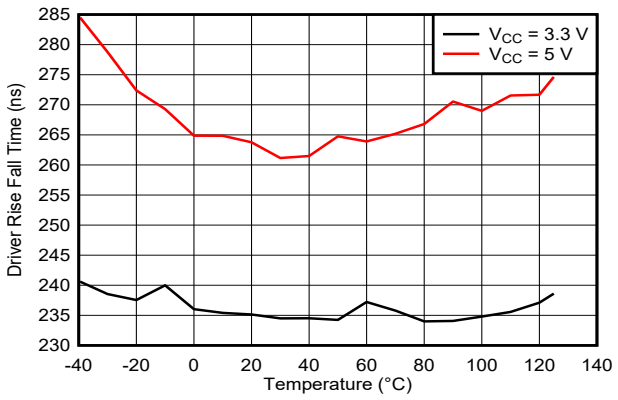
T_A = 25°C R_L = 54Ω DIR = L2 = V_{IO}
RS-485 Full Duplex mode

Figure 5-7. RS-485 Supply Current vs Supply Voltage



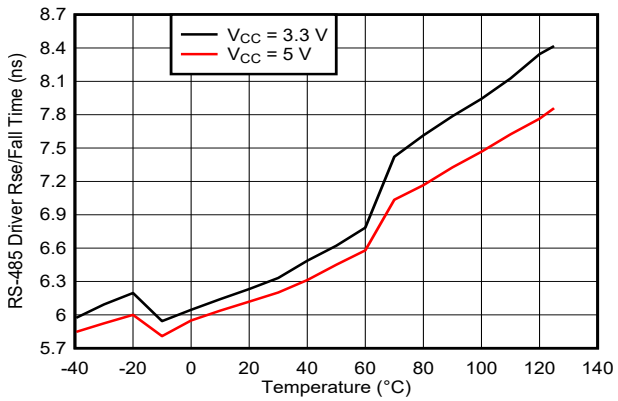
DIR = L2 = V_{IO} R_L = 54Ω
RS-485 Full Duplex mode

Figure 5-8. RS-485 Driver Differential Output Voltage vs Temperature



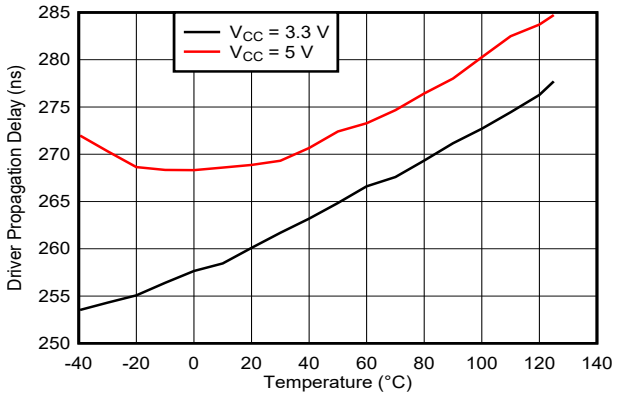
Bus Load = 54Ω ||50 pF SLR = V_{IO} DIR = V_{IO}

Figure 5-9. RS-485 500kbps Driver Rise or Fall Time vs Temperature



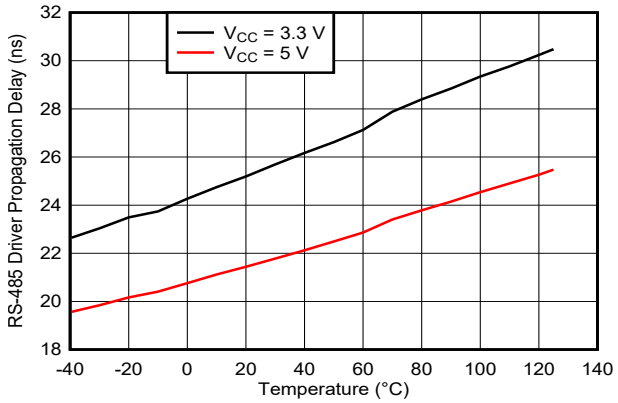
Bus Load = 54Ω || 50pF SLR = GND DIR = V_{IO}

Figure 5-10. RS-485 20Mbps Driver Rise or Fall Time vs Temperature



Bus Load = 54Ω ||50 pF SLR = V_{IO} DIR = V_{IO}

Figure 5-11. RS-485 500kbps Driver Propagation Delay vs Temperature

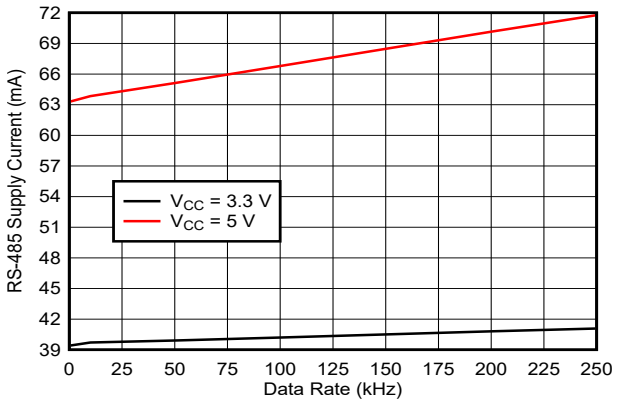


Bus Load = 54Ω || 50pF SLR = GND DIR = V_{IO}

Figure 5-12. RS-485 20Mbps Driver Propagation Delay vs Temperature

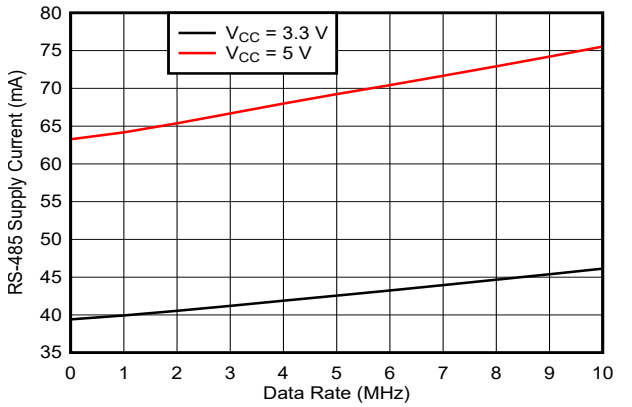
Copyright © 2024 Texas Instruments Incorporated

5.14 Typical Characteristics (continued)



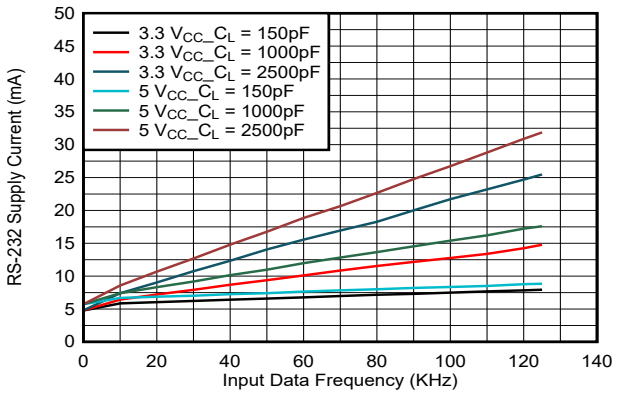
T_A = 25°C R_L = 54Ω DIR = V_{IO}

Figure 5-13. RS-485 500kbps Supply Current vs Signaling Rate



T_A = 25°C R_L = 54Ω DIR = V_{IO}

Figure 5-14. RS-485 20Mbps Supply Current vs Signaling Rate

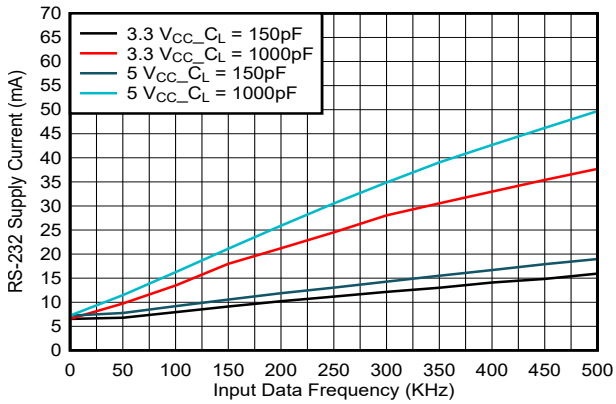


T_A = 25°C SLR = V_{IO}

Driver output loaded with 5kΩ ; device in RS-232 1T1R mode

L2 = toggling

Figure 5-15. RS-232 Supply Current vs Signaling Rate for 250 kbps Mode



T_A = 25°C SLR = GND

Driver output loaded with 5kΩ ; device in RS-232 1T1R mode

L2 = toggling

Figure 5-16. RS-232 Supply Current vs Signaling Rate for 1 Mbps Mode

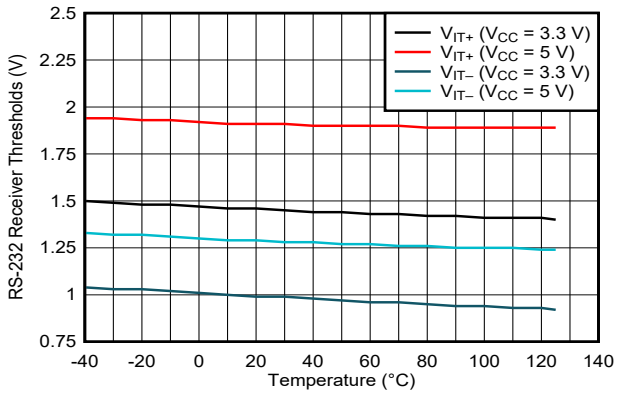


Figure 5-17. RS-232 Receiver Thresholds vs Temperature

Copyright © 2024 Texas Instruments Incorporated

6 Parameter Measurement Information

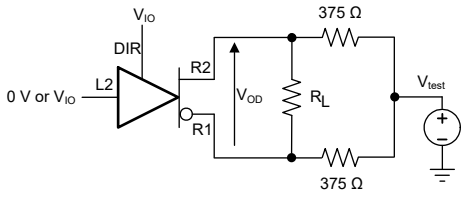


Figure 6-1. Measurement of RS-485 Driver Differential Output Voltage With Common-Mode Load

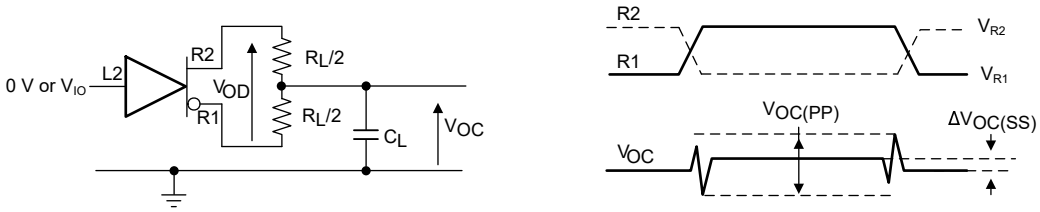


Figure 6-2. Measurement of RS-485 Driver Differential and Common-Mode Output With RS-485 Load

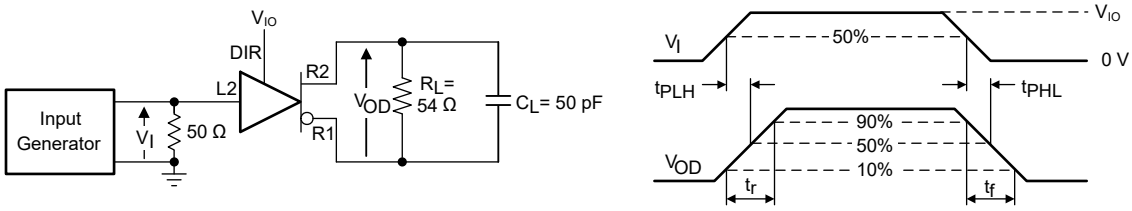


Figure 6-3. Measurement of RS-485 Driver Differential Output Rise and Fall Times and Propagation Delays

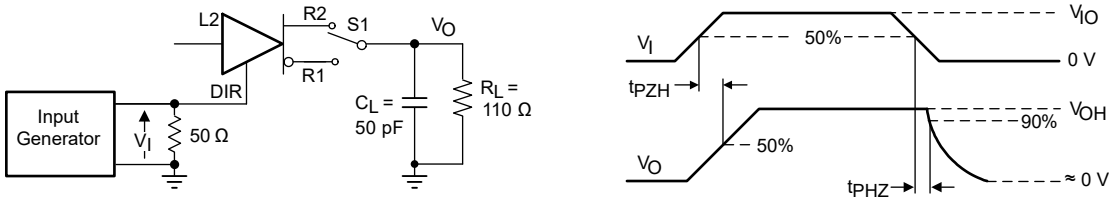


Figure 6-4. Measurement of RS-485 Driver Enable and Disable Times With Active High Output and Pull-Down Load

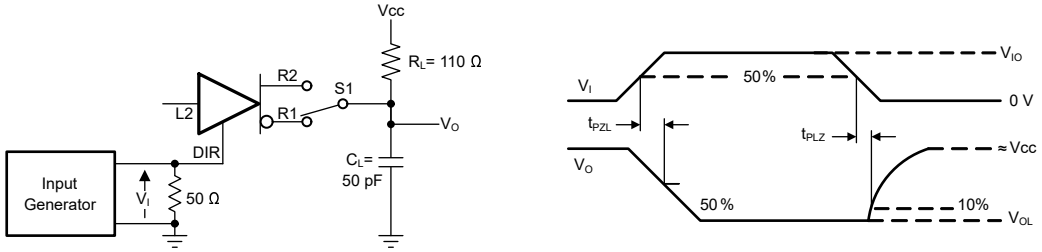


Figure 6-5. Measurement of RS-485 Driver Enable and Disable Times With Active Low Output and Pull-up Load

Copyright © 2024 Texas Instruments Incorporated

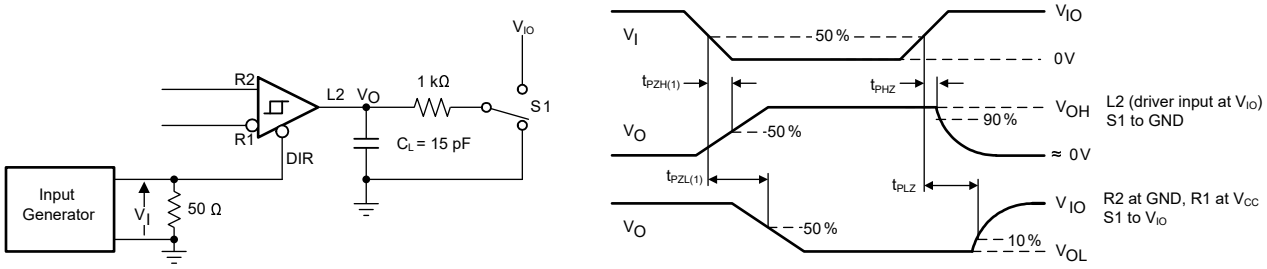


Figure 6-6. Measurement of RS-485 Receiver Output Rise and Fall Times and Propagation Delays

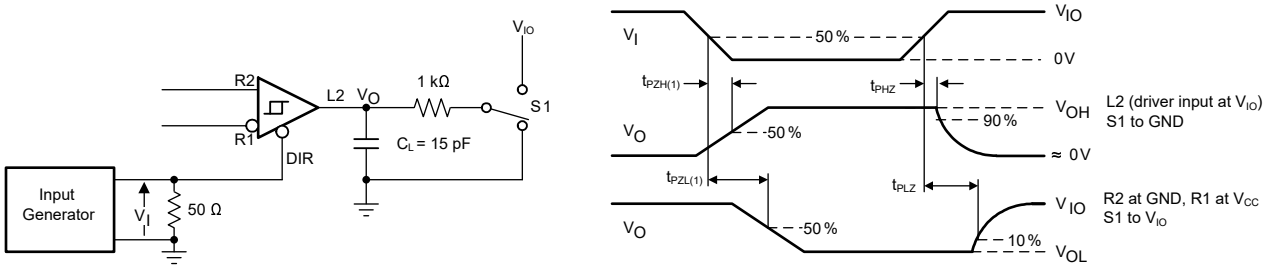


Figure 6-7. Measurement of RS-485 Receiver Enable and Disable Times in Half Duplex Mode

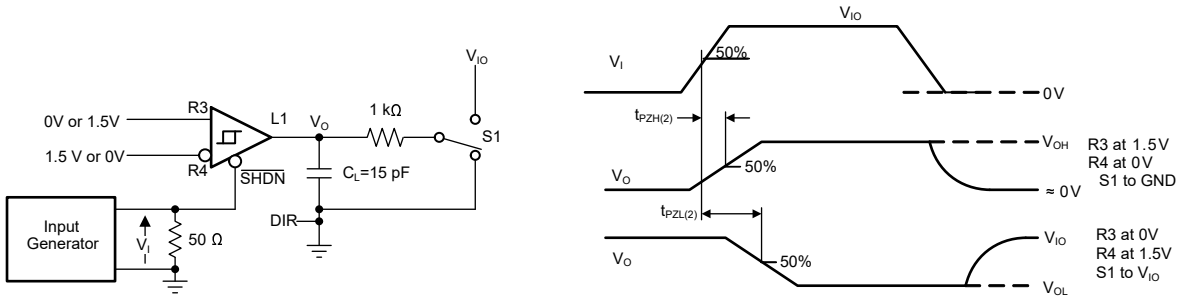


Figure 6-8. Measurement of RS-485 Receiver Enable Time from Shutdown with TX disabled: Full Duplex Mode

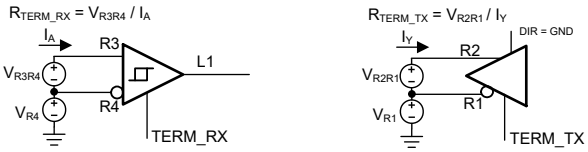


Figure 6-9. Termination Resistor Measurement

Copyright © 2024 Texas Instruments Incorporated

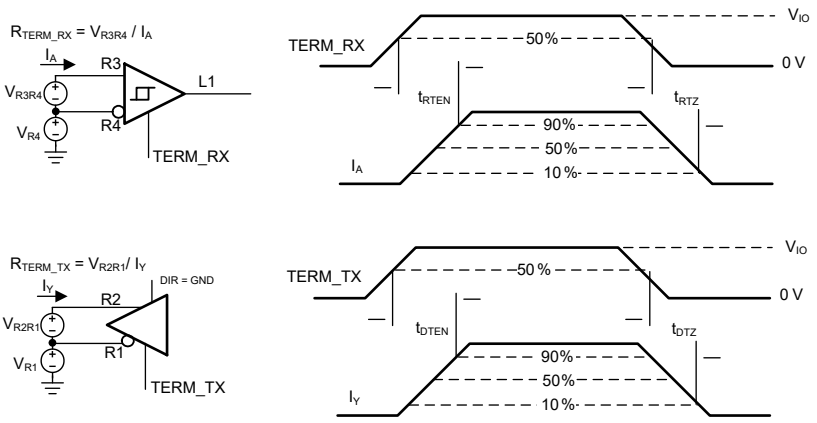


Figure 6-10. Termination Resistor Switching Measurement

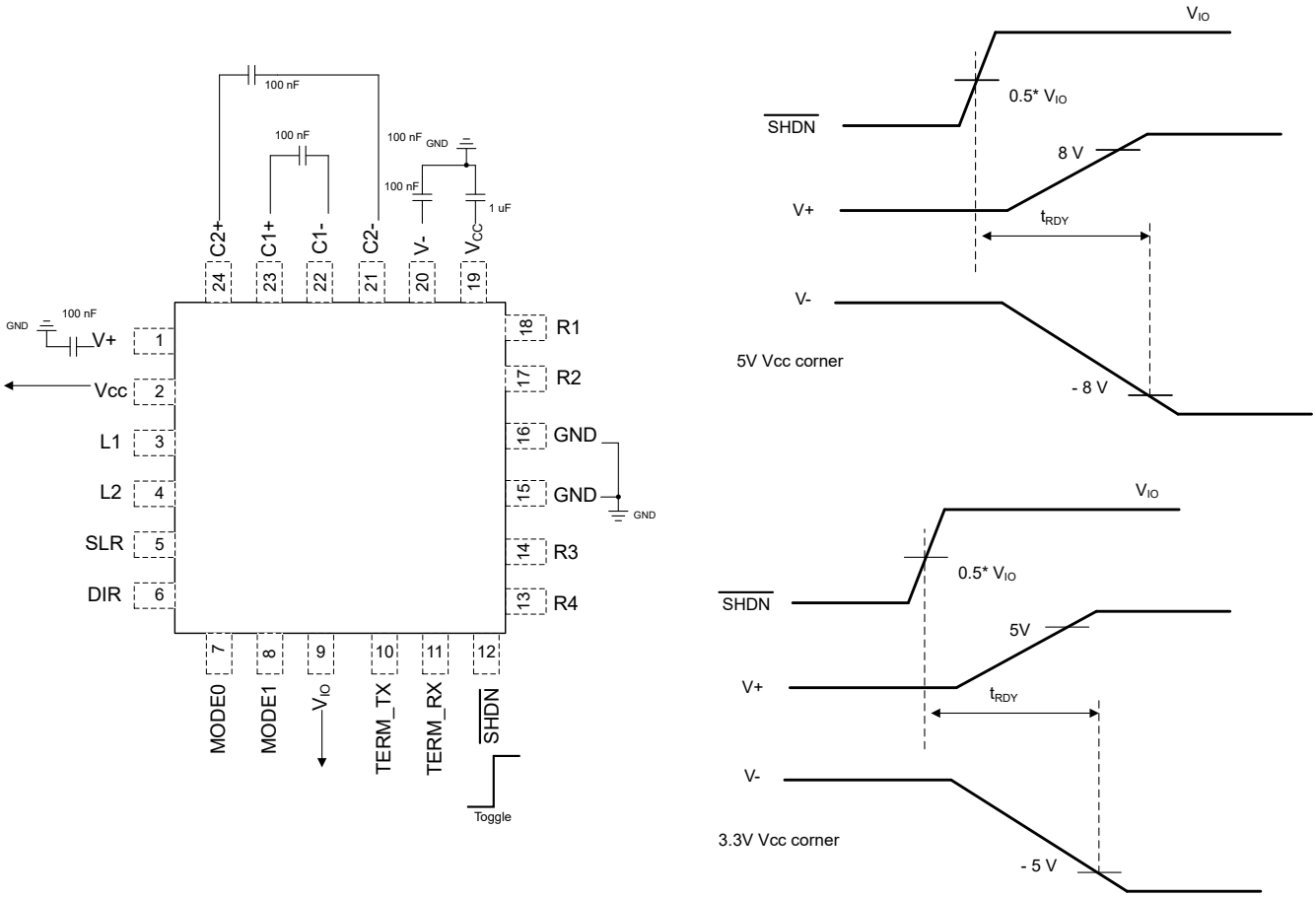


Figure 6-11. Time from Shutdown to RS-232 Ready

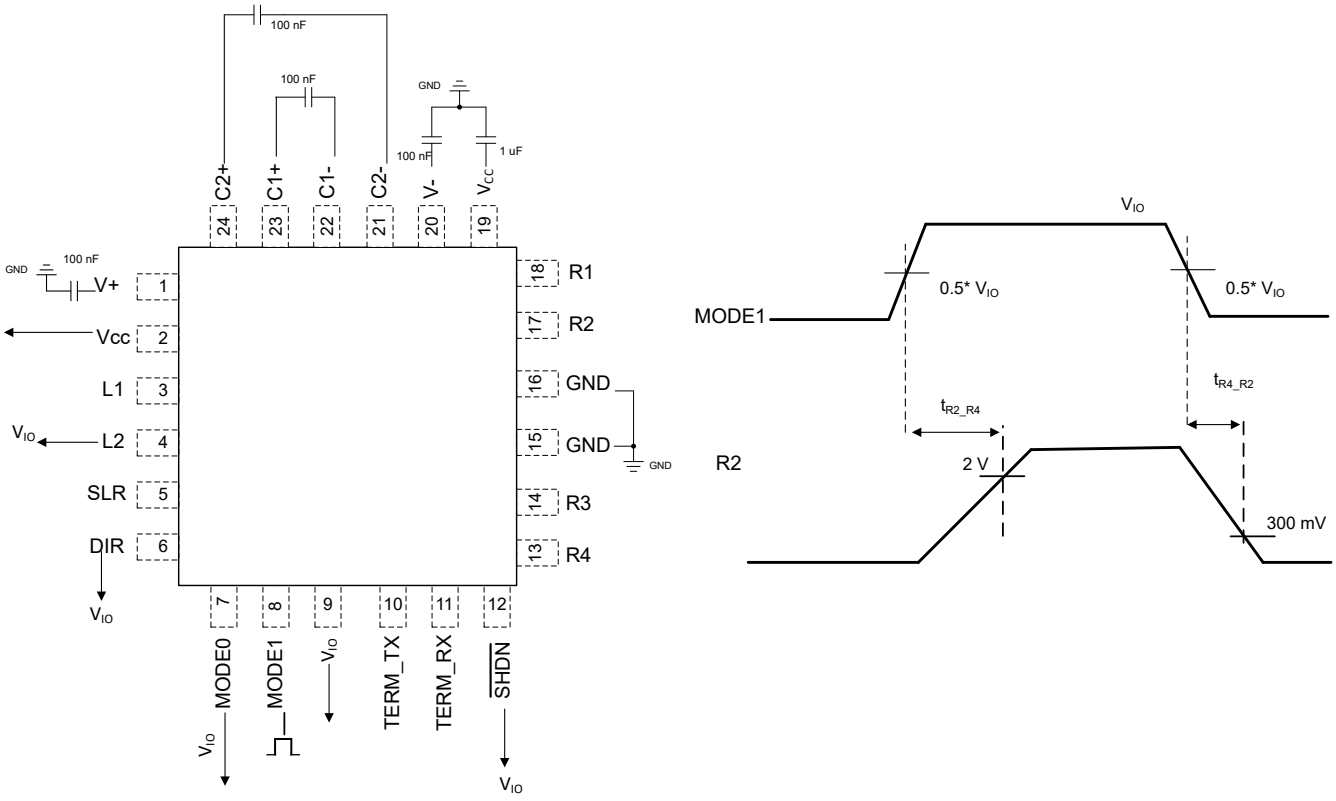


Figure 6-12. Time to Switch from RS-232 Mode to RS-485 Full Duplex Mode and Back

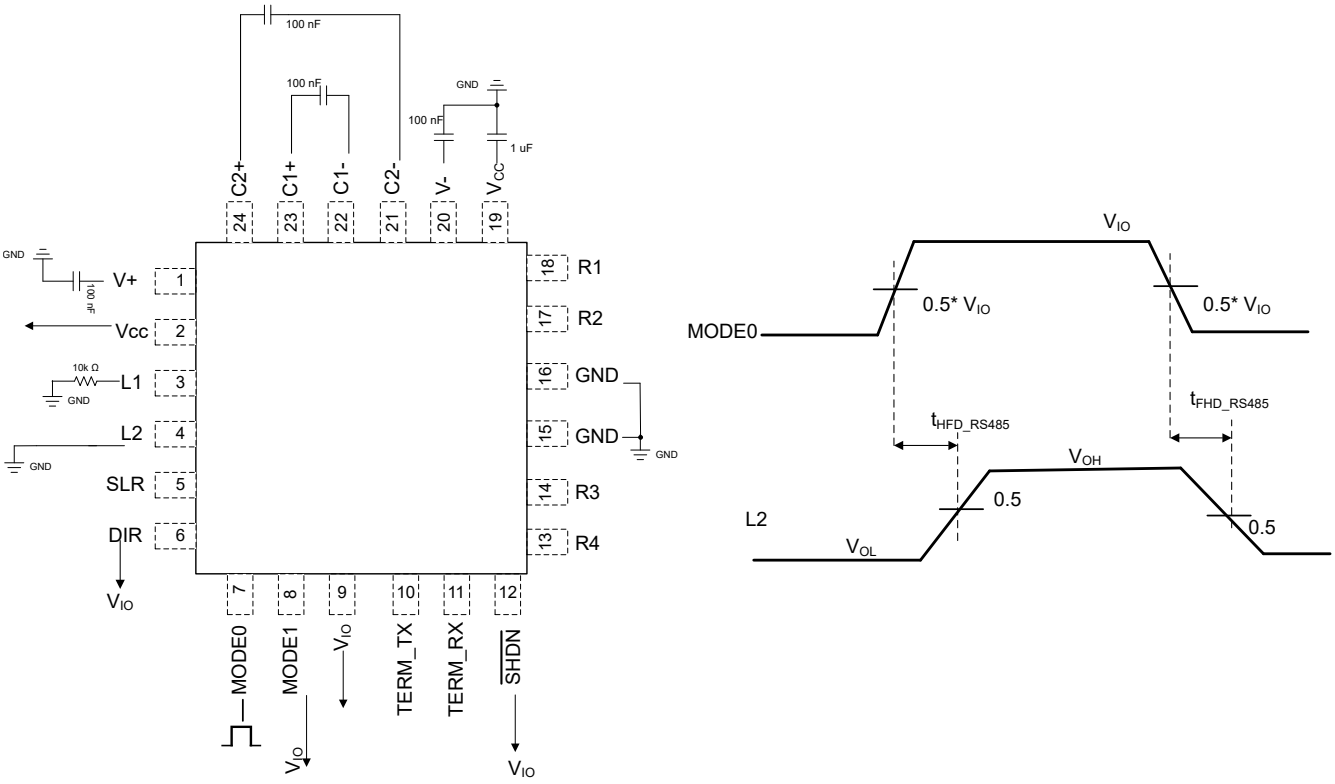
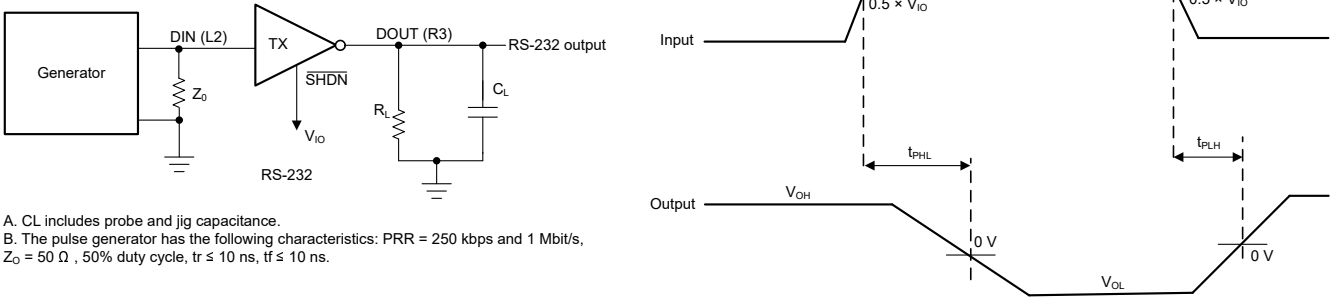


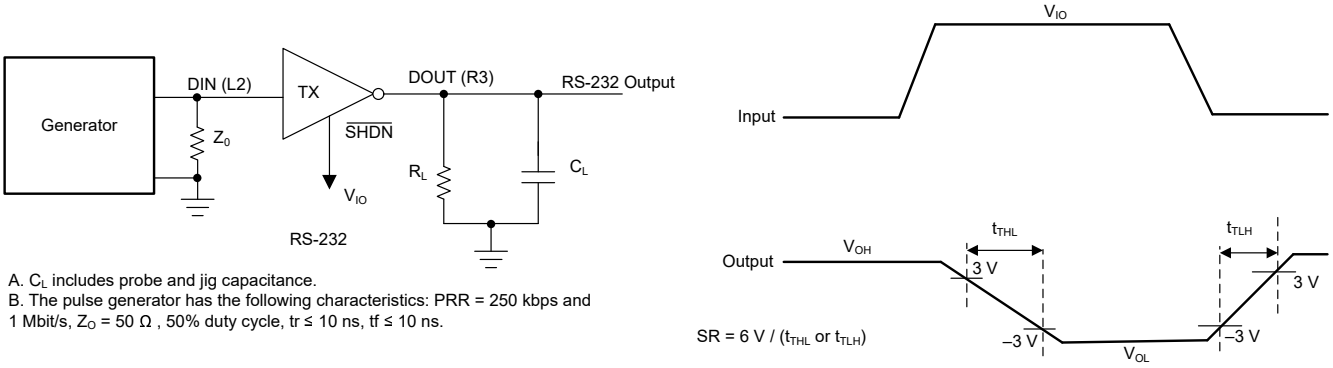
Figure 6-13. Time to Switch from RS-485 Full Duplex to Half Duplex and Back

Copyright © 2024 Texas Instruments Incorporated



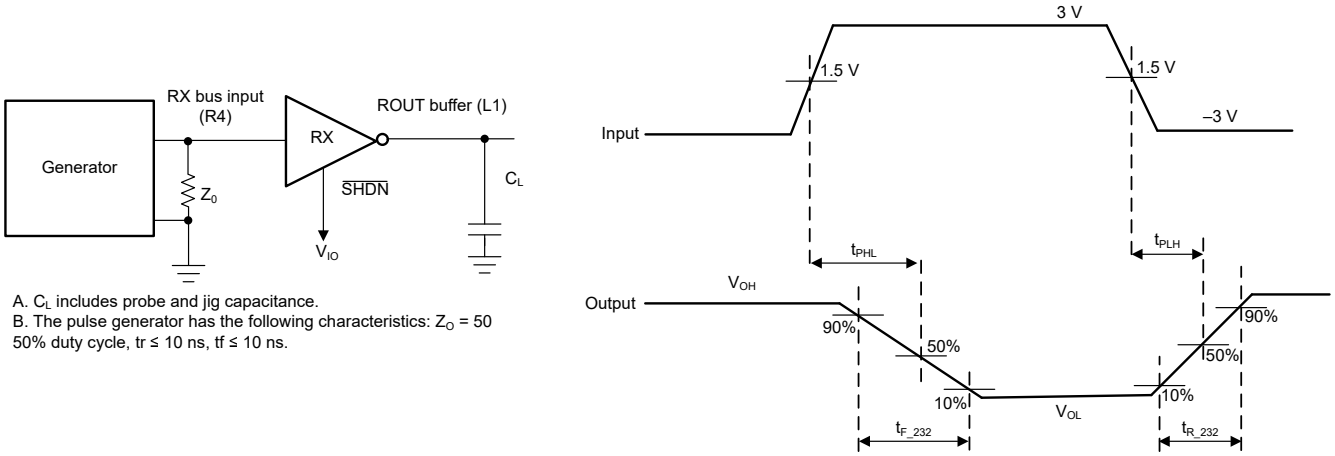
A. CL includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbps and 1 Mbit/s, Z_O = 50 Ω , 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

Figure 6-14. RS-232 Driver Prop Delay, Pulse Skew



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbps and 1 Mbit/s, Z_O = 50 Ω , 50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

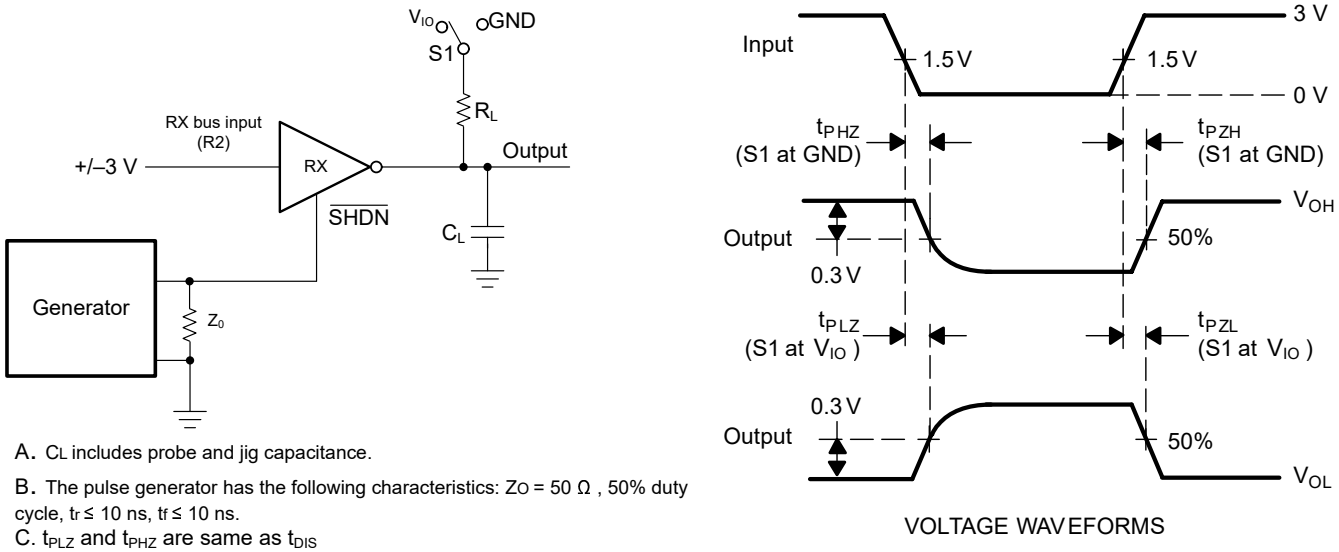
Figure 6-15. RS-232 Driver Slew Rate



A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50
50% duty cycle, tr ≤ 10 ns, tf ≤ 10 ns.

Figure 6-16. RS-232 Receiver Propagation Delay, Pulse Skew

Copyright © 2024 Texas Instruments Incorporated



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω , 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.

C. t_{PLZ} and t_{PHZ} are same as t_{DIS}

D. t_{PZL} and t_{PZH} are same as t_{EN}

Figure 6-17. RS-232 Receiver Enable and Disable Time

Copyright © 2024 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

THVD4411 is a highly integrated and robust multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layers. The device has one transmitter and one receiver to enable 1T1R RS-232 port. Device also integrates one transmitter and one receiver to enable half and full duplex RS-485 port. MODE selection pins enable shared bus and logic pins for the protocols to share a common single connector.

The device has SLR pin which allows it to be used for two different maximum speed settings for RS-232 and for RS-485. This is beneficial as customers can qualify one device and use it in two separate end-applications. The devices also have flexible I/O supply pin V_{IO} which enables digital interface voltage range, from 1.65V to 5.5V, different from bus voltage supply 3V to 5.5V.

7.2 Functional Block Diagram

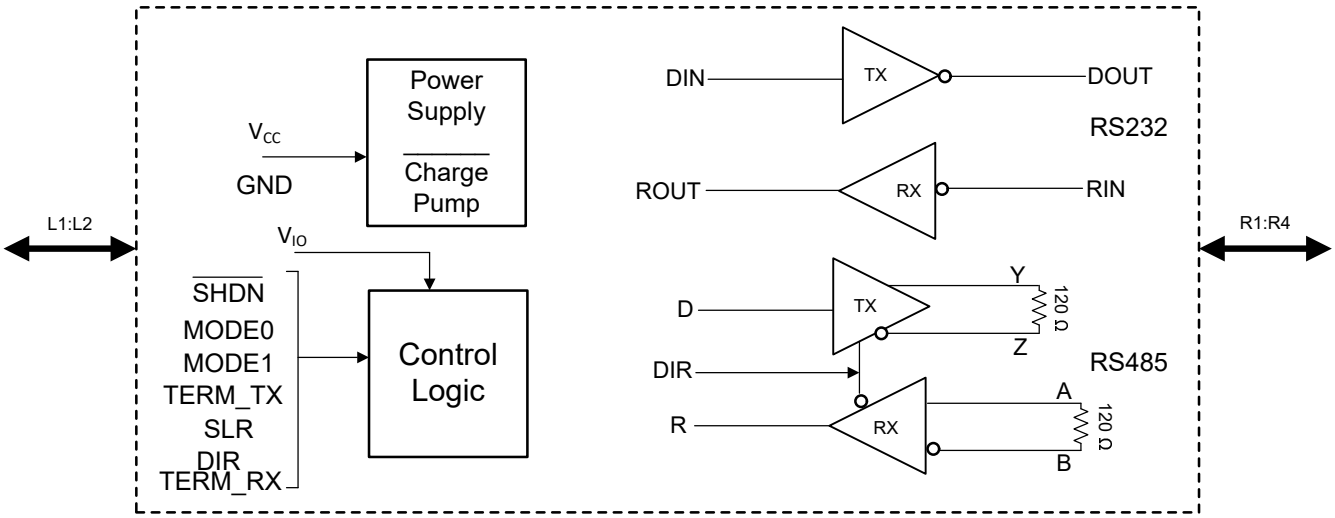


Figure 7-1. THVD4411 Block Diagram

7.3 Feature Description

7.3.1 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect all the transceiver bus pins (driver and receiver) against electrostatic discharges (ESD) according to IEC 61000-4-2 up to ±8kV for contact diacharge and ±15kV (air-discharge) for all operating modes. Bus lines in RS-485 mode can also withstand electrical fast transients (EFT) according to IEC 61000-4-4 for up to ±4kV.

7.3.2 Protection Features

The THVD4411 bus pins are protected against any DC supply shorts in the range of -16V to +16V. In the RS-485 mode, the short circuit current is limited to ±250mA to comply with the TIA/EIA-485A standard. In RS-232 mode, current limiting of ±60mA is applicable for scenarios where bus pins can short to ground.

The device also features thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation on-chip.

Supply undervoltage protection is present on both V_{CC} and V_{IO} supplies. This maintains the bus output and receiver logic output in known driven state when both the supplies are above their rising undervoltage thresholds. Table below describes the device behavior in various scenarios of supply levels.

Table 7-1. Supply Function Table

V_{CC}	V_{IO}	Driver Output	Receiver Output
> $UV_{VCC(rising)}$	> $UV_{VIO(rising)}$	For RS-485 mode, determined by DIR and L2 inputs. For RS-232 mode, determined by L2 input. For shutdown mode, Hi-Z	For RS-485 mode, determined by DIR and (R1-R2) or (R3-R4) inputs. For RS-232 mode, determined by R2 input. For shutdown mode, Hi-Z
< $UV_{VCC(falling)}$	> $UV_{VIO(rising)}$	High impedance	Undetermined
> $UV_{VCC(rising)}$	< $UV_{VIO(falling)}$	High impedance	High impedance
< $UV_{VCC(falling)}$	< $UV_{VIO(falling)}$	High impedance	High impedance

Copyright © 2024 Texas Instruments Incorporated

7.3.3 Receiver Fail-Safe Operation

The RS-485 differential receiver of the THVD4411 is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200mV. The receiver parameters which determine the failsafe performance are V_{TH+}, $V_{TH–}$, and V_{HYS} (the separation between V_{TH+} and $V_{TH–}$). As shown in the Receiver Function table, differential signals more negative than –200 mV always causes a low receiver output, and differential signals more positive than 200 mV always causes a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output is high. Only when the differential input is more than V_{HYS} below V_{TH+} does the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault conditions includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{TH+}.

7.3.4 Low-Power Shutdown Mode

Driving the $\overline{SHDN}$ pin low puts the device into the shutdown mode. This is the lowest power mode of the device and current consumption is 10 uA typical. All the blocks get are disabled in this mode.

7.3.5 On-chip Switchable Termination resistor

THVD4411 has 2 termination resistors of nominal 120Ω, one across R1/R2 and another across R3/R4 in RS-485 mode. Both termination resistors are enabled or disabled using pins as described in Table 7-2. Both the termination resistors can be enabled or disabled independent of the state of driver or receiver. Termination is OFF in RS-232 1T1R, unpowered and thermal shutdown modes.

Table 7-2. On-chip termination function table

Signal state	Device mode	Function	Comments
TERM_TX = V_{IO}	Full duplex mode	120Ω enabled between R1 and R2	Termination between R1/R2 is disabled by default
TERM_TX = GND or floating	Full duplex mode	120Ω disabled between R1 and R2	
TERM_RX = V_{IO}	Full duplex mode	120Ω enabled between R3 and R4	Termination between R3/R4 is disabled by default
TERM_RX = GND or floating	Full duplex mode	120Ω disabled between R3 and R4	
TERM_RX = X, TERM_TX = V_{IO}	Half duplex mode	120Ω enabled between R1 and R2	In half duplex mode, TERM_RX is don't care and TERM_TX has higher priority
TERM_RX = X, TERM_TX = GND	Half duplex mode	120Ω disabled between R1 and R2	

On-chip 120Ω termination resistor is designed to have a minimum variation with temperature and across common mode voltage on bus pins. Also, the termination block offers a resistive load to the bus, and does not alter the magnitude or phase of the bus signals from DC to 20Mbps signaling.

Copyright © 2024 Texas Instruments Incorporated

7.3.6 Operational Data Rate

THVD4411 can be used in slow speed or fast speed RS-485 and RS-232 applications by configuring slew rate control (SLR) pin. Table 7-3 describes slew rate control function.

Table 7-3. Slew rate control function table

Signal state	Driver	Receiver	Comment
SLR = V_{IO}	Maximum speed of operation for RS-485 = 500kbps. Maximum speed of operation in RS-232 mode is 250kbps	Maximum speed of operation for RS-485 = 500kbps. Maximum speed of operation in RS-232 mode is 250kbps	Active high slew rate limiting applied on driver output. In this configuration, glitch filter in receiver path for RS-485 is enabled
SLR = GND or floating	Maximum speed of operation for RS-485= 20Mbps. Maximum speed of operation in RS-232 mode is 1Mbps	Maximum speed of operation for RS-485 = 20Mbps. Maximum speed of operation in RS-232 mode is 1Mbps	Slew rate limiting on driver output disabled.

For RS-485 half and full duplex modes, receiver path in the slow speed mode (500kbps) provides additional noise filtering. To attenuate high frequency noise pulses from the bus which can be wrongly interpreted as valid data, SLR = V_{IO} enables a low pass filter to filter out pulses with frequency higher than typical 800kHz.

7.3.7 Integrated Charge Pump for RS-232

THVD4411 has a integrated high-efficiency and low-noise charge pump to generate large output voltages for RS-232 signals. Charge pump consists of a voltage doubler and an inverter to regulate the voltage to ± 6V or ± 10V for 3.3V or 5V V_{CC} operation respectively. Charge pump needs four external ceramic capacitors and allows for single supply operation for RS-232. For a generic description of RS-232 charge pump operation, please refer to the blog: How the RS-232 Transceiver's Regulated Charge-pump Circuitry Works

Copyright © 2024 Texas Instruments Incorporated

7.4 Device Functional Modes

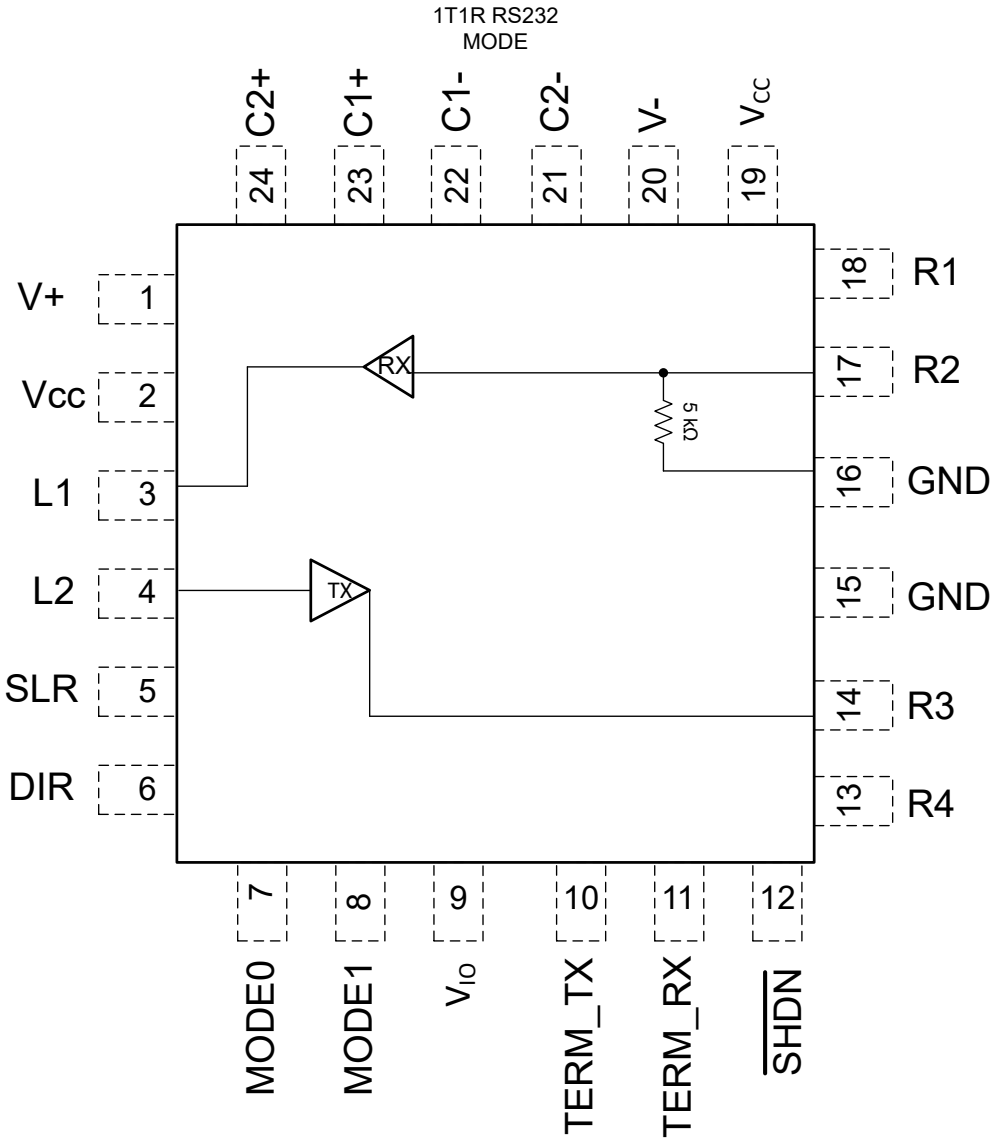


Figure 7-2. RS-232 Mode

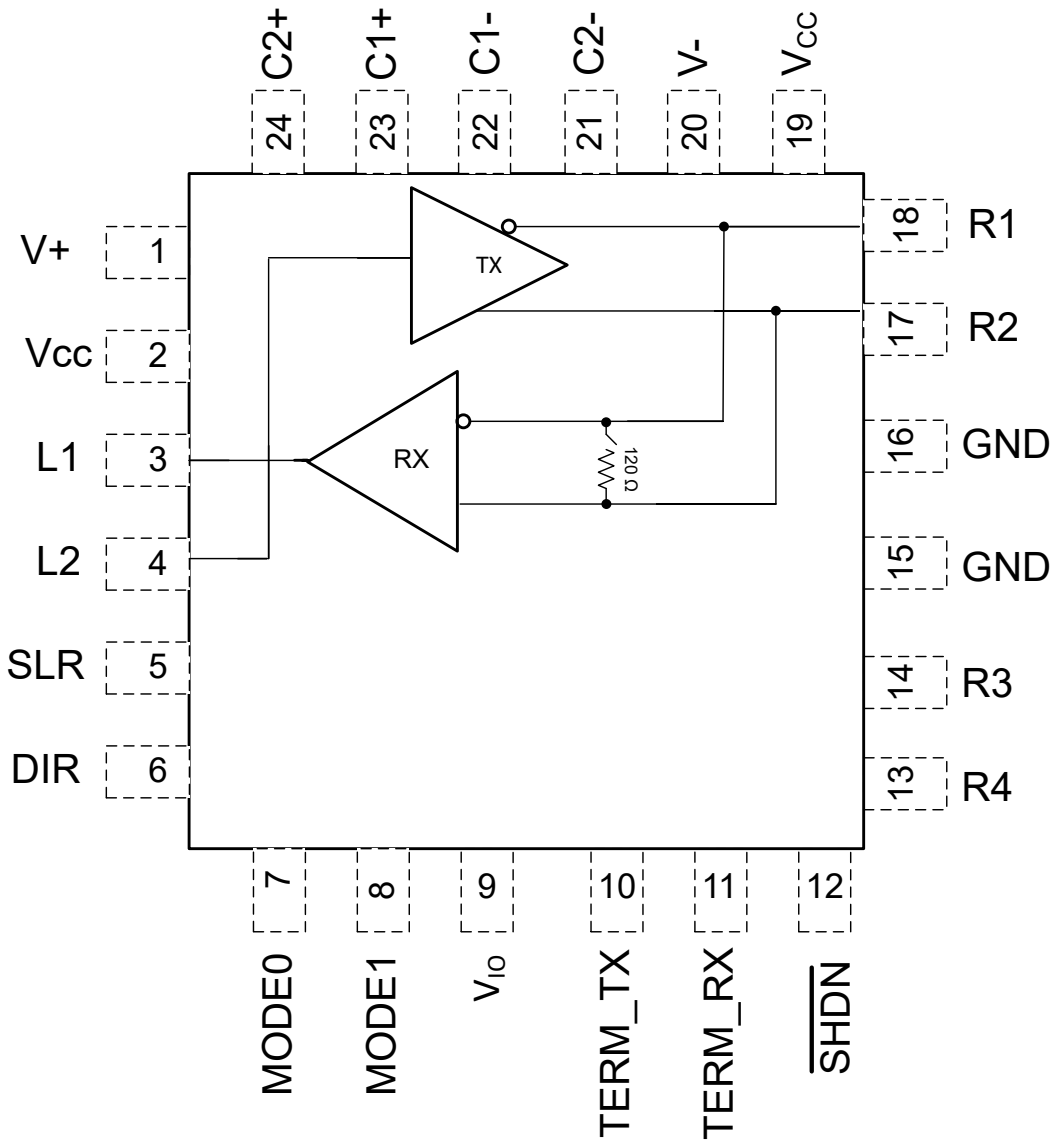


Figure 7-3. RS-485 Half Duplex Mode

Copyright © 2024 Texas Instruments Incorporated

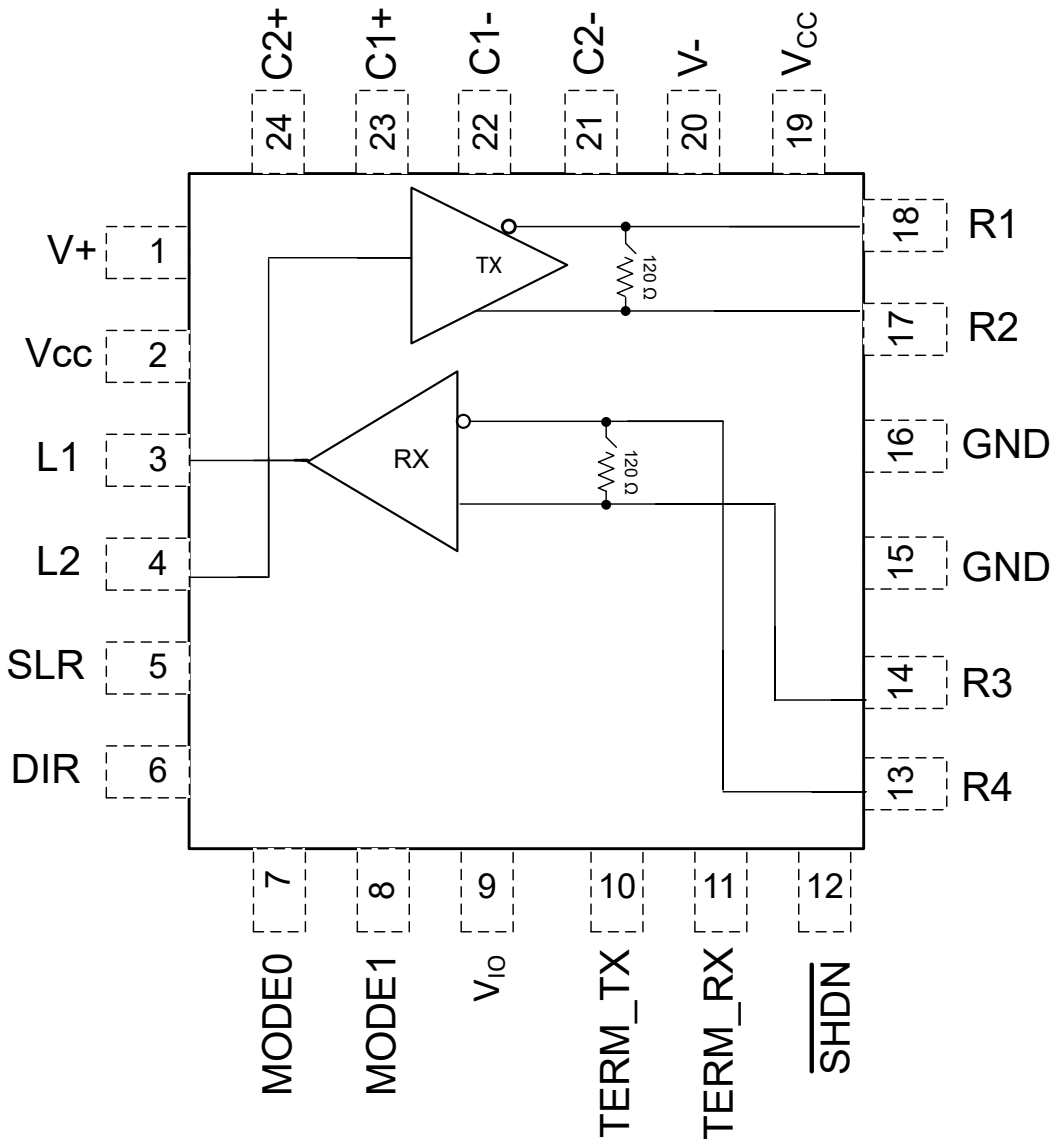


Figure 7-4. RS-485 Full Duplex Mode

7.4.1 RS-485 Functionality

When the driver enable pin, DIR, is logic high, the differential outputs R2 and R1 follow the logic states at data input L2. A logic high at L2 causes R2 to turn high and R1 to turn low. In this case the differential output voltage defined as $V_{OD} = V_{R2} – V_{R1}$ is positive. When L2 is low, the output states reverse: R1 turns high, R2 becomes low, and V_{OD} is negative.

When DIR is low, both outputs turn high-impedance. In this condition the logic state at L2 is irrelevant. The DIR pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The L2 pin has an internal pull-up resistor to V_{IO}, thus, when left open while the driver is enabled, output R2 turns high and R1 turns low.

Table 7-4. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
L2	DIR	R2	R1	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	High impedance	High impedance	Driver disabled
X	OPEN	High impedance	High impedance	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

Table 7-4 is valid for both half duplex and full duplex modes, and is independent of state of TERM_TX, TERM_RX and SLR pins.

In full duplex mode, if $\overline{SHDN}$ is high, receiver is always enabled. In half duplex mode, receiver is enabled is DIR = Low/floating and disabled if DIR = V_{IO}. When the differential input voltage defined as $V_{ID} = V_{R2} – V_{R1}$ or $V_{R3} – V_{R4}$ is higher than the positive input threshold, V_{TH+}, the receiver output, L2, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, L2, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

In half duplex mode, when DIR is high, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 7-5. Receiver Function Table

DIFFERENTIAL INPUT	OUTPUT	FUNCTION
$V_{ID} = V_{R2} – V_{R1}$(Half duplex mode) or $V_{R3} – V_{R4}$(Full duplex mode)	L1	
$V_{TH+} < V_{ID}$	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	Receive valid bus low
X	High impedance for DIR = V_{IO} in Half duplex mode	Receiver disabled in half duplex mode for DIR = V_{IO}
Open-circuit bus	H	Fail-safe high output
Short-circuit bus	H	Fail-safe high output
Idle (terminated) bus	H	Fail-safe high output

Table 7-5 is valid irrespective of state of TERM_TX, TERM_RX and SLR pins.

Copyright © 2024 Texas Instruments Incorporated

7.4.2 RS-232 Functionality

In RS-232 mode, only way to disable driver is to go in shutdown mode by pulling $\overline{SHDN}$ pin low. A logic high at input for driver L2 causes driver output R3 to be driven low towards negative charge pump output V-. A logic low at input for driver L2 causes driver output R3 to be driven high towards positive charge pump output V+. If logic input is left floating due to the pull-up resistors on driver logic input, the driver output is driven low towards V-.

Table 7-6. Driver Function Table

INPUT	ENABLE	OUTPUTS	FUNCTION
L2	$\overline{SHDN}$	R3	
H	H	Low (driven towards V-)	Normal operation with inverting logic
L	H	H (Driven towards V+)	Normal operation with inverting logic
X	L	High impedance	TX and RX are disabled in shutdown mode
Open	H	Low (driven towards V-)	Since pull-up on logic input pin, output driven low by default

Table 7-6 is valid irrespective of the state of SLR pin.

For RS-232 receiver, if receiver bus input is above rising threshold V_{IT+}, then received logic output goes low. Also, if receiver bus input is below falling threshold V_{IT-}, received logic output goes high.

Table 7-7. Receiver Function Table

RS-232 BUS INPUT	LOGIC OUTPUT	FUNCTION
V_{IRx} (voltage on R2)	L1	
$V_{IT+} < V_{IRx}$	L	Normal operation with inverting logic
$V_{IT-} < V_{IRx} < V_{IT+}$	?	Indeterminate bus state
$V_{IRx} < V_{IT-}$	H	Normal operation with inverting logic
X	High impedance for $\overline{SHDN}$ = GND	Receiver disabled in shutdown mode
Open-circuit bus	H	Fail-safe high output

Table 7-7 is valid irrespective of the state of SLR pin.

7.4.3 Mode Control

Table 7-8. MODE Control Function Table

MODE1	MODE0	Operating mode	Function
L	H	RS-232 1T1R mode, charge pump is ON, V+/V- are regulated	1T1R mode; L2 is Logic input for RS232 driver; L1 is Logic output
H	L	RS-485 half duplex mode (charge pump is off)	L1 is RX Logic output; L2 is Driver Logic input; R1 R2 are Bus inverting and non-inverting terminals respectively
H	H	RS-485 full duplex mode (charge pump is off)	R1R2 are inverting and non-inverting driver terminals; R3R4 are non-inverting and inverting receiver terminals.

Copyright © 2024 Texas Instruments Incorporated

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

THVD4411 is a highly integrated multiprotocol transceiver supporting RS-232, RS-422 and RS-485 physical layer and is used for asynchronous data transmissions. MODE pins allow for the configuration of different operating modes. Device allows point-to-point RS-232 communication port and multipoint RS-485 communication port over common connector. The device also features integrated 120Ω switchable termination resistor on RS-485 bus lines which enables same device to be used for middle nodes or end nodes in an RS-485 network. When the device is configured in RS-232 mode, RS-485 circuits and 120Ω termination are disabled and do not interfere in RS-232 communication. For RS-232 communication, charge pump and 5kΩ resistor to ground on receiver bus pin is integrated in the device. This 5kΩ resistor and charge pump is automatically disabled in RS-485 mode. Slew rate limiting pin is provided so that same device can be used in slow speed or fast speed RS-485 and RS-232 applications. When ultra low power consumption is needed, device can be put in shutdown mode using $\overline{SHDN}$ pin. All these features make the device completely flexible and suitable for various application needs. Integration of termination resistor saves significant PCB area compared to discrete implementation.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

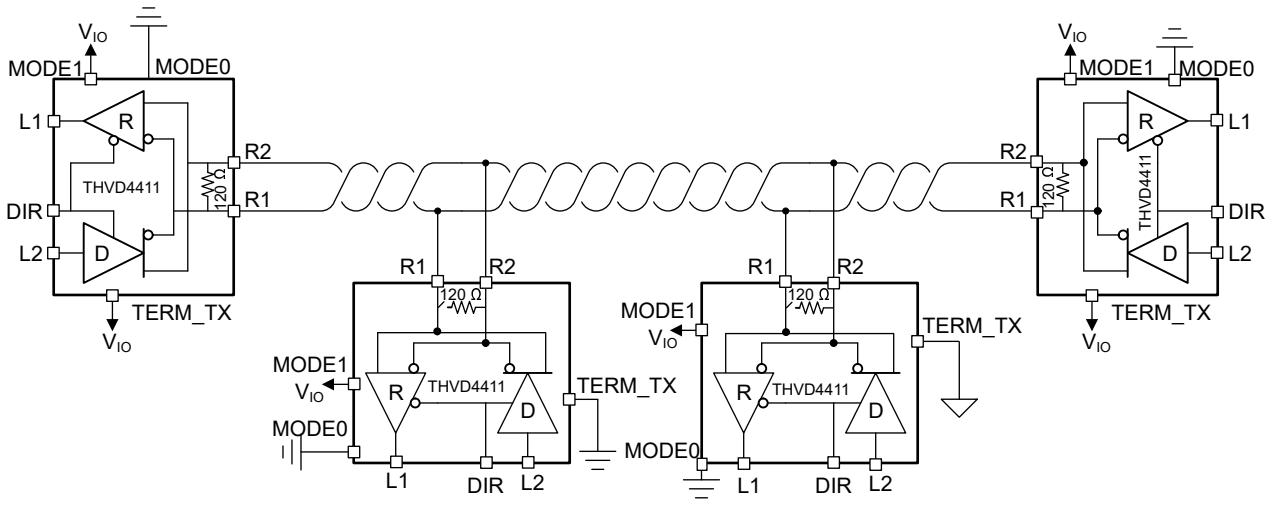


Figure 8-1. Typical RS-485 Network With Half-Duplex Transceivers

Copyright © 2024 Texas Instruments Incorporated

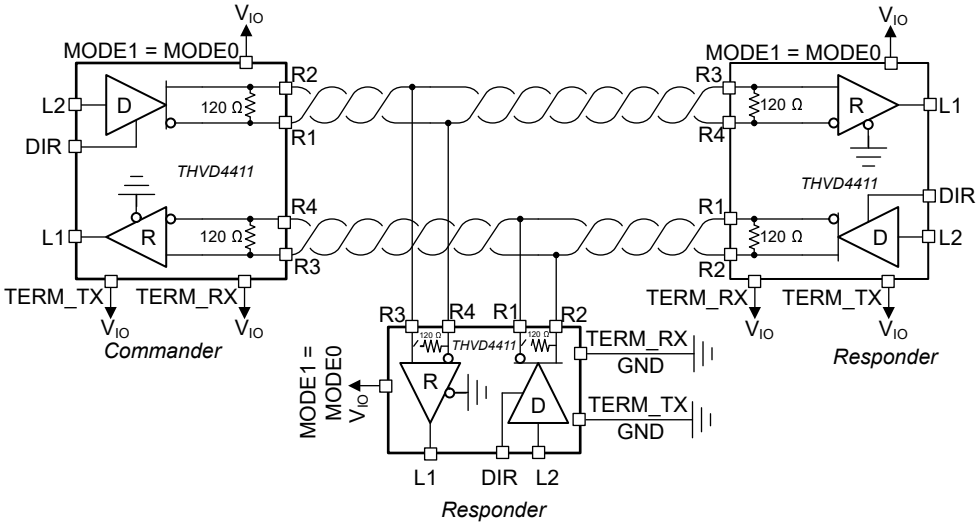


Figure 8-2. Typical RS-485 Network With Full-Duplex Transceivers

THVD4411 can be used in both networks (half and full duplex) and at all nodes (end node or middle nodes) since device has the configurability based on MODE1, MODE0 pins and TERM_TX, TERM_RX pins.

THVD4411 also consists of one line driver, one line receiver and dual charge pump circuit to enable RS-232 serial communication port. This device provides the electrical interface between an asynchronous communication controller and the serial-port connector.

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes. RS-232 is more suitable for debug or configuration point to point applications.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the short the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

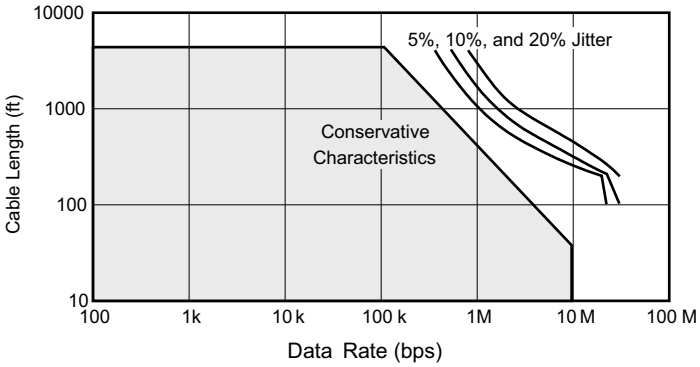


Figure 8-3. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50Mbps for the THVD24xxV) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

Copyright © 2024 Texas Instruments Incorporated

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver; thus, giving a maximum physical stub length as shown in Equation 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the THVD4411 device in RS-485 half and full duplex mode consists of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible for a limited common mode range of - 7V to 12V.

Copyright © 2024 Texas Instruments Incorporated

8.2.2 Detailed Design Procedure

Figure 8-4 suggests an application schematic for THVD4411. Device has all logic pins on one side and bus side pins on other side to enable a flow-through layout in end application.

All V_{CC} power pins should have 1µF decoupling capacitor close to the respective device pins. RS-232 charge pump is designed such that 100 nF charge pump capacitors work for both 3.3V and 5V operating V_{CC} supply.

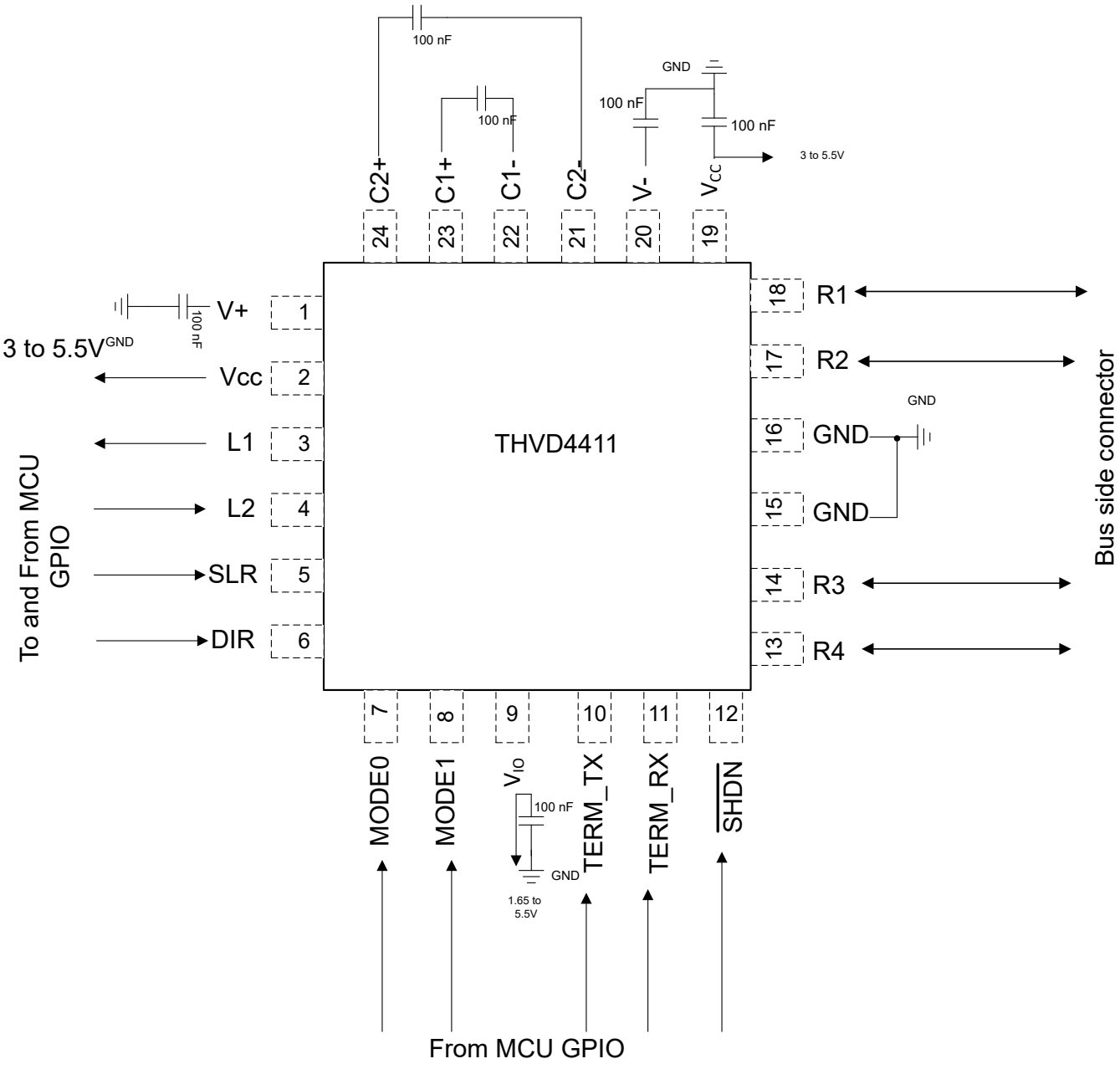
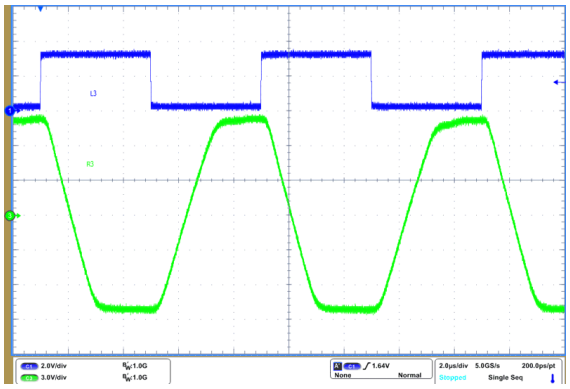


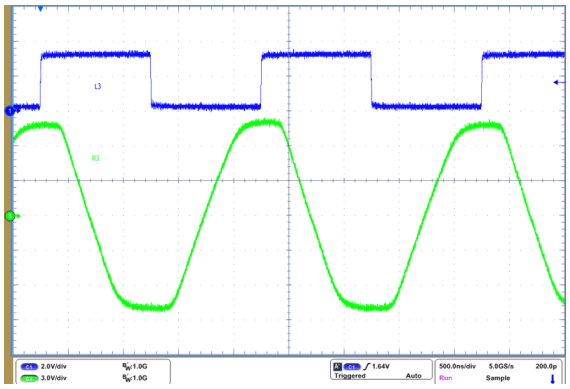
Figure 8-4. Typical application diagram for THVD4411

8.2.3 Application Curves



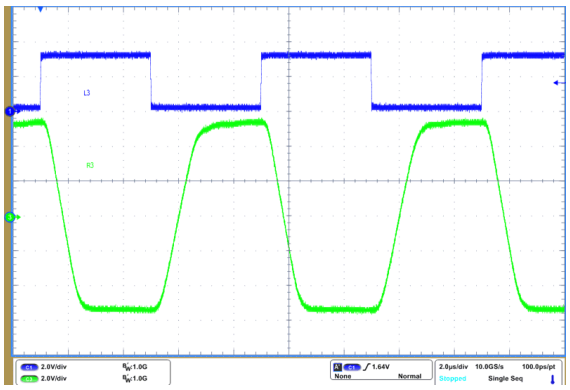
V_{CC} = 5V Bus Load = 5kΩ||2.5nF
250kbps SLR = V_{IO}

Figure 8-5. RS-232 Driver Waveform at 250kbps and V_{CC} = 5V



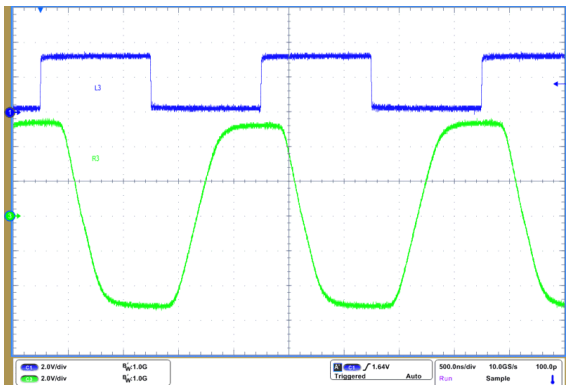
V_{CC} = 5V Bus Load = 5kΩ||1nF
1Mbps SLR = GND

Figure 8-6. RS-232 Driver Waveform at 1Mbps and V_{CC} = 5V



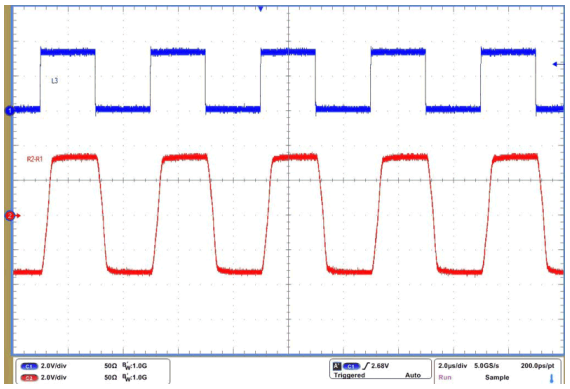
V_{CC} = 3.3V Bus Load = 5kΩ||2.5nF
250kbps SLR = V_{IO}

Figure 8-7. RS-232 Driver Waveform at 250kbps and V_{CC} = 3.3V



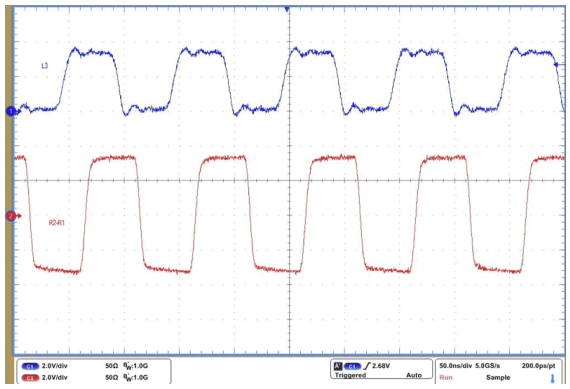
V_{CC} = 3.3V R_L = 5kΩ||1nF
1kbps SLR = GND

Figure 8-8. RS-232 Driver Waveform at 1Mbps and V_{CC} = 3.3V



V_{CC} = 5V Bus Load = 54Ω||50pF
SLR = V_{IO} Square wave at 500kbps

Figure 8-9. RS-485 Driver Waveform at 500 kbps and V_{CC} = 5V



V_{CC} = 5V Bus Load = 54Ω||50pF
SLR = GND Square wave at 20kbps

Figure 8-10. RS-485 Driver Waveform at 20 Mbps and V_{CC} = 5V

Copyright © 2024 Texas Instruments Incorporated

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a ceramic capacitor located as close to the supply pins as possible. Recommended bypass capacitor for V_{CC} is 1µF, for V_{IO} is 100nF, for V+, V- charge pump voltage supplies is 100nF. Besides this, two charge pump flying capacitors of 100nF each are needed between C1+, C1- terminals and between C2+, C2- terminals. For V_{CC} = 3.3V ±10%, V+ and V- voltages are regulated to +5.5V and -5.5V typically. If an application needs larger RS-232 output voltages, V_{CC} = 5V ± 10% is recommended because V+ and V- are regulated to ±9.5V.

8.4 Layout

8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices to protect against surge transients that may occur in industrial environments. THVD4411 has integrated IEC ESD and EFT protection. So if the application does not need IEC Surge protection, external transient protection may not be needed. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the external protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply decoupling capacitors as close as possible to the V_{CC}, V_{IO}, V+, V- pins of transceiver.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Optionally, use 1kΩ to 10kΩ pull-up and pull-down resistors for control lines to limit noise currents in these lines during transient events.

Copyright © 2024 Texas Instruments Incorporated

8.4.2 Layout Example

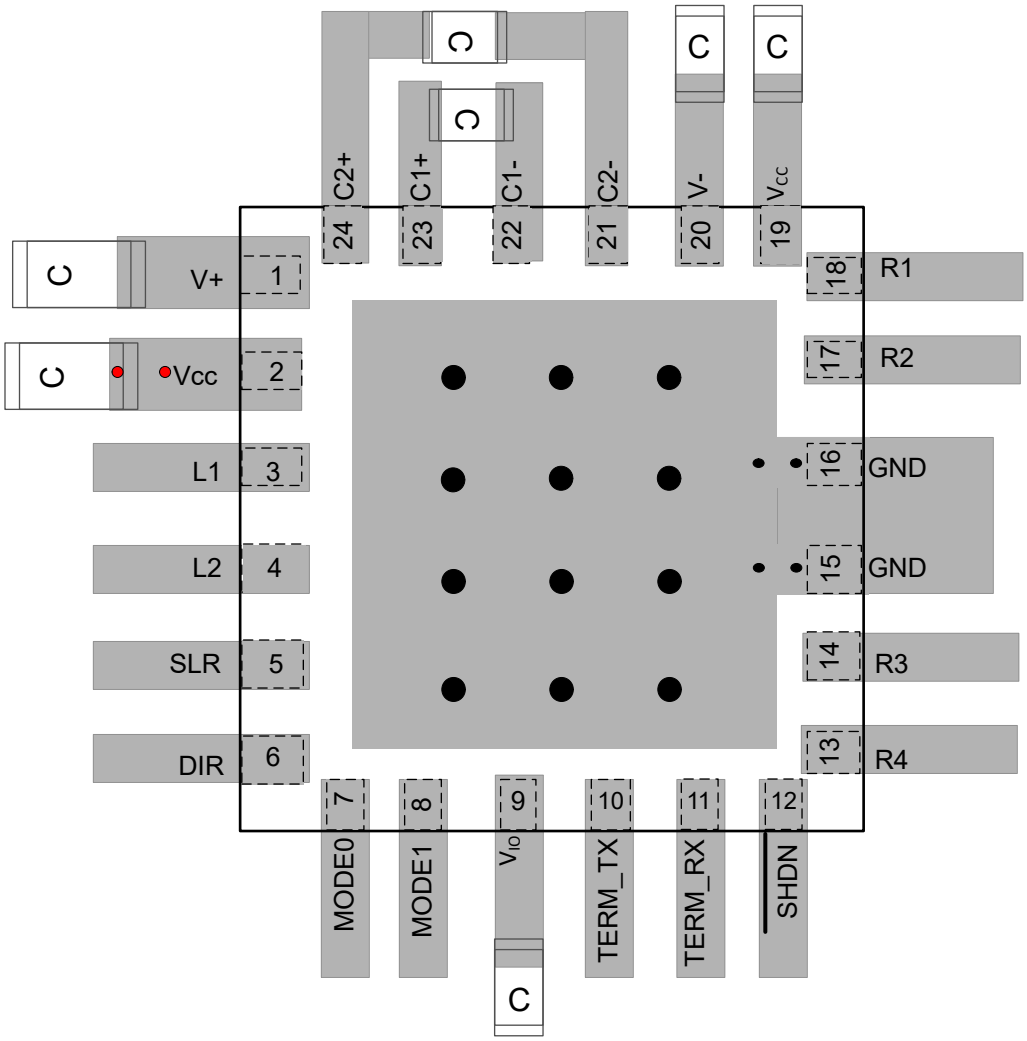


Figure 8-11. Layout Example

Copyright © 2024 Texas Instruments Incorporated

9 Device and Documentation Support

9.1 Device Support

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision * (April 2024) to Revision A (April 2024)	Page
• Added images cross references to the *Specification* tables	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2024 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD4411RGER	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	THVD 4411
THVD4411RGER.A	Active	Production	VQFN (RGE) | 24	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	THVD 4411

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

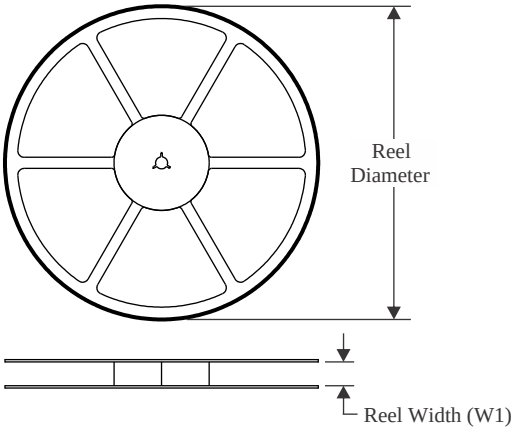
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

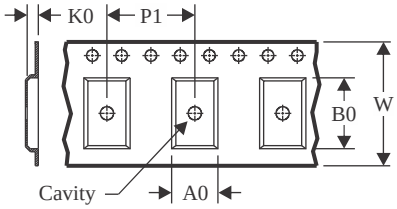
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

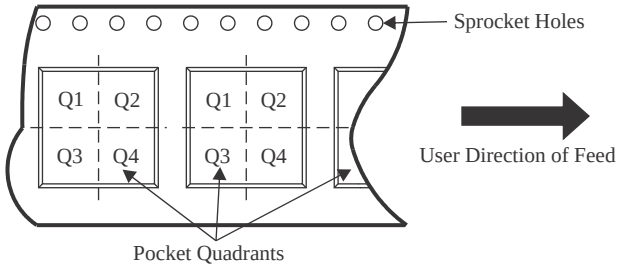


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

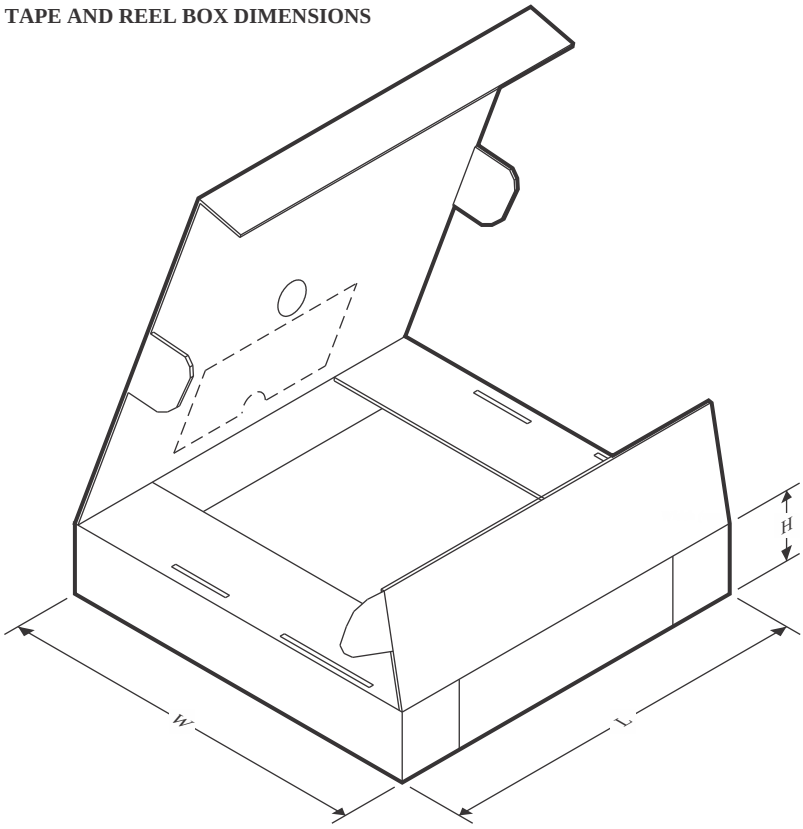
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD4411RGER	VQFN	RGE	24	5000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q2
THVD4411RGER	VQFN	RGE	24	5000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



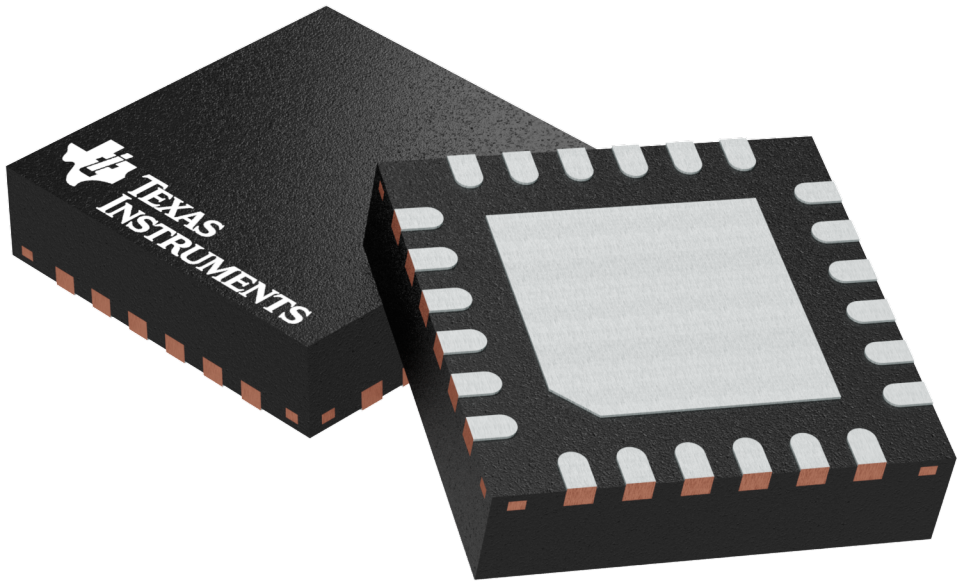
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD4411RGER	VQFN	RGE	24	5000	356.0	356.0	36.0
THVD4411RGER	VQFN	RGE	24	5000	360.0	360.0	36.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

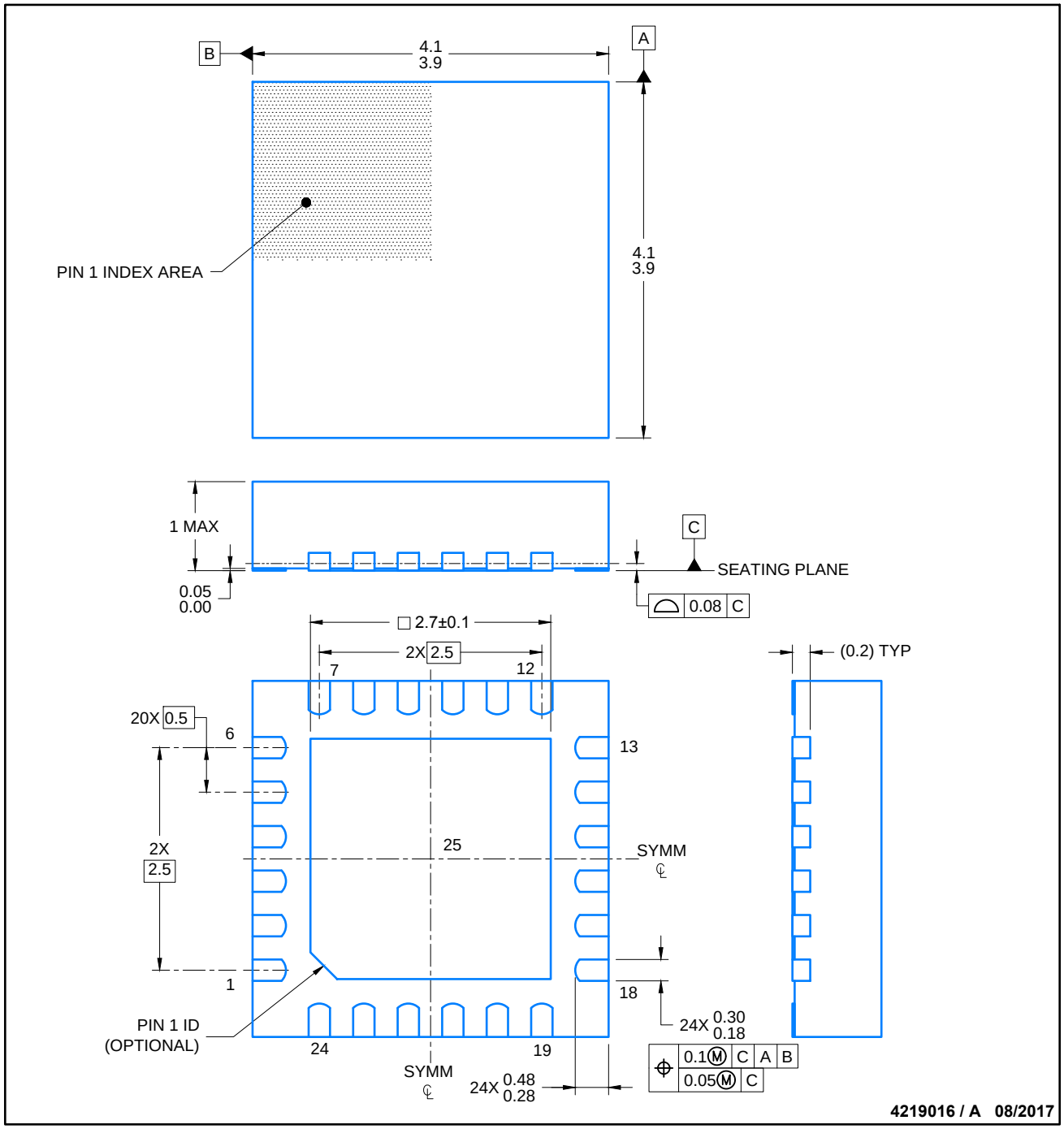
4204104/H

PACKAGE OUTLINE

RGE0024H

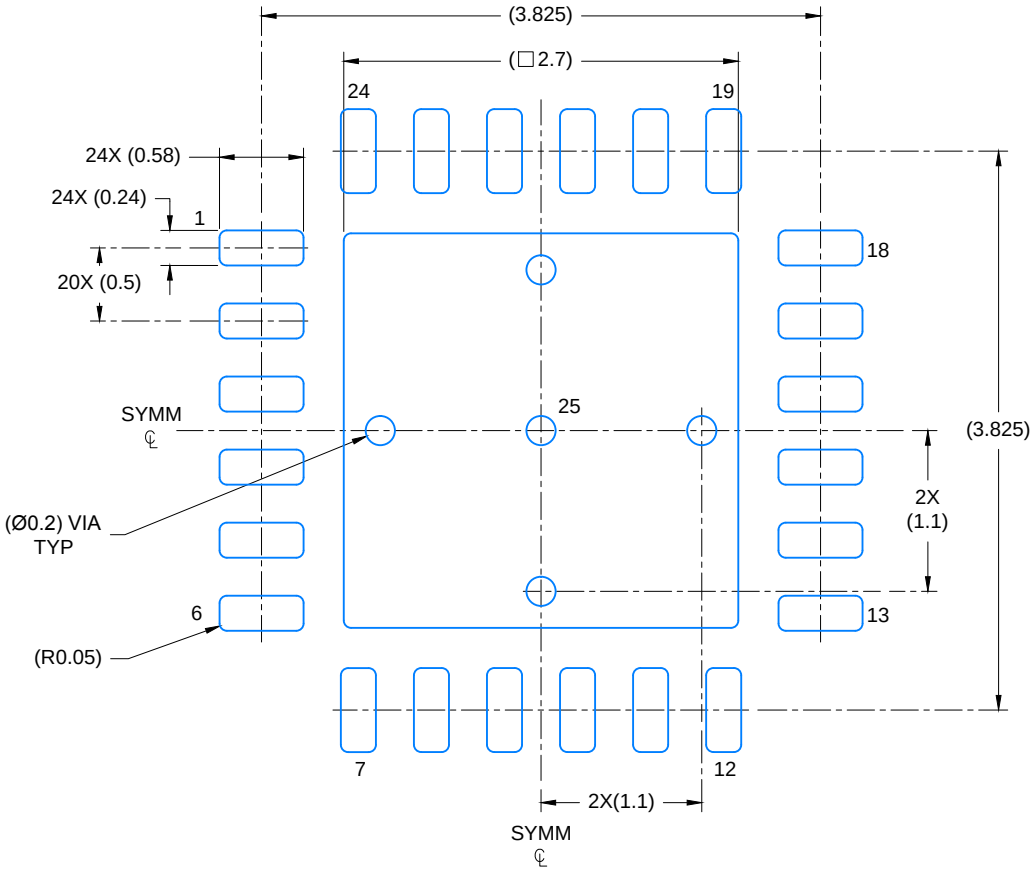
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



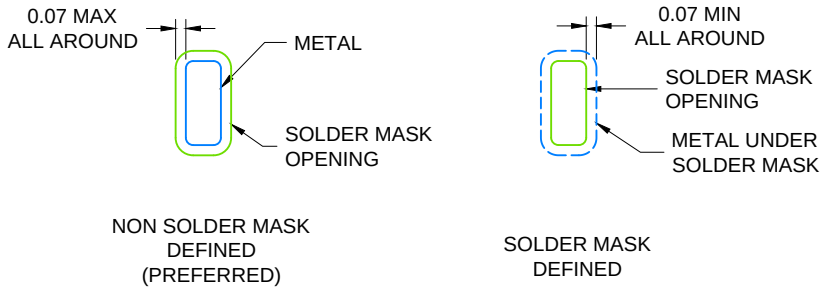
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

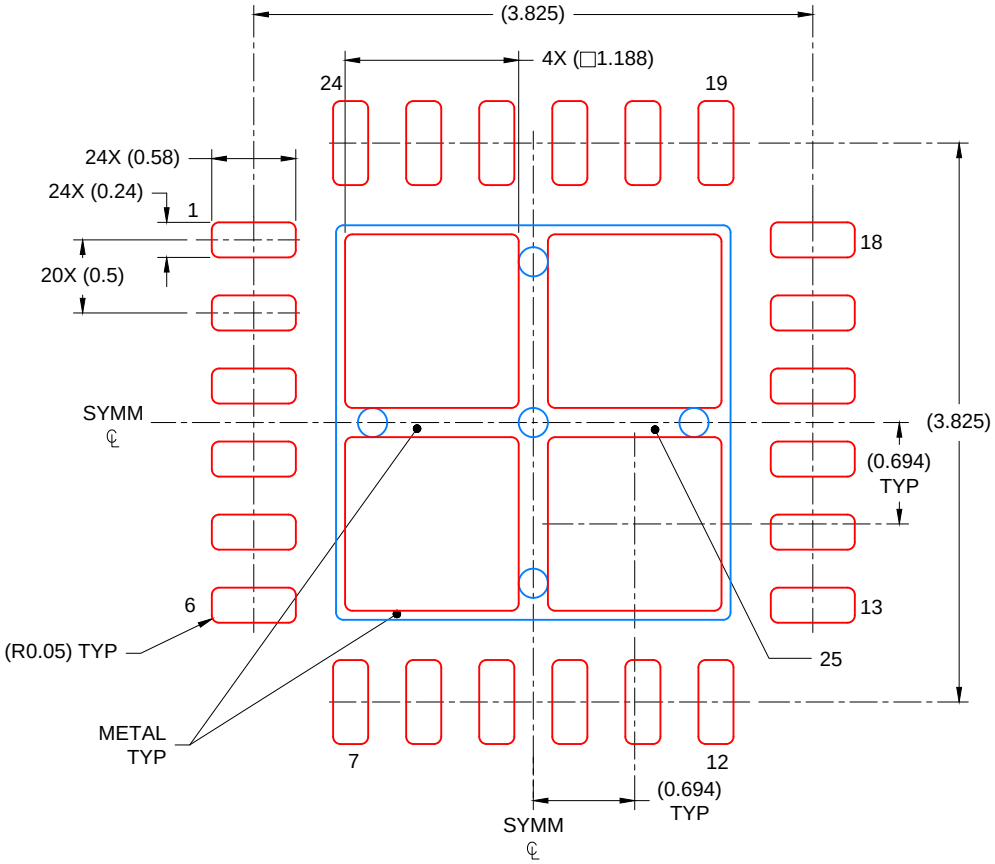


SOLDER MASK DETAILS

4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025