

TIOM2212 Dual Channel IO-Link Master With Integrated Frame Handler, Supply Controller and Diagnostics

1 Features

- Two independent IO-Link PHY channels
 - High performance C/Q driver: 1Ω $R_{DS(on)}$, up to 700mA DC
 - Configurable PNP, NPN, push-pull, or IO-Link 1.1.5 compliant output supporting IEC 61131-9 COM1, COM2, and COM3
- Integrated IO-Link frame handler simplifies board level signal routing, reducing need for UART
 - Offloads protocol-related processing from the microcontroller/processor
 - Supports up to 25MHz high-speed SPI with optional UART support
 - 1.8V to 5.5V I/O compatibility
 - Integrated diagnostics: overtemperature, overvoltage and undervoltage, C/Q & L+ overcurrent, reverse polarity
 - Hardware interrupt and reset pins
 - Integrated wake-up pulse generation and communication sequencer
 - Ready pulse detection for OSSDe compatibility
- Integrated gate drivers for external NFETs supporting both L+ and C/Q
 - Capable of driving >4A NFETs for actuator support
 - Capable of L+ and C/Q current sense feedback to external ADC
- Two outputs configurable to IEC61131-2 digital input channels (type 1 or type 3)
- Robust protection on all interface pins (C/Q, DI, L+, VCC, S, G, C/QG, C/QS)
 - $\pm 65V$ DC protection and $\pm 70V$ transient protection
 - Reverse polarity protection (C/Q and L+)
 - Reverse current blocking (C/Q and L+)
- 12 LED register controlled PWM drivers (6 per channel)

2 Applications

- Advanced and Standard IO-Link Modules
- [IO-link PHY in remote IO](#)
- OSSDe Light Curtains
- [Stand-alone remote IO](#)
- [Factory automation](#)
- [Process automation](#)

3 Description

The TIOM2212 dual channel IO-Link controller implements two independent IO-Link interfaces for industrial bidirectional, point-to-point communication with an integrated frame handler. The device can be connected to two IO-Link devices through a three-wire interface and integrates automatic wake-up pulse generation, communication sequencer, and ready pulse detection for simplified communication with IO-Link devices. The integrated frame handlers can be controlled via SPI, eliminating the need for external UARTs, but for legacy systems or non-standard frame sizes, a UART interface is available for maximum flexibility.

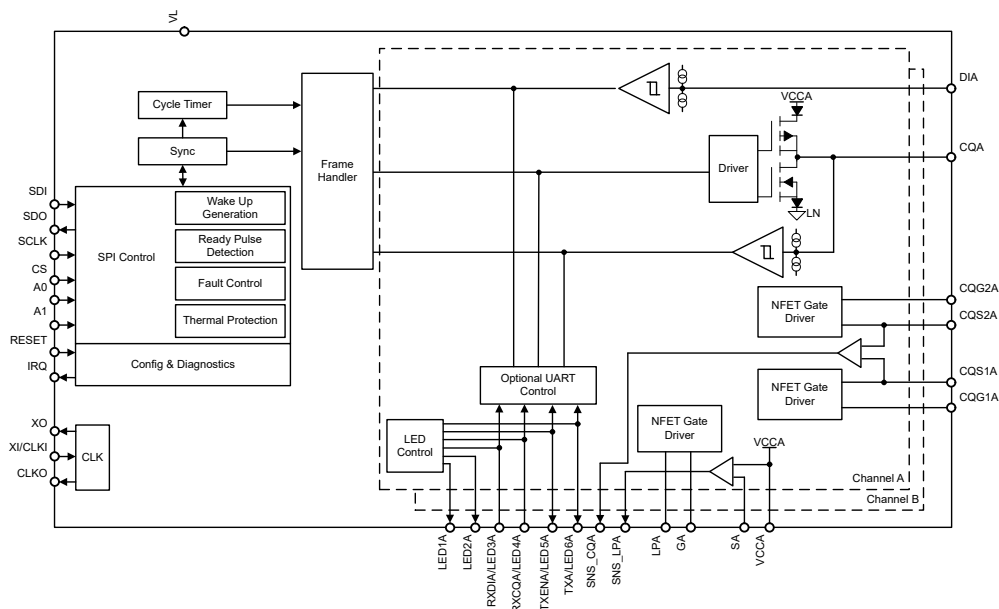
The TIOM2212 is designed to provide high flexibility and system-level integration for industrial automation. This device supports advanced status indications with integrated LED drivers, external NFET gate drivers for high-power L+ supply and C/Q device actuation, and configurable digital features for port synchronization and system monitoring. The device architecture also enables efficient, high-speed SPI communication for rapid data updates and maximum system integration.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TIOM2212	48, VQFN	7mm x 7mm

- (1) For all available packages, see [Section 11](#).
 (2) The package size (length × width) is a nominal value and includes pins, where applicable.





Device Block Diagram

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4 Pin Configuration and Functions

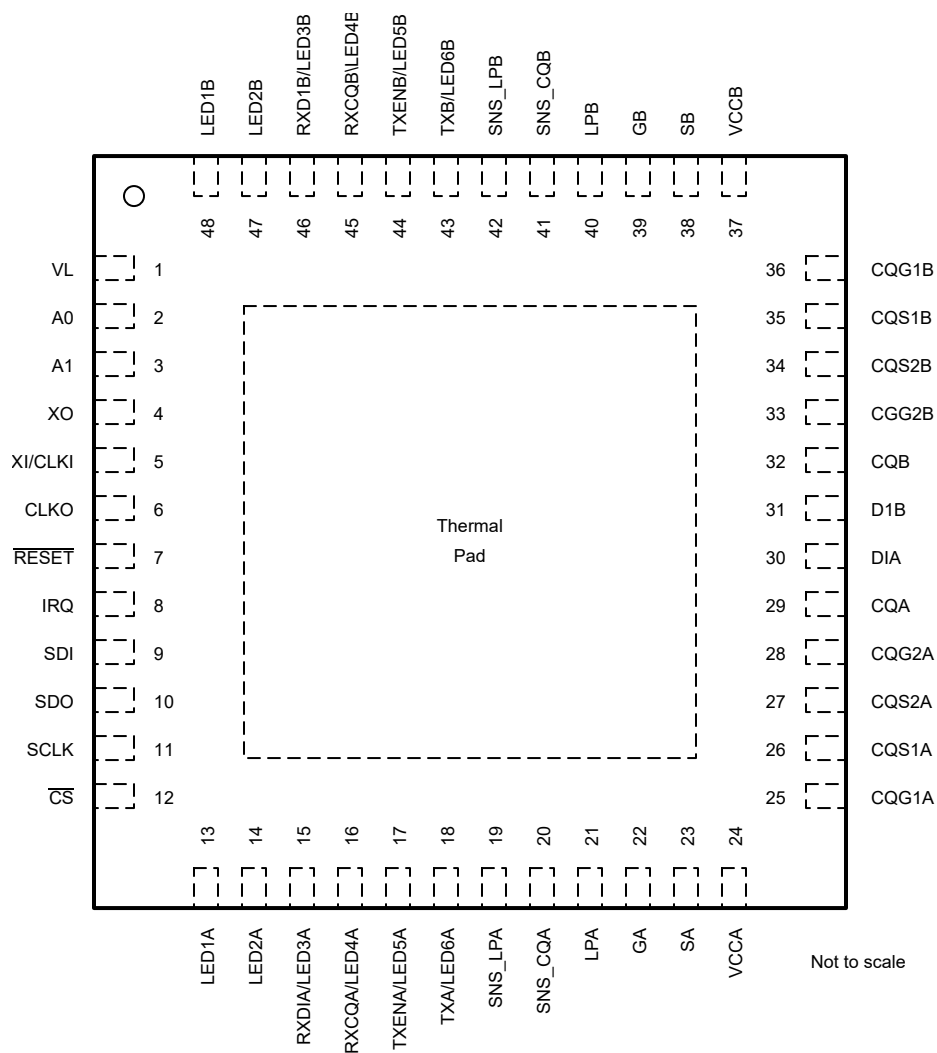


Figure 4-1. RGZ (VQFN) Package, 48 Pin (Top View)

Table 4-1. Pin Functions

PIN NO	PIN NAME	TYPE	DESCRIPTION
1	VL	Supply	1.71V-5.5V logic supply.
2	A0	I	Address input 0. Connect directly to VL or ground.
3	A1	I	Address input 1. Connect directly to VL or ground.
4	XO	O	Crystal oscillator input. Connect a crystal between XI and XO to use crystal clocking. Leave unconnected if using the internal clock.
5	XI/CLKI	I	Crystal oscillator input. Connect a crystal between XI and XO to use crystal clocking. Can also be configured as clock input from adjacent device on start-up.
6	CLKO	O	Internal clock out, connect to CLKI of the next device when using multiple. To reduce the need for multiple crystal oscillators.
7	RESET	I	Active-low hardware reset input. Connect to VL through a pull-up resistor.
8	IRQ	O	Active-low hardware interrupt output. Connect to VL through a pull-up resistor.
9	SDI	I	SPI Serial Data Input. Data is captured on the positive edge of SCLK.
10	SDO	O	SPI Serial Data Output. Data is shifted out on the negative edge of SCLK.
11	SCLK	I	SPI Clock Input.
12	CS	I	SPI Chip Select Pin (active low).
13	LED1A	O	Channel A LED driver. Connect a current limiting resistor in series.
14	LED2A	O	Channel A LED driver. Connect a current limiting resistor in series.
15	RXDIA/LED3A	O	Channel A DI receiver output / configurable LED driver. When used as RX, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
16	RXCQA/LED4A	O	Channel A C/Q receiver output / configurable LED driver. When used as RX, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
17	TXENA/LED5A	I	Channel A optional UART C/Q transmit enable / configurable LED driver. When used as TX enable, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
18	TXA/LED6A	I	Channel A optional UART C/Q transmit input / configurable LED driver. When used as TX input, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
19	SNS_LPA	O	Channel A L+ current sense output. Connect resistor to ground.
20	SNS_CQA	O	Channel A C/Q current sense output. Connect resistor to ground.
21	LPA	Supply	Power supply input (24V nominal) to the device. Connect 100Ω in series with L+. Connect 1μF capacitor to LM (ground) as close to the device as possible.
22	GA	O	Channel A external gate driver control for L+. Connect to gate of external NMOS for reverse current blocking and L+ control.
23	SA	I	Channel A sense input for external gate driver control on L+. Connect across shunt resistor with VCCA.
24	VCCA	Supply	Channel A VCC supply input. Connect 1μF capacitor to LM (ground) as close to the device as possible. Internally shorted to VCCB.
25	CQG1A	O	Channel A external gate driver control for C/Q HSS. Connect to gate of external NMOS FET to enable high current, C/Q drive.
26	CQS1A	I	Channel A sense input for external gate driver control on C/Q high-side switch (HSS). Connect across shunt resistor with CQS2.
27	CQS2A	I	Channel A sense input for external gate driver control on C/Q high-side switch. Connect across shunt resistor with CQS1.
28	CQG2A	O	Channel A external gate driver control for C/Q HSS. Connect to gate of external NMOS to enable high current C/Q drive.
29	CQA	I/O	Channel A transceiver input/output
30	DIA	I	Channel A digital input, connect a 100Ω resistor in series.
31	D1B	I	Channel B digital input, connect a 100Ω resistor in series.
32	CQB	I/O	Channel B transceiver input/output
33	CGG2B	O	Channel B external gate driver control for C/Q HSS. Connect to gate of external NMOS to enable high current, C/Q drive.
34	CQS2B	I	Channel B sense input for external gate driver control on C/Q HSS. Connect across shunt resistor with CQS1.
35	CQS1B	O	Channel B sense input for external gate driver control on C/Q HSS. Connect across shunt resistor with CQS2.
36	CQG1B	I	Channel B external gate driver control for C/Q HSS. Connect to gate of external NMOS to enable high current C/Q drive.

Table 4-1. Pin Functions (continued)

PIN NO	PIN NAME	TYPE	DESCRIPTION
37	VCCB	Supply	Channel B VCC supply input. Connect 1µF capacitor to LM (ground) as close to the device as possible. Internally shorted to VCCA
38	SB	I	Channel B sense input for external gate driver control on L+. Connect across shunt resistor with VCCA.
39	GB	O	Channel B external gate driver control for L+. Connect to gate of external NMOS for reverse current blocking and L+ control.
40	LPB	Supply	Power supply input (24V nominal) to the device. Connect 100Ω in series with L+. Connect 1µF capacitor to LM (ground) as close to the device as possible.
41	SNS_CQB	O	Channel B C/Q current sense output. Connect resistor to ground.
42	SNS_LPB	O	Channel B L+ current sense output. Connect resistor to ground.
43	TXB/LED6B	I	Channel B optional UART C/Q transmit input / configurable LED driver. When used as TX input, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
44	TXENB/LED5B	I	Channel B optional UART C/Q transmit enable / configurable LED driver. When used as TX enable, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
45	RXCQB/LED4B	O	Channel B C/Q receiver output / configurable LED driver. When used as RX, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
46	RXD1B/LED3B	O	Channel B DI receiver output / configurable LED driver. When used as RX, connect to micro-controller as part of optional UART control. When used as LED driver, connect a current limiting resistor in series.
47	LED2B	O	Channel B LED driver. Connect a current limiting resistor in series.
48	LED1B	O	Channel B LED driver. Connect a current limiting resistor in series.
–	Thermal Pad	GND	Connect to L- for maximum thermal and electrical performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
LPA, CQA, DIA, LPB, CQB, DIB	Bus pins steady state voltage	–65	65	V
	Bus pins transient pulse width < 100 μ s	–70	70	V
VCCA, VCCB, SA, SB	Supply pins steady state voltage	–0.3	65	V
	Supply pins transient pulse width < 100 μ s	–0.3	70	V
$V_{(SA)} - V_{(VCCA)}$, $V_{(SB)} - V_{(VCCB)}$	Voltage across sense resistor	–0.3	0.3	V
GA, GB, CQG1A, CQG1B, CQG2A, CQG2B	Gate driver output voltage	–65	65	V
CQS1A, CQS1B, CQS2A, CQS2B	HSS sense pins	–65	65	V
$ V_{(BUS1)} - V_{(BUS2)} $	Voltage drop between any combination of bus pins		65	V
$V_{(VCCA,B)} - V_{(BUS)}$	Voltage drop between supply and any bus pins	–65	65	V
$ V_{(GA)} - V_{(LPA)} $, $ V_{(GB)} - V_{(LPB)} $	NFET gate - source voltage	–0.3	14	V
$ V_{(CQG1A)} - V_{(CQS1A)} $, $ V_{(CQG2A)} - V_{(CQS2A)} $, $ V_{(CQG1B)} - V_{(CQS1B)} $, $ V_{(CQG2B)} - V_{(CQS2B)} $	NFET gate - source voltage	–0.3	14	V
$V_{(CQA)} - V_{(CQS1A)}$, $V_{(CQA)} - V_{(CQS2A)}$, $V_{(CQB)} - V_{(CQS1B)}$, $V_{(CQB)} - V_{(CQS2B)}$	CQ to HSS sense pin voltage	–1	65	V
V_L	Logic supply voltage	–0.3	6	V
TXA, TXB, TXENA, TXENB, RXDIA, RXCQA, RXDIB, RXCQB, SDI, SDO, SCK, $\overline{CS}$, XO, XI, CLKI, CLKO, IRQ, A0, A1, LED*	Logic pin voltage	–0.3	$\min(V_L + 0.3, 6)$	V
Output current	RXCQA, RXDIA, RXCQB, RXDIA, SDO, CLKO, IRQ	–5	5	mA
Output current	SNS_CQA, SNS_CQB, SNS_LPA, SNS_LPB	–10	2	mA
Continuous current	LM, VCCA,B	–2	2	A
Continuous current	CQA, CQB	–1	1	A
Storage temperature, T_{stg}		–55	170	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime. All voltages are with reference to the L- pin, unless otherwise specified.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins	± 2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	All pins	± 750	V

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{(VCCA,B)}$	24V Input Supply Voltage	7	24	36	V
$V_{(VL)}$	Logic Supply Voltage	1.71	3.3	5.5	V
$V_{(I)}$	Logic level input voltage at TXA, TXB, TXENA, TXENB, SDI, $\overline{CS}$, CLKI			VL	V
t_{RESETB}	Minimum pulse width on RESETB		300		μ s
$1/t_{BIT}$	Data rate (Communication mode)			250	kbps
T_A	Operating ambient temperature	–40		125	°C
T_{J-ET}	Extended Junction temperature for -ET/-EP readiness	–55		150	°C
T_J	Junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TIOL1221	UNIT
		RGZ (48 Pins)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at $V_{CC} = 24V$, $V_L = 5V$ and $T_A = 25^\circ C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VCCA,B)							
I _(VCC-SHDN)	Supply quiescent current in shutdown mode	All TX, RX, Gate drivers HiZ. FETs not installed for LP and HSS. No load at CQ or LP. Sink/Source disabled.			2.5	4.7	mA
I _(VCC-RX-ONLY)	Supply current when only inputs are enabled	TX disabled, RX enabled, Gate drivers HiZ. FETs not installed for LP and HSS. No load at CQ or LP. Sink/Source disabled.			2.5	4.7	mA
I _(VCC-SHDN)	Supply quiescent current in shutdown mode	All TX, RX, Gate drivers disabled. FETs installed for LP and HSS. No load at CQ or LP. Sink/Source disabled.	All TX, RX, Gate drivers HiZ. FETs not installed for LP and HSS.		3.6	6	mA
I _(VCC-CQ)	Quiescent supply current in enabled condition	All TX, RX, and LP gate driver enabled. HSS gate driver disabled. FETs installed for LP and HSS. No load at CQ or LP. Sink/Source disabled.			1.5	2	mA

5.5 Electrical Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 5V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _(VCC-OVLO,R)	VCC over voltage warning	VCC rising	VCC rising			48	V
V _(VCC-OVLO,F)	VCC over voltage warning	VCC falling	VCC falling	40			V
V _(VCC-OVLO,HYS)	VCC over voltage hysteresis	Rising to falling threshold	Rising to falling threshold		550		mV
V _(VCC-UVLO)	VCC under voltage lockout	VCC falling		5.6	6		V
V _(VCC-UVLO)	VCC under voltage lockout	VCC rising			6.2	6.8	V
V _(VCC-UVLO,HYS)	VCC under voltage hysteresis	Rising to falling threshold		150	210		mV
V _(VCCW)	VCC undervoltage warning	VCC falling		16		18	V
V _(VCCW-HYS)	VCC undervoltage warning hysteresis	Rising to falling threshold			530		mV
VL							
V _(VL-UVLO,F)	Falling UVLO level for VL	VL Falling		1.3			V
V _(VL-UVLO,R)	Rising UVLO level for VL	VL Rising				1.6	V
V _(VL-UVLO,HYS)	VL UVLO hysteresis				0.1		V
I _(VL)	Input supply current at VL	All enabled			2.7		mA
POWER SUPPLIES (LPA,B)							
V _(G1-LP)	Gate to source (LP) voltage			7.5		13	V
V _{ILP_DET}	Over-current detection threshold	Rising threshold	LP_CFG0[4:3]=3h	100	120	140	mV
			LP_CFG0[4:3]=2h	50	60	70	mV
			LP_CFG0[4:3]=1h	25	30	35	mV
			LP_CFG0[4:3]=0h	12.5	15	17.5	mV
GM _{SNS,LP}	Transconductance of current sense output		LP_CFG0[4:3]=0h		300		mS
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 10mV			3		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 5mV			1.5		mA
A _{SNS}	Accuracy of current sense			-40		40	%
GM _{SNS,LP}	Transconductance of current sense output		LP_CFG0[4:3]=1h		150		mS
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 20mV			3		mA
A _{SNS}	Accuracy of current sense			-10		10	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 10mV			1.5		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 5mV			0.75		mA
A _{SNS}	Accuracy of current sense			-40		40	%

5.5 Electrical Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 5V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
GM _{SNS,LP}	Transconductance of current sense output				75		mS
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 40mV	LP_CFG0[4:3]= 2h		3		mA
A _{SNS}	Accuracy of current sense			-5		5	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 20mV			1.5		mA
A _{SNS}	Accuracy of current sense			-10		10	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 10mV			0.75		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 5mV			0.375		mA
A _{SNS}	Accuracy of current sense			-40		40	%
GM _{SNS,LP}	Transconductance of current sense output		LP_CFG0[4:3]= 3h		37.5		mS
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 80mV			3		mA
A _{SNS}	Accuracy of current sense			-5		5	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 40mV			1.5		mA
A _{SNS}	Accuracy of current sense			-5		5	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 20mV			0.75		mA
A _{SNS}	Accuracy of current sense			-10		10	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 10mV			0.375		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(VCCA) - V _(SA) , V _(VCCB) -V _(SB) = 5mV			0.1875		mA
A _{SNS}	Accuracy of current sense			-40		40	%
I _{SNS,HR}	Headroom needed for current sense functionality	V _(VL) - V _(VSNS,LP) , I _{SNS} = 3mA		0.6			V
I _{SNS,HIZ}	Leakage current through SNS_LPA,B pins	V _(VSNS,LP) = V _(VL) , 0				20	μA
I _{SN}	SN input current					50	μA
I _{LP}	LP input current					30	μA
V _(LP-WARN)	LP under voltage warn	LP falling		18			V
V _(LP-WARN)	LP under voltage warn	LP rising				20	V
V _(LP-UVLO,HYS)	LP under voltage hysteresis	Rising to falling threshold			540		mV
V _(LP_BLK_VTH)	LP dynamic blanking threshold	V _(VCC) > 18V	LP_DYBL_EN = 0b1		6.2		V
C _{GATE}	External NFET gate capacitance				1		nF
DRIVER OUTPUT (CQA, CQB)							
R _{DSON-HS}	High-side driver on-resistance	I _{LOAD} = 200mA, Current Limit = 500mA			1	2	Ω
R _{DSON-LS}	Low-side driver on-resistance	I _{LOAD} = 200mA, Current Limit = 500mA			1	2	Ω

5.5 Electrical Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 5V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I _{O(LIM)}	Driver output current limit	V _(DRIVER) = (V _{VCC} - 3) V or 3V,	CQ_DRV_CFG[4:3] = 3h	100	150	195	mA
			CQ_DRV_CFG[4:3] = 2h	200	230	330	mA
			CQ_DRV_CFG[4:3] = 1h	300	350	485	mA
			CQ_DRV_CFG[4:3] = 0h	500	600		mA
I _{OZ(CQ)}	CQ leakage	0 ≤ V _(CQ) ≤ (V _{VCC} - 0.1V)	Driver disabled, pull up/down disabled, RX enabled	-115		2	μA
I _{IN-CQ}	CQ Input current	Driver disabled, pull up/down disabled	-5V ≤ V _{CQ} ≤ VCC+5V	-150		10	μA
I _{LLM(CQ)}	CQ current sink	V _(CQ) ≥ 5V, CQ_SNK_EN = 0b1, CQ_SCR_EN = 0b0	5mA Sink (CQ_SRC_SNK = 0b00)	5	7.5	10	mA
I _{LLM(CQ)}			2mA Sink (CQ_SRC_SNK = 0b01)	2	3	4	mA
I _{LLM(CQ)}	CQ current source	V _(VCC-CQ) ≥ 5V, CQ_SRC_EN = 0b1, CQ_SNK_EN = 0b0	5mA Sink (CQ_SRC_SNK = 0b00)	-10	-7.5	-5	mA
I _{LLM(CQ)}			2mA Sink (CQ_SRC_SNK = 0b01)	-4	-3	-2	mA
I _{PU-CQ}	CQ driver weak pull-up current	Driver disabled, Weak pull-up enabled, CQ_SRC_EN = 0b1, CQ_SNK_EN = 0b0	0 ≤ V _(CQ) ≤ (V _{VCC} - 5V), CQ_SRC_SNK = 0b10	-310		-150	μA
I _{PD-CQ}	CQ driver weak pull-down current	Driver disabled, Weak pull-down enabled, CQ_SNK_EN = 0b1, CQ_SCR_EN = 0b0	5 ≤ V _(CQ) ≤ V _{VCC} , CQ_SRC_SNK = 0b10	150		300	μA
C _{IN-CQ}	CQ input capacitance	CQ driver disabled, pull-up/pull-down disabled, f = 100kHz			130		pF
RECEIVER INPUT (CQA, DIA, CQB, DIB)							
V _(THH)	Input threshold "H"	V _(LP) > 18V, RX Enabled, RX config - IOLINK_standard, type 1	CQ_CFG[2:1] = 0h; CQ_DRV_DI_CFG[2:1] = 0h	10.5		13	V
V _(THL)	Input threshold "L"			8		11.5	V
V _(HYS)	Receiver Hysteresis (V _(THH) - V _(THL))				2.5		V

5.5 Electrical Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 5V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _(THH)	Input threshold “H”	V _(LP) > 18V, RX Enabled, RX config - ratiometric	CQ_CFG[2:1] = 1h; CQ_DRV_DI_C FG[2:1] = 1h	10.5		13	V	
V _(THL)	Input threshold “L”			8		11.5	V	
V _(HYS)	Receiver Hysteresis (V _(THH) - V _(THL))			2.5			V	
V _(THH)	Input threshold “H”	V _(LP) = 17V, RX Enabled, RX config - ratiometric		10.5		13	V	
V _(THH)	Input threshold “H”	V _(LP) = 12V, RX Enabled, RX config - ratiometric		7.5		9.4	V	
V _(THH)	Input threshold “H”	V _(LP) = 7V, RX Enabled, RX config - ratiometric		4.4		5.8	V	
V _(THH)	Input threshold “H”	V _(LP) < 18V, RX Enabled, RX config - ratiometric		See Note (1)		See Note (2)	V	
V _(THL)	Input threshold “L”	V _(LP) = 17V, RX Enabled, RX config - ratiometric		8		11.5	V	
V _(THL)	Input threshold “L”	V _(LP) = 12V, RX Enabled, RX config - ratiometric		5.8		8.5	V	
V _(THL)	Input threshold “L”	V _(LP) = 7V, RX Enabled, RX config - ratiometric		3.6		5.4	V	
V _(THL)	Input threshold “L”	V _(LP) < 18V, RX Enabled, RX config - ratiometric		See Note (3)		See Note (4)	V	
V _(HYS)	Receiver Hysteresis (V _(THH) - V _(THL))	V _(LP) < 18V, RX Enabled, RX config - ratiometric		1.8			V	
V _(THH)	Input threshold “H”	V _(LP) > 18V, RX Enabled, RX config - type 2/3		CQ_CFG[2:1] = 2h; CQ_DRV_DI_C FG[2:1] = 2h	7.5		11	V
V _(THL)	Input threshold “L”			6		8	V	
V _(HYS)	Receiver Hysteresis (V _(THH) - V _(THL))			1.8			V	
C _{IN-DI}	DI input capacitance	f =100kHz		14			pF	
I _{LLM(DI)}	DI current sink	V _(DI) >= 5V	DI_SNK_EN = 0b1, DI_SRC_EN = 0b0	2	3	4	mA	
I _{LLM(DI)}	DI current source	V _(DI) >= 5V	DI_SNK_EN = 0b0, DI_SRC_EN = 0b1	−4	−3	−2	mA	
I _{IN-DI}	DI Input current	DI receiver enabled, pull up/ down disabled	-1V <= V _{DI} <= V _(LP) +1V	−5		50	μA	
LOGIC-LEVEL INPUTS (CS̄, SCK, SDI, TXENA, TXA, TXENA, ENB, TXB, TXENB, CLKI)								
V _{IH}	Input logic high voltage			0.7*VL			V	
V _{IL}	Input logic low voltage			0.3*VL			V	
I _{IN}	Input leakage current	V _I = 0V or VL		−6		6	μA	
LOGIC-LEVEL OUTPUTS (IRQ̄, SDO, RXCQA, RXCQB, CLKO, RXDIA, RXDIB)								
V _{OH}	Output logic high voltage	I _O = 4mA	I _O = 4mA	VL−0.4			V	
V _{OL}	Output logic low voltage	I _O = 4mA		0.4			V	
I _{OZ}	Output high impedance leakage	Output in Hi-Z, V _O = 0V or VL		−1		1	μA	
PROTECTION CIRCUITS								

5.5 Electrical Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 5V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T _(WRN)	Thermal warning	Die temperature T _J		125			°C
T _(SDN)	Thermal shutdown			150	180		°C
T _(HYS)	Thermal hysteresis for shutdown			8			°C
T _(WRN)	Thermal hysteresis for warning	Die temperature T _J		8.5			°C
I _{REV}	CQ, DI Leakage current in reverse polarity (Drivers disabled, pull up/down disabled, HSS G1/G2 disabled - FET not installed on board)	VCC= 24V V _(CQ/DI) = (V _(VCC) -36V) OR V _(CQ/DI) = (V _(VCC) +36V)		-115		185	μA
		VCC= 24V V _(CQ/DI) = (V _(VCC) -65V) OR V _(CQ/DI) = 65V		-300		200	μA
	CQ (Drivers enabled, pull up/down disabled, HSS G1/G2 disabled - FET not installed on board)	V _(CQ to VCC) > 0V, NSIDE OFF, PSIDE ON				310	μA
		V _(CQ to LM) < 0V, PSIDE OFF, NSIDE ON		-350		-160	μA
CRYSTAL OSCILLATOR							
F _(XTAL)	Crystal frequency			14.7456			MHz
I _(XTAL)	Crystal oscillator current	VL current increase if crystal oscillator is used	XTAL_EN=0b1	400	675		μA
ESR _(XTAL)	Equivalent crystal oscillator resistance	f _{XTAL} = 14.7456MHz				100	Ω
CS _(XTAL)	Crystal shunt capacitance	f _{XTAL} = 14.7456MHz				8	pF
CIN _(XO,XI)	Pin input capacitance			10			pF
INTERNAL OSCILLATOR							
I _(OSC)	Internal oscillator current	VL current increase if internal oscillator is used				320	μA
EXTERNAL CLOCK							
D _(EXT)	External clock duty cycle			42		58	%
F _(EXT)	External clock frequency			3.686			MHz
LED							
F _(PWM)	PWM frequency			225			Hz
DU_CY	Duty cycle			1		100	%
I _{OUT}	LED output current			2		20	mA
I _{OUT_ACC}	LED output current accuracy			-25		25	%
HSS DRIVER (CQA,B)							
V _(CQG1-CQS1) , V _(CQG2-CQS2)	Gate to source voltage, NFET mode			7.5		13	V
V _{IHSS_REG_G2}	Regulated forward threshold	V _(CQA,B) - V _(CQS2A,B)		2	30	58	mV
V _{IHSS_REV_G2}	Reverse-current blocking threshold	V _(CQS2A,B) - V _(CQA,B)		-58	-30	-2	mV

5.5 Electrical Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 5V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IHSS_DET}	Over-current detection threshold	Rising threshold	HSS_CFG0[4:3] J= 3h	100	120	140	mV
			HSS_CFG0[4:3] J= 2h	50	60	70	mV
			HSS_CFG0[4:3] J= 1h	25	30	35	mV
			HSS_CFG0[4:3] J= 0h	12.5	15	17.5	mV
GM _{SNS,HSS}	Transconductance of HSS current sense output				300		mS
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 10mV	HSS_CFG0[4:3] J= 0h		3		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 5mV			1.5		mA
A _{SNS}	Accuracy of current sense			-40		40	%
GM _{SNS,HSS}	Transconductance of current sense output				150		mS
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 20mV	HSS_CFG0[4:3] J= 1h		3		mA
A _{SNS}	Accuracy of current sense			-10		10	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 10mV			1.5		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 5mV			0.75		mA
A _{SNS}	Accuracy of current sense			-40		40	%
GM _{SNS,HSS}	Transconductance of current sense output				75		mS
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 40mV			3		mA
A _{SNS}	Accuracy of current sense		HSS_CFG0[4:3] J= 2h	-5		5	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 20mV			1.5		mA
A _{SNS}	Accuracy of current sense			-10		10	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 10mV			0.75		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 5mV			0.375		mA
A _{SNS}	Accuracy of current sense			-40		40	%
GM _{SNS,HSS}	Transconductance of current sense output				37.5		mS
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 80mV	HSS_CFG0[4:3] J= 3h		3		mA
A _{SNS}	Accuracy of current sense			-5		5	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 40mV			1.5		mA
A _{SNS}	Accuracy of current sense			-5		5	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 20mV			0.75		mA
A _{SNS}	Accuracy of current sense			-10		10	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 10mV			0.375		mA
A _{SNS}	Accuracy of current sense			-20		20	%
I _{SNS}	Current sense current	V _(CQS1A) - V _(CQS2A) , V _(CQS1B) - V _(CQS2B) = 5mV			0.1875		mA
A _{SNS}	Accuracy of current sense			-40		40	%
I _{SNS,HR}	Headroom needed for current sense functionality	V _(VL) - V _(VSNS,HSS) , I _{SNS} = 3mA		0.6			V

5.5 Electrical Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 5V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISNS,HIZ	Leakage current through SNS_CQA,B pins	$V_{(V_{SNS,HSS})} = V_{(V_L)}$, 0				20	μA
ICQS1, ICQS2	CQS1, CQS2 input current	HSS driver is enabled; $V_{(CQS1)} = V_{(CQS2)}$	HSS_GATE_DR V_EN = 0b1			100	μA
ICQ	CQ input current	HSS driver is enabled	HSS_GATE_DR V_EN = 0b1			30	μA
V(HSS_BLK_VTH)	HSS dynamic blanking threshold		HSS_DYBL_EN = 0b1		6.8		V
CGATE	External NFET gate capacitance				1		nF

- (1) $V_{THH} (min) = 5V + (11/18) [V_{(LP)} - 8V]$
- (2) $V_{THH} (max) = 6.5V + (13/18) [V_{(LP)} - 8V]$
- (3) $V_{THL} (min) = 4V + (8/18) [V_{(LP)} - 8V]$
- (4) $V_{THL} (max) = 6V + (11/18) [V_{(LP)} - 8V]$

5.6 Switching Characteristics

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 3.3V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CQ DRIVER						
t _{PLH}	Driver propagation delay, low-to-high transition	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R _L = 2kΩ C _L = 5nF Push-pull and PNP configuration CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00		800	1200	ns
t _{PHL}	Driver propagation delay, high-to-low transition	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R _L = 2kΩ C _L = 5nF Push-pull and NPN configuration CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00		800	1200	ns
t _{P(skew)}	Driver propagation delay skew. t _{PLH} - t _{PHL}	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R _L = 2kΩ C _L = 5nF Push-pull configuration CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00		120		ns
t _{PZH}	Driver enable delay high	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R _L = 2kΩ C _L = 5nF Push-pull and PNP configuration only CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00			4	μs

5.6 Switching Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 3.3V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PZL}	Driver enable delay low	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R _L = 2kΩ C _L = 5nF Push-pull and NPN configuration only CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00			4	μs
t _{PHZ}	Driver disable delay high	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R _L = 2kΩ C _L = 5nF Push-pull and PNP configuration only CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00			4	μs
t _{PLZ}	Driver disable delay low	See Test Circuit for Driver Output Measurements and Driver Enable/Disable Timing Diagrams R _L = 2kΩ C _L = 5nF Push-pull and NPN configuration only CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00			4	μs
t _r	Driver output rise time	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R _L = 2kΩ C _L = 5nF Push-pull and PNP configuration CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00	0.25	0.55	0.86	μs
t _f	Driver output fall time	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R _L = 2kΩ C _L = 5nF Push-pull and NPN configuration CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00	0.25	0.55	0.86	μs
t _r – t _f	Difference in rise and fall time	See Test Circuit for Driver Output Measurements and Driver Output Switching Waveforms R _L = 2kΩ C _L = 5nF Push-pull configuration only CQ_DRV_DI_CFG[7:6] = 2b'00 CQ_DRV_CFG[4:3] = 2b'00		50		ns
t _{AR}	Auto retry time after current limit	CQ_DRV_CFG[2:1] = 0h		50		ms
t _{AR}	Auto retry time after current limit	CQ_DRV_CFG[2:1] = 1h		0.5		s
t _{AR}	Auto retry time after current limit	CQ_DRV_CFG[2:1] = 2h		4		s
t _{AR}	Auto retry time after current limit	CQ_DRV_CFG[2:1] = 3h		10		s
t _{SC}	Current limit blanking time	CQ_DRV_CFG[6:5] = 0h	5	5.5		ms
t _{SC}	Current limit blanking time	CQ_DRV_CFG[6:5] = 1h	15	16.5		ms
t _{SC}	Current limit blanking time	CQ_DRV_CFG[6:5] = 2h	50	55		ms

5.6 Switching Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 3.3V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t _{SC}	Current limit blanking time	CQ_DRV_CFG[6:5] = 3h		150	165		ms
t _(UVLO)	CQ re-enable delay after VCC UVLO (1)	VL is powered on. VCC is powering up.				0.05	ms
CQ, DI RECEIVER							
t _{PLH_CQ} , t _{PHL_CQ}	CQ Receiver propagation delay	C _L =15pF	CQ_GFILT_EN=1b0		0.3	0.8	μs
			CQ_GFILT_EN=1b1		1.5	2.4	μs
				300	ns		
t _{PLH_DI} , t _{PHL_DI}	DI Receiver propagation delay		DI_GFILT_EN=1b0		1.3	2	μs
			DI_GFILT_EN=1b1		2.3	3.8	μs
t _{P(skew)}	Receiver propagation delay skew. t _{PLH_DI} - t _{PHL_DI}					800	ns
WAKE TIMING							
t _{WU-DEL}	Delay time to wake up pulse					80	μs
t _{WU}	Wake up pulse duration			75	80	85	μs
t _{WU-DIS}	Delay in turning off the driver after wake up pulse				2		μs
LP TIMING							
t _{ON}	Time to turn on NFET	C _{GATE} =1nF			0.17		ms
t _{OFF}	Time to turn off NFET	C _{GATE} =1nF			10		μs
t _{SC}	Current limit blanking time	LP_CFG0[6:5] = 0h		5	5.5		ms
		LP_CFG0[6:5] = 1h		15	16.5		ms
		LP_CFG0[6:5] = 2h		50	55		ms
		LP_CFG0[6:5] = 3h		150	165		ms
t _{AR}	Auto retry time after current limit	LP_CFG0[2:1] = 0h			50		ms
		LP_CFG0[2:1] = 1h			0.5		s
		LP_CFG0[2:1] = 2h			4		s
		LP_CFG0[2:1] = 3h			10		s
CQ HSS TIMING							
t _{OFF}	Time to turn off NFET	C _{GATE} =1nF			4		μs
t _{ON}	Time to turn on NFET	C _{GATE} =1nF			0.15		ms
t _{SC}	Current limit blanking time	HSS_CFG0[6:5] = 0h		5	5.5		ms
		HSS_CFG0[6:5] = 1h		15	16.5		ms
		HSS_CFG0[6:5] = 2h		50	55		ms
		HSS_CFG0[6:5] = 3h		150	165		ms
t _{AR}	Auto retry time after current limit	HSS_CFG0[2:1] = 0h			50		ms
		HSS_CFG0[2:1] = 1h			0.5		s
		HSS_CFG0[2:1] = 2h			4		s
		HSS_CFG0[2:1] = 3h			10		s
SPI Timing (CS, SCK, SDI, SDO)							

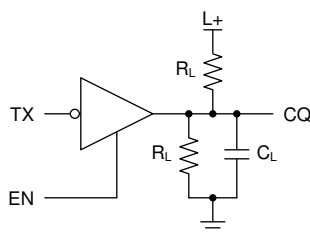
5.6 Switching Characteristics (continued)

Over recommended operating s and recommended free-air temperature range (unless otherwise noted). Typical values are at VCC = 24V, VL = 3.3V and TA = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{SCK_BURST}	Maximum SPI clock frequency	Burst mode; V _(VL) < 3V			15	MHz
t _{SCK}	SCK period	Burst mode; V _(VL) < 3V	66			ns
t _{SCKH}	SCK pulse-width high	Burst mode; V _(VL) < 3V	33			ns
t _{SCKL}	SCK pulse-width low	Burst mode; V _(VL) < 3V	33			ns
f _{SCK_BURST}	Maximum SPI clock frequency	Burst mode; V _(VL) ≥ 3V			25	MHz
t _{SCK}	SCK period		40			ns
t _{SCKH}	SCK pulse-width high		20			ns
t _{SCKL}	SCK pulse-width low		20			ns
f _{SCK}	Maximum SPI clock frequency	Non-burst mode; V _(VL) < 3V			15	MHz
t _{SCK}	SCK period	Non-burst mode; V _(VL) < 3V	66			ns
t _{SCKH}	SCK pulse-width high	Non-burst mode; V _(VL) < 3V	33			ns
t _{SCKL}	SCK pulse-width low	Non-burst mode; V _(VL) < 3V	33			ns
f _{SCK}	Maximum SPI clock frequency	Non-burst mode; V _(VL) ≥ 3V			25	MHz
t _{SCK}	SCK period		40			ns
t _{SCKH}	SCK pulse-width high		20			ns
t _{SCKL}	SCK pulse-width low		20			ns
t _{CSS}	CS falling edge to SCK rise time	V _(VL) < 3V	66			ns
t _{CSS}	CS falling edge to SCK rise time	V _(VL) ≥ 3V	40			ns
t _{CSH}	SCK rise to CS rise hold time	V _(VL) < 3V	66			ns
t _{CSH}	SCK rise to CS rise hold time	V _(VL) ≥ 3V	40			ns
t _{DH}	SDI hold time		5			ns
t _{DS}	SDI setup time				5	ns
t _{DO}	SDO data propagation delay	C _{OUT} = 10pF; V _(VL) < 3V			28	ns
t _{DO}	SDO data propagation delay	C _{OUT} = 10pF; V _(VL) ≥ 3V			15	ns
t _{DORF}	SDO rise and fall time	C _{OUT} = 10pF			4	ns
t _{CSPW}	Minimum CS pulse width (idle time between SPI transactions)		10			ns

(1) CQ/DO output remains Hi-Z for this time

6 Parameter Measurement Information



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Figure 6-1. Test Circuit for Driver Switching

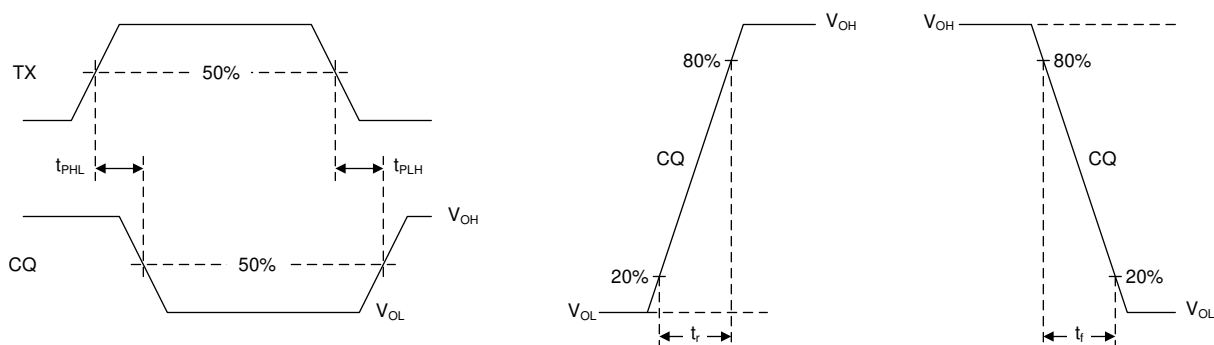


Figure 6-2. Waveforms for Driver Output Switching Measurements

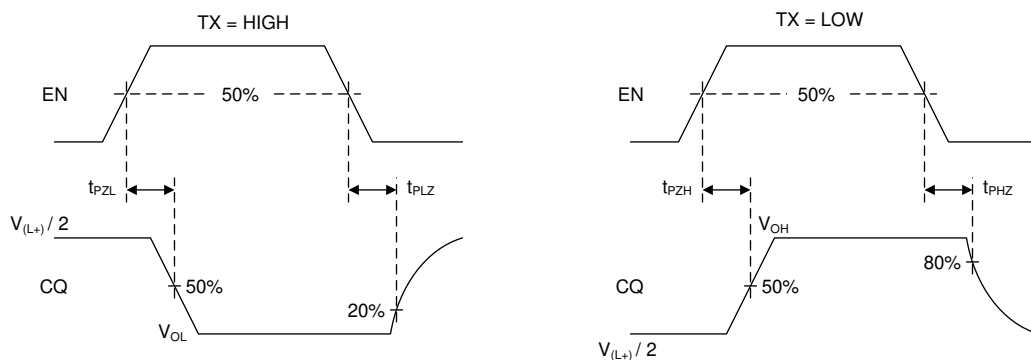


Figure 6-3. Waveforms for Driver Enable or Disable Time Measurements

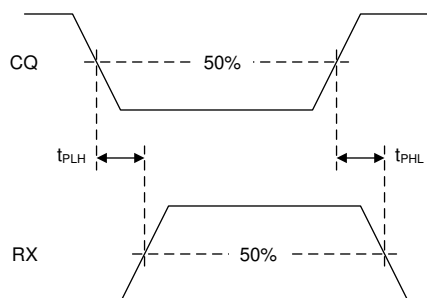


Figure 6-4. Receiver Switching Measurements

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

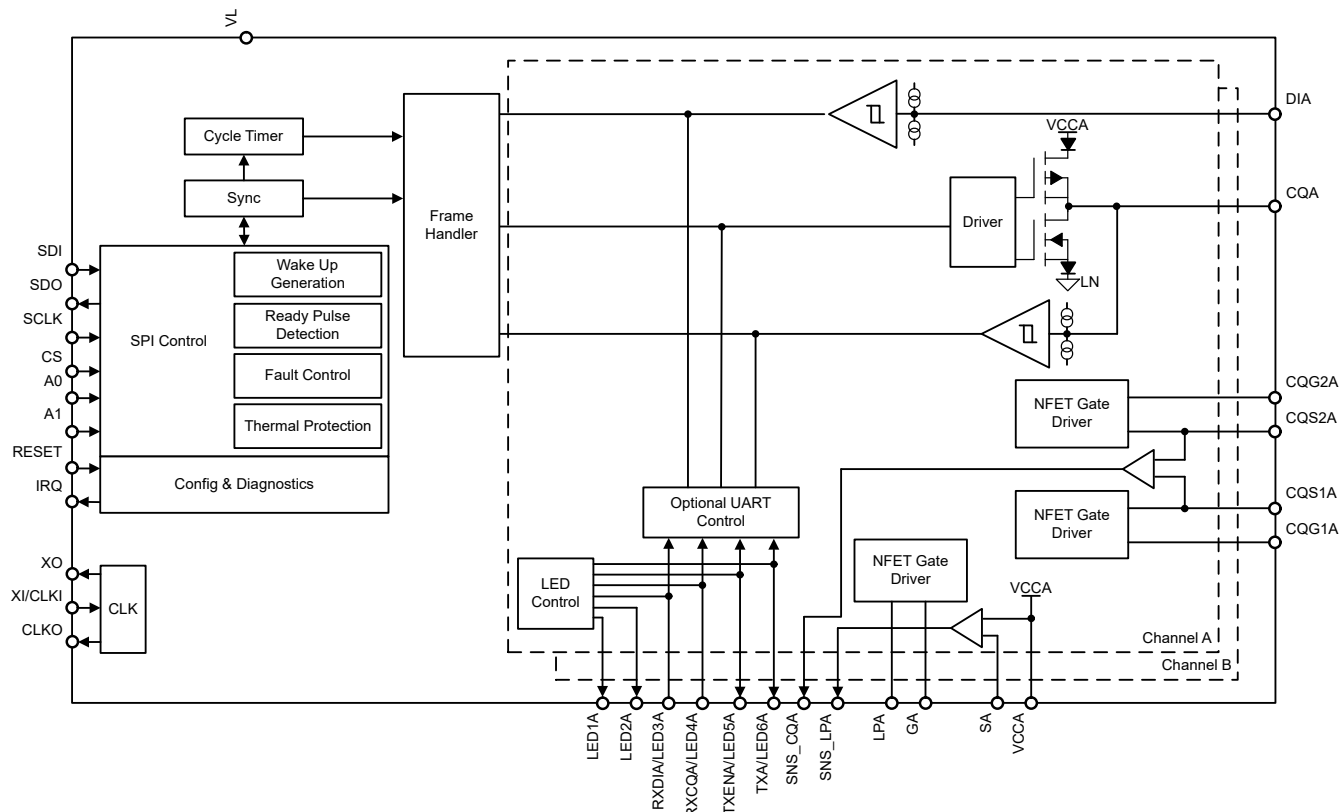
The **TIOM221x functional block diagram** demonstrates the features available in the device. The device's C/Q driver can be used in either push-pull, high-side, or low-side configuration using the enable (TXEN) and transmit data (TX) input pins. The internal receiver converts the 24V signal on the CQ line to standard logic levels on the receive data (RXD) pin. A simple parallel interface is used to receive/transmit data and status information between the device and the local controller.

These devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to $\pm 65\text{V}$ static and $\pm 70\text{V}$ transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features simplify system level design by reducing external protection circuitry.

The device also implements protection features for overcurrent, overvoltage and over-temperature conditions, and the driver output can be current-limited using an external resistor.

Internal low-voltage supply is derived from the IO-Link L+ voltage (24V nominal) via an integrated linear regulator to provide power to the local controller and sensor circuitry.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 L+ Supply Controller

TIOM2212 provides two L+ supply controllers – one for each channel. Each L+ supply is generated using a single NFET transistor. The gate of the external NFET is actively controlled to provide current limiting, auto-retry functionality and L+ undervoltage detection functionality. L+ supplies are reverse voltage tolerant and support DC voltages up to $\pm 65\text{V}$ and transient voltages up to $\pm 70\text{V}$.

A sense resistor, R_{SENSE} , can be connected between the Sx and VCCx pins to enable the device to sense current through the L+ path. The current through the sense resistor is actively controlled to $I_{LIM} = V_{TH}/R_{SENSE}$. A default threshold of $V_{TH} = 15mV$ is set across the sense resistor. This threshold can be configured using LP_CFG0 register (LP_CLIM bits) to one of the following values: 15mV, 30mV, 60mV or 120mV.

Each channel's L+ supply controller can be individually enabled using the LP_GATE_DRV_EN bit in the LP_CFG1 register for the corresponding channels. If it is desired to use a separate supply controller, the LP_GATE_HIZ bit can be set high. This bit disables all functionality related to current sense, but the device will still sense and handle UVLO events on the L+ node.

7.3.1.1 Auto-retry feature

LP_CFG0 register settings can be used to configure the L+ supply current limits. LP_TSC and LP_TAR set the current fault blanking time and auto-recovery time, respectively. LP_AR_DIS controls the auto-recovery behavior. If current through the L+ path exceeds the I_{LIM} set by LP_CLIM bits, then an overcurrent fault is generated. The controller periodically rechecks if the output is still in a current limited condition. In this condition, the device is switched on for LP_TSC and switched off for LP_TAR.

To further reduce the power dissipated in the NFET transistors during turn-on of loads that require large inrush currents (e.g., capacitive loads), the current limiter includes a dynamic blanking time mode that reduces the blanking time when the voltage across the NFET is high, limiting the pulse energy during the initial turn-on phase. Dynamic blanking time mode is operational when the L+ output voltage is below 7V and must be enabled by setting the LP_DYBL_EN bit in the LP_CFG1 register.

7.3.1.2 Current sense feature

TIOM2212 provides current sensing feature for the LP supply controllers. The voltage across the sense resistor is converted into a current using GMSNS_LP and sourced into the pin SNS_LPA/B. The GMSNS_LP scales proportionally to V_{TH} (15mV, 30mV, 60mV, 120mV) the setting. A resistor can be connected between SNS_LPA/B and LM pins to convert the current into a voltage which can be sensed by the Micro-controller ADC. Current sense feature can be enabled by setting LP_SNS_EN bit in LP_CFG1 register.

7.3.2 C/Q Transceiver

TIOM2212 provides two channels each with two IOLINK compliant drivers at CQA and CQB. These can be configured as Push-Pull, NPN and PNP mode. Use IOLINK_PHY registers for this setting. This register can also be used to enable or disable the CQ driver and to set CQ output to High or Low.

CQ current limit can be set in CQ_DRV_CFG register between 100mA to 500mA typical (700mA maximum). CQ drivers are thermally protected using a thermal sensor which shuts down the CQ driver whose temperature exceeds 160°C.

7.3.2.1 CQ Driver Fault Detection

The TIOM2212 signals a fault when the C/Q driver exceeds the CQ_ILIM for longer than the blanking time duration. The current limit, blanking time, and auto-retry time can each be set in the CQ_DRV_CFG register. Upon a C/Q overcurrent fault, the CQ_OC bit is set in CPIREQ register. This condition can be ignored by masking the bit using the CPIMASK register. The device supports two modes (set by CQ_DRV_AR_DIS) when the C/Q driver exceeds CQ_ILIM. The device can either continue to supply current indefinitely until it reaches the thermal shutdown threshold, or it can operate in auto-retry mode. In auto-retry mode, the device supplies current equal to CQ_ILIM for a duration equal to the current blanking time, and then disables the output for a duration equal to the auto-retry time. As long as the C/Q driver continues to exceed CQ_ILIM, this routine will repeat a number of times until it reaches the value set in the CQ_DRV_MAX_AR field (and it will repeat an infinite number of times if the value of this field is 0000b).

7.3.2.2 CQ Reverse Polarity Protection

CQ driver provides reverse polarity protection with LM and VCC. The CQ driver actively limits current and gets disabled if the CQ voltage goes below LM or above VCC.

7.3.2.3 CQ Current Source or Sink

Each CQ driver supports internal pull up/down programmable internal current sources.

The current value and direction can be set using the CQ_CFG register. The internal pull up/down are automatically disabled while the driver is enabled. CQ_SNK_SRC bits can be used to set the sink/source current to 150uA/2mA/5mA. CQ_SRC_EN/CQ_SNK_EN bits are used to enable the source or sink current sources.

7.3.2.4 CQ Receiver Output

CQA/B receiver outputs are RXA/B. These are mux'ed with the LED drivers.

The RX can be disabled by setting CQ_RX_VTH_EN bits (in CQ_CFG) to 11. RXA/B will be high impedance in this mode.

7.3.2.5 CQ Receiver Threshold

CQ receiver thresholds are compliant to the IOLINK standard by default. However, to enable operations for lower LP values, the threshold can be set to ratio-metric with respect to LP. This can be done by setting CQ_RX_VTH_EN bits (in CQ_CFG) to 01. The thresholds will now be compatible with IOLINK standard for LP $\geq 18V$ and is ratio-metric for LP $< 18V$ (**FigureX**).

The thresholds can also be set to be compatible with IEC 61131-2 type 2/3 by setting CQ_RX_VTH_EN bits (in CQ_CFG) to 10.

7.3.2.6 CQ/RX Receiver Glitch Filter

The noise immunity of the CQ Receiver can be improved by setting the bit CQ_GFILT_EN in CQ_CFG register. When the glitch filter is enabled, any glitches less than 1.15us (typical) are ignored at by the RX.

7.3.3 High-side Switch (HSS) Gate Driver

The device features high-side switch (HSS) gate drivers to provide additional drive on C/Q outputs. The gate drivers control the pins CQG1x and CQG2x to provide active current limiting, reverse polarity protection, and auto-retry functionality for the HSS. The current through the HSS is sensed using a sense resistor placed between CQS1x and CQS2x. The current through the sense resistor is actively controlled to $I_{LIM} = V_{TH}/R_{SENSE}$. A default threshold of $V_{TH} = 15\text{mV}$ is set across the sense resistor. This threshold can be configured using HSS_CFG0 register (HSS_CLIM bits) to one of the following values: 15mV, 30mV, 60mV, and 120mV.

The CQx HSS controllers can be individually enabled using HSS_GATE_DRV_EN bit in HSS_CFG1 register for the corresponding channels.

The FET connected to CQG1x controls the HSS current value and state (ON/OFF) while the FET connected to CQG2x provides reverse polarity protection. The threshold for reverse polarity is set at 100mV across the sense resistor. The state of both FETs can be individually controlled using the HSS_CQG1_EN and HSS_CQG2_EN bits in HSS_CFG1.

All gate drivers support NFETs for lower overall system cost. These drivers are capable of switching external NFETs at speeds >10kHz.

Auto-retry feature

The HSS_CFG0 register can be used to configure the HSS current limits. HSS_TSC and HSS_TAR set the current blanking time and auto-retry time, respectively. If the HSS current exceed the I_{LIM} set by HSS_CLIM bits, then an overcurrent fault is generated. The device supports two modes (set by HSS_AR_DIS) when the HSS exceeds HSS_CLIM. The device can either continue to supply current indefinitely until it reaches the thermal shutdown threshold, or it can operate in auto-retry mode. In auto-retry mode, the device supplies current equal to HSS_CLIM for a duration equal to the current blanking time, and then disables the output for a duration equal to the auto-retry time. As long as the HSS continues to exceed HSS_CLIM, this routine will repeat a number of times until it reaches the value set in the HSS_MAX_AR field (and it will repeat an infinite number of times if the value of this field is 0000b).

To further reduce the power dissipated in external NFETs during turn-on of loads that require large inrush currents (e.g., capacitive loads), the current limiter includes a dynamic blanking time mode that reduces the blanking time when the voltage across the FET is high, limiting the pulse energy during the initial turn-on phase. Dynamic blanking time mode is operational when the HSS output voltage is below 7V and must be enabled by setting the HSS_DYBL_EN bit in the HSS_CFG1 register.

Current sense feature

TIOM2212 provides current sensing feature for the HSS. The voltage across the sense resistor is converted into a current using GMSNS,HSS and sourced into the pin SNS_CQA/B. The GMSNS,HSS scales proportionally to V_{TH} (15mV, 30mV, 60mV, 120mV) the setting. A resistor can be connected between SNS_CQA/B and LM pins to convert the current into a voltage which can be sensed by the Micro-controller ADC. Current sense feature can be enabled by setting HSS_SNS_EN bit in HSS_CFG1 register.

7.3.4 DI Receiver

The device includes two auxiliary receivers DIA and DIB. These receivers can be enabled by setting bits of `DI_RX_VTH_EN = 0b11` in each channel-specific register `CQ_DRV_DI_CFG`.

These inputs are reverse polarity protected with respect to LP, CQ, LM and VCC.

Each DI receiver implements an internal pull up/down internal current source of 2mA. The direction can be set using the `CQ_DRV_DI_CFG` register. `CQ_SRC_EN/CQ_SNK_EN` bits are used to enable the source or sink current sources.

DI receiver thresholds are compliant to the IO-Link standard by default. However, to enable operations for lower LP values, the threshold can be ratiometric with respect to LP by setting the `DI_RX_VTH_EN` bits (in `CQ_DRV_DI_CFG`) to 01b. This makes the device's thresholds compatible with the IO-Link standard when $L+ \geq 18V$ and will be ratiometric for $L+ < 18V$. The thresholds can also be set to be compatible with IEC 61131-2 type 2/3 by setting `DI_RX_VTH_EN` bits (in `CQ_DRV_DI_CFG`) to 10b.

The noise immunity of the DI Receiver can be improved by setting the bit `DI_GFILT_EN` in `CQ_DRV_DI_CFG` register. When the glitch filter is enabled, any glitches $< 1.8\mu s$ (typical) are ignored by the RX.

7.3.5 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the L+, CQ and L- pins. The maximum voltage between any of the pins may not exceed 65V DC at any time.

Figure 7-1 and Figure 7-2 shows all the possible connection combinations.

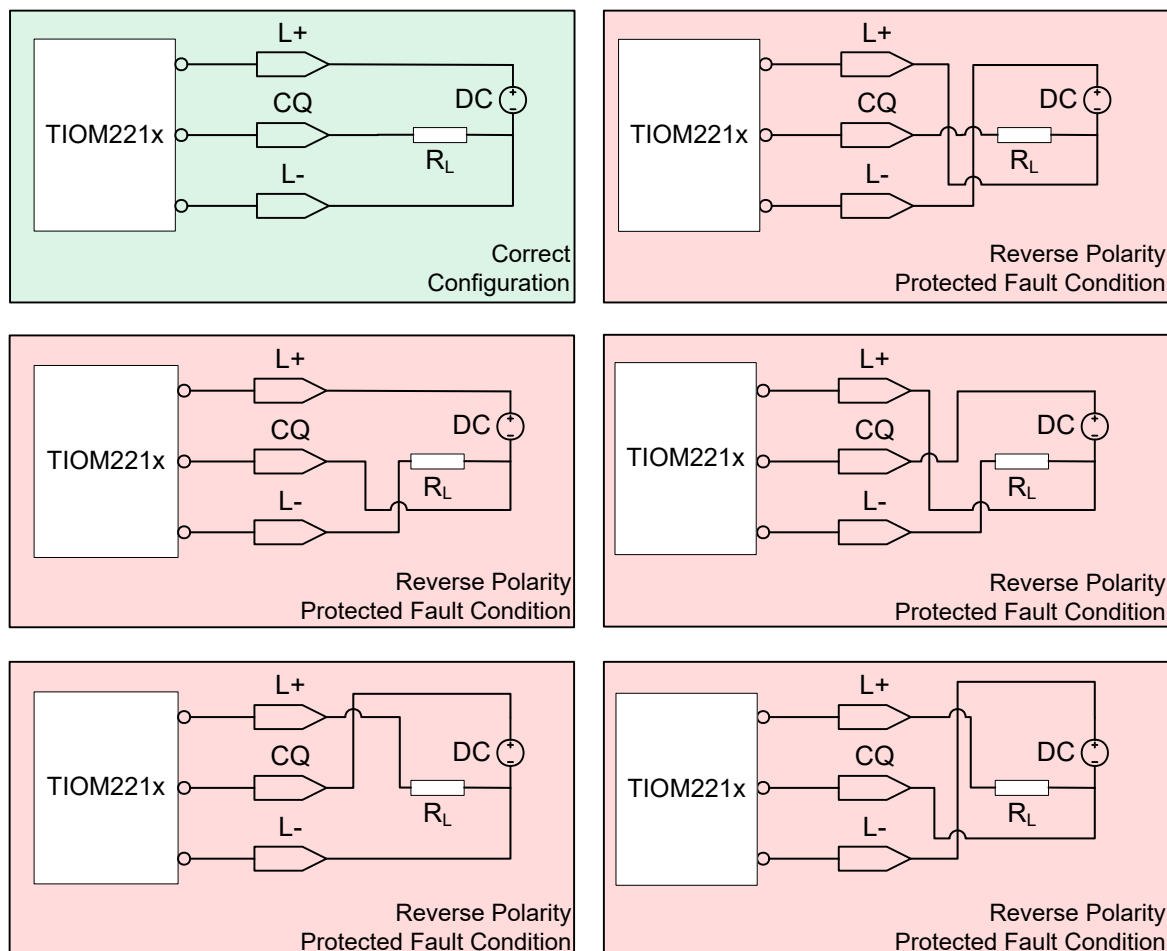


Figure 7-1. High-Side Driver Configuration

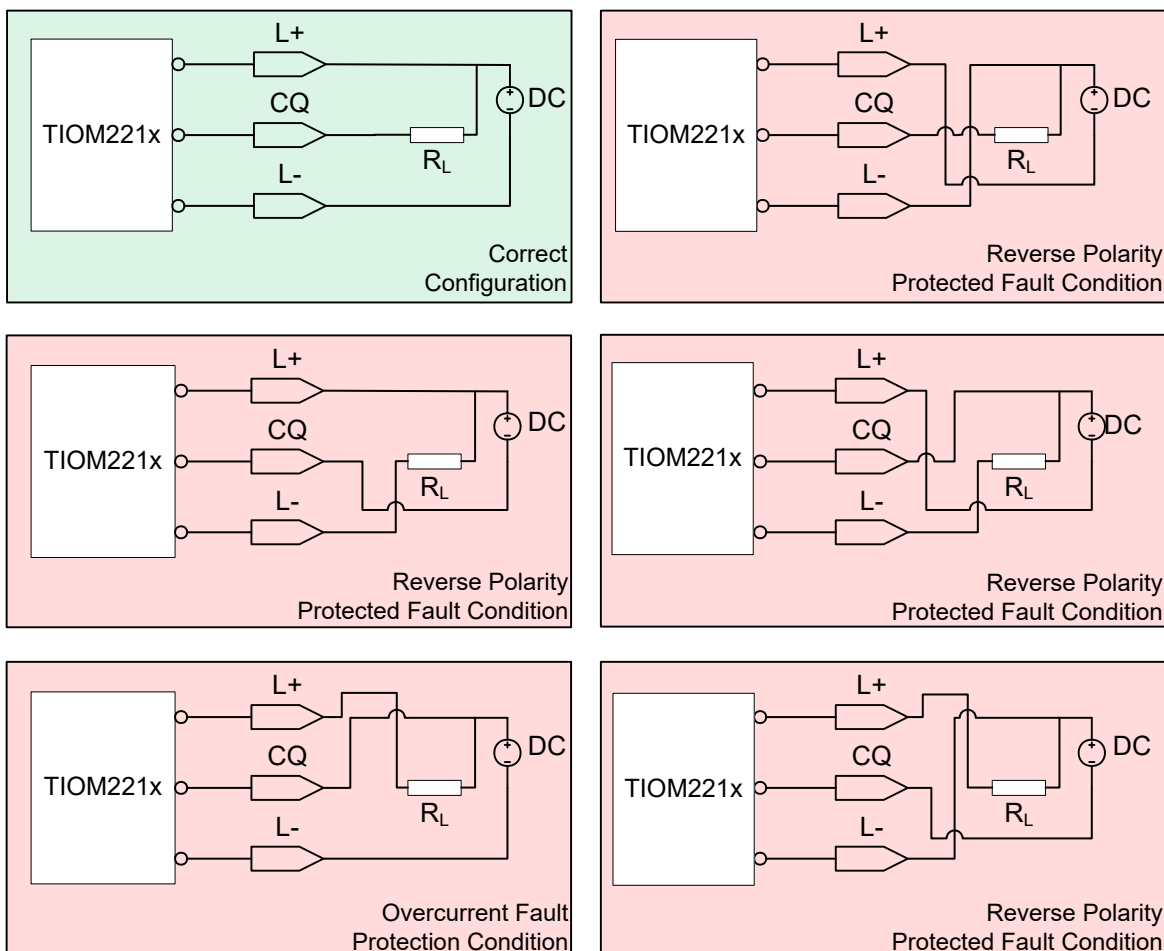


Figure 7-2. Low-Side Driver Configuration

7.3.6 Thermal Warning and Shutdown

If the die temperature exceeds $T_{(WRN)}$, an over-temperature fault is generated by setting the bit in the OT_WARN bit of the CPSTAT register, but the output is not disabled. If the temperature continues to rise past $T_{(FAULT)}$, the OT_FAULT bit of the CPSTAT bit is set and the output is disabled. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal thermal protection circuit re-enables the driver.

7.3.7 Clocking

XO and XI are used for a crystal oscillator. Use a 14.747MHz crystal connected across these pins. The 14.747MHz is internally divided down to 3.686MHz to be used for the IOLINK Frame-handler. The crystal oscillator can be enabled by setting the bit XTAL_EN to 1. This output is also available at CLKO pin and can be used by other TIOM2212 devices on the same board. The CLKO pin can be configured to output the crystal oscillator clock by setting CLKO_EN to 1. The devices receiving the clock externally must set the bit CLKIN_EN to 1.

A capacitance of 10pF is provided internally on XO and XI. Select the CL1 and CL2 to provide the required CL for the crystal to resonate at the target frequency.

In case, UART is used instead of the internal Frame-handler, the internal oscillator accuracy is sufficient and must be enabled by setting the INT_OSC_EN to 1.

7.3.8 Power Up Sequence (TIOM2212)

VCC and L+ domains can be powered up in any sequence. If L+ is powered and VCC is not, the CQ pin remains in high impedance.

If the VL voltage falls below 1.3V (VL UVLO threshold), even with VCC or L+ present still, the digital module is reset and the device must be re-configured again.

7.3.9 Device Functional Modes

There are four modes of operation for a given channel. Each channel can be independently configured to act in either of these four modes. This channel mode can be configured using the CLMD field in the LCFG register:

1. IOLINK PHY mode
2. UART mode
3. Frame handler mode
4. Extended frame handler mode

7.3.9.1 IO-Link PHY Mode

The IO-Link PHY Mode is the basic PHY driver mode, in which the CQ is directly controlled using the TX and TXEN pins. In this mode, the C/Q driver can be configured to select the source of TX and TXEN based on the PHY Mode configuration register CQSRC in the corresponding channel register.

CQSRC	TXD Source	TXEN Source
0 (SPI Mode)	CQ_TXD field in IOLINK_PHY register	CQ_MD field in IOLINK_PHY register
1 (Pin Mode)	TXD pin	TXEN pin

In both the SPI and PIN sub-modes of this mode, the RXCQ pin acts as the RXD for that channel, if that pin is selected as RXD using the LED4_SEL field in the HSS_ALT_FUNC_SEL register.

In the PIN sub-mode, the CQ_MD field in IOLINK_PHY register is used to configure the CQ driver mode of operation. In the SPI sub-mode, the CQ_MD field in IOLINK_PHY register is used to configure the driver.

Pin Mode

In the PIN sub-mode, the value of CQ_TXD field in IOLINK_PHY register is ignored.

CQ_MD	TXEN pin	TXD pin	CQ	RXCQ pin CQ_RXD register field ~CQ [LED4_SEL = 0 & CQ_RX_VTH_DIS != 11]
00	X	X	HiZ	~CQ
01 (NPN)	0	0	HiZ	~CQ
01 (NPN)	0	1	HiZ	~CQ
01 (NPN)	1	0	HiZ	~CQ
01 (NPN)	1	1	Low	~CQ
10 (PNP)	0	0	HiZ	~CQ
10 (PNP)	0	1	HiZ	~CQ
10 (PNP)	1	0	High	~CQ
10 (PNP)	1	1	HiZ	~CQ
11 (Push Pull)	0	0	HiZ	~CQ
11 (Push Pull)	0	1	HiZ	~CQ
11 (Push Pull)	1	0	High	~CQ
11 (Push Pull)	1	1	Low	~CQ

Note: when LED4_SEL = 0 & CQ_RX_VTH_DIS == 11, then RXCQ is undefined.

SPI Mode

In the SPI sub-mode, the values of TX & TXEN pins are ignored.

CQ_MD	CQ_TXD	CQ	RXCQ pin CQ_RXD register field [LED4_SEL = 0 & CQ_RX_VTH_DIS != 11]
00	X	HiZ	~CQ
01 (NPN)	0	HiZ	~CQ
01 (NPN)	1	Low	~CQ
10 (PNP)	0	High	~CQ
10 (PNP)	1	HiZ	~CQ
11 (Push Pull)	0	High	~CQ
11 (Push Pull)	1	Low	~CQ

Note: when LED4_SEL = 0 & CQ_RX_VTH_DIS == 11, then RXCQ is undefined.

7.3.9.1.1 Integrated Automated Sequences

The IO-Link PHY mode integrates several automated sequences to reduce the load on MCU during the startup sequence of the IO-Link protocol:

1. Ready Pulse Detection with Timeout (RPD)
2. Wake Pulse Generation (WPG)
3. Ready Pulse Detection with Timeout followed by Wake Pulse Generation (RPDWPG)
4. Establish Communication Sequence (ECS)
5. Ready Pulse Detection with Timeout followed by Establish Communication Sequence (RPDECS)

Ready Pulse Detection with Timeout (RPD)

Ready Pulse Detection starts with setting the AUTO_START field to 3b010 in the IOLINK_PHY register. The sequence starts by setting the Lplus supply enable internally, enabling the Lplus supply and it waits for the Lplus UVLO status to go low. The Timeout Timer runs parallel for period configured in the RPD_OFST_TMR. Until the timer expires, it will try to detect a valid ready pulse with period tRP as per the IOLINK standard.

If a valid ready pulse is detected, ASEQ_OK Interrupt in the CLIREQ will be logged and indicated on IRQ pin based on CLIMASK. Else in the case of invalid pulse length detection or no pulse detection, in the period of detection, RPD_ERR interrupt in the CLIREQ will be triggered at timeout.

User can issue an abort command (AUTO_START = 0x7) to stop the ready pulse detection sequence

Wake Pulse Generation (WPG)

The TIOM2212 is capable of generating a wake pulse of length t_{WU} (80μs) as per the IO-Link Standard. The wake pulse is generated by inverting the CQ state for length t_{WU} and again inverting the CQ state for length t_{WUI} .

The following procedure should be followed when generating a wake pulse:

1. Set the C/Q driver to receive mode:
 - a. If the device is in UART mode, drive the TXEN and TX pins low.
 - b. If the device is in a SPI-controlled mode, set the TXEN and TX bits low in the corresponding channel register.
2. Write a value of 0x1 into the AUTO_START field in the corresponding channel register.
3. Wait for the wake pulse routine to execute.

If a valid wake pulse is generated, the ASEQ_OK interrupt bit in the CLIREQ register will be set. In the case of any bus faults, the WPG_ERR interrupt bit in the CLIREQ register will be set.

Ready Pulse Detection with Timeout followed by Wake Pulse Generation (RPDWPG)

In this combination sequence, the wake pulse is generated after the RPD Timer expiry and t_{RW} timer expiry.

If the sequence is successful, ASEQ_OK interrupt flag is set. Else in case of RPD or WPG fail, the corresponding RPD_ERR or WPG_ERR flags will be set.

Establish Communication Sequence (ECS)

The Establish Communication Sequence (ECS) is initiated by setting the AUTO_START register to a value of 0x4 in the corresponding channel register. This automated sequence follows the standard with configuration override of T₂ and T_A. In this sequence, a wake pulse is generated, and then a read minimum cycle time message is transmitted on the C/Q line at each COMx rate, starting at COM3 and progressively moving towards slower rates.

If a valid response is received, the ASEQ_OK interrupt bit in the CLIREQ register will be set, and the user can read the successful COM rate from the COM field in the LCFG register and minimum cycle time from the FH_CYCT register. In the case of a failure, the ECS_ERR interrupt bit in the CLIREQ register will be set.

Ready Pulse Detection with Timeout followed by Establish Communication Sequence (RPDECS)

The Ready Pulse Detection with Timeout followed by Establish Communication Sequence (RPDECS) combines the RPD and ECS sequences and is initiated by setting the AUTO-START register to a value of 0x5 in the corresponding channel register. Once the RPD sequence is complete, after a length of t_{RW}, the ECS sequence will be executed. Refer to both the RPD and ECS descriptions for more information.

In the case of success over the full sequence, the ASEQ_OK interrupt bit in the CLIREQ register will be set. In the case of a failure along any part of the sequence, the corresponding RPD_ERR or ECS_ERR interrupt bit in the CLIREQ register will be set.

7.3.9.2 UART Mode

In UART Mode, the channel will act like a basic UART transmitter with one-byte buffer. It's fundamentally a UART with IO-Link base UART format. This mode can be used to send and receive IO-Link frames byte by byte. In this mode all the IO-Link PHY configurations are applicable other than T_A, T₂, PHYMD, and CQ_TXD.

Transmission & Reception

To transmit in UART mode, write the data byte into the UART register when the TX_RDY is set for transmitting the message. To receive in UART mode, read the data byte from the UART register when RX_RDY is set for reading the received message.

If a data byte is unread by the microcontroller, and the UART receives the next byte, an overrun interrupt (OR_ERR) is generated. A receiver error (RX_ERR) interrupt is generated when a frame error or parity error is detected during reception. A transmission error (TX_ERR) interrupt is generated when transmitted data is not reflected on the CQ channel.

7.3.9.3 Frame Handler Mode

In Frame Handler Mode, the PHY is capable of sending and receiving IO-Link frames that conform to the standard. The configuration registers also allow the PHY to operate outside the IO-Link standard in some critical timing specifications such as t₁, t_A, and t₂.

Message Sequence Configuration

An IO-Link Message constitutes of MC, CKT, MPD and OD in the master transmitted message and OD, DPD and CKS in the device message response, based on the type of IO-Link message.

The length of each message changes with respect to the M-Sequence Type, Read/Write Operation, IO-Link Communication Channel used, length of Master Process Data, length of Device Process Data and length of

On-demand Data. To configure the IO-Link frame, provide the Master Process Data Length in the FH_MPDLEN register, Device Process Data Length in the FH_DPDLEN register and the On-demand Data Length in the FH_ODLEN register. Other required information like the frame type, read or write status, and IO-Link channel used is parsed from the first two bytes of the message to be transmitted.

The FH_ODLEN, FH_MPDLEN and FH_DPDLEN SPI accessible registers are used to configure the lengths of the data fields.

The access type, channel and M-Sequence Type information is parsed from the first two bytes written into the transmit buffer.

In the case of nonstandard message length configuration in the FH_ODLEN, FH_MPDLEN and FH_DPDLEN registers for a given TX and RX data length computation, a nonstandard message is sent and expected at the receiver.

Table 7-1. TX Message Length Calculation

Frame Type	R/W	Channel	TX Data Length
0	R	X	0
0	W	X	1
1	R	X	0
1	W	process	2
1	W	! process	FH_ODLEN
2	R	X	FH_MPDLEN
2	W	X	FH_MPDLEN + FH_ODLEN
3	R	X	0
3	W	X	1
default	R	X	FH_MPDLEN
default	W	X	FH_MPDLEN + FH_ODLEN

Table 7-2. RX Message Length Calculation

Frame Type	R/W	Channel	RX Data Length
0	W	X	0
0	R	X	1
1	W	X	0
1	R	process	2
1	R	! process	FH_ODLEN
2	W	X	FH_DPDLEN
2	R	X	FH_ODLEN + FH_DPDLEN
3	W	X	0
3	R	X	1
default	W	X	FH_DPDLEN
default	R	X	FH_ODLEN + FH_DPDLEN

Frame Buffer

The frame handler comes with an integrated 128-byte frame buffer, which is used to stage data for transmission and store received data during reception.

Checksum

The device features an integrated hardware checksum generator that can be enabled by setting the CKSM field in the FH register. When this bit is enabled, the checksum field loaded in the data to be transmitted is ignored,

and instead a computed checksum is appended as part of the message to be transmitted. To use the automatic checksum, the entire message to be transmitted has to be filled in the transmit buffer before the send event is triggered. If the checksum generator is disabled, the TX checksum is computed internally to compare to the data frame. When the last message is received in the TX buffer and the device compares this internal checksum to the loaded checksum, if this comparison fails, the device will set the CKSM_ERR interrupt.

In all receive message events, the received message checksum is computed and validated against the checksum part of the received messages.

Transceiver Modes

The Frame Handler decides upon the following criteria when an M-sequence can be started:

Automatic Checksum enabled (CKSM bit in the FH register):

- If enabled, a full Master Message must be available in the frame buffer before a transmission starts.
- If disabled, a transmission can start as soon as at least one byte of the Master Message is available in the frame buffer.

Synchronization enabled (SYNC_INT_EN or SYNC_EXT_EN bits in the FH register):

- If enabled, a synchronization event starts the Offset Timer. After the Offset Timer has elapsed, a Master Message is sent if available in the frame buffer. If inadequate data is available in the frame buffer when the Offset Timer elapsed, no transmission is started.

Cycle Timer enabled (FH_CYCT register):

- If enabled (the FH_CYCT register is not zero), the Cycle Timer starts if a Master Message is available in the frame buffer or, if synchronization is enabled, a synchronization request is received.
- If the Cycle Timer has elapsed the next Master Message can be sent.

If an M-sequence is to be started (Cycle Timer elapsed or Offset Timer elapsed) and no Master Message data is available in the frame buffer, the Frame Handler ignores this event without triggering an error.

Automatic Checksum Off, Synchronization Off, Cycle Timer Off

A byte written to the FHD register is immediately sent at the CQ pin. After the last byte of the Master Message is sent, the Frame Handler waits for the Device Message. A new Master Message can be sent after the Device Message was read from the frame buffer.

Note: The IO-Link specification requires a UART “*frame transmission delay for master ports*” (IO-Link Interface and System Specification) of maximum 1 T_{BIT} . After a byte is transmitted at the CQ pin, the next byte must be available in the frame buffer at least within 1 T_{BIT} delay or T_1 timeout will occur, in effect setting the T1_TA_T2_TO_ERR bit.

Automatic Checksum Off, Synchronization Off, Cycle Timer On

A byte written to the FHD register is immediately sent at the CQ pin. Simultaneously, the Cycle Timer starts. After the last byte of the Master Message is sent, the Frame Handler waits for the Device Message.

If the Cycle Timer elapses and at least one byte of the next Master Message is available in the frame buffer, the Cycle Timer restarts and the data available in the frame buffer is sent at the CQ pin.

If the Cycle Timer elapses and no Master Message data is available in the frame buffer, the Cycle Timer stops until a new byte is written to the frame buffer via the FHD register. Then the Cycle Timer restarts and the Master Message bytes are sent via the CQ pin.

Automatic Checksum Off, Synchronization On, Cycle Timer Off

When a synchronization request is received, the Offset Timer starts. When the Offset Timer elapses, the Master Message in the frame buffer is sent via the CQ pin. If no data is available in the frame buffer when the Offset Timer elapses, no data is sent.

When a subsequent synchronization request is received and the offset time has not elapsed, the synchronization request is ignored. If the transmission of a Master Message started, synchronization requests are ignored until the Device Message is fetched from the frame buffer completely.

Automatic Checksum Off, Synchronization On, Cycle Timer On

After an initial synchronization request is received, the Offset and Cycle Timers start. When the Offset Timer elapses, an available Master Message in the frame buffer is sent via the CQ pin. Transmission starts if at least one byte of a Master Message is available in the frame buffer. It is up to the user to write the remaining bytes of the Master Message fast enough to the frame buffer to not violate the UART frame transmission delay for master ports. If no Master Message data is available in the frame buffer when the Offset Timer elapses, no UART frames are sent during this cycle. After the last byte of the Master Message is sent, the Frame Handler waits for the Device Message.

After the Cycle Timer elapses, the process restarts by starting the Offset Timer and restarting the Cycle Timer.

Note

The Offset Timer timeout must not exceed the Cycle Timer timeout, otherwise the behavior of the Frame Handler is undefined.

While the Cycle Timer is running, additional synchronization events are ignored. The Cycle Timer continues running until the Frame Handler is reset or the Cycle Timer is disabled. A Frame Handler SKIP does not disable or reset the Cycle Timer.

Automatic Checksum On, Synchronization Off, Cycle Timer Off

Once a full Master Message is written to the frame buffer via the FHD register, the message is sent via the CQ pin. After the last byte of the Master Message is sent, the Frame Handler waits for the Device Message. A new Master Message can be sent after the Device Message is read from the frame buffer.

Automatic Checksum On, Synchronization Off, Cycle Timer On

After a full Master Message is written to the frame buffer via the FHD register, the message is immediately sent at the CQ pin and the Cycle Timer is started. After the last byte of the Master Message is sent, the Frame Handler waits for the Device Message.

If the Cycle Timer elapses and a full Master Message is available in the frame buffer, the Cycle Timer restarts, and the Master Message is sent at the CQ pin.

If the Cycle Timer elapses and no full Master Message is available at the frame buffer, the Cycle Timer stops until a full Master Message is written to the frame buffer. Immediately after, the Cycle Timer is restarted, and the Master Message is sent via the CQ pin.

Automatic Checksum On, Synchronization On, Cycle Timer Off

If a synchronization request is received, the Offset Timer starts. When the Offset Timer elapses, the Master Message in the frame buffer is sent via the CQ pin. If no full Master Message is available in the frame buffer when the Offset Timer elapses, no data is sent.

If a subsequent synchronization request is received and the offset time has not elapsed, the synchronization request is ignored. If the transmission of a Master Message started, synchronization requests are ignored until the Device Message is fetched from the frame buffer completely.

Automatic Checksum On, Synchronization On, Cycle Timer On

After an initial synchronization request is received, the Offset and Cycle Timers start. When the Offset Timer elapses, the Master Message available in the frame buffer is sent via the CQ pin. If no full Master Message is available in the frame buffer when the Offset Timer elapses, no data is sent during this cycle. After the last byte of the Master Message is sent, the Frame Handler waits for the Device Message.

After the Cycle Timer elapses, the process starts over by starting the Offset Timer and restarting the Cycle Timer. Note: The Offset Timer timeout must not exceed the Cycle Timer timeout, otherwise the behavior of the Frame Handler is undefined.

While the Cycle Timer is running, additional synchronization events are ignored. The Cycle Timer continues running until the Frame Handler is reset or the Cycle Timer is disabled. A Frame Handler SKIP does not disable or reset the Cycle Timer.

M-Sequence Handling

Interrupts can be configured to trigger after either portions of a Device Message or the complete Device Message are received. The interrupt behavior can be modified using the CLIMASK and FH_BTLVL register.

Parity or checksum errors in the received Device Message are indicated by the CLSTAT.STATE register. The erroneous Device Message is stored in the frame buffer.

The Frame Handler checks the following timing constraints of the IO-Link Interface and System Specification:

- UART frame transmission delay of Master ports (Annex A.3.3), t_1
- UART frame transmission delay of Devices (Annex A.3.4), t_2
- Response time of Devices (Annex A.3.5), t_A

If any of these timing constraints are violated by the M-sequence (Master and/or the Device Message), a timeout is flagged.

According to the IO-Link Interface and System Specification [1] (Annex A.3.5, Response time of Devices) the device is expected to respond within $1 T_{BIT} \leq t_A \leq 10 T_{BIT}$ after the Master Message is sent. However, some IO-Link busses in the field violate this constraint. To be able to support such devices, the T_A bits in the LCFG register can be used to extend the timeout.

To allow support for devices which violate the UART frame transmission delay (t_2), the threshold used by the Frame Handler to check for this timeout can be relaxed using the T2 bits in the LCFG register.

States, Skip and Reset Function

The Frame Handler is implemented as a finite-state-machine (FSM) which is either idle, transmitting a Master Message, or receiving a Device Message.

In IDLE mode, the Frame Handler waits for Master Message Data to be available in the frame buffer, the expiry of the offset, or elapsing of the Cycle Timer depending on the transceiver modes. The Frame Handler is only sending data at CQ while in TRANSMIT mode. The Frame Handler is only waiting for or receiving and storing Device Message data to the frame buffer while in RECEIVE mode.

Setting the RST or the SKIP bit of the FH register immediately resets the FSM to the idle state by aborting the transmission of a Master Message or reception of the Device Message. Data present in the frame buffer is rejected but the Frame Handler configuration (FH, FH_MPDLEN, FH_ODLEN, FH_DPDLEN) is retained. If the RST bit is set, the SKIP bit is ignored. If RST is set to one, the Cycle Timer is also reset. If only the SKIP bit is set, the Cycle Timer is left untouched.

The Frame Handler is also reset while it is not in the idle state and at least one of the following is true:

- the FH register is written and the SKIP bit is not set, or
- the Cycle Timer is enabled or disabled, or
- any of the FH_ODLEN, FH_MPDLEN and FH_DPDLEN registers are written.

State	FH SKIP	FH RST
Communication speed (COM)	Retained	Retained
Frame buffer	Data invalidated, ready to receive new Master Message via SPI	Data invalidated, ready to receive new Master Message via SPI
FH_MPDLEN, FH_ODLEN, FH_DPDLEN registers	Retained	Retained
Cycle Timer	Continues running	Reset and needs to be restarted
FH_CYCT register	Retained	Retained
Offset Timer	Reset	Reset
Offset Timer register	Retained	Retained

Cycle Timer

A Cycle Timer is available for channels configured in Frame Handler mode. It enables the user to comply with the configured IO-Link cycle times without further effort. The cycle time is set up in the FH_CYCT register. The format of this register resembles the defined structure in the IO-Link Interface and System Specification.

TI does not recommend to configure cycle times that are shorter than 400µs which is the minimum cycle time stated by the standard (IO-Link Interface and System Specification). To disable the Cycle Timer, set the register to zero.

By setting the SKIP bit in the FH register, the Frame Handler can be reset without affecting the Cycle Timer. The Cycle Timer is stopped, and its internal counter resets to zero. The CYCT register content does not change due to a Frame Handler reset.

If the Cycle Timer is disabled (FH_CYCT set to 0), a write to the FH_CYCT register does not start the Cycle Timer. A trigger to start the transmission of a Master Message is required to start the Cycle Timer.

If the Cycle Timer is already running and a new value is written to the FH_CYCT register, the Cycle Timer uses the new value after the current timeout period elapses.

If the Cycle Timer started, a new Master Message is not sent until the configured cycle time (and the Offset Timer if enabled) has elapsed.

Synchronization

The start of transmission can be triggered by an external signal or by writing to the SYNC bits of the SYNC register.

Synchronization to an external signal can be enabled by setting the SYNC_EXT_EN bit in the FH register. Each channel can select one of the TXA, TXB pins as synchronization source via the SYNC_SRC_SEL bits. If enabled, a rising or falling edge initiates the start of transmission. The SYNC_EDGE bit selects the active edge of the synchronization signal. The synchronization pulse must be at least 1µs wide to be properly detected.

If the SYNC_INT_EN bit in the FHC register is set, the start of transmission can be triggered by writing the SYNC bit of the SYNC register. Writing '1' to the SYNC bit of the corresponding channel starts the transmission of a message.

Offset Timer

To delay the start of transmission of a Master Message, the Offset Timer (RPD_OFST_PSC_TMR) can be used. This allows the device to align the start of a Device Message across multiple channels. This requires knowing the delay between the start of the Master Message and the start of the Device Message. Note: this is an experimental feature, and the mentioned delay is device dependent and not part of the IO-Link IODD specification.

The Offset Timer timeout can be set by the PSC field and TMR field in the RPD_OFST_PSC_TMR register.

Keep TX Buffer

Setting the TKEEP bit in the FH register will enable this feature, which retains the message in the TX buffer for retransmission. This can be used in combination with the cycle timer to do periodic transmission of specific messages, without refilling the TX buffer.

The TX buffer will be reloaded once the transmission ends and the frame handler becomes idle, waiting for next message start trigger based on the Transceiver Modes defined using the Automatic checksum, Synchronization & Cycle Timer. The TX buffer will be flushed in case of TX checksum error and t_1 timeout error, where user fails to fill the buffer before the t_1 timeout.

7.3.9.4 Extended Frame Handler Mode

In extended frame handler mode, the device can send and receive IO-Link standard defined UART frames. This mode provides the user with flexibility to implement extended message features. It comes with a 128-byte integrated buffer and can be used to send and receive messages of any length with the help of provided interrupts.

Operation

Configure the channel into extended frame handler mode by setting the CLMD = 11 in the LCFG register. To transmit a message, fill the TX buffer by writing into the FH_DATA register with the message bytes to transfer. Once the entire message is transmitted, the extended frame handler changes to receive mode and fills the RX buffer for the messages received. At a given time, the TX buffer and RX buffer can hold 128-bytes of data.

User can configure the TX_BTLVL and RX_BTLVL registers with valid values less than or equal to value 128 to enable the TX_BTLVL_FBT and RX_BTLVL_RATL interrupts. The TX_BTLVL_FBT interrupt is set when the TX buffer level falls below the configured trigger level, and the RX_BTLVL_RATL interrupt is set when the RX buffer level rises above the configured trigger level. The TX_BEMPTY interrupt indicates that the TX buffer is empty, and the RX_BFULL interrupt indicates that the RX buffer is full. If the RX buffer is full and still there is data being received in the CQ interface, OR_ERR is set to indicate that there is a UART overrun error. If the transmitted message is not reflecting on the CQ line, TX_ERR interrupt is set to indicate that there is a transmission error. If the RX frame contains either a parity or frame error, the RX_ERR interrupt is set.

Note: None of the frame handler features are enabled in this extended frame handler mode to provide full flexibility to the user.

CQ OC, LP OC, HSS OC & Reverse Polarity Auto Recovery

The auto recovery feature helps the device to recover from temporary faults, with the help of disable and re-enable cycles. In all CQ, LP, HSS overcurrent and HSS reverse polarity fault conditions, if the fault condition exists for $t > t_{SC}$ (blanking time), the device will detect a fault. In the case that auto recovery is disabled, the status and interrupt registers will reflect the fault status, but the device will not disable the driver until a TSD fault occurs. When auto recovery is enabled, based on the count value in the CQ_DRV_MAX_AR, LP_MAX_AR, HSS_MAX_AR registers, auto recovery will be attempted. If the count value is 0, auto recovery will be attempted indefinitely, and otherwise, the auto recovery will be attempted for the count value.

Once auto recovery fails the number of attempts in these registers, this feature must be disabled and re-enabled by configuring the CQ_DRV_AR_DIS, LP_AR_DIS and HSS_AR_DIS bits. Only after configuring these bits, will the corresponding driver be re-enabled.

LED Driver

The device integrates NPN LED drivers, suitable for widely used common anode RGB LEDs. The device is equipped with PWM (pulse width) and I_{DRV} (max current) configurability to control the output average current, in order to achieve the required colors.

PWM frequency = **225Hz**

Config	Exponential DC Scaling %	On Time (S)	Off Time (S)	Avg Current (mA) IDR _V = 2mA	Avg Current (mA) IDR _V = 8mA	Avg Current (mA) IDR _V = 14mA	Avg Current (mA) IDR _V = 20mA
0	0	0.00E+00	4.44E-03	0	0	0	0
1	1.4	6.21E-05	4.38E-03	0.027954102	0.111816406	0.195678711	0.279541016
2	1.8	7.98E-05	4.36E-03	0.035888672	0.143554688	0.251220703	0.358886719
3	2.5	1.11E-04	4.33E-03	0.049926758	0.199707031	0.349487305	0.499267578
4	3.4	1.51E-04	4.29E-03	0.067993164	0.271972656	0.475952148	0.679931641
5	4.6	2.04E-04	4.24E-03	0.091918945	0.367675781	0.643432617	0.919189453
6	6.3	2.80E-04	4.16E-03	0.125976563	0.50390625	0.881835938	1.259765625
7	8.6	3.82E-04	4.06E-03	0.17199707	0.687988281	1.203979492	1.719970703
8	11	4.89E-04	3.96E-03	0.219970703	0.879882813	1.539794922	2.199707031
9	16	7.11E-04	3.73E-03	0.319946289	1.279785156	2.239624023	3.199462891
10	22	9.78E-04	3.47E-03	0.439941406	1.759765625	3.079589844	4.399414063
11	29	1.29E-03	3.16E-03	0.579956055	2.319824219	4.059692383	5.799560547
12	40	1.78E-03	2.67E-03	0.799926758	3.199707031	5.599487305	7.999267578
13	54	2.40E-03	2.04E-03	1.079956055	4.319824219	7.559692383	10.79956055
14	74	3.29E-03	1.16E-03	1.479980469	5.919921875	10.35986328	14.79980469
15	100	4.44E-03	0.00E+00	2	8	14	20

Faults/Interrupts/Status Handling

All interrupts are logged by default in the corresponding IREQ register at the rising edge of that event . The effect of the IREQ register on the IRQ pin is controlled by the corresponding IMASK register. For example, the CLIREQ logs all listed interrupts, but its effect on the IRQ pin is enabled and disabled using the CLIMASK register.

S No	Category	Sub Category	Acronym	Description	Interrupt Clear Method
1	Device Fault	Fault	VCC_OV	VCC Over Voltage	Clear on Read
2		Fault	VCC_WARN	VCC Warning	Clear on Read
3		Fault	VCC_UVLO	VCC Undervoltage	Clear on Read
4	Channel Fault	Fault	OT_FAULT	Channel level over temperature fault	Clear on Read
5		Status	OT_WARN	Channel level over temperature warning	Clear on Read
6		Fault	CQ_OC	CQ driver overcurrent	Clear on Read
7		Fault	LP_OC	Lplus supply overcurrent	Clear on Read
8		Fault	LP_UVLO	Lplus supply undervoltage lockout	Clear on Read
9		Fault	CQx_AR	CQ Overcurrent auto recovery failed after max retries	Clear on Read
10		Fault	LPx_AR	LP Overcurrent auto recovery failed after max retries	Clear on Read
11		Fault	HSSx_AR	HSS Overcurrent or Reverse Polarity auto recovery failed after max retries	Clear on Read

S No	Category	Sub Category	Acronym	Description	Interrupt Clear Method
12	Channel Interrupt - PHY	Interrupt	CQ_F	CQ Fell	Clear on Read
13		Interrupt	CQ_R	CQ Rose	Clear on Read
14		Interrupt	DI_F	DI Fell	Clear on Read
15		Interrupt	DI_R	DI Rose	Clear on Read
16		Interrupt	ASEQ_OK	Wake pulse Generated	Clear on Read
17		Error	RPD_ERR	Establish Communication Sequence Error	Clear on Read
18		Error	WPG_ERR	Establish Communication Sequence Complete	Clear on Read
19		Error	ECS_ERR	Establish Communication Sequence Error * ECS No response	Clear on Read
20		Status	CQ_RXD	CQ RXD level	
21		Status	DI_RXD	DI RXD level	
22		Status	TXD	TXD level	
23		Status	TXEN	TXEN level	
24	Channel Interrupt - UART	Interrupt	RX_RDY	Received Byte Ready	Clear if RX Buffer is empty or Clear on read
25		Interrupt	TX_RDY	Transmitter Ready	Clear if TX not ready or Clear on read
26		Error	OR_ERR	Overrun Error	Clear on Read
27		Error	RX_ERR	Parity or Frame Error	Clear on Read
28		Error	TX_ERR	Transmission Error (Tx Byte != CQ Byte)	Clear on Read

S No	Category	Sub Category	Acronym	Description	Interrupt Clear Method
29	Channel Interrupt - FH	Interrupt	MSG_RDY	IOLINK Message Ready for Reading	Clear if RX Buffer is empty or Clear on read
30		Interrupt	BLVL_RT	Buffer Level Reached configured trigger level (Combined TX & RX Buffer level trigger) Note: To disable specific tx or rx trigger, use a trigger value greater than 128	Clear if rx buffer is below configured level or Clear if tx buffer level is above configured level or Clear on read
31		Interrupt	SOR	Start of Reception	Clear on Read
32		Interrupt	SOT	Start of Transmission	Clear on Read
33		Interrupt	TBUF_EMPTY_AT_CT_EXP	Transmit Buffer Empty at Cycle Timer Expiry	Clear on Read
34		Error	CKSM_ERR	Checksum Error	Clear on Read
35		Error	T1_TA_T2_TO_ERR	Response Time tA or Frame Delay t1 or t2 Timeout Error	Clear on Read
36		Error	TRX_ERR	Transmission or Reception Error * TX Byte != CQ Byte * Parity or Frame Error	Clear on Read
37		Status	STATE	FSM State * IDLE * TXING * RXING	

S No	Category	Sub Category	Acronym	Description	Interrupt Clear Method
38	Channel Interrupt - EFH	Error	TX_ERR	Transmission Error (Tx Byte != CQ Byte)	Clear on Read
39		Error	RX_ERR	Parity or Frame Error	Clear on Read
40		Error	OR_ERR	Overrun Error (Received CQ message, when RX buffer is full)	Clear on Read
41		Interrupt	RX_BFULL	RX Buffer is full	Clear on Read
42		Interrupt	TX_BEMPTY	TX Buffer is empty	Clear on Read
43		Interrupt	RX_BVLV_RATL	RX Buffer rose above trigger level	Clear if rx buffer fell below configured trigger level or Clear on Read
44		Interrupt	TX_BVLV_FBTL	TX Buffer fell below trigger level	Clear if tx buffer rose above configured trigger level or Clear on Read

7.3.10 SPI Communication

Controlling the device via SPI can be handled via normal SPI mode, with one target and one register read and write, but for flexibility and to maximize throughput on the SPI bus, the device also supports alternative modes. Both broadcast and burst modes are supported to minimize overhead of the host MCU.

Normal unicast mode enables read and writes to one device and one register based on the hardware address and register address.

Global broadcast ignores the hardware address bits and implements the write command across all devices sharing a CS line. This allows the user to write defaults quickly for the whole system with one command.

Burst mode increments either the byte or bank address (depending on the mode) to write or read multiple registers with a single command. Byte burst mode increments the register address by 1, while bank burst mode increments to the next bank (device bank, channel A bank, channel B bank).

Burst mode and broadcast mode can be used together, to write the configuration to all devices in the system, across multiple registers, with one SPI command. SDI bytes are returned during write to validate the data written.

Note: In broadcast, the SPI SDO loop back to verify written data cannot be used.

7.3.11 SPI Modes and Frame Formats

SDI	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BYTE0	Global Broadcast	HW ADDR		R/W	Register Address (MSB Nibble)			
BYTE1	Register Address (LSB Nibble)				Reserved		Broadcast Mode	Burst Mode
BYTE2	Write Data or Read Padding							
.	Write Data or Read Padding							
.	Write Data or Read Padding							
BYTEN	Write Data or Read Padding							

SDI Fields

Global Broadcast

0 – Unicast (target hardware addressed device will receive the message)

1 – Broadcast (a;; hardware addressed devices will receive the message)

Hardware Address (HW ADDR)

2-bit device address (to identify multiple devices using common chip select)

R/W

0 – Write

1 – Read

Register Address

8-bit address used to address the register space

Broadcast Mode

0 – Device – Broadcast to all connected devices

Writing to channel A will affect all connected channel As and writing to B will affect all the connected channel Bs

1 – Channel – Broadcast to all connected device channels

Writing on channel A will affect both channels & writing on channel B will affect both channels

Burst Mode

00 – No burst (single target address R/W, with no address increment)

01 – 1-byte address increment Burst Mode (each write increments the register address + 1, with roll over at 0xFF)

10 – 1-bank address increment Burst Mode (each write increments the register address + 32, with roll over at 0x5F)

11 – Reserved

SPI Mode Select

Global Broadcast	R/W	Burst Mode	SPI Mode
0	1/0	00	Unicast Non-Burst Read/Write
0	1/0	01	Unicast Byte Burst Read/Write (+1 Address)
0	1/0	10	Unicast Bank Burst Read/Write (+32 Address)
1	0	00	Broadcast Non-Burst Write
1	0	01	Broadcast Byte Burst Write (+1 Address)
1	0	10	Broadcast Bank Burst Write (+32 Address)

SDO Unicast Read Frame Format

SDO	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BYTE0	HiZ			Device Fault	Channel A OK	Channel A ERR	Channel B OK	Channel B ERR
BYTE1	Channel A CQ_RXD	Channel A DI_RXD	Channel A Fault	Channel A Interrupt	Channel B CQ_RXD	Channel B DI_RXD	Channel B Fault	Channel B Interrupt

BYTE2	DATA 0
.	...
.	...
BYTEN	DATA N

SDO Unicast Write Frame Format

SDO	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BYTE0	HiZ			Device Fault	Channel A OK	Channel A ERR	Channel B OK	Channel B ERR
BYTE1	SDI RETURN BYTE 0 – CMD 0							
BYTE2	SDI RETURN BYTE 1 – CMD 1							
.	SDI RETURN BYTE 2 – DATA 0							
.	...							
BYTEN	SDI RETURN BYTE N – DATA N-1							

SDO Broadcast Read/Write Frame Format

SDO	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BYTE0	HiZ							
.								
.								
BYTEN								

SDO Fields**Device Fault**

Device Fault = VCC_OV | VCC_UVLO

Channel X OK

Channel X OK = ASEQ_OK | RX_RDY | (MSG_RDY | BLVL_RT) | (RX_BLVL_RATL | TX_BLVL_FBTl)

Channel X ERR

Channel X ERR =

(ECS_ERR | WPG_ERR | RPD_ERR) |

(TX_ERR | RX_ERR | OR_ERR) |

(TRX_ERR | TA_T2_TO_ERR | CKSM_ERR) |

(TX_ERR | RX_ERR | OR_ERR)

Channel X CQ_RXD

CQ_RXD value

Channel X DI_RXD

DI_RXD value

Channel X Fault

Channel X Fault = OT_FAULT | EXT_CQ_OC | CQ_OC | LP_OC | LP_UVLO | CQ_AR | LP_AR | HSS_AR

Channel X Interrupt

Channel X Interrupt =
(CQ_R|CQ_F|DI_R|DI_F) |
(TBUF_EMPTY_AT_CT_EXP|SOT|SOR) |
(RX_BFULL | TX_BEMPTY)

7.3.12 Memory and Registry Maps

Memory Map

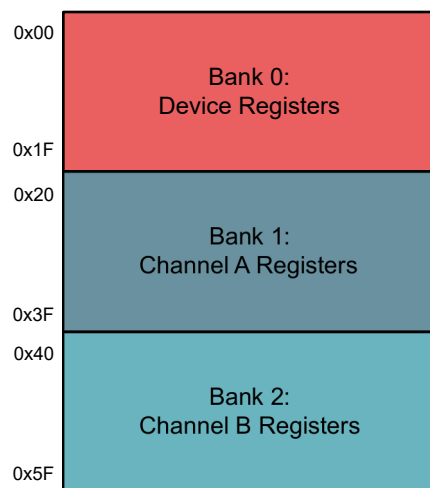


Figure 7-3. TIOM221x Memory Map

7.3.12.1 device Registers

Table 7-3 lists the memory-mapped registers for the device registers. All register offset addresses not listed in Table 7-3 should be considered as reserved locations and the register contents should not be modified.

Table 7-3. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	Revision Identifier	Device revision identifier	Section 7.3.12.1.1
1h	Clock Configuration	System clock configuration	Section 7.3.12.1.2
2h	Device Logic Interrupt Mask		Section 7.3.12.1.3
3h	Device Phy Interrupt Mask		Section 7.3.12.1.4
4h	Device Control		Section 7.3.12.1.5
5h	Synchronization	Device channels soft master trigger synchronizer	Section 7.3.12.1.6
6h	DEV6		Section 7.3.12.1.7
7h	DEV7		Section 7.3.12.1.8
8h	DEV8		Section 7.3.12.1.9
9h	DEV9		Section 7.3.12.1.10
Ah	DEV10		Section 7.3.12.1.11
Bh	DEV11		Section 7.3.12.1.12
Ch	DEV12		Section 7.3.12.1.13
Dh	DEV13		Section 7.3.12.1.14
Eh	DEV14		Section 7.3.12.1.15
Fh	DEV15		Section 7.3.12.1.16
10h	DEV16		Section 7.3.12.1.17
11h	DEV17		Section 7.3.12.1.18
12h	DEV18		Section 7.3.12.1.19
13h	DEV19		Section 7.3.12.1.20
14h	DEV20		Section 7.3.12.1.21
15h	DEV21		Section 7.3.12.1.22
16h	Device Logic Status		Section 7.3.12.1.23
17h	Device Phy Status		Section 7.3.12.1.24
18h	Device Logic Interrupt Request		Section 7.3.12.1.25
19h	Device Phy Interrupt Request		Section 7.3.12.1.26
1Ah	DEV26		Section 7.3.12.1.27
1Bh	Extended Feature Support 0		Section 7.3.12.1.28
1Ch	Extended Feature Support 1		Section 7.3.12.1.29
1Dh	CQ Driver Max Auto Recovery		Section 7.3.12.1.30
1Eh	LP Max Auto Recovery		Section 7.3.12.1.31
1Fh	HSS Max Auto Recovery		Section 7.3.12.1.32

Complex bit access types are encoded to fit into small table cells. Table 7-4 shows the codes that are used for access types in this section.

Table 7-4. device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		

Table 7-4. device Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.3.12.1.1 Revision Identifier Register (Offset = 0h) [Reset = 00h]

Revision Identifier is shown in [Table 7-5](#).

Return to the [Summary Table](#).

Table 7-5. Revision Identifier Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MAJOR	R	0h	Major device revision identifier Identifies full-layer die revision 0h = revision 0 (original release) 1h = revision 1 2h = revision 2 3h = revision 3 4h = revision 4 5h = revision 5 6h = revision 6 7h = revision 7 8h = revision 8 9h = revision 9 Ah = revision 10 Bh = revision 11 Ch = revision 12 Dh = revision 13 Eh = revision 14 Fh = revision 15
3-0	MINOR	R	0h	Minor device revision identifier Identifies metal-layer die revision 0h = revision 0 (original release) 1h = revision 1 2h = revision 2 3h = revision 3 4h = revision 4 5h = revision 5 6h = revision 6 7h = revision 7 8h = revision 8 9h = revision 9 Ah = revision 10 Bh = revision 11 Ch = revision 12 Dh = revision 13 Eh = revision 14 Fh = revision 15

7.3.12.1.2 Clock Configuration Register (Offset = 1h) [Reset = 00h]

Clock Configuration is shown in [Table 7-6](#).

Return to the [Summary Table](#).

Table 7-6. Clock Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-4	ESR	R/W	0h	Effective series resistance select Sets the effective series resistance used in current sensing for the L+ supply driver; see [section X.Y] for more information 0h = 200 andx3A9;# 1h = 100 andx3A9;# 2h = 75 andx3A9;# 3h = 50 andx3A9;#
3	CLKO_EN	R/W	0h	Clock output enable Enables output of internal oscillator on CLKO pin 0h = CLKO pin is high impedance 1h = internal crystal oscillator clock output on CLKO pin
2	CLKIN_EN	R/W	0h	Clock input enable Enables dependence of external clock on CLKIN pin 0h = CLKIN input is ignored 1h = external clock input on CLKIN pin expected
1	RESERVED	R	0h	Reserved
0	XTAL_EN	R/W	0h	Crystal oscillator enable Enables internal oscillator 0h = crystal oscillator disabled 1h = crystal oscillator enabled

7.3.12.1.3 Device Logic Interrupt Mask Register (Offset = 2h) [Reset = 00h]

Device Logic Interrupt Mask is shown in [Table 7-7](#).

Return to the [Summary Table](#).

Table 7-7. Device Logic Interrupt Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MASK	R/W	0h	Device logic interrupt mask Sets mask to ignore interrupt events; see [section] for more details 0h = interrupt not masked 1h = interrupt masked

7.3.12.1.4 Device Phy Interrupt Mask Register (Offset = 3h) [Reset = 00h]

Device Phy Interrupt Mask is shown in [Table 7-8](#).

Return to the [Summary Table](#).

Table 7-8. Device Phy Interrupt Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MASK	R/W	0h	Device physical interrupt mask Sets mask to ignore interrupt events; see [section] for more details 0h = interrupt not masked 1h = interrupt masked

7.3.12.1.5 Device Control Register (Offset = 4h) [Reset = 00h]

Device Control is shown in [Table 7-9](#).

Return to the [Summary Table](#).

Table 7-9. Device Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	EN	R/W	0h	Device enable Enables device 0h = device disabled 1h = device enabled
0	RST	W	0h	Device digital soft reset Resets device 0h = normal operation 1h = digital reset

7.3.12.1.6 Synchronization Register (Offset = 5h) [Reset = 00h]

Synchronization is shown in [Table 7-10](#).

Return to the [Summary Table](#).

Table 7-10. Synchronization Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	LED_SYNC	W	0h	Sync all LED Synchronize all LED's 0h = LEDs not synchronized 1h = LEDs synchronized
3-2	RESERVED	R	0h	Reserved
1	SYNCB	W	0h	Channel B sync control Triggers the immediate transfer of data in the TX buffer 0h = no transmission 1h = transmit data
0	SYNCA	W	0h	Channel A sync control Triggers the immediate transfer of data in the TX buffer 0h = no transmission 1h = transmit data

7.3.12.1.7 DEV6 Register (Offset = 6h) [Reset = 00h]

DEV6 is shown in [Table 7-11](#).

Return to the [Summary Table](#).

Table 7-11. DEV6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.8 DEV7 Register (Offset = 7h) [Reset = 00h]

DEV7 is shown in [Table 7-12](#).

Return to the [Summary Table](#).

Table 7-12. DEV7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.9 DEV8 Register (Offset = 8h) [Reset = 00h]

DEV8 is shown in [Table 7-13](#).

Return to the [Summary Table](#).

Table 7-13. DEV8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.10 DEV9 Register (Offset = 9h) [Reset = 00h]

DEV9 is shown in [Table 7-14](#).

Return to the [Summary Table](#).

Table 7-14. DEV9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.11 DEV10 Register (Offset = Ah) [Reset = 00h]

DEV10 is shown in [Table 7-15](#).

Return to the [Summary Table](#).

Table 7-15. DEV10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.12 DEV11 Register (Offset = Bh) [Reset = 00h]

DEV11 is shown in [Table 7-16](#).

Return to the [Summary Table](#).

Table 7-16. DEV11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.13 DEV12 Register (Offset = Ch) [Reset = 00h]

DEV12 is shown in [Table 7-17](#).

Return to the [Summary Table](#).

Table 7-17. DEV12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.14 DEV13 Register (Offset = Dh) [Reset = 00h]

DEV13 is shown in [Table 7-18](#).

Return to the [Summary Table](#).

Table 7-18. DEV13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.15 DEV14 Register (Offset = Eh) [Reset = 00h]

DEV14 is shown in [Table 7-19](#).

Return to the [Summary Table](#).

Table 7-19. DEV14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.16 DEV15 Register (Offset = Fh) [Reset = 00h]

DEV15 is shown in [Table 7-20](#).

Return to the [Summary Table](#).

Table 7-20. DEV15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.17 DEV16 Register (Offset = 10h) [Reset = 00h]

DEV16 is shown in [Table 7-21](#).

Return to the [Summary Table](#).

Table 7-21. DEV16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.18 DEV17 Register (Offset = 11h) [Reset = 00h]

DEV17 is shown in [Table 7-22](#).

Return to the [Summary Table](#).

Table 7-22. DEV17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.19 DEV18 Register (Offset = 12h) [Reset = 00h]

DEV18 is shown in [Table 7-23](#).

Return to the [Summary Table](#).

Table 7-23. DEV18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.20 DEV19 Register (Offset = 13h) [Reset = 00h]

DEV19 is shown in [Table 7-24](#).

Return to the [Summary Table](#).

Table 7-24. DEV19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.21 DEV20 Register (Offset = 14h) [Reset = 00h]

DEV20 is shown in [Table 7-25](#).

Return to the [Summary Table](#).

Table 7-25. DEV20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.22 DEV21 Register (Offset = 15h) [Reset = 00h]

DEV21 is shown in [Table 7-26](#).

Return to the [Summary Table](#).

Table 7-26. DEV21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.23 Device Logic Status Register (Offset = 16h) [Reset = 00h]

Device Logic Status is shown in [Table 7-27](#).

Return to the [Summary Table](#).

Table 7-27. Device Logic Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CQB_AR	R	0h	C/Q channel B overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field CQB_DRV_MAX_AR 0h = limit not reached 1h = limit reached
6	CQA_AR	R	0h	C/Q channel A overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field CQA_DRV_MAX_AR 0h = limit not reached 1h = limit reached
5	LPB_AR	R	0h	L+ channel B overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field LPB_MAX_AR 0h = limit not reached 1h = limit reached
4	LPA_AR	R	0h	L+ channel A overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field LPA_MAX_AR 0h = limit not reached 1h = limit reached
3	HSSB_AR	R	0h	High side switch (HSS) channel B overcurrent/reverse polarity recovery retry limit reached Indicates driver has reached maximum number of retries from field HSSB_MAX_AR 0h = limit not reached 1h = limit reached
2	HSSA_AR	R	0h	High side switch (HSS) channel A overcurrent/reverse polarity recovery retry limit reached Indicates driver has reached maximum number of retries from field HSSA_MAX_AR 0h = limit not reached 1h = limit reached
1	XTAL_OR_EXT_GOOD	R	0h	Internal crystal or external clock good Indicates internal crystal or external clock has achieved initialization 0h = initialization not complete 1h = initialization complete
0	INIT_DONE	R	0h	Device initialization complete Indicates device has completed startup and is ready to begin communication 0h = initialization not complete 1h = initialization complete

7.3.12.1.24 Device Phy Status Register (Offset = 17h) [Reset = 00h]

Device Phy Status is shown in [Table 7-28](#).

Return to the [Summary Table](#).

Table 7-28. Device Phy Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	LPB_WARN	R	0h	LPB Warning LPB Warning 0h = no LPB warning 1h = LPB warning
4	LPA_WARN	R	0h	LPA Warning LPA Warning 0h = no LPA warning 1h = LPA warning
3	RESERVED	R	0h	Reserved
2	VCC_OV	R	0h	VCC over voltage status Indicates voltage on VCC pin has exceeded overvoltage limit [more details on OV limit] 0h = limit not reached 1h = limit reached
1	VCC_WARN	R	0h	VCC under voltage warning Indicates voltage on VCC pin has decreased below undervoltage warning limit [more details on UV limit] 0h = limit not reached 1h = limit reached
0	VCC_UVLO	R	0h	VCC UVLO status Indicates voltage on VCC pin has decreased below UVLO limit [more details on UV limit] 0h = limit not reached 1h = limit reached

7.3.12.1.25 Device Logic Interrupt Request Register (Offset = 18h) [Reset = 00h]

Device Logic Interrupt Request is shown in [Table 7-29](#).

Return to the [Summary Table](#).

Table 7-29. Device Logic Interrupt Request Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CQB_AR	RC	0h	C/Q channel B overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field CQB_DRV_MAX_AR 0h = limit not reached 1h = limit reached
6	CQA_AR	RC	0h	C/Q channel A overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field CQA_DRV_MAX_AR 0h = limit not reached 1h = limit reached
5	LPB_AR	RC	0h	L+ channel B overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field LPB_MAX_AR 0h = limit not reached 1h = limit reached
4	LPA_AR	RC	0h	L+ channel A overcurrent recovery retry limit reached Indicates driver has reached maximum number of retries from field LPA_MAX_AR 0h = limit not reached 1h = limit reached
3	HSSB_AR	RC	0h	High side switch (HSS) channel B overcurrent/reverse polarity recovery retry limit reached Indicates driver has reached maximum number of retries from field HSSB_MAX_AR 0h = limit not reached 1h = limit reached
2	HSSA_AR	RC	0h	High side switch (HSS) channel A overcurrent/reverse polarity recovery retry limit reached Indicates driver has reached maximum number of retries from field HSSA_MAX_AR 0h = limit not reached 1h = limit reached
1	XTAL_OR_EXT_GOOD_CHANGE	RC	0h	Change in Internal crystal or external clock good Indicates internal crystal or external clock has changed 0h = no change in clock 1h = change in clock
0	INIT_DONE	RC	0h	Device initialization complete Indicates device has completed startup and is ready to begin communication 0h = initialization not complete 1h = initialization complete

7.3.12.1.26 Device Phy Interrupt Request Register (Offset = 19h) [Reset = 00h]

Device Phy Interrupt Request is shown in [Table 7-30](#).

Return to the [Summary Table](#).

Table 7-30. Device Phy Interrupt Request Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	RC	0h	Reserved
6	RESERVED	RC	0h	Reserved
5	LPB_WARN	RC	0h	LPB Warning LPB Warning 0h = no LPB warning 1h = LPB warning
4	LPA_WARN	RC	0h	LPA Warning LPA Warning 0h = no LPA warning 1h = LPA warning
3	RESERVED	RC	0h	Reserved
2	VCC_OV	RC	0h	VCC over voltage status Indicates voltage on VCC pin has exceeded overvoltage limit [more details on OV limit] 0h = limit not reached 1h = limit reached
1	VCC_WARN	RC	0h	VCC under voltage warning Indicates voltage on VCC pin has decreased below undervoltage warning limit [more details on UV limit] 0h = limit not reached 1h = limit reached
0	VCC_UVLO	RC	0h	VCC UVLO status Indicates voltage on VCC pin has decreased below UVLO limit [more details on UV limit] 0h = limit not reached 1h = limit reached

7.3.12.1.27 DEV26 Register (Offset = 1Ah) [Reset = 00h]

DEV26 is shown in [Table 7-31](#).

Return to the [Summary Table](#).

Table 7-31. DEV26 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0h	Reserved

7.3.12.1.28 Extended Feature Support 0 Register (Offset = 1Bh) [Reset = 00h]

Extended Feature Support 0 is shown in [Table 7-32](#).

Return to the [Summary Table](#).

Table 7-32. Extended Feature Support 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	Reserved
2	FH_TX_CKSM_ERR_DIS	R/W	0h	Disable Frame Handler TX Checksum Error 0h = checksum error detection enabled 1h = checksum error detection disabled
1	FH_T1_TA_T2_DIS	R/W	0h	Disable Frame Handler T1, TA and T2 Timeouts 0h = timeout detection enabled 1h = timeout detection disabled
0	TRX_ERR_DIS	R/W	0h	Disable Transmission Error Check 0h = transmission error detection enabled 1h = transmission error detection disabled

7.3.12.1.29 Extended Feature Support 1 Register (Offset = 1Ch) [Reset = 00h]

Extended Feature Support 1 is shown in [Table 7-33](#).

Return to the [Summary Table](#).

Table 7-33. Extended Feature Support 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSSB_TSC_DIS	R/W	0h	HSSB Blanking Time Disable 0h = blanking time enabled 1h = blanking time disabled
6	LPB_TSC_DIS	R/W	0h	LPB Blanking Time Disable 0h = blanking time enabled 1h = blanking time disabled
5	CQB_TSC_DIS	R/W	0h	CQB Blanking Time Disable 0h = blanking time enabled 1h = blanking time disabled
4	EXTD_COM_B	R/W	0h	Channel B Extended COM Rate Support Enable 0h = extended COM rate support enabled 1h = extended COM rate support disabled
3	HSSA_TSC_DIS	R/W	0h	HSSA Blanking Time Disable 0h = blanking time enabled 1h = blanking time disabled
2	LPA_TSC_DIS	R/W	0h	LPA Blanking Time Disable 0h = blanking time enabled 1h = blanking time disabled
1	CQA_TSC_DIS	R/W	0h	CQA Blanking Time Disable 0h = blanking time enabled 1h = blanking time disabled
0	EXTD_COM_A	R/W	0h	Channel A Extended COM Rate Support Enable 0h = extended COM rate support enabled 1h = extended COM rate support disabled

7.3.12.1.30 CQ Driver Max Auto Recovery Register (Offset = 1Dh) [Reset = 00h]

CQ Driver Max Auto Recovery is shown in [Table 7-34](#).

Return to the [Summary Table](#).

Table 7-34. CQ Driver Max Auto Recovery Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CQB_DRV_MAX_AR	R/W	0h	C/Q channel B driver maximum auto recovery Sets the maximum number of times the driver will attempt to recover from an overcurrent fault 0h = unlimited retries 1h = 1 retry 2h = 2 retries 3h = 3 retries 4h = 4 retries 5h = 5 retries 6h = 6 retries 7h = 7 retries 8h = 8 retries 9h = 9 retries Ah = 10 retries Bh = 11 retries Ch = 12 retries Dh = 13 retries Eh = 14 retries Fh = 15 retries
3-0	CQA_DRV_MAX_AR	R/W	0h	C/Q channel A driver maximum auto recovery Sets the maximum number of times the driver will attempt to recover from an overcurrent fault 0h = unlimited retries 1h = 1 retry 2h = 2 retries 3h = 3 retries 4h = 4 retries 5h = 5 retries 6h = 6 retries 7h = 7 retries 8h = 8 retries 9h = 9 retries Ah = 10 retries Bh = 11 retries Ch = 12 retries Dh = 13 retries Eh = 14 retries Fh = 15 retries

7.3.12.1.31 LP Max Auto Recovery Register (Offset = 1Eh) [Reset = 00h]

LP Max Auto Recovery is shown in [Table 7-35](#).

Return to the [Summary Table](#).

Table 7-35. LP Max Auto Recovery Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LPB_MAX_AR	R/W	0h	L+ channel B driver maximum auto recovery Sets the maximum number of times the driver will attempt to recover from an overcurrent fault 0h = unlimited retries 1h = 1 retry 2h = 2 retries 3h = 3 retries 4h = 4 retries 5h = 5 retries 6h = 6 retries 7h = 7 retries 8h = 8 retries 9h = 9 retries Ah = 10 retries Bh = 11 retries Ch = 12 retries Dh = 13 retries Eh = 14 retries Fh = 15 retries
3-0	LPA_MAX_AR	R/W	0h	L+ channel A driver maximum auto recovery Sets the maximum number of times the driver will attempt to recover from an overcurrent fault 0h = unlimited retries 1h = 1 retry 2h = 2 retries 3h = 3 retries 4h = 4 retries 5h = 5 retries 6h = 6 retries 7h = 7 retries 8h = 8 retries 9h = 9 retries Ah = 10 retries Bh = 11 retries Ch = 12 retries Dh = 13 retries Eh = 14 retries Fh = 15 retries

7.3.12.1.32 HSS Max Auto Recovery Register (Offset = 1Fh) [Reset = 00h]

HSS Max Auto Recovery is shown in [Table 7-36](#).

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Table 7-36. HSS Max Auto Recovery Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HSSB_MAX_AR	R/W	0h	High side switch channel B driver maximum auto recovery Sets the maximum number of times the driver will attempt to recover from an overcurrent fault 0h = unlimited retries 1h = 1 retry 2h = 2 retries 3h = 3 retries 4h = 4 retries 5h = 5 retries 6h = 6 retries 7h = 7 retries 8h = 8 retries 9h = 9 retries Ah = 10 retries Bh = 11 retries Ch = 12 retries Dh = 13 retries Eh = 14 retries Fh = 15 retries
3-0	HSSA_MAX_AR	R/W	0h	High side switch channel A driver maximum auto recovery Sets the maximum number of times the driver will attempt to recover from an overcurrent fault 0h = unlimited retries 1h = 1 retry 2h = 2 retries 3h = 3 retries 4h = 4 retries 5h = 5 retries 6h = 6 retries 7h = 7 retries 8h = 8 retries 9h = 9 retries Ah = 10 retries Bh = 11 retries Ch = 12 retries Dh = 13 retries Eh = 14 retries Fh = 15 retries

7.3.12.2 channel Registers

Table 7-37 lists the memory-mapped registers for the channel registers. All register offset addresses not listed in Table 7-37 should be considered as reserved locations and the register contents should not be modified.

Table 7-37. CHANNEL Registers

Offset	Acronym	Register Name	Section
0h	CQ Driver Configuration	Phy Config	Section 7.3.12.2.1
1h	CQ Driver, Receiver Configuration	Phy Config	Section 7.3.12.2.2
2h	CQ Driver, DI Receiver Configuration	Phy Config	Section 7.3.12.2.3
3h	CQ Driver, Lplus Supply Configuration	Phy Config	Section 7.3.12.2.4
4h	Lplus Supply Configuration	Phy Config	Section 7.3.12.2.5
5h	High Side Switch Configuration 0	Phy Config	Section 7.3.12.2.6
6h	High Side Switch Configuration 1	Phy Config	Section 7.3.12.2.7
7h	Alternate Function Select Configuration	Phy Config	Section 7.3.12.2.8
8h	Channel Logic Interrupt Mask	Logic Config	Section 7.3.12.2.9
9h	Channel Phy Interrupt Mask	Logic Config	Section 7.3.12.2.10
Ah	RPD, Offset Timer Configuration	Logic Config	Section 7.3.12.2.11
Bh	Common Logic Configuration	Logic Config	Section 7.3.12.2.12
Ch	IOLink Phy Mode Control	Logic Control	Section 7.3.12.2.13
Dh	UART Mode Control	Uart Data	Section 7.3.12.2.14
Eh	Frame Handler Mode Control	Frame Handler Config and Control	Section 7.3.12.2.15
Fh	FH + EFH Mode RX Buffer Trigger Level	Trigger Buffer Level	Section 7.3.12.2.16
10h	FH + EFH Mode TX Buffer Trigger Level	Cycle Timer	Section 7.3.12.2.17
11h	On Demand data Length	Logic Control	Section 7.3.12.2.18
12h	Master Process Data Length	Logic Control	Section 7.3.12.2.19
13h	Device Process Data Length	Logic Control	Section 7.3.12.2.20
14h	FH Mode Cycle Timer Control	Logic Control	Section 7.3.12.2.21
15h	FH Mode Data	Logic Control	Section 7.3.12.2.22
16h	Channel Logic Status	Muxed Status (PHY, UART, FH)	Section 7.3.12.2.23
17h	Channel Phy Status	Phy Status (Ext CQ, CQ, LP)	Section 7.3.12.2.24
18h	Channel Logic Interrupt REQuest	Muxed Interrupt Request (PHY, UART, FH)	Section 7.3.12.2.25
19h	Channel Physical Interrupt REQuest	Interrupt Request (Ext CQ, CQ, LP)	Section 7.3.12.2.26
1Ah	LED Config 1	LED Config / Control	Section 7.3.12.2.27
1Bh	LED Config 2	LED Config / Control	Section 7.3.12.2.28
1Ch	LED Config 3	LED Config / Control	Section 7.3.12.2.29
1Dh	LED Config 4	LED Config / Control	Section 7.3.12.2.30
1Eh	LED Config 5	LED Config / Control	Section 7.3.12.2.31
1Fh	LED Config 6	LED Config / Control	Section 7.3.12.2.32

Complex bit access types are encoded to fit into small table cells. Table 7-38 shows the codes that are used for access types in this section.

Table 7-38. channel Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		

Table 7-38. channel Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.3.12.2.1 CQ Driver Configuration Register (Offset = 0h) [Reset = 00h]

CQ Driver Configuration is shown in [Table 7-39](#).

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Table 7-39. CQ Driver Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-5	CQ_DRV_TSC	R/W	0h	Driver current blanking time Sets the C/Q driver's duration for blanking. See [section] for more information. 0h = 5ms 1h = 15ms 2h = 50ms 3h = 150ms
4-3	CQ_DRV_CLIM	R/W	0h	Driver current limit Sets the C/Q driver's output current limit. 0h = 500mA 1h = 300mA 2h = 200mA 3h = 100mA
2-1	CQ_DRV_TAR	R/W	0h	Driver current auto retry time Sets the C/Q driver's duration to wait after a fault before retrying. See [section] for more information. 0h = 50ms 1h = 500ms 2h = 4s 3h = 10s
0	CQ_DRV_AR_DIS	R/W	0h	Driver auto retry disable Disables the C/Q driver's attempt to automatically retry. 0h = Driver auto retry enabled 1h = Driver auto retry disabled

7.3.12.2.2 CQ Driver, Receiver Configuration Register (Offset = 1h) [Reset = 00h]

CQ Driver, Receiver Configuration is shown in [Table 7-40](#).

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Table 7-40. CQ Driver, Receiver Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CQ_NO_INV	R/W	0h	Disable TX to C/Q and C/Q to RX Inversion 0h = Inversion Enabled 1h = Inversion Disabled
6-5	CQ_SNK_SRC	R/W	0h	Driver sink or source current value Sets the C/Q driver's source and sink value while in receive mode. 0h = 5mA 1h = 2 mA 2h = 150uA 3h = Reserved
4	CQ_SRC_EN	R/W	0h	Driver current source enable Enables the C/Q driver's high-side current source. 0h = current source disabled 1h = current source enabled
3	CQ_SNK_DIS	R/W	0h	Driver current sink enable Enables the C/Q driver's low-side current source. 0h = current sink enabled 1h = current sink disabled
2-1	CQ_RX_VTH_DIS	R/W	0h	C/Q RX threshold select and disable Sets the C/Q pin's type of logic while in receive. See [section] for more information. 0h = Fixed Threshold compliant to IO-Link Standard for all LP range 1h = Ratiometric threshold for LP less-than 18V, fixed threshold for LP greater-than or equal-to 18V 2h = Type 2/3 threshold 3h = RX disabled
0	CQ_GFILT_EN	R/W	0h	C/Q RX glitch filter enable Enables the C/Q pin's receive glitch filtering. See [section] for more information. 0h = CQ RX glitch filter disabled 1h = CQ RX glitch filter enabled

7.3.12.2.3 CQ Driver, DI Receiver Configuration Register (Offset = 2h) [Reset = 00h]

CQ Driver, DI Receiver Configuration is shown in [Table 7-41](#).

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Table 7-41. CQ Driver, DI Receiver Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CQ_DRV_RISE_FALL	R/W	0h	Driver rise/fall time setting Sets the C/Q driver's rise and fall time. 0h = Rise/fall time set to 400ns nominal 1h = Rise/fall time set to 800ns nominal 2h = Rise/fall time set to 1.6us nominal 3h = Rise/fall time set to 3.2us nominal
5	DI_NO_INV	R/W	0h	Disable DI to RX Inversion 0h = Inversion Enabled 1h = Inversion Disabled
4	DI_SRC_EN	R/W	0h	DI RX current source enable Enables the DI pin's high-side current source. 0h = 2mA source disabled 1h = 2mA source enabled
3	DI_SNK_EN	R/W	0h	DI RX current sink enable Enables the DI pin's low-side current source. 0h = 2mA sink disabled 1h = 2mA sink enabled
2-1	DI_RX_VTH_DIS	R/W	0h	DI RX threshold select and disable Sets the DI pin's type of logic while in receive. See [section] for more information. 0h = Fixed Threshold compliant to IO-Link Standard for all LP range 1h = Ratiometric threshold for LP less-than 18V, fixed threshold for LP greater-than or equal-to 18V 2h = Type 2/3 threshold 3h = RX disabled
0	DI_GFILT_EN	R/W	0h	DI RX glitch filter enable Enables the DI pin's receive glitch filtering. See [section] for more information. 0h = DI RX glitch filter disabled 1h = DI RX glitch filter enabled

7.3.12.2.4 CQ Driver, Lplus Supply Configuration Register (Offset = 3h) [Reset = 00h]

CQ Driver, Lplus Supply Configuration is shown in [Table 7-42](#).

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Table 7-42. CQ Driver, Lplus Supply Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	N_DIODE_MD	R/W	0h	N-side blocking diode mode enable 0h = Nside in switch-diode mode 1h = Nside in blocking diode mode
6-5	LP_TSC	R/W	0h	L+ current blanking time Sets the L+ driver's duration for blanking. See [section] for more information. 0h = 5ms 1h = 15ms 2h = 50ms 3h = 150ms
4-3	LP_CLIM	R/W	0h	L+ current limit Sets the L+ driver's output current limit. 0h = 15mV 1h = 30 mV 2h = 60 mV 3h = 120 mV
2-1	LP_TAR	R/W	0h	L+ current auto retry time Sets the L+ driver's duration to wait after a fault before retrying. See [section] for more information. 0h = 50ms 1h = 500ms 2h = 4s 3h = 10s
0	LP_AR_DIS	R/W	0h	L+ auto retry disable Disables the L+ driver's attempt to automatically retry. 0h = LP auto retry enabled 1h = LP auto retry disabled

7.3.12.2.5 Lplus Supply Configuration Register (Offset = 4h) [Reset = 00h]

Lplus Supply Configuration is shown in [Table 7-43](#).

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Table 7-43. Lplus Supply Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7	P_DIODE_MD	R/W	0h	Pside blocking diode mode enable 0h = Pside in switch-diode mode 1h = Pside in blocking diode mode
6-5	RESERVED	R	0h	Reserved
4	LP_GATE_DRV_EN	R/W	0h	L+ gate driver enable Enables the external L+ gate driver. See [section] for more information. 0h = LP gate driver disabled 1h = LP gate driver enabled
3	LP_SNS_EN	R/W	0h	L+ sense enable Enables the sensing functionality for the external L+ gate driver. See [section] for more information. 0h = LP sense disable 1h = LP sense enable
2	LP_DYBL_EN	R/W	0h	L+ dynamic blanking enable Enables dynamic blanking for the external L+ driver. See [section] for more information. 0h = LP dynamic blanking disabled 1h = LP dynamic blanking enabled
1	LP_REG_EN	R/W	0h	L+ current regulation loop enable Enables the current regulation loop for the external L+ driver. See [section] for more information. 0h = LP current regulation loop disabled 1h = LP current regulation loop enabled
0	LP_GATE_HIZ	R/W	0h	L+ gate driver output tristate Sets the external L+ gate driver's output to tristate. 0h = LP gate driver output driven 1h = LP gate driver output tristated

7.3.12.2.6 High Side Switch Configuration 0 Register (Offset = 5h) [Reset = 00h]

High Side Switch Configuration 0 is shown in [Table 7-44](#).

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Table 7-44. High Side Switch Configuration 0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSS_RP_PROT_EN	R/W	0h	HSS reverse polarity protection enable Enables the high-side switch reverse polarity protection. 0h = HSS Reverse Polarity Protection Disable 1h = HSS Reverse Polarity Protection Enable
6-5	HSS_TSC	R/W	0h	HSS current blanking time Sets the external HSS driver's duration for blanking. See [section] for more information. 0h = 5ms 1h = 15ms 2h = 50ms 3h = 150ms
4-3	HSS_CLIM	R/W	0h	HSS current limit Sets the external HSS driver's output current limit. 0h = 15mV 1h = 30 mV 2h = 60 mV 3h = 120 mV
2-1	HSS_TAR	R/W	0h	HSS current auto retry time Sets the external HSS driver's duration to wait after a fault before retrying. See [section] for more information. 0h = 50ms 1h = 500ms 2h = 4s 3h = 10s
0	HSS_AR_DIS	R/W	0h	HSS auto retry disabled Disables the external HSS driver's attempt to automatically retry. 0h = HSS auto retry enabled 1h = HSS auto retry disabled

7.3.12.2.7 High Side Switch Configuration 1 Register (Offset = 6h) [Reset = 01h]

High Side Switch Configuration 1 is shown in [Table 7-45](#).

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Phy Config

Table 7-45. High Side Switch Configuration 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	HSS_CQG1_STATE	R/W	0h	HSS top FET state enable Enables the external HSS top FET state. 0h = HSS top FET state is OFF 1h = HSS top FET state is ON
6	HSS_CQG2_STATE	R/W	0h	HSS bottom FET state Enables the external HSS bottom FET state. 0h = HSS bottom FET state is OFF 1h = HSS bottom FET state is ON
5-4	HSS_SLEW	R/W	0h	HSS switching rate control Sets the external HSS driver's switching rate. 0h = 100 KHz Switching Rate 1h = 10 KHz Switching Rate 2h = Slow Switching 3h = Reserved
3	HSS_SNS_EN	R/W	0h	HSS sense enable Enables the sensing functionality for the external HSS gate driver. See [section] for more information. 0h = HSS Sense Disable 1h = HSS Sense Enable
2	HSS_DYBL_EN	R/W	0h	HSS dynamic blanking enable Enables dynamic blanking for the external HSS driver. See [section] for more information. 0h = HSS dynamic blanking is disabled 1h = HSS dynamic blanking is enabled
1	HSS_REG_EN	R/W	0h	HSS current regulation loop enable Enables the current regulation loop for the external HSS driver. See [section] for more information. 0h = HSS current regulation disabled 1h = HSS current regulation enabled
0	HSS_GATE_HIZ	R/W	1h	HSS gate driver output tristate Sets the external HSS gate driver's output to tristate. 0h = HSS gate driver output driven 1h = HSS gate driver output tristate

7.3.12.2.8 Alternate Function Select Configuration Register (Offset = 7h) [Reset = 00h]

Alternate Function Select Configuration is shown in [Table 7-46](#).

Return to the [Summary Table](#).

Phy Config

Table 7-46. Alternate Function Select Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	LED6_SEL	R/W	0h	LED 6 select 0h = Default Function 1h = LED Function
2	LED5_SEL	R/W	0h	LED 5 select 0h = Default Function 1h = LED Function
1	LED4_SEL	R/W	0h	LED 4 select 0h = Default Function 1h = LED Function
0	LED3_SEL	R/W	0h	LED 3 select 0h = Default Function 1h = LED Function

7.3.12.2.9 Channel Logic Interrupt Mask Register (Offset = 8h) [Reset = 00h]

Channel Logic Interrupt Mask is shown in [Table 7-47](#).

Return to the [Summary Table](#).

Logic Config

Table 7-47. Channel Logic Interrupt Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MASK	R/W	0h	Channel logic interrupt mask 0h = Do not mask interrupt 1h = Mask interrupt

7.3.12.2.10 Channel Phy Interrupt Mask Register (Offset = 9h) [Reset = 00h]

Channel Phy Interrupt Mask is shown in [Table 7-48](#).

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Logic Config

Table 7-48. Channel Phy Interrupt Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MASK	R/W	0h	Channel physical interrupt mask 0h = Do not mask interrupt 1h = Mask interrupt

7.3.12.2.11 RPD, Offset Timer Configuration Register (Offset = Ah) [Reset = 00h]

RPD, Offset Timer Configuration is shown in [Table 7-49](#).

Return to the [Summary Table](#).

Logic Config

Table 7-49. RPD, Offset Timer Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PSC	R/W	0h	Ready pulse detector or offset prescale Sets offset prescale and ready pulse detection. 0h = OFST - 1us; RPD - 1 ms 1h = OFST - 4.34us; RPD - 10 ms 2h = OFST - 10 us; RPD - 100 ms 3h = OFST - 47.74us; RPD -1 S
5-0	COUNT	R/W	0h	Ready pulse detector or offset timer Timeout for Ready Pulse = (COUNT + 1) * PSC time unit Offset Time = COUNT * PSC time unit

7.3.12.2.12 Common Logic Configuration Register (Offset = Bh) [Reset = 00h]

Common Logic Configuration is shown in [Table 7-50](#).

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Logic Config

Table 7-50. Common Logic Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	COM	R/W	0h	Channel COM rate Sets the channel COM rate. Applicable to UART and frame handler modes. 0h = Disabled 1h = COM5 2h = COM2 3h = COM3
5-4	TA	R/W	0h	Response time (tA) Select Sets the duration that the master PHY will wait for the device's first response until throwing a communication error. Applicable to IOLINK PHY AUTOSTART and frame handler modes. 0h = 10 tBIT 1h = 20 tBIT 2h = 40 tBIT 3h = 80 tBIT
3	T2	R/W	0h	Device frame delay (t2) select Sets the duration that the master PHY will wait between device frames until throwing a communication error. Applicable to IOLINK PHY AUTOSTART and frame handler modes. 0h = 3 tBIT 1h = 6 tBIT
2	T1	R/W	0h	Master frame delay (t1) select Sets the duration that the master PHY will wait between master frame transmissions. Applicable to IOLINK PHY AUTOSTART and frame handler modes. 0h = 1 tBIT 1h = 2 tBIT
1-0	CLMD	R/W	0h	Channel logic mode select Sets the channel's logic mode. See [section] for more information. 0h = phy mode 1h = UART mode 2h = frame handler mode 3h = extended frame handler mode

7.3.12.2.13 IOLink Phy Mode Control Register (Offset = Ch) [Reset = 00h]

IOLink Phy Mode Control is shown in [Table 7-51](#).

Return to the [Summary Table](#).

Logic Control

Table 7-51. IOLink Phy Mode Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	AUTO_START	R/W	0h	Auto-start sequence select Sets the sequence that is executed once device initialization is complete. See [section] for more information. 0h = no operation 1h = wake pulse generation 2h = ready pulse detection 3h = ready pulse detection followed by wake pulse generation 4h = establish communication sequence 5h = ready pulse detection followed by establish communication sequence 6h = no operation 7h = abort
4	CQSRC	R/W	0h	CQ Source Select Selects the C/Q driver source in IOLINK PHY mode. 0h = SPI register field control 1h = PIN control
3-2	CQ_MD	R/W	0h	CQ Mode Select with Disable Selects the C/Q mode when the internal driver is selected. 0h = disable CQ driver 1h = NPN mode 2h = PNP mode 3h = push-pull mode
1	CQ_TXD	R/W	0h	CQ TXD Sets C/Q driver state when both in IOLINK PHY mode andbit CQSRC is set to SPI register field control 0h = CQ high 1h = CQ low
0	CQ_TXEN	R/W	0h	CQ TXEN Sets C/Q driver enable state when both in IOLINK PHY mode andbit CQSRC is set to SPI register field control 0h = CQ disable 1h = CQ enable

7.3.12.2.14 UART Mode Control Register (Offset = Dh) [Reset = 00h]

UART Mode Control is shown in [Table 7-52](#).

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Logic Control

Table 7-52. UART Mode Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA	R/W	0h	UART Data Raw UART data read and write register

7.3.12.2.15 Frame Handler Mode Control Register (Offset = Eh) [Reset = 00h]

Frame Handler Mode Control is shown in [Table 7-53](#).

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Logic Control

Table 7-53. Frame Handler Mode Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FH_RST	R/W	0h	Frame handler reset Reset frame handler logic and registers 0h = no reset 1h = reset frame handler
6	SKIP_CT	R/W	0h	Ignore cycle timer reset during frame handler reset Ignore cycle timer reset while resetting the frame handler logic 0h = reset cycle timer during frame handler reset 1h = no reset
5	CKSM	R/W	0h	Enable auto checksum Enables automatic CRC computation for each transmitted message 0h = disable automatic checksum 1h = enable automatic checksum
4	TKEEP	R/W	0h	TX buffer keep Enables transmit buffer retention and retransmit functionality 0h = disable TX keep and retransmit 1h = enable TX keep and retransmit
3	INT_SYNC_EN	R/W	0h	Internal Frame Handler Sync Enable 0h = Internal Synchronization Disabled 1h = Internal Synchronization Enabled
2	EXT_SYNC_EN	R/W	0h	External Frame Handler Sync Enable 0h = External Synchronization Enabled 1h = External Synchronization Disabled
1	SYNC_SRC_SEL	R/W	0h	External Sync Source Select 0h = TXD[0] is used as external sync 1h = TXD[1] is used as external sync
0	SYNC_SRC_EDGE	R/W	0h	External Sync Source Edge Select 0h = falling edge of source signal starts sync 1h = rising edge of source signal starts sync

7.3.12.2.16 FH + EFH Mode RX Buffer Trigger Level Register (Offset = Fh) [Reset = 00h]

FH + EFH Mode RX Buffer Trigger Level is shown in [Table 7-54](#).

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Logic Control

Table 7-54. FH + EFH Mode RX Buffer Trigger Level Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RX_BTLVL	R/W	0h	RX Buffer Trigger Level FH: At what RX buffer level the BLVLRT interrupt request will get logged (Rose Above Trigger) EFH: At what RX buffer level the RX_BLVL_RATL interrupt request will get logged

7.3.12.2.17 FH + EFH Mode TX Buffer Trigger Level Register (Offset = 10h) [Reset = 00h]

FH + EFH Mode TX Buffer Trigger Level is shown in [Table 7-55](#).

Return to the [Summary Table](#).

Logic Control

Table 7-55. FH + EFH Mode TX Buffer Trigger Level Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_BTLVL	R/W	0h	TX Buffer Trigger Level FH: At what TX buffer level the BLVLRT interrupt request will get logged (Fell Below Trigger) EFH: At what TX buffer level the TX_BLVF_FBTB interrupt request will get logged

7.3.12.2.18 On Demand data Length Register (Offset = 11h) [Reset = 00h]

On Demand data Length is shown in [Table 7-56](#).

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Logic Control

Table 7-56. On Demand data Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	LEN	R/W	0h	On-demand Data length

7.3.12.2.19 Master Process Data Length Register (Offset = 12h) [Reset = 00h]

Master Process Data Length is shown in [Table 7-57](#).

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Logic Control

Table 7-57. Master Process Data Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	LEN	R/W	0h	Master Process Data Length

7.3.12.2.20 Device Process Data Length Register (Offset = 13h) [Reset = 00h]

Device Process Data Length is shown in [Table 7-58](#).

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Logic Control

Table 7-58. Device Process Data Length Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	LEN	R/W	0h	Device Process Data Length

7.3.12.2.21 FH Mode Cycle Timer Control Register (Offset = 14h) [Reset = 00h]

FH Mode Cycle Timer Control is shown in [Table 7-59](#).

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Logic Control

Table 7-59. FH Mode Cycle Timer Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BASE	R/W	0h	Cycle Timer Base 0h = 100us + no offset 1h = 400us + 6.4ms offset 2h = 1.6ms + 32ms 3h = reserved
5-0	MULT	R/W	0h	Cycle Timer Multiplier Cycle Timer Multiplier 0..63 (Valid Values) tCYC = offset + (BASE * MULT)

7.3.12.2.22 FH Mode Data Register (Offset = 15h) [Reset = 00h]

FH Mode Data is shown in [Table 7-60](#).

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Logic Control

Table 7-60. FH Mode Data Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DATA	R/W	0h	Frame Handler Data Read and Write Register Frame Handler Data Read and Write Register

7.3.12.2.23 Channel Logic Status Register (Offset = 16h) [Reset = 00h]

Channel Logic Status is shown in [Table 7-61](#).

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Logic Status

Table 7-61. Channel Logic Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3	DI_RXD	R	0h	DI_RXD Instantaneous value of DI receive pin 0h = DI low 1h = DI high
2-0	CLSTAT	R	0h	Channel Logic Status Based on channel logic mode phy_mode : CLSTAT[2] - TXEN; CLSTAT[1] - TXD; CLSTAT[0] - RXD uart_mode : N/A fh_mode and extended fh_mode : CLSTAT - Frame Handler State 0h = IDLE 1h = TX 2h = RX 3h = RESERVED 4h = RESERVED 5h = RESERVED 6h = RESERVED 7h = RESERVED

7.3.12.2.24 Channel Phy Status Register (Offset = 17h) [Reset = 00h]

Channel Phy Status is shown in [Table 7-62](#).

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Physical Status

Table 7-62. Channel Phy Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OT_FAULT	R	0h	Over temperature fault Instantaneous value of over temperature fault 0h = no over temperature fault 1h = over temperature fault
6	OT_WARN	R	0h	Over temperature warning Instantaneous value of over temperature warning 0h = no over temperature warning 1h = over temperature warning
5	EXT_CQ_OC	R	0h	External CQ overcurrent Instantaneous value of external CQ overcurrent 0h = no external CQ overcurrent 1h = external CQ overcurrent
4	CQ_OC	R	0h	CQ overcurrent Instantaneous value of CQ overcurrent 0h = no CQ overcurrent 1h = CQ overcurrent
3	LP_OC	R	0h	L+ overcurrent Instantaneous value of L+ overcurrent 0h = no L+ overcurrent 1h = L+ overcurrent
2	LP_UVLO	R	0h	L+ undervoltage lockout Instantaneous value of L+ undervoltage lockout 0h = no L+ undervoltage lockout 1h = L+ undervoltage lockout
1-0	RESERVED	R	0h	Reserved

7.3.12.2.25 Channel Logic Interrupt REQuest Register (Offset = 18h) [Reset = 00h]

Channel Logic Interrupt REQuest is shown in [Table 7-63](#).

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Logic Interrupt

Table 7-63. Channel Logic Interrupt REQuest Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLIREQ7	RC	0h	Channel Logic Interrupt Request 7 Value dependent on channel mode: iolink_phy_mode : ECS_ERR - Establish Communication Sequence Error uart_mode : TX_ERR - Transmission Error fh_mode : TRX_ERR - Transmit (Transmission) or Receive Error (Parity, Frame) ext_fh_mode: TX_ERR - Transmission Error 0h = No interrupt event registered 1h = Interrupt event registered
6	CLIREQ6	RC	0h	Channel Logic Interrupt Request 6 Value dependent on channel mode: iolink_phy_mode : WPG_ERR - Wake Pulse Generation Error uart_mode : RX_ERR - Reception Error (Parity or Frame) fh_mode : T1_TA_T2_TO_ERR - t1, tA or t2 Timeout Error ext_fh_mode: RX_ERR - Reception Error (Parity or Frame Error) 0h = No interrupt event registered 1h = Interrupt event registered
5	CLIREQ5	RC	0h	Channel Logic Interrupt Request 5 Value dependent on channel mode: iolink_phy_mode : RPD_ERR - Ready Pulse Detection Error uart_mode : OR_ERR - Over Run Error fh_mode : CKSM_ERR - Check Sum Error (Transmit or Receive Checksum) ext_fh_mode: N/A 0h = No interrupt event registered 1h = Interrupt event registered
4	CLIREQ4	RC	0h	Channel Logic Interrupt Request 4 Value dependent on channel mode: iolink_phy_mode : ASEQ_OK - Automated Start Sequence Completed without Errors uart_mode : N/A fh_mode : TBUF_EMPTY_AT_CT_EXP - Tx Buffer was Empty at Cycle Timer Expiry ext_fh_mode: N/A 0h = No interrupt event registered 1h = Interrupt event registered
3	CLIREQ3	RC	0h	Channel Logic Interrupt Request 3 Value dependent on channel mode: iolink_phy_mode : N/A uart_mode : N/A fh_mode : SOT - Start Of iolink message Transmission ext_fh_mode: RX_BFULL - Rx Buffer Full 0h = No interrupt event registered 1h = Interrupt event registered
2	CLIREQ2	RC	0h	Channel Logic Interrupt Request 2 Value dependent on channel mode: iolink_phy_mode : N/A uart_mode : N/A fh_mode : SOR - Start of iolink message Reception ext_fh_mode: TX_BEMPTY - Tx Buffer Empty 0h = No interrupt event registered 1h = Interrupt event registered
1	CLIREQ1	RC	0h	Channel Logic Interrupt Request 1 Value dependent on channel mode: iolink_phy_mode : CQ_R - CQ Rose uart_mode : TX_RDY - Transmitter Ready fh_mode : BLVL_RT - Buffer Level Reached Trigger level (Both TX and RX) ext_fh_mode: RX_BLVL_RATL - Rx Buffer Level Rose Above Trigger Level 0h = No interrupt event registered 1h = Interrupt event registered

Table 7-63. Channel Logic Interrupt REQuest Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CLIREQ0	RC	0h	Channel Logic Interrupt Request 0 Value dependent on channel mode: iolink_phy_mode : CQ_F - CQ Fell uart_mode : RX_RDY - Receiver Ready (Received byte available for read) fh_mode : MSG_RDY - Message Ready (IO-Link Message received without errors) ext_fh_mode: TX_BLVL_FBTl - Tx Buffer Level Fell Below Trigger Level 0h = No interrupt event registered 1h = Interrupt event registered

7.3.12.2.26 Channel Physical Interrupt REQuest Register (Offset = 19h) [Reset = 00h]

Channel Physical Interrupt REQuest is shown in [Table 7-64](#).

Return to the [Summary Table](#).

Physical Interrupt

Table 7-64. Channel Physical Interrupt REQuest Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OT_FAULT	RC	0h	Over temperature fault Latched (read-to-clear) value of over temperature fault 0h = No interrupt event registered 1h = Interrupt event registered
6	OT_WARN	RC	0h	Over temperature warning Latched (read-to-clear) value of over temperature warning 0h = No interrupt event registered 1h = Interrupt event registered
5	EXT_CQ_OC	RC	0h	External CQ overcurrent Latched (read-to-clear) value of external CQ overcurrent 0h = No interrupt event registered 1h = Interrupt event registered
4	CQ_OC	RC	0h	CQ overcurrent Latched (read-to-clear) value of CQ overcurrent 0h = No interrupt event registered 1h = Interrupt event registered
3	LP_OC	RC	0h	L+ overcurrent Latched (read-to-clear) value of L+ overcurrent 0h = No interrupt event registered 1h = Interrupt event registered
2	LP_UVLO	RC	0h	L+ undervoltage lockout Latched (read-to-clear) value of L+ undervoltage lockout 0h = No interrupt event registered 1h = Interrupt event registered
1	DI_R	RC	0h	DI rose Latched (read-to-clear) DI rising edge detected 0h = No interrupt event registered 1h = Interrupt event registered
0	DI_F	RC	0h	DI fell Latched (read-to-clear) DI falling edge detected 0h = No interrupt event registered 1h = Interrupt event registered

7.3.12.2.27 LED Config 1 Register (Offset = 1Ah) [Reset = 00h]

LED Config 1 is shown in [Table 7-65](#).

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LED Config / Control

Table 7-65. LED Config 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BLINK	R/W	0h	LED Blinking Configuration Sets the blinking pattern for LED1. 0h = disable blinking 1h = 100 ms high - 100 ms low (1:1) blink 2h = 100 ms high - 300 ms low (1:3) blink 3h = 100 ms high - 1100 ms low (1:11) blink
5-4	IDRV	R/W	0h	LED Driver Current Config Sets the current source for LED1. 0h = 2 mA 1h = 8 mA 2h = 14 mA 3h = 20 mA
3-0	PWM	R/W	0h	PWM duty cycle configuration Sets the PWM duty cycle for LED1. 0h = 0 % (LED off) 1h = 1.4 % 2h = 1.8 % 3h = 2.5 % 4h = 3.4 % 5h = 4.6 % 6h = 6.3 % 7h = 8.6 % 8h = 11 % 9h = 16 % Ah = 22 % Bh = 29 % Ch = 40 % Dh = 54 % Eh = 74 % Fh = 100 % (LED on)

7.3.12.2.28 LED Config 2 Register (Offset = 1Bh) [Reset = 00h]

LED Config 2 is shown in [Table 7-66](#).

Return to the [Summary Table](#).

LED Config / Control

Table 7-66. LED Config 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BLINK	R/W	0h	LED Blinking Configuration Sets the blinking pattern for LED2. 0h = disable blinking 1h = 100 ms high - 100 ms low (1:1) blink 2h = 100 ms high - 300 ms low (1:3) blink 3h = 100 ms high - 1100 ms low (1:11) blink
5-4	IDRV	R/W	0h	LED Driver Current Config Sets the current source for LED2. 0h = 2 mA 1h = 8 mA 2h = 14 mA 3h = 20 mA
3-0	PWM	R/W	0h	PWM duty cycle configuration Sets the PWM duty cycle for LED2. 0h = 0 % (LED off) 1h = 1.4 % 2h = 1.8 % 3h = 2.5 % 4h = 3.4 % 5h = 4.6 % 6h = 6.3 % 7h = 8.6 % 8h = 11 % 9h = 16 % Ah = 22 % Bh = 29 % Ch = 40 % Dh = 54 % Eh = 74 % Fh = 100 % (LED on)

7.3.12.2.29 LED Config 3 Register (Offset = 1Ch) [Reset = 00h]

LED Config 3 is shown in [Table 7-67](#).

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LED Config / Control

Table 7-67. LED Config 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BLINK	R/W	0h	LED Blinking Configuration Sets the blinking pattern for LED3. 0h = disable blinking 1h = 100 ms high - 100 ms low (1:1) blink 2h = 100 ms high - 300 ms low (1:3) blink 3h = 100 ms high - 1100 ms low (1:11) blink
5-4	IDRV	R/W	0h	LED Driver Current Config Sets the current source for LED3. 0h = 2 mA 1h = 8 mA 2h = 14 mA 3h = 20 mA
3-0	PWM	R/W	0h	PWM duty cycle configuration Sets the PWM duty cycle for LED3. 0h = 0 % (LED off) 1h = 1.4 % 2h = 1.8 % 3h = 2.5 % 4h = 3.4 % 5h = 4.6 % 6h = 6.3 % 7h = 8.6 % 8h = 11 % 9h = 16 % Ah = 22 % Bh = 29 % Ch = 40 % Dh = 54 % Eh = 74 % Fh = 100 % (LED on)

7.3.12.2.30 LED Config 4 Register (Offset = 1Dh) [Reset = 00h]

LED Config 4 is shown in [Table 7-68](#).

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LED Config / Control

Table 7-68. LED Config 4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BLINK	R/W	0h	LED Blinking Configuration Sets the blinking pattern for LED4. 0h = disable blinking 1h = 100 ms high - 100 ms low (1:1) blink 2h = 100 ms high - 300 ms low (1:3) blink 3h = 100 ms high - 1100 ms low (1:11) blink
5-4	IDRV	R/W	0h	LED Driver Current Config Sets the current source for LED4. 0h = 2 mA 1h = 8 mA 2h = 14 mA 3h = 20 mA
3-0	PWM	R/W	0h	PWM duty cycle configuration Sets the PWM duty cycle for LED4. 0h = 0 % (LED off) 1h = 1.4 % 2h = 1.8 % 3h = 2.5 % 4h = 3.4 % 5h = 4.6 % 6h = 6.3 % 7h = 8.6 % 8h = 11 % 9h = 16 % Ah = 22 % Bh = 29 % Ch = 40 % Dh = 54 % Eh = 74 % Fh = 100 % (LED on)

7.3.12.2.31 LED Config 5 Register (Offset = 1Eh) [Reset = 00h]

LED Config 5 is shown in [Table 7-69](#).

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LED Config / Control

Table 7-69. LED Config 5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BLINK	R/W	0h	LED Blinking Configuration Sets the blinking pattern for LED5. 0h = disable blinking 1h = 100 ms high - 100 ms low (1:1) blink 2h = 100 ms high - 300 ms low (1:3) blink 3h = 100 ms high - 1100 ms low (1:11) blink
5-4	IDRV	R/W	0h	LED Driver Current Config Sets the current source for LED5. 0h = 2 mA 1h = 8 mA 2h = 14 mA 3h = 20 mA
3-0	PWM	R/W	0h	PWM duty cycle configuration Sets the PWM duty cycle for LED5. 0h = 0 % (LED off) 1h = 1.4 % 2h = 1.8 % 3h = 2.5 % 4h = 3.4 % 5h = 4.6 % 6h = 6.3 % 7h = 8.6 % 8h = 11 % 9h = 16 % Ah = 22 % Bh = 29 % Ch = 40 % Dh = 54 % Eh = 74 % Fh = 100 % (LED on)

7.3.12.2.32 LED Config 6 Register (Offset = 1Fh) [Reset = 00h]

LED Config 6 is shown in [Table 7-70](#).

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LED Config / Control

Table 7-70. LED Config 6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	BLINK	R/W	0h	LED Blinking Configuration Sets the blinking pattern for LED6. 0h = disable blinking 1h = 100 ms high - 100 ms low (1:1) blink 2h = 100 ms high - 300 ms low (1:3) blink 3h = 100 ms high - 1100 ms low (1:11) blink
5-4	IDRV	R/W	0h	LED Driver Current Config Sets the current source for LED6. 0h = 2 mA 1h = 8 mA 2h = 14 mA 3h = 20 mA
3-0	PWM	R/W	0h	PWM duty cycle configuration Sets the PWM duty cycle for LED6. 0h = 0 % (LED off) 1h = 1.4 % 2h = 1.8 % 3h = 2.5 % 4h = 3.4 % 5h = 4.6 % 6h = 6.3 % 7h = 8.6 % 8h = 11 % 9h = 16 % Ah = 22 % Bh = 29 % Ch = 40 % Dh = 54 % Eh = 74 % Fh = 100 % (LED on)

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

When the TIOM2212 is connected to one or more IO-Link devices through a three-wire interface (Figure 8-1), the application can initiate communication and exchange data with a remote node with the TIOM2212 IO-Link transceiver acting as a complete physical layer for the communication.

8.2 Typical Application

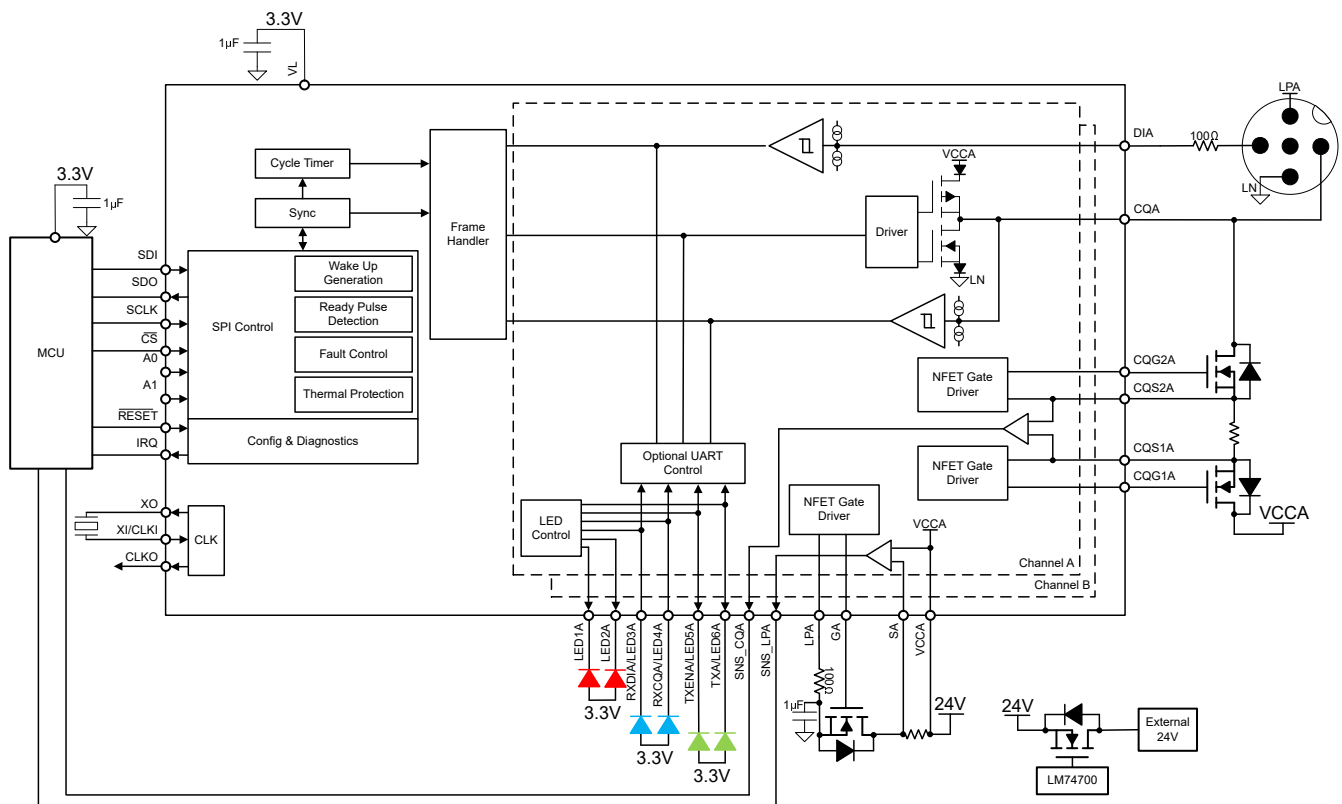


Figure 8-1. Typical Application Schematic

8.3 Power Supply Recommendations

The TIOM2212 is designed to operate from a 24V nominal supply at L+, which can vary by +12V and -17V from the nominal value to remain within the devices recommended supply voltage range of 7V to 36V. This supply should be buffered with at least a 100nF/100V capacitor.

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

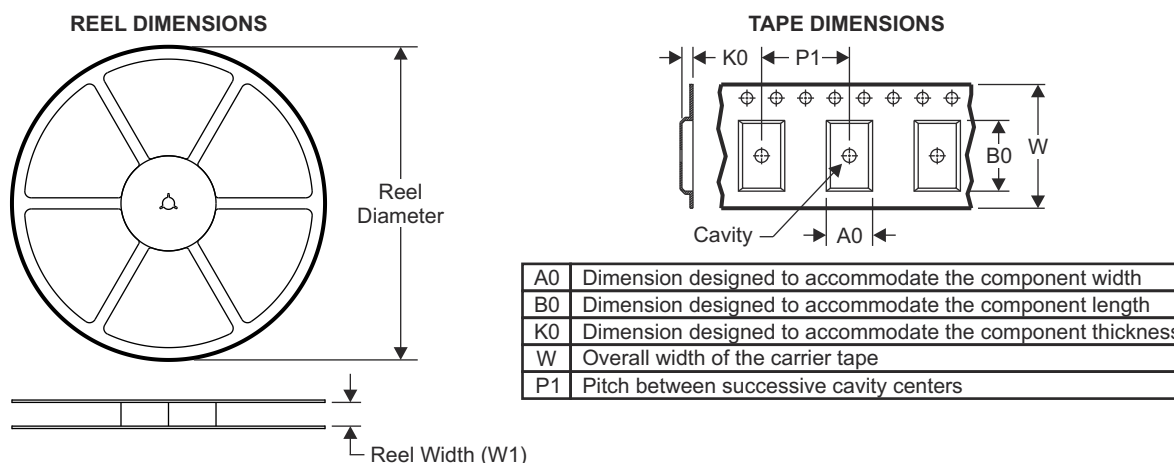
10 Revision History

DATE	REVISION	NOTES
October 2026	*	Initial release

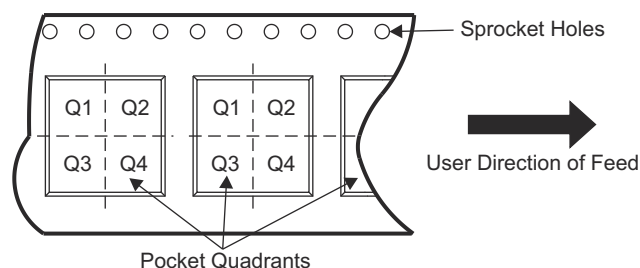
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

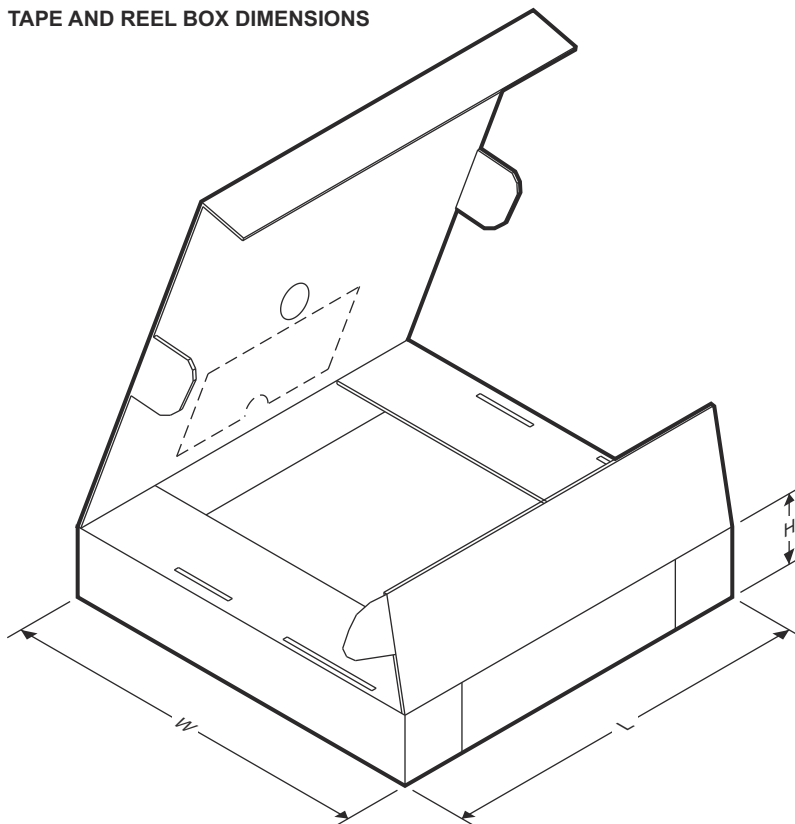


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

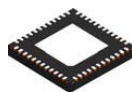


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TIOM2212RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TIOM2212RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TIOM2212RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TIOM2212RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0



PLASTIC QUAD FLATPACK - NO LEAD

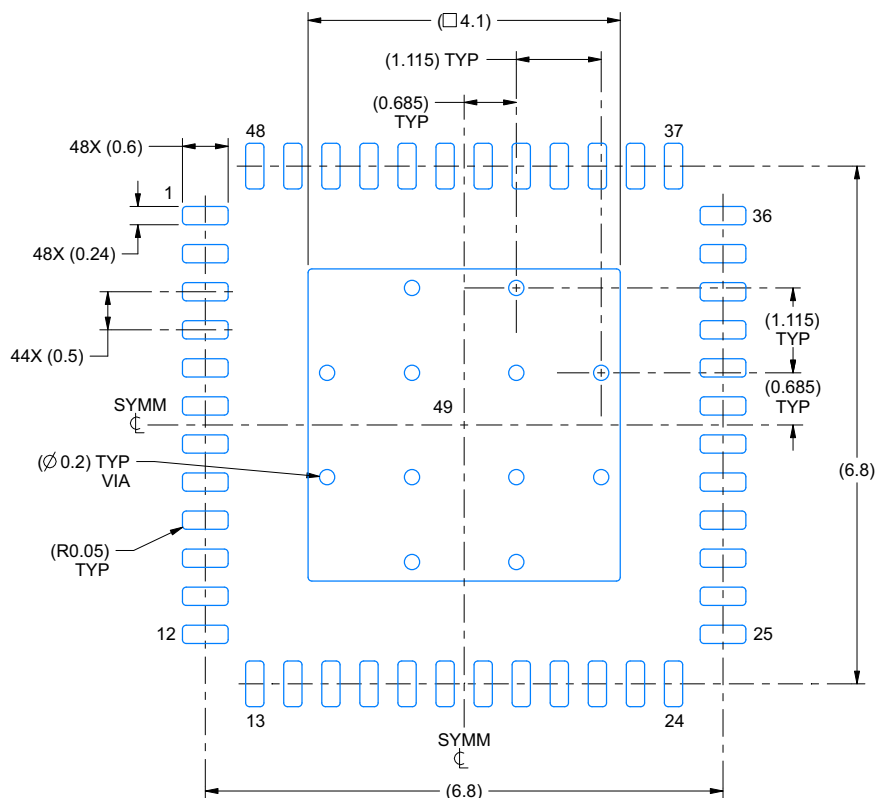
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

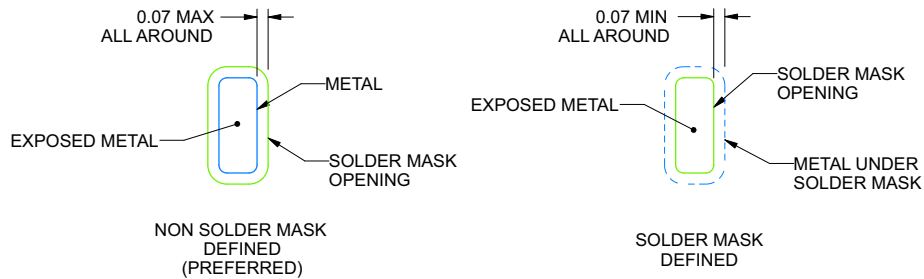
RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4218795/B 02/2017

NOTES: (continued)

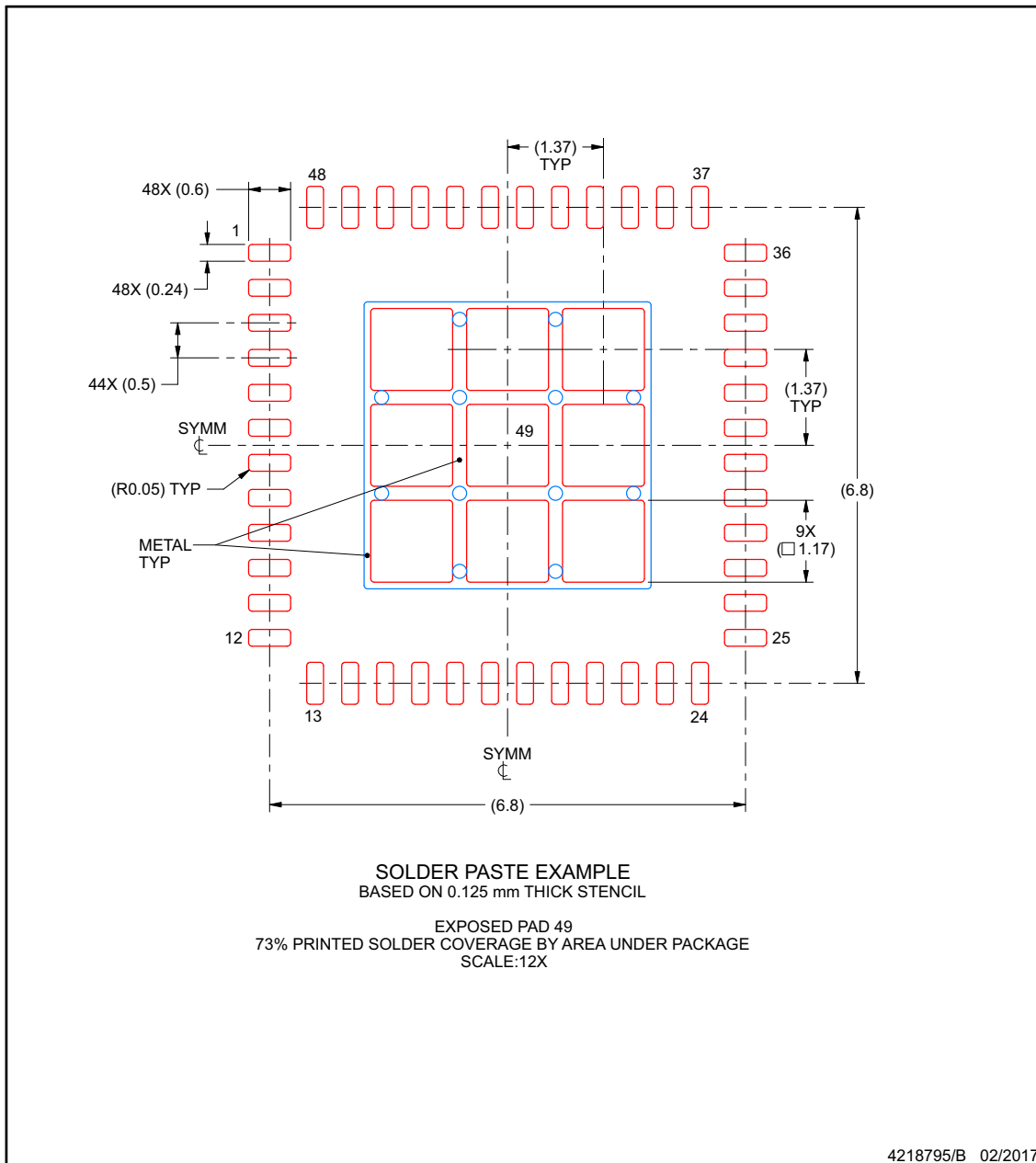
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTIOM2212RGZR	Active	Preproduction	VQFN (RGZ) 48	4000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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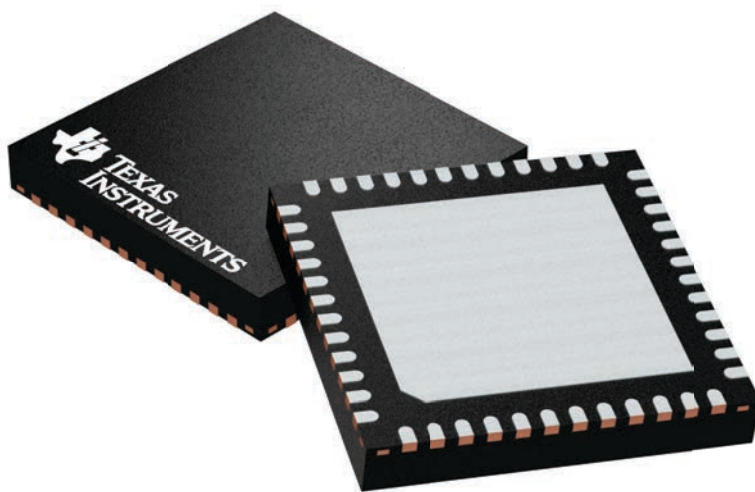
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

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