TL03x, TL03xA Enhanced-FET Low-Power Low-Offset Operational Amplifiers

1 Features

- Direct upgrades for the TL06x low-power amplifiers
- Low power consumption
- On-chip offset-voltage trimming for improved DC performance (1.5mV, TL031ID)
- Higher slew rate and bandwidth without increased power consumption
- Available in TSSOP for small form-factor designs

2 Applications

- Solar energy: string and central inverter
- Motor drives: ac and servo drive control and power-stage modules
- Single-phase online UPS

3 Description

The TL03x series of FET-input operational amplifiers offer improved DC and AC characteristics over the TL06x family of low-power operational amplifiers. The Texas Instruments improved FET process and optimized designs also yield improved bandwidths and slew rates without increased power consumption.

FET operational amplifiers offer the inherently higher input impedance of the FET-input transistors. This higher input impedance makes the TL03x amplifiers better suited for interfacing with high-impedance sensors or very low-level AC signals.

The TL03x family has been optimized for micropower operation, while improving on the performance of the TL06x series. Designers requiring significantly faster AC response must consider the TLE206x family of low-power FET operational amplifiers.

The FET operational amplifiers are designed for use with dual power supplies, therefore take care to observe common-mode input-voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required, and loads must be terminated to a virtual-ground node at mid supply. The TI TLE2426 integrated virtual-ground generator is useful when operating amplifiers from single supplies.

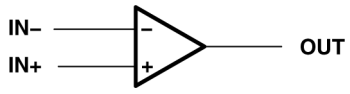
The TL03x devices are fully specified at ±15V and ±5V. For operation in low-voltage and/or single-supply systems, the TI LinCMOS families of operational amplifiers (TLC prefix) are recommended.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to 85°C.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TL031	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
TL031A	N (PDIP, 14)	19.3mm × 9.4mm
	D (SOIC, 8)	8.65mm × 6mm
TL032	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
	PS (SOP, 8)	6.2mm × 7.8mm
TL032A	P (PDIP, 8)	9.81mm × 9.43mm
	D (SOIC, 8)	4.9mm × 6mm
TL034	N (PDIP, 14)	19.3mm × 9.4mm
	D (SOIC, 14)	8.65mm × 6mm
	NS (SOP, 14)	10.2mm × 7.8mm
	PW (TSSOP, 14)	5mm × 6.4mm
TL034A	N (PDIP, 14)	19.3mm × 9.4mm
	D (SOIC, 14)	8.65mm × 6mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol (Each Amplifier)

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4 Pin Configuration and Functions

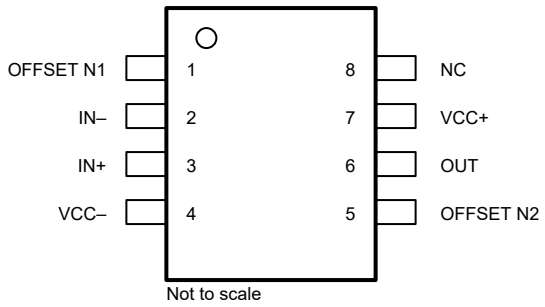


Figure 4-1. TL031ID, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions of TL031ID

PIN		TYPE	DESCRIPTION
NAME	NO.		
OFFSET N1	1	—	Input offset adjustment
IN–	2	Input	Inverting Input
IN+	3	Input	Non Inverting Input
VCC–	4	—	Power supply negative
OFFSET N2	5	—	Input offset adjustment
OUT	6	Output	Output
VCC+	7	—	Power supply positive
NC	8	—	Do not connect

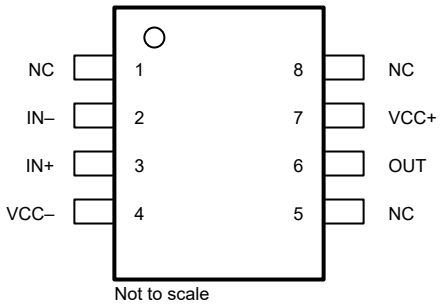


Figure 4-2. TL031x, TL031Ax D or P Package, 8-Pin SOIC or PDIP (Top View)

Table 4-2. Pin Functions of TL031x, TL031Ax

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1	—	Do not connect
IN–	2	Input	Inverting Input
IN+	3	Input	Non Inverting Input
VCC–	4	—	Power supply negative
NC	5	—	Do not connect
OUT	6	Output	Output
VCC+	7	—	Power supply positive
NC	8	—	Do not connect

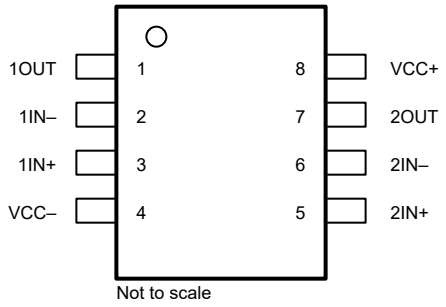


Figure 4-3. TL032x, TL032Ax D, or P Package, 8-Pin SOIC, or PDIP (Top View)

Table 4-3. Pin Functions of TL032x, TL032Ax

PIN		TYPE	DESCRIPTION
NAME	NO.		
1OUT	1	Output	Output, channel 1
1IN–	2	Input	Inverting Input, channel 1
1IN+	3	Input	Non Inverting Input, channel 1
VCC–	4	—	Power supply negative
2IN+	5	Input	Non Inverting Input, channel 2
2IN–	6	Input	Inverting Input, channel 2
2OUT	7	Output	Output, channel 2
VCC+	8	—	Power supply positive

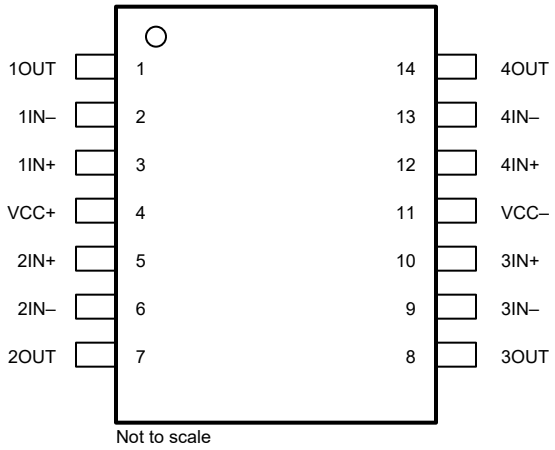


Figure 4-4. TL034x, TL034Ax D, N, or PW Package, 14-Pin SOIC, PDIP, or TSSOP (Top View)

Table 4-4. Pin Functions of TL034x, TL034Ax

PIN		TYPE	DESCRIPTION
NAME	NO.		
1OUT	1	Output	Output, channel 1
1IN–	2	Input	Inverting Input, channel 1
1IN+	3	Input	Non Inverting Input, channel 1
VCC+	4	—	Power supply positive
2IN+	5	Input	Non Inverting Input, channel 2
2IN–	6	Input	Inverting Input, channel 2
2OUT	7	Output	Output, channel 2
3OUT	8	Output	Output, channel 3
3IN–	9	Input	Inverting Input, channel 3
3IN+	10	Input	Non Inverting Input, channel 3
VCC–	11	—	Power supply negative
4IN+	12	Input	Non Inverting Input, channel 4
4IN–	13	Input	Inverting Input, channel 4
4OUT	14	Output	Output, channel 4

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage(2)			18	V
V_{CC-}	Supply voltage			–18	V
	Differential input voltage(3)		–30	30	V
V_I	Input voltage range(2) (4)	Any input	–15	15	V
I_I	Input current	Each input	–1	1	mA
I_O	Output current	Each output	–40	40	mA
	Duration of short-circuit current at (or below) 25°C(5)			Unlimited	
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds:	D, N, P, or PW package		260	℃
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+ with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whichever is less.
(5) The output can be shorted to either supply. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction.

5.2 Thermal Information

THERMAL METRIC(1)		TL031x TL031Ax TL032x TL032Ax		TL034x TL034Ax			UNIT
		D	P	D	N	PW	
		8	8	14	14	14	
θ_{JA}	Junction-to-ambient thermal resistance	97	85	86	80	113	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application note.

5.3 Recommended Operating Conditions

			C SUFFIX		I SUFFIX		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC±}$	Supply voltage		±5	±15	±5	±15	V
V_{IC}	Common-mode input voltage	$V_{CC±}$ = ±5V	−1.5	4	−1.5	4	V
		$V_{CC±}$ = ±15V	−11.5	14	−11.5	14	
T_A	Operating free-air temperature		0	70	−40	85	°C

5.4 TL031C and TL031AC Electrical Characteristics

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TL031C, TL031AC						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ =±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL031C	25°C		0.54	3.5		0.5	1.5	mV
				Full range[1]			4.5			2.5	
			TL031AC	25°C		0.41	2.8		0.34	1.5	
				Full range[1]			3.8			1.8	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, V_{IC} =0, R_S = 50Ω	TL031C	25°C to 70°C		7.1			5.9		µV/°C
			TL031AC	25°C to 70°C		7.1			5.9	25	
	Input offset voltage long-term drift[2]	V_O = 0, V_{IC} =0, R_S = 50Ω		25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		25°C		5	100		5	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		25°C		10	200		10	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.2		−11.5 to 14	−13.4 to 15.2		V
				Full range[1]	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.995		13	14.955		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	−3	−4.995		−12.5	−14.955		V
A_{VD}	Large-signal differential voltage amplification[3]	R_L = 10kΩ		25°C	72	130		72	130		dB
				0°C		125			125		
				70°C		125			125		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		4			4		pF
CMRR	Common-mode rejection ratio	(V_{CC-}) + 3.5V < V_{IC} < (V_{CC+}) − 2V, V_O = 0, R_S = 50Ω		25°C	70	90		75	94		dB
				0°C	70	90		75	94		
				70°C	70	90		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0, R_S = 50Ω		25°C	75	140		75	140		dB
				0°C	75	140		75	140		
				70°C	75	140		75	140		
I_{CC}	Supply current per amplifier	V_O = 0, No load		25°C		130	250		130	280	µA

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96eV.
(3) At $V_{CC\pm}$ = ±5V, V_O = ±2.3V; at $V_{CC\pm}$ = ±15V, V_O = ±10V

5.5 TL031C and TL031AC Operating Characteristics

at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL031C, TL031AC						UNIT
						$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ = ±15V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		2			2.9		V/μs
					0°C		1.8			2.6		
					70°C		2.2			3.2		
SR−	Negative slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		3.9			5.1		V/μs
					0°C		3.7			5		
					70°C		4			5		
V_n	Equivalent input noise voltage	TL031C	R_S = 20Ω	f = 10Hz	25°C		115			115		nV/√Hz
				f = 1kHz			30			30		
		TL031AC		f = 10Hz	25°C		115			115		
				f = 1kHz			30			30		
I_n	Equivalent input noise current		f = 1kHz		25°C		2			2		fA/√Hz
B_1	Unity-gain bandwidth		V_I = 10mV R_L = 10kΩ, C_L = 25pF		25°C		1.1			1.1		MHz
ϕ_m	Phase margin at unity gain		V_I = 10mV R_L = 10kΩ, C_L = 25pF		25°C		60°			60°		

(1) For $V_{CC\pm}$ = ±5V, $V_{I(PP)}$ = ±1V; for $V_{CC\pm}$ = ±15V, $V_{I(PP)}$ = ±5V

5.6 TL031I and TL031AI Electrical Characteristics

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TL031I, TL031AI						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$=±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL031I	25°C		0.54	3.5		0.5	1.5	mV
				Full range[1]			5.3			3.3	
			TL031AI	25°C		0.41	2.8		0.34	1.5	
				Full range[1]			4.6			2.6	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL031I	25°C to 85°C		6.5			6.2		µV/°C
			TL031AI	25°C to 85°C		6.5			6.2	25	
	Input offset voltage long-term drift[2]	V_O = 0, V_{IC} = 0, R_S = 50Ω		25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		25°C		5	100		5	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		25°C		10	200		10	200	pA
				85°C		0.2	0.9		0.2	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.2		−11.5 to 14	−13.4 to 15.2		V
				Full range[1]	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.995		13	14.955		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	−3	−4.995		−12.5	−14.955		V
A_{VD}	Large-signal differential voltage amplification[3]	R_L = 10kΩ		25°C	72	130		72	130		dB
				−40°C		125			125		
				85°C		125			125		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		4			4		pF
CMRR	Common-mode rejection ratio	$(V_{CC-}) + 3.5V < V_{IC} < (V_{CC+}) - 2V$, V_O = 0, R_S = 50Ω		25°C	70	90		75	94		dB
				−40°C	70	90		75	94		
				85°C	70	90		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0, R_S = 50Ω		25°C	75	140		75	140		dB
				−40°C	75	140		75	140		
				85°C	75	140		75	140		
I_{CC}	Supply current per amplifier	V_O = 0, No load		25°C		130	250		130	280	µA

(1) Full range is −40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96eV.

(3) At $V_{CC\pm}$ = ±5V, V_O = ±2.3V; at $V_{CC\pm}$ = ±15 V, V_O = ±10V

5.7 TL031I and TL031AI Operating Characteristics

at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL031I, TL031AI						UNIT
						$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ = ±15 V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain (1)		R_L = 10 kΩ, C_L = 100 pF		25°C		2			2.9		V/µs
					−40°C		1.6			2.1		
					85°C		2.3			3.3		
SR−	Negative slew rate at unity gain (1)		R_L = 10 kΩ, C_L = 100 pF		25°C		3.9			5.1		V/µs
					−40°C		3.3			4.8		
					85°C		4.1			4.9		
V_n	Equivalent input noise voltage	TL031I	R_S = 20Ω	f = 10Hz	25°C		115			115		nV/√Hz
				f = 1kHz			30			30		
		TL031AI		f = 10Hz	25°C		115			115		
				f = 1kHz			30			30		
I_n	Equivalent input noise current		f = 1kHz		25°C		2			2		fA/√Hz
B_1	Unity-gain bandwidth		V_I = 10mV R_L = 10kΩ, C_L = 25pF		25°C		1.1			1.1		MHz
ϕ_m	Phase margin at unity gain		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		60°			60°		

(1) For $V_{CC\pm}$ = ±5V, $V_{I(PP)}$ = ±1V; for $V_{CC\pm}$ = ±15V, $V_{I(PP)}$ = ±5V

5.8 TL032C and TL032AC Electrical Characteristics

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TL032C, TL032AC						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$=±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL032C	25°C		0.69	3.5		0.57	1.5	mV
				Full range (1)			4.5			2.5	
			TL032AC	25°C		0.53	2.8		0.39	1.5	
				Full range (1)			3.8			1.8	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL032C	25°C to 70°C		11.5			10.8		µV/°C
			TL032AC	25°C to 70°C		11.5			10.8	25	
	Input offset voltage long-term drift (2)	V_O = 0, V_{IC} = 0, R_S = 50Ω		25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		25°C		5	100		5	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		25°C		10	200		10	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.2		−11.5 to 14	−13.4 to 15.2		V
				Full range (1)	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.995		13	14.955		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	−3	−4.995		−12.5	−14.955		V
A_{VD}	Large-signal differential voltage amplification (3)	R_L = 10kΩ		25°C	72	130		72	130		dB
				0°C		125			125		
				70°C		125			125		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		4			4		pF
CMRR	Common-mode rejection ratio	(V_{CC-}) + 3.5V < V_{IC} < (V_{CC+}) − 2V, V_O = 0, R_S = 50Ω		25°C	70	90		75	94		dB
				0°C	70	90		75	94		
				70°C	70	90		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5V to ±15V, V_O = 0, R_S = 50Ω		25°C	75	140		75	140		dB
				0°C	75	140		75	140		
				70°C	75	140		75	140		
I_{CC}	Supply current per amplifier	V_O = 0, No load		25°C		120	250		120	280	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100dB		25°C		120			120		dB

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96eV.
(3) At $V_{CC\pm}$ = ±5V, V_O = 2.3V; at $V_{CC\pm}$ = ±15V, V_O = ±10V

5.9 TL032C and TL032AC Operating Characteristics

at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL032C, TL032AC						UNIT
						$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ = ±15V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain (1)		R_L = 10 kΩ, C_L = 100pF		25°C		1.2			2.9		V/μs
					0°C		1.8			2.6		
					70°C		2.2			3.2		
SR−	Negative slew rate at unity gain (1)		R_L = 10 kΩ, C_L = 100pF		25°C		3.9			5.1		V/μs
					0°C		3.7			5		
					70°C		4			5		
V_n	Equivalent input noise voltage	TL032C	R_S = 20Ω	f = 10Hz	25°C		115			115		nV/√Hz
				f = 1kHz			30			30		
		TL032AC		f = 10Hz	25°C		115			115		
				f = 1kHz			30			30		
I_n	Equivalent input noise current		f = 1kHz		25°C		2			2		fA/√Hz
B_1	Unity-gain bandwidth		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		1.1			1.1		MHz
ϕ_m	Phase margin at unity gain		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		60°			60°		

(1) For $V_{CC\pm}$ = ±5V, $V_{I(PP)}$ = ±1V; for $V_{CC\pm}$ = ±15V, $V_{I(PP)}$ = ±5V

5.10 TL032I and TL032AI Electrical Characteristics

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TL032I, TL032AI						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$=±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL032I	25°C		0.69	3.5		0.57	1.5	mV
				Full range (1)			5.3			3.3	
			TL032AI	25°C		0.53	2.8		0.39	1.5	
				Full range (1)			4.6			2.6	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL032I	25°C to 85°C		11.4			10.8		µV/°C
			TL032AI	25°C to 85°C		11.4			10.8	25	
	Input offset voltage long-term drift(2)	V_O = 0, V_{IC} = 0, R_S = 50Ω		25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		25°C		5	100		5	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		25°C		10	200		10	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.2		−11.5 to 14	−13.4 to 15.2		V
				Full range (1)	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.995		13	14.955		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	−3	−4.995		−12.5	−14.955		V
A_{VD}	Large-signal differential voltage amplification (3)	R_L = 10kΩ		−40°C		125			125		dB
				85°C		125			125		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		4			4		pF
CMRR	Common-mode rejection ratio	(V_{CC-}) + 3.5V < V_{IC} < (V_{CC+}) − 2V, V_O = 0, R_S = 50Ω		25°C	70	90		75	94		dB
				−40°C	70	90		75	94		
				85°C	70	90		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±5V to ±15V, V_O = 0, R_S = 50Ω		25°C	75	140		75	140		dB
				−40°C	75	140		75	140		
				85°C	75	140		75	140		
I_{CC}	Supply current per amplifier	V_O = 0, No load		25°C		120	250		120	280	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100dB		25°C		120			120		dB

(1) Full range is −40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96eV.
(3) At $V_{CC\pm}$ = ±5V, V_O = 2.3V; at $V_{CC\pm}$ = ±15V, V_O = ±10V

5.11 TL032I and TL032AI Operating Characteristics

at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL032I, TL032AI						UNIT
						$V_{CC±}$ = ±5V			$V_{CC±}$=±15V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		2			2.9		V/µs
					−40°C		1.6			2.1		
					85°C		2.3			3.3		
SR−	Negative slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		3.9			5.1		V/µs
					−40°C		3.3			4.8		
					85°C		4.1			4.9		
V_n	Equivalent input noise voltage	TL032I	R_S = 20Ω	f = 10Hz	25°C		115			115		nV/√Hz
				f = 1kHz			30			30		
		TL032AI		f = 10Hz	25°C		115			115		
				f = 1kHz			30			30		
I_n	Equivalent input noise current		f = 1kHz		25°C		2			2		fA/√Hz
B_1	Unity-gain bandwidth		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		1.1			1.1		MHz
ϕ_m	Phase margin at unity gain		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		60°			60°		

(1) For $V_{CC±}$ = ±5V, $V_{I(PP)}$ = ±1V; for $V_{CC±}$ = ±15V, $V_{I(PP)}$ = ±5V

5.12 TL034C and TL034AC Electrical Characteristics

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TL034C, TL034AC						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$=±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL034C	25°C		0.91	6		0.79	4	mV
				Full range (1)			8.2			6.2	
			TL034AC	25°C		0.7	3.5		0.58	1.5	
				Full range (1)			5.7			3.7	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL034C	25°C to 70°C		11.6			12		µV/°C
			TL034AC	25°C to 70°C		11.6			12	25	
	Input offset voltage long-term drift (2)	V_O = 0, V_{IC} = 0, R_S = 50Ω		25°C		0.04			0.04		µV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		25°C		5	100		5	100	pA
				70°C		9	200		12	200	
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		25°C		10	200		10	200	pA
				70°C		50	400		80	400	
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.2		−11.5 to 14	−13.4 to 15.2		V
				Full range (1)	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.995		13	14.955		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	−3	−4.995		−12.5	−14.955		V
A_{VD}	Large-signal differential voltage amplification(3)	R_L = 10kΩ		25°C	72	130		72	130		dB
				0°C		125			125		
				70°C		125			125		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		4			4		pF
CMRR	Common-mode rejection ratio	$(V_{CC-}) + 3.5V < V_{IC} < (V_{CC+}) - 2V$, V_O = 0, R_S = 50Ω		25°C	70	90		75	94		dB
				0°C	70	90		75	94		
				70°C	70	90		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0, R_S = 50Ω		25°C	75	140		75	140		dB
				0°C	75	140		75	140		
				70°C	75	140		75	140		
I_{CC}	Supply current per amplifier	V_O = 0, No load		25°C		120	500		120	280	µA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD}=100		25°C		120			120		dB

(1) Full range is 0°C to 70°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.
(3) At $V_{CC\pm}$ = ±5V, V_O = ±2.3V; at $V_{CC\pm}$ = ±15V, V_O = ±10V

5.13 TL034C and TL034AC Operating Characteristics

at specified free-air temperature

PARAMETER			TEST CONDITIONS		T_A	TL034C, TL034AC						UNIT
						$V_{CC\pm}$ = ±5V			$V_{CC\pm}$ = ±15V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		2			2.9		V/μs
					0°C		1.8			2.6		
					70°C		2.2			3.2		
SR−	Negative slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		3.9			5.1		V/μs
					0°C		3.7			5		
					70°C		4			5		
V_n	Equivalent input noise voltage	TL034C	R_S = 20Ω	f = 10Hz	25°C		115			115		nV/√Hz
				f = 1kHz			30			30		
		TL034AC		f = 10Hz	25°C		115			115		
				f = 1kHz			30			30		
I_n	Equivalent input noise current		f = 1kHz		25°C		2			2		fA/√Hz
B_1	Unity-gain bandwidth		V_I = 10mVR_L = 10kΩ, C_L = 25pF		25°C		1.1			1.1		MHz
ϕ_m	Phase margin at unity gain		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		60°			60°		

(1) For $V_{CC\pm}$ = ±5V, $V_{I(PP)}$ = ±1V; for $V_{CC\pm}$ = ±15V, $V_{I(PP)}$ = ±5V

5.14 TL034I and TL034AI Electrical Characteristics

at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TL034I, TL034AI						UNIT
					$V_{CC\pm}$ = ±5V			$V_{CC\pm}$= ±15V			
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL034I	25°C		0.91	3.6		0.79	4	mV
				Full range (1)			9.3			7.3	
			TL034AI	25°C		0.7	3.5		0.58	1.5	
				Full range (1)			6.8			4.8	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	V_O = 0, V_{IC} = 0, R_S = 50Ω	TL034I	25°C to 85°C		11.5			11.6		μV/°C
			TL034AI	25°C to 85°C		11.5			11.6	25	
	Input offset voltage long-term drift (2)	V_O = 0, V_{IC} = 0, R_S = 50Ω		25°C		0.04			0.04		μV/mo
I_{IO}	Input offset current	V_O = 0, V_{IC} = 0		25°C		5	100		5	100	pA
				85°C		0.02	0.45		0.02	0.45	nA
I_{IB}	Input bias current	V_O = 0, V_{IC} = 0		25°C		10	200		10	200	pA
				85°C		0.2	0.9		0.3	0.9	nA
V_{ICR}	Common-mode input voltage range			25°C	−1.5 to 4	−3.4 to 5.2		−11.5 to 14	−13.4 to 15.2		V
				Full range (1)	−1.5 to 4			−11.5 to 14			
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10kΩ		25°C	3	4.995		13	14.955		V
V_{OM-}	Maximum negative peak output voltage swing	R_L = 10kΩ		25°C	−3	−4.995		−12.5	−14.955		V
A_{VD}	Large-signal differential voltage amplification (3)	R_L = 10kΩ		−40°C		125			125		dB
				85°C		125			125		
r_i	Input resistance			25°C		10^{12}			10^{12}		Ω
c_i	Input capacitance			25°C		4			4		pF
CMRR	Common-mode rejection ratio	(V_{CC-}) + 3.5V < V_{IC} < (V_{CC+}) − 2V, V_O = 0, R_S = 50Ω		25°C	70	90		75	94		dB
				−40°C	70	90		75	94		
				85°C	70	90		75	94		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_O = 0, R_S = 50Ω		25°C	75	140		75	140		dB
				−40°C	75	140		75	140		
				85°C	75	140		75	140		
I_{CC}	Supply current per amplifier	V_O = 0, No load		25°C		120	250		120	280	μA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} =100		25°C		120			120		dB

(1) Full range is −40°C to 85°C.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96eV.
(3) At $V_{CC\pm}$ = ±5V, V_O = ±2.3V; at $V_{CC\pm}$ = ±15V, V_O = ±10V

5.15 TL034I and TL034AI Operating Characteristics

PARAMETER			TEST CONDITIONS		T_A	TL034I, TL034AI						UNIT
						$V_{CC±}$ = ±5V			$V_{CC±}$ = ±15V			
						MIN	TYP	MAX	MIN	TYP	MAX	
SR+	Positive slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		2			2.9		V/µs
					−40°C		1.6			2.1		
					85°C		2.3			3.3		
SR−	Negative slew rate at unity gain (1)		R_L = 10kΩ, C_L = 100pF		25°C		3.9			5.1		V/µs
					−40°C		3.3			4.8		
					85°C		4.1			4.9		
V_n	Equivalent input noise voltage	TL034I	R_S = 20Ω	f = 10Hz	25°C		115			115		nV/√Hz
				f = 1kHz			30			30		
		TL034AI		f = 10Hz	25°C		115			115		
				f = 1kHz			30			30		
I_n	Equivalent input noise current		f = 1kHz		25°C		2			2		fA/√Hz
B_1	Unity-gain bandwidth		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		1.1			1.1		MHz
ϕ_m	Phase margin at unity gain		V_I = 10mV, R_L = 10kΩ, C_L = 25pF		25°C		60°			60°		

(1) For $V_{CC±}$ = ±5V, $V_{I(PP)}$ = ±1V; for $V_{CC±}$ = ±15V, $V_{I(PP)}$ = ±5V

5.16 Typical Characteristics

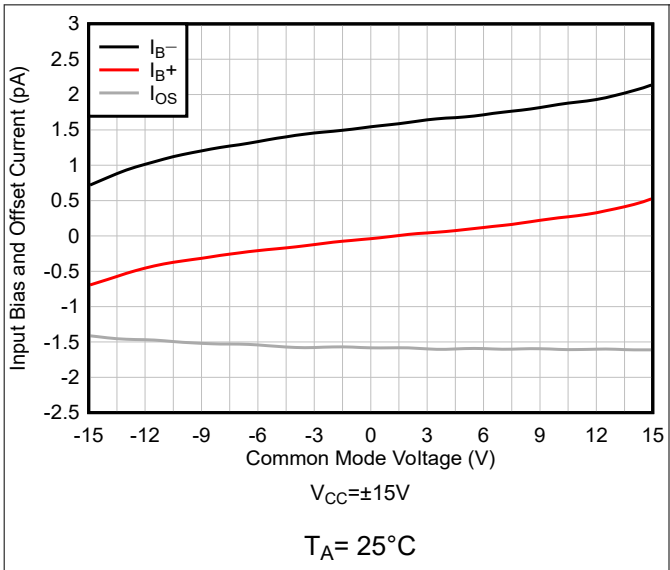


Figure 5-1. Input Bias Current vs Common-Mode Voltage

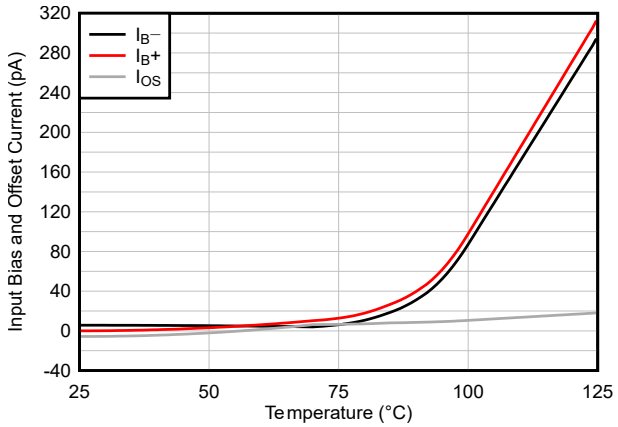


Figure 5-2. Input Bias Current vs Temperature

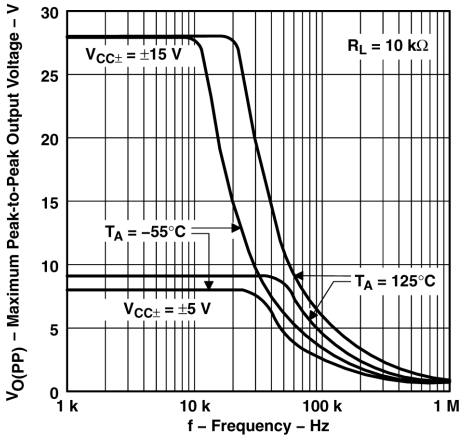


Figure 5-3. Maximum Peak-to-peak Output Voltage† vs Frequency

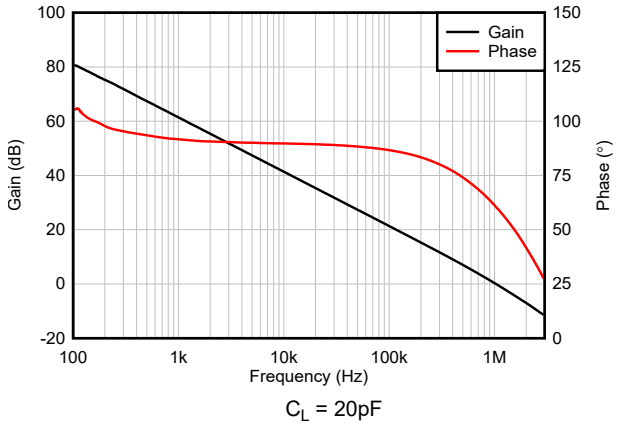


Figure 5-4. Open-Loop Gain and Phase vs Frequency

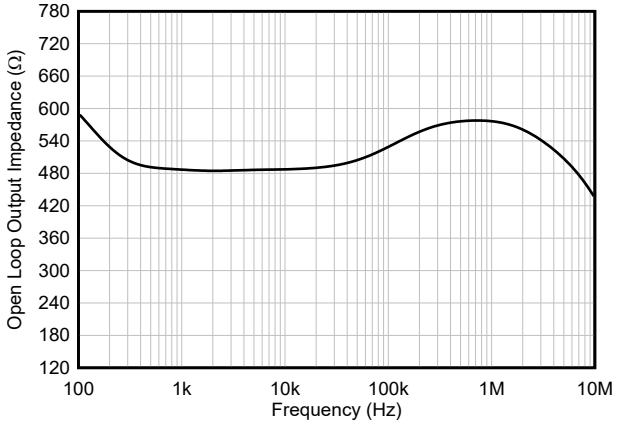


Figure 5-5. Open-Loop Output Impedance vs Frequency

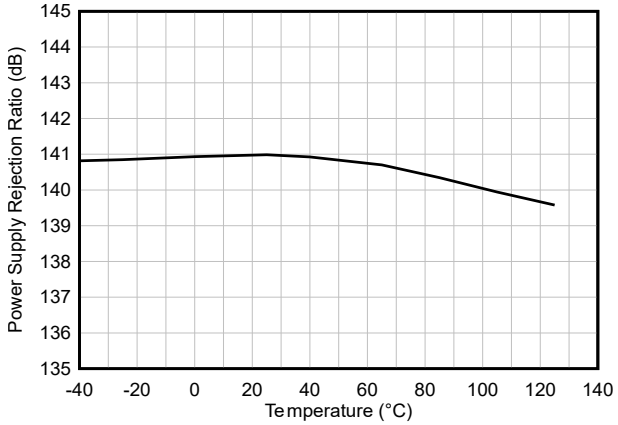


Figure 5-6. PSRR vs Temperature (dB)

5.16 Typical Characteristics (continued)

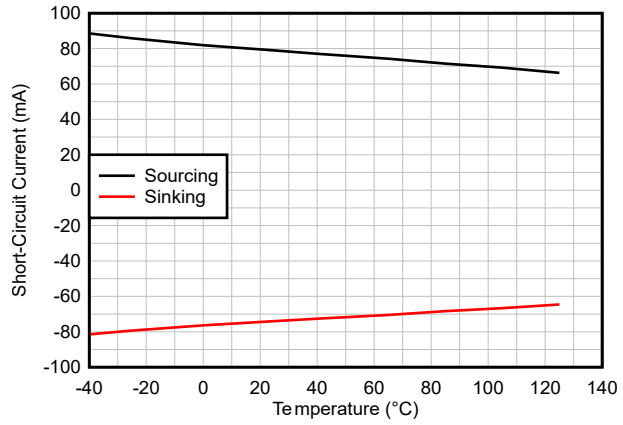


Figure 5-7. Short-Circuit Current vs Temperature

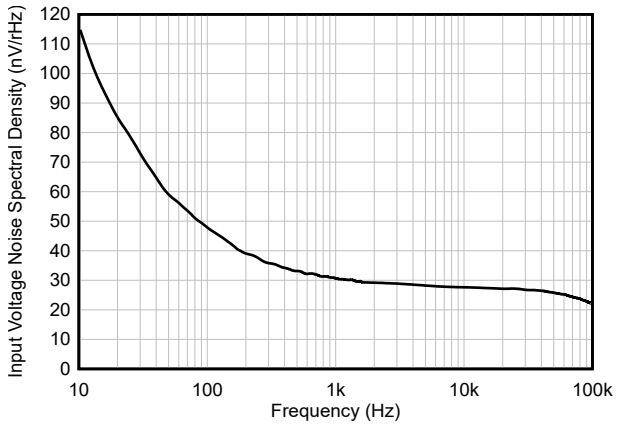


Figure 5-8. Input Voltage Noise Spectral Density vs Frequency

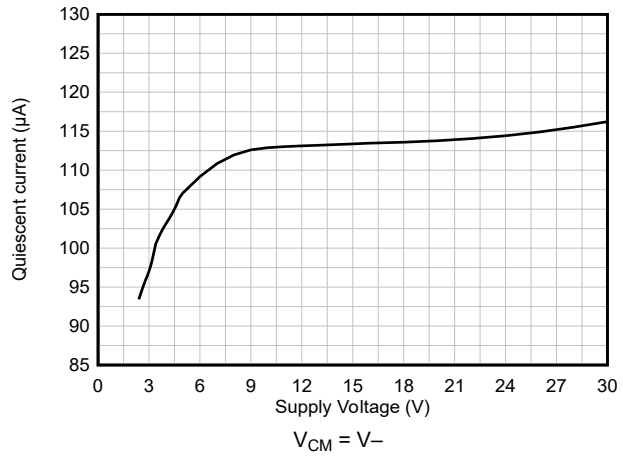


Figure 5-9. Quiescent Current vs Supply Voltage

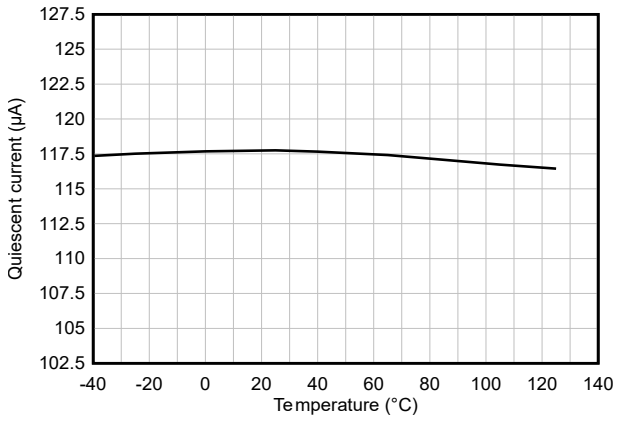


Figure 5-10. Quiescent Current vs Temperature

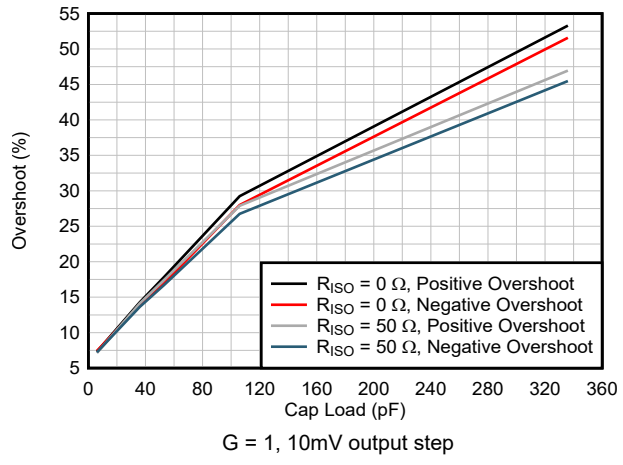


Figure 5-11. Small-Signal Overshoot vs Capacitive Load

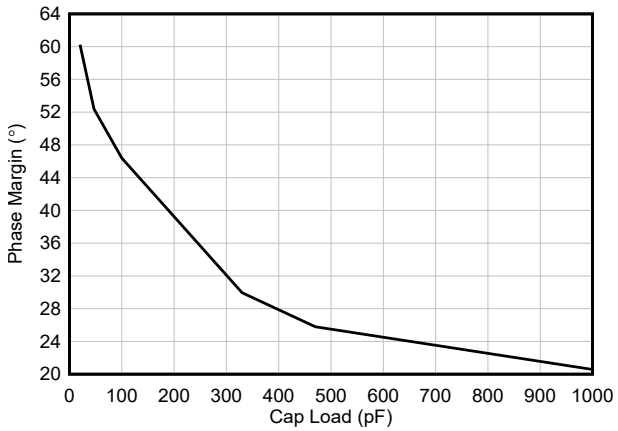
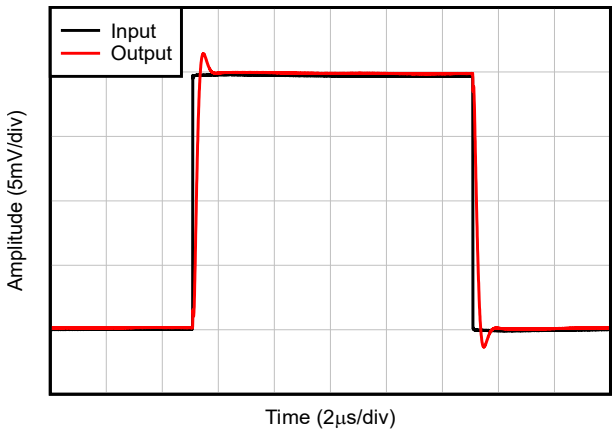


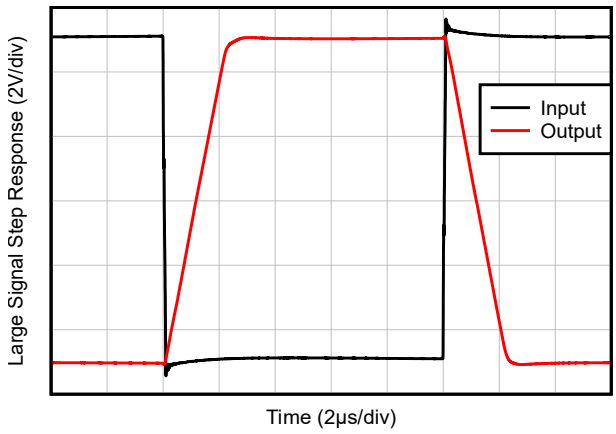
Figure 5-12. Phase Margin vs Capacitive Load

5.16 Typical Characteristics (continued)



C_L = 20pF, G = 1, 20mV step response

Figure 5-13. Small-Signal Step Response



C_L = 20pF, G = –1

Figure 5-14. Large-Signal Step Response

6 Parameter Measurement Information

6.1 Typical Values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

6.2 Input Bias and Offset Current

At the picoampere bias current level typical of the TL03x and TL03xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test-socket leakages easily can exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

6.3 Noise

With the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is performed at f = 1kHz, unless otherwise noted.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

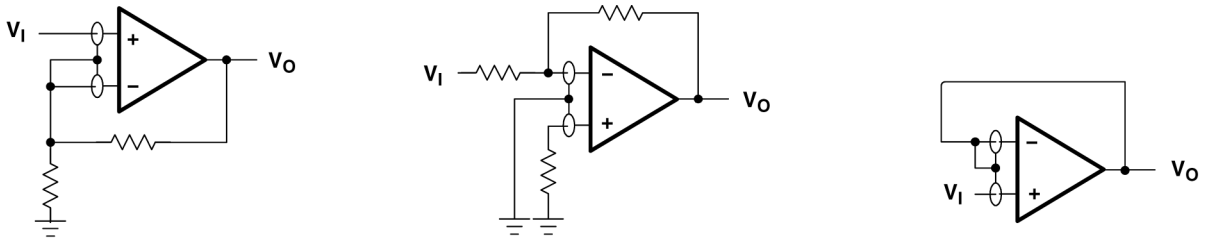
7.1 Application Information

7.1.1 Input Characteristics

The TL03x and TL03xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Due to of the extremely high input impedance and resulting low bias-current requirements, the TL03x and TL03xA are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets easily can exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 7-1). These guard rings should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded unity-gain followers to avoid oscillation.



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 7-1. Use of Guard Rings

7.1.2 Output Characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100pF load capacitance. The TL03x and TL03xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 7-3). Capacitive loads of 1000pF and larger can be driven if enough resistance is added in series with the output (see Figure 7-2).

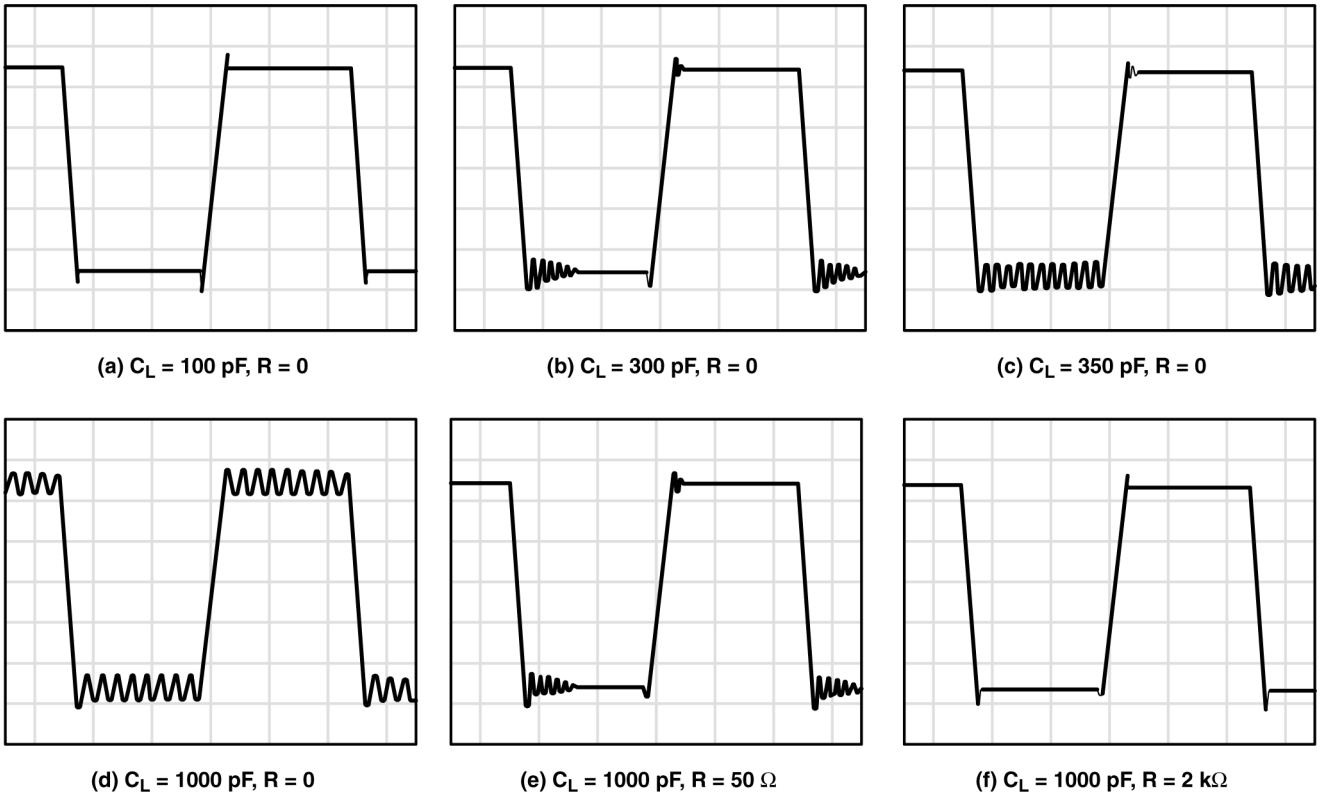
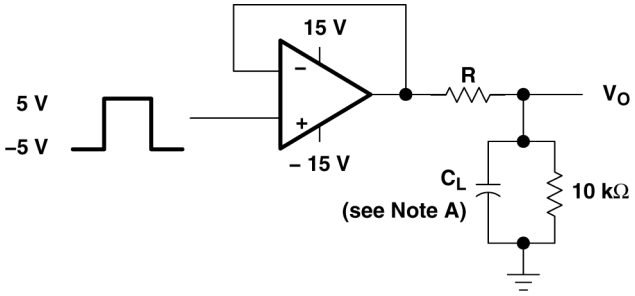


Figure 7-2. Effect of Capacitive Loads



A. C_L includes fixture capacitance.

Figure 7-3. Test Circuit for Output Characteristics

7.1.3 Transimpedance Amplifier

The low-power precision TL03x allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL03xA greatly simplify the design of a transimpedance amplifier. At room temperature, this design achieves 10-bit accuracy with an error of less than 1/2 LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F\left(\frac{R1 + R2}{R2}\right)$$

Using the resistor values shown in the schematic for a 1nA input current, the output voltage equals −0.1V. If the V_O limit for the TL03xA is measured at ±12V, the maximum input current for these resistor values is ±120nA. Similarly, one LSB on a 10-bit scale corresponds to 12mV of output voltage, or 120pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = -\left[V_{IO} + R_F\left(I_{IO} + I_{IB}\right)\right]\left(\frac{R1 + R2}{R2}\right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard PN diodes. Instead, use low-leakage Siliconix SN4117 FETs (or equivalent) connected as diodes across the TL03xA inputs (see Figure 7-4).

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using high-quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.

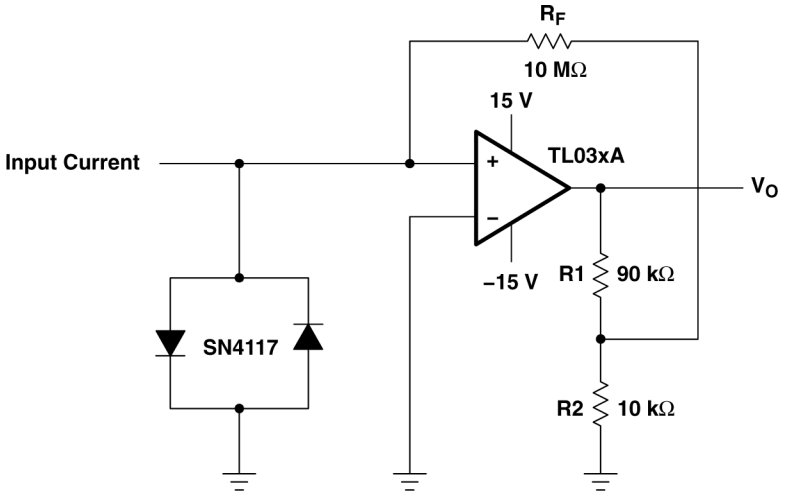


Figure 7-4. Transimpedance Amplifier

7.1.4 4mA to 20mA Current Loops

Often, information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The circuit in Figure 7-5 requires three wires from the transmitting to receiving circuitry, while the second variation in Figure 7-6 requires only two wires, but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL03xA because many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL03xA is zero, the following equation determines the output current:

$$I_O = V_I\left(\frac{R3}{R1 \times R_S}\right) + 5V\left(\frac{R3}{R2 \times R_S}\right) = 0.16 \times V_I + 4mA$$

The circuits presently provide 4mA to 20mA output current for an input voltage of 0 to 100mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL03xA is used:

$$I_O = V_I\left(\frac{R3}{R1 \times R_S}\right) + 5V\left(\frac{R3}{R2 \times R_S}\right) - V_I\left(\frac{R3}{R1 \times R_S} + \frac{R3}{R2 \times R_S} + \frac{R1}{R_S}\right)$$
$$= 0.16 \times V_I + 4mA - 0.17 \times V_I$$

For example, an offset voltage of 1mV decreases the output current by 0.17mA.

Due to the low power consumption of the TL03xA, both circuits have at least 2mA available to drive the actual sensor from the 5V reference node.

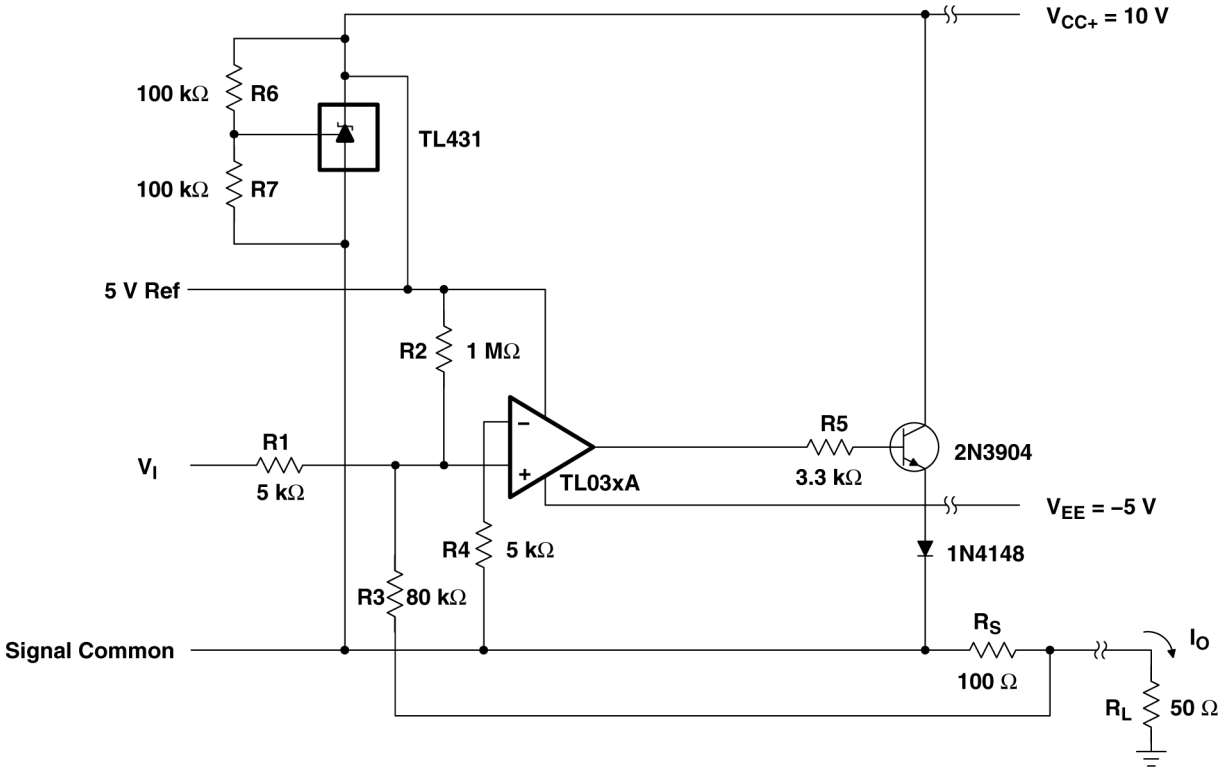


Figure 7-5. Three-Wire 4mA to 20mA Current Loop

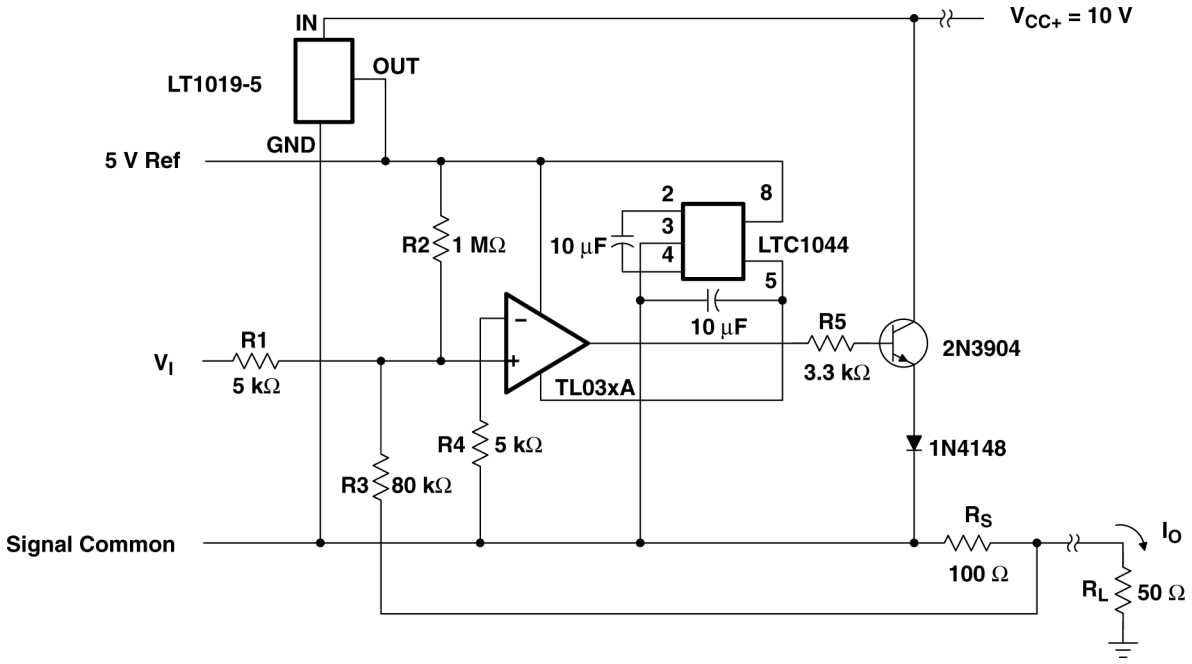


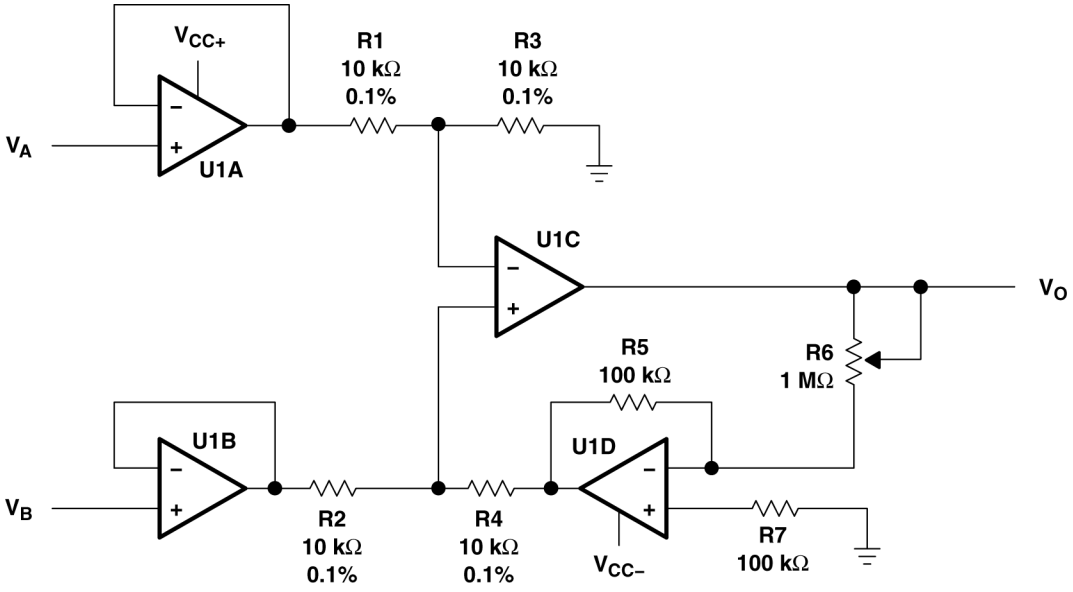
Figure 7-6. Two-Wire 4mA to 20mA Current Loop

7.1.5 Instrumentation Amplifier with Linear Gain Adjust

The low offset voltage and low power consumption of the TL03x provide an accurate but inexpensive instrumentation amplifier (see Figure 7-7). This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R6}{R5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 always must be greater than, or equal to, the value of R5 to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors must be 0.1%-tolerance resistors.



A. U1A through U1D = TL03x; $V_{CC\pm}$ = ±15V

Figure 7-7. Instrumentation Amplifier with Linear Gain-Adjust Circuit

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2001) to Revision D (April 2026) **Page**

- Updated on-chip offset-voltage trimming from TL031A to TL031ID in the *Features* ... 1
- Added links to applications in the *Applications* section... 1
- Updated the numbering format for tables, figures, and cross-references throughout the document... 1
- Deleted Equivalent schematic from the document... 1
- Deleted the *Available Options* table from the document... 1
- Changed from *JFET-input* and *BiFET-input* to *FET-input* throughout the document... 1
- Deleted references to M-suffix devices throughout the document... 1
- Updated Pin diagram as per new die... 3
- Added *Pin Functions* tables... 3
- Updated pin diagrams to new format... 3
- Deleted references to FK, J, and JG packages in the *Absolute Maximum Ratings* table... 6
- Deleted Total current into V_{CC+} and out of V_{CC-} spec in *Absolute Maximum Ratings* table... 6
- Deleted Continuous total power dissipation row in *Absolute Maximum Ratings* table... 6
- Moved package thermal impedance information into the *Thermal Information* table... 6
- Deleted the *Dissipation Ratings* table from the document... 6
- Added the *Thermal Information* table... 6
- Deleted all M-suffix package information in the *Recommended Operating Conditions* table... 6
- Changed Input offset voltage for TL031AC at 25°C maximum value from 0.8mV to 1.5mV in all *Electrical Characteristics* tables... 7
- Changed Input offset current typical value at 25°C from 1pA to 5pA in all *Electrical Characteristics* tables... 7
- Changed Input bias current typical value at 25°C from 2pA to 10pA in all *Electrical Characteristics* tables... 7
- Changed Common-mode input voltage range typical for 5V at 25°C from 5.2V to 5.4V in all *Electrical Characteristics* tables... 7
- Changed Common-mode input voltage range typical for 15V at 25°C from 15.2V to 15.4V in all *Electrical Characteristics* tables... 7
- Changed Maximum positive and negative peak output voltage swing typical for 5V at 25°C from ±4.3V to ±4.995V in all *Electrical Characteristics* tables... 7
- Changed Maximum positive and negative peak output voltage swing typical for 15V at 25°C from ±14V to ±14.955V in all *Electrical Characteristics* tables... 7
- Changed Large-signal differential voltage amplification minimum value at 25°C to 72dB in all *Electrical Characteristics* tables... 7
- Changed Large-signal differential voltage amplification at 0°C and 70°C typical value from 11.1V/mV and 13.5V/mV to 125dB in all *Electrical Characteristics* tables... 7
- Changed Input Capacitance for 5V from 5pF to 4pF in all *Electrical Characteristics* tables... 7
- Changed Common Mode Rejection Ratio 5V typical values from 87dB to 90dB in all *Electrical Characteristics* tables... 7
- Changed Supply Voltage Rejection Ratio typical values from 96dB to 140dB in all *Electrical Characteristics* tables... 7
- Deleted Total power dissipation spec in all *Electrical Characteristics* tables... 7
- Changed Supply Current per amplifier typical value for 5V from 192µA to 130µA and 15V from 217µA to 130µA... 7
- Deleted Supply Current per amplifier typical value for 0°C and 70°C... 7
- Deleted Rise time, Fall time and Overshoot factor specs in all *Operating Characteristics* tables... 8
- Deleted minimum values for Positive and Negative slew rate at unity gain in all *Operating Characteristics* tables... 8
- Changed Equivalent input noise voltage from 61nV/$\sqrt{Hz}$ to 115nV/$\sqrt{Hz}$ and from 41nV/$\sqrt{Hz}$ to 30nV/$\sqrt{Hz}$ in all *Operating Characteristics* tables... 8
- Changed Equivalent input noise current from 0.003pA/$\sqrt{Hz}$ to 2fA/$\sqrt{Hz}$ in all *Operating Characteristics* tables 8

- Changed Phase margin at unity gain from 61° and 65° to 60° in all *Operating Characteristics* tables..... 8
- Changed Unity gain bandwidth for 5V from 1MHz to 1.1MHz in all *Operating Characteristics* tables..... 8
- Changed Supply Current per amplifier typical value for 5V from 192µA to 130µA and 15V from 217µA to 130µA..... 9
- Deleted Supply Current per amplifier typical value for −40°C and 85°C..... 9
- Changed Supply Current per amplifier typical value for ±5V from 368µA to 120µA and ±15V from 422µA to 120µA and maximum values for ±5V from 500µA to 250µA and for ±15V from 560µA to 280µA..... 11
- Deleted Supply Current per amplifier typical value for 70°C..... 11
- Changed Equivalent input noise voltage from 49nV/√Hz to 115nV/√Hz and from 41nV/√Hz to 30nV/√Hz in all *Operating Characteristics* tables..... 12
- Changed Supply Current per amplifier typical value for 5V from 384µA to 120µA and 15V from 434µA to 120µA and maximum values for ±5V from 500µA to 250µA and for ±15V from 560µA to 280µA..... 13
- Deleted Supply Current per amplifier typical value for −40°C and 85°C..... 13
- Changed Equivalent input noise voltage from 49nV/√Hz to 115nV/√Hz and from 41nV/√Hz to 30nV/√Hz in all *Operating Characteristics* tables..... 14
- Changed Supply Current per amplifier typical value for ±5V from 770µA to 120µA and ±15V from 870µA to 120µA and maximum values for ±5V from 1000µA to 250µA and for ±15V from 1120µA to 280µA..... 15
- Deleted Supply Current per amplifier typical value for 70°C and 0°C..... 15
- Updated plots as per New Die characteristics in *Typical Characteristics* 19
- Deleted all figures from the *Parameter Measurement Information* section 22
- Deleted *High-Q Notch Filter*, *Low-level Light-detector Preamplifier*, and *Audio-distribution Amplifier* sections from the document..... 23

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL031CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	TL031C
TL031CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL031C
TL031CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL031C
TL031CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL031CP
TL031CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL031CP
TL031ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL031I
TL031ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL031I
TL031IDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL031I
TL031IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL031IP
TL031IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL031IP
TL032ACD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	032AC
TL032ACDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	032AC
TL032ACDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	032AC
TL032ACDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	032AC
TL032ACDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	032AC
TL032ACP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL032ACP
TL032ACP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL032ACP
TL032AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	032AI
TL032AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	032AI
TL032AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	032AI
TL032AIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL032AIP
TL032AIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL032AIP
TL032CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	TL032C
TL032CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL032C
TL032CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL032C
TL032CDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL032C
TL032CDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL032C
TL032CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL032CP
TL032CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL032CP

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL032CPE4	Active	Production	PDIP (P) | 8	50 | TUBE	-	Call TI	Call TI	0 to 70	
TL032CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T032
TL032CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T032
TL032ID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	TL032I
TL032IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL032I
TL032IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL032I
TL032IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL032IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL032IP
TL032IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL032IP
TL034ACD	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	0 to 70	TL034AC
TL034ACDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034AC
TL034ACDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034AC
TL034ACN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL034ACN
TL034ACN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL034ACN
TL034AID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	TL034AI
TL034AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL034AI
TL034AIDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL034AI
TL034AIN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL034AIN
TL034AIN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL034AIN
TL034CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034C
TL034CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034C
TL034CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL034CN
TL034CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL034CN
TL034CNSR	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034
TL034CNSR.A	Active	Production	SOP (NS) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL034
TL034CPW	Obsolete	Production	TSSOP (PW) | 14	-	-	Call TI	Call TI	0 to 70	T034
TL034CPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T034
TL034CPWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T034
TL034ID	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-40 to 85	TL034I
TL034IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL034I
TL034IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL034I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL034IDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TL034IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL034IN
TL034IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL034IN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

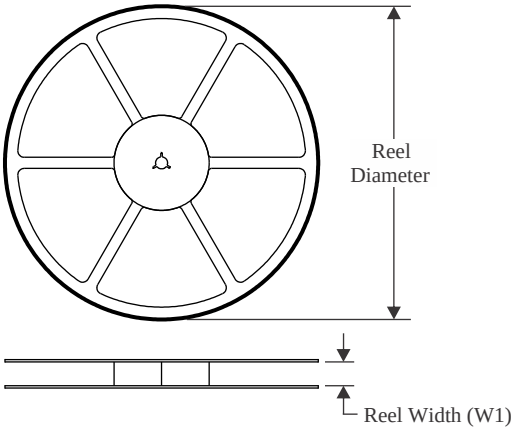
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

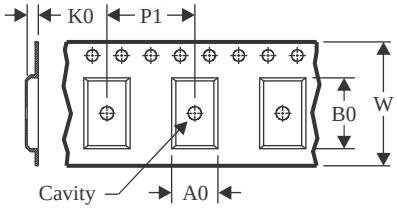
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

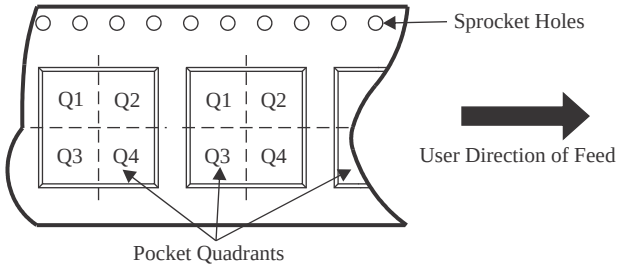


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

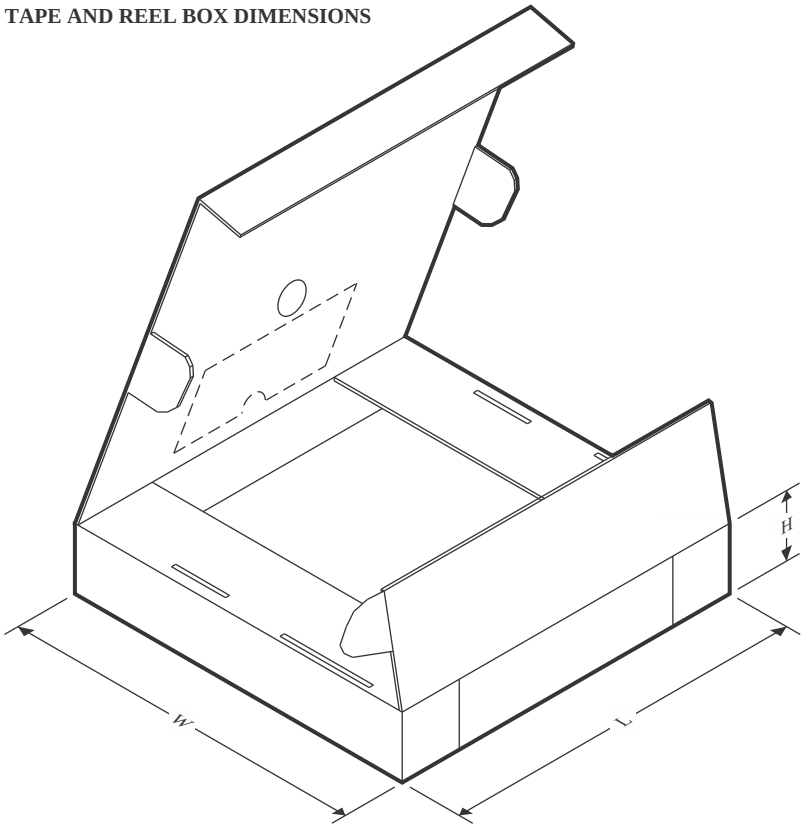
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL031CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032ACDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032CDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL032CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL032IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL034ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL034CNSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
TL034CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL034CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL034IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

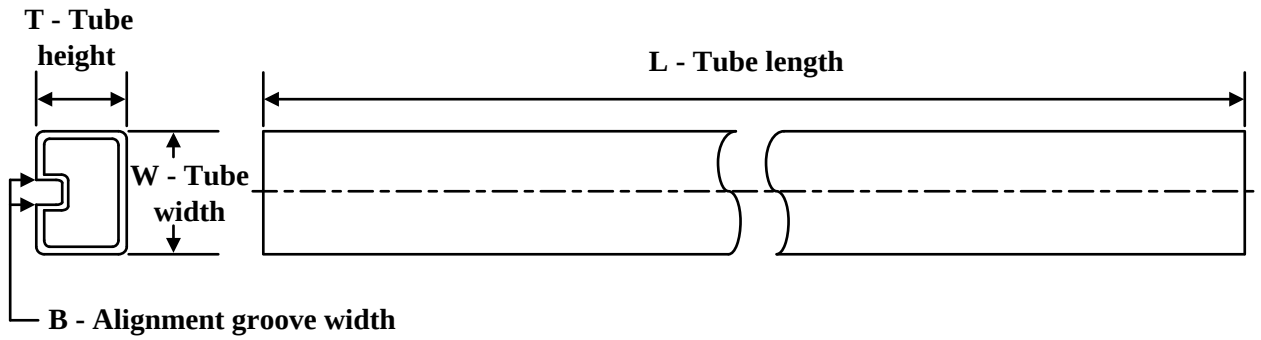
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

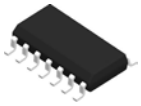
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL031CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL032ACDR	SOIC	D	8	2500	353.0	353.0	32.0
TL032ACDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL032AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TL032CDR	SOIC	D	8	2500	353.0	353.0	32.0
TL032CDRG4	SOIC	D	8	2500	353.0	353.0	32.0
TL032CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL032IDR	SOIC	D	8	2500	353.0	353.0	32.0
TL034ACDR	SOIC	D	14	2500	353.0	353.0	32.0
TL034AIDR	SOIC	D	14	2500	353.0	353.0	32.0
TL034CDR	SOIC	D	14	2500	353.0	353.0	32.0
TL034CNSR	SOP	NS	14	2000	353.0	353.0	32.0
TL034CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL034CPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TL034IDR	SOIC	D	14	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL031CP	P	PDIP	8	50	506	13.97	11230	4.32
TL031CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL031ID	D	SOIC	8	75	507	8	3940	4.32
TL031ID.A	D	SOIC	8	75	507	8	3940	4.32
TL031IDG4	D	SOIC	8	75	507	8	3940	4.32
TL031IP	P	PDIP	8	50	506	13.97	11230	4.32
TL031IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL032ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL032ACP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL032AIP	P	PDIP	8	50	506	13.97	11230	4.32
TL032AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL032CP	P	PDIP	8	50	506	13.97	11230	4.32
TL032CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL032IP	P	PDIP	8	50	506	13.97	11230	4.32
TL032IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL034ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL034ACN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL034AIN	N	PDIP	14	25	506	13.97	11230	4.32
TL034AIN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL034CN	N	PDIP	14	25	506	13.97	11230	4.32
TL034CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TL034IN	N	PDIP	14	25	506	13.97	11230	4.32
TL034IN.A	N	PDIP	14	25	506	13.97	11230	4.32

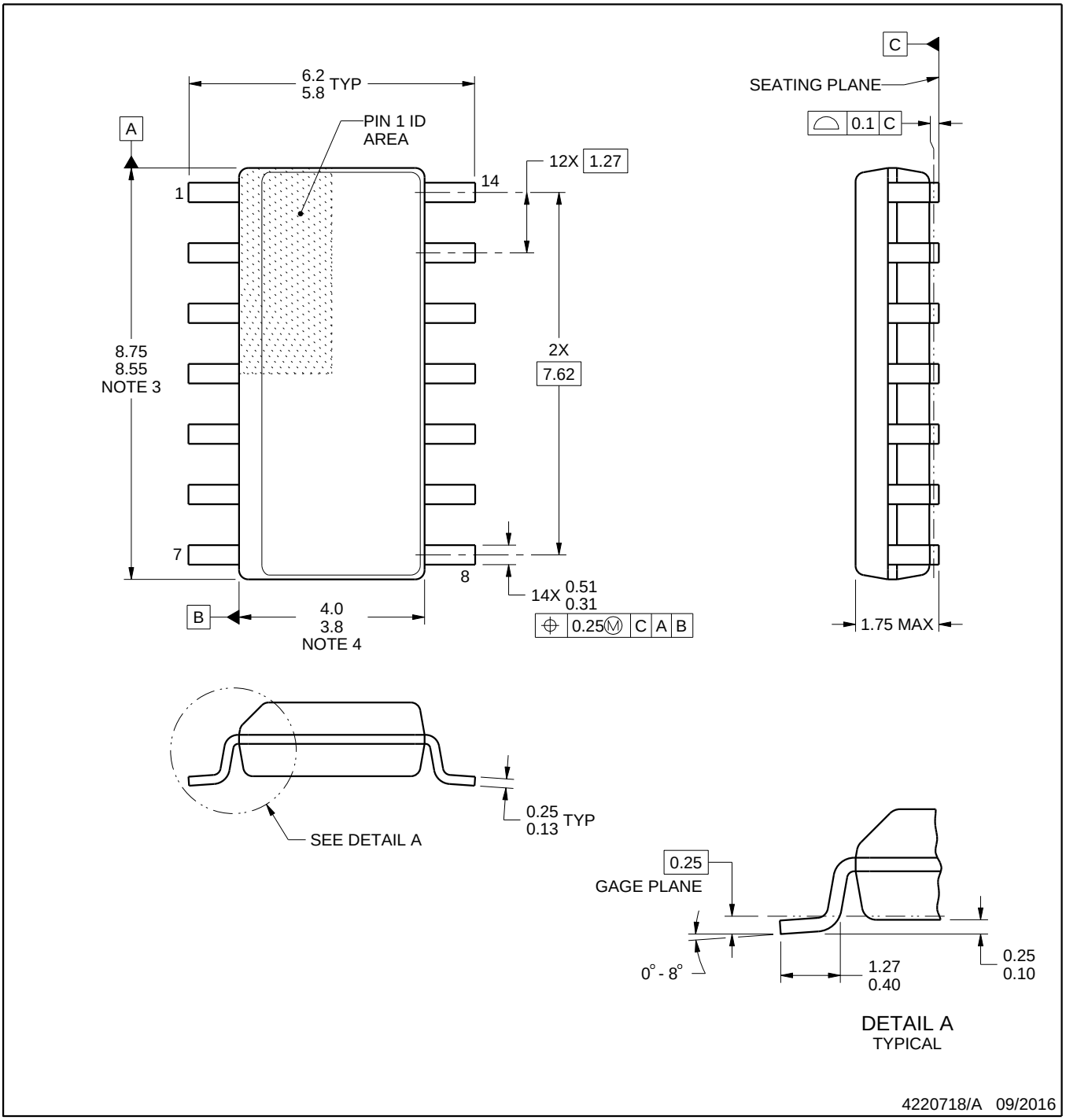


PACKAGE OUTLINE

D0014A

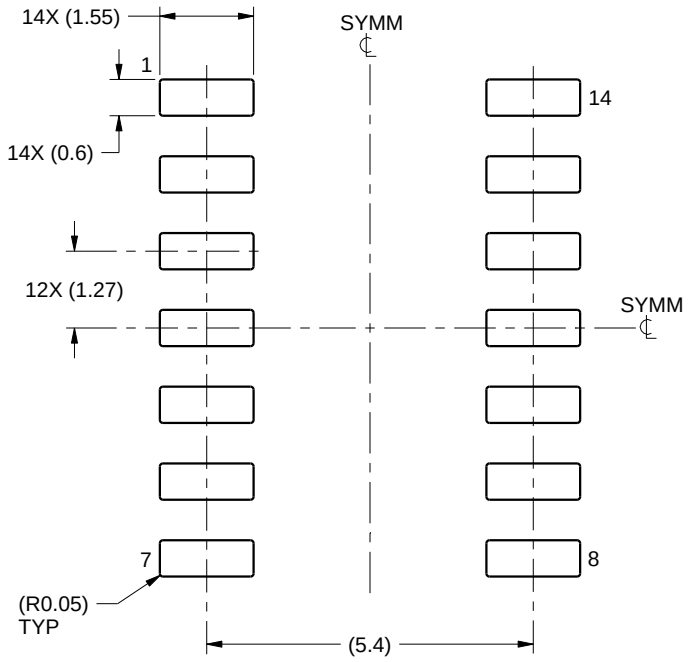
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

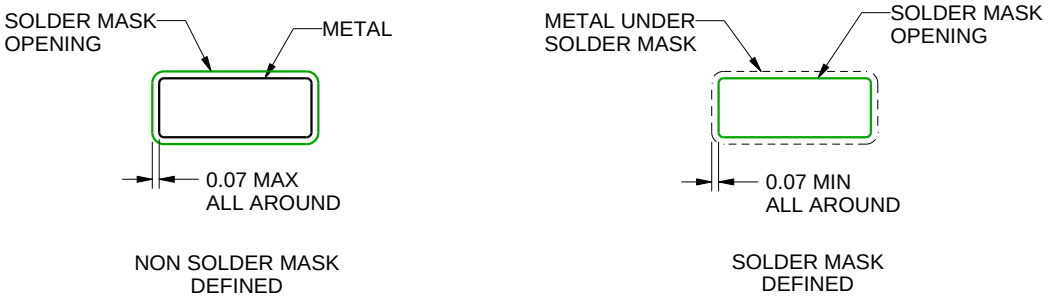


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

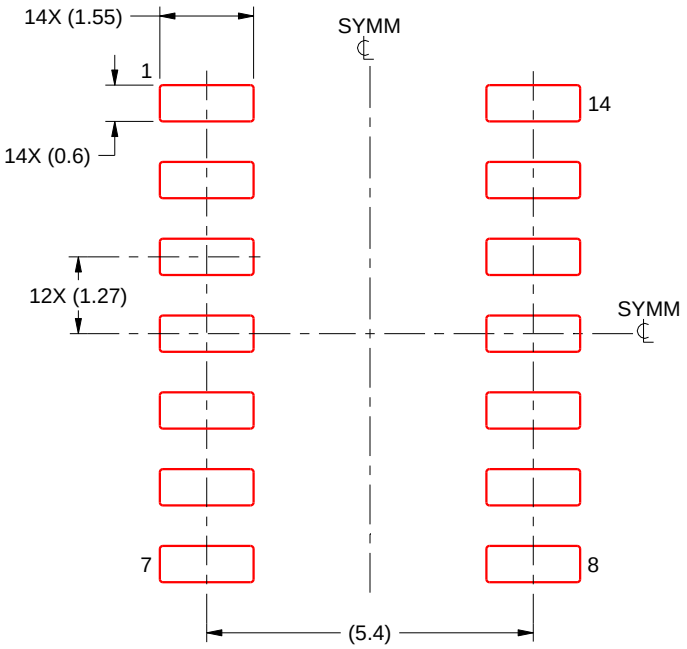
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

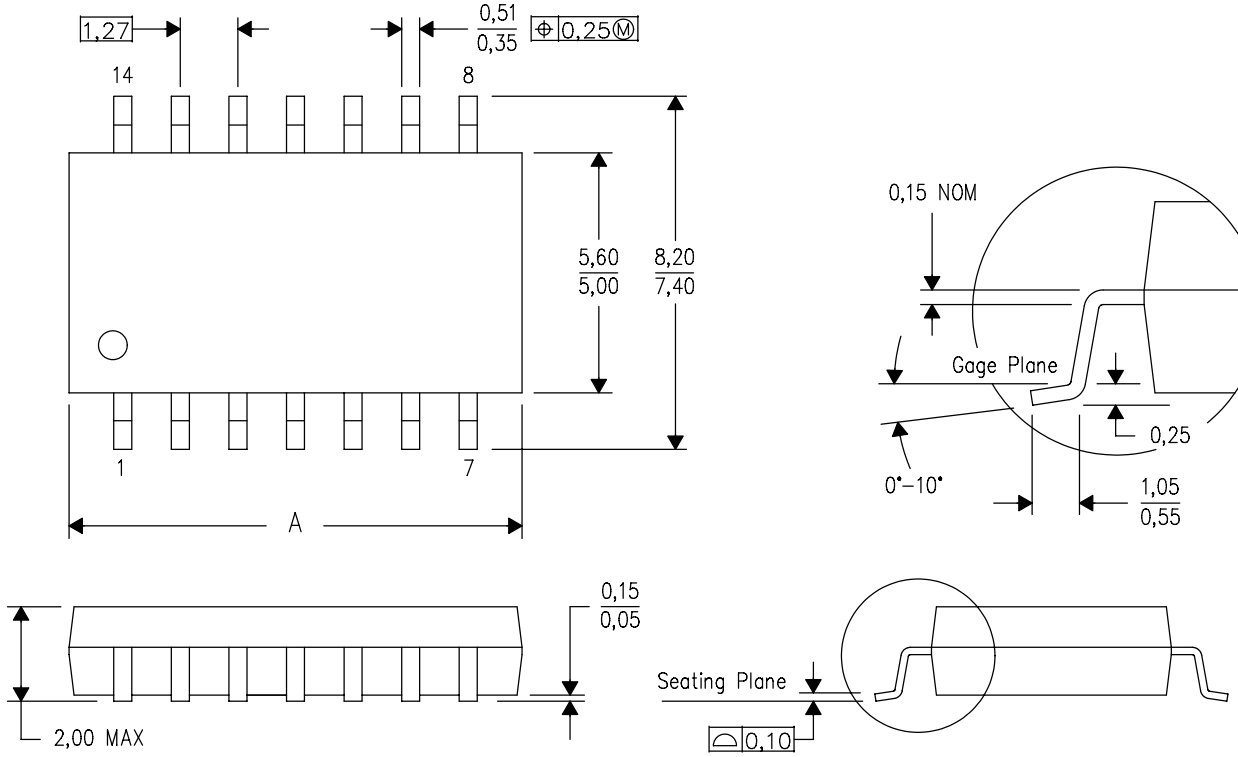
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

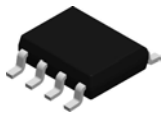
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

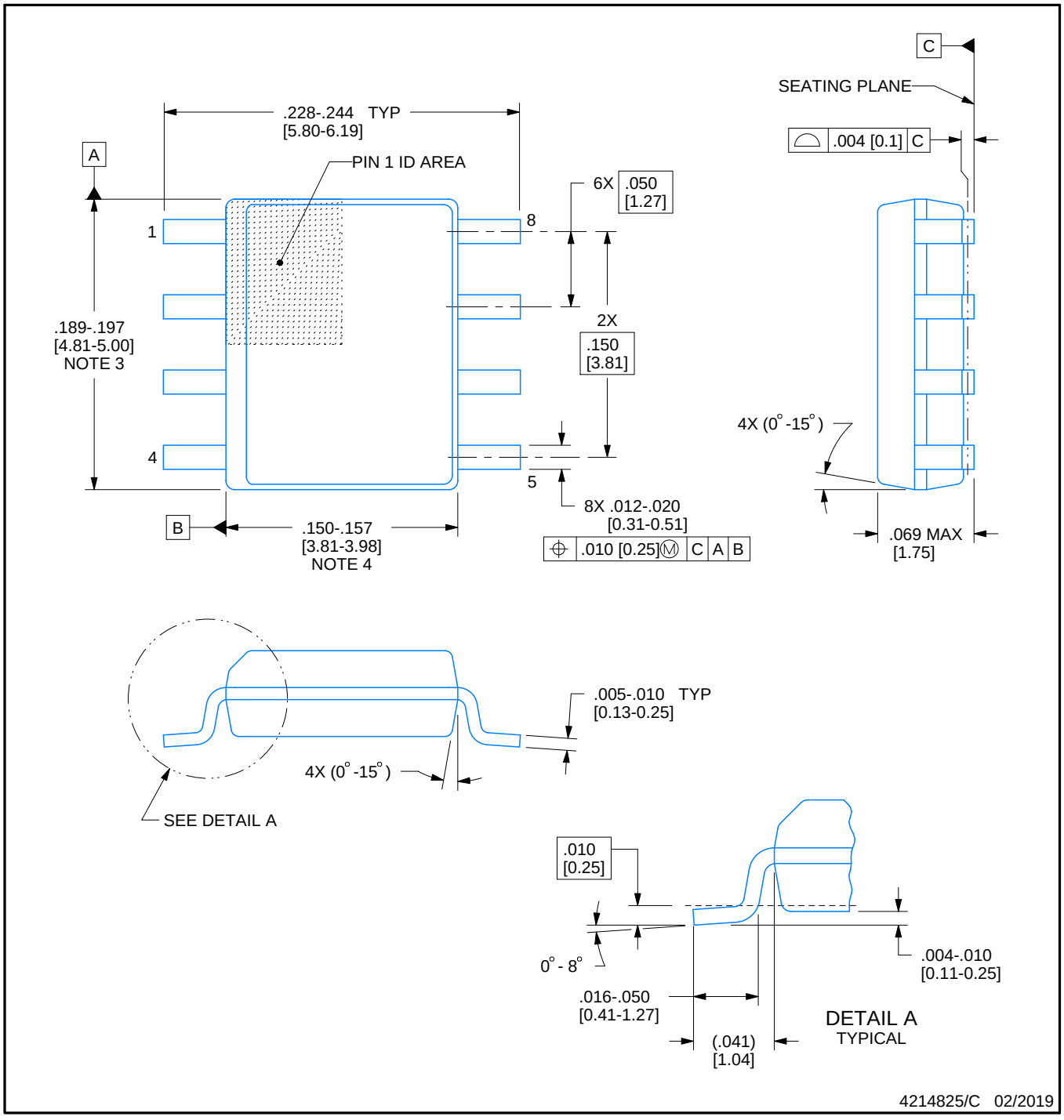


PACKAGE OUTLINE

D0008A

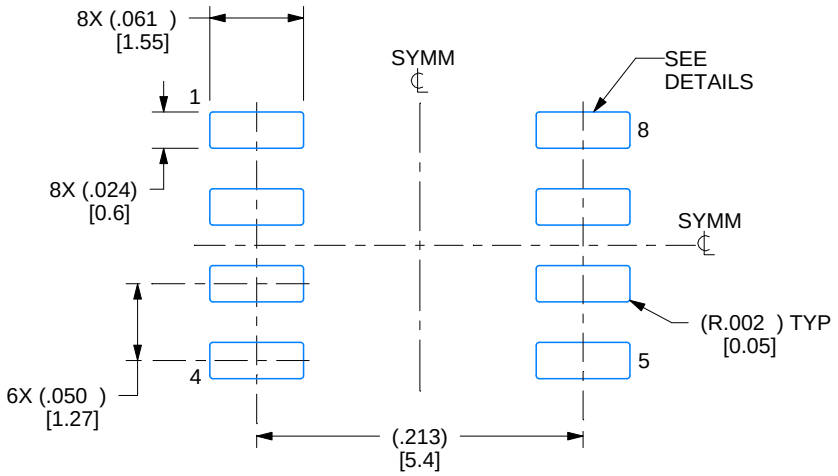
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

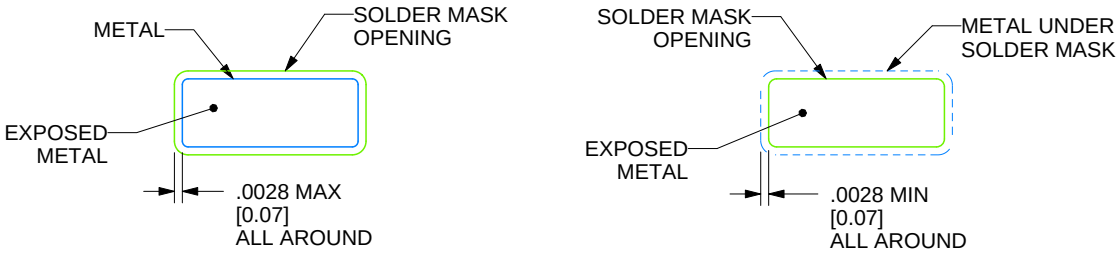


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

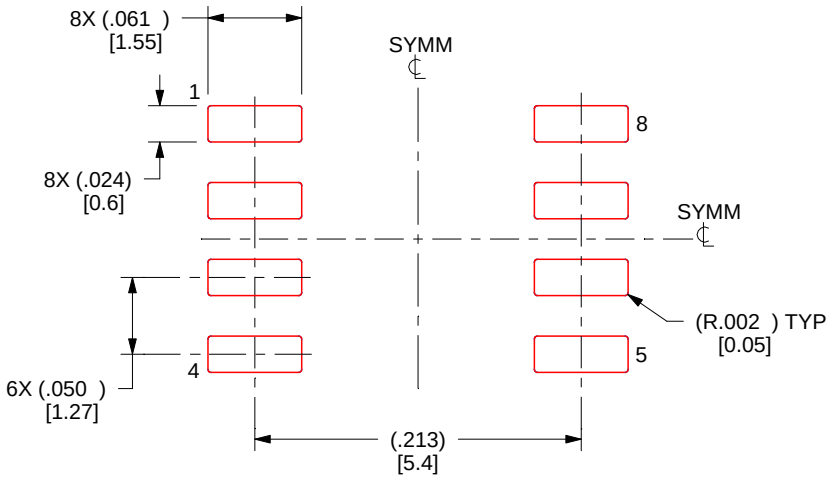
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

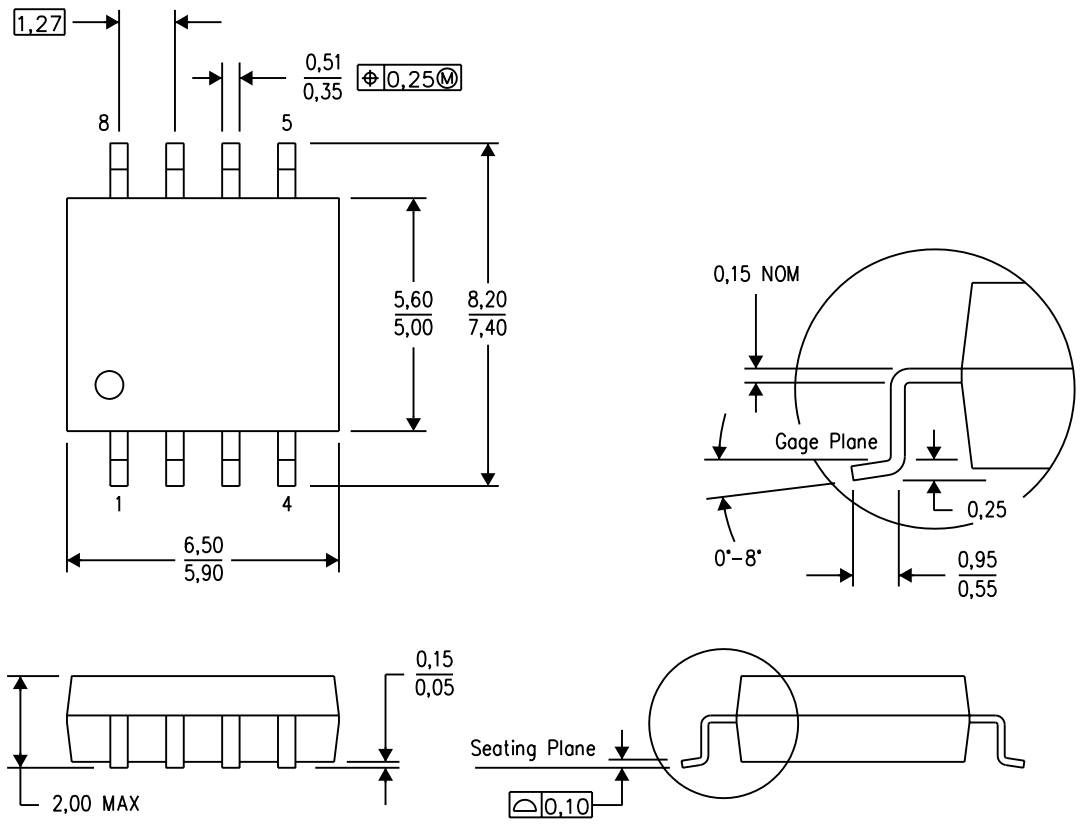
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

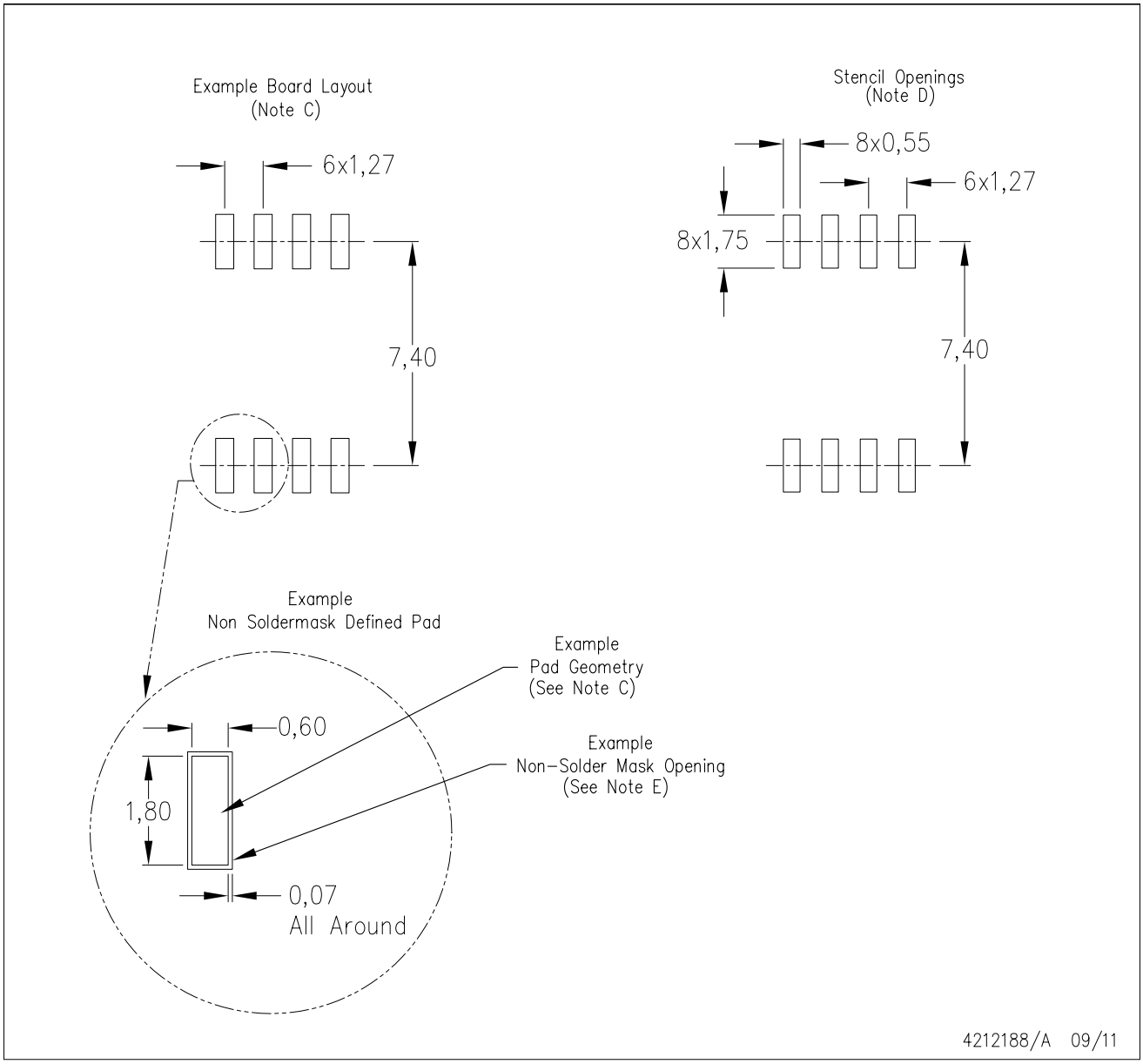
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

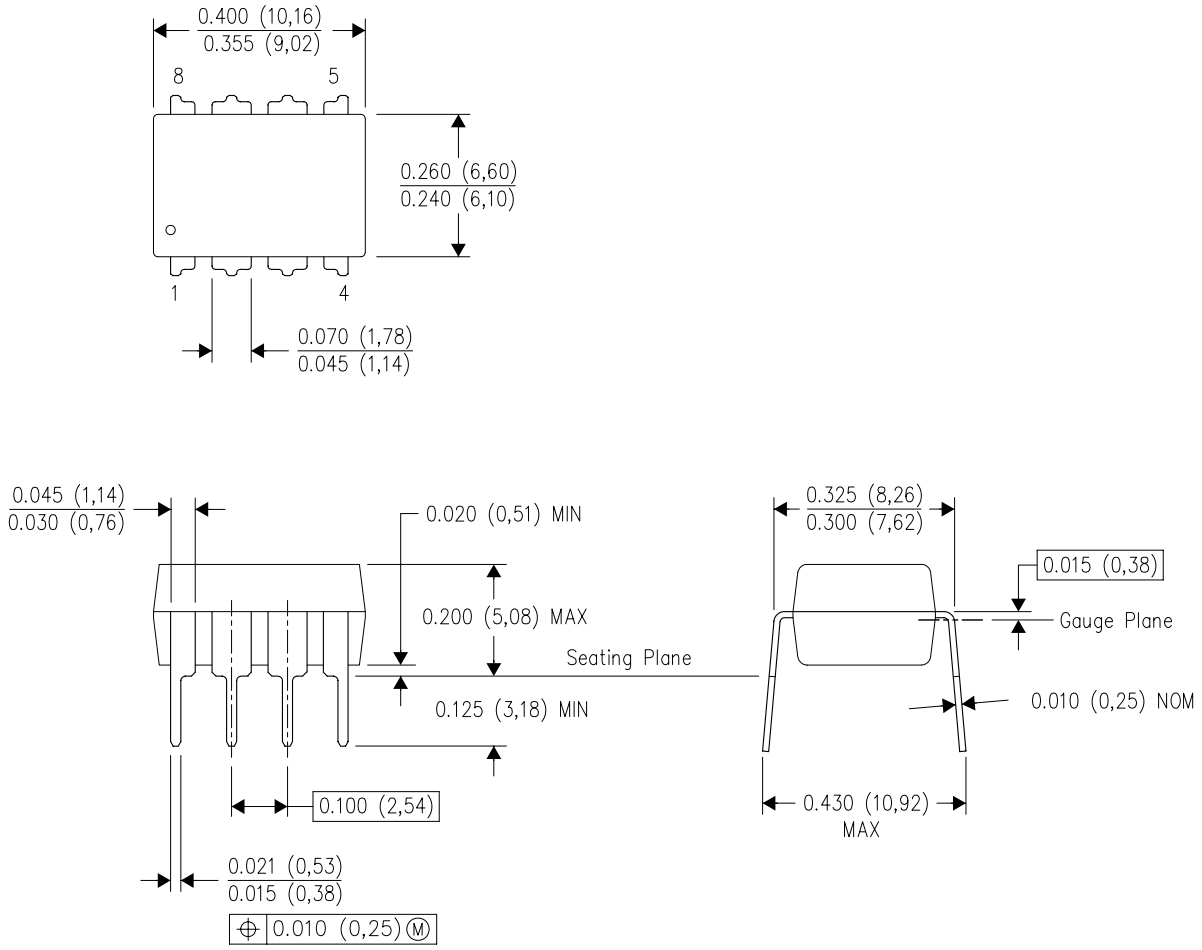
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

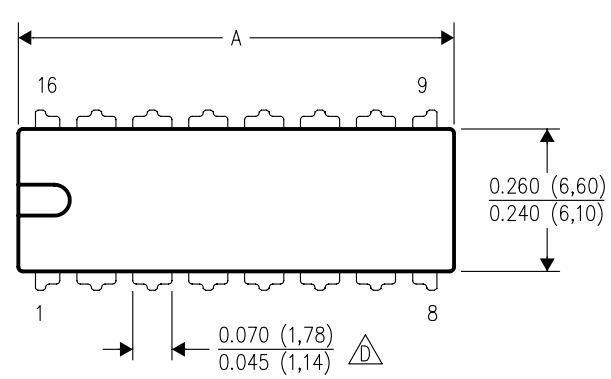


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

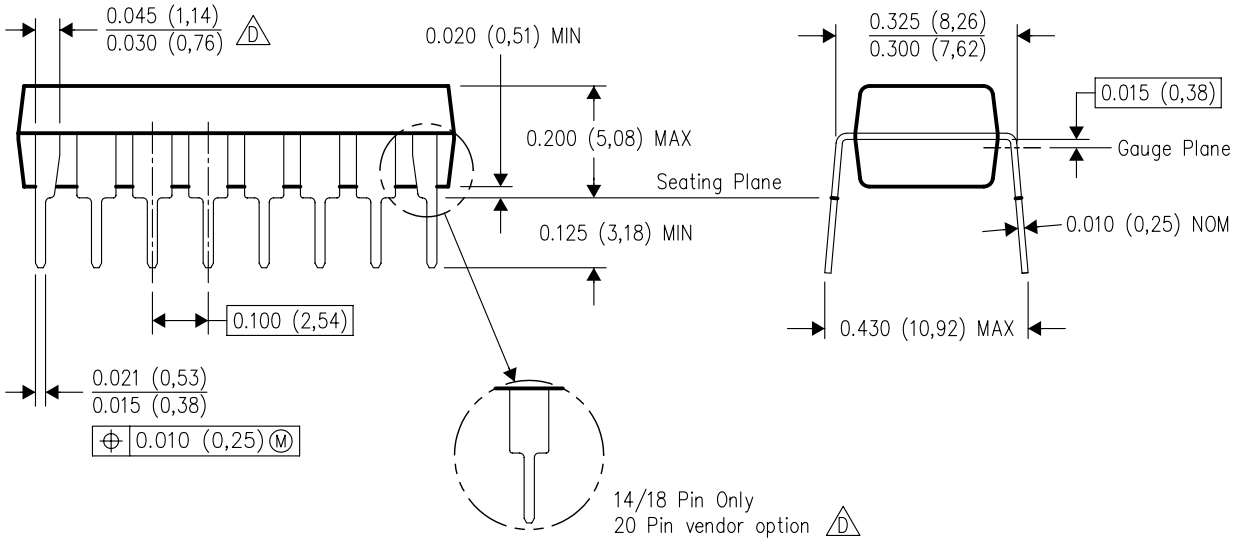
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

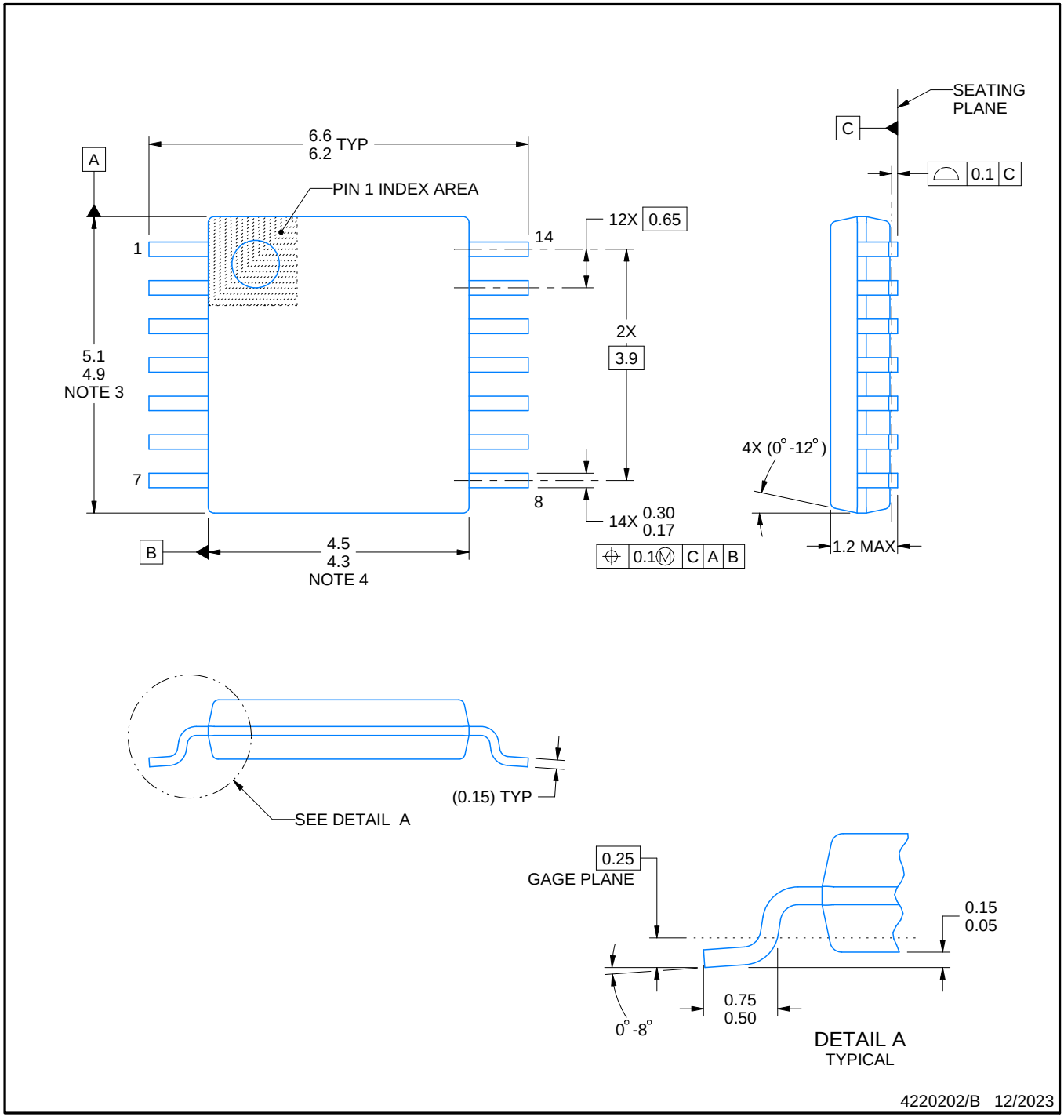
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

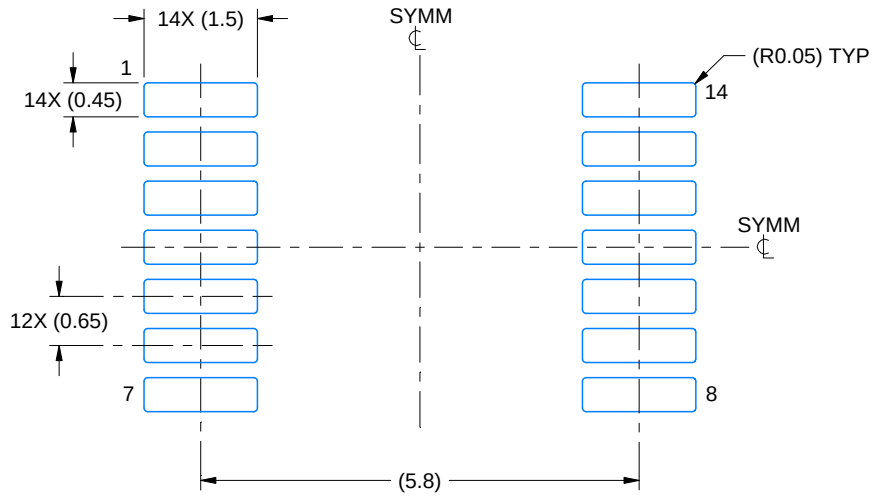
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

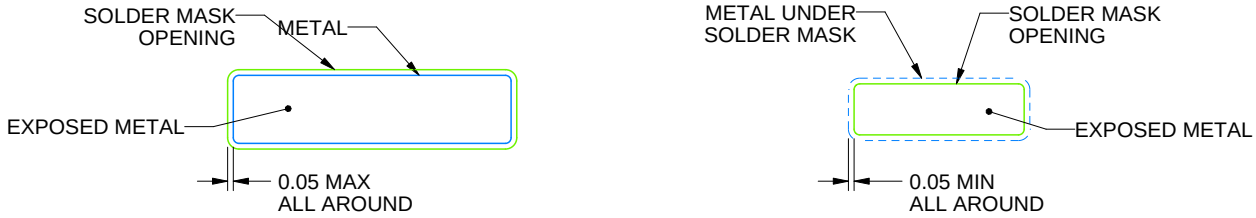


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

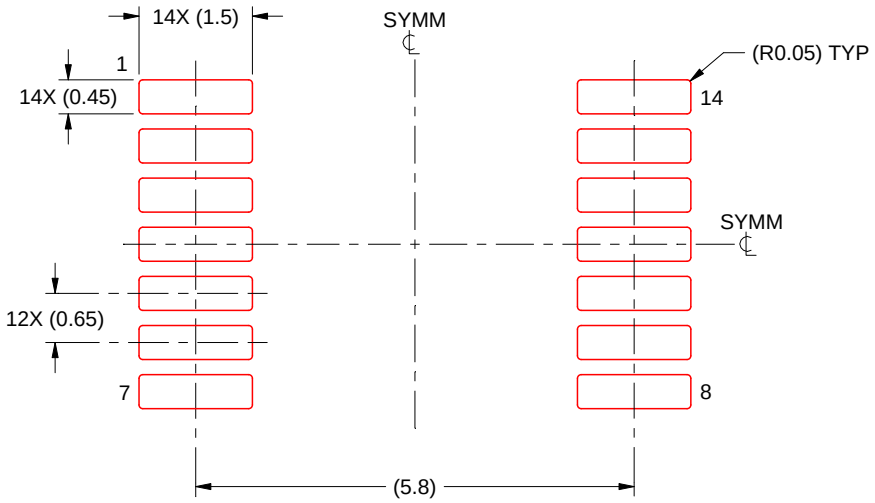


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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