

TL343 Single Low-Power Operational Amplifier

1 Features

- Wide range of supply voltages, single supply 3V to 30V, or dual supplies
- Class AB output stage
- True differential-input stage
- Low input bias current
- Short-circuit protection

2 Applications

- [Multiplexed data-acquisition systems](#)
- [Test and measurement equipment](#)
- [Motor drive: power stage and control modules](#)
- [Power delivery: UPS, server, and merchant network power](#)
- [ADC driver and reference buffer amplifier](#)
- [Programmable logic controllers](#)
- [Analog input and output modules](#)
- [High-side and low-side current sensing](#)
- [High precision comparator](#)

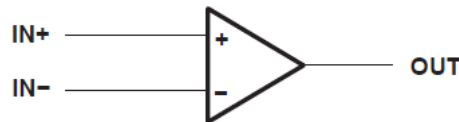
3 Description

The TL343 is a single operational amplifier with excellent DC precision and AC performance. Operational amplifier is designed to operate from a single supply over a range of voltages from 3V to 30V. Operation from split supplies also is possible, provided the difference between the two supplies is 3V to 30V. The common-mode input range includes the negative supply. Output range is from the negative supply to $V_{CC} - 1.5V$.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
TL343IDBVR	DBV (SOT-23 5)	2.90mm × 1.60mm
TL343IDBVT		2.90mm × 1.60mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Symbol



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4 Pin Configuration and Functions

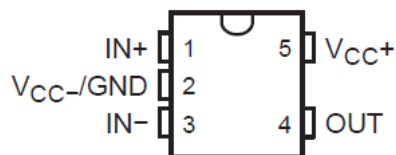


Figure 4-1. DBV Package (Top View)

Table 4-1. Pin Functions

NAME	PIN NO.	TYPE ⁽¹⁾	DESCRIPTION
IN+	1	I	Non inverting input
VCC– / GND	2	—	Power supply negative or ground
IN–	3	I	Inverting input
OUT	4	O	Output
VCC+	5	—	Positive power supply

(1) I = input, O = output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply voltage, $V_S = (V+) - (V-)$		0	36	V
Signal input pins	Common-mode voltage ⁽³⁾	$(V-) - 0.5$	$(V+) + 0.5$	V
	Differential voltage ⁽³⁾		$V_S + 0.2$	V
	Current ⁽³⁾	-10	10	mA
Output short-circuit ⁽²⁾		Continuous		
Operating ambient temperature, T_A		-55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to ground, one amplifier per package. Extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual destruction. See the Thermal Protection section for more information.
- (3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10 mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Single-supply voltage	3	30	V
V_{CC+}	Dual-supply voltage	1.5	15	V
V_{CC-}		-1.5	-15	
T_A	Operating free-air temperature	-40	125	°C

5.4 Thermal information

THERMAL METRIC ⁽¹⁾		TL343	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	37.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

at specified free-air temperature, $V_{CC\pm} = \pm 15V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{CM} = V_-$	25°C		±0.3	10	mV
			Full range			12	
$a_{V_{IO}}$	Temperature coefficient of input offset voltage		Full range		0.6		μV/°C
I_{IO}	Input offset current		25°C		±0.005	50	nA
I_{IB}	Input bias current		25°C		±0.01	–500	nA
V_{ICR}	Common-mode input voltage range		25°C	(V–) to 13	(V–) – 0.2 to (V+) + 0.2		V
V_{OM}	Peak output-voltage swing	$R_L = 10k\Omega$	25°C	±12	±14.95		V
		$R_L = 2k\Omega$	25°C	±10	±14.8		
			Full range	±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10V$, $R_L = 2k\Omega$	25°C	86	145		dB
			Full range	83			
B_{OM}	Maximum-output-swing bandwidth	$V_{OPP} = 20V$, THD ≤ 5%, $A_{VD} = 1$, $R_L = 10k\Omega$	25°C		40		kHz
B_1	Unity-gain bandwidth	$V_O = 50mV$, $R_L = 10k\Omega$	25°C		1		MHz
θ_m	Phase margin	$C_L = 80pF$, $R_L = 2k\Omega$	25°C		44		Deg
r_i	Input resistance		25°C		540		GΩ
r_o	Output resistance	$f = 1MHz$	25°C		575		WΩ
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$	25°C	70	115		dB
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm 2.5V$ to $\pm 15V$	25°C		0.75	150	μV/V
I_{OS}	Short-circuit output current		25°C	±10	±80		mA
I_{CC}	Total supply current	$I_O = 0A$	25°C		0.13	2.8	mA

5.6 Electrical Characteristics

$V_{CC+} = 3V$ and $5V$, $V_{CC-} = 0V$, $T_A = 25^\circ C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 1.5V$ and $2.5V$			0.3	10	mV
I_{IO}	Input offset current	$V_O = 1.5V$ and $2.5V$			0.005	50	nA
I_{IB}	Input bias current	$V_O = 1.5V$ and $2.5V$			–0.01	–500	nA
V_{OM}	Peak output voltage swing	$R_L = 10k\Omega$		3.3	4.8		V
A_{VD}	Large-signal differential voltage amplification	$V_O = 1.7V$ to $3.3V$, $R_L = 2k\Omega$		86	118		dB
k_{SVR}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC\pm}$)	$V_{CC\pm} = \pm 2.5V$ to $\pm 15V$				150	μV/V
I_{CC}	Supply current	$V_O = 1.5V$ and $2.5V$, No load			0.13	1.75	mA

5.7 Operating Characteristics

$V_{CC\pm} = \pm 15V$, $T_A = 25^\circ C$, $A_{VD}=1$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
SR	Slew rate at unity gain	$V_I = \pm 2V$, $C_L = 20pF$, $R_L = 10k\Omega$	4.5	V/ μs
t_S	Setting time	$V_{STEP} = 2V$, $C_L = 20pF$, $R_L = 10k\Omega$	2	μs
THD+N	Total Harmonic Distortion + Noise	$V_O = 1V_{RMS}$, $G = 1$, $f = 1kHz$	0.002	%

5.8 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $R_{\text{LOAD}} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{pF}$ (unless otherwise noted)

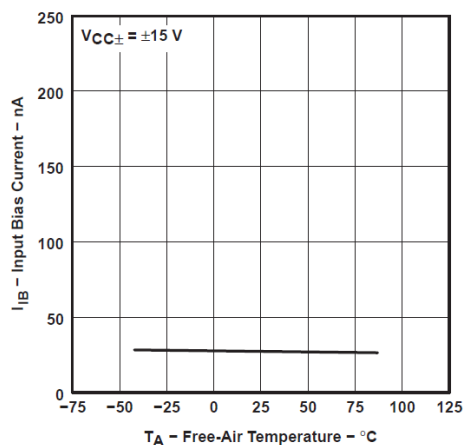


Figure 5-1. Input Bias Current vs Free-Air Temperature, Old Die

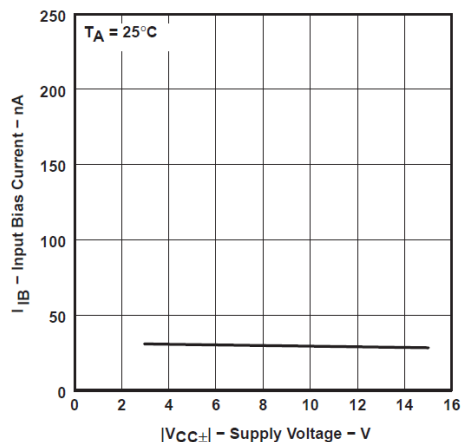


Figure 5-2. Input Bias Current vs Supply Voltage, Old Die

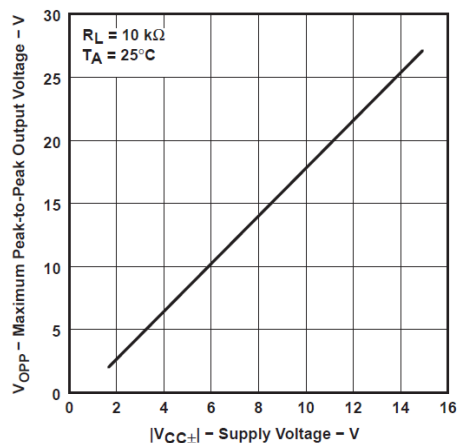


Figure 5-3. Maximum Peak-to-Peak Output Voltage vs Supply Voltage, Old Die

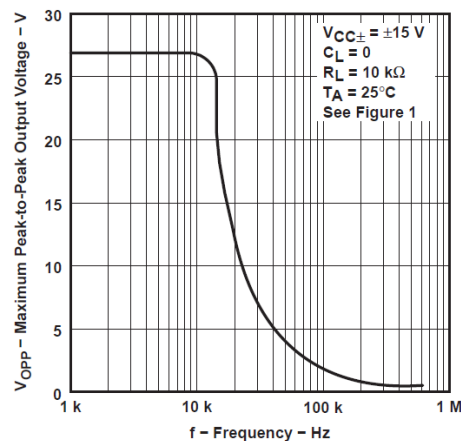


Figure 5-4. Maximum Peak-to-Peak Output Voltage vs Frequency, Old Die

5.8 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $R_{\text{LOAD}} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{pF}$ (unless otherwise noted)

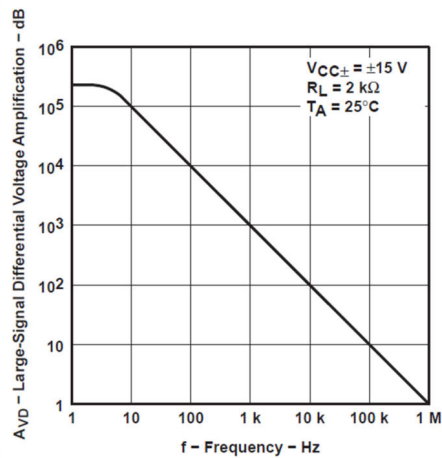


Figure 5-5. Large-Signal Differential Voltage Amplification vs Frequency, Old Die

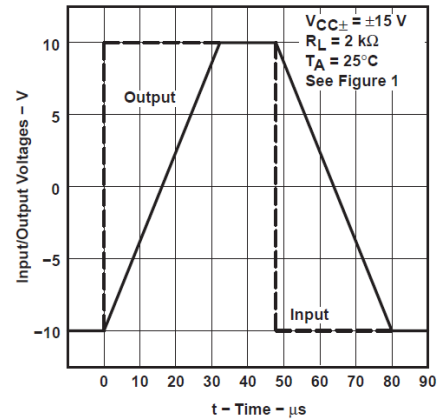


Figure 5-6. Voltage-Follower Large-Signal Pulse Response, Old Die

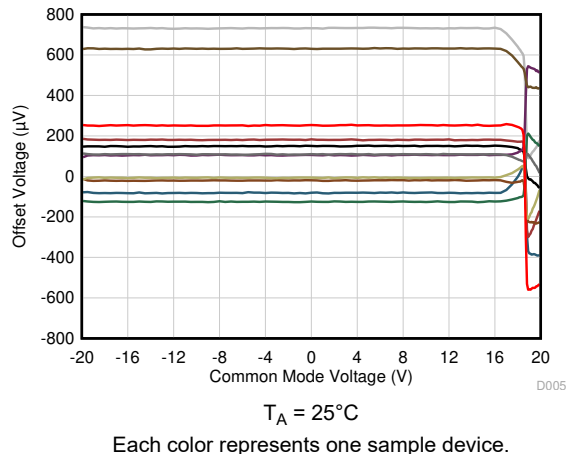


Figure 5-7. Offset Voltage vs Common-Mode Voltage, New Die

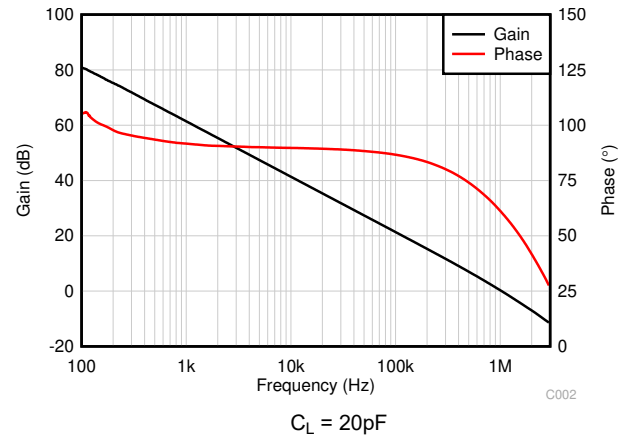


Figure 5-8. Open-Loop Gain and Phase vs Frequency, New Die

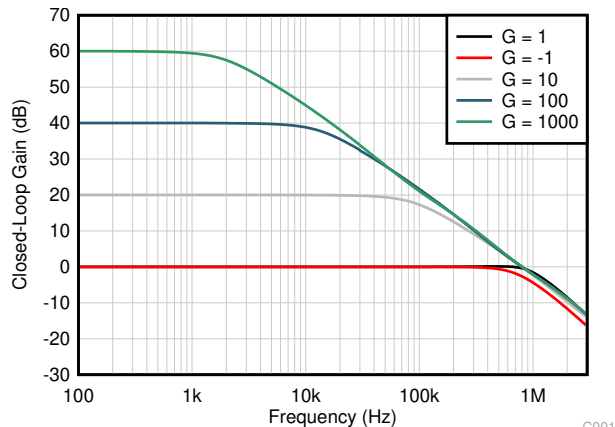


Figure 5-9. Closed-Loop Gain vs Frequency, New Die

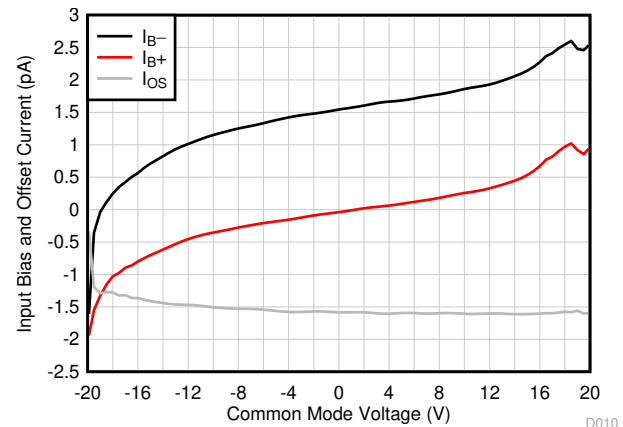


Figure 5-10. Input Bias Current vs Common-Mode Voltage, New Die

5.8 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $R_{\text{LOAD}} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{pF}$ (unless otherwise noted)

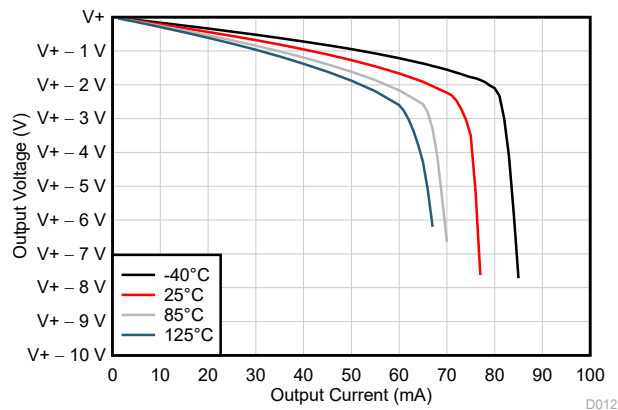


Figure 5-11. Output Voltage Swing vs Output Current (Sourcing), New Die

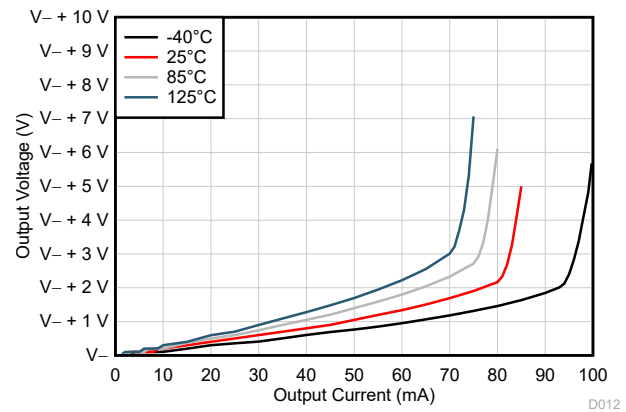


Figure 5-12. Output Voltage Swing vs Output Current (Sinking), New Die

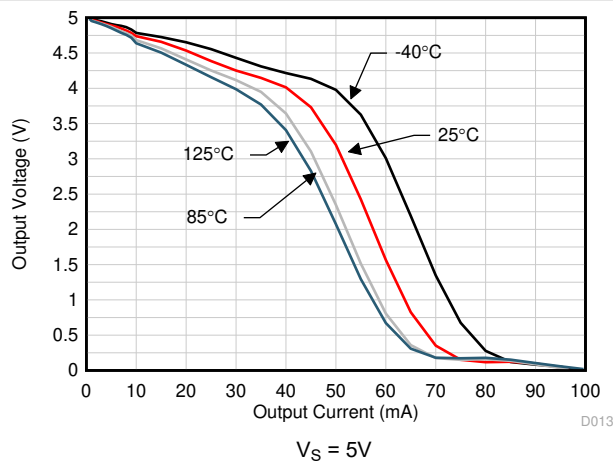


Figure 5-13. Output Voltage Swing vs Output Current (Sourcing), New Die

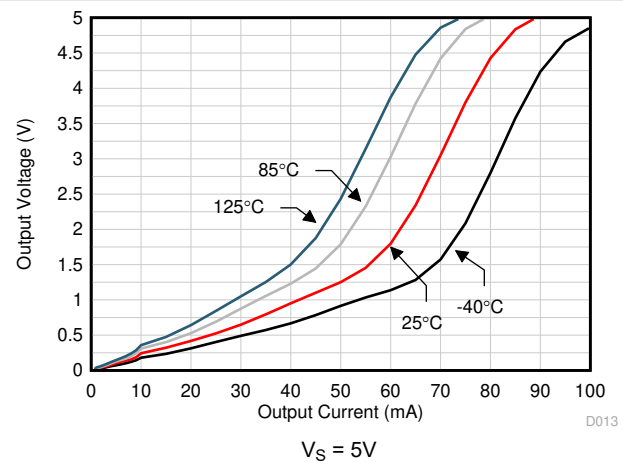


Figure 5-14. Output Voltage Swing vs Output Current (Sinking), New Die

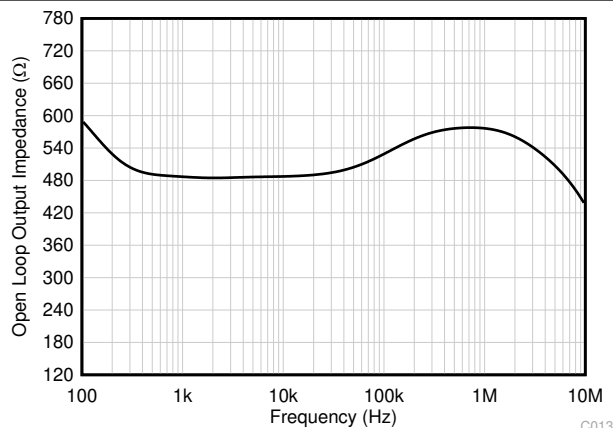


Figure 5-15. Open-Loop Output Impedance vs Frequency, New Die

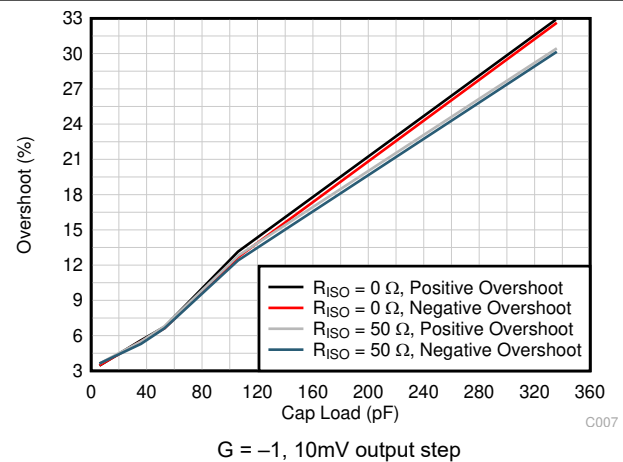


Figure 5-16. Small-Signal Overshoot vs Capacitive Load, New Die

5.8 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $R_{\text{LOAD}} = 10\text{k}\Omega$ connected to $V_S / 2$, and $C_L = 10\text{pF}$ (unless otherwise noted)

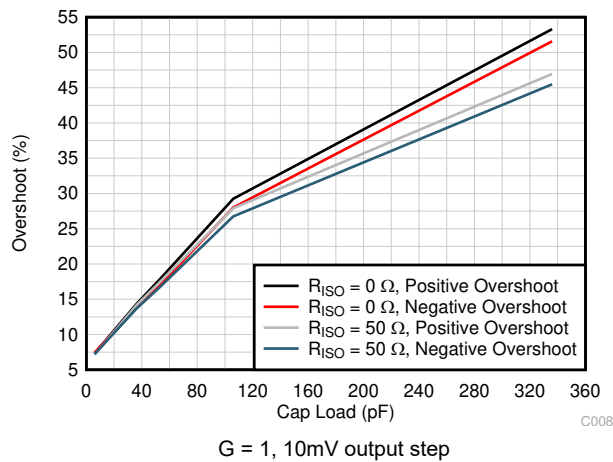


Figure 5-17. Small-Signal Overshoot vs Capacitive Load, New Die

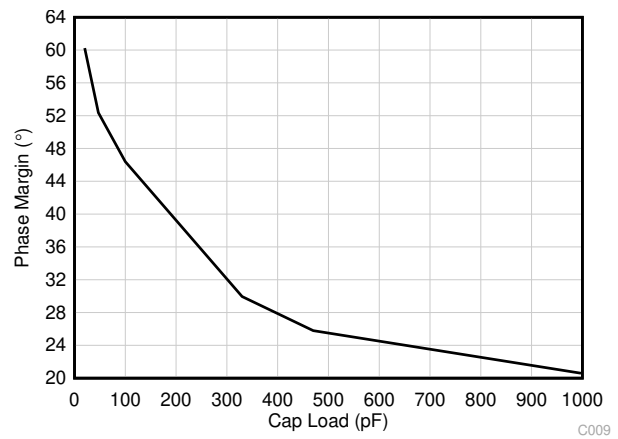


Figure 5-18. Phase Margin vs Capacitive Load, New Die

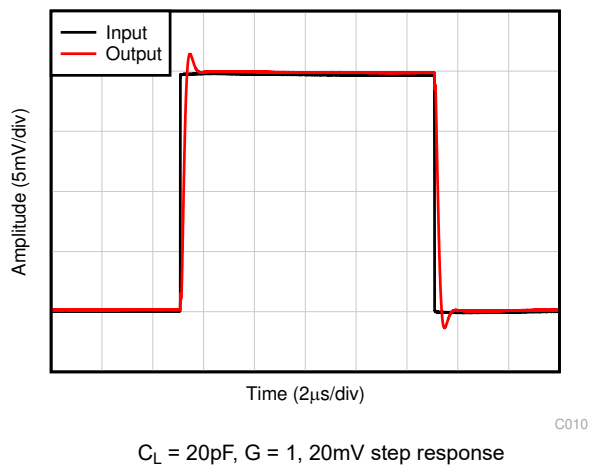


Figure 5-19. Small-Signal Step Response, New Die

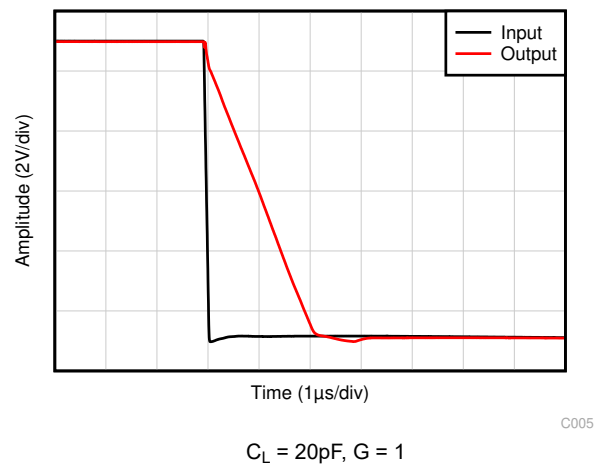


Figure 5-20. Large-Signal Step Response (Falling), New Die

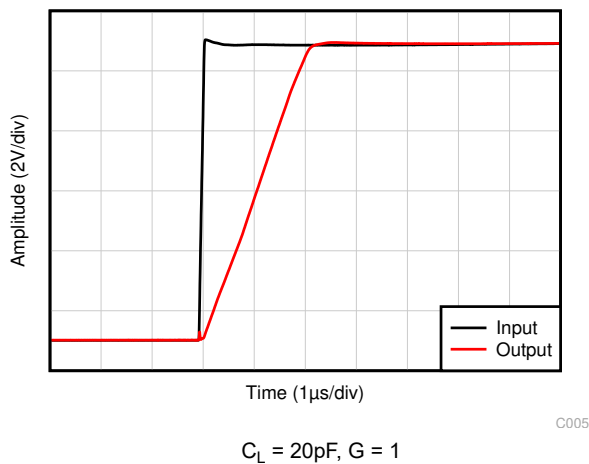


Figure 5-21. Large-Signal Step Response (Rising), New Die

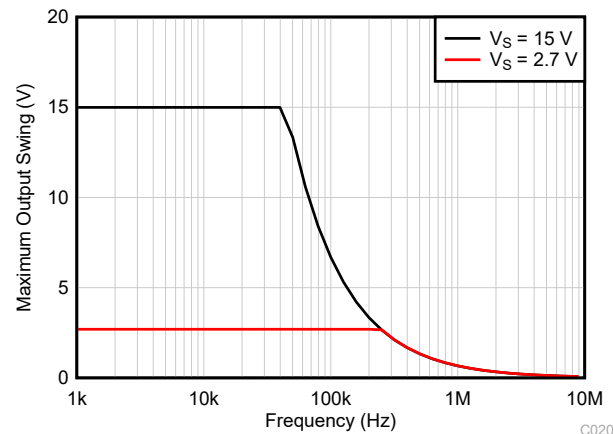


Figure 5-22. Maximum Output Voltage vs Frequency, New Die

5.9 Old vs New Die Comparison

As of the publication of revision H of this data sheet, Texas Instruments has moved manufacturing of the die for TL343 to a modern fabrication site. The two different die are referred to in this document as “old” (previous fabrication site) and “new” die. The die origin can be separated from the “Chip Source Origin” (CSO) parameter in the shipping information. The old die CSO is “SHE”, for the new die CSO is “RFB”. The old die information is maintained in this data sheet for comparison purposes, but all new manufacturing has moved to the new die.

6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

6.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2005) to Revision H (September 2026)	Page
• Deleted Internal frequency compensation from Features section.....	1
• Added Applications section.....	1
• Updated ordering information table from old to new format.....	1
• Deleted sample schematic diagram.....	1
• Updated Absolute Maximum Ratings.....	4
• Added ESD Ratings section.....	4
• Added Thermal Information section.....	4
• Changed Input offset voltage TYP value from 2mV to $\pm 0.3\text{mV}$ and test conditions.....	5
• Changed Temperature coefficient of input offset voltage TYP value from $10\mu\text{V}/^\circ\text{C}$ to $0.6\mu\text{V}/^\circ\text{C}$ and deleted test conditions.....	5
• Changed Input offset current TYP value from $\pm 30\text{nA}$ to $\pm 0.005\text{nA}$ and deleted test conditions and deleted Full range row.....	5
• Deleted Temperature coefficient of input offset current.....	5
• Changed Input bias current from -200nA to $\pm 0.01\text{nA}$ and deleted test conditions and deleted Full range row.....	5
• Changed Common-mode input voltage range MIN value from $V_{\text{CC-}}$ to 13 to (V-) to 13 and TYP value from $V_{\text{CC-}}$ to 13.5 to (V-) - 0.2 to (V+) + 0.2.....	5
• Changed Peak output-voltage swing typical voltage for $R_L = 10\text{k}\Omega$ from $\pm 13.5\text{V}$ to $\pm 14.95\text{V}$ and for $R_L = 2\text{k}\Omega$ from $\pm 13\text{V}$ to $\pm 14.8\text{V}$	5

• Changed Large-signal differential voltage amplification at 25°C minimum value from 20V/mV to 86V/mV and typical value from 200V/mV to 145V/mV.	5
• Changed Large-signal differential voltage amplification at Full range minimum value from 15V/mV to 83V/mV	5
• Changed Maximum-output-swing bandwidth typical value from 9kHz to 40kHz and test condition of $R_L = 2k\Omega$ to $R_L = 10k\Omega$	5
• Changed Phase margin test condition from $C_L = 200pF$ to $C_L = 80pF$	5
• Changed Input resistance typical value from 1M Ω to 540G Ω and deleted Min and Max values and test condition.....	5
• Changed Output resistance typical value from 75 Ω to 575 Ω and changed test condition from $f = 20Hz$ to $f = 1MHz$	5
• Changed Common-mode rejection ratio typical value from 90dB to 115dB.....	5
• Changed Supply-voltage sensitivity typical value from 30 $\mu V/V$ to 0.75 $\mu V/V$	5
• Changed Short-circuit output current TYP value from 30mA to 80mA.....	5
• Deleted Short-circuit output current MAX value.....	5
• Changed Total supply current TYP value from 0.7mA to 0.13mA and changed test conditions.....	5
• Deleted Electrical Characteristics table notes.....	5
• Changed Input offset voltage typical value from 2mV to 0.3mV.....	5
• Changed Input offset current typical value from 30nA to 0.005nA.....	5
• Changed Input bias current typical value from -200nA to 0.01nA.....	5
• Changed Peak output voltage swing typical value from 3.5V to 4.8V.....	5
• Changed Large-signal differential voltage amplification minimum value from 20V/mV to 86db and typical value from 200V/mV to 118db.....	5
• Changed Supply current typical value from 0.7mA to 0.13mA.....	5
• Changed Slew rate at unity gain typical value from 1V/ μs to 4.5V/ μs and updated test conditions.....	6
• Changed Rise time to Settling time and typical value from 0.35 μs to 2 μs and updated test conditions.....	6
• Deleted Fall time.....	6
• Deleted Overshoot factor.....	6
• Changed Crossover distortion to Total Harmonic Distortion + Noise and typical value from 1% to 0.002% and updated test conditions.....	6
• Deleted Parameter Measurement Information section.....	6
• Updated <i>Typical Characteristics</i> section as per New Die characteristics.....	7
• Added <i>Old vs New Die Comparison</i> topic.....	11

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL343IDBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(T41J, T4IG, T4IJ, T4IL, T4IS)
TL343IDBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(T41J, T4IG, T4IJ, T4IL, T4IS)
TL343IDBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	(T4IG, T4IJ, T4IL, T4IU)

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL343IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL343IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

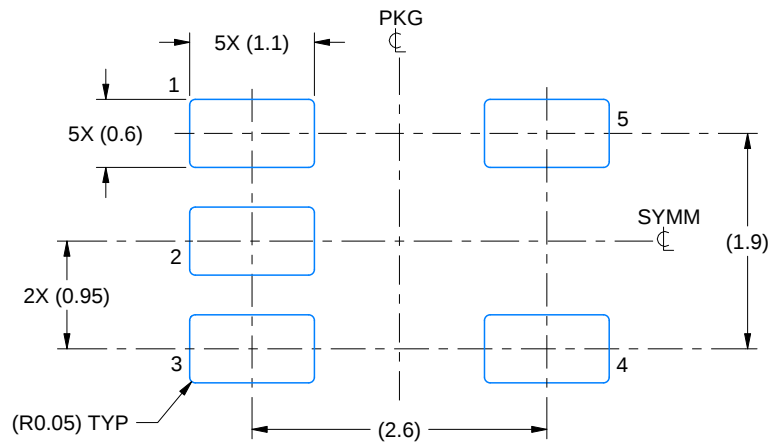
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3431DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL3431DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

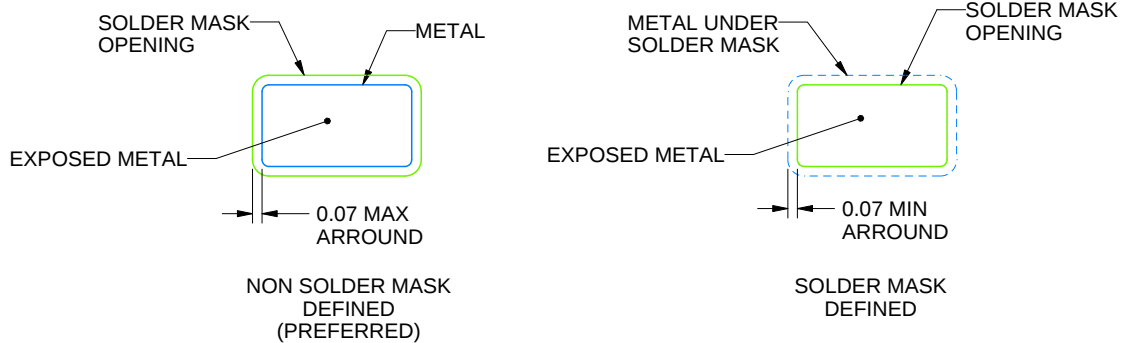
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

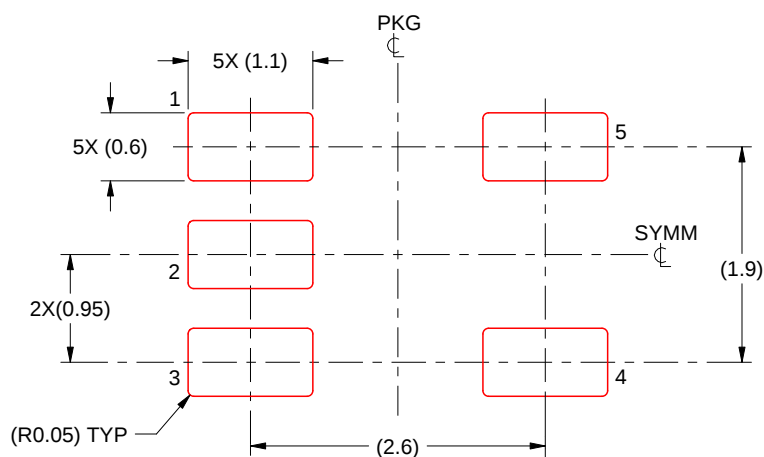
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025