

## TLC2274AM-MIL Advanced LinCMOS Rail-to-Rail Operational Amplifier

### 1 Features

- Output Swing Includes Both Supply Rails
- Low Noise:  $9 \text{ nV}/\sqrt{\text{Hz}}$  Typical at  $f = 1 \text{ kHz}$
- Low-Input Bias Current:  $1\text{-pA}$  Typical
- Fully-Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth:  $2.2\text{-MHz}$  Typical
- High Slew Rate:  $3.6\text{-V}/\mu\text{s}$  Typical
- Low Input Offset Voltage:  $2.5 \text{ mV}$  Maximum at  $T_A = 25^\circ\text{C}$
- Macromodel Included
- Performance Upgrades for the TLC272 and TLC274
- Available in Q-Temp Automotive

### 2 Applications

- White Goods (Refrigerators, Washing Machines)
- Hand-held Monitoring Systems
- Configuration Control and Print Support
- Transducer Interfaces
- Battery-Powered Applications

### 3 Description

The TLC2274AM-MIL device is a quadruple operational amplifier from Texas Instruments. The device exhibits rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC2274AM-MIL device offers 2 MHz of bandwidth and  $3 \text{ V}/\mu\text{s}$  of slew rate for higher-speed applications. The device offers comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC2274AM-MIL device has a noise voltage of  $9 \text{ nV}/\sqrt{\text{Hz}}$ , two times lower than competitive solutions.

The TLC2274AM-MIL device, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources such as piezoelectric transducers. Because of the micropower dissipation levels, the device works well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this device a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC2274AM-MIL device is available with a maximum input offset voltage of  $950 \mu\text{V}$ . This device is fully characterized at 5 V and  $\pm 5 \text{ V}$ .

The TLC2274AM-MIL device also makes a great upgrade to the TLC272 in standard designs, offering increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows the device to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices.

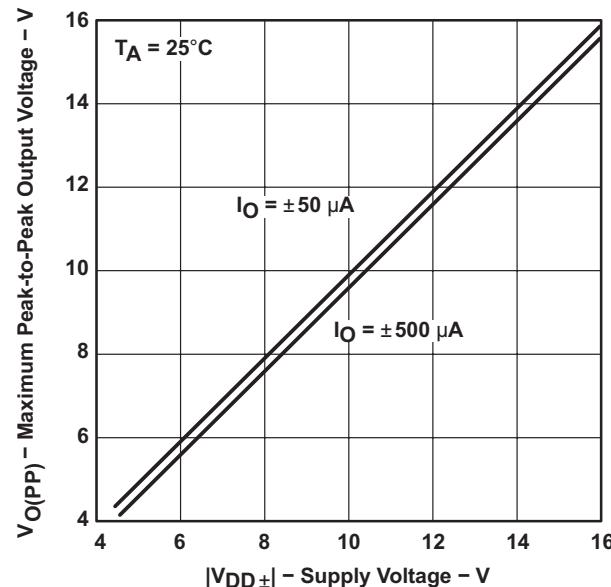
If the design requires single amplifiers, see the TLV2211, TLV2221 and TLV2231 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC2274AM-MIL	SOIC (14)	$3,91 \text{ mm} \times 8,65 \text{ mm}$
	CDIP (14)	$6,67 \text{ mm} \times 19,56 \text{ mm}$
	LCCC (20)	$8,89 \text{ mm} \times 8,89 \text{ mm}$
	CFP (14)	$6,35 \text{ mm} \times 19,30 \text{ mm}$

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Maximum Peak-to-Peak Output Voltage vs Supply Voltage



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

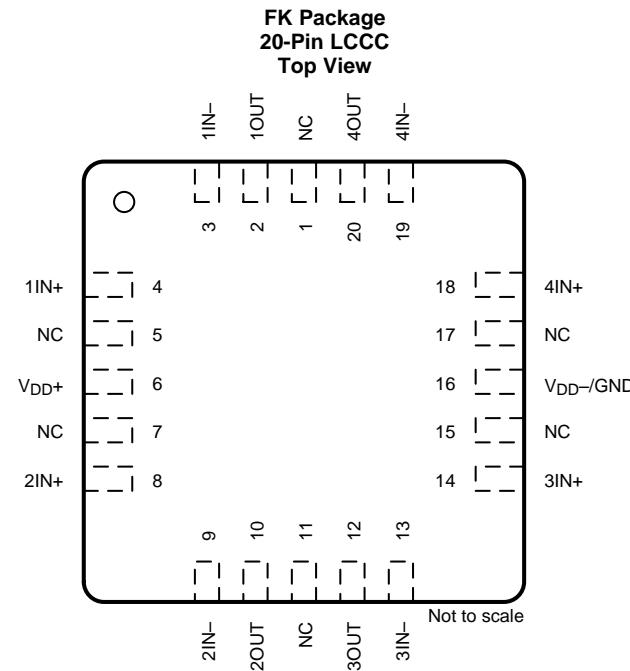
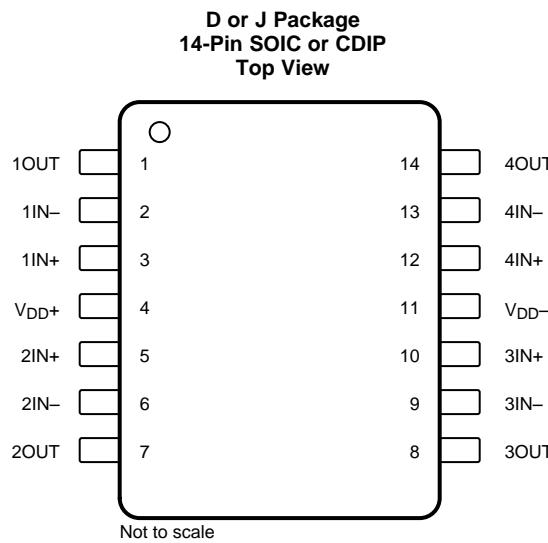
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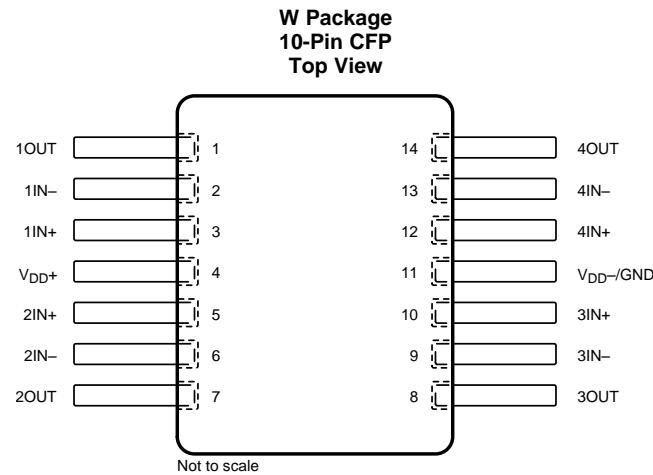
## 4 Revision History

DATE	REVISION	NOTE
June 2017	*	Initial release

## 5 Pin Configuration and Functions



NC – No internal connection



NC – No internal connection

## Pin Functions

NAME	PIN		I/O	DESCRIPTION		
	NO.					
	D, J, N, or W	FK				
1IN+	3	4	I	Non-inverting input, Channel 1		
1IN-	2	3	I	Inverting input, Channel 1		
1OUT	1	2	O	Output, Channel 1		
2IN+	5	8	I	Non-inverting input, Channel 2		
2IN-	6	9	I	Inverting input, Channel 2		
2OUT	7	10	O	Output, Channel 2		
3IN+	10	14	I	Non-inverting input, Channel 3		
3IN-	9	13	I	Inverting input, Channel 3		
3OUT	8	12	O	Output, Channel 3		
4IN+	12	18	I	Non-inverting input, Channel 4		
4IN-	13	19	I	Inverting input, Channel 4		
4OUT	14	20	O	Output, Channel 4		
V <sub>DD</sub> +	4	6	—	Positive (highest) supply		
V <sub>DD</sub> -	11	16	—	Negative (lowest) supply		
V <sub>DD</sub> -/GND	—	—	—	Negative (lowest) supply		
NC	—	1, 5, 7, 11, 15, 17	—	No connection		

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, $V_{DD+}$ <sup>(2)</sup>		8	V
$V_{DD-}$ <sup>(2)</sup>		-8	V
Differential input voltage, $V_{ID}$ <sup>(3)</sup>		±16	V
Input voltage, $V_I$ (any input) <sup>(2)</sup>	$V_{DD-} - 0.3$	$V_{DD+}$	V
Input current, $I_I$ (any input)		±5	mA
Output current, $I_O$		±50	mA
Total current into $V_{DD+}$		±50	mA
Total current out of $V_{DD-}$		±50	mA
Duration of short-circuit current at (or below) 25°C <sup>(4)</sup>	Unlimited		
Operating ambient temperature range, $T_A$	-55	125	
Storage temperature, $T_{stg}$	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between  $V_{DD+}$  and  $V_{DD-}$ .
- (3) Differential voltages are at  $IN+$  with respect to  $IN-$ . Excessive current will flow if input is brought below  $V_{DD-} - 0.3$  V.
- (4) The output may be shorted to either supply. Temperature or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	Devices in D packages	$\pm 2000$
	Charged-device model (CDM), per AEC Q100-011	Devices in D packages	$\pm 1000$

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{DD\pm}$	Supply voltage	$\pm 2.2$	$\pm 8$	V
$V_I$	Input voltage	$V_{DD-}$	$V_{DD+} - 1.5$	V
$V_{IC}$	Common-mode input voltage	$V_{DD-}$	$V_{DD+} - 1.5$	V
$T_A$	Operating ambient temperature	-55	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TLC2274AM-MIL					UNIT
	D (SOIC)	J (CDIP)	FK (LCCC)	N (PDIP)	W (CFP)	
	14-PIN	14-PIN	20-PIN	14-PIN	14-PIN	
$R_{\theta,JA}$	Junction-to-ambient thermal resistance <sup>(2)(3)</sup>	115.6	—	—	—	°C/W
$R_{\theta,JC(\text{top})}$	Junction-to-case (top) thermal resistance <sup>(2)(3)</sup>	61.8	16.2	18	121.3	°C/W
$R_{\theta,JB}$	Junction-to-board thermal resistance	55.9	—	—	—	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	14.3	—	—	—	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	55.4	—	—	—	°C/W
$R_{\theta,JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	—	—	—	8.68	°C/W

- (1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).
- (2) Maximum power dissipation is a function of  $T_{J(\text{max})}$ ,  $R_{\theta,JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(\text{max})} - T_A) / R_{\theta,JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

## 6.5 Electrical Characteristics $V_{DD} = 5$ V

at specified ambient temperature,  $V_{DD} = 5$  V;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage	$V_{IC} = 0$ V, $V_{DD\pm} = \pm 2.5$ V, $V_O = 0$ V, $R_S = 50$ $\Omega$		$T_A = 25^\circ\text{C}$	300	950	$\mu\text{V}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	1500			
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{IC} = 0$ V, $V_{DD\pm} = \pm 2.5$ V, $V_O = 0$ V, $R_S = 50$ $\Omega$		2			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift <sup>(1)</sup>		$V_{IC} = 0$ V, $V_{DD\pm} = \pm 2.5$ V, $V_O = 0$ V, $R_S = 50$ $\Omega$		0.002			$\mu\text{V}/\text{mo}$	
$I_{IO}$	Input offset current	$V_{IC} = 0$ V, $V_{DD\pm} = \pm 2.5$ V, $V_O = 0$ V, $R_S = 50$ $\Omega$		$T_A = 25^\circ\text{C}$	0.5	60	$\text{pA}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	800			
$I_{IB}$	Input bias current	$V_{IC} = 0$ V, $V_{DD\pm} = \pm 2.5$ V, $V_O = 0$ V, $R_S = 50$ $\Omega$		$T_A = 25^\circ\text{C}$	1	60	$\text{pA}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	800			
$V_{ICR}$	Common-mode input voltage	$R_S = 50$ $\Omega$ ; $ V_{IO}  \leq 5$ mV		$T_A = 25^\circ\text{C}$	-0.3	2.5	4	$\text{V}$
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	0	2.5	3.5	
$V_{OH}$	High-level output voltage	$I_{OH} = -20$ $\mu\text{A}$		4.99			$\text{V}$	
		$I_{OH} = -200$ $\mu\text{A}$		$T_A = 25^\circ\text{C}$	4.85	4.93		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	4.85			
		$I_{OH} = -1$ mA		$T_A = 25^\circ\text{C}$	4.25	4.65		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	4.25			
$V_{OL}$	Low-level output voltage	$I_{OL} = 50$ $\mu\text{A}$		0.01			$\text{V}$	
		$I_{OL} = 500$ $\mu\text{A}$		$T_A = 25^\circ\text{C}$	0.09	0.15		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	0.15			
		$I_{OL} = 5$ mA		$T_A = 25^\circ\text{C}$	0.9	1.5		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	1.5			
$A_{VD}$	Large-signal differential voltage amplification	$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V, $R_L = 10$ k $\Omega$ <sup>(2)</sup>		$T_A = 25^\circ\text{C}$	15	35	$\text{V}/\text{mV}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	15			
		$V_{IC} = 2.5$ V, $V_O = 1$ V to 4 V; $R_L = 1$ M $\Omega$ <sup>(2)</sup>		175				
$r_{id}$	Differential input resistance			10 <sup>12</sup>			$\Omega$	
$r_i$	Common-mode input resistance			10 <sup>12</sup>			$\Omega$	
$C_i$	Common-mode input capacitance	$f = 10$ kHz, P package		8			$\text{pF}$	
$Z_o$	Closed-loop output impedance	$f = 1$ MHz, $A_V = 10$		140			$\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = 0$ V to 2.7 V, $V_O = 2.5$ V, $R_S = 50$ $\Omega$		$T_A = 25^\circ\text{C}$	70	75	$\text{dB}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	70			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD} = 4.4$ V to 16 V, $V_{IC} = V_{DD} / 2$ , no load		$T_A = 25^\circ\text{C}$	80	95	$\text{dB}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	80			
$I_{DD}$	Supply current	$V_O = 2.5$ V, no load		$T_A = 25^\circ\text{C}$	4.4	6	$\text{mA}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	3			
SR	Slew rate at unity gain	$V_O = 0.5$ V to 2.5 V, $R_L = 10$ k $\Omega$ <sup>(2)</sup> , $C_L = 100$ pF <sup>(2)</sup>		$T_A = 25^\circ\text{C}$	2.3	3.6	$\text{V}/\mu\text{s}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	1.7			
$V_n$	Equivalent input noise voltage	$f = 10$ Hz		50			$\text{nV}/\sqrt{\text{Hz}}$	
		$f = 1$ kHz		9				
$V_{NPP}$	Peak-to-peak equivalent input noise voltage	$f = 0.1$ Hz to 1 Hz		1			$\mu\text{V}$	
		$f = 0.1$ Hz to 10 Hz		1.4				
$I_n$	Equivalent input noise current			0.6			$\text{fA}/\sqrt{\text{Hz}}$	
THD+N	Total harmonic distortion + noise	$V_O = 0.5$ V to 2.5 V, $f = 20$ kHz, $R_L = 10$ k $\Omega$ <sup>(2)</sup>		$A_V = 1$	0.0013%			
				$A_V = 10$	0.004%			
				$A_V = 100$	0.03%			
Gain-bandwidth product		$f = 10$ kHz, $R_L = 10$ k $\Omega$ <sup>(2)</sup> , $C_L = 100$ pF <sup>(2)</sup>		2.18			$\text{MHz}$	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 2$ V, $A_V = 1$ , $R_L = 10$ k $\Omega$ <sup>(2)</sup> , $C_L = 100$ pF <sup>(2)</sup>		1			$\text{MHz}$	
$t_s$	Settling time	$A_V = -1$ , $R_L = 10$ k $\Omega$ <sup>(2)</sup> , Step = 0.5 V to 2.5 V, $C_L = 100$ pF <sup>(2)</sup>		To 0.1%	1.5		$\mu\text{s}$	
				To 0.01%	2.6			

(1) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at  $T_A = 150^\circ\text{C}$  extrapolated to  $T_A = 25^\circ\text{C}$  using the Arrhenius equation and assuming an activation energy of 0.96 eV.

(2) Referenced to 0 V.

## Electrical Characteristics $V_{DD} = 5$ V (continued)

at specified ambient temperature,  $V_{DD} = 5$  V;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\varphi_m$ Phase margin at unity gain	$R_L = 10 \text{ k}\Omega^{(2)}$ , $C_L = 100 \text{ pF}^{(2)}$		50		$^\circ$
Gain margin	$R_L = 10 \text{ k}\Omega^{(2)}$ , $C_L = 100 \text{ pF}^{(2)}$		10		dB

## 6.6 Electrical Characteristics $V_{DD\pm} = \pm 5$ V

at specified ambient temperature,  $V_{DD\pm} = \pm 5$  V;  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
$V_{IO}$	Input offset voltage	$V_{IC} = 0$ V, $V_O = 0$ V, $R_S = 50 \Omega$		$T_A = 25^\circ\text{C}$	300	950	$\mu\text{V}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	1500			
$\alpha_{VIO}$	Temperature coefficient of input offset voltage	$V_{IC} = 0$ V, $V_O = 0$ V, $R_S = 50 \Omega$		2			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift		$V_{IC} = 0$ V, $V_O = 0$ V, $R_S = 50 \Omega$		0.002			$\mu\text{V}/\text{mo}$	
$I_{IO}$	Input offset current	$V_{IC} = 0$ V, $V_O = 0$ V, $R_S = 50 \Omega$		$T_A = 25^\circ\text{C}$	0.5	60	$\text{pA}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	800			
$I_{IB}$	Input bias current	$V_{IC} = 0$ V, $V_O = 0$ V, $R_S = 50 \Omega$		$T_A = 25^\circ\text{C}$	1	60	$\text{pA}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	800			
$V_{ICR}$	Common-mode input voltage	$R_S = 50 \Omega$ ; $ V_{IO}  \leq 5$ mV		$T_A = 25^\circ\text{C}$	-5.3	0	$\text{V}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	-5	0		
$V_{OM+}$	Maximum positive peak output voltage	$I_O = -20 \mu\text{A}$		4.99			$\text{V}$	
		$I_O = -200 \mu\text{A}$		$T_A = 25^\circ\text{C}$	4.85	4.93		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	4.85			
		$I_O = -1 \text{ mA}$		$T_A = 25^\circ\text{C}$	4.25	4.65		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	4.25			
$V_{OM-}$	Maximum negative peak output voltage	$V_{IC} = 0$ V, $I_O = 50 \mu\text{A}$		-4.99			$\text{V}$	
				$T_A = 25^\circ\text{C}$	-4.85	-4.91		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	-4.85			
				$T_A = 25^\circ\text{C}$	-3.5	-4.1		
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	-3.5			
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 4$ V; $R_L = 10 \text{ k}\Omega$		$T_A = 25^\circ\text{C}$	20	50	$\text{V}/\text{mV}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	20			
$V_O = \pm 4$ V; $R_L = 1 \text{ M}\Omega$				300				
$r_{id}$	Differential input resistance			10 <sup>12</sup>			$\Omega$	
$r_i$	Common-mode input resistance			10 <sup>12</sup>			$\Omega$	
$C_i$	Common-mode input capacitance	$f = 10$ kHz, P package		8			$\text{pF}$	
$Z_o$	Closed-loop output impedance	$f = 1$ MHz, $A_V = 10$		130			$\Omega$	
CMRR	Common-mode rejection ratio	$V_{IC} = -5$ V to $2.7$ V, $V_O = 0$ V, $R_S = 50 \Omega$		$T_A = 25^\circ\text{C}$	75	80	$\text{dB}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	75			
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD+} = 2.2$ V to $\pm 8$ V, $V_{IC} = 0$ V, no load		$T_A = 25^\circ\text{C}$	80	95	$\text{dB}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	80			
$I_{DD}$	Supply current	$V_O = 0$ V, no load		$T_A = 25^\circ\text{C}$	4.8	6	$\text{mA}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	6			
SR	Slew rate at unity gain	$V_O = \pm 2.3$ V, $R_L = 10 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$		$T_A = 25^\circ\text{C}$	2.3	3.6	$\text{V}/\mu\text{s}$	
				$T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$	1.7			
$V_n$	Equivalent input noise voltage	$f = 10$ Hz		50			$\text{nV}/\sqrt{\text{Hz}}$	
				9				
$V_{NPP}$	Peak-to-peak equivalent input noise voltage	$f = 0.1$ Hz to $1$ Hz		1			$\mu\text{V}$	
				1.4				
$I_n$	Equivalent input noise current			0.6			$\text{fA}/\sqrt{\text{Hz}}$	
THD+N	Total harmonic distortion + noise	$V_O = \pm 2.3$ , $f = 20$ kHz, $R_L = 10 \text{ k}\Omega$		$A_V = 1$	0.0011%			
				$A_V = 10$	0.004%			
				$A_V = 100$	0.03%			
Gain-bandwidth product		$f = 10$ kHz, $R_L = 10 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$		2.25			$\text{MHz}$	
$B_{OM}$	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6$ V, $A_V = 1$ , $R_L = 10 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$		0.54			$\text{MHz}$	
$t_s$	Settling time	$A_V = -1$ , $R_L = 10 \text{ k}\Omega$ , Step = $-2.3$ V to $2.3$ V, $C_L = 100 \text{ pF}$		To 0.1%	1.5		$\mu\text{s}$	
				To 0.01%	3.2			
$\phi_m$	Phase margin at unity gain	$R_L = 10 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$		52			$^\circ$	
Gain margin		$R_L = 10 \text{ k}\Omega$ , $C_L = 100 \text{ pF}$		10			$\text{dB}$	

## 6.7 Typical Characteristics

**Table 1. Table of Graphs**

			<b>FIGURE<sup>(1)</sup></b>
V <sub>IO</sub>	Input offset voltage	Distribution	1, 2
		vs Common-mode voltage	3, 4
α <sub>VIO</sub>	Input offset voltage temperature coefficient	Distribution	5, 6 <sup>(2)</sup>
I <sub>IB</sub> / I <sub>IO</sub>	Input bias and input offset current	vs Ambient temperature	7 <sup>(2)</sup>
		vs Supply voltage	8
V <sub>I</sub>	Input voltage	vs Ambient temperature	9 <sup>(2)</sup>
		vs Supply voltage	8
V <sub>OH</sub>	High-level output voltage	vs High-level output current	10 <sup>(2)</sup>
V <sub>OL</sub>	Low-level output voltage	vs Low-level output current	11, 12 <sup>(2)</sup>
V <sub>OM+</sub>	Maximum positive peak output voltage	vs Output current	13 <sup>(2)</sup>
V <sub>OM-</sub>	Maximum negative peak output voltage	vs Output current	14 <sup>(2)</sup>
V <sub>O(PP)</sub>	Maximum peak-to-peak output voltage	vs Frequency	15
I <sub>os</sub>	Short-circuit output current	vs Supply voltage	16
		vs Ambient temperature	17 <sup>(2)</sup>
V <sub>O</sub>	Output voltage	vs Differential input voltage	18, 19
AvD	Large-signal differential voltage amplification	vs Load resistance	20
	Large-signal differential voltage amplification and phase margin	vs Frequency	21, 22
	Large-signal differential voltage amplification	vs Ambient temperature	23 <sup>(2)</sup> , 24 <sup>(2)</sup>
z <sub>0</sub>	Output impedance	vs Frequency	25, 26
CMRR	Common-mode rejection ratio	vs Frequency	27
		vs Ambient temperature	28
k <sub>SVR</sub>	Supply-voltage rejection ratio	vs Frequency	29, 30
		vs Ambient temperature	31 <sup>(2)</sup>
I <sub>DD</sub>	Supply current	vs Supply voltage	(2), 32 <sup>(2)</sup>
		vs Ambient temperature	(2), 33 <sup>(2)</sup>
SR	Slew rate	vs Load Capacitance	34
		vs Ambient temperature	35 <sup>(2)</sup>
V <sub>O</sub>	Inverting large-signal pulse response		36, 37
	Voltage-follower large-signal pulse response		38, 39
	Inverting small-signal pulse response		40, 41
	Voltage-follower small-signal pulse response		42, 43
V <sub>n</sub>	Equivalent input noise voltage	vs Frequency	44, 45
	Noise voltage over a 10-second period		46
	Integrated noise voltage	vs Frequency	47
THD+N	Total harmonic distortion + noise	vs Frequency	48
		vs Supply voltage	49
φ <sub>m</sub>	Phase margin	vs Ambient temperature	50 <sup>(2)</sup>
		vs Load capacitance	51
	Gain margin	vs Load capacitance	52

(1) For all graphs where V<sub>DD</sub> = 5 V, all loads are referenced to 2.5 V.

(2) Data at high and low temperatures are applicable only within the rated operating ambient temperature ranges of the various devices.

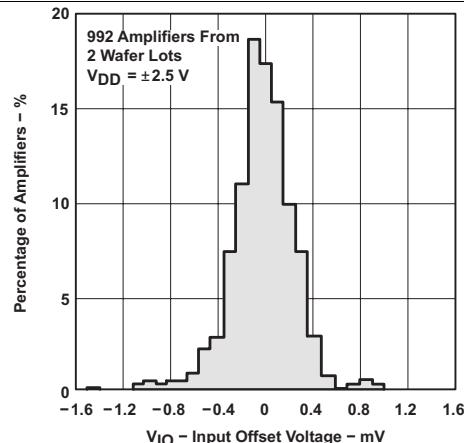


Figure 1. Distribution of Input Offset Voltage

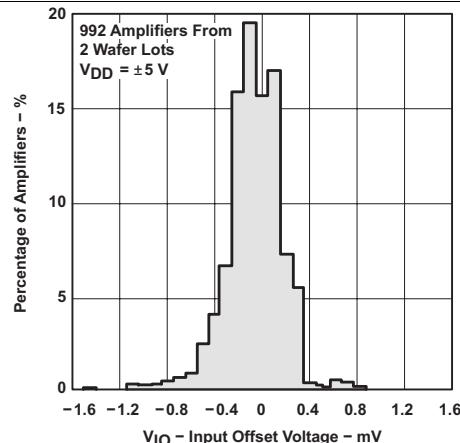


Figure 2. Distribution of Input Offset Voltage

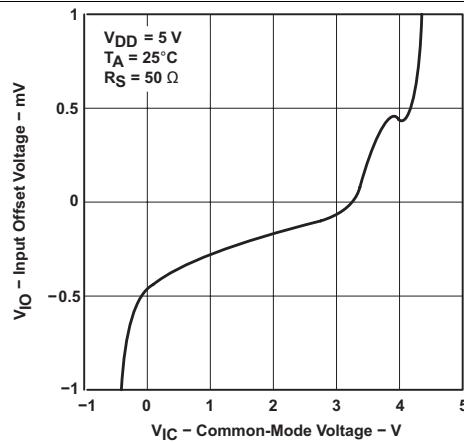


Figure 3. Input Offset Voltage vs Common-Mode Voltage

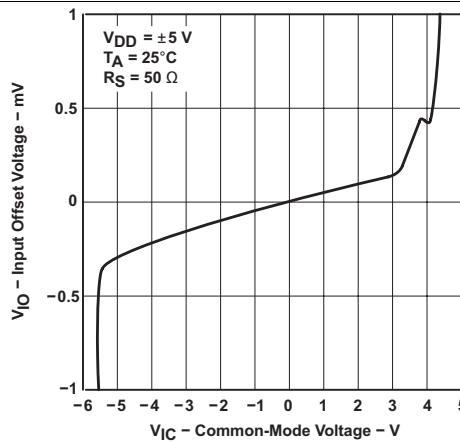


Figure 4. Input Offset Voltage vs Common-Mode Voltage

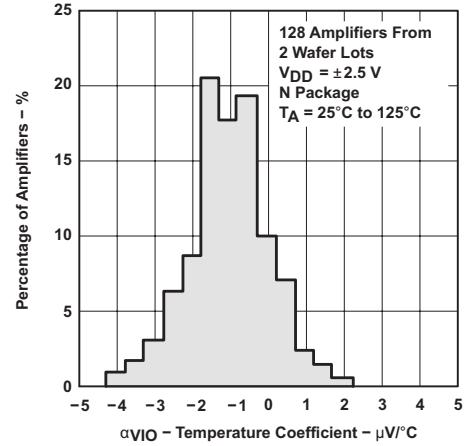


Figure 5. Distribution vs Input-Offset-Voltage Temperature Coefficient

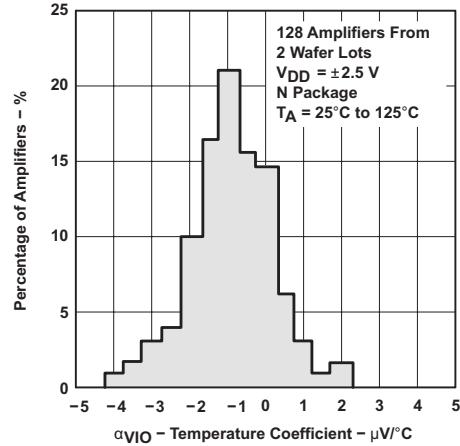
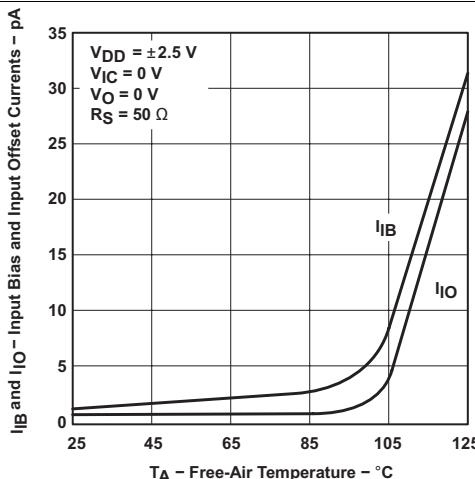
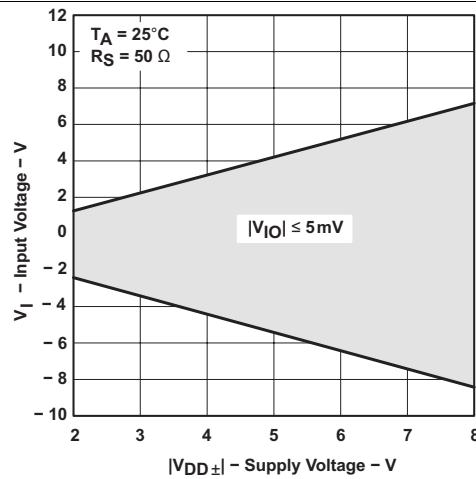


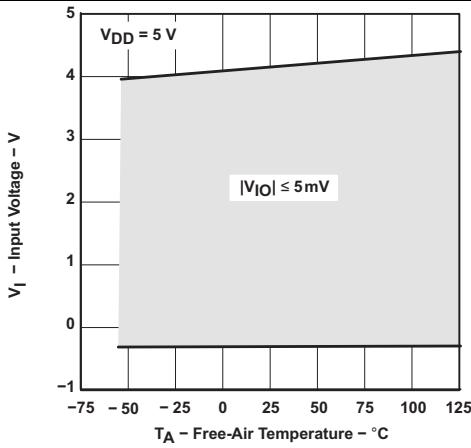
Figure 6. Distribution vs Input-Offset-Voltage Temperature Coefficient



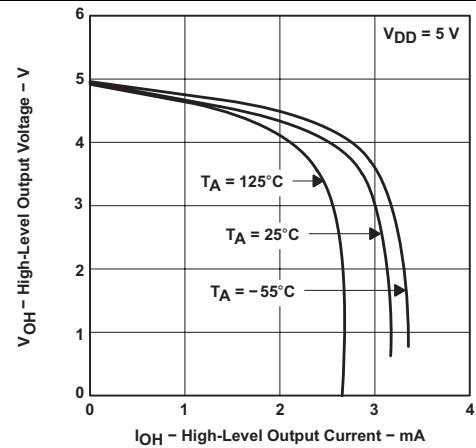
**Figure 7. Input Bias and Input Offset Current vs Ambient Temperature**



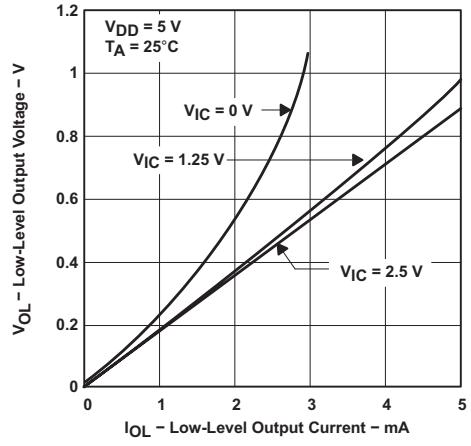
**Figure 8. Input Voltage vs Supply Voltage**



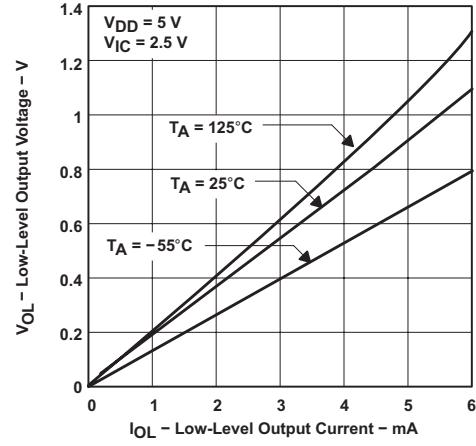
**Figure 9. Input Voltage vs Ambient Temperature**



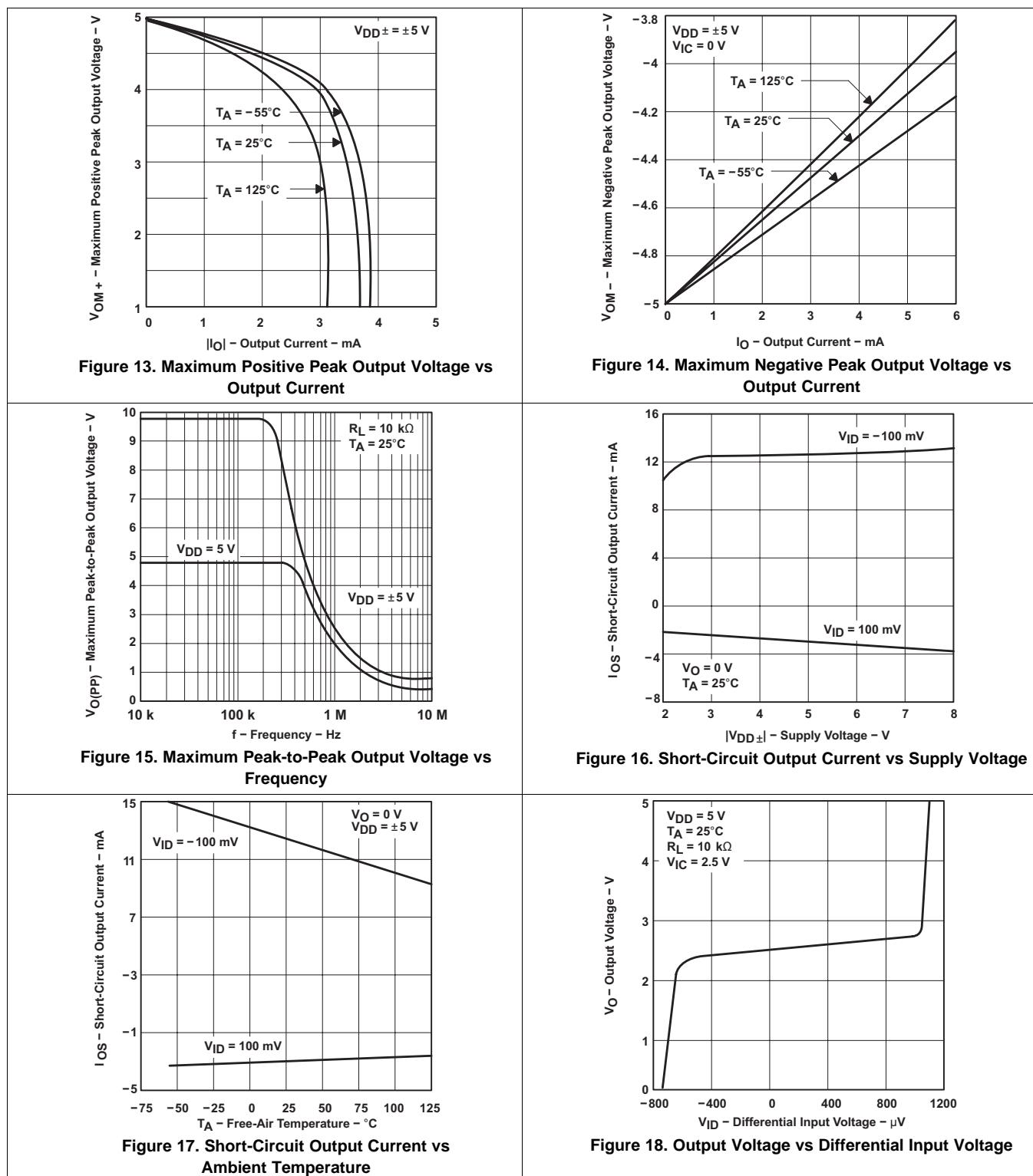
**Figure 10. High-Level Output Voltage vs High-Level Output Current**

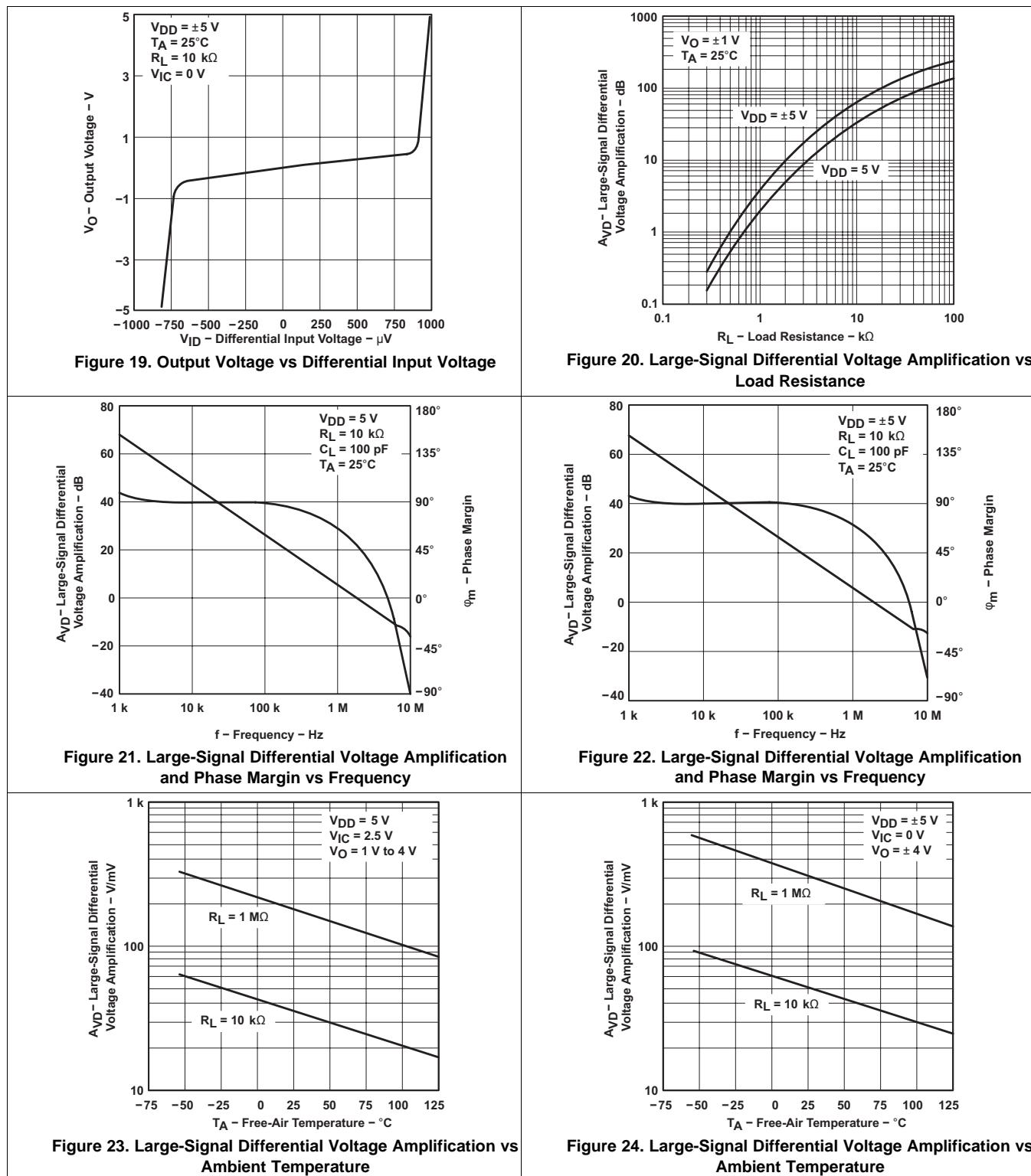


**Figure 11. Low-Level Output Voltage vs Low-Level Output Current**



**Figure 12. Low-Level Output Voltage vs Low-Level Output Current**




**Figure 19. Output Voltage vs Differential Input Voltage**
**Figure 20. Large-Signal Differential Voltage Amplification vs Load Resistance**
**Figure 21. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency**
**Figure 22. Large-Signal Differential Voltage Amplification and Phase Margin vs Frequency**
**Figure 23. Large-Signal Differential Voltage Amplification vs Ambient Temperature**
**Figure 24. Large-Signal Differential Voltage Amplification vs Ambient Temperature**

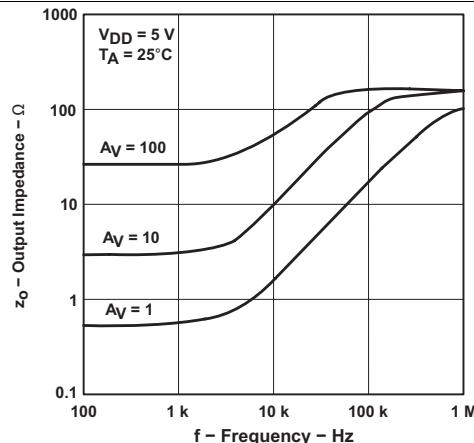


Figure 25. Output Impedance vs Frequency

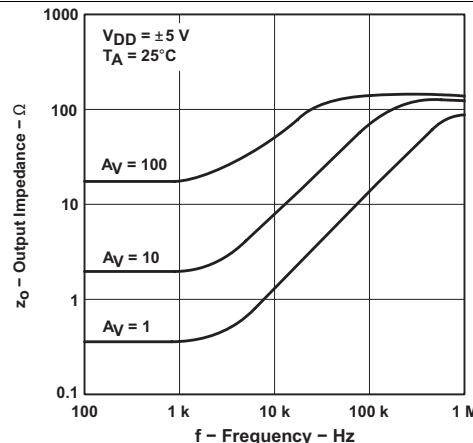


Figure 26. Output Impedance vs Frequency

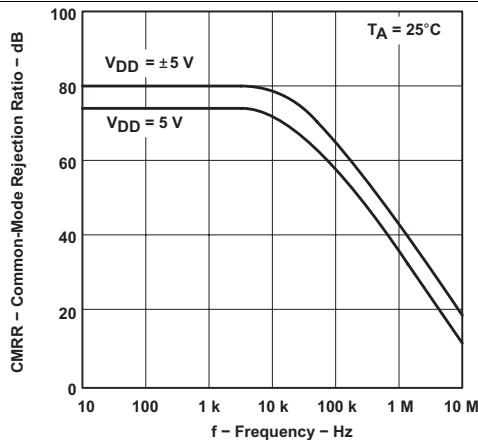


Figure 27. Common-Mode Rejection Ratio vs Frequency

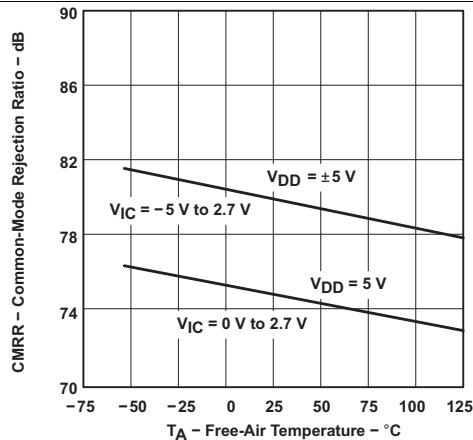


Figure 28. Common-Mode Rejection Ratio vs Ambient Temperature

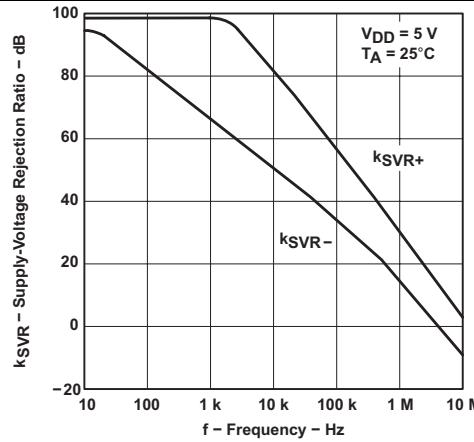


Figure 29. Supply-Voltage Rejection Ratio vs Frequency

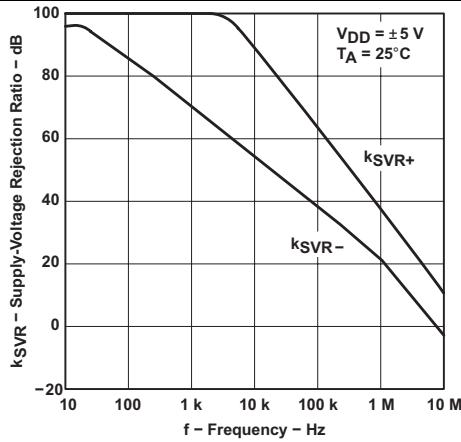
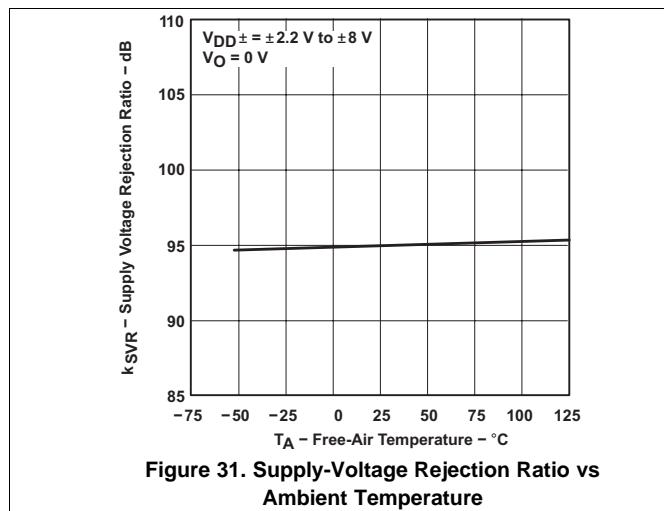
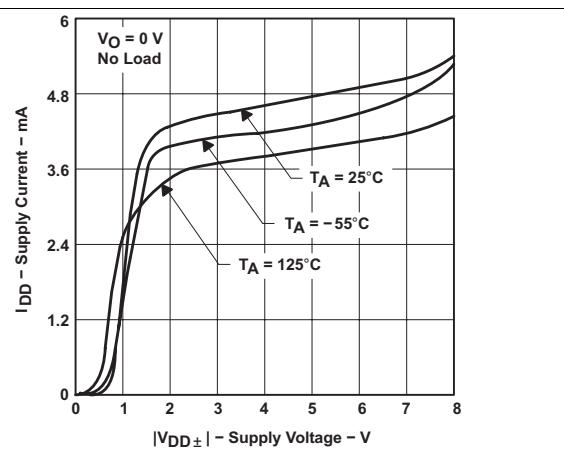


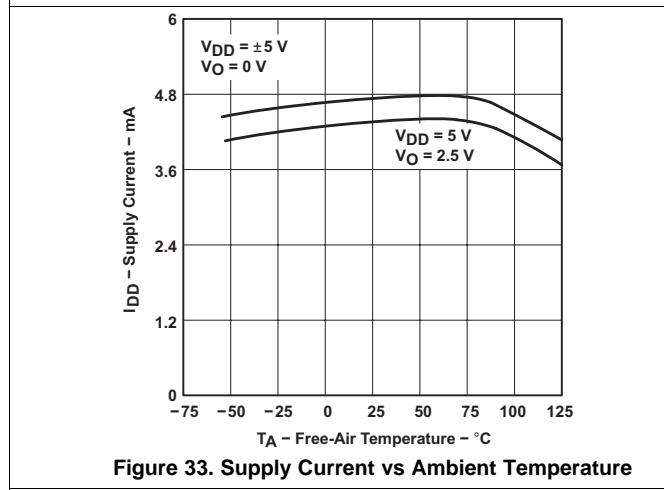
Figure 30. Supply-Voltage Rejection Ratio vs Frequency



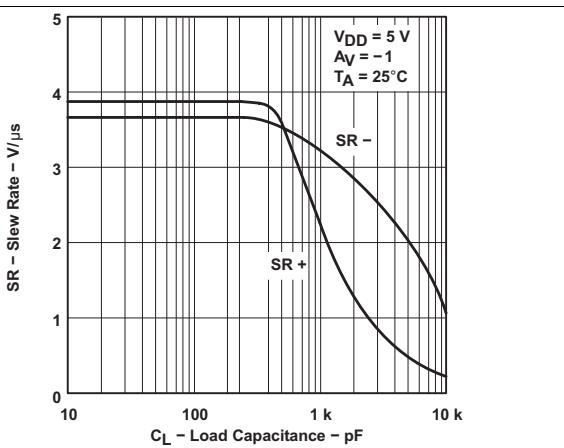
**Figure 31. Supply-Voltage Rejection Ratio vs Ambient Temperature**



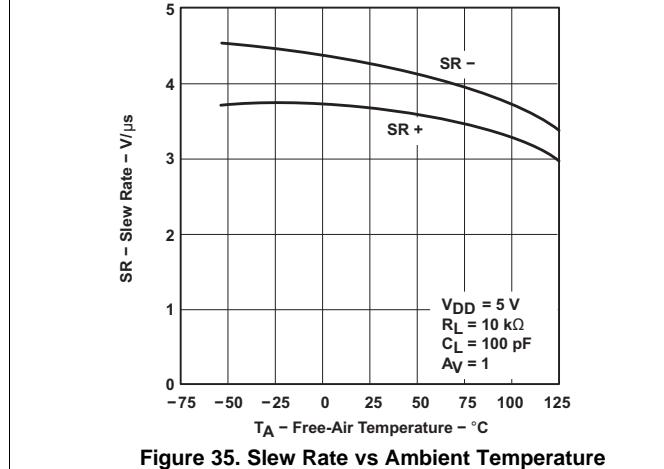
**Figure 32. Supply Current vs Supply Voltage**



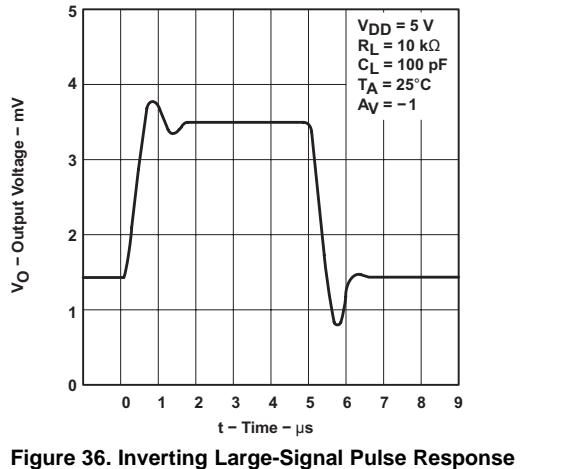
**Figure 33. Supply Current vs Ambient Temperature**



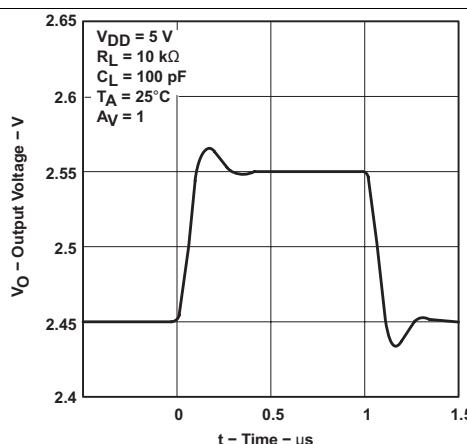
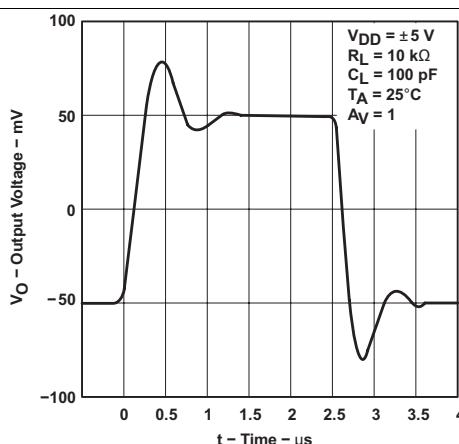
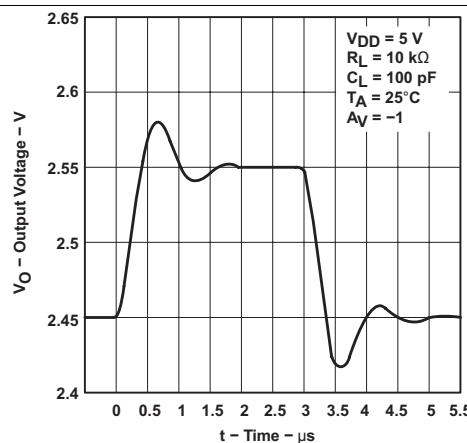
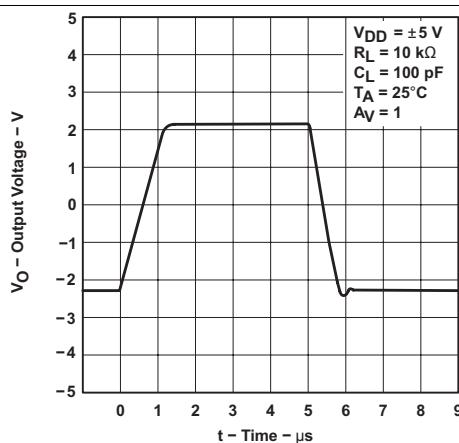
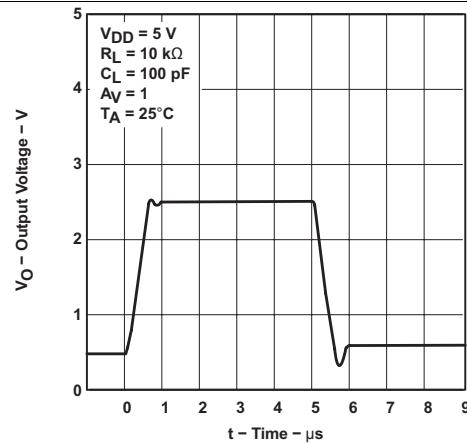
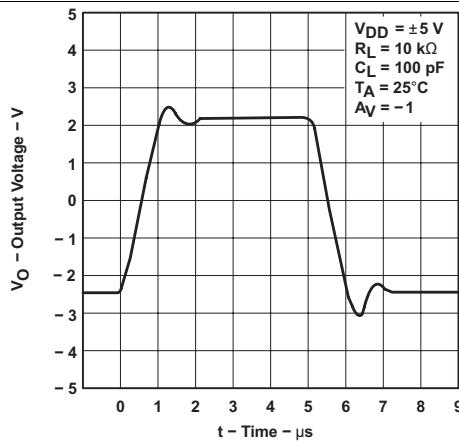
**Figure 34. Slew Rate vs Load Capacitance**

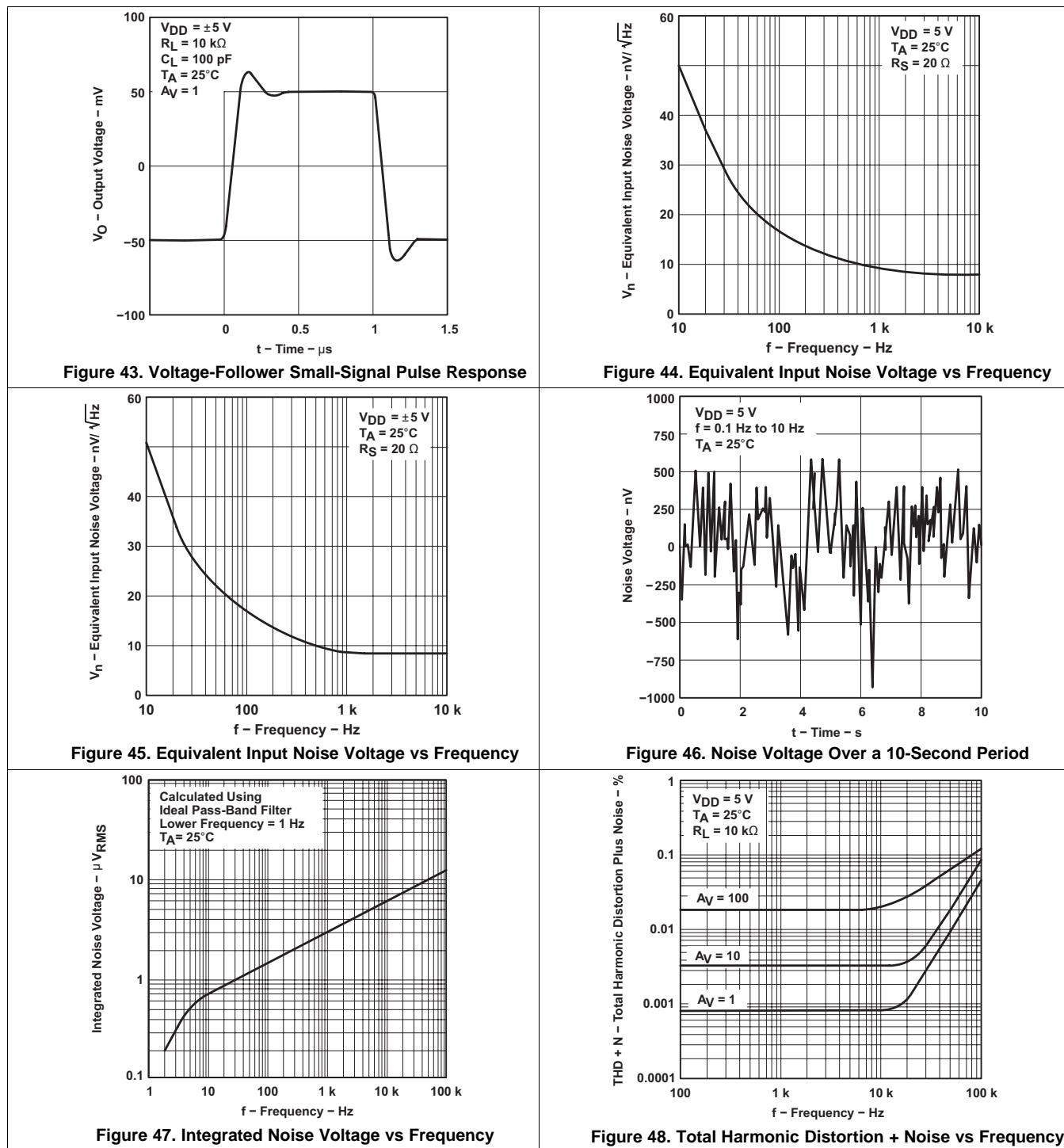


**Figure 35. Slew Rate vs Ambient Temperature**



**Figure 36. Inverting Large-Signal Pulse Response**





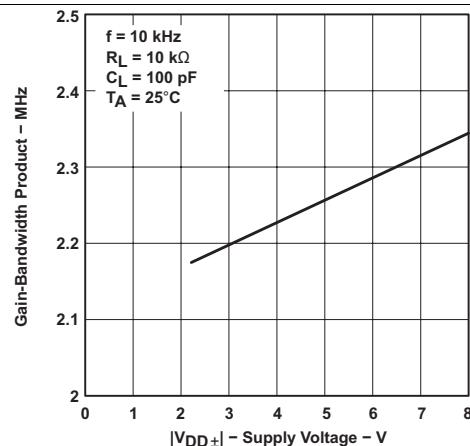


Figure 49. Gain-Bandwidth Product vs Supply Voltage

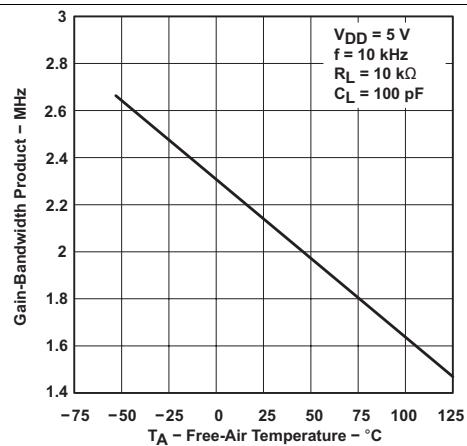


Figure 50. Gain-Bandwidth Product vs Ambient Temperature

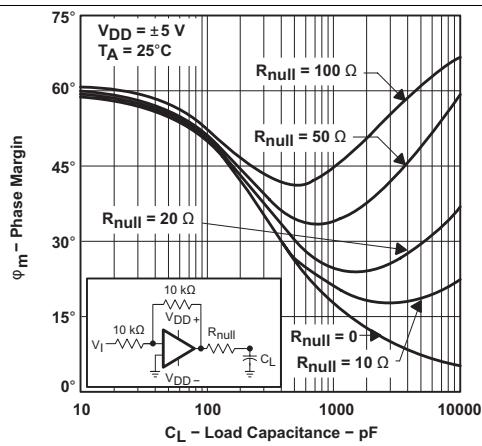


Figure 51. Phase Margin vs Load Capacitance

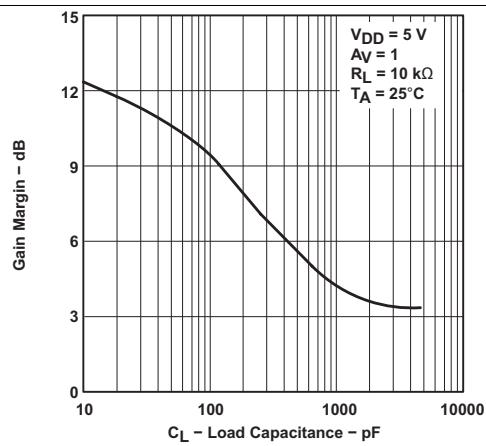


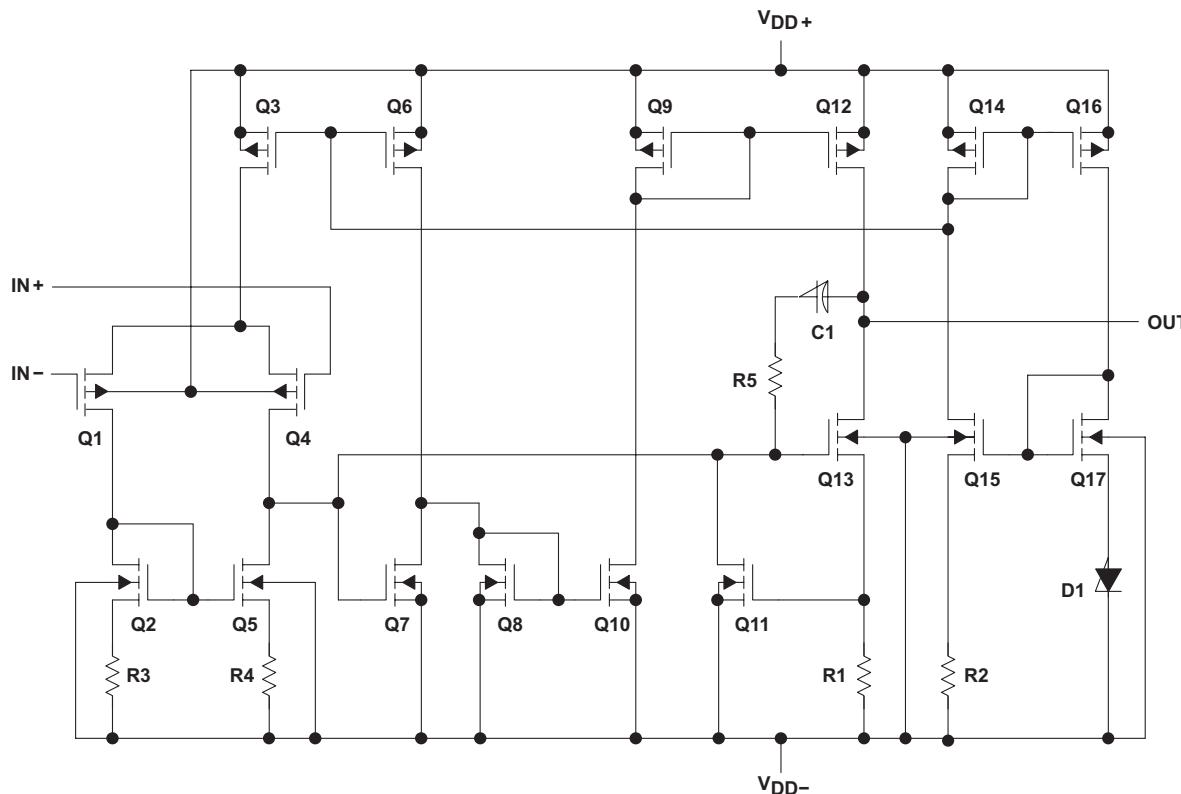
Figure 52. Gain Margin vs Load Capacitance

## 7 Detailed Description

### 7.1 Overview

The TLC2274AM-MIL device is a rail-to-rail output operational amplifier. The device operates from a 4.4-V to 16-V single supply or  $\pm 2.2$ -V to  $\pm 8$ -V dual supply, is unity-gain stable, and is suitable for a wide range of general-purpose applications.

### 7.2 Functional Block Diagram



**Table 2. Device Component Count<sup>(1)</sup>**

COMPONENT	COUNT
Transistors	76
Resistors	52
Diodes	18
Capacitors	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry.

### 7.3 Feature Description

The TLC2274AM-MIL device features 2-MHz bandwidth and voltage noise of  $9 \text{ nV}/\sqrt{\text{Hz}}$  with performance rated from 4.4 V to 16 V across a temperature range ( $-55^\circ\text{C}$  to  $125^\circ\text{C}$ ). LinMOS suits a wide range of audio, automotive, industrial, and instrumentation applications.

### 7.4 Device Functional Modes

The TLC2274AM-MIL device is powered on when the supply is connected. The device may operate with single or dual supply, depending on the application. The device is in its full-performance mode once the supply is above the recommended value.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

#### 8.1.1 Macromodel Information

Macromodel information provided was derived using MicroSim Parts™, the model generation software used with MicroSim PSpice™. The Boyle macromodel<sup>(1)</sup> and subcircuit in Figure 53 were generated using the TLC2274AM-MIL typical electrical and operating characteristics at  $T_A = 25^\circ\text{C}$ . Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

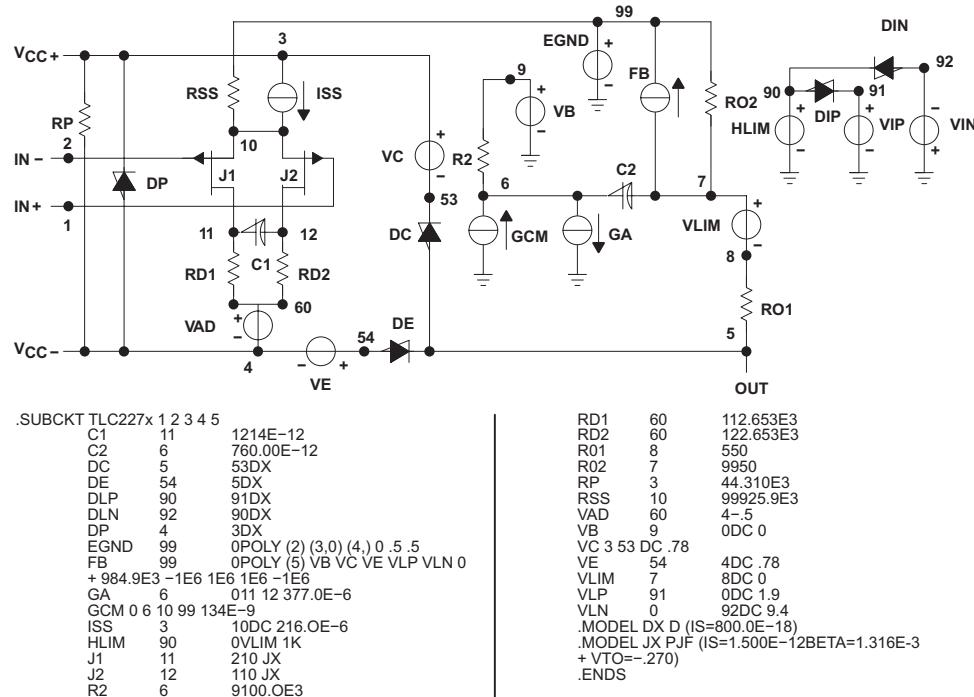
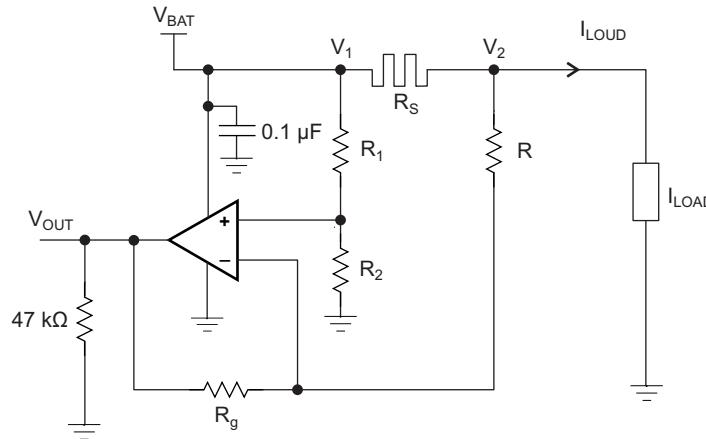


Figure 53. Boyle Macromodel and Subcircuit

(1) Macromodeling of Integrated Circuit Operational Amplifiers, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

## 8.2 Typical Application

### 8.2.1 High-Side Current Monitor



**Figure 54. Equivalent Schematic (Each Amplifier)**

#### 8.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#) as the input parameters.

**Table 3. Design Parameters**

PARAMETER	VALUE
$V_{BAT}$	Battery voltage
$R_{SENSE}$	Sense resistor
$I_{LOAD}$	Load current
Operational amplifier	Set in differential configuration with gain = 10

#### 8.2.1.2 Detailed Design Procedure

This circuit is designed for measuring the high-side current in automotive body control modules with a 12-V battery or similar applications. The operational amplifier is set as differential with an external resistor network.

##### 8.2.1.2.1 Differential Amplifier Equations

[Equation 1](#) and [Equation 2](#) are used to calculate  $V_{OUT}$ .

$$V_{OUT} = \frac{R_g}{R} \left( \frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times \frac{V_1 + V_2}{2} + \frac{1 + \frac{1}{2} \left( \frac{R_1}{R_2} + \frac{R}{R_g} \right)}{1 + \frac{R_1}{R_2}} (V_1 - V_2) \right) \quad (1)$$

$$V_{OUT} = \frac{R_g}{R} \left( \frac{\frac{R}{R_g} - \frac{R_1}{R_2}}{1 + \frac{R_1}{R_2}} \times V_{BAT} + \frac{1 + \frac{1}{2} \left( \frac{R_1}{R_2} + \frac{R}{R_g} \right)}{1 + \frac{R_1}{R_2}} \times R_S \times I_{Load} \right) \quad (2)$$

In an ideal case  $R_1 = R$  and  $R_2 = R_g$ , and  $V_{OUT}$  can then be calculated using [Equation 3](#):

$$V_{OUT} = \frac{R_g}{R} \times R_S \times I_{Load} \quad (3)$$

However, as the resistors have tolerances, they cannot be perfectly matched.

$$\begin{aligned}
 R_1 &= R \pm \Delta R_1 \\
 R_2 &= R_2 \pm \Delta R_2 \\
 R &= R \pm \Delta R \\
 R_g &= R_g \pm \Delta R_g \\
 \text{Tol} &= \frac{\Delta R}{R}
 \end{aligned} \tag{4}$$

By developing the equations and neglecting the second order, the worst case is when the tolerances add up. This is shown by [Equation 5](#).

$$V_{\text{OUT}} = \pm (4 \text{ Tol}) \frac{R_g}{R + R_g} \times V_{\text{BAT}} + \left( 1 \pm 2 \text{ Tol} \left( 1 + \frac{2R}{R + R_g} \right) \right) \frac{R_g}{R} \times R_s \times I_{\text{LOAD}}$$

where

- Tol = 0.01 for 1%
- Tol = 0.001 for 0.1%

5

If the resistors are perfectly matched, then Tol = 0 and  $V_{\text{OUT}}$  is calculated using [Equation 6](#).

$$V_{\text{OUT}} = \frac{R_g}{R} \times R_s \times I_{\text{LOAD}} \tag{6}$$

The highest error is from the common mode, as shown in [Equation 7](#).

$$4 (\text{Tol}) \frac{R_g}{R + R_g} \times V_{\text{BAT}} \tag{7}$$

Gain of 10,  $R_g / R = 10$ , and Tol = 1%:

$$\text{Common mode error} = ((4 \times 0.01) / 1.1) \times 12 \text{ V} = 0.436 \text{ V}$$

Gain of 10 and Tol = 0.1%:

$$\text{Common mode error} = 43.6 \text{ mV}$$

The resistors were chosen from 2% batches.

$$R_1 \text{ and } R \text{ } 12 \text{ k}\Omega$$

$$R_2 \text{ and } R_g \text{ } 120 \text{ k}\Omega$$

$$\text{Ideal Gain} = 120 / 12 = 10$$

The measured value of the resistors:

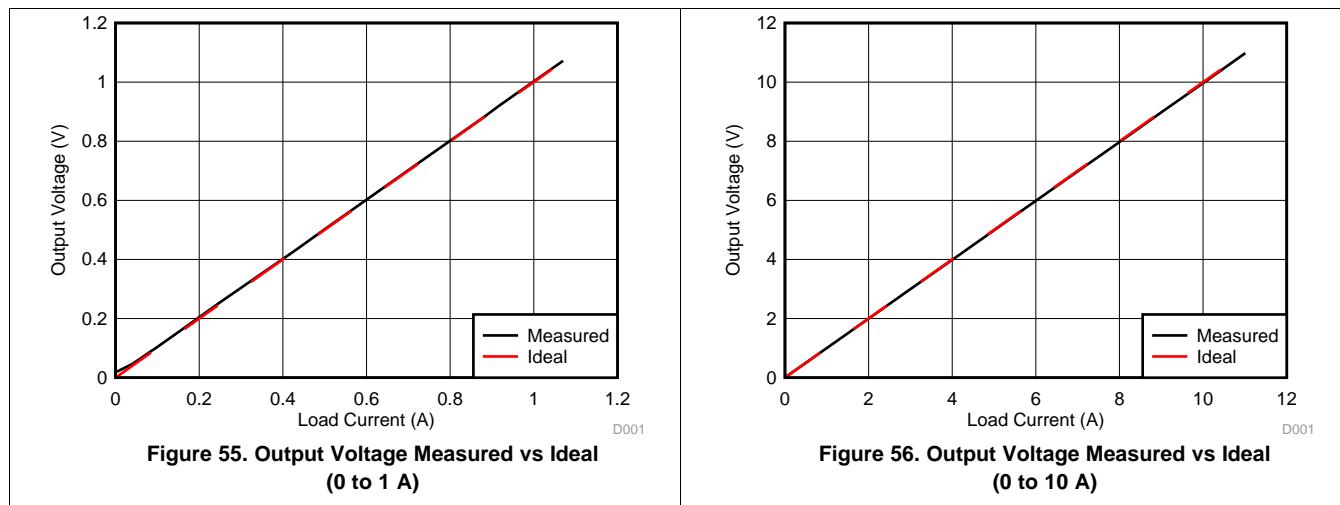
$$R_1 = 11.835 \text{ k}\Omega$$

$$R = 11.85 \text{ k}\Omega$$

$$R_2 = 117.92 \text{ k}\Omega$$

$$R_g = 118.07 \text{ k}\Omega$$

### 8.2.1.3 Application Curves



## 9 Power Supply Recommendations

Supply voltage for a single supply is from 4.4 V to 16 V, and from  $\pm 2.2$  V to  $\pm 8$  V for a dual supply. In the high-side sensing application, the supply is connected to a 12-V battery.

## 10 Layout

### 10.1 Layout Guidelines

The TLC2274AM-MIL device is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed-circuit-board (PCB) layout practices are required. Low-loss  $0.1\text{-}\mu\text{F}$  bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

### 10.2 Layout Example

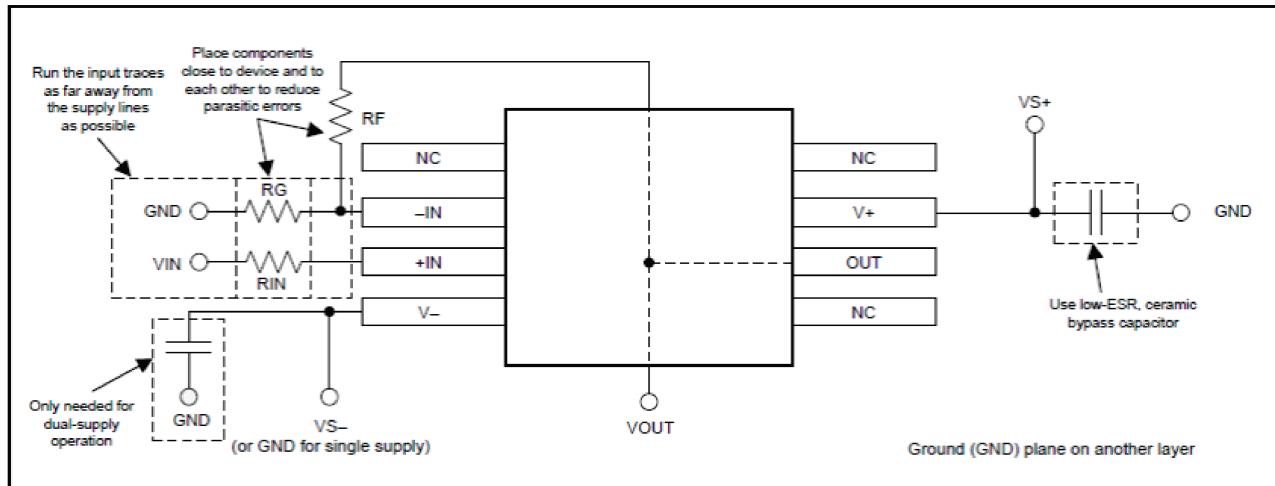
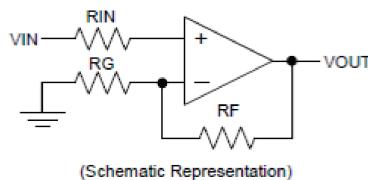


Figure 57. Layout Example

## 11 Device and Documentation Support

### 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

MicroSim Parts, PSpice are trademarks of MicroSim.

All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9318202Q2A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB
5962-9318202QCA	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QC A TLC2274AMJB
5962-9318202QDA	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QD A TLC2274AMWB
TLC2274AMFKB	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB
TLC2274AMFKB.A	Active	Production	LCCC (FK)   20	55   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202Q2A TLC2274 AMFKB
TLC2274AMJB	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QC A TLC2274AMJB
TLC2274AMJB.A	Active	Production	CDIP (J)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QC A TLC2274AMJB
TLC2274AMWB	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QD A TLC2274AMWB
TLC2274AMWB.A	Active	Production	CFP (W)   14	25   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9318202QD A TLC2274AMWB

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

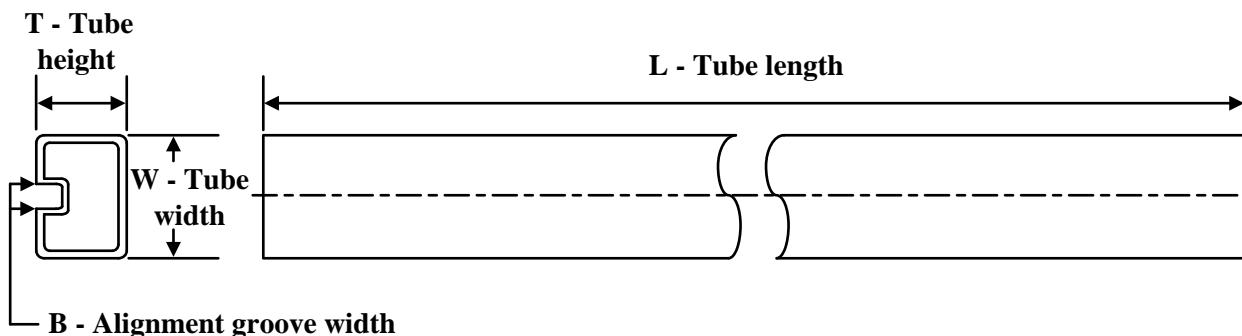
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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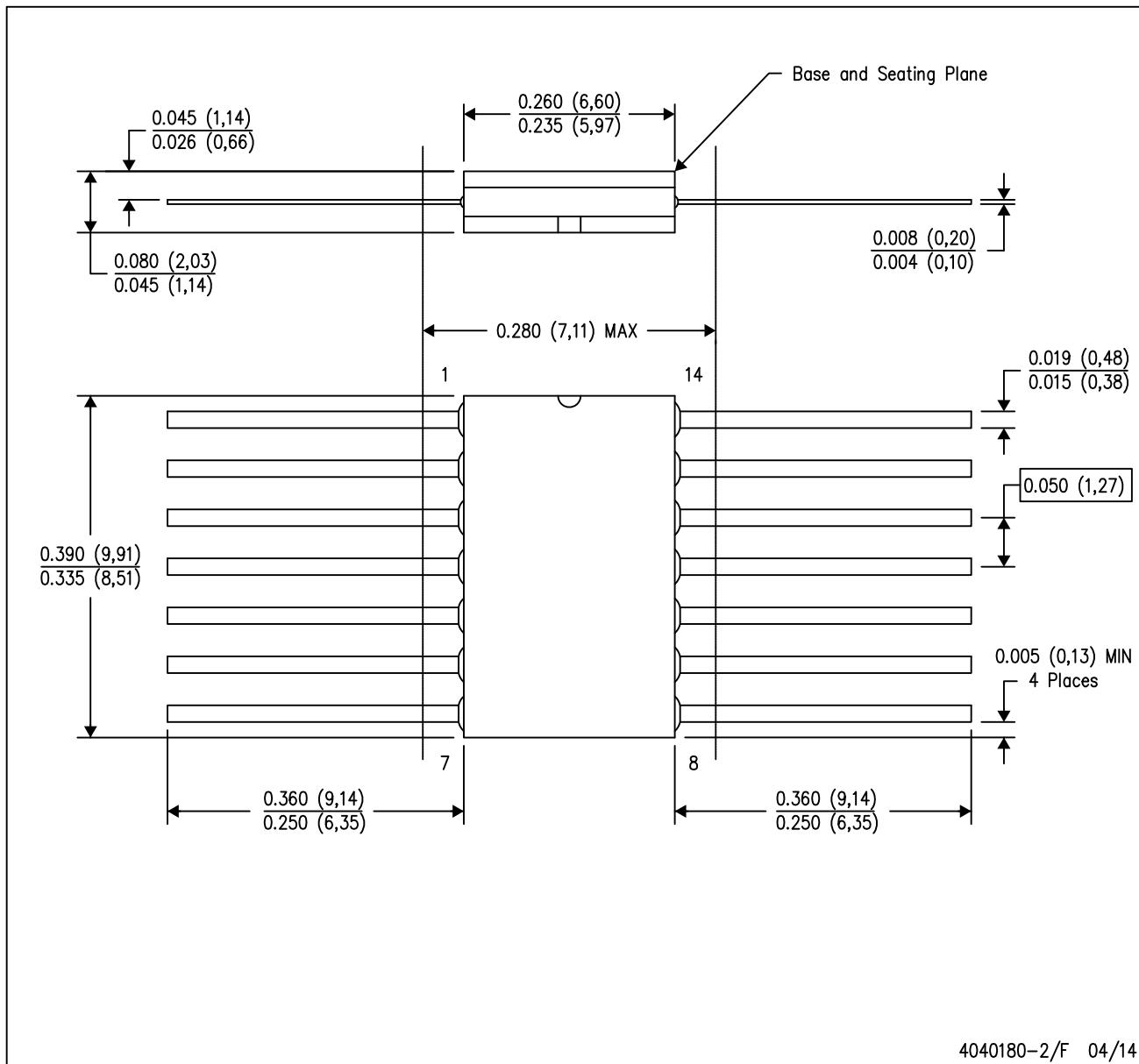
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T ( $\mu$ m)	B (mm)
5962-9318202Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9318202QDA	W	CFP	14	25	506.98	26.16	6220	NA
TLC2274AMFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2274AMFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC2274AMWB	W	CFP	14	25	506.98	26.16	6220	NA
TLC2274AMWB.A	W	CFP	14	25	506.98	26.16	6220	NA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP1-F14

# GENERIC PACKAGE VIEW

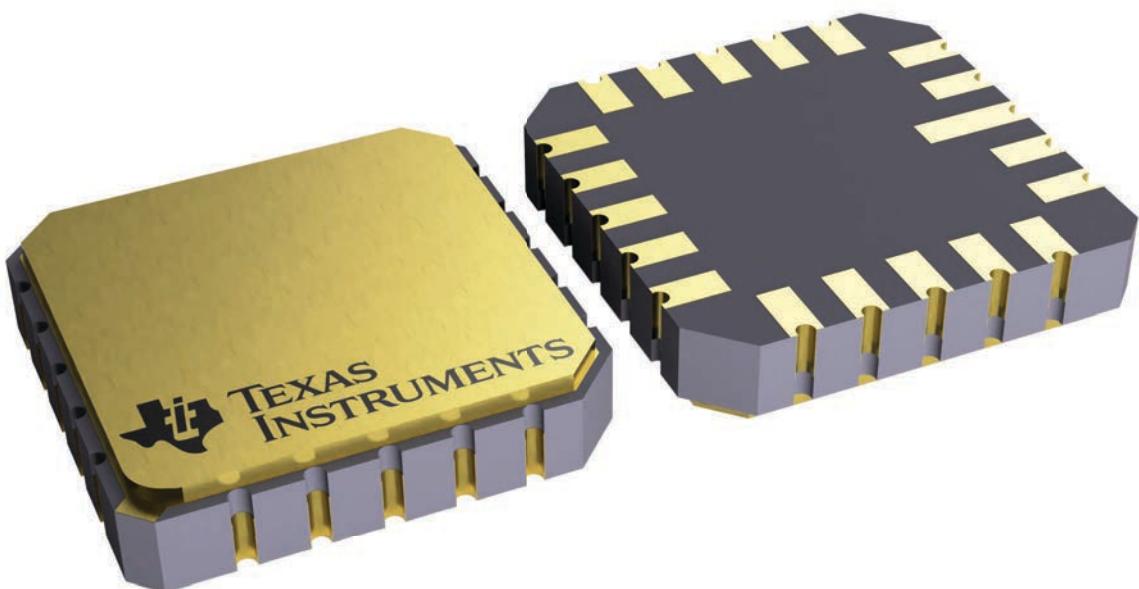
**FK 20**

**LCCC - 2.03 mm max height**

**8.89 x 8.89, 1.27 mm pitch**

**LEADLESS CERAMIC CHIP CARRIER**

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



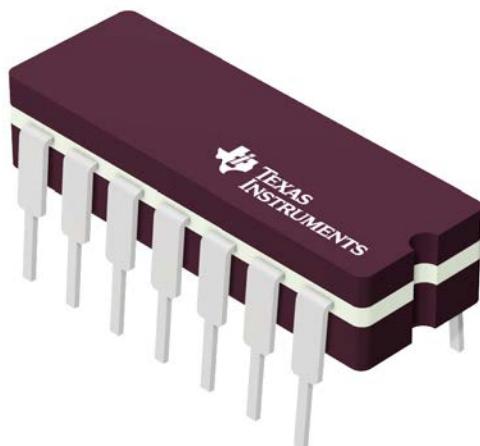
4229370VA\

# GENERIC PACKAGE VIEW

**J 14**

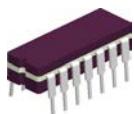
**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

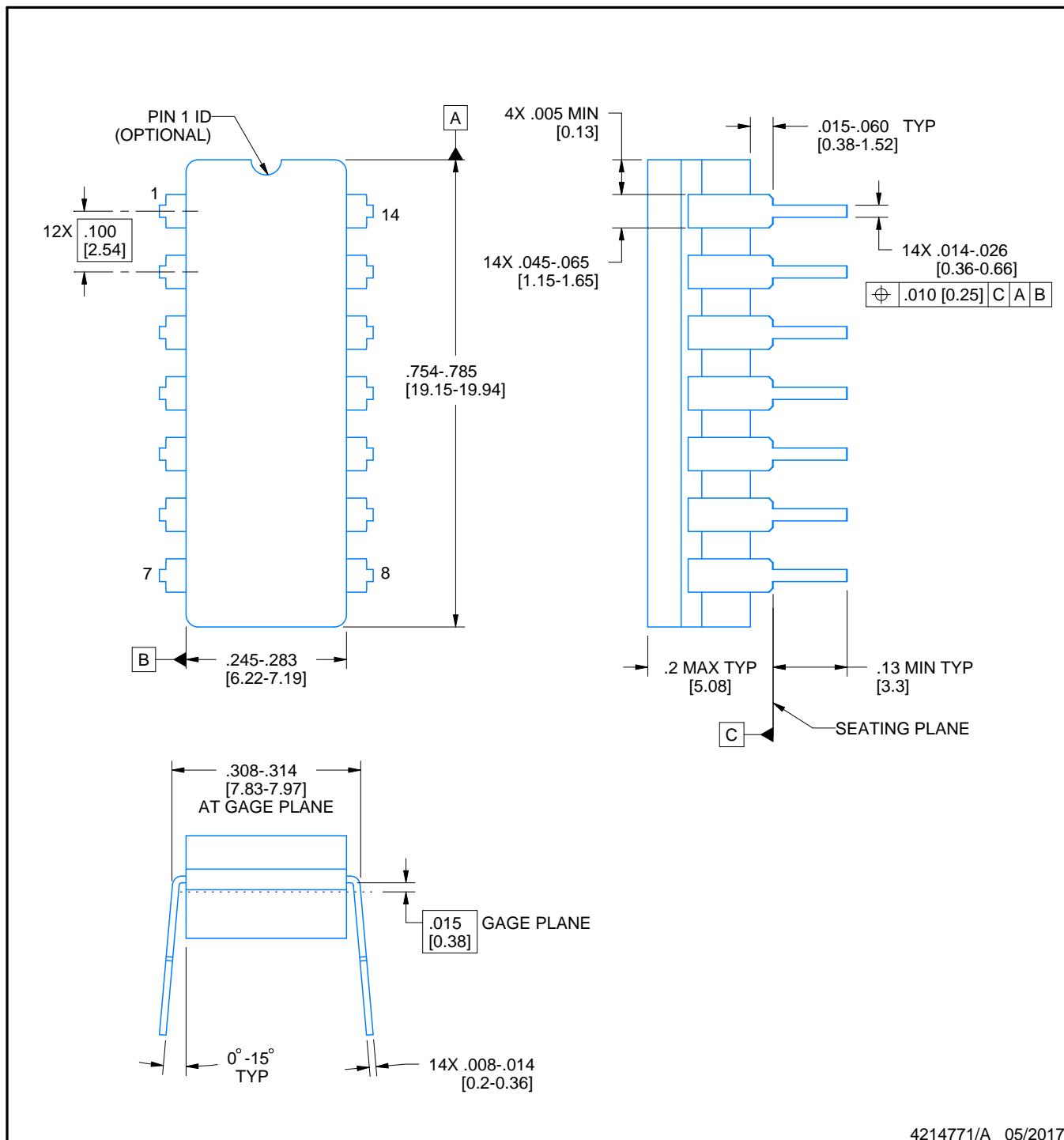


# PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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## NOTES:

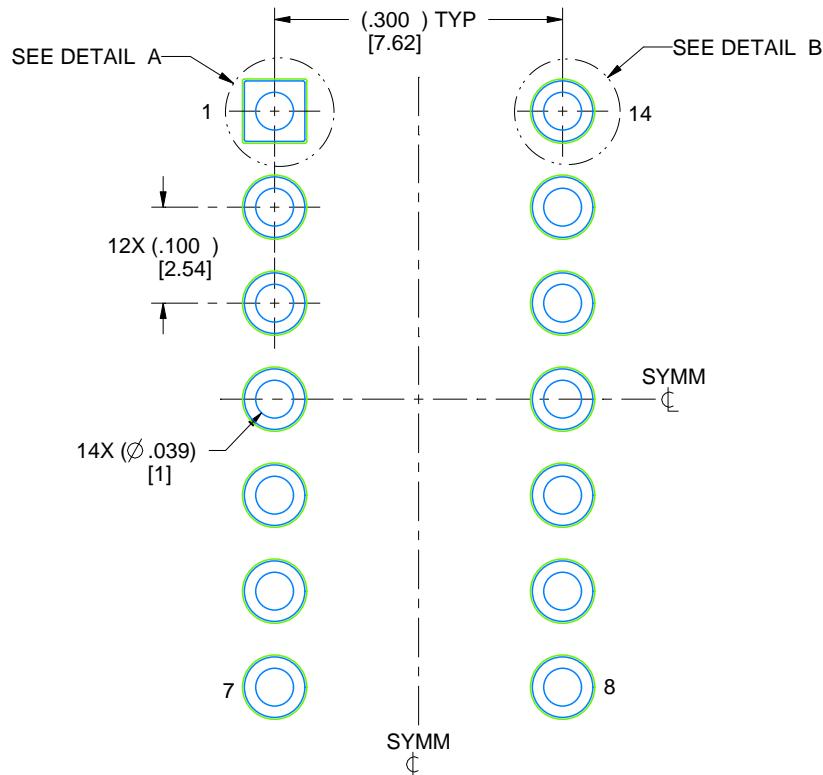
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

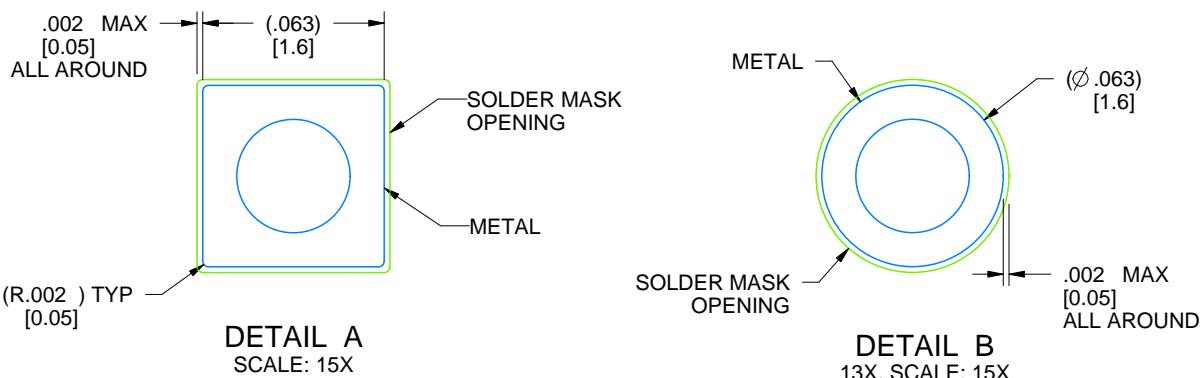
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



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