TLC372-EP Dual Differential Comparator

1 Features

- Controlled baseline
  - One assembly/test site, one fabrication site
- Extended temperature performance of –55°C to 125°C
- ESD protection exceeds 2000V per MIL-STD-883, method 3015; exceeds 100V using machine model (C = 200pF, R = 0)
- Single or dual-supply operation
- Wide range of supply voltages . . .4V to 16V
- Very low supply current drain . . .10µA typical
- Fast response time . . . 420ns typical for TTL-level input step
- Built-in ESD protection
- High input impedance . . . $10^{12}\Omega$ typical
- Extremely low input bias current. . .5pA typical
- Ultra-stable low input offset voltage
- Common-mode input voltage range includes ground
- Output compatible with TTL, MOS, and CMOS
- Pin-compatible with LM393

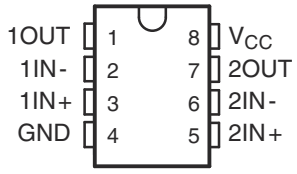
2 Description

This device is fabricated using CMOS technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 4V to 16V. Each device features extremely high input impedance (typically greater than $10^{12}\Omega$), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000V ESD rating using human-body-model (HBM) testing. However, care must be exercised in handling this device as exposure to ESD can result in a degradation of the device parametric performance.

The TLC372 is characterized for operation from –55°C to 125°C.

D PACKAGE
(TOP VIEW)



SYMBOL (each comparator)

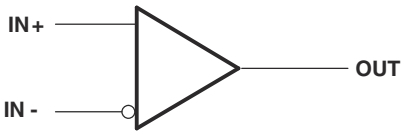


Table of Contents

Ordering Information

T_A (1)	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOIC-(D)	Tape and reel	TLC372MDREP	372MEP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

3 Specifications

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage (2)		18	V
V_{ID}	Differential input voltage(3)		±VDD	V
V_I	Input voltage range	–0.3	VDD	V
V_O	Output voltage		18	V
I_I	Input current		±5	mA
I_O	Output current		20	mA
	Duration of output short circuit to ground(4)			unlimited
T_A	Operating free-air temperature range	–55	125	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1.6mm (1/16 in) from case for 10s:		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltage values except differential voltages are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

3.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage		4	16	V
V_{IC}	Common-mode input voltage	V_{DD} = 5V	0	3.5	V
		V_{DD} = 10V	0	8.5	
T_A	Operating free-air temperature		–55	125	°C

3.3 Electrical Characteristics

at specified free-air temperature, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min(2)		25°C		1	5	mV
				Full range			10	
I_{IO}	Input offset current			25°C		1		pA
				Max			10	nA
I_{IB}	Input bias current			25°C		5		pA
				Max			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} – 1			V
				Full range	0 to V_{DD} – 1.5			
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V	25°C		0.1		nA
			V_{OH} = 15V	Full range			3	µA
V_{OL}	Low-level output voltage	V_{ID} = –1V,	I_{OL} = 4mA	25°C		150	400	mV
				Full range			700	
I_{OL}	Low-level output current	V_{ID} = –1V,	V_{OL} = 1.5V	25°C	6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = –1V,	No load	25°C		10	20	µA
				Full range			30	

(1) All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is –55°C to 125°C. IMPORTANT: See Parameter Measurement Information.
(2) The offset voltage limits given are the maximum values required to drive the output above 4V or below 400mV with a 10kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

3.4 Switching Characteristics

V_{DD} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5V through 5.1kΩ, C_L = 15pF(1) (2)	100mV input step with 10mV overdrive	650	ns
		100mV overdrive	420	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

3.5 Typical Characteristics

T_A = 25°C, V_S = 12V, R_{PULLUP} = 2.5k, C_L = 20pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

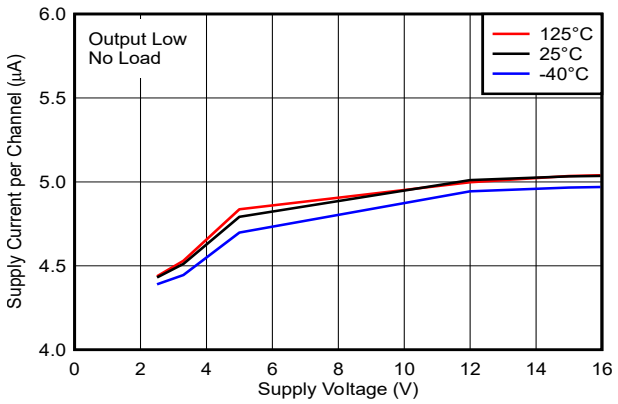


Figure 3-1. Supply Current per Channel vs. Supply Voltage, Output Low

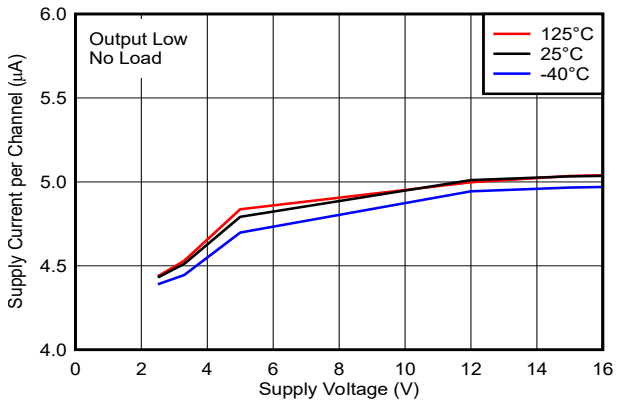


Figure 3-2. Supply Current per Channel vs. Supply Voltage, Output High

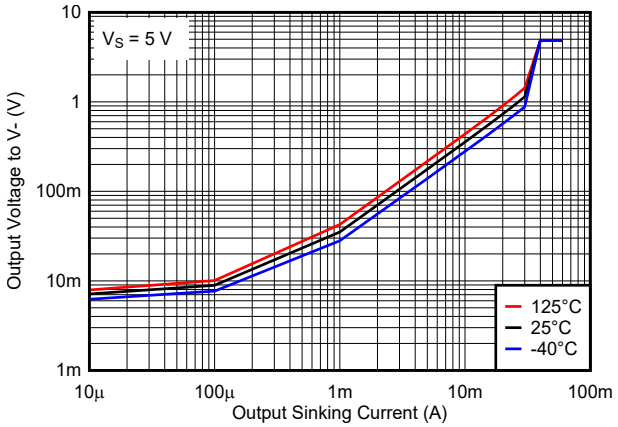


Figure 3-3. Output Voltage vs. Output Sinking Current, 5V

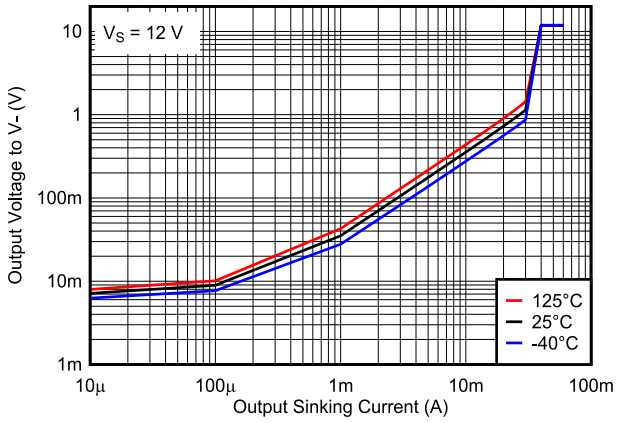


Figure 3-4. Output Voltage vs. Output Sinking Current, 12V

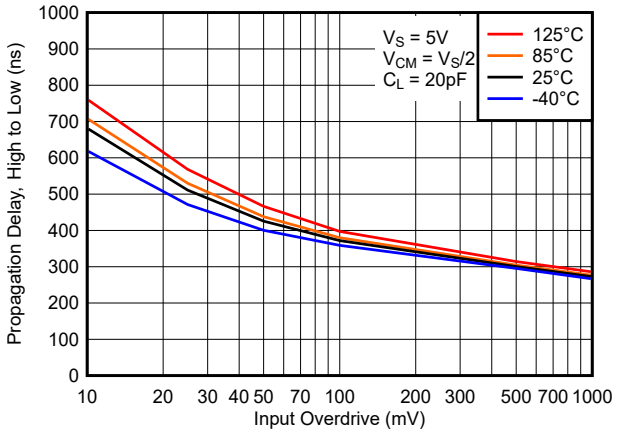


Figure 3-5. Propagation Delay, High to Low, 5V

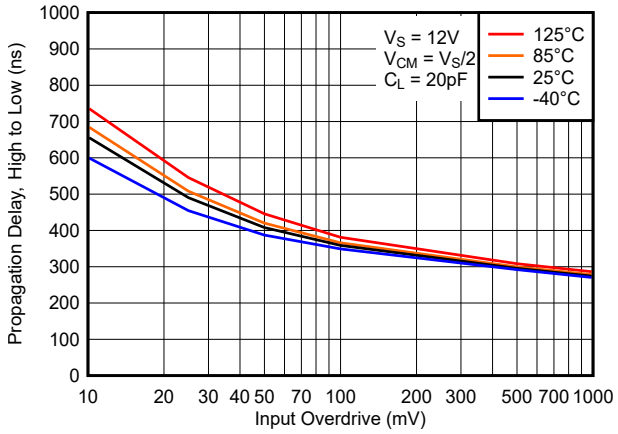


Figure 3-6. Propagation Delay, High to Low, 12V

4 Detailed Description

4.1 Overview

The TLC372-EP device is a micro-power comparator with open-drain output. Operating down to 4V while only consuming only 5µA per channel, the TLC372-EP is excellent for power conscious applications.

4.2 Functional Block Diagrams

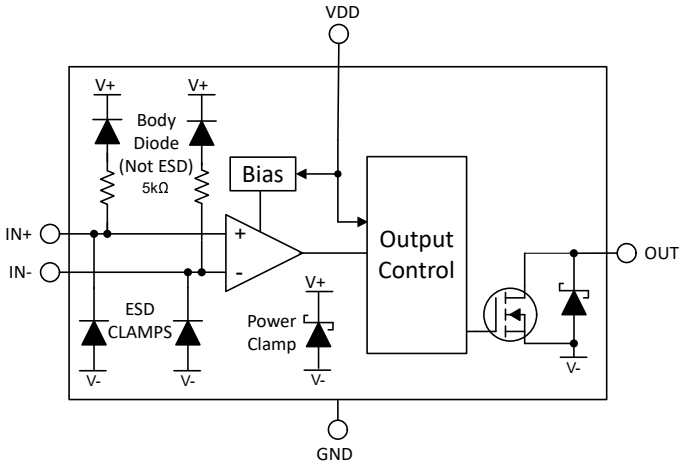


Figure 4-1. Block Diagram

4.3 Feature Description

The TLC372-EP comparator consists of a CMOS differential pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The output consists of an open-drain output stage capable of sinking current with a negative differntial input voltage.

4.4 Device Functional Modes

4.4.1 Input

The TLC372-EP input voltage range extends from V- to 1.5V below V+ over the full temperature range. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

4.4.2 ESD Protection

The TLC372-EP open-drain output ESD protection consists of a snapback ESD clamp between the output and GND to allow the output to be pulled above VCC to a maximum of 16V. For the inputs, there is a "lower" ESD clamp between GND and the inputs and there is also a parasitic "upper" ESD soft-clamp diode between the input and VCC with a 5kΩ equivelent resistance. TI does not recommend applying signals to the inputs with no supply voltage.

When the inputs are connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limitng the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

4.4.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage.

4.4.4 Open-Drain Output

The TLC372-EP features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 16V, independent of the comparator supply voltage (VDD). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values can help increase the rising edge rise-time, but at the expense of increasing VOL and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) creates an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to VDD can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs can be left floating, or can be tied to the GND pin if floating pins are not desired.

4.4.5 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 4-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

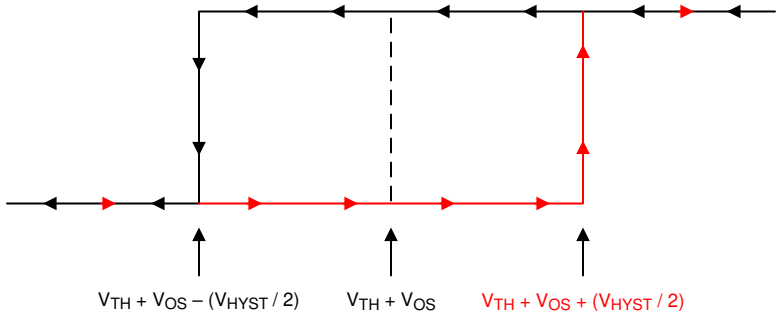


Figure 4-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

5 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

5.1 Application Information

5.1.1 Basic Comparator Definitions

5.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 5-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 5-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 5-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

5.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 5-1 and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called overdrive (V_{OD}) and underdrive (V_{UD}) voltage levels (see section below).

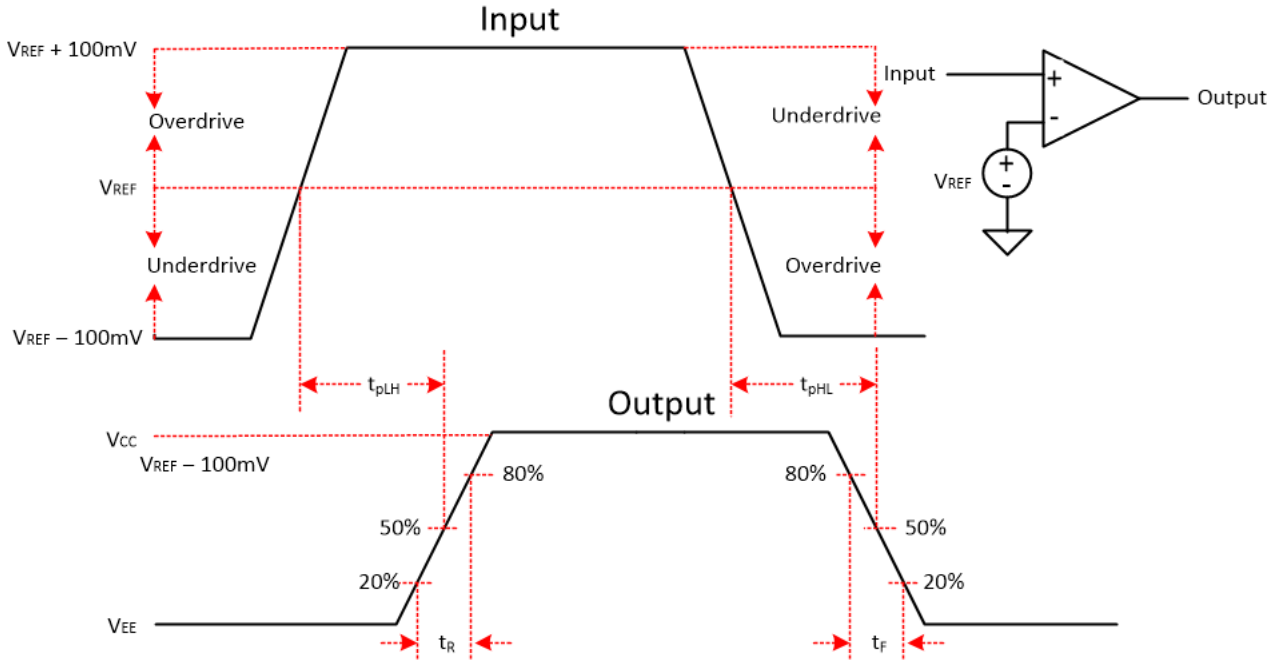


Figure 5-1. Comparator Timing Diagram

5.1.1.3 Overdrive and Underdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 5-1 example. Similarly, underdrive voltage, V_{UD}, is how far below REF the input starts. The overdrive and underdrive voltages influence the propagation delay (t_p). See curves in the Typical Characteristics section for more details. The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes propagation delay to increase. This is particularly important in applications where rail-to-rail input swings are present at the comparator inputs. The result can be skewed propagation delay (difference between tp_{LH} and tp_{HL}). As a low power comparator, do not use this comparator family if variation in propagation delay is critical.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

5.2 Typical Applications

5.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. The figure below shows a simple window comparator circuit monitoring a 24V PLC power supply.

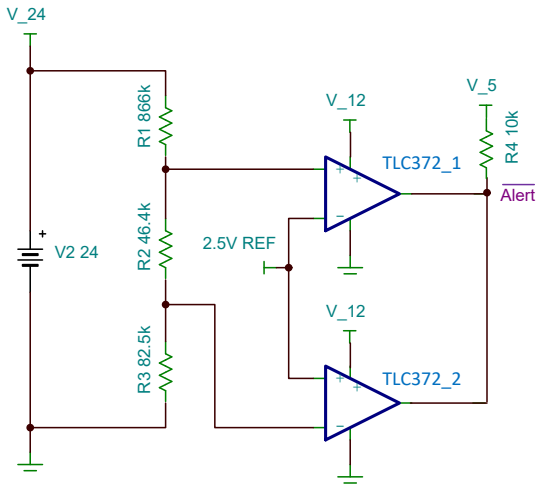


Figure 5-2. Window Comparator

5.2.1.1 Design Requirements

For this design, follow these design requirements:

- UV_Alert (logic low output) when the 24V supply is less than 19.2V
- OV_Alert (logic low output) when the 24V supply is greater than 30V
- Current dissipated in the resistor string is 30uA
- Comparator operates from the 12V supply
- 2.5V external reference is utilized

5.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLC372-EP is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, OV_Alert and UV_Alert nets are pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from 2.5V / 30uA which is approximately 83.3kohms.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from (2.5V /19.2uA) - R3 which is approximately 46.9kohms.

Lastly, the value of R1 is calculated from 1Mohm - (R2 + R3) which is approximately 870kohms. Please note that standard 1% resistor values were selected for the circuit

The respective comparator outputs (OV_Alert and UV_Alert) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.

5.2.1.3 Application Curve

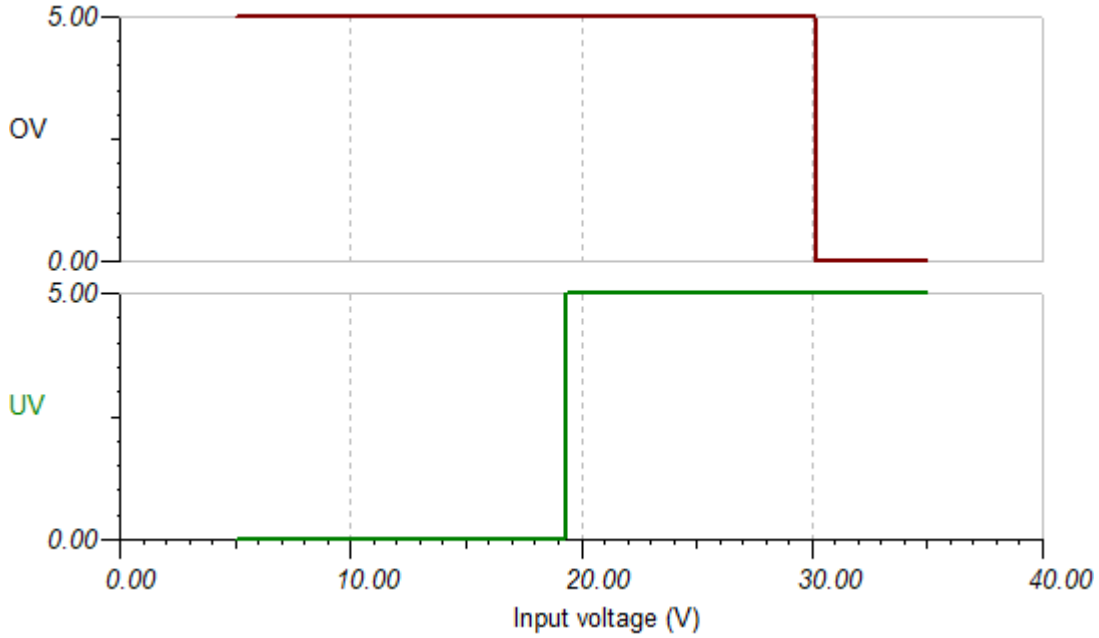


Figure 5-3. Window Comparator Results

5.3 Power Supply Recommendations

Due to the fast output edge rates, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between V+ pin and ground pins. Narrow, peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

5.4 Layout

5.4.1 Layout Guidelines

For accurate comparator applications, a clean, stable power supply is important to minimize output glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The

bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the VCC and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a VCC or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (≤100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

5.4.2 Layout Example

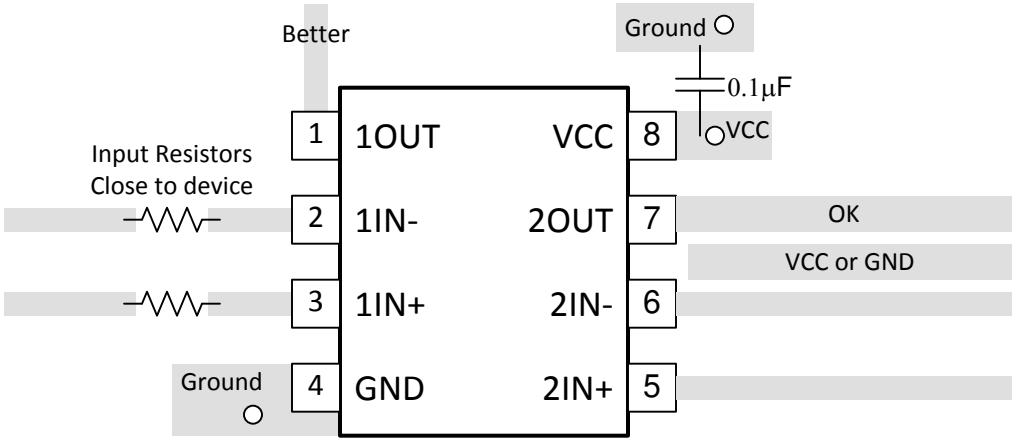


Figure 5-4. Dual Layout Example

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

6.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2007) to Revision A (June 2025)	Page
• Changes throughout data sheet to reflect the performance of the new design	1
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC372MDREP	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	372MEP
TLC372MDREP.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	372MEP
V62/06675-01XE	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	372MEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

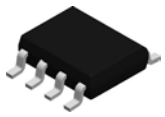
OTHER QUALIFIED VERSIONS OF TLC372-EP :

- Catalog : TLC372

- Military : TLC372M

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

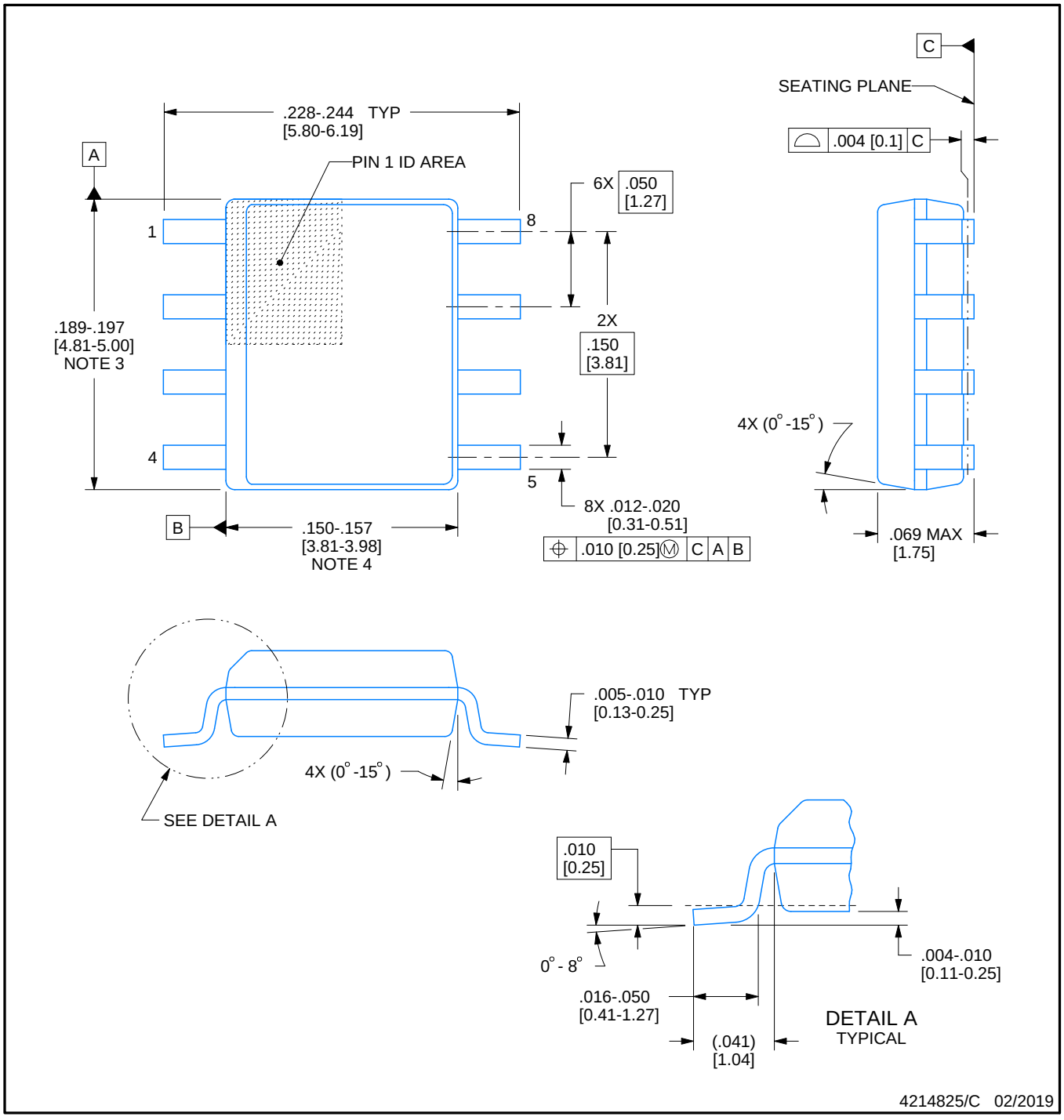


PACKAGE OUTLINE

D0008A

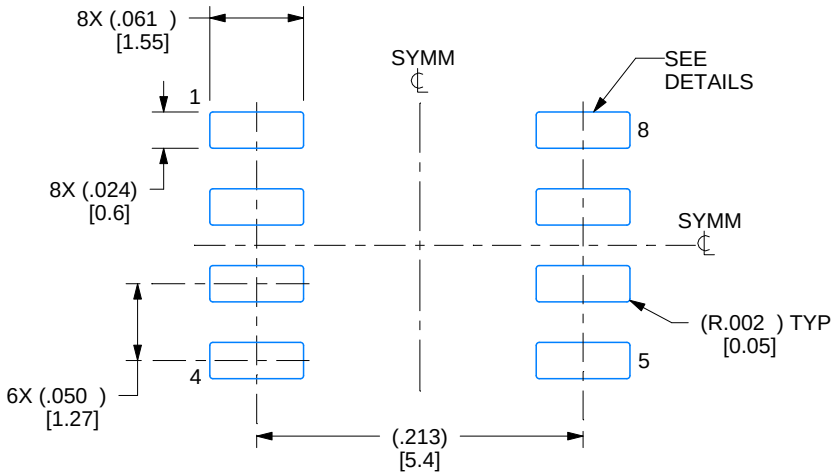
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

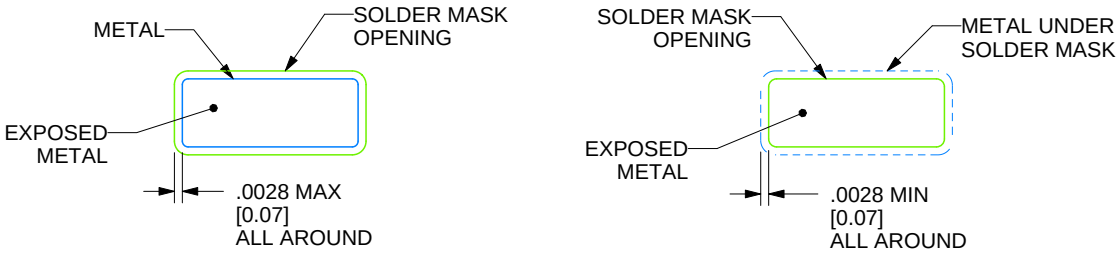


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

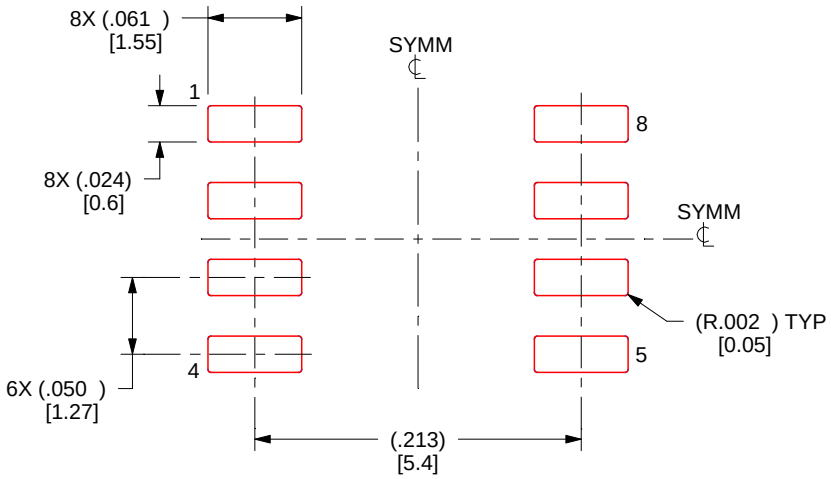
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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