TLC372 Dual Differential Comparators

1 Features

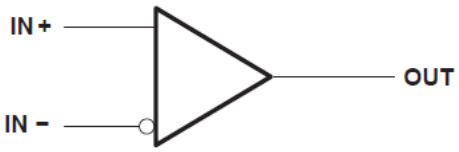
- Single or dual-supply operation
- Wide range of supply voltages: 3V to 16V
- Low supply current drain 150μA typical at 5V
- Fast response time: 200ns typical for TTL-Level input step
- Built-in ESD protection
- High input impedance: $10^{12}\Omega$ typical
- Extremely low input bias current: 5pA typical
- Ultra-stable low input offset voltage
- Common-mode input voltage range includes ground
- Output compatible with TTL, MOS, and CMOS
- Pin-compatible with LM393

2 Description

This device is fabricated using CMOS technology and consists of two independent voltage comparators, each designed to operate from a single power supply. Operation from dual supplies is also possible if the difference between the two supplies is 3V to 16V. Each device features extremely high input impedance (typically greater than $10^{12}\Omega$), allowing direct interfacing with high-impedance sources. The outputs are n-channel open-drain configurations and can be connected to achieve positive-logic wired-AND relationships.

The TLC372 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 1000V ESD rating using human body model testing. However, care should be exercised in handling this device as exposure to ESD may result in a degradation of the device parametric performance.

The TLC372C is characterized for operation from 0°C to 70°C. The TLC372I is characterized for operation from−40°C to 85°C. The TLC372M is characterized for operation over the full military temperature range of −55°C to 125°C. The TLC372Q is characterized for operation from −40°C to 125°C.



Symbol (Each Comparator)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Device Comparison Table

Available Options (1)

T_A	V_{IO} max at 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)(2)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLAT PACK (U)
0°C to 70°C	5mV	TLC372CD	—	—	TLC372CP	TLC372CPW	—
−40°C to 85°C	5mV	TLC372ID	—	—	TLC372IP	—	—
−55°C to 125°C	5mV	TLC372MD	TLC372MFK	TLC372MJG	TLC372MP	—	TLC372MU
−40°C to 125°C	5mV	TLC372QD	—	—	TLC372QP	—	—

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The D packages are available taped and reeled. Add R suffix to device type (e.g., TLC372CDR).

4 Pin Configuration and Functions

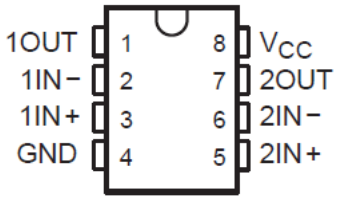
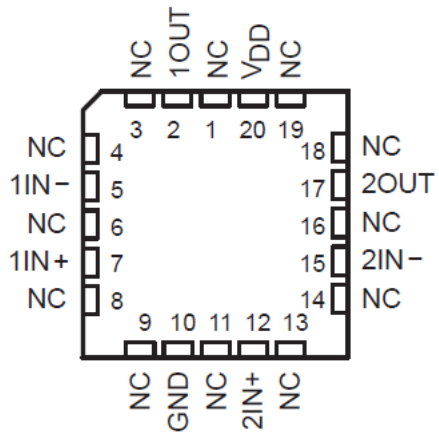


Figure 4-1. TLC372C, TLC372I, TLC372M, TLC372QD, P, or PW Package TLC372M JG Package (Top View)



A. NC− No internal connection.

Figure 4-2. TLC372M FK Package (Top View)

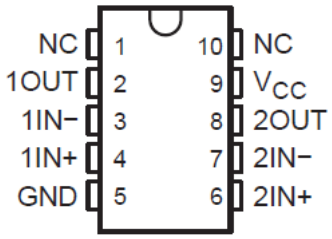


Figure 4-3. TLC372M U Package (Top View)

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage(2)			18	V
V_{ID}	Differential input voltage(3)			±18	V
V_I	Input voltage range		–0.3	VDD	V
V_O	Output voltage			18	V
I_I	Input current			±5	VmA
I_O	Output current			20	mA
	Duration of output short circuit to ground(4)		Unlimited		
θ_{JA}	Package thermal impedance(5) (6)	D package		97.1	°C/W
		P package		84.6	
		PW package		149	
θ_{JC}	Package thermal impedance(5) (6)	FK package		5.6	°C/W
		JG package		14.5	
		U package		14.7	
T_A	Operating free-air temperature range	TLC372C	0	70	°C
		TLC372I	–40	85	
		TLC372M	–55	125	
		TLC372Q	–40	125	
	Storage temperature range		–65	150	°C
	Case temperature for 60 seconds	FK package		260	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds	D package		260	°C
		P package			
		PW package			
	Lead temperature 1.6mm (1/16 inch) from case for 60 seconds	JG package		300	°C
		U package			

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential voltages are with respect to network ground.
(3) Differential voltages are at IN+ with respect to IN−.
(4) Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.
(5) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(6) The package thermal impedance is calculated in accordance with JESD 51-7 (plastic) or MIL-STD-883 Method 1012 (ceramic).

5.2 Recommended Operating Conditions

			TLC372C		TLC372I		TLC372M		TLC372Q		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{DD}	Supply voltage		3	16	3	16	4	16	4	16	V
V_{IC}	Common-mode input voltage	V_{DD} = 5V	0	3.5	0	3.5	0	3.5	0	3.5	V
		V_{DD} = 10V	0	8.5	0	8.5	0	8.5	0	8.5	
T_A	Operating free-air temperature,		0	70	−40	85	−55	125	−40	125	°C

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5.3 Electrical Characteristics

at specified free-air temperature, V_{DD} = 5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	TLC372C			TLC372I			TLC372M, TLC372Q			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min (2)		25°C		1	5		1	5		1	5	mV
				Full range			6.5			7			10	
I_{IO}	Input offset current			25°C		1			1			1		pA
				MAX			0.3			1			10	nA
I_{IB}	Input bias current			25°C		5			5			5		pA
				MAX			0.6			2			20	nA
V_{ICR}	Common-mode input voltage range			25°C	0 to V_{DD} −1			0 to V_{DD} −1			0 to V_{DD} −1			V
				Full range	0 to V_{DD} −1.5			0 to V_{DD} −1.5			0 to V_{DD} −1.5			
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V	25°C		0.1			0.1			0.1		nA
			V_{OH} = 15V	Full range			1			1			3	μA
V_{OL}	Low-level output voltage	V_{ID} = −1V	I_{OL} = 4mA	25°C		150	400		150	400		150	400	mV
				Full range			700			700			700	
I_{OL}	Low-level output current	V_{ID} = −1V	V_{OL} = 1.5V	25°C	6	16		6	16		6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1V	No load	25°C		150	300		150	300		150	300	μA
				Full range			400			400			400	

(1) All characteristics are measured with zero common-mode input voltage unless otherwise noted. Full range is 0°C to 70°C for TLC372C, −40°C to 85°C for TLC372I, and −55°C to 125°C for TLC372M and −40°C to 125°C for TLC372Q.
(2) The offset voltage limits given are the maximum values required to drive the output above 4V or below 400mV with a 10kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

5.4 Switching Characteristics

V_{DD} = 5V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L connected to 5V through 5.1kΩ, C_L = 15pF (1) (2)	100mV input step with 10mV overdrive		200		ns
		100mV overdrive		100		

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4V.

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5.5 Electrical Characteristics

at specified free-air temperature, V_{DD} = 5V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		TLC372Y			UNIT
				MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_{IC} = V_{ICR}min[2]			1	5	mV
I_{IO}	Input offset current				1		pA
I_{IB}	Input bias current				5		pA
V_{ICR}	Common-mode input voltage range			0 to V_{DD} −1			V
I_{OH}	High-level output current	V_{ID} = 1V	V_{OH} = 5V		0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1V	I_{OL} = 4mA		150	400	mV
I_{OL}	Low-leve loutput current	V_{ID} = −1V	V_{OL} = 1.5V	6	16		mA
I_{DD}	Supply current (two comparators)	V_{ID} = 1V	No load		150	300	µA

(1) All characteristics are measured with zero common-mode input voltage unless otherwise noted.
(2) The offset voltage limits given are the maximum values required to drive the output above 4V or below 400mV with a 10kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

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6 Typical Characteristics

At T_A = 25°C, V_S = 12V, V_{CM} = V_S/2V, C_L = 15pF, Input Overdrive = Input Underdrive = 100mV, R_{PU} = 10kΩ, unless otherwise noted.

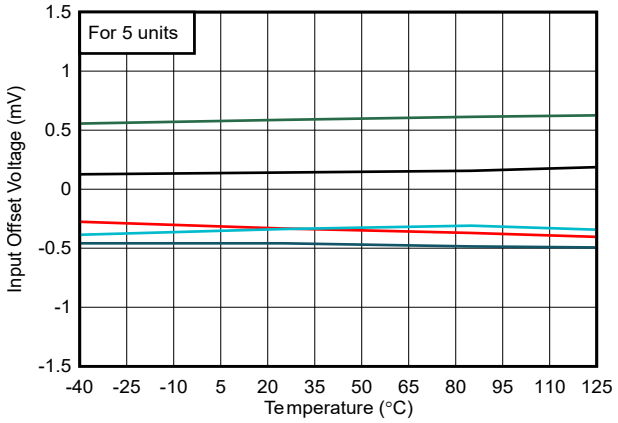

Figure 6-1. Offset vs. Temperature

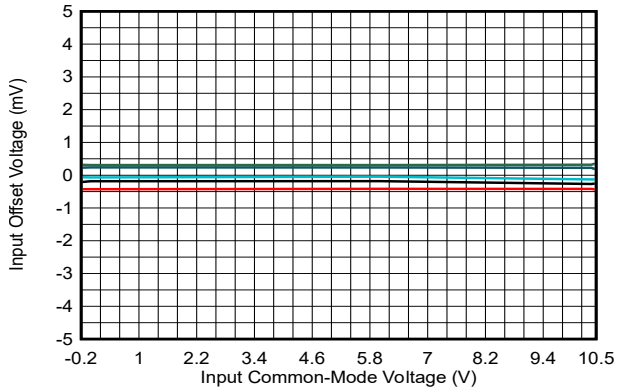

Figure 6-2. Offset Voltage vs. Common-Mode, 12V

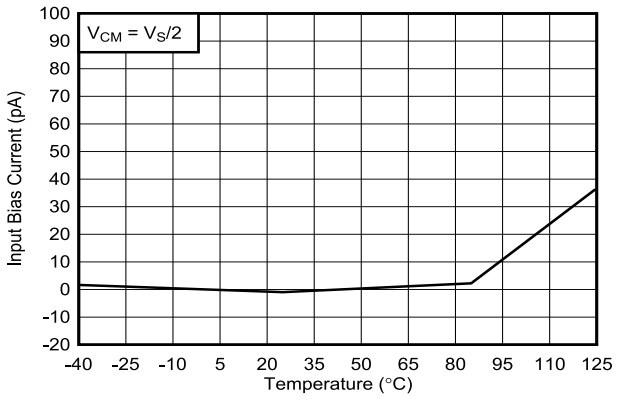

Figure 6-3. Bias Current vs. Temperature

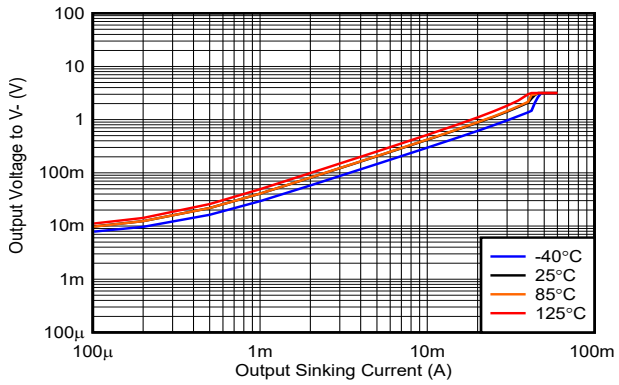

Figure 6-4. Output Voltage vs. Sinking Current, 3.3V

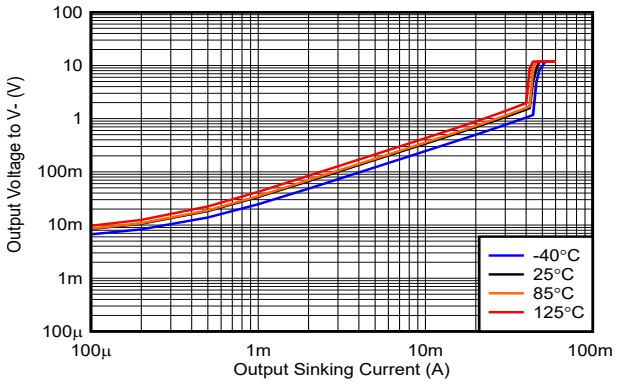

Figure 6-5. Output Voltage vs. Sinking Current, 12V

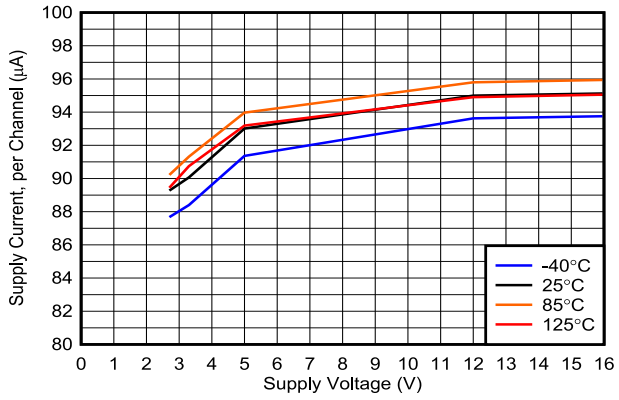

Figure 6-6. Supply Current vs. Supply Voltage, Output LOW, No Load

6 Typical Characteristics (continued)

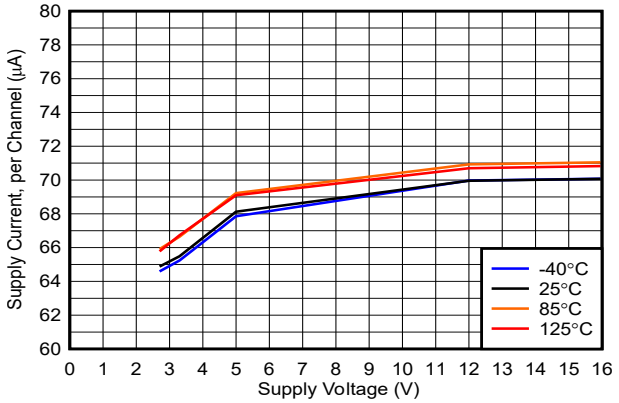

Figure 6-7. Supply Current vs. Supply Voltage, Output HIGH, No Load

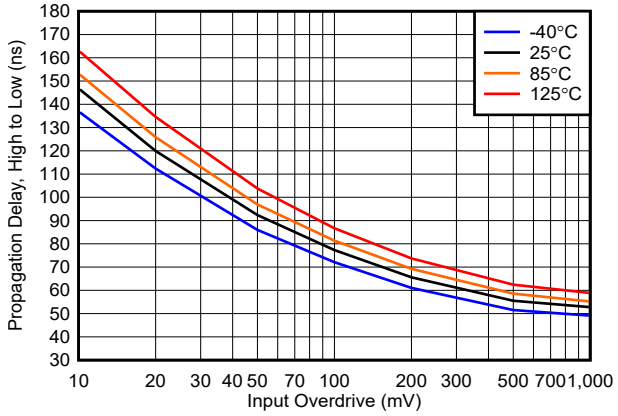

Figure 6-8. Propagation Delay, (High to Low) vs. Input Overdrive, 3.3V

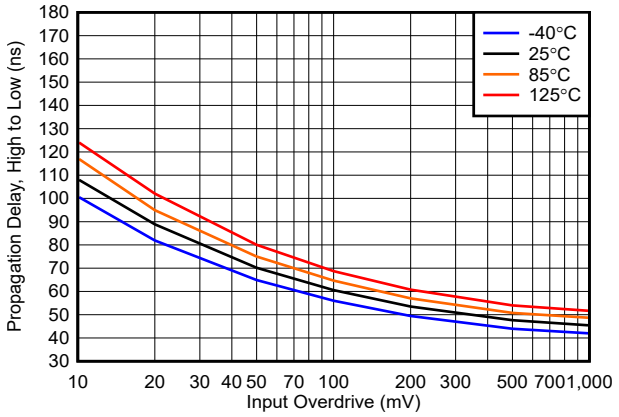

Figure 6-9. Propagation Delay, (High to Low) vs. Input Overdrive, 12V

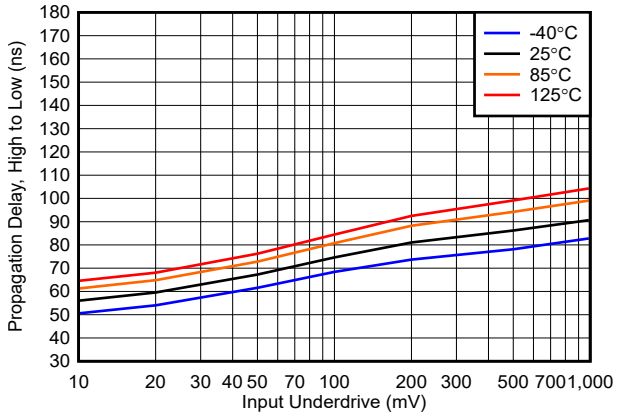

Figure 6-10. Propagation Delay, (High to Low) vs. Input Underdrive, 3.3V

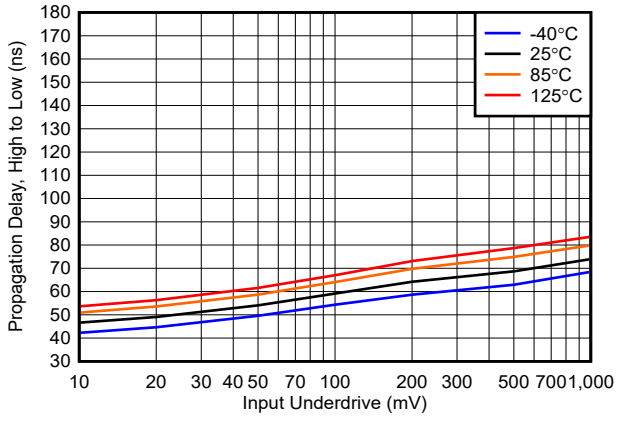

Figure 6-11. Propagation Delay, (High to Low) vs. Input Underdrive, 12V

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7 Detailed Description

7.1 Overview

The TLC372 device is a micro-power comparator with open-drain output. Operating down to 3V while only consuming only 75µA per channel, the TLC372 is excellent for power conscious applications.

7.2 Functional Block Diagrams

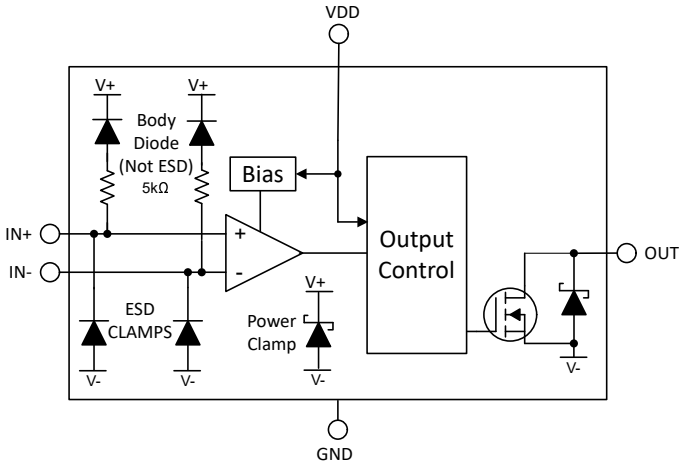

Figure 7-1. Block Diagram

7.3 Feature Description

The TLC372 comparator consists of a CMOS differential pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The output consists of an open-drain output stage capable of sinking current with a negative differntial input voltage.

7.4 Device Functional Modes

7.4.1 Input

The TLC3x2 input voltage range extends from V- to 1.5V below V+ over the full temperature range. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input voltages stay within the specified range.

7.4.2 ESD Protection

The TLC3x2 input and output ESD protection contains a conventional diode-type "upper" ESD clamp between the I/O pins and V+, and a "lower" ESD clamp between the I/O pins and V-. The inputs or output must not exceed the supply rails by more than 300mV. TI does not recommend applying signals to the inputs with no supply voltage.

When the inputs are connected to a low impedance source, such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any currents when the clamps conduct. The current must be limited 10mA or less, though TI recommends limitng the current to 1mA or less. This series resistance can be part of any resistive input dividers or networks.

7.4.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency chatter as the device triggers on it's own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage.

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7.4.4 Open-Drain Output

The TLC3x2 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to an external voltage from 0V up to 16V, independent of the comparator supply voltage (VDD). The open-drain output allows logical OR'ing of multiple open drain outputs and logic level translation. TI recommends setting the pull-up resistor current to between 100uA and 1mA. Lower value pull-up resistor values can help increase the rising edge rise-time, but at the expense of increasing VOL and higher power dissipation. The rise-time is dependent on the time constant of the total pull-up resistance and total load capacitance. Large value pull-up resistors (>1 MΩ) creates an exponential rising edge due to the output RC time constant and increase the rise-time.

Directly shorting the output to VDD can result in thermal runaway and eventual device destruction at high (>12V) pull-up voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused open drain outputs can be left floating, or can be tied to the GND pin if floating pins are not desired.

7.4.5 Hysteresis

The basic comparator configuration can oscillate or produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator.

This problem can be prevented by the addition of hysteresis or positive feedback.

The hysteresis transfer curve is shown in Figure 7-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

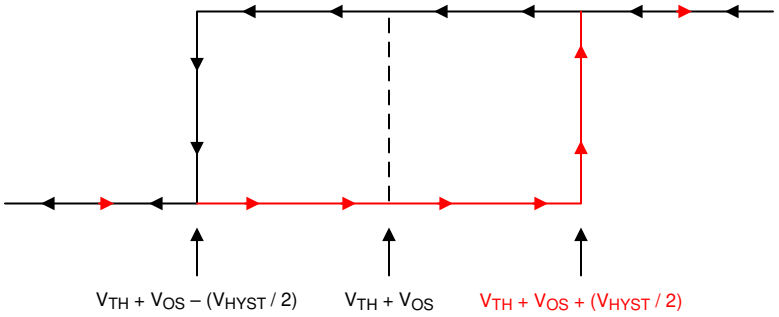

Figure 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.4.5.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown below.

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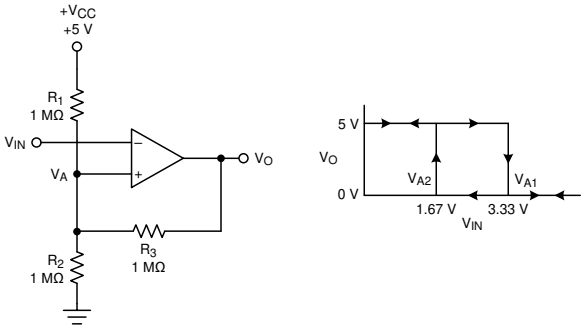

Figure 7-3. Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown below.

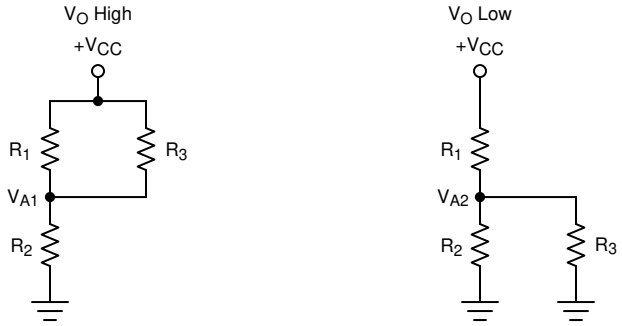

Figure 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown above on the left.

The equation below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown above on the right.

Use the equation below to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

The equation below defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

7.4.5.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 7-5.

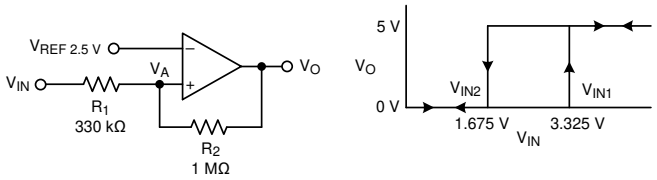

Figure 7-5. Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 7-6.

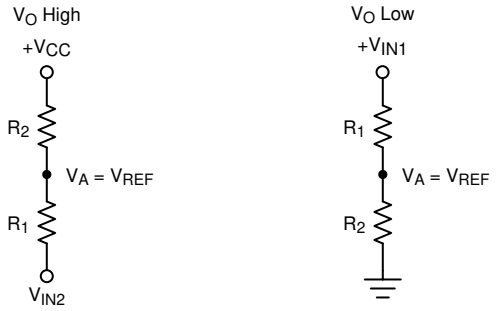

Figure 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Basic Comparator Definitions

8.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 8-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is in a high-Z state. Table 8-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 8-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

8.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 8-1 and is measured from the mid-point of the input to the midpoint of the output. Likewise, propagation varies with what is called overdrive (V_{OD}) and underdrive (V_{UD}) voltage levels (see section below).

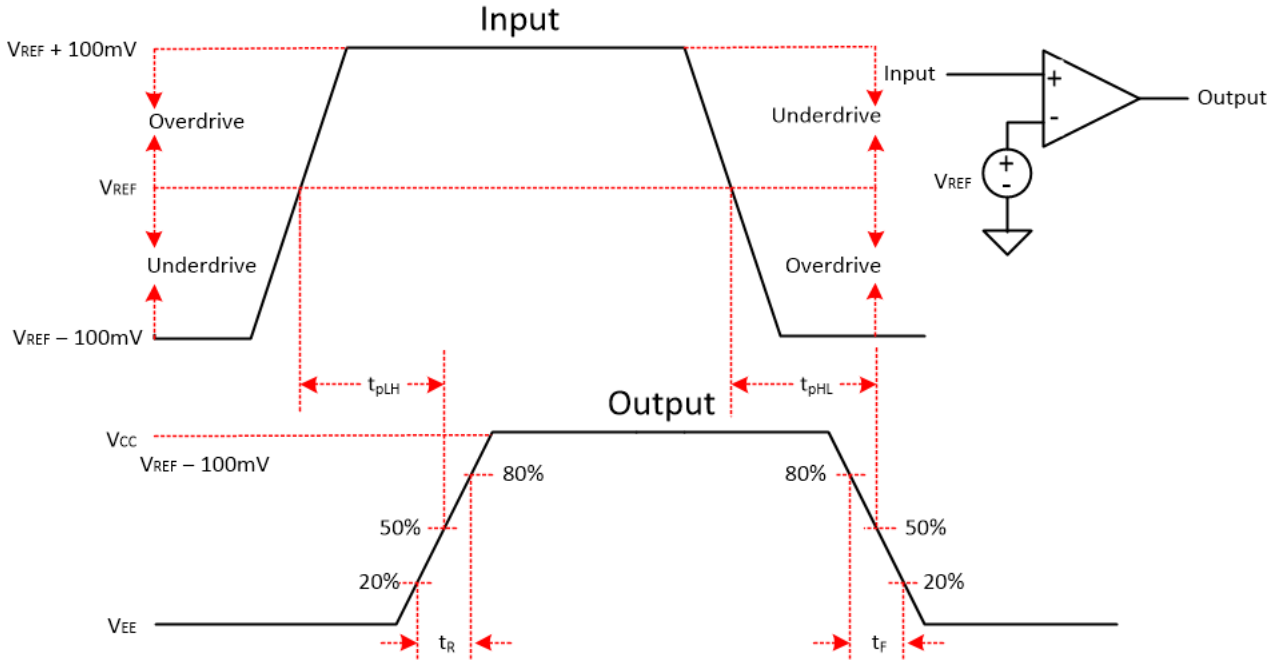

Figure 8-1. Comparator Timing Diagram

8.1.1.3 Overdrive and Underdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 8-1 example. Similarly, underdrive voltage, V_{UD}, is how far below REF the input starts. The overdrive and underdrive voltages influence the propagation delay (t_p). See curves in the Typical Characteristics section for more details. The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible. Contrary to overdrive voltage, larger underdrive voltage causes propagation delay to increase.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

8.2 Typical Applications

8.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. The figure below shows a simple window comparator circuit monitoring a 24V PLC power supply.

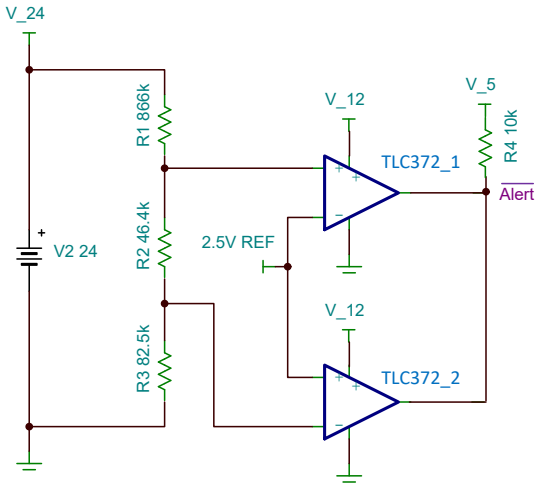

Figure 8-2. Window Comparator

8.2.1.1 Design Requirements

For this design, follow these design requirements:

- UV_Alert (logic low output) when the 24V supply is less than 19.2V
- OV_Alert (logic low output) when the 24V supply is greater than 30V
- Current dissipated in the resistor string is 30uA
- Comparator operates from the 5V supply
- 2.5V external reference is utilized

8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in the circuit above where the 2.5V REF from the TLC372 is used as the reference voltage and the resistor string of R1, R2, and R3 define the upper and lower threshold voltages for the 24V PLC power supply. When the comparator detects that the 24V supply has exceeded the maximum voltage of 30V or has drooped below the minimum voltage of 19.2V, OV_Alert and UV_Alert nets are pulled to a logic LOW state.

The first step is to determine the sum total resistance of the resistor string (R1, R2, R3) using the dissipation limit of 30uA. With a maximum operating voltage of 30V, the resistor string draws 30uA if the total resistance of R1+R2+R3 is 1Mohm.

The second step is to set the value of R3 such that the lower comparator changes output state from HIGH to LOW when the 24V supply reaches 30V. This is achieved when the voltage at the junction of R2 and R3 is equal

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to the reference voltage of 2.5V. Since 30uA is passing through the resistor string at 30V, R3 can be calculated from 2.5V / 30uA which is approximately 83.3kohms.

The third step is to set the value of R2 such that the upper comparator changes output state from HIGH to LOW when the 24V supply reaches 19.2V. This is achieved when the voltage at the junction of R1 and R2 is equal to the reference voltage of 2.5V. Since 19.2uA passes through the resistor string at 19.2V, R2 can be calculated from (2.5V /19.2uA) - R3 which is approximately 46.9kohms.

Lastly, the value of R1 is calculated from 1Mohm - (R2 + R3) which is approximately 870kohms. Please note that standard 1% resistor values were selected for the circuit

The respective comparator outputs (OV_Alert and UV_Alert) are LOW when the 24V PLC power supply is less than 19.2V or greater than 30V. Likewise, the respective comparator outputs are HIGH when the 24V supply is within the range of 19.2V to 30V (within the "window"), as shown below.

8.2.1.3 Application Curve

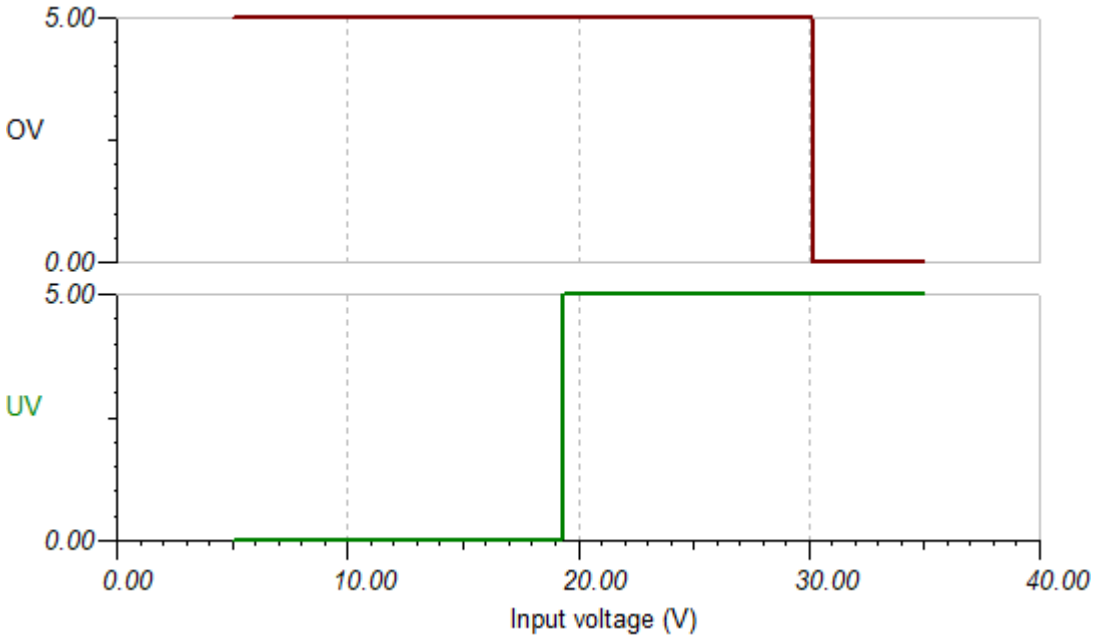

Figure 8-3. Window Comparator Results

8.3 Power Supply Recommendations

Due to the fast output edge rates, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between V+ pin and ground pins. Narrow, peak currents are drawn during the output transition time. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies (V+ and V-), or "single" supplies (V+ and GND), with GND applied to the V- pin. Input signals must stay within the specified input range (between V+ and V-) for either type. Note that with a "split" supply the output swings "low" (V_{OL}) to V- potential and not GND.

8.4 Layout

8.4.1 Layout Guidelines

For accurate comparator applications, a clean, stable power supply is important to minimize output glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The

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bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V+ and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V+ or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (≤100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

8.4.2 Layout Example

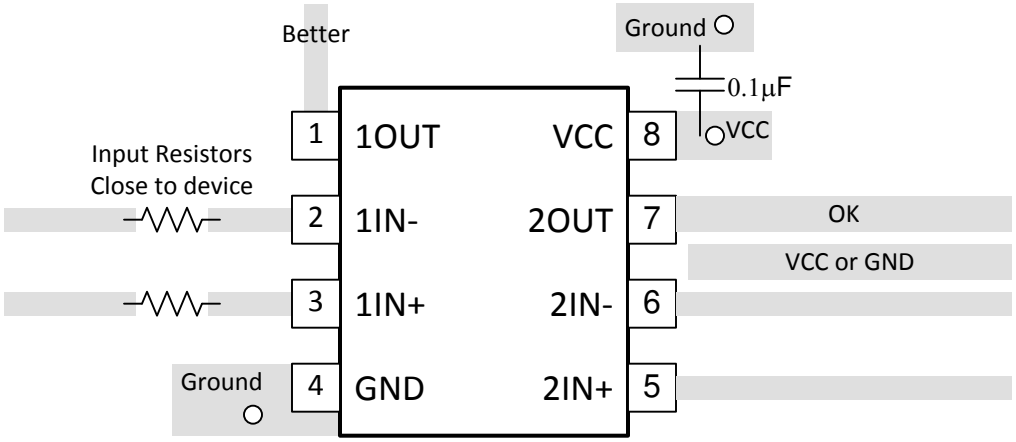

Figure 8-4. Dual Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (July 2008) to Revision F (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updates throughout data sheet to reflect performance of new die	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-87658012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87658012A TLC372MFKB
5962-8765801PA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8765801PA TLC372M
5962-9554901NXD	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q372M
5962-9554901NXDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q372M
5962-9554901NXDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	Q372M
TLC372CD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	372C
TLC372CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	372C
TLC372CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	372C
TLC372CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC372CP
TLC372CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC372CP
TLC372CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P372
TLC372CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P372
TLC372CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P372
TLC372CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P372
TLC372CPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	0 to 70	P372
TLC372CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P372
TLC372CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	P372
TLC372IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	372I
TLC372IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	372I
TLC372IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLC372IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC372IP
TLC372IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC372IP
TLC372MD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-55 to 125	
TLC372MDG4	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-	
TLC372MDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	372M
TLC372MDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	372M
TLC372MDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	372M

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC372MDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	372M
TLC372MFKB	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87658012A TLC372MFKB
TLC372MFKB.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-87658012A TLC372MFKB
TLC372MJG	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC372MJG
TLC372MJG.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC372MJG
TLC372MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8765801PA TLC372M
TLC372MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8765801PA TLC372M
TLC372MP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	TLC372MP
TLC372MP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	TLC372MP
TLC372MUB	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC372MUB
TLC372MUB.A	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	TLC372MUB
TLC372QD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	
TLC372QDG4	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	
TLC372QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	372Q
TLC372QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	372Q
TLC372QDRG4	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	372Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLC372, TLC372M :

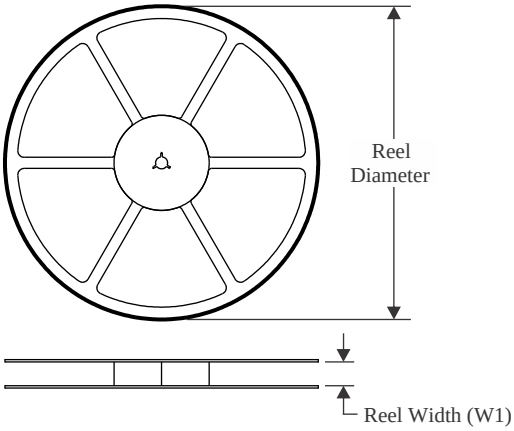
- Catalog : TLC372
- Enhanced Product : TLC372-EP, TLC372-EP
- Military : TLC372M

NOTE: Qualified Version Definitions:

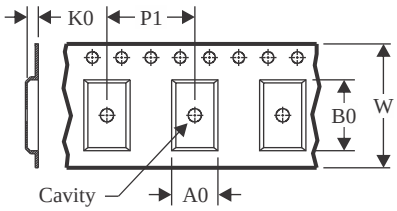
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

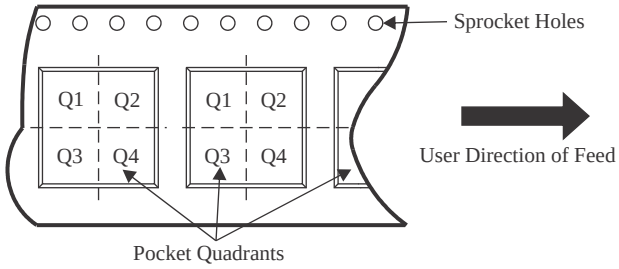


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

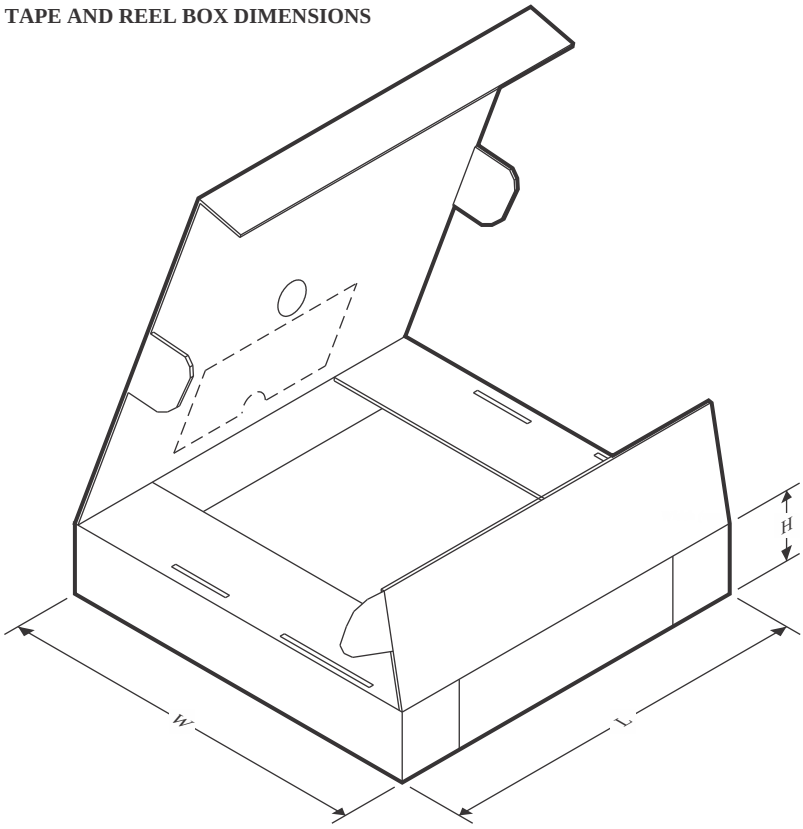
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
5962-9554901NXDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC372CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC372CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC372CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TLC372CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLC372IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC372IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC372MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC372MDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC372QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

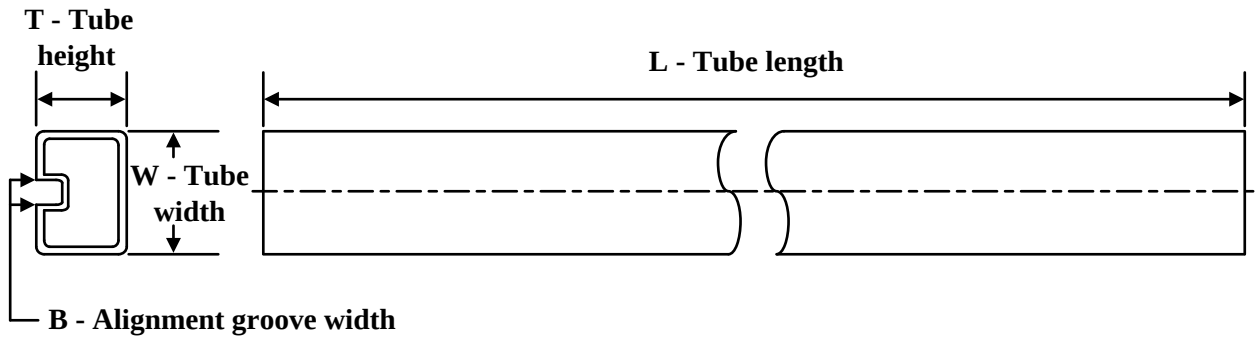
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
5962-9554901NXDR	SOIC	D	8	2500	350.0	350.0	43.0
TLC372CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC372CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC372CPSR	SO	PS	8	2000	353.0	353.0	32.0
TLC372CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLC372IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC372IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC372MDR	SOIC	D	8	2500	340.5	338.1	20.6
TLC372MDRG4	SOIC	D	8	2500	340.5	338.1	20.6
TLC372QDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

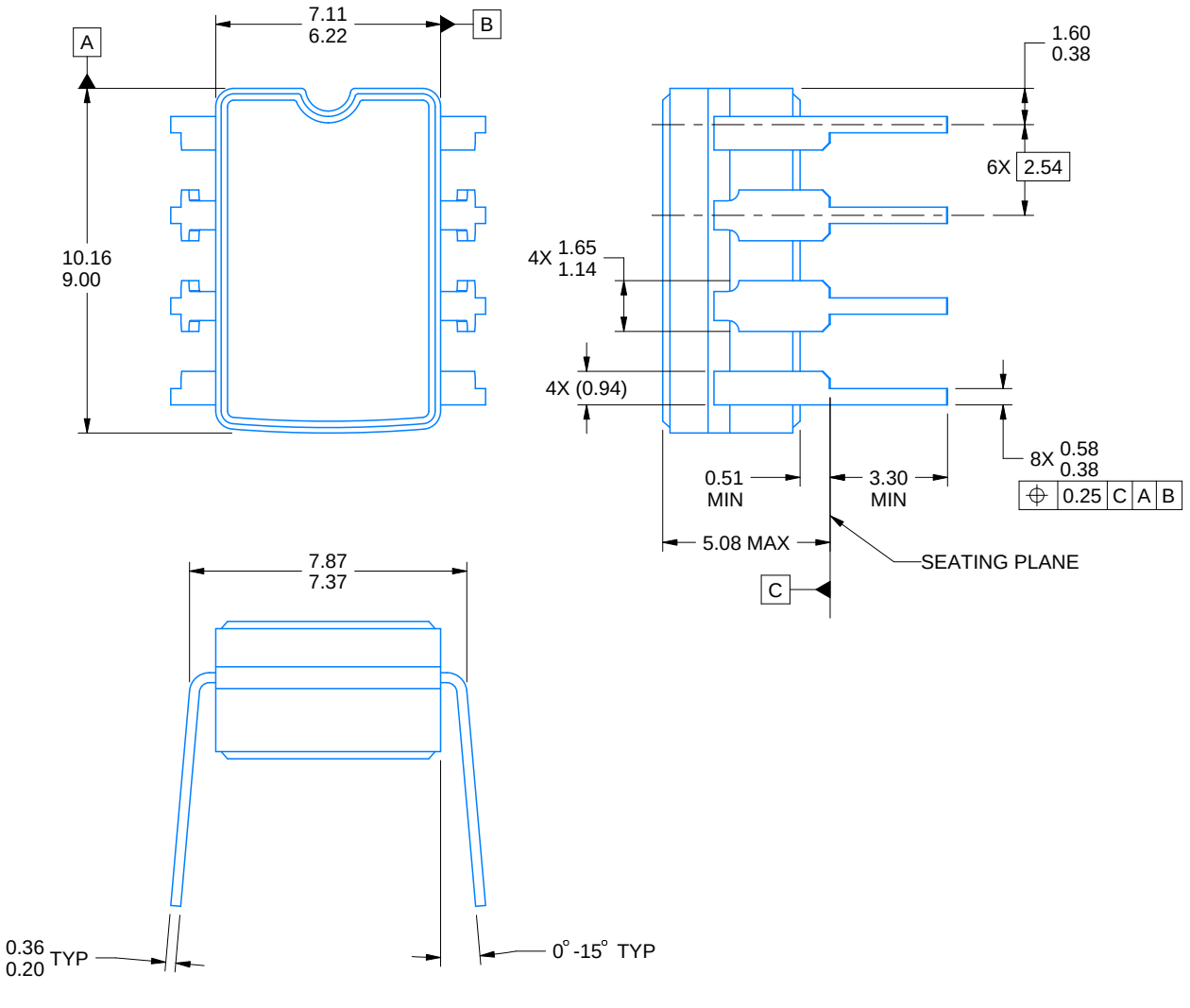
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-87658012A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC372CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC372CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC372CPS	PS	SOP	8	80	530	10.5	4000	4.1
TLC372CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TLC372IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC372IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC372MFKB	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC372MFKB.A	FK	LCCC	20	55	506.98	12.06	2030	NA
TLC372MP	P	PDIP	8	50	506	13.97	11230	4.32
TLC372MP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC372MUB	U	CFP	10	25	506.98	26.16	6220	NA
TLC372MUB.A	U	CFP	10	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

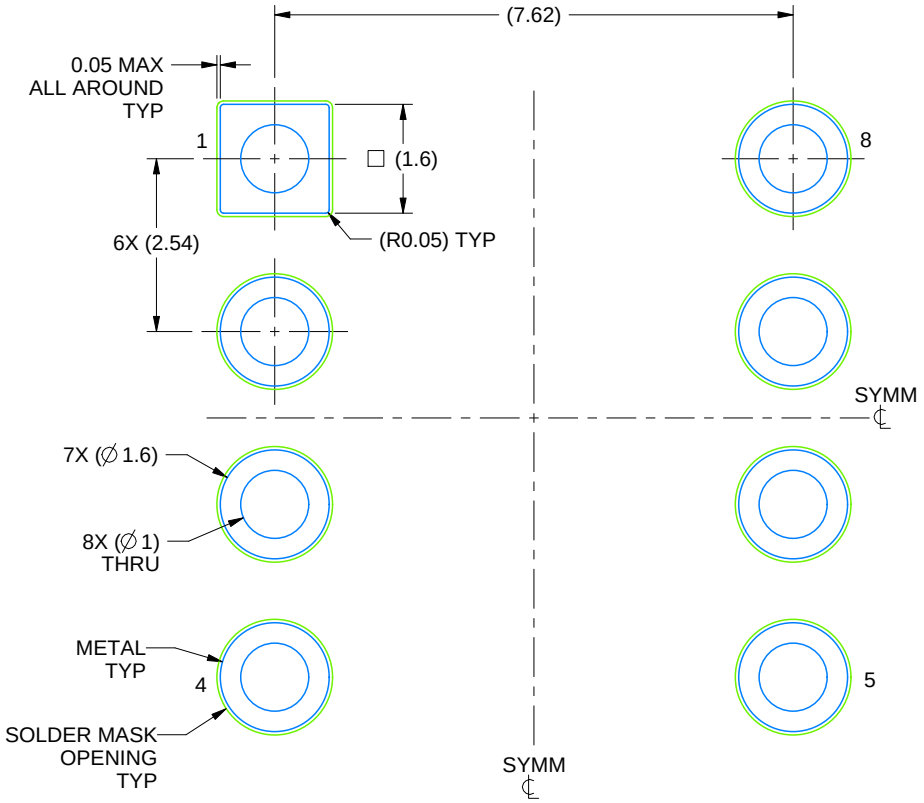
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

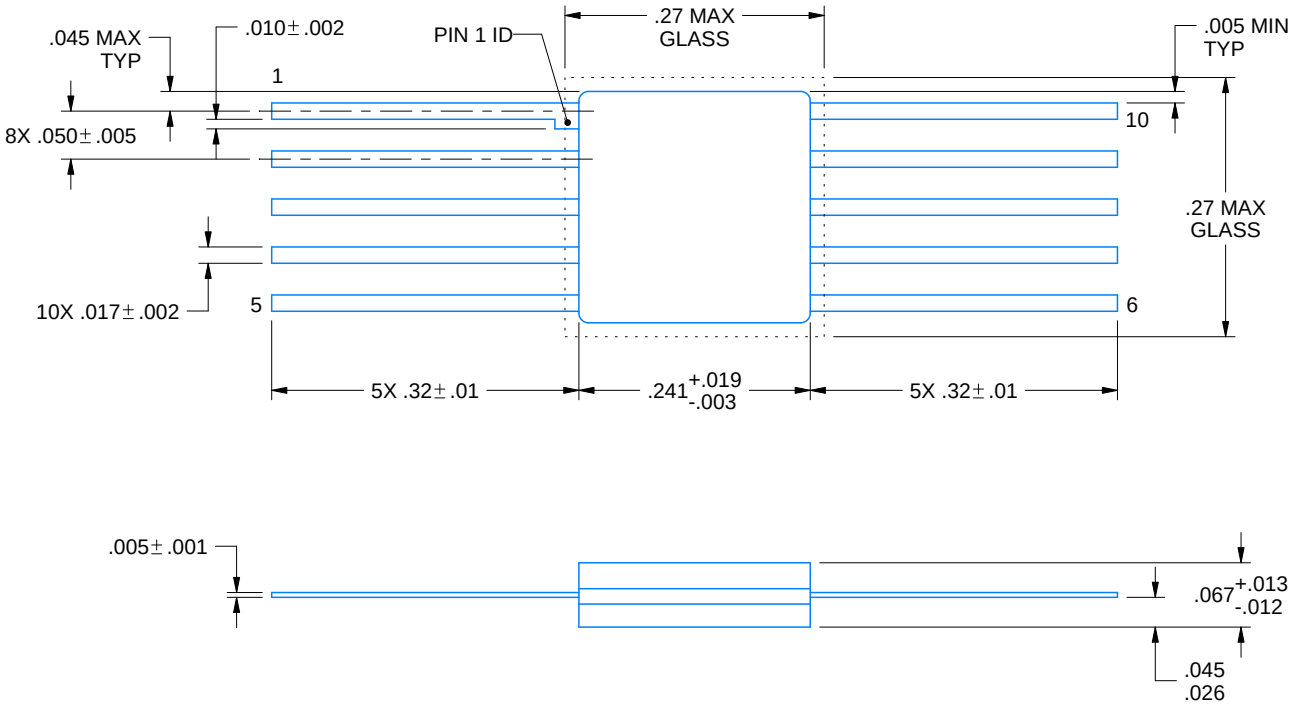
4230036/A 09/2023

U0010A

PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4225582/A 01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

GENERIC PACKAGE VIEW

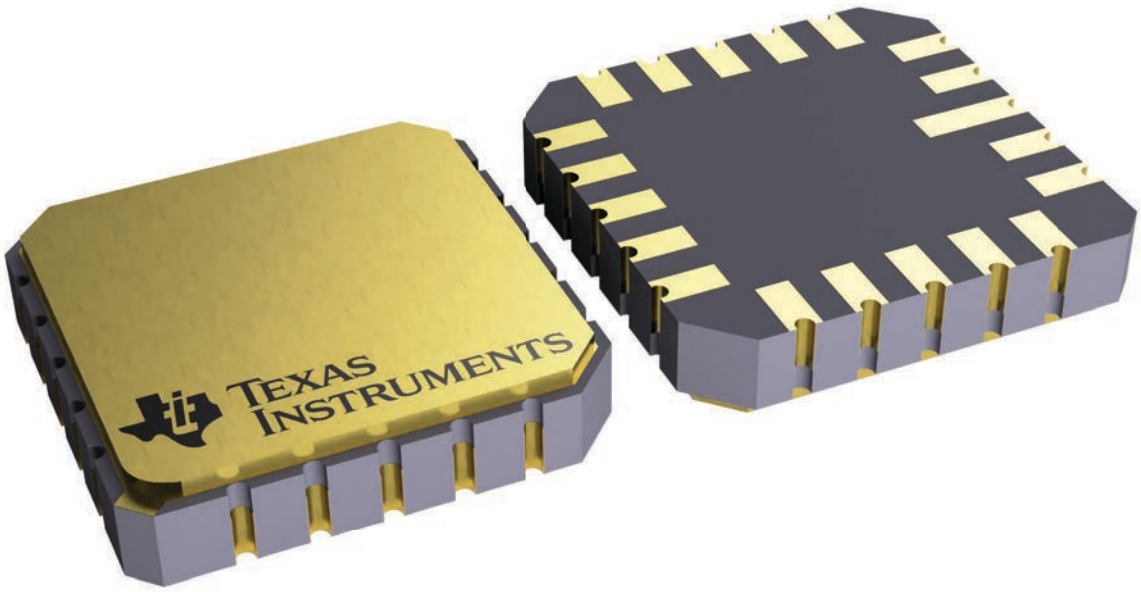
FK 20

LCCC - 2.03 mm max height

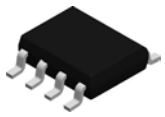
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

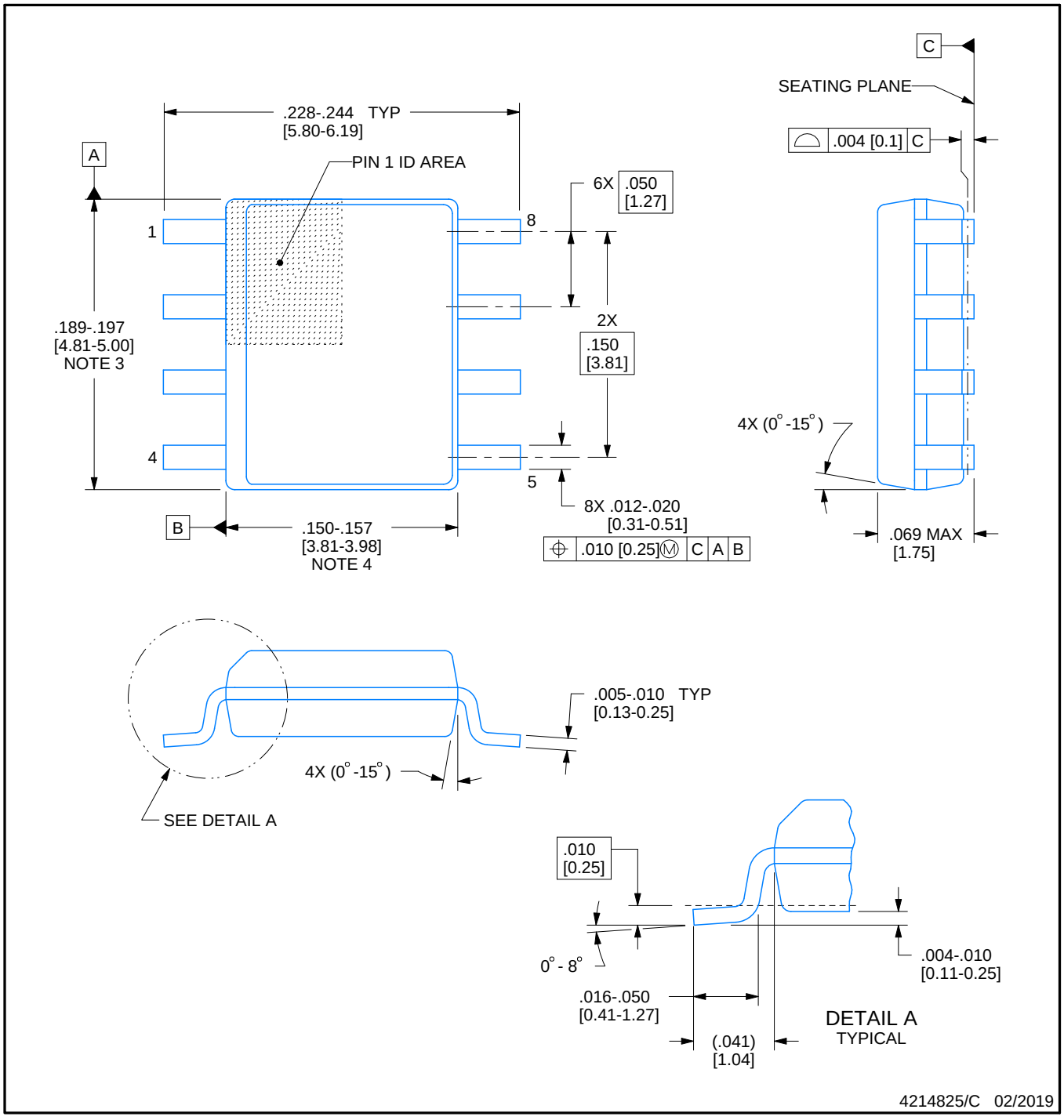


PACKAGE OUTLINE

D0008A

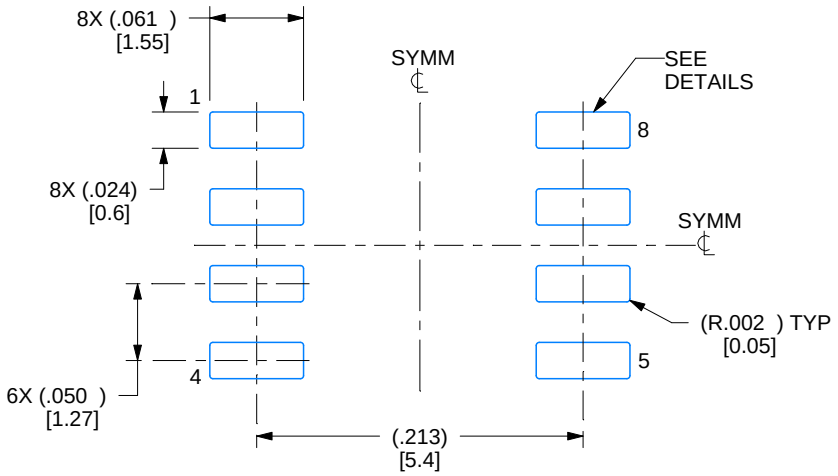
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

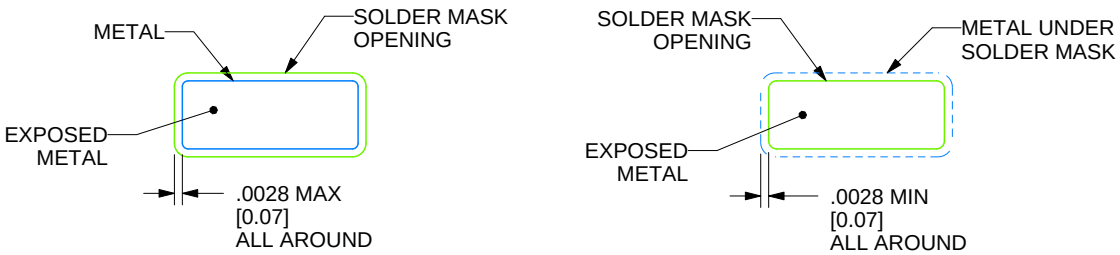


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

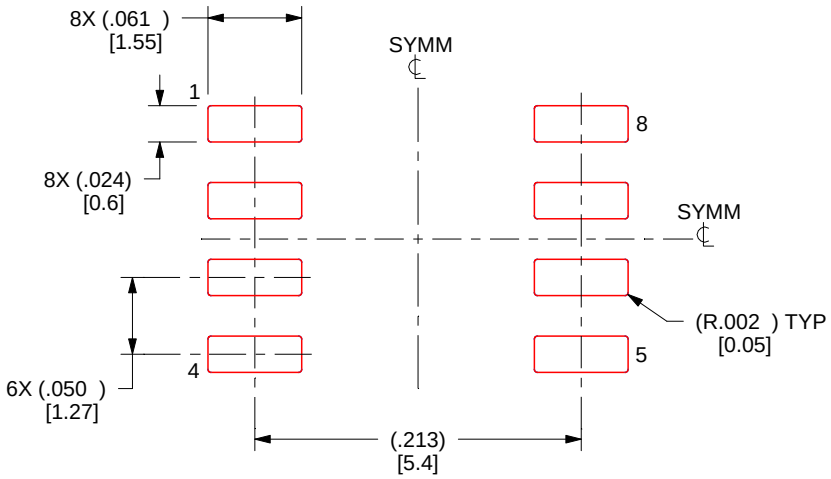
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

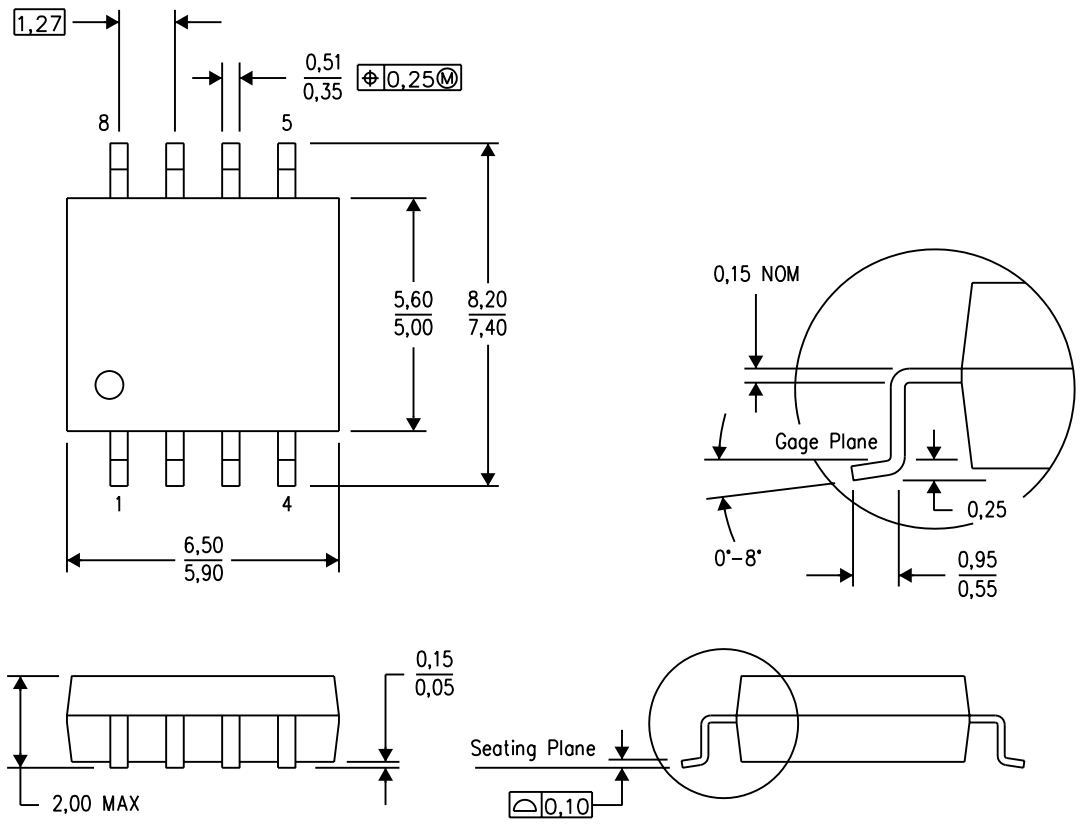
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

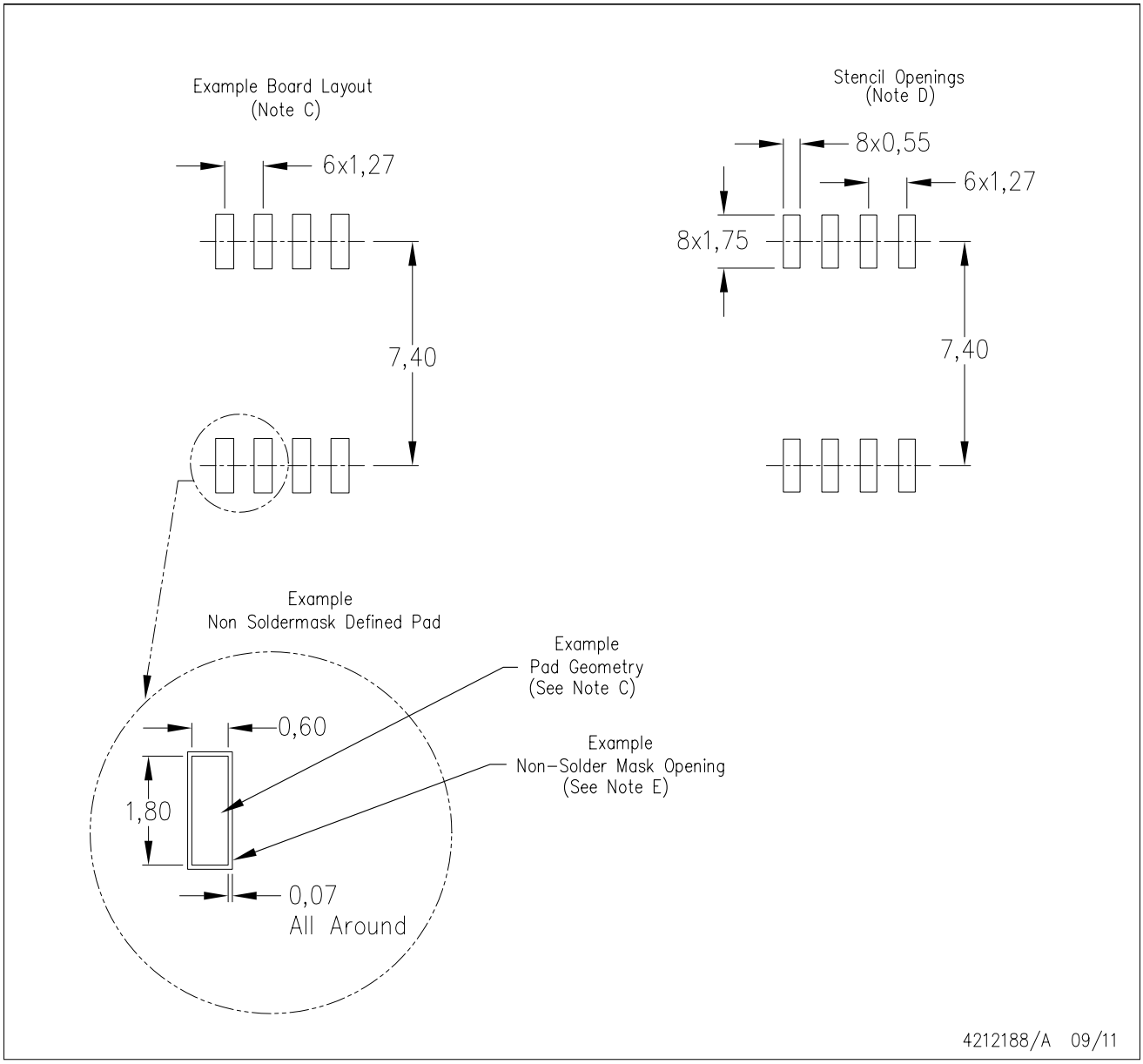
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

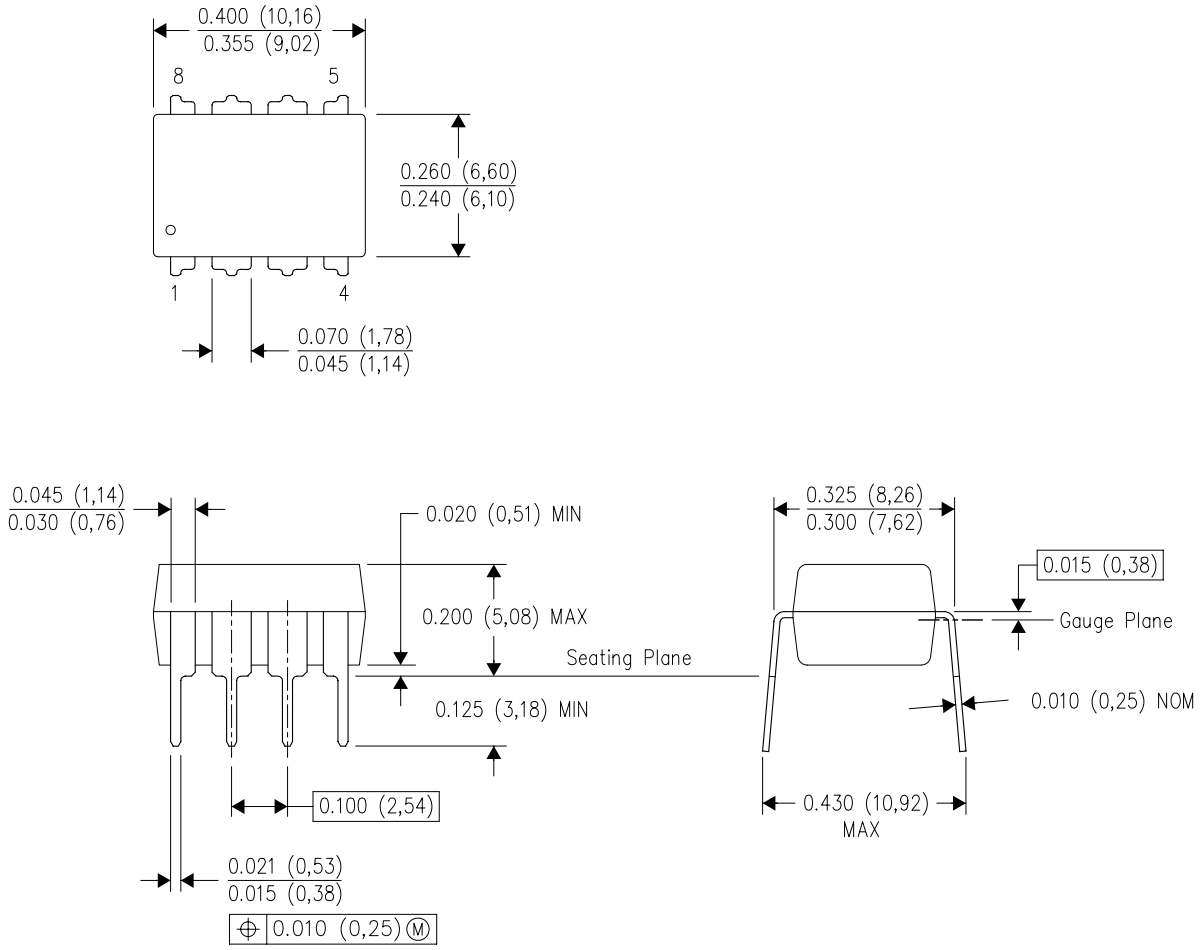
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



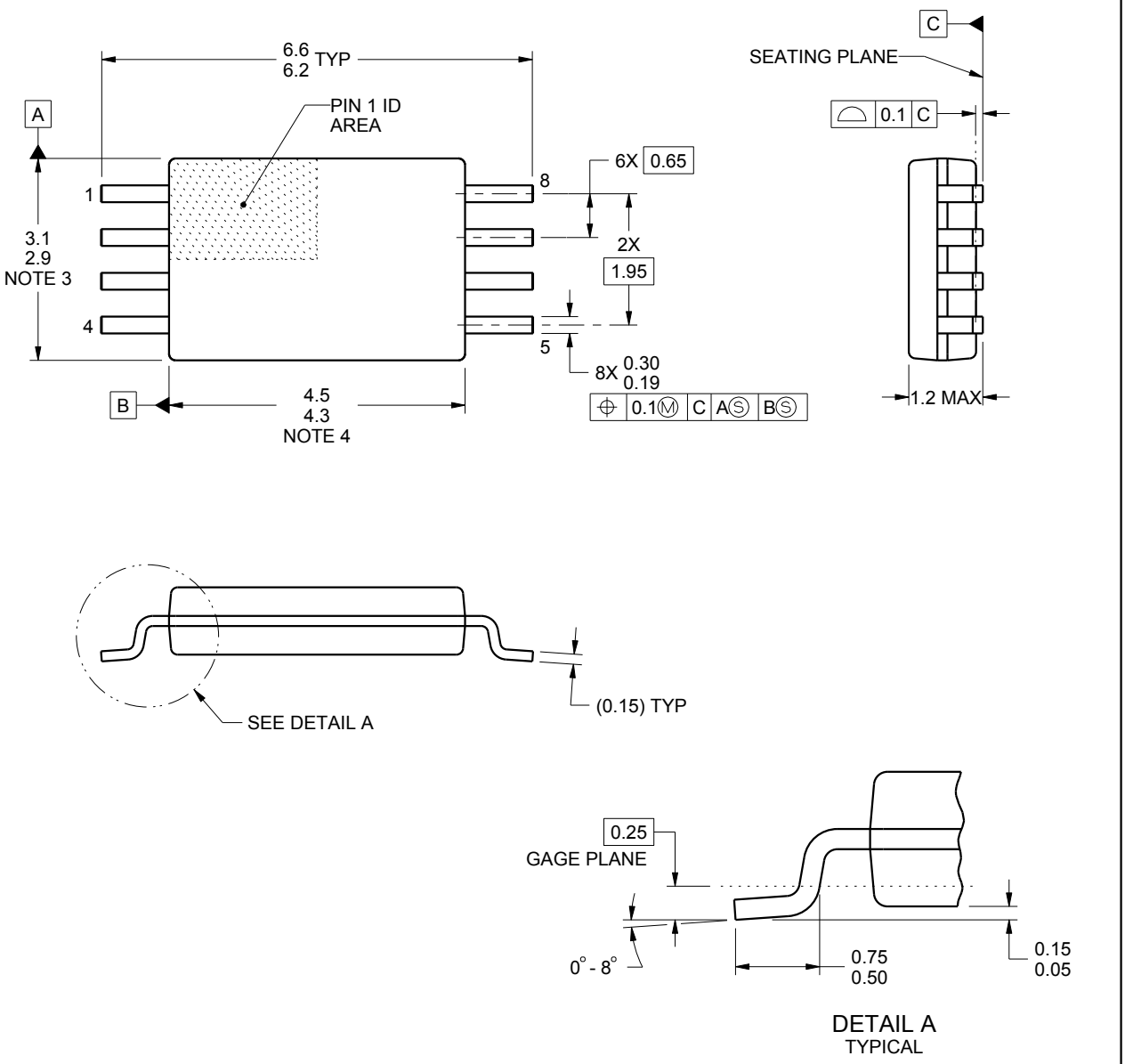
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

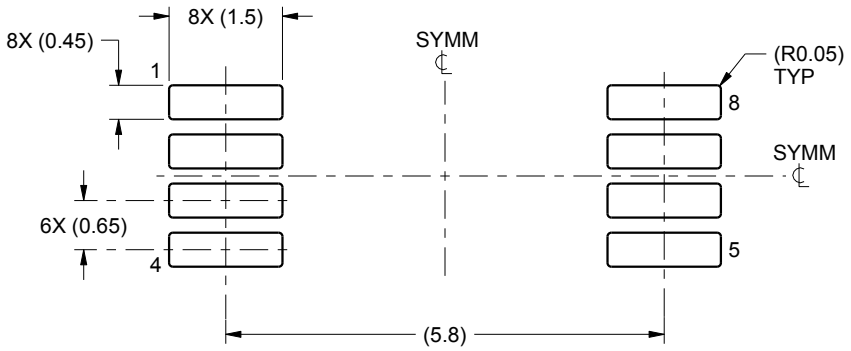
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

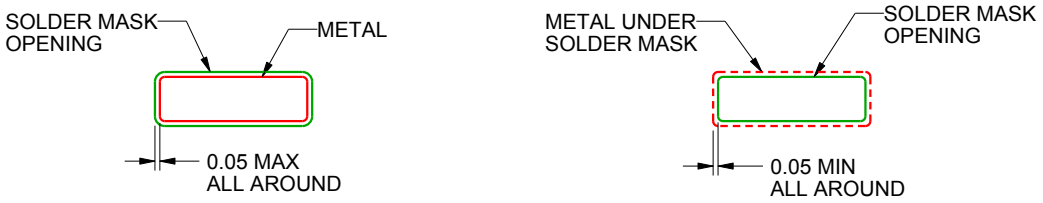


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

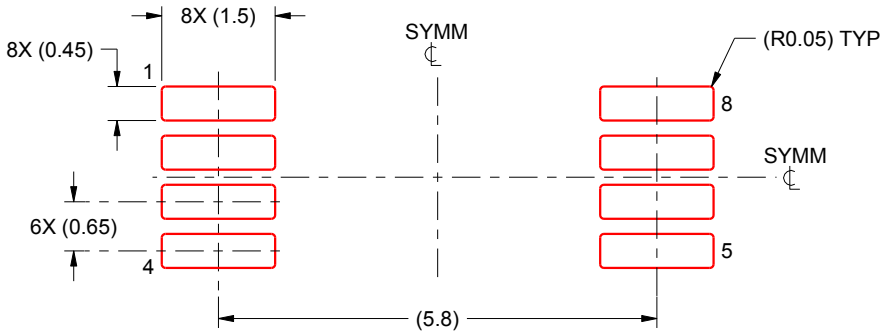


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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