TLIN1124A-Q1 Automotive Quad Local Interconnect Network (LIN) Transceiver with Integrated Commander Pull-up Resistor and Inhibit

1 Features

- AEC-Q100 Qualified for automotive applications
- Compliant to LIN2.0, LIN2.1, LIN2.2, LIN2.2A and ISO 17987–4 electrical physical layer (EPL) specification
- Compliant to SAE J2602-1 LIN Network for vehicle applications
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Wide input operational voltage range
  - V_{SUP} range from 5V to 28V
- LIN transmit data rate up to 20kbps
- LIN receive data rate up to 100kbps
- Operating modes: Normal, Standby and Sleep
- Low-power mode wake-up support with source recognition
  - Remote wake-up over the LIN bus
  - Local wake-up via SLP
- 4 LIN channels in one package with Integrated diode and commander pull-up resistor (±6% tolerant pull-up in normal mode)
- Tighter responder pull-up (27k to 48k) integrated for all 4 LIN channels
- INHN pin to control external power regulator
- 2.97V to 5.5V V_{io} logic interface support
- Power-up/down glitch-free operation on LIN bus and RXD output
- Protection features:
  - Bus-Fault Protection ±40V
  - Under voltage protection on V_{SUP} and V_{IO}
  - TXD dominant time out protection to prevent the faulty channel from occupying bus for extended duration
  - LIN dominant timeout protection to prevent excess on-chip power dissipation
  - Thermal shutdown protection
  - Unpowered node or ground disconnection fail-safe at system level.
- Junction temperatures from -40°C to 150°C
- 3.5mm × 5.5mm QFN package with improved automated optical inspection (AOI) capability

2 Applications

- Body electronics and lighting
- Automotive infotainment and cluster
- Hybrid electric vehicles and powertrain systems
- Industrial transportation

3 Description

The TLIN1124A-Q1 device is a quad Local Interconnect Network (LIN) physical layer transceiver with integrated commander and responder termination, inhibit, wake-up and protection features, complaint to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO/DIS 17987-4 and SAE J2602-1 standards.

LIN is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20kbps. The LIN receiver supports data rates up to 100kbps for in-line programming.

The TLIN1124A-Q1device supports 12V battery applications with wider operating voltage (5V to 28V) and extended LIN bus-fault (±40V) protection. The device converts the LIN protocol data stream on the TXDx input into a LINx bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the push-pull RXD output pin. Ultra-low current consumption is possible using the sleep mode which allows wake up via LIN bus or SLP pin.

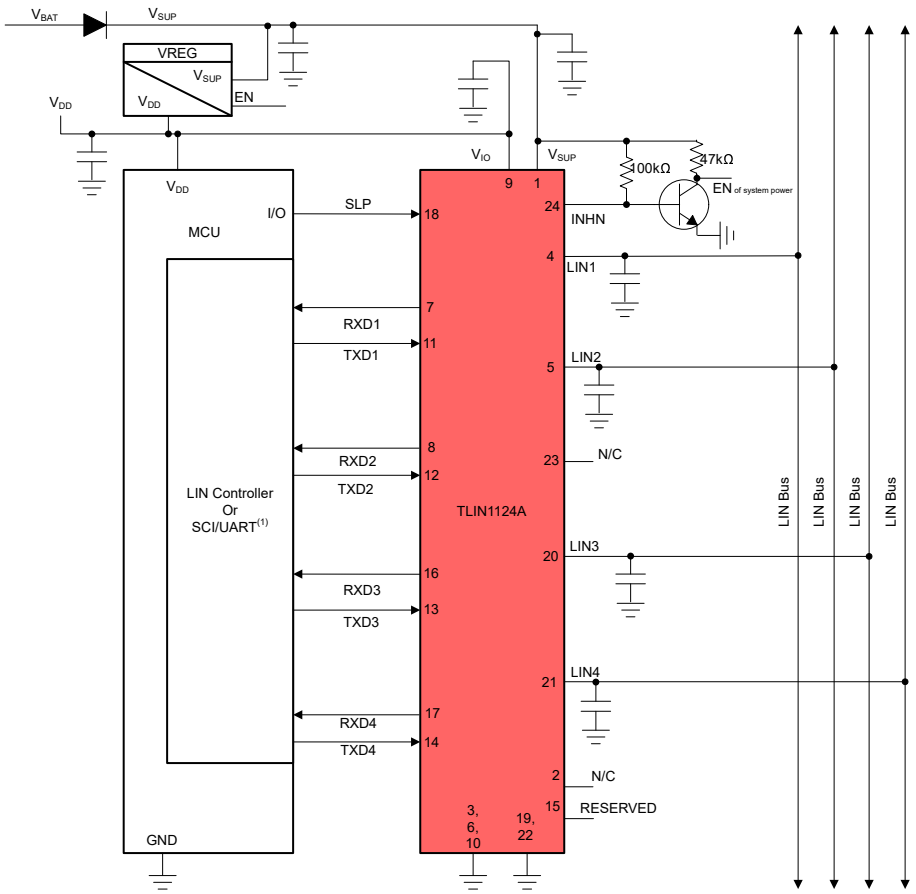
The integrated commander and responder diode and resistor, electrostatic discharge (ESD) protection, and fault protection allow designers to save board space in the system. The device prevents back-feed current through LIN to the supply if the ground shift or supply voltage is disconnected.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLIN1124A-Q1	VQFN (24)	5.5mm × 3.5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ADVANCE INFORMATION



Decoupling capacitor values are system dependent but usually have 100nF, 1µF and ≥10µF

Simplified Schematic

Table of Contents

ADVANCE INFORMATION

ADVANCE INFORMATION

4 Pin Configuration and Functions

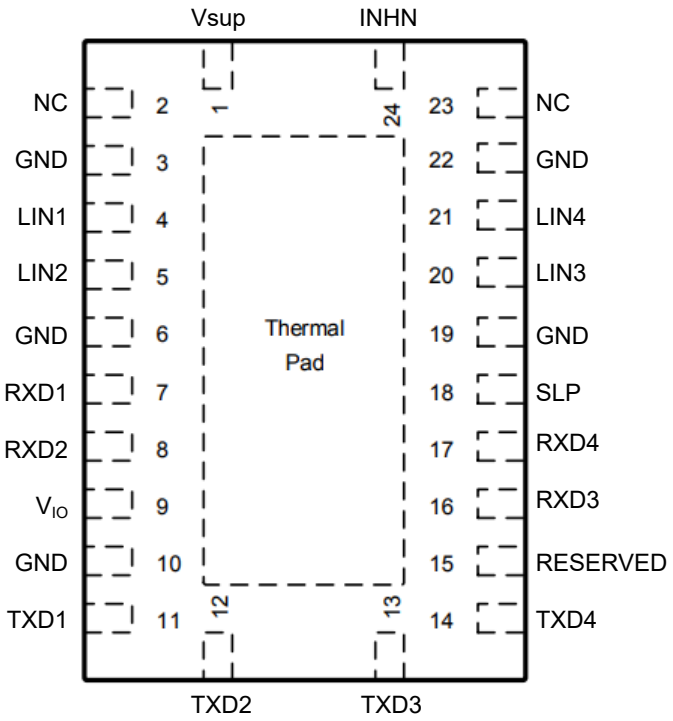


Figure 4-1. RGY Package, 24-Pin (VQFN)
Top View

Table 4-1. Pin Functions

PIN[1]		TYPE	DESCRIPTION
NO.	NAME		
1	V_{SUP}	Power	High voltage supply from battery
2	NC	-	Not connected
3	GND	GND	Ground
4	LIN1	Bus I/O	Channel 1 LIN Bus single-wire transmitter and receiver
5	LIN2	Bus I/O	Channel 2 LIN Bus single-wire transmitter and receiver
6	GND	GND	Ground
7	RXD1	Digital Output	Channel 1 RXD Output (push-pull) interface reporting state of LIN1 bus
8	RXD2	Digital Output	Channel 2 RXD Output (push-pull) interface reporting state of LIN2 bus
9	V_{IO}	Power	Logic interface supply voltage
10	GND	GND	Ground
11	TXD1	Digital Input	Channel 1 TXD input interface to control state of LIN1 output; integrated weak pull-down and pull-up;
12	TXD2	Digital Input	Channel 2 TXD input interface to control state of LIN2 output; integrated weak pull-down and pull-up;
13	TXD3	Digital Input	Channel 3 TXD input interface to control state of LIN3 output; integrated weak pull-down and pull-up;
14	TXD4	Digital Input	Channel 4 TXD input interface to control state of LIN4 output; integrated weak pull-down and pull-up;
15	RESERVED	Digital Input	For normal operation. This pin must be driven low or connected to GND
16	RXD3	Digital Output	Channel 3 RXD Output (push-pull) interface reporting state of LIN3 bus
17	RXD4	Digital Output	Channel 4 RXD Output (push-pull) interface reporting state of LIN4 bus
18	SLP	Digital input	Logic input to control state of LIN channels, integrated pull-up to V_{IO}
19	GND	GND	Ground
20	LIN3	Bus I/O	Channel 3 LIN Bus single-wire transmitter and receiver
21	LIN4	Bus I/O	Channel 4 LIN Bus single-wire transmitter and receiver
22	GND	GND	Ground
23	NC	-	Not connected
24	INHN	High voltage output	Inhibit output to control system voltage, high voltage. Active low, open drain.
PAD	Thermal pad	-	Must be grounded on PCB for optimum thermal performance

(1) Pin 3, 6, 10, 19 and 22: All GND pins are shorted internally.

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{SUP}	Supply voltage range	–0.3	40	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{LIN}	LIN Bus input voltage	–40	40	V
V_{INHN}	INHN pin output voltage	–0.3	V_{SUP} + 0.3	V
V_{LOGIC_INPUT}	Logic input voltage (TXDx, SLP)	–0.3	V_{IO} + 0.3	V
V_{LOGIC_OUTPUT}	Logic output voltage (RXDx)	–0.3	V_{IO} + 0.3	V
I_O	Digital pin output current (RXDx)		8	mA
$I_{O(INHN)}$	Inhibit terminal input current		4	mA
T_J	Junction Temp	–40	165	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM) classification level 3B: V_{SUP}, LIN, INHN with respect to ground		±8000	V
		Human body model (HBM) classification level 3A: all other pins, per AEC Q100-002(1)		±2000	
		Charged device model (CDM) classification level C5, per AEC Q100-011	All pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 ESD Ratings - IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge according to IEC 62228-2 for LIN (1)	Contact discharge on LIN, V_{SUP} with respect to GND	±8000	V
		Indirect ESD discharge on LIN	±15000	
$V_{(ESD)}$	Electrostatic discharge according to SAE J2962-1 for LIN (2)	Contact discharge on LIN	±8000	V
		Air-gap discharge on LIN	±25000	V
V_{TRAN}	IEC 62228-2 Pulse transients per IEC 62215-3 12 V electrical systems LIN, V_{SUP} terminal to GND(1)	Pulse 1	-100	V
		Pulse 2	75	
		Pulse 3a	-150	
		Pulse 3b	100	
	LIN terminal to GND(2)	SAE J2962-1 per ISO 7637-3 Direct Coupling Capacitor - Slow transient pulse	±30	

(1) Results given here are specific to the IEC 62228-2. Testing performed by OEM approved independent third party
(2) Results given here are specific to the SAE J2962-1. Testing performed by OEM approved independent third party

5.4 Recommended Operating Conditions

parameters valid across -40℃ ≤ T_J ≤ 150℃ (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{SUP}	Supply Voltage	5		28	V
V_{IO}	Logic interface supply voltage	2.97		5.5	V
V_{LIN}	LIN Bus input voltage	0		28	V
V_{LOGIC}	Logic Pin Voltage (TXDx, RXDx, SLP)	0		V_{IO}	V
$I_{OH(DO)}$	Digital output (RXDx) high level current, V_{IO} = 3V to 3.6V, 4.5V to 5.5V	–4			mA
$I_{OL(DO)}$	Digital output (RXDx) low level current, V_{IO} = 3V to 3.6V, 4.5V to 5.5V			4	mA
$I_{O(INHN)}$	Inhibit pin input current			2	mA
T_J	Operating virtual junction temperature range	-40		150	°C
T_{SDR}	Thermal shutdown rising	160			°C
T_{SDF}	Thermal shutdown falling			140	°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis		25		°C

5.5 Thermal Information

THERMAL METRIC[1]		TLIN1124ARGYRQ1 VQFN 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

5.6 Power Supply Characteristics

parameters valid across -40°C ≤ T_J ≤ 150°C, V_{SUP} = 5V to 28V, V_{IO} = 2.97V to 5.5V, Typical values are at V_{SUP} = 12V, V_{IO} = 3.3V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage and Current						
V_{SUP}	Operating voltage range	LIN signal 10khz square wave 50% duty cycle with 28V swing.	5		28	V
I_{SUP}	Supply current Bus dominant	TLIN1124A Normal mode LIN1 (dominant) = 0V, other 3 channels recessive, V_{SLP} = 0V, INHN = Floating, V_{TXDx} = V_{IO}		TBD	38	mA
I_{SUP}	Supply current Bus dominant	TLIN1124A Normal mode All LIN bus (dominant) = 0V, V_{SLP} = 0V, INHN = Floating, V_{TXDx} = V_{IO}		80	150	mA
	Supply current, device dominant	TLIN1124A Normal mode V_{TXD1} = 0V, Other channels recessive, V_{SLP} = 0V, INHN = floating		TBD	40	mA
	Supply current, device dominant	TLIN1124A Normal mode V_{TXDx} = 0V, all channels driving dominant, V_{SLP} = 0V, INHN = floating		TBD	150	mA
I_{SUP}	Supply current Bus recessive	TLIN1124A, Normal mode, V_{TXDx} = V_{IO}, V_{SLP} = 0V, V_{LINx} = V_{SUP}, INHN = Float		TBD	1.7	mA
I_{SUP}	Supply current Bus recessive	TLIN1124A, Standby mode INHN = Float, V_{LINx} = V_{SUP}		TBD	150	µA
I_{SUP}	Supply current Sleep mode	TLIN1124A, T_J ≤ 125°C V_{SLP} = V_{IO}, V_{LINx} = V_{SUP}		TBD	20	µA
I_{IO}	Supply current logic pin V_{IO}	Sleep mode, TXDx floating, T_J ≤ 85°C		5	6	µA
		Sleep mode, TXDx floating, T_J ≤ 125°C		TBD	9	µA
		Normal mode, V_{TXDx} = V_{IO}		TBD	125	µA
$UV_{SUP-rising}$	Under voltage V_{SUP} threshold	rising		4.6	4.9	V
$UV_{SUP-falling}$	Under voltage V_{SUP} threshold	falling	4.1	4.45		V
$UV_{SUP-falling\_sleep}$	Under voltage V_{SUP} threshold in sleep mode. Transitions from sleep mode to low voltage sleep mode (recovery time of 650us needed to transition out of low voltage sleep mode)	falling	4.1	4.45		V
$UV_{SUP-falling\_LVsleep}$	Under voltage V_{SUP} threshold in sleep mode. Transitions from low voltage sleep mode to OFF mode	falling	1.9	2.4	3.1	V
$UV_{SUP-HYS}$	Hysteresis voltage for V_{SUP} under voltage threshold		80	130		mV
$UV_{VIO-rising}$	Under voltage on V_{IO}	rising	2.5	2.65	2.8	V
$UV_{VIO-falling}$	Under voltage on V_{IO}	falling	2.4	2.5	2.6	V
$UV_{VIO-hys}$	Hysteresis voltage for V_{IO} under voltage threshold		80	100		mV

ADVANCE INFORMATION

5.7 Electrical Characteristics

parameters valid across entire recommended range of V_{SUP}, V_{IO} and Junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RXDx Output Terminal						
V_{OH}	High level output voltage	I_O = -4mA, Normal mode, V_{IO} = 2.97V to 3.6V, 4.5V to 5.5V	V_{IO}-0.4			V
V_{OL}	Low-level voltage	I_O = 4mA, Normal mode, V_{IO} = 2.97V to 3.6V, 4.5V to 5.5V			0.4	V
R_{PU}	Pull-up resistor	Low power mode	38	60	88	kΩ
I_{LKG}	Off state leakage current	V_{SUP} =0, V_{RXDx} = V_{IO}	–5		5	µA
TXDx Input Terminal						
V_{IL}	Low-level input voltage				0.3*V_{IO}	V
V_{IH}	High-level input voltage		0.7*V_{IO}		V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{IO} = 5.5V		16	50	µA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{IO} = 5.5V	-2		2	µA
$I_{LKG(OFF)}$	Off state input leakage current	TXD = 5.5V, V_{SUP} = V_{IO} = 0V			120	µA
R_{TXD_PD}	Internal pull-down resistor value	V_{TXD} < 0.25 VIO	38	60	88	kΩ
R_{TXD_PU}	Internal pull-up resistor value	V_{TXD} > 0.75 VIO	38	60	88	kΩ
SLP Input Terminal						
V_{IL}	Low-level input voltage				0.3*V_{IO}	V
V_{IH}	High-level input voltage		0.7*V_{IO}		V_{IO}	V
I_{IH}	High-level input leakage current	SLP = V_{IO} = 5.5V	-2		2	µA
I_{IL}	Low-level input leakage current	SLP = 0V, V_{IO} = 5.5V	-125			µA
R_{SLP}	Internal pull-up resistor to V_{IO} on SLP terminal		38	60	88	kΩ
LINx Terminal						
$V_{SUP\_NON\_OP}$	V_{SUP} range where impact to recessive LIN bus < 5%[2]	V_{TXDx} = V_{IO}, 5V ≤ V_{LIN} ≤ 28V, Normal mode	–0.3		40	V
V_{OH}	LIN recessive high-level output voltage[2]	V_{TXDx} = V_{IO}, Normal mode 5V ≤ V_{SUP} < 7V $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON	3			V
V_{OH}	LIN recessive high-level output voltage[2]	V_{TXDx} = V_{IO}, 7 V ≤ V_{SUP} ≤ 28 V, Normal mode $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON	0.85			V_{SUP}
V_{OH}	LIN recessive high-level output voltage[1]	V_{TXDx} = V_{IO}, 7V ≤ V_{SUP} ≤ 28V, Normal mode TLIN1124A (commander termination enabled)	0.8			V_{SUP}
V_{OH}	LIN recessive high-level output voltage	V_{TXDx} = V_{IO}, 7V ≤ V_{SUP} ≤ 28V, Normal mode $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON	0.8			V_{SUP}
V_{OL}	LIN dominant low-level output voltage[2]	V_{TXDx} = 0V, Normal mode 5V ≤ V_{SUP} < 7V $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON			1.2	V
V_{OL}	LIN dominant low-level output voltage[2]	V_{TXDx} = 0V, Normal mode 7V ≤ V_{SUP} ≤ 28V $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage[1]	V_{TXDx} = 0V, Normal mode 7V ≤ V_{SUP} ≤ 28V TLIN1124A (commander termination enabled)			0.2	V_{SUP}
V_{OL}	LIN dominant low-level output voltage	$R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON			0.2	V_{SUP}
V_{BUSdom}	Receiver Low-level input voltage	Receiver dominant state (including LIN dominant for wake up)			0.4	V_{SUP}
V_{BUSrec}	Receiver High-level input voltage	Receiver recessive state	0.6			V_{SUP}
V_{IH}	Receiver High voltage (recessive) input threshold[1]	5V ≤ V_{SUP} ≤ 28V	0.47		0.6	V_{SUP}
V_{IL}	Receiver Low voltage (dominant) input threshold[1]	5V ≤ V_{SUP} ≤ 28V	0.4		0.53	V_{SUP}
V_{BUS_CNT}	Receiver center threshold [3]	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2, Normal Mode, 7V ≤ V_{SUP} ≤ 28V	0.475	0.5	0.525	V_{SUP}

ADVANCE INFORMATION

parameters valid across entire recommended range of V_{SUP}, V_{IO} and Junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS_CNT}	Receiver center threshold (3)	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$, Normal Mode, $5V \le V_{SUP} \le 7V$	0.45	0.5	0.55	V_{SUP}
V_{BUS_CNT}	Receiver center threshold (3)	$5V \le V_{SUP} \le 28V$, $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec})/2$	0.47	0.5	0.54	V_{SUP}
V_{HYS}	Hysteresis voltage (ISO 17987) (3)	$5V \le V_{SUP} \le 28V$, $V_{HYS} = V_{th\_rec} - V_{th\_dom}$			0.175	V_{SUP}
V_{HYS}	Hysteresis voltage (SAE J2602)	$5V \le V_{SUP} \le 28V$, $V_{HYS} = V_{IH} - V_{IL}$	0.07		0.175	V_{SUP}
V_{SERIAL_DIODE}	Serial diode LIN commander and responder termination pull-up path (5)	I_{SERIAL_DIODE} = 10µA for $R_{RESPONDER}$, 1mA for $R_{COMMANDER}$	0.4	0.7	1.0	V
$I_{BUS(LIM)}$	Limiting current for driver dominant state	V_{TXD} = 0V, V_{LIN} = 18V, V_{SUP} = 18V, $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON	40	90	200	mA
$I_{BUS\_PAS\_dom}$	Input leakage current at receiver including pull-up resistor, bus dominant	Driver off, V_{LIN} = 0V, $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON V_{SUP} = 12V	–1			mA
$I_{BUS\_PAS\_dom}$	Input leakage current at receiver including pull-up resistor, bus dominant	Driver off, V_{LIN} = 0V, $R_{COMMANDER}$ OFF, $R_{RESPONDER}$ ON V_{SUP} = 28V	–1.5			mA
$I_{BUS\_PAS\_rec}$	Input leakage current at receiver, bus recessive	Driver off, $V_{LIN} \ge V_{SUP}$ $5V \le V_{SUP} \le 28V$, $5V \le V_{LIN} \le 28V$			30	µA
$I_{BUS\_PAS\_rec}$	Input leakage current at receiver, bus recessive	Driver off, $V_{LIN} \ge V_{SUP}$ $5V \le V_{SUP} \le 18V$, $5V \le V_{LIN} \le 18V$			20	µA
$I_{BUS\_NO\_GND}$	Bus current during loss of ground	$GND_{Device} = V_{SUP}$ = 12V R_{Meas} = 1kΩ $0V < V_{LIN} < 18V$	–1		1	mA
$I_{BUS\_NO\_GND}$	Bus current during loss of ground	$GND_{Device} = V_{SUP}$ = 12V R_{Meas} = 1kΩ $0V < V_{LIN} < 28V$	–1.5		1.5	mA
$I_{leak\ gnd(dom)}$	Device Bus leakage current with ground disconnected, bus dominant(4)	V_{SUP} = 8V, GND = open; V_{SUP} = 28V, GND = open LIN = dominant,	–1		1	mA
$I_{leak\ gnd(rec)}$	Device Bus leakage current with ground disconnected, bus recessive(4)	V_{SUP} = 8V, GND = open, V_{SUP} = 28V, GND = open LIN = recessive,	–100		100	µA
$I_{leak\ batt}$	Device bus leakage current battery supply disconnected	V_{SUP} = 8V or V_{SUP} = 28V	-30		30	µA
$I_{BUS\_NO\_BAT}$	Bus current during loss of supply	V_{SUP} = GND $0V \le V_{LIN} \le 28V$			30	µA
$R_{commander}$	Internal commander pull-up resistor to V_{SUP}	Normal and standby modes	900		1010	Ω
		Sleep mode	900	1200	1500	Ω
$R_{responder}$	Internal responder pull-up resistor to V_{SUP}	All operating modes as described in datasheet	27.66	37	48	kΩ
C_{LIN}	Capacitance of the LIN pin (5)	V_{SUP} = 5V to 28V,			25	pF
INHN Output Terminal						
V_{OL}	Low level output voltage	I_{OL} = 0.2mA			0.4	V
$I_{LKG(INH)}$	Leakage current sleep mode	Full range of V_{SUP}	–1		1	µA
Duty Cycle Characteristics						
D1	Duty cycle 1(1) (2) ISO 17987 Param 27/SAE J2602 Commander	$TH_{REC(MAX)} = 0.744 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.581 \times V_{SUP}$, V_{SUP} = 7V to 28V, t_{BIT} = 50µs/52µs $D1 = t_{BUS\_rec(min)}/(2 \times t_{BIT})$ Internal commander termination disabled	0.396			
$D1_{LB}$	Duty cycle 1 at low battery(1) (2) (5) ISO 17987 Param 88/SAE J2602 Commander	$TH_{REC(MAX)} = 0.665 \times V_{SUP}$, $TH_{DOM(MAX)} = 0.499 \times V_{SUP}$, V_{SUP} = 5V to 7V, t_{BIT} = 50µs/52µs Internal commander termination disabled	0.396			
D2	Duty cycle 2(1) (2) ISO 17987 Param 28/SAE J2602 Commander	$TH_{REC(MIN)} = 0.422 \times V_{SUP}$, $TH_{DOM(MIN)} = 0.284 \times V_{SUP}$, V_{SUP} = 7.6V to 28V, t_{BIT} = 50µs/52µs $D2 = t_{BUS\_rec(MAX)}/(2 \times t_{BIT})$ Internal commander termination disabled			0.581	

ADVANCE INFORMATION

parameters valid across entire recommended range of V_{SUP}, V_{IO} and Junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D2_{LB}$	Duty cycle 2 at low battery(1) (2) (5) ISO 17987 Param 89/SAE J2602 Commander	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 5.6V to 7.6V, t_{BIT} = 50µs/52µs Internal commander termination enabled			0.581	
D3	Duty cycle 3(1) (2) ISO 17987 Param 29/SAE J2602 Commander	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} V_{SUP} = 7V to 28V, t_{BIT} = 96µs D3 = $t_{BUS\_rec(min)}$/(2 x t_{BIT}) Internal commander termination disabled	0.417			
$D3_{LB}$	Duty cycle 3 at low battery(1) (2) (5) ISO 17987 Param 90/SAE J2602 Commander	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP}, V_{SUP} = 5V to 7V, t_{BIT} = 96µs Internal commander termination enabled	0.417			
D4	Duty cycle 4(1) (2) ISO 17987 Param 30/SAE J2602 Commander	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} V_{SUP} = 7.6V to 28V, t_{BIT} = 96µs D4 = $t_{BUS\_rec(MAX)}$/(2 x t_{BIT}) Internal commander termination disabled			0.59	
D_{4LB}	Duty cycle 4 at low battery(1) (2) (5) ISO 17987 Param 91/SAE J2602 Commander	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} V_{SUP} = 5.6V to 7.6V, t_{BIT} = 96µs Internal commander termination enabled			0.59	
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle(1) Recessive to dominant SAE J2602	$TH_{REC(MAX)}$ = 0.744 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.581 x V_{SUP} 7V ≤ V_{SUP} ≤ 28V, t_{BIT} = 52µs $t_{REC(MAX)\_D1}$ - $t_{DOM(MIN)\_D1}$			10.8	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle(1) Dominant to recessive SAE J2602	$TH_{REC(MAX)}$ = 0.422 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.284 x V_{SUP} 7.6V ≤ V_{SUP} ≤ 28V, t_{BIT} = 52µs $t_{DOM(MAX)\_D2}$ - $t_{REC(MIN)\_D2}$			8.4	µs
$T_{r\text{-}d\ max}$	Transmitter propagation delay timings for the duty cycle(1) Recessive to dominant SAE J2602	$TH_{REC(MAX)}$ = 0.778 x V_{SUP} $TH_{DOM(MAX)}$ = 0.616 x V_{SUP} 7V ≤ V_{SUP} ≤ 28V, t_{BIT} = 96µs $t_{REC(MAX)\_D3}$ - $t_{DOM(MIN)\_D3}$			15.9	µs
$T_{d\text{-}r\ max}$	Transmitter propagation delay timings for the duty cycle(1) Dominant to recessive SAE J2602	$TH_{REC(MIN)}$ = 0.389 x V_{SUP} $TH_{DOM(MIN)}$ = 0.251 x V_{SUP} 7.6V ≤ V_{SUP} ≤ 28V, t_{BIT} = 96µs $t_{DOM(MAX)\_D4}$ - $t_{REC(MIN)\_D4}$			17.28	µs
$T_{r\text{-}d\ max\_low}$	Low battery transmitter propagation delay timings for the duty cycle(1) (5) Recessive to dominant SAE J2602	$TH_{REC(MAX)}$ = 0.665 x V_{SUP}, $TH_{DOM(MAX)}$ = 0.499 x V_{SUP} 5V ≤ V_{SUP} ≤ 7V, t_{BIT} = 52µs $t_{REC(MAX)\_low}$ - $t_{DOM(MIN)\_low}$			10.8	µs
$T_{d\text{-}r\ max\_low}$	Low battery transmitter propagation delay timings for the duty cycle(1) (5) Dominant to recessive SAE J2602	$TH_{REC(MAX)}$ = 0.496 x V_{SUP} $TH_{DOM(MAX)}$ = 0.361 x V_{SUP} 5.6V ≤ V_{SUP} ≤ 7.6V, t_{BIT} = 52µs $t_{DOM(MAX)\_low}$ - $t_{REC(MIN)\_low}$			8.4	µs

(1) SAE 2602 commander node load conditions: 5.5nF/4kΩ and 889pF/20kΩ; t_{BIT} = 52µs/96µs
(2) ISO 17987 bus load conditions (C_{LINBUS}, R_{LINBUS}) include 1nF/1kΩ; 6.8nF/660Ω; 10nF/500Ω; t_{BIT} = 50µs/96µs
(3) V_{HYS} = (V_{th_rec} - V_{th_dom}) where V_{th_rec} and V_{th_dom} are the actual voltage values from V_{BUSrec} and V_{BUSdom}
(4) $I_{leak\ gnd}$ = (V_{BAT} - V_{LIN})/R_{Load}
(5) Guaranteed by design, not production tested

ADVANCE INFORMATION

5.8 AC Switching Characteristics

parameters valid across entire recommended range of V_{SUP}, V_{IO} and Junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time ISO 17987 Param 31	5V ≤ V_{SUP} < 7V, V_{IO} = 2.97V to 5.5V, C_{RXD} = 20pF			6.5	µs
t_{rx_pdr} t_{rx_pdf}	Receiver rising/falling propagation delay time ISO 17987 Param 31	7V ≤ V_{SUP} < 28V, V_{IO} = 2.97V to 5.5V, C_{RXD} = 20pF			6	µs
t_{rx_sym}	Symmetry of receiver propagation delay ISO 17987 Param 32	Rising edge with respect to falling edge $t_{rx\_sym} = t_{rx\_pdf} - t_{rx\_pdr}$ 5V ≤ V_{SUP} < 28V, V_{IO} = 2.97V to 5.5V, C_{RXD} = 20pF	–2		2	µs
t_{LINBUS}	Minimum dominant time on LIN bus for wake-up		25	65	150	µs
t_{MODE_CHANGE}	Mode change delay time	Time to change from normal mode to sleep mode through SLP pin Time to change from sleep or standby to normal mode through SLP pin	10		30	µs
t_{NOMINT}	Normal mode initialization time	Time for normal mode to initialize and data on RXD pin to be valid, includes t_{MODE_CHANGE} for standby/sleep to normal mode.			100	µs
t_{STBINT}	Standby mode initialization time	Transition time from sleep mode to standby mode after receiving wakeup			80	µs
t_{SLP}	Time to go to low power sleep mode	Time to fully transition to low power sleep mode from normal mode (includes t_{MODE_CHANGE})			60	µs
t_{TXD_DTO}	Dominant state time out (time started at falling edge on TXDx in normal mode)		6	10	14	ms
t_{LIN_DTO}	LIN dominant timeout (Time started at falling edge of LINx in normal/STB/sleep mode)		17	25	37	ms
t_{UV_SLP}	Delay time from VIO UV to Low power sleep mode			200	225	ms
t_{UVD}	V_{IO} undervoltage detection time			10	30	µs
t_{UVR}	V_{IO} undervoltage recovery time			550	660	µs
t_{PWR}	Power-up time	Time it takes for valid data on RXD upon power-up in normal mode			1.5	ms

5.9 Typical Characteristics

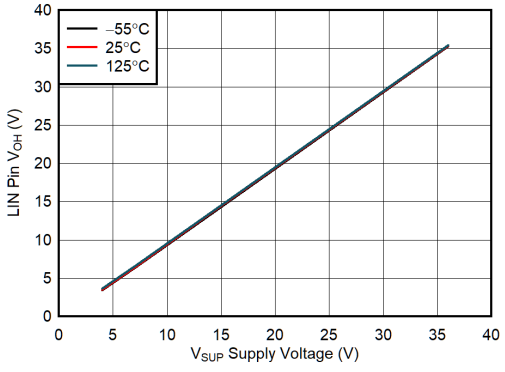


Figure 5-1. V_{OH} vs V_{SUP} and Temperature

6 Parameter Measurement Information

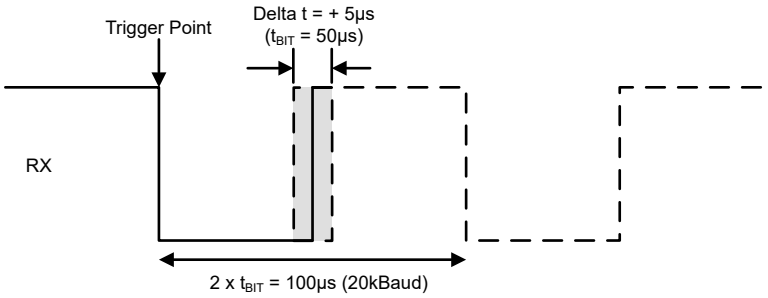


Figure 6-1. RX Response: Operating Voltage Range

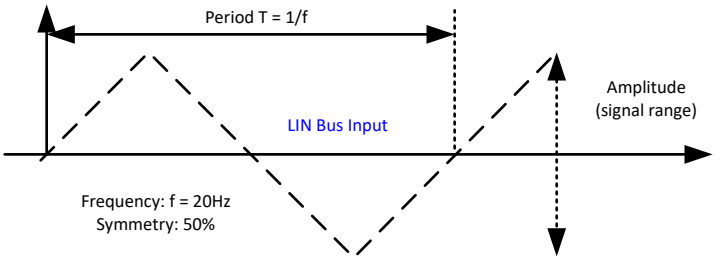


Figure 6-2. LIN Bus Input Signal

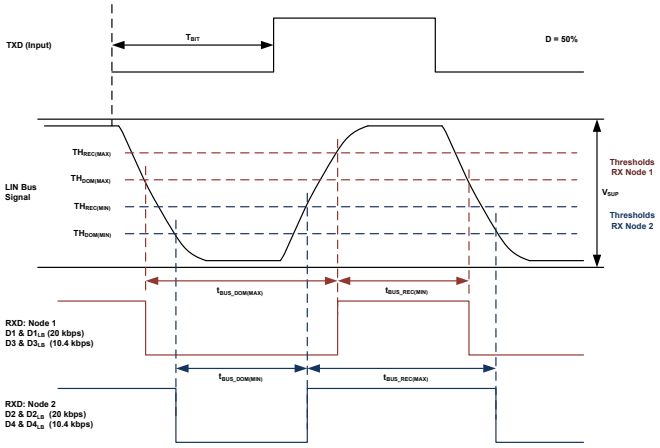


Figure 6-3. Definition of Bus Timing Parameters

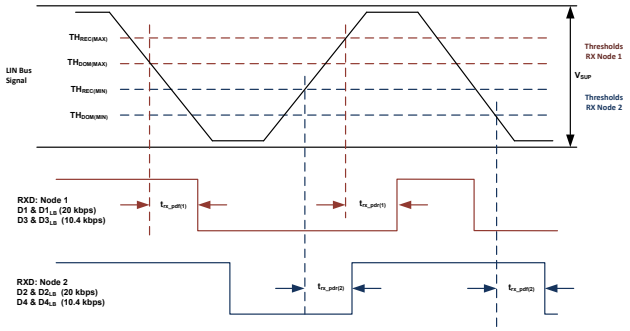


Figure 6-4. Receiver Propagation Delay

ADVANCE INFORMATION

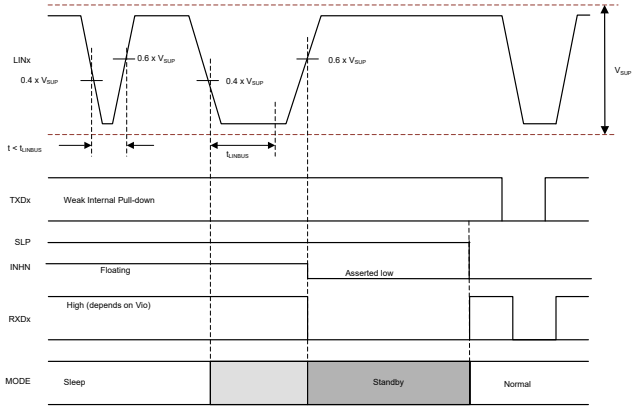


Figure 6-5. Wakeup through LIN

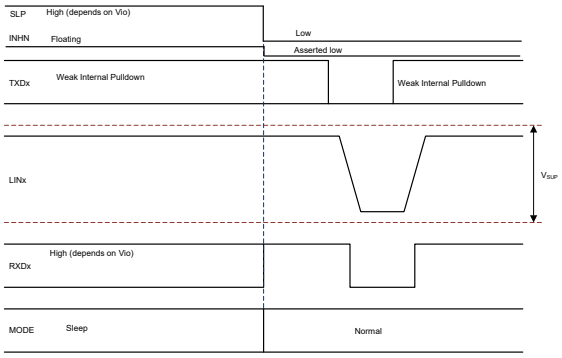


Figure 6-6. Wake-up through SLP

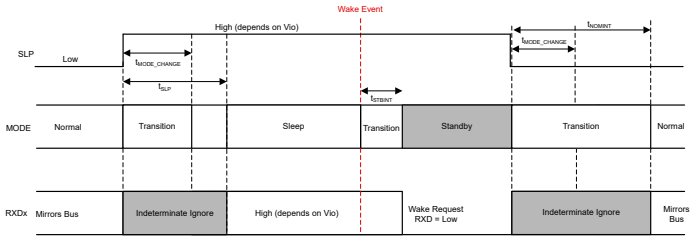


Figure 6-7. Mode Transitions

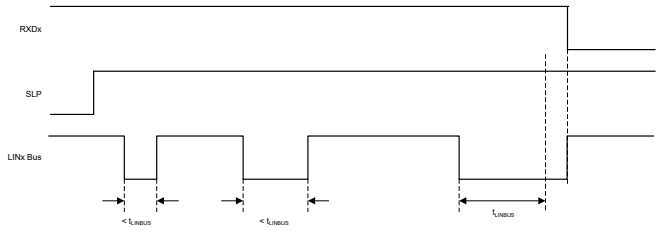


Figure 6-8. Entering Sleep Mode with Bus Recessive Condition and Wake-up

7 Detailed Description

7.1 Overview

The TLIN1124A-Q1 device is a Quad Local Interconnect Network (LIN) physical layer transceiver, compliant to LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A, ISO/DIS 17987-4, and SAE J2602-1 with integrated commander and responder termination diode and resistor along with wake-up and protection features. LIN is a single wire bidirectional bus typically used for low speed in-vehicle networks using data rates up to 20kbps. The LIN receiver supports data rates up to 100kbps for in-line programming. The device supports 12V battery applications with wider operating voltage (5V to 28V) and extended LIN bus-fault (±40V) protection. The device converts the LIN protocol data stream on the TXDx input into a LINx bus signal using a current-limited wave-shaping driver which reduces electromagnetic emissions (EME). The receiver converts the data stream to logic level signals that are sent to the microprocessor through the push-pull RXD output pin. Ultra-low current consumption is possible using the sleep mode which allows wake up via LIN bus or SLP pin. The integrated commander and responder diode and resistor, electrostatic discharge (ESD) protection, and fault protection allow designers to save board space in their applications. The device prevents back-feed current through LIN to the supply in case of ground shift or supply voltage disconnection.

The LIN bus has two states: dominant state (voltage near ground) and recessive state (voltage near battery). In the recessive state, the LIN bus is pulled high by the internal pull-up resistor and a series diode. The device has integrated resister and series diode for controller nodes on all four LIN channels so that no external pull-up components are required.

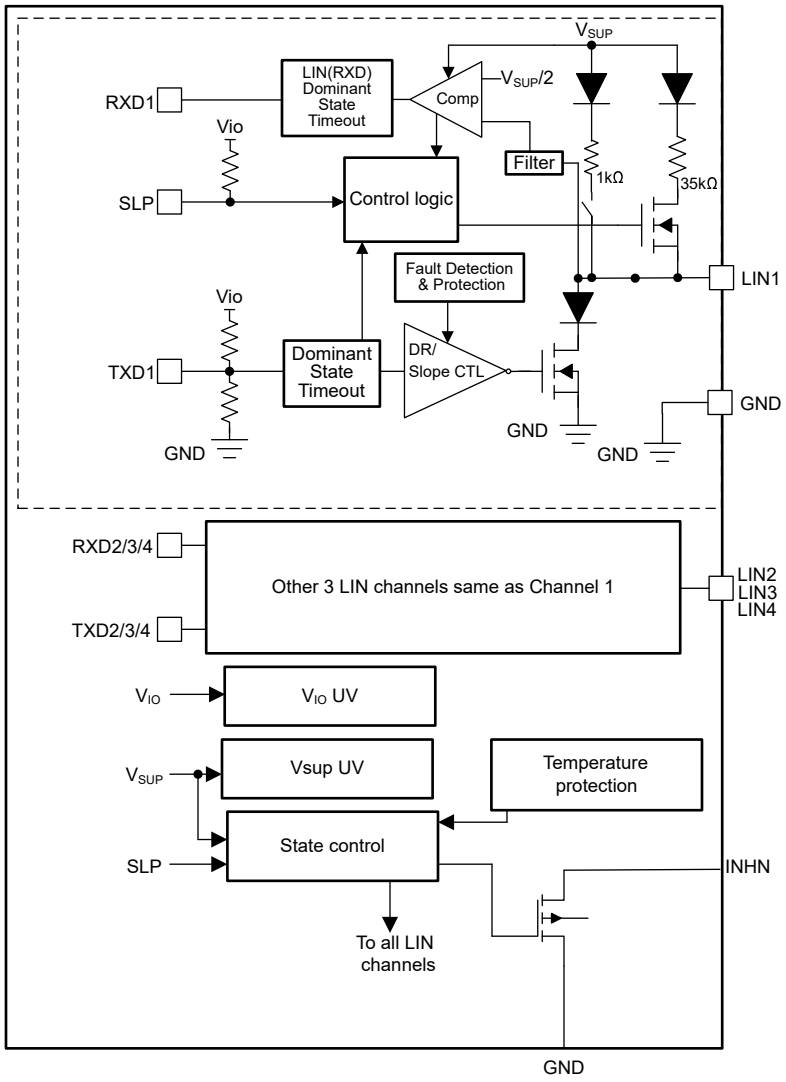
The TLIN1124A-Q1 support wide operating ranges with V_{SUP} of 5V to 28V LIN bus fault protection, -40°C to 150°C junction temperature. Ultra low power consumption is achieved in sleep mode. There are two methods of to wake up the device from sleep mode; by the LIN bus and local wake-up using the SLP pin.

There are many protection features provided by the device such as HBM ESD, IEC ESD protection, under voltage protection on V_{SUP} and V_{IO}, TXD Dominant Time Out Protection (TXD DTO), LIN dominant timeout protection (LIN DTO), thermal shutdown protection and unpowered node or ground disconnection failsafe at system level.

ADVANCE INFORMATION

ADVANCE INFORMATION

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 LIN (Local Interconnect Network) Bus

These high voltage input/output pins are single wire LIN bus transmitters and receivers. The LIN pins can survive excessive DC and transient voltages up to ±40V. Reverse currents from the LIN pins to supply (V_{SUP}) are minimized with blocking diodes, even in the event of a ground shift or loss of supply (V_{SUP}).

7.3.1.1 LIN Transmitter Characteristics

The transmitter is fully compliant to ISO 17987-4 and SAE J2602-1 physical layer LIN specification. The transmitter is a low side transistor with internal current limitation and thermal shutdown. During a thermal shutdown condition, the transmitter is disabled to protect the device. There are internal pull-up resistors with a serial diodes to V_{SUP} for both commander and responder, so no external pull-up components are required for any LIN applications.

7.3.1.2 LIN Receiver Characteristics

The receiver characteristic thresholds are ratio-metric with the device supply pin according to the LIN specification.

The receiver is capable of receiving higher data rates (up to 100kbps) than supported by LIN or SAE J2602 specifications. This allows the TLIN1124A-Q1 to be used for high speed downloads at the end-of-line production or other applications. The actual data rate achievable depends on system time constants (bus capacitance and pull-up resistance) and driver characteristics used in the system.

7.3.1.2.1 Termination

With the integrated commander and responder pull-up resistors along with serial diodes to V_{SUP}, no external pull-up components are required on the LIN bus with TLIN1124A-Q1.

Table 7-1 shows states of these pull-up termination in various operating modes of the device.

Table 7-1. Integrated termination in various modes

Device	Sleep(1)	Standby	Normal, TXD DTO	VIO UV	Over temperature	OFF	LIN DTO
TLIN1124A-Q1	RT = OFF, CT = ON	RT = OFF, CT = ON	RT = OFF, CT = ON	RT = OFF, CT = ON	RT = ON, CT = OFF	RT = OFF, CT = OFF	RT = ON, CT = OFF

(1) RT = Responder termination (35 kΩ typical), CT = Commander termination (1 kΩ typical)

7.3.2 TXDx (Transmit Input and Output)

TXD is the interface to the MCU LIN protocol controller or SCI and UART that is used to control the state of the LIN output. When TXD is low the LIN output is dominant (near ground) and when TXD is high the LIN output is recessive (near VSUP). TXDx is in the V_{io} domain (with CMOS input thresholds) and the input structure is compatible with 3.3V and 5V microcontrollers. TXD also integrates a weak pull-down and pull-up resistor. The LIN bus is protected from being stuck dominant (from a system failure driving TXD low) through the dominant state timer-out timer.

Upon every transition to normal mode, the LIN transmitter is blocked until TXDx goes high (recessive level) to prevent transmitting dominant (due to internal pull-down on TXDx).

7.3.3 RXDx (Receive Output)

RXD is the interface to the MCU's LIN protocol controller, which reports the state of the LIN bus voltage. LIN recessive (near V_{SUP}) is represented by a high level on the RXD and LIN dominant (near ground) is represented by a low level on the RXD pin. RXD is a push-pull output buffer in Vio domain. In standby mode, if the transition is via sleep mode, the RXD pin is driven low to indicate a wake-up request. In sleep mode, RXD is pulled-up high as long as Vio is present.

7.3.4 V_{SUP} (Supply Voltage)

V_{SUP} is the power supply pin. V_{SUP} is connected to the battery through an external reverse-blocking diode. If there is a loss of power at the ECU level, the device has extremely low leakage from the LINx pin, which does not load the bus down. This is optimal for LIN systems in which some of the nodes are unpowered (ignition supplied) while the rest of the network remains powered (battery supplied).

7.3.5 V_{IO} (logic interface supply voltage)

V_{IO} is supply voltage for I/O interface buffers on chip: SLP, TXDx and RXDx. V_{IO} and V_{SUP} are independent supplies. So some applications can have V_{IO} independently available even if V_{SUP} is in undervoltage lockout. Applications controlling V_{IO} generation using INHN always have V_{SUP} come up first followed by V_{IO}.

7.3.6 GND (Ground)

GND is the device ground connection. The device can operate with a ground shift as long as the ground shift does not reduce the V_{SUP} below the minimum operating voltage. If there is a loss of ground at the ECU level, the device has low leakage from the LIN pin, which does not load the bus down.

ADVANCE INFORMATION

7.3.7 SLP (Sleep Input)

SLP controls the operational modes of the device. When SLP is low the device is in normal operating mode (assuming V_{IO} is present) allowing a transmission path from TXDx to LINx and from LINx to RXDx. When SLP is high (assuming V_{IO} is present), the device is put into sleep mode and there are no transmission paths available. SLP has an internal pull-up resistor to V_{IO}.

7.3.8 INHN (Inhibit high voltage output terminal)

INHN is high voltage output. The optional feature controls system power management allowing for a significant reduction in battery quiescent current consumption while the application is in sleep mode. The INHN pin has two states: asserted low and high impedance (floating). The INHN pin is low in the normal and standby modes and is floating when in sleep mode. A 100kΩ pull-up to V_{SUP} can be added to the INHN output pin for a fast transition from the driven low state to the high state, and to make sure the pin is high when left floating.

The INHN terminal should be considered a high-voltage logic terminal and not a power output. Thus should be used to drive the EN terminal of the systems power-management device. This terminal is not reverse battery protected and thus should not be connected outside the system module.

7.3.9 Protection Features

The TLIN1124A-Q1 has several protection features that are described as follows.

7.3.9.1 TXD Dominant Time Out (TXD DTO)

While the LIN driver is in normal (active) mode, a TXD DTO circuit prevents the local node from blocking network communication in event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}. TLIN1124A-Q1 has TXD DTO on all LIN channels. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the time-out t_{TXD_DTO} expires, the LIN driver is disabled releasing the bus line to the recessive level. This keeps the bus free for communication between other nodes on the network. The LINx driver is re-activated on the next dominant to recessive transition on the TXDx terminal, thus clearing the dominant time-out. During this fault, the transceiver remains in normal mode, the integrated LIN bus pull-up termination remains on, and the LIN receiver and RXD terminal remain active reflecting the LIN bus data.

7.3.9.2 LIN Dominant timeout (LIN DTO)

TLIN1124A-Q1 has LIN dominant timeout function on all LIN channels. If the LINx bus remains dominant for longer than t_{LIN_DTO}, this function switches off LINx commander termination resistor $R_{COMMANDER}$. Responder termination resistor $R_{RESPONDER}$ remains ON. This is to protect device from excessive on-chip power dissipation in case LIN bus is shorted to ground due to some fault. Once LINx bus level is recessive again, LIN commander termination resistor is switched ON and t_{LIN_DTO} timer is reset.

If bus is dominant on entering normal/standby or sleep mode, LIN DTO timer starts immediately upon transition to respective modes.

7.3.9.3 Thermal Shutdown

The device is protected by limiting the on-chip power dissipation in fault scenarios. If the junction temperature, T_J , of the device exceeds the thermal shutdown threshold rising threshold T_{SDR}, the device will react depending on the current state (see below). Once the over temperature fault condition has been removed and the junction temperature has cooled beyond the hysteresis temperature, device transitions to the previous state before thermal shutdown (TSD) had occurred.

Normal Mode

During a TSD event, the control logic puts all the LINx transmitters into the recessive state and the commander termination $R_{COMMANDER}$ is switched off for all channels. INHN is kept at the same logic as before entering TSD, while TXDx, SLP pins are ignored.

Standby Mode

During a TSD event, the control logic puts all the LINx transmitters into the recessive state and the commander termination $R_{COMMANDER}$ is switched off for all channels. INHN is kept same at the logic as before entering TSD,

while TXDx, SLP pins are ignored. Received wakeup events are cleared while in over temperature state (RXDx is made high).

Sleep Mode

In sleep mode, the over temperature monitor is turned off for power savings.

7.3.9.4 Under Voltage on V_{SUP} and V_{IO}

The device contains undervoltage circuit on both V_{SUP} and V_{IO} to avoid false bus messages or unknown behavior during under voltage conditions. When these levels are reached after being on, the device transitions into one of two modes of operation depending upon which power rail reached the undervoltage falling level.

Unpowered (off) state: When V_{SUP} reaches $UV_{SUP\_falling}$, the device enters the unpowered state and makes sure the unpowered ECU is passive (no load) to ongoing communication on bus-since in automotive applications. Some LIN nodes in a system can be unpowered, ignition supplied, while others in the network remains powered by the battery. From any node, if V_{SUP} falls below $UV_{SUP\text{-}falling}$, device transitions to unpowered (OFF) state. In this state, SLP, TXDx are ignored, driver, integrated pull-up termination for commander/responder and receiver for all channels are switched off and INHN is floating.

Under Voltage V_{IO} Mode: When V_{SUP} is in proper operating range, but V_{IO} is less than $UV_{VIO\text{-}falling}$, the device transitions to VIO UV Mode from Normal or Standby modes. In this mode, all LIN channel driver is switched OFF. V_{io} domain signals, TXDx and SLP, are ignored and RXDx is floating, while INHN remains asserted low. While in this mode, new wake events are not recognized but the device retains the previous wake event if device has entered Standby mode due a wake event. There are two ways the device transitions out of this mode.

- When $V_{IO} > UV_{VIO\_rising}$, the device transitions to Normal or Standby mode depending upon the state of the SLP pin.
- If V_{IO} does not exceed UV_{VIO_rising} by the time t_{UV_SLP} timer expires, the device transitions to Sleep mode. When this takes place, all existing wake events are cleared.

If V_{IO} is present while the device is in Sleep mode, a UV_{VIO} event does not cause a mode change.

7.3.9.5 Unpowered Device and LIN Bus

In automotive applications, some LIN nodes in a system can be unpowered (ignition supplied) while others in the network remains powered by the battery. The TLIN1124A-Q1 has a low unpowered leakage current from the bus, so an unpowered node does not affect the network or load it down.

ADVANCE INFORMATION

7.4 Device Functional Modes

TLIN1124A-Q1 has three main functional modes of operation: Normal, Standby and low power sleep. Besides this, there are three other states for fault/power events: Overtemperature, unpowered (OFF) and V_{IO} undervoltage (V_{IO} UV) mode. See Figure 7-1 for more details.

Table 7-2. Operating Modes

MODE	SLP	TXD	RXD	INHN	TRANSMITTER	RECEIVER
OFF	X	X	Pull-up	High impedance	OFF	OFF
Sleep	High	Weak pull-down / pull-up	Pull-up	High impedance	OFF	ON
Standby	High	Weak pull-down / pull-up	Low if coming from sleep mode or wake event; same as previous state if transitioning from Overtemp or V_{IO} UV mode	Low	OFF	ON
Normal	Low	If high, bus recessive; if Low, bus dominant	LIN bus	Low	ON	ON
Overtemperature	X	X	Pull-up	Same as previous state	OFF	ON
UV V_{IO}	X	X	Pull-up	Low	OFF	ON
TXD DTO	Low	Timer started with TXD high to low edge and DTO triggered after timer times out	LIN bus	Low	OFF (only specific channel)	ON
LIN DTO	Low (normal mode) or High (standby/ sleep mode)	X	Same as previous state	MODE dependent	MODE dependent	ON

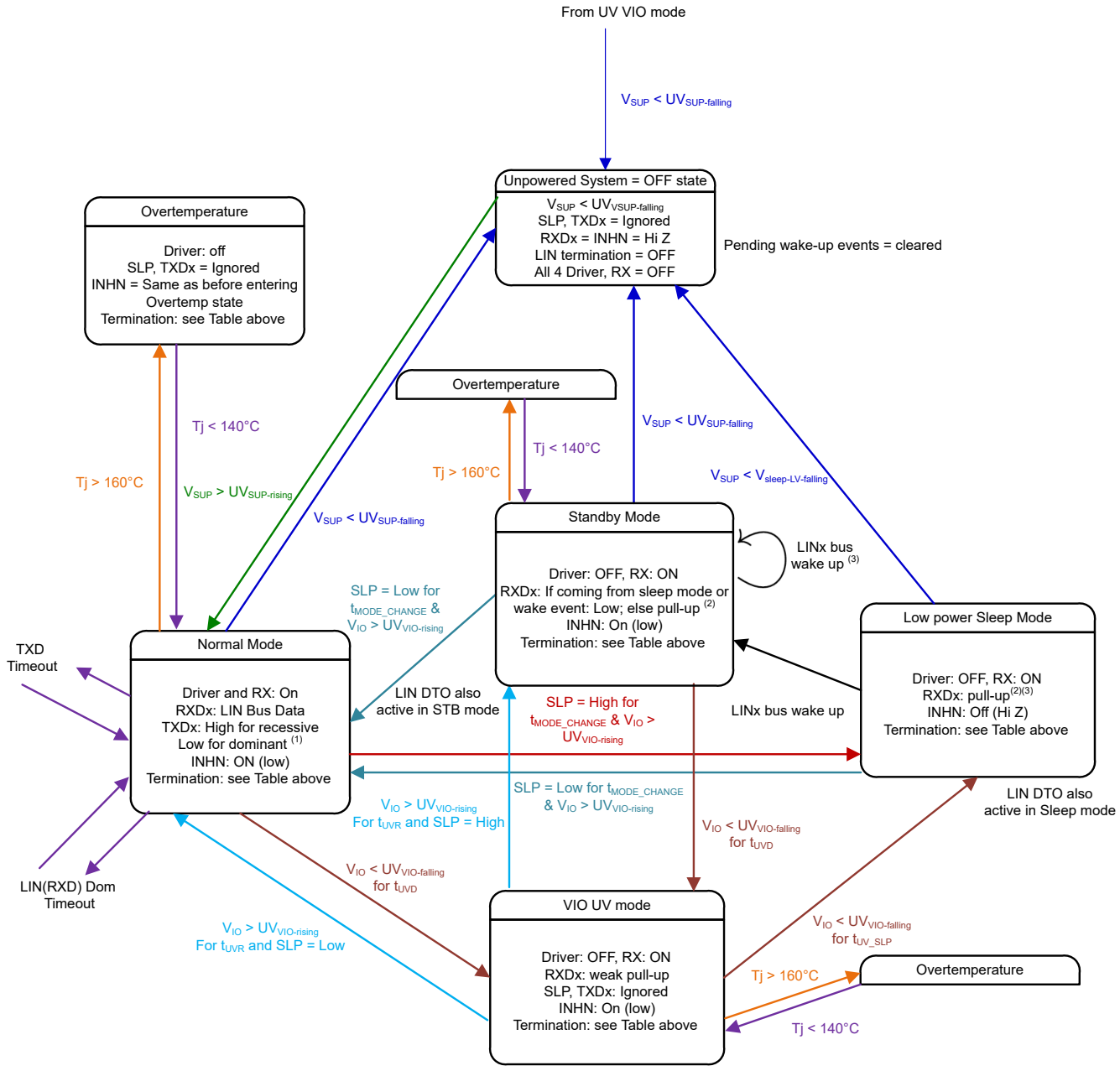


Figure 7-1. Operating State Diagram

Note

1. If TXD pin is dominant at the time of entering normal mode the LIN transmitter is kept off until a recessive is applied to TXD
2. Assumes V_{IO} is above $UV_{VIO\text{-}rising}$
3. If V_{IO} is on in sleep mode and an UV_{IO} event takes place, the device remains in sleep mode.

ADVANCE INFORMATION

7.4.1 Normal Mode

Once V_{SUP} crosses the $UV_{SUP\text{-}rising}$ threshold, the device powers up in normal mode. V_{IO} is checked only after the transition to normal mode. If V_{IO} is above $UV_{VIO\text{-}rising}$, device checks SLP pin. If SLP is high for for at least t_{MODE_CHANGE}, device transitions to sleep mode. If SLP is low, device stays in normal mode. But if V_{IO} is below $UV_{VIO\text{-}falling}$ after entry to normal mode, device goes to intermediate state V_{IO} UV mode where it waits for V_{IO} to come up.

In normal mode, all LIN channel driver, pull-up termination and receiver are fully functional. INHN is asserted low. TXDx can be used to transmit data on LINx bus, RXDx reflects LINx bus data.

7.4.2 Sleep Mode

This is the lowest power consuming mode of the device. All channel receivers are kept ON to detect LIN bus wakeup. TLIN1124A-Q1 cannot send or receive LIN bus data on this state, but can detect LIN bus wakeup. V_{IO} presence or absence does not matter for the device to be in this mode. All LIN channel drivers are OFF. RXDx is pulled up to V_{IO}. INHN is floating, so when INHN is used for system power management control, all components on ECU are switched off except LIN device which can turn on the module upon wakeup.

If V_{IO} is present, transition of SLP from high to low and being low for at least t_{MODE_CHANGE} puts the device in normal mode.

7.4.3 Standby Mode

When the device receives a LIN bus wakeup in sleep mode, the device transitions to standby mode. In standby mode, all LIN channels driver are OFF, receiver is ON but RXDx is latched low. If LIN bus wakeup was the reason to transition to standby mode, only corresponding RXD of LIN channel is latched low which received LIN wakeup. INHN can be asserted low to enable V_{io} to come up if INHN is used to control system power management. Transition of SLP from high to low by MCU and SLP being held low for at least t_{MODE_CHANGE}, transitions the device to normal mode. For the initialization of device in normal mode, t_{NOMINT} time is required.

If device had transitioned to standby mode due to a wakeup event, another wakeup event in standby mode keeps the device in standby mode until MCU forces the device to go to normal mode using SLP pin.

If the device had transitioned to standby mode from V_{io} UV mode with SLP = high, RXDx is high since wakeup had not forced the device into standby mode.

7.4.4 Wake Up Events

The TLIN1124A-Q1 supports two methods for wake-up from sleep mode:

- Wake-up over the LIN bus via the LIN wake-up receiver: Remote wake-up initiated by the falling edge of a recessive-to-dominant state transition on the LIN bus where the dominant state is be held than t_{LINBUS} filter time. After the t_{LINBUS} filter time has been met, a rising edge on the LIN bus going from dominant-to-recessive initiates a remote wake-up event. The pattern and t_{LINBUS} filter time used for the LIN wake-up prevents noise and bus stuck dominant faults from causing false wake requests.
- For a local wake-up via the SLP pin, the SLP pin must be set low for $t > t_{MODE\_CHANGE}$ for the device to wake-up and fully transition to normal mode within t_{NOMINT}.

7.4.4.1 Wake Up Request (RXD)

When the TLIN1124A-Q1 encounters a wake-up event, the RXDx output is driven low. The output remains low until SLP is asserted low for the device to enter normal mode. Once the device enters normal mode, the wake-up event is cleared, and the RXDx output is released. The RXDx output is fully operation and reflects the receiver output from the LINx bus.

7.4.4.2 Mode Transitions

When the TLIN1124A-Q1 is transitioning between modes the device needs the time, t_{MODE_CHANGE}, to allow the change to fully propagate from the SLP pin through the device into the new state. When transitioning from sleep or standby mode to normal mode, the transition time is the sum of t_{MODE_CHANGE} and t_{NOMINT}. Similarly when the device is transitioning from normal to sleep mode via SLP pin, the transition time is the sum of t_{MODE_CHANGE} and t_{SLP}.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TLIN1124A-Q1 is a commander device for a LIN network with integrated commander pull-up resistor.

8.2 Typical Application

The device comes with an integrated 37kΩ and 1kΩ pull-up resisters and series diodes for commander applications. Figure 8-1 shows the device being used as a commander.

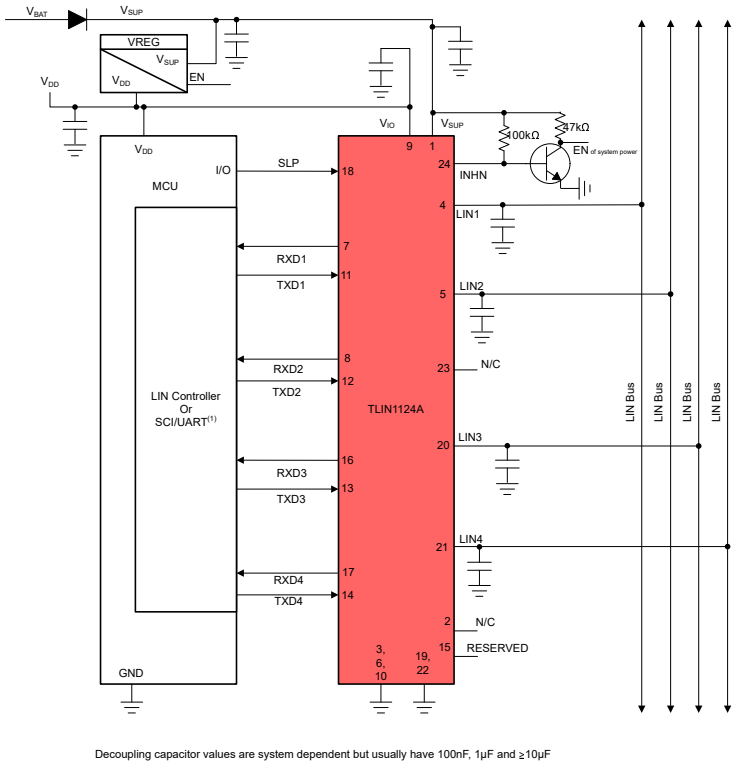


Figure 8-1. Typical LIN Bus

8.2.1 Design Requirements

1. RXD output from TLIN1124A-Q1 is push-pull type; no external pull-up resistor from RXD to V_{IO} is needed.
2. Decoupling capacitor values on V_{SUP} and V_{IO} are system dependent, but normally it is recommended to have a 100nF on each terminal as close as possible to device package pins.

8.2.1.1 Detailed Design Procedure

The RXD output structure is a push-pull output stage the in V_{IO} domain. V_{IO} support from 2.97V to 5.5V allows TLIN1124A-Q1 to be easily interfaced to 3.3V or 5V I/O micrcontrollers.

The V_{SUP} and V_{IO} pins of the device should be decoupled with a 100nF capacitor as close to the supply pin on the device as possible.

ADVANCE INFORMATION

8.3 Power Supply Recommendations

The TLIN1124A-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 5V to 28V. A 100nF decoupling capacitor should be placed as close possible to the V_{SUP} and V_{IO} pins of the device. Most applications include 1µF and ≥ 10µF decoupling capacitors.

8.4 Layout

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3MHz to 3GHz, high frequency layout techniques must be applied during PCB design. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

8.4.1 Layout Guidelines

- **Pins 7, 8, 16 and 17 (RXD):** The pins are open drain outputs and require an external pull-up resistor in the range of 1kΩ and 10kΩ to function properly. If the microprocessor paired with the transceiver does not have an integrated pull-up, an external resistor must be placed between RXD and the regulated voltage supply for the microprocessor.
- **Pins 11, 12, 13 and 14 (TXD):**The TXD pins are the transmitter input signals to the device from the microprocessor. A series resistor can be placed to limit the input current to the device in the case of an overvoltage on this pin. A capacitor to ground can be placed close to the input pin of the device to filter noise.
- **Pin 18 (SLP):** SLP is an input pin which enables an optional sleep mode in the device. SLP can be tied directly to the MCU I/O.
- **Pin 24 (INH):** INH is an open drain output pin. It must be connected with a 100kΩ pull-up to V_{SUP} for a fast transition from the driven low state to the high state, and to make sure the pin is high when left floating.
- **Pins 4, 5, 20, and 21 (LIN):** This pin connects to the LIN bus. For responder node applications a 220pF capacitor to ground is implemented. For commander node applications and additional series resistor and blocking diode must be placed between the LIN pin and the V_{SUP} pin.For commander applications, typically 680pF from LIN pin to GND is used.
- **Pins 3, 6, 10, 15, 19 and 22 (GND and RSVD):**This is the ground connection for the device. This pin must be tied to the ground plane through a short trace with the use of two vias to limit total return inductance
- **Pins 1 and 9 (V_{SUP} and V_{IO}):** These are the supply pin for the device. A 100nF decoupling capacitor must be placed as close to the device as possible
- **Pins 2 and 23 (NC):** Not Connected

Note

All ground and power connections must be made as short as possible and use at least two vias to minimize the total loop inductance.

ADVANCE INFORMATION

8.4.2 Layout Example

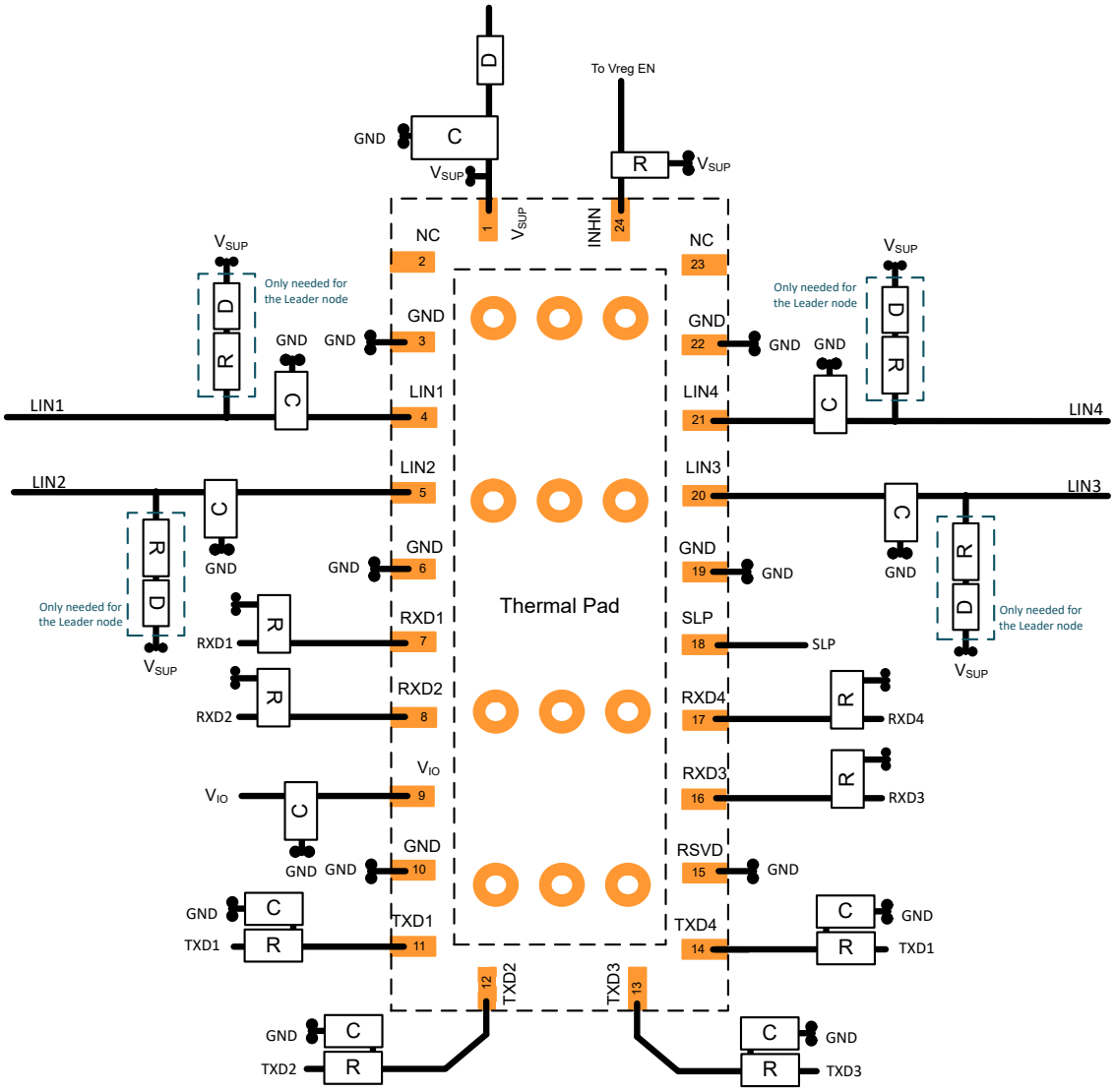


Figure 8-2. Layout Example

ADVANCE INFORMATION

ADVANCE INFORMATION

9 Device and Documentation Support

9.1 Documentation Support

This device will conform to the following LIN standards. The core of what is needed is covered within this system spec, however reference should be made to these standards and any discrepancies pointed out and discussed. This document should provide all the basics of what is needed.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Package Option Addendum

Table 11-1. Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(4)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking(5) (6)
TLIN1124ARGYRQ1	ACTIVE	VQFN	RGY	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL124

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

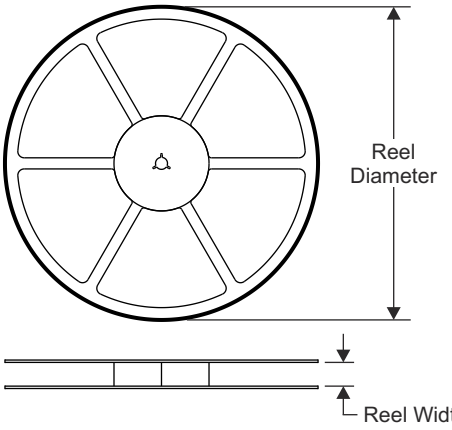
(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

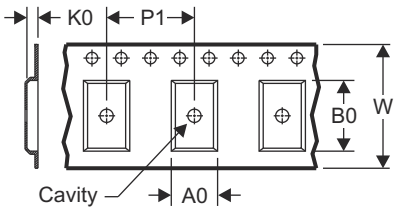
ADVANCE INFORMATION

11.2 Tape and Reel Information

REEL DIMENSIONS

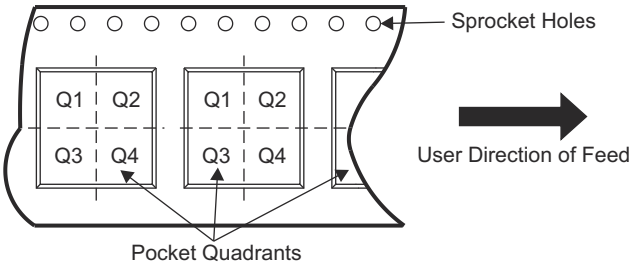


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

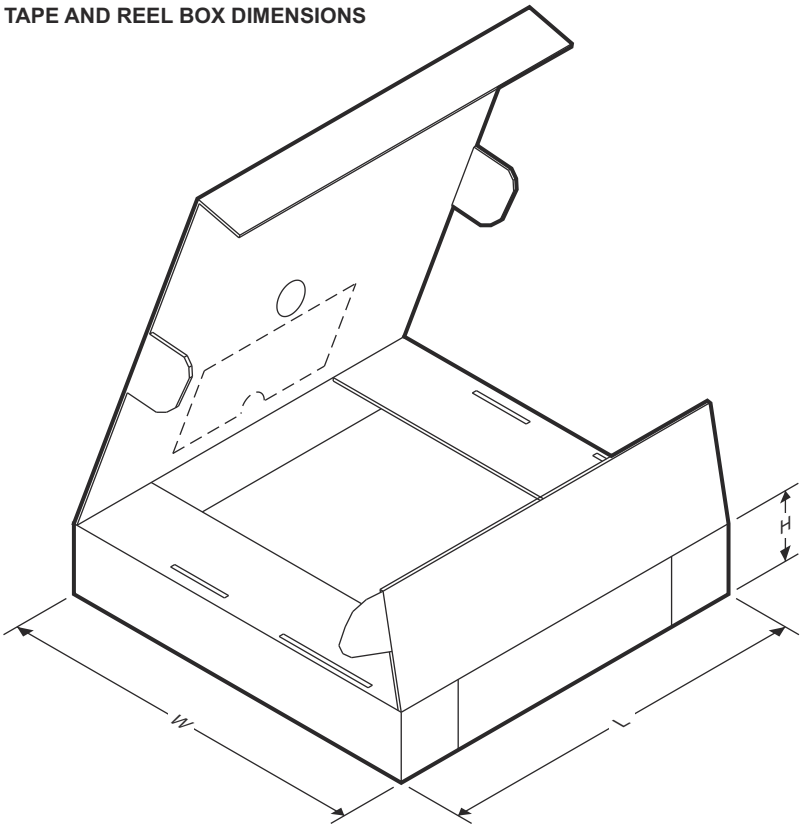
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLIN1124ARGYRQ1	VSON	RGY	24	3000	330.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLIN1124RGYRQ1	VSON	RGY	24	3000	367.0	367.0	35.0

ADVANCE INFORMATION

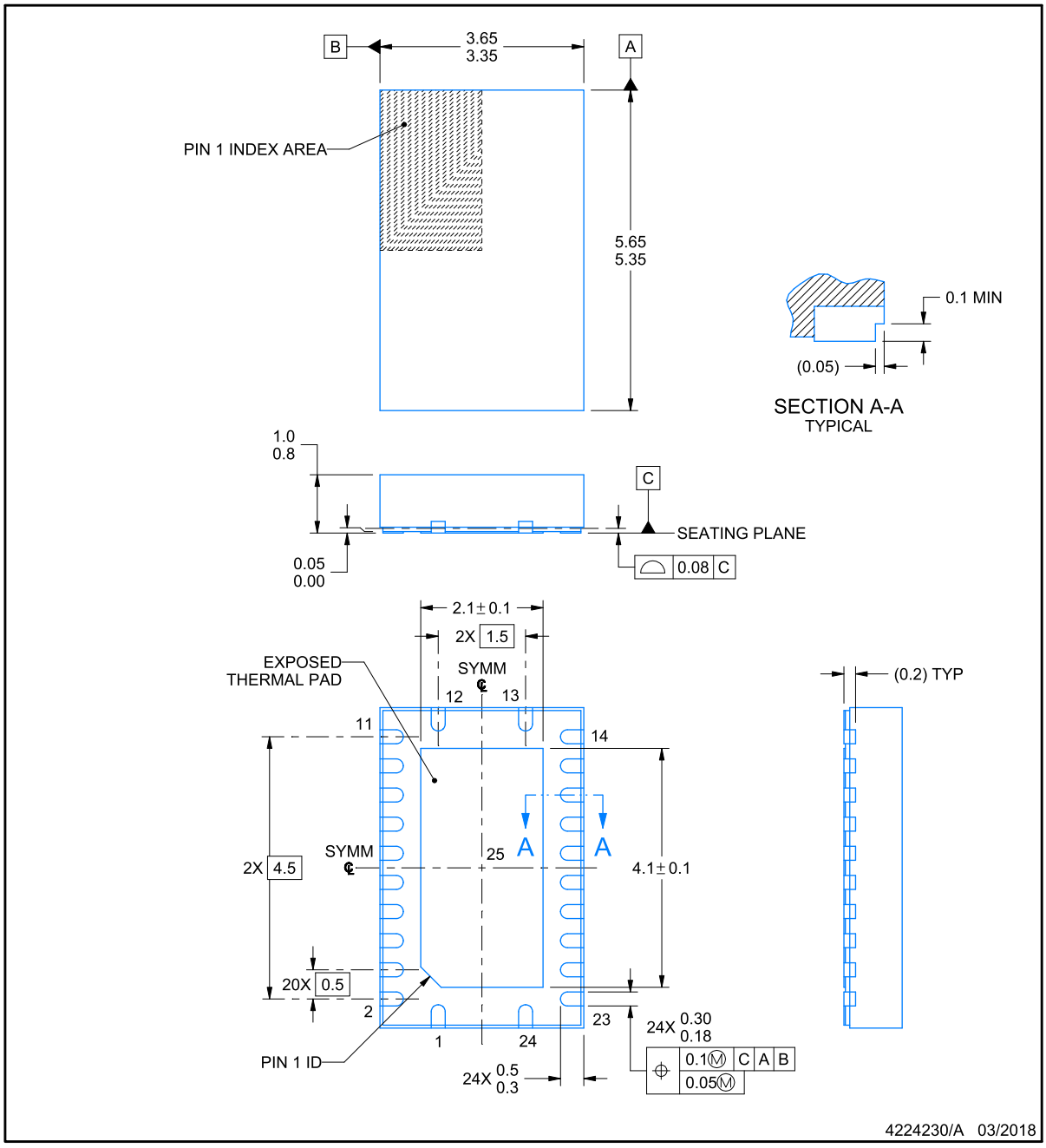
ADVANCE INFORMATION

11.3 Mechanical Data

PACKAGE OUTLINE

RGY0024C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

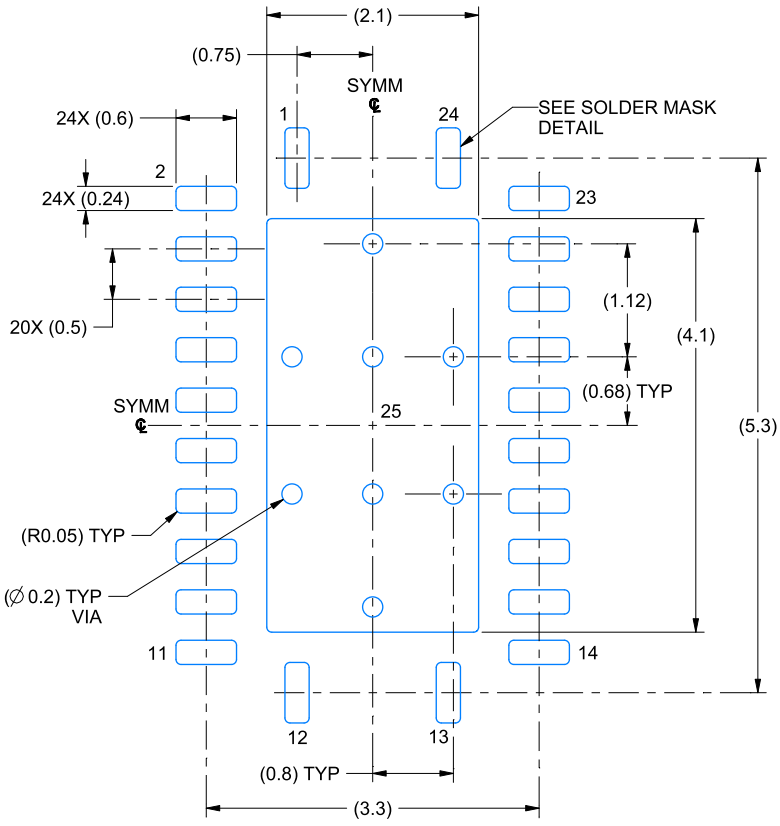
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

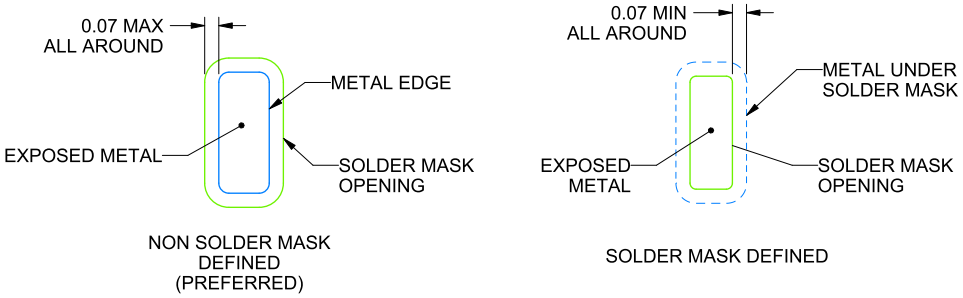
RGY0024C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4224230/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

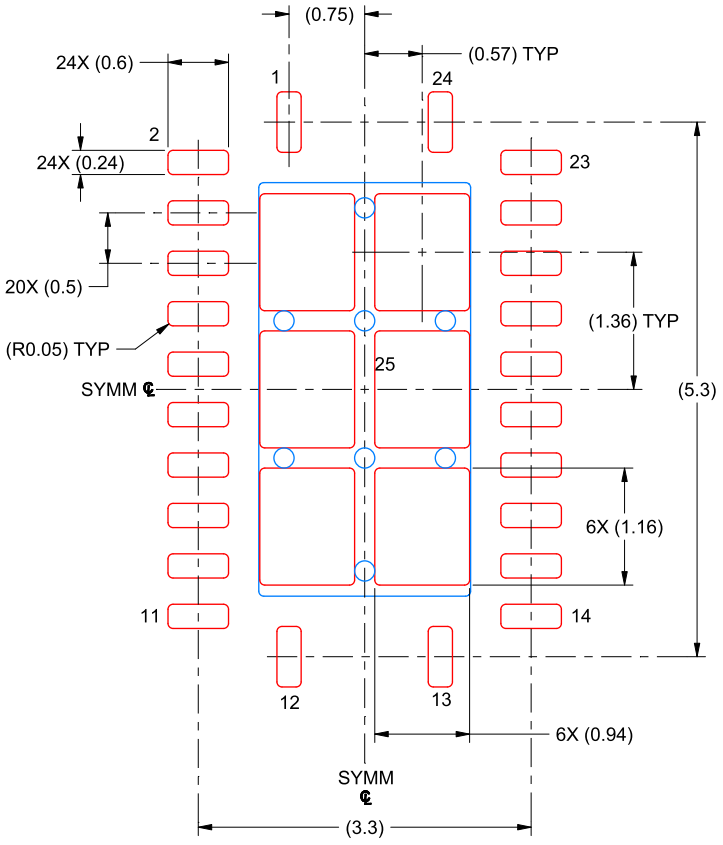
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGY0024C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 25
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224230/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTLIN1124ARGYRQ1	Active	Preproduction	VQFN (RGY) | 24	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

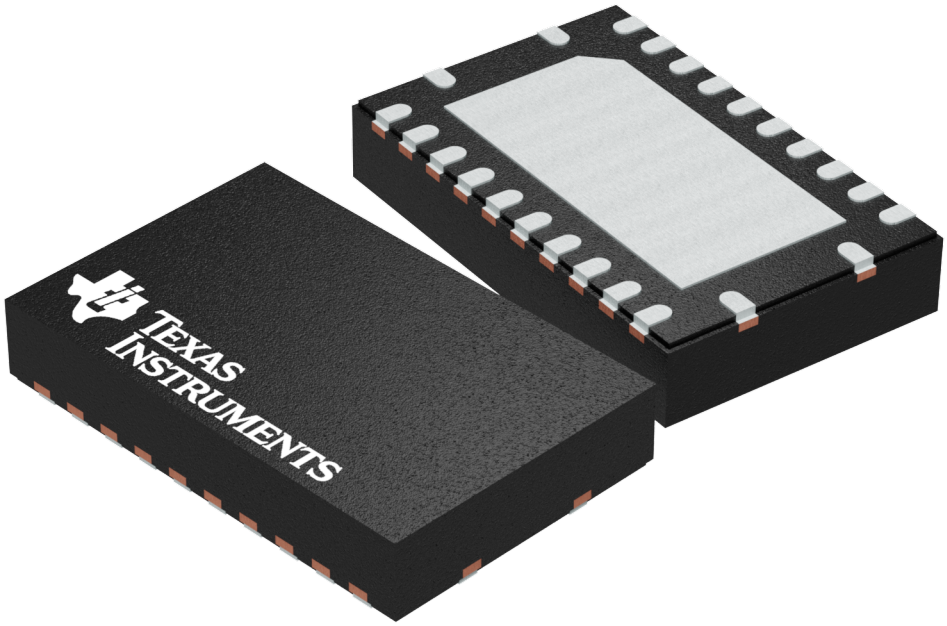
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

RGY 24

VQFN - 1 mm max height

5.5 x 3.5 mm, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025