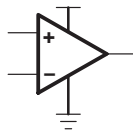


## FAMILY OF LOW-POWER WIDE BANDWIDTH SINGLE SUPPLY OPERATIONAL AMPLIFIERS WITH AND WITHOUT SHUTDOWN

### FEATURES

- Rail-To-Rail Output
- $V_{ICR}$  Includes Ground
- Gain-Bandwidth Product . . . 9 MHz
- Supply Current . . . 730  $\mu\text{A}/\text{Channel}$
- Single, Duals, and Quad Versions
- Ultralow Power Down Mode  
 $I_{DD}(\text{SHDN}) = 4 \mu\text{A}/\text{Channel}$
- Specified Temperature Range  
 $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  . . . Industrial Grade
- Supply Voltage Range . . . 2.7 V to 5.5 V
- Ultrasmall Packaging  
5 or 6 Pin SOT-23 (TLV2630/1)  
8 or 10 Pin MSOP (TLV2632/3)
- Universal Op-Amp EVM (See SLOU060  
for More Information)

Operational Amplifier



### DESCRIPTION

The TLV263x single supply operational amplifiers provide rail-to-rail output with an input range that includes ground. The TLV263x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ) while adding the rail-to-rail output swing feature. The TLV263x also provides a 9 MHz gain-bandwidth product from only 730  $\mu\text{A}$  of supply current. The maximum recommended supply voltage is 5.5 V, which, when coupled with a 2.7-V minimum, allows the devices to be operated from lithium ion cells.

The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications. The ground input range allows it to directly interface to ground rail referred systems.

All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power microcontrollers available today including TI's MSP430.

AMPLIFIER SELECTION TABLE

DEVICE	$V_{DD}$ [V]	$I_{DD}/\text{ch}$ [ $\mu\text{A}$ ]	$V_{ICR}$ [V]	GBW [MHz]	SLEW RATE [V/ $\mu\text{s}$ ]	$V_n$ , 1 kHz [nV/ $\sqrt{\text{Hz}}$ ]	$I_O$ [mA]
OPAx343	2.5–5.5	850	$-0.3$ to $V_{DD} + 0.3$	5.5	6	25	40
OPAx743	3.5–12	1100	$-0.1$ to $V_{DD} + 0.1$	7	10	30	20
TLV278x	1.8–3.6	650	$-0.2$ to $V_{DD} + 0.2$	8	5	9	10
<b>TLV263x</b>	<b>2.7–5.5</b>	<b>730</b>	<b>GND to <math>V_{DD} - 1</math></b>	<b>9</b>	<b>9.5</b>	<b>50</b>	<b>28</b>
TLV262x	2.7–5.5	750	1 V to $V_{DD} + 0.2$	11	10	27	28
OPAx353	2.7–5.5	8000	$-0.1$ to $V_{DD} + 0.1$	44	22	7	40



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TLV2630, TLV2631**  
**TLV2632, TLV2633**  
**TLV2634, TLV2635**

SLOS362A – JUNE 2001 – REVISED JANUARY 2005

**PACKAGE/ORDERING INFORMATION(1)**

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	SPECIFIED TEMPERATURE RANGE	ORDER NUMBER	TRANSPORT MEDIA
<b>Single with Shutdown</b>						
TLV2630ID	SOIC-8	D	—	-40°C to 125°C	TLV2630ID TLV2630IDR	Tube Tape and Reel
TLV2630IDBV	SOT-23-6	DBV	VAYI		TLV2630IDBVR† TLV2630IDBVT‡	Tape and Reel
TLV2630IP	DIP-8	P	—		TLV2630IP	Tube
<b>Single without Shutdown</b>						
TLV2631ID	SOIC-8	D	—	-40°C to 125°C	TLV2631ID TLV2631IDR	Tube Tape and Reel
TLV2631IDBV	SOT-23-5	DBV	VAZI		TLV2631IDBVR† TLV2631IDBVT‡	Tape and Reel
TLV2631IP	DIP-8	P	—		TLV2631IP	Tube
<b>Dual without Shutdown</b>						
TLV2632ID	SOIC-8	D	—	-40°C to 125°C	TLV2632ID TLV2632IDR	Tube Tape and Reel
TLV2632IDGK	MSOP-8	DGK	AKG		TLV2632IDGK TLV2632IDGKR	Tube Tape and Reel
TLV2632IP	DIP-8	P	—		TLV2632IP	Tube
<b>Dual with Shutdown</b>						
TLV2633ID	SOIC-14	D	—	-40°C to 125°C	TLV2633ID TLV2633IDR	Tube Tape and Reel
TLV2633IDGS	MSOP-10	DGS	AKK		TLV2633IDGS TLV2633IDGSR	Tube Tape and Reel
TLV2633IN	DIP-14	N	—		TLV2633IN	Tube
<b>Quad without Shutdown</b>						
TLV2634ID	SOIC-14	D	—	-40°C to 125°C	TLV2634ID TLV2634IDR	Tube Tape and Reel
TLV2634IN	DIP-14	N	—		TLV2634IN	Tube
TLV2634IPW	TSSOP-14	PW	—		TLV2634IPW TLV2634IPWR	Tube Tape and Reel
<b>Quad with Shutdown</b>						
TLV2635ID	SOIC-16	D	—	-40°C to 125°C	TLV2635ID TLV2635IDR	Tube Tape and Reel
TLV2635IN	DIP-16	N	—		TLV2635IN	Tube
TLV2635IPW	TSSOP-16	PW	—		TLV2635IPW TLV2635IPWR	Tube Tape and Reel

† The SOT23 package devices are only available taped and reeled. The R Suffix denotes quantities (3,000 pieces per reel).

‡ The T Suffix denotes smaller quantities (250 pieces per mini-reel).

1. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{DD}$ (see Note 1)	6 V
Differential input voltage, $V_{ID}$	$\pm V_{DD}$
Input voltage range, $V_I$ (see Note 1)	GND to $V_{DD} - 1$ V
Input current, $I_I$ (any input)	$\pm 10$ mA
Output current, $I_O$	$\pm 40$ mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : I-suffix	$-40^\circ\text{C}$ to $125^\circ\text{C}$
Maximum junction temperature, $T_J$	$150^\circ\text{C}$
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: All voltage values, except differential voltages, are with respect to GND.

**recommended operating conditions**

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$	Single supply	2.7	5.5	V
	Split supply	$\pm 1.35$	$\pm 2.75$	
Common-mode input voltage range, $V_{ICR}$		GND	$V_{DD}-1$	V
Operating free-air temperature, $T_A$	I-suffix	-40	125	$^\circ\text{C}$
Shutdown on/off voltage level‡	$V_{IL}$		0.4	V
	$V_{IH}$	2		

‡ Relative to GND.

**electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7$  V, 5 V (unless otherwise noted)**

**dc performance**

PARAMETER	TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$V_{IO}$ Input offset voltage	$V_{IC} = V_{DD}/2$ , $V_O = V_{DD}/2$	TLV2634/5	25 $^\circ\text{C}$	250	3500	$\mu\text{V}$
			Full range		4500	
		25 $^\circ\text{C}$	250	4200	$\mu\text{V}$	
		Full range		5200		
$\alpha_{VIO}$ Temperature coefficient of input offset voltage		25 $^\circ\text{C}$		3	$\mu\text{V}/^\circ\text{C}$	
CMRR Common-mode rejection ratio	$V_{IC} = \text{GND to } V_{DD}-1$ V	$V_{DD} = 2.7$ V	25 $^\circ\text{C}$	76	100	dB
			Full range	67		
		$V_{DD} = 5$ V	25 $^\circ\text{C}$	77	100	
			Full range	74		
$A_{VD}$ Large-signal differential voltage amplification	$R_L = 2$ k $\Omega$ , $V_{O(PP)} = V_{DD}-1$ V	25 $^\circ\text{C}$	90	100	dB	
		Full range	82			

**electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7\text{ V}, 5\text{ V}$  (unless otherwise noted) (continued)**

**input characteristics**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$I_{IO}$ Input offset current	$V_{IC} = V_{DD}/2,$ $V_O = V_{DD}/2$	25°C		1	50	pA
		Full range			100	
25°C				1	50	
		Full range			200	
$r_{i(d)}$ Differential input resistance		25°C		1000		GΩ
$C_{i(c)}$ Common-mode input capacitance	$f = 1\text{ kHz}$	25°C		12		pF

† Full range is –40°C to 125°C for the I-suffix.

**output characteristics**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT	
$V_{OH}$ High-level output voltage	$V_{IC} = V_{DD}/2, I_{OH} = -1\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C	2.6	2.67	V	
			Full range		2.55		
		$V_{DD} = 5\text{ V}$	25°C	4.92	4.98		
			Full range		4.9		
	$V_{IC} = V_{DD}/2, I_{OH} = -10\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C	2.25	2.43		
			Full range		2.15		
		$V_{DD} = 5\text{ V}$	25°C	4.7	4.8		
			Full range		4.65		
$V_{OL}$ Low-level output voltage	$V_{IC} = V_{DD}/2, I_{OL} = 1\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C		0.03	0.1	mV
			Full range			0.15	
		$V_{DD} = 5\text{ V}$	25°C		0.025	0.08	
			Full range			0.1	
	$V_{IC} = V_{DD}/2, I_{OL} = 10\text{ mA}$	$V_{DD} = 2.7\text{ V}$	25°C		0.26	0.45	
			Full range			0.47	
		$V_{DD} = 5\text{ V}$	25°C		0.2	0.3	
			Full range			0.35	
$I_O$ Output current	$V_{DD} = 2.7\text{ V},$ $V_O = 0.5\text{ V}$ from rail	Sourcing	25°C		14	mA	
		Sinking			19		
	$V_{DD} = 5\text{ V},$ $V_O = 0.5\text{ V}$ from rail	Sourcing			28		
		Sinking			28		
$I_{OS}$ Short-circuit output current	Sourcing	$V_{DD} = 2.7\text{ V}$	25°C		50	mA	
		$V_{DD} = 5\text{ V}$			95		
	Sinking	$V_{DD} = 2.7\text{ V}$			50		
		$V_{DD} = 5\text{ V}$			95		

† Full range is –40°C to 125°C for the I-suffix.

**power supply**

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	MIN	TYP	MAX	UNIT
$I_{DD}$ Supply current (per channel)	$V_O = V_{DD}/2,$ $\overline{\text{SHDN}} = V_{DD}$	25°C		730	1000	μA
		Full range			1350	
PSRR Supply voltage rejection ratio ( $\Delta V_{DD} / \Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V}$ to $5.5\text{ V},$ $V_{IC} = V_{DD}/2$	No load	25°C	70	90	dB
		Full range			65	

† Full range is –40°C to 125°C for the I-suffix.

electrical characteristics at specified free-air temperature,  $V_{DD} = 2.7\text{ V}, 5\text{ V}$  (unless otherwise noted)  
 (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
GBWP	Gain-bandwidth product	$R_L = 2\text{ k}\Omega, C_L = 10\text{ pF}, f = 10\text{ kHz}$		25°C		9		MHz
SR+	Positive slew rate at unity gain	$R_L = 2\text{ k}\Omega, C_L = 50\text{ pF}$	$V_{DD} = 2.7\text{ V}, V_{O(PP)} = 1.7\text{ V}$			6		V/ $\mu\text{s}$
			$V_{DD} = 5\text{ V}, V_{O(PP)} = 3.5\text{ V}$			6		
SR-	Negative slew rate at unity gain	$R_L = 2\text{ k}\Omega, C_L = 50\text{ pF}$	$V_{DD} = 2.7\text{ V}, V_{O(PP)} = 1.7\text{ V}$			10		V/ $\mu\text{s}$
			$V_{DD} = 5\text{ V}, V_{O(PP)} = 3.5\text{ V}$			9.5		V/ $\mu\text{s}$
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega, C_L = 10\text{ pF}$				50		°
	Gain margin				20		dB	

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for the I-suffix.

noise/distortion performance

PARAMETER		TEST CONDITIONS		$T_A$	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	$V_{O(PP)} = V_{DD}/2, R_L = 2\text{ k}\Omega, f = 10\text{ kHz}$	$A_V = 1$	25°C	0.003%			
			$A_V = 10$		0.02%			
			$A_V = 100$		0.095%			
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$			50			nV/ $\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$			30			
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$			0.9			fA/ $\sqrt{\text{Hz}}$

shutdown characteristics

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	MIN	TYP	MAX	UNIT
$I_{DD(SHDN)}$	Supply current, per channel in shutdown mode (TLV2630, TLV2633, TLV2635)	$\overline{\text{SHDN}} = 0.4\text{ V}$		25°C	4		17	$\mu\text{A}$
				Full range			19	
$t_{(on)}$	Amplifier turnon time $^\ddagger$	$R_L = 2\text{ k}\Omega, C_L = 10\text{ pF}$	$V_{DD} = 2.7\text{ V}$	25°C	4.5			$\mu\text{s}$
	$V_{DD} = 5\text{ V}$		1.5					
$t_{(off)}$	Amplifier turnoff time $^\ddagger$				200			ns

$^\dagger$  Full range is  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  for the I-suffix.

$^\ddagger$  Disable time and enable time are defined as the interval between application of the logic signal to  $\overline{\text{SHDN}}$  and the point at which the supply current has reached half its final value.

**DISSIPATION RATING TABLE**

PACKAGE	$\Theta_{JC}$ (°C/W)	$\Theta_{JA}$ (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.3	1022 mW	204.4 mW
D (16)	25.7	114.7	1090 mW	218 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DBV (6)	55	294.3	425 mW	85 mW
DGK (8)	54.2	259.9	481 mW	96.1 mW
DGS (10)	54.1	259.7	485 mW	97 mW
N (14, 16)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW
PW (16)	28.7	161.4	774 mW	154.9 mW

**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			FIGURE
$V_{IO}$	Input offset voltage	vs Common-mode input voltage	1, 2
CMRR	Common-mode rejection ratio	vs Frequency	3
$V_{OH}$	High-level output voltage	vs High-level output current	4, 6
$V_{OL}$	Low-level output voltage	vs Low-level output current	5, 7
$I_{DD}$	Supply current	vs Supply voltage	8
$I_{DD}$	Supply current	vs Free-air temperature	9
PSRR	Power supply rejection ratio	vs Frequency	10
$A_{VD}$	Differential voltage amplification & phase	vs Frequency	11
	Gain-bandwidth product	vs Supply voltage	12
		vs Free-air temperature	13
SR	Slew rate	vs Supply voltage	14
		vs Free-air temperature	15, 16
$\phi_m$	Phase margin	vs Load capacitance	17
$V_n$	Equivalent input noise voltage	vs Frequency	18
	Crosstalk	vs Frequency	19
	Voltage-follower large-signal pulse response		20
	Voltage-follower small-signal pulse response		21
$I_{DD(SHDN)}$	Shutdown supply current	vs Free-air temperature	22
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	23
$I_{DD(SHDN)}$	Shutdown supply current/output voltage	vs Time	24

TYPICAL CHARACTERISTICS

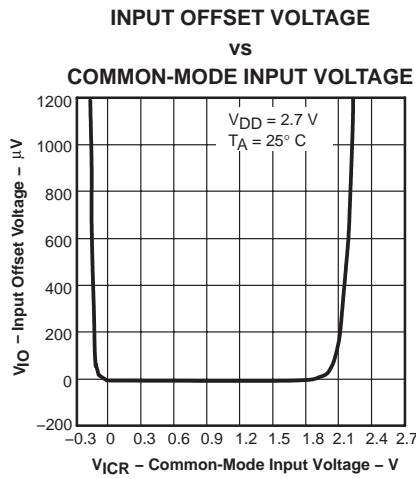


Figure 1

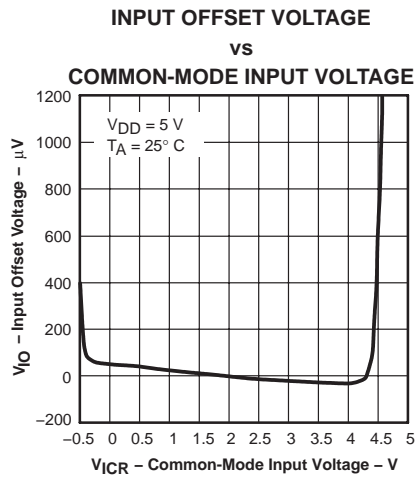


Figure 2

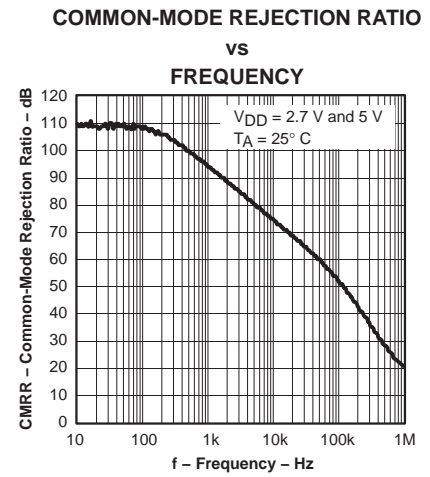


Figure 3

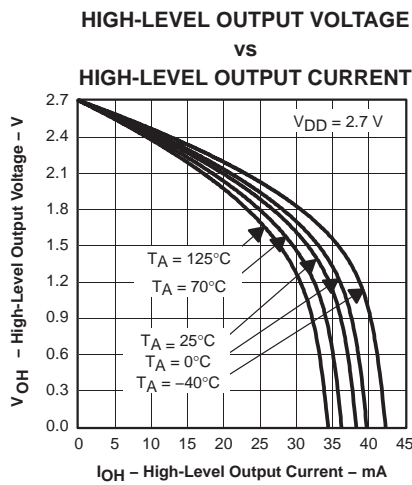


Figure 4

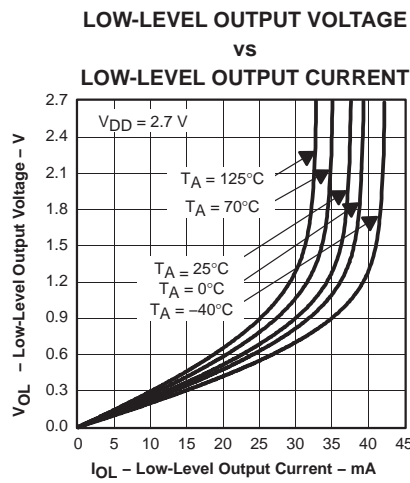


Figure 5

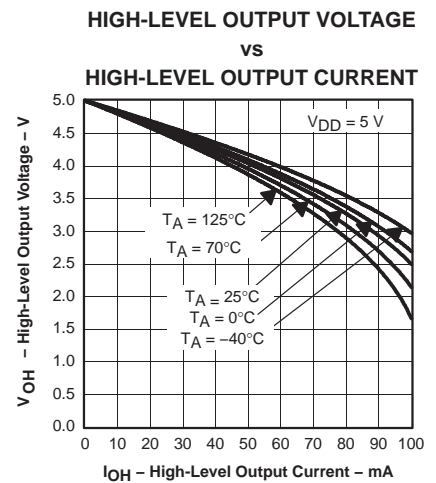


Figure 6

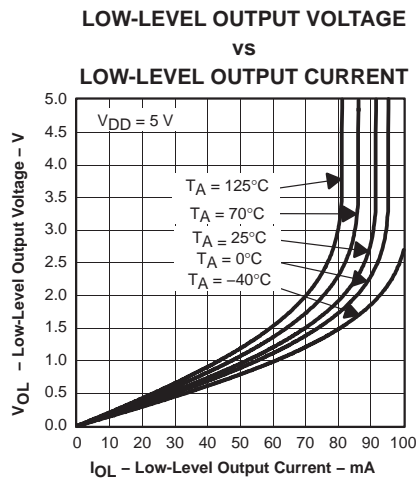


Figure 7

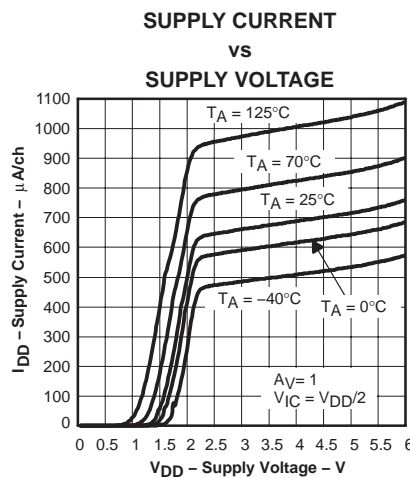


Figure 8

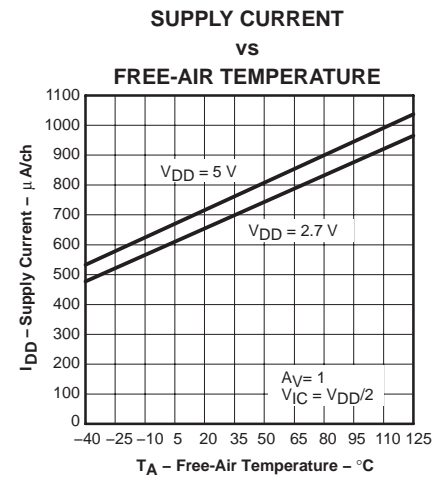


Figure 9

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO

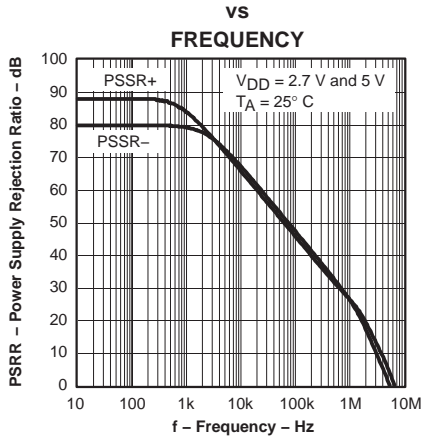


Figure 10

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE

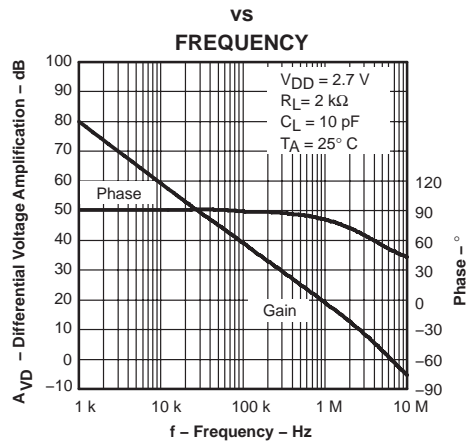


Figure 11

GAIN-BANDWIDTH PRODUCT

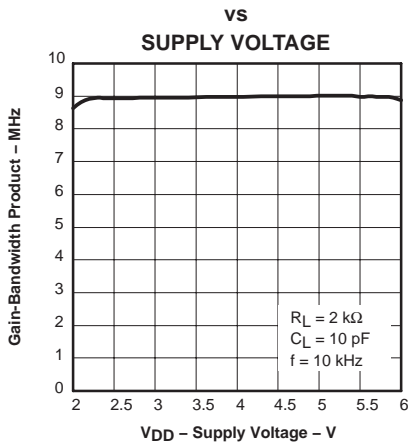


Figure 12

GAIN-BANDWIDTH PRODUCT

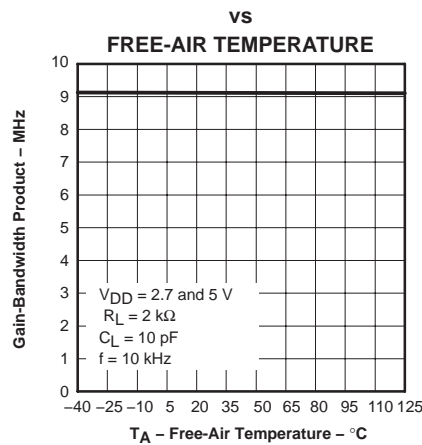


Figure 13

SLEW RATE

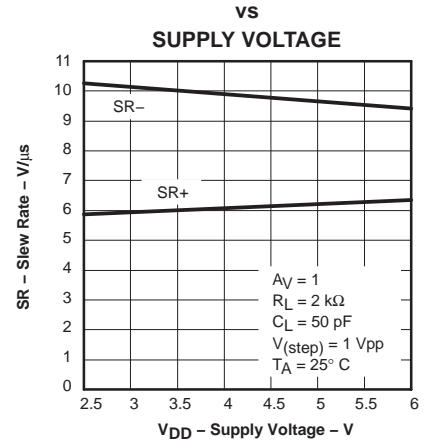


Figure 14

SLEW RATE

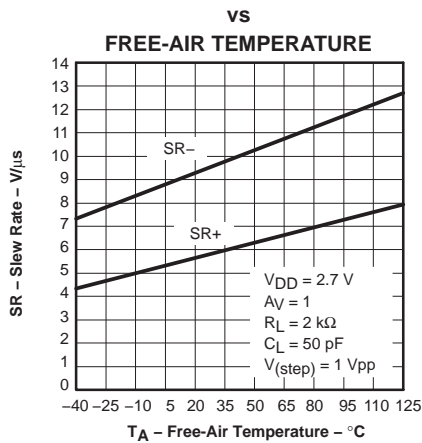


Figure 15

SLEW RATE

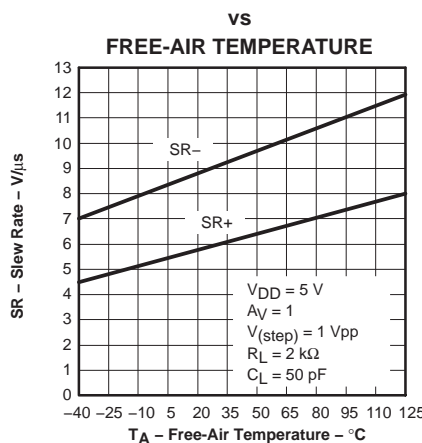


Figure 16

PHASE MARGIN

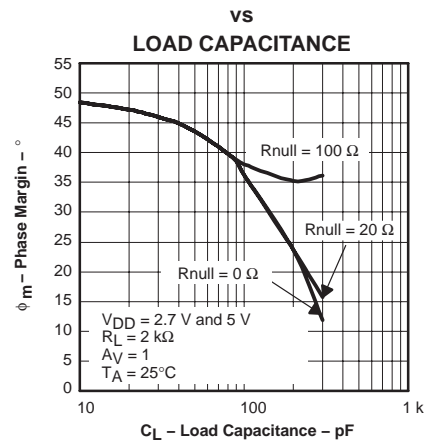


Figure 17



TYPICAL CHARACTERISTICS

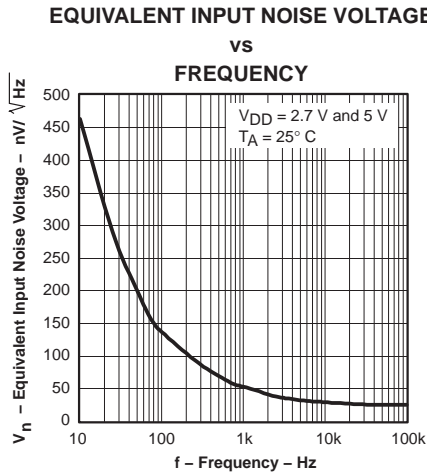


Figure 18

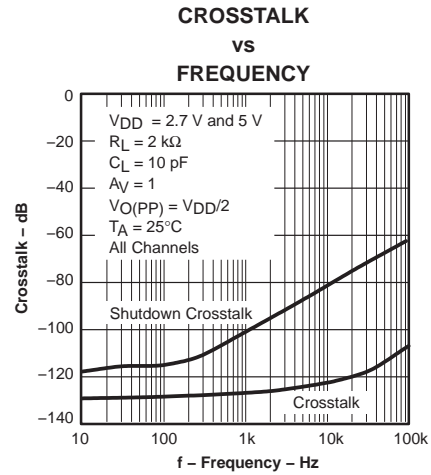


Figure 19

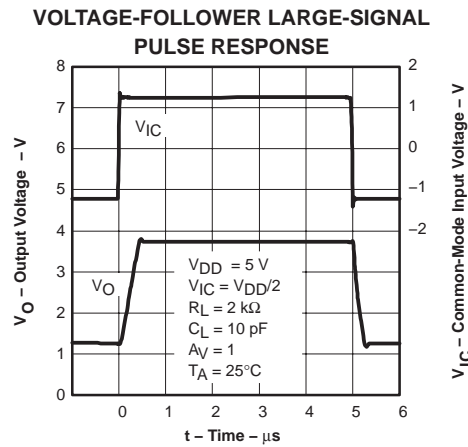


Figure 20

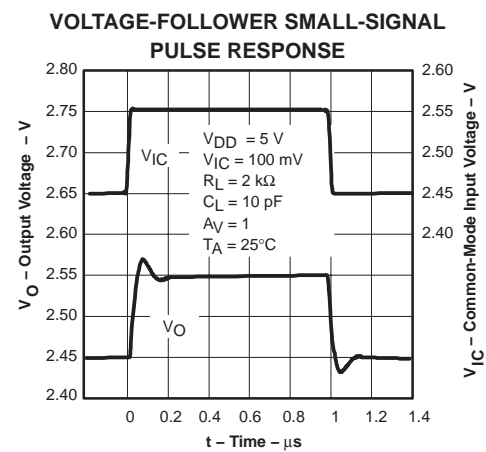


Figure 21

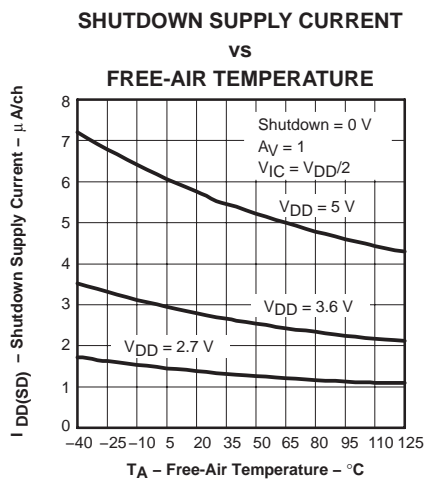


Figure 22

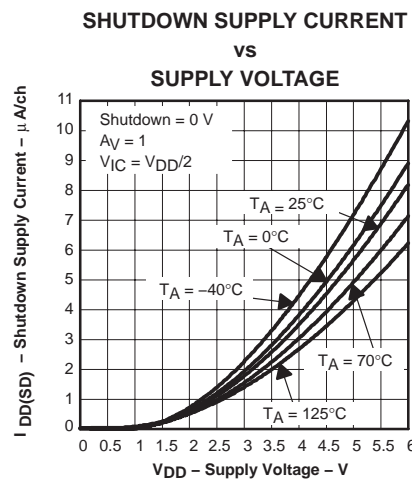


Figure 23

### TYPICAL CHARACTERISTICS

#### SHUTDOWN SUPPLY CURRENT / OUTPUT VOLTAGE vs TIME

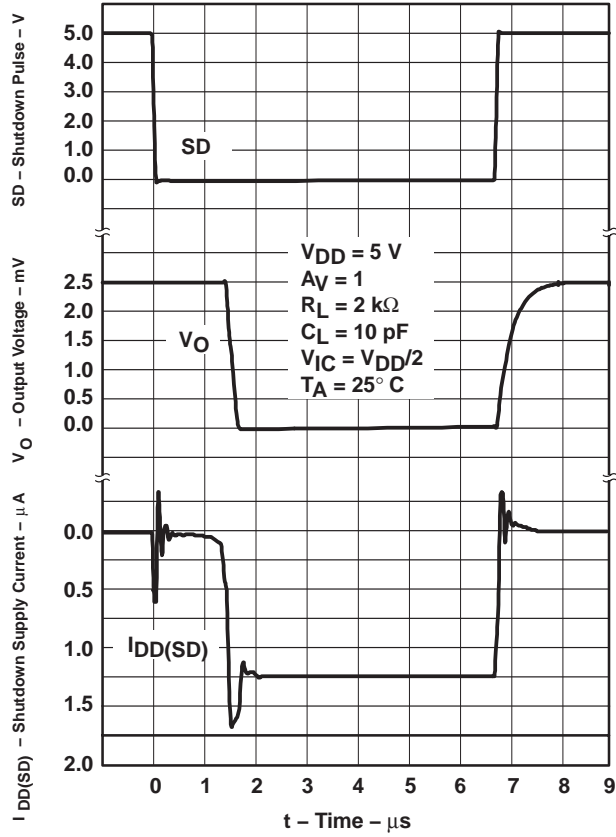
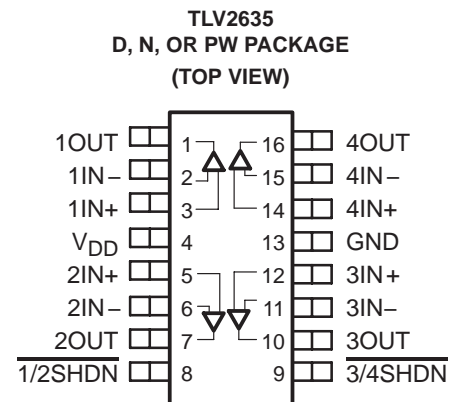
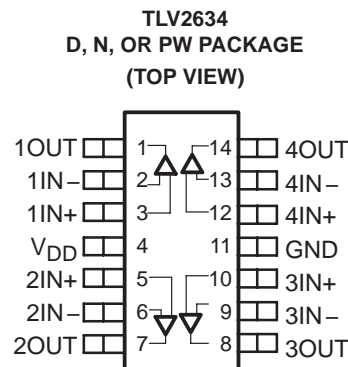
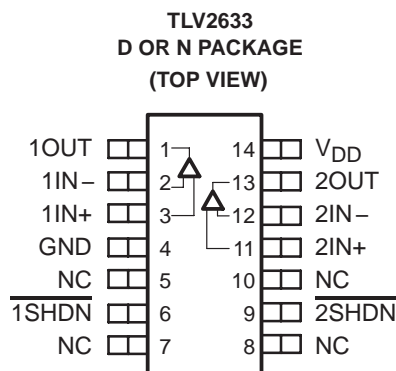
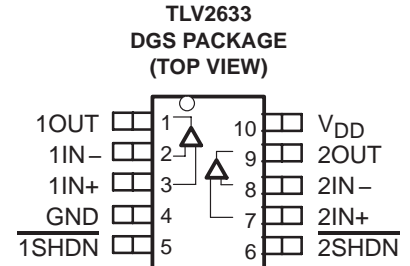
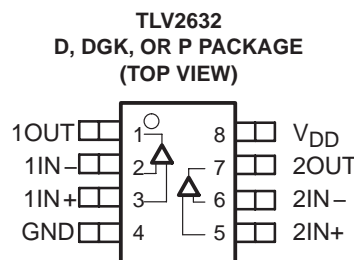
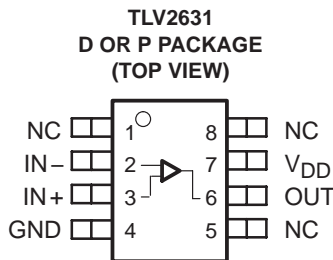
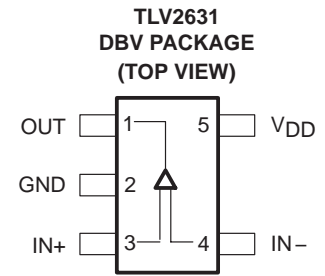
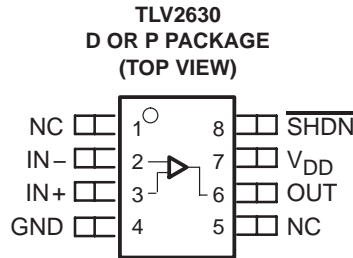
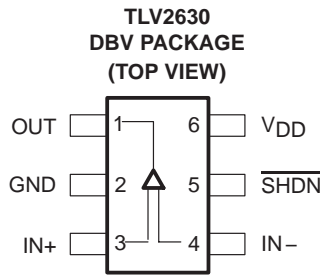


Figure 24

**TLV263x PACKAGE PINOUTS**



NC – No internal connection

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLV2630IDBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAYI
TLV2630IDBVR.A	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAYI
<a href="#">TLV2631IDBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAZI
TLV2631IDBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAZI
<a href="#">TLV2631IDBVT</a>	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAZI
TLV2631IDBVT.A	Active	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAZI
<a href="#">TLV2632IDGKR</a>	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKG
TLV2632IDGKR.A	Active	Production	VSSOP (DGK)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AKG
<a href="#">TLV2632IDR</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2632I
TLV2632IDR.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2632I
<a href="#">TLV2634ID</a>	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2634I
TLV2634ID.A	Active	Production	SOIC (D)   14	50   TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2634I
<a href="#">TLV2634IPWR</a>	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2634I
TLV2634IPWR.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2634I

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2630IDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2631IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2631IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2632IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2632IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2634IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

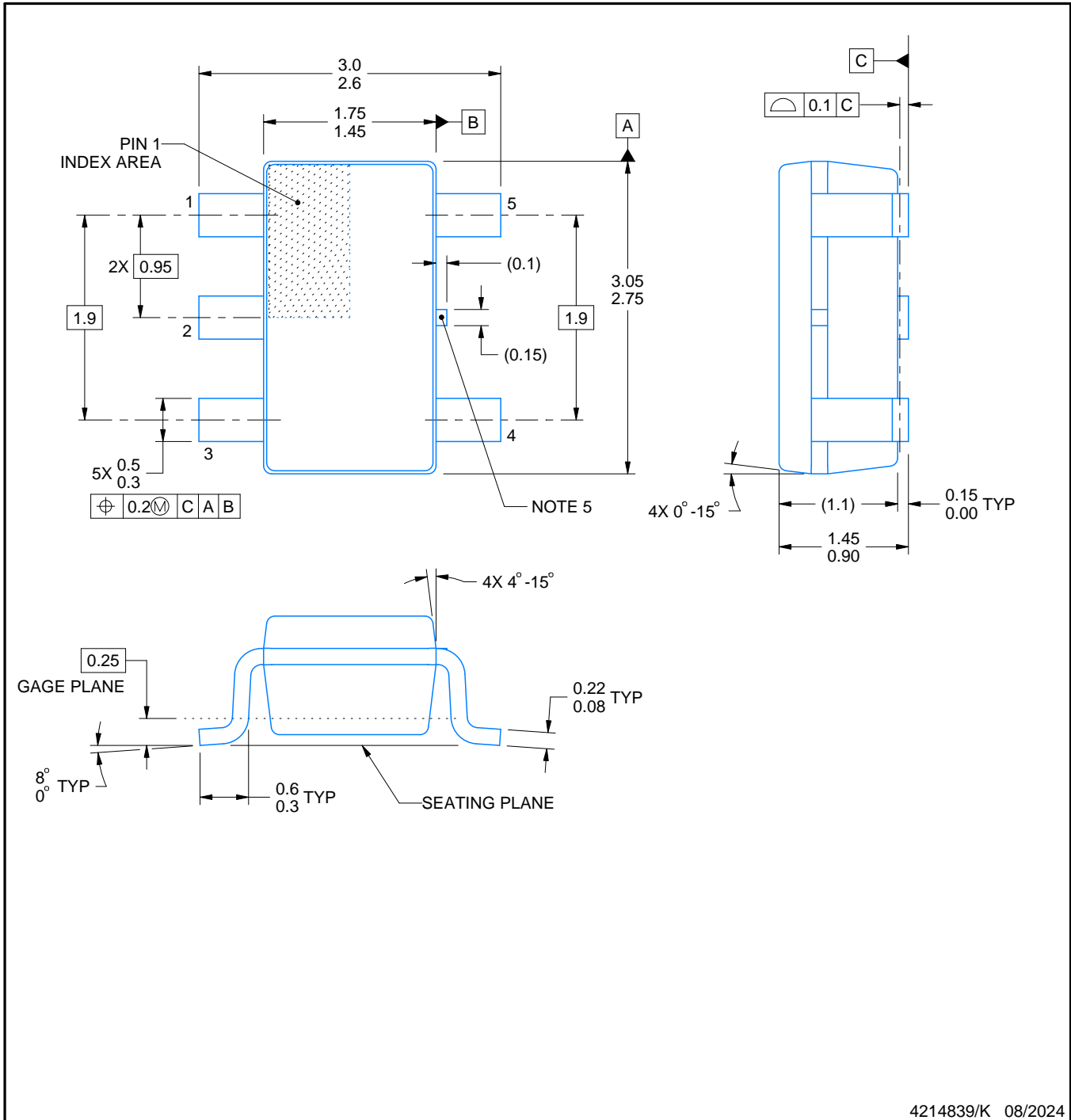
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2630IDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2631IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2631IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2632IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2632IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2634IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2634ID	D	SOIC	14	50	507	8	3940	4.32
TLV2634ID.A	D	SOIC	14	50	507	8	3940	4.32





4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

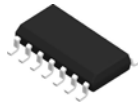


SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



# D0014A

# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DBV0006A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

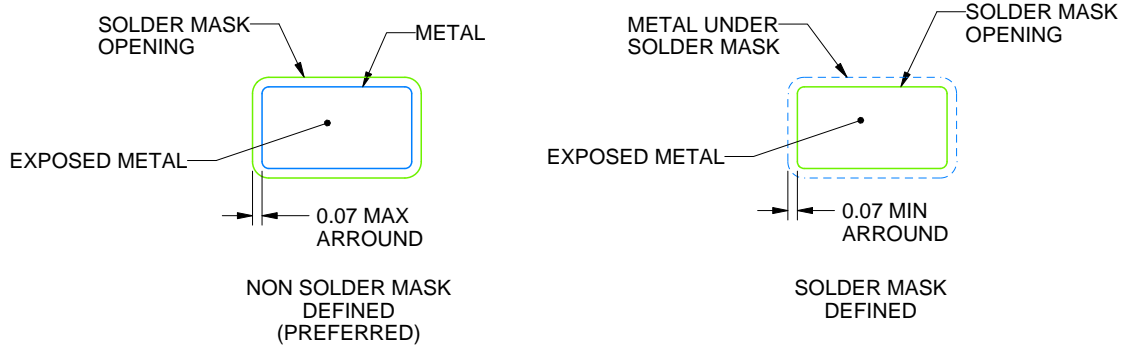
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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