TLV320ADC3100 Low-Power Stereo ADC for Voice-Activated Systems and Portable Audio

1 Features

- Stereo Audio ADC:
  - 92-dBA Signal-to-Noise Ratio
  - Supports ADC Sample Rates From 8 kHz to 96 kHz
- Flexible Digital Filtering With Programmable Coefficients and Built-In Processing Blocks:
  - Low-Latency IIR Filters for Voice
  - Linear Phase FIR Filters for Audio
  - Up to 5 Additional Programmable Bi-Quad Filters
  - Programmable High-Pass Filter
- Four Audio Inputs With Configurable Automatic Gain Control (AGC):
  - Programmable in Single-Ended or Fully Differential Configurations
  - Optionally Tri-Stated for Easy Interoperability With Other Audio Devices
- Low Power Consumption and Extensive Modular Power Control:
  - 6-mW Mono Record, 8-kHz
  - 11-mW Stereo Record, 8-kHz
  - 10-mW Mono Record, 48-kHz
  - 17-mW Stereo Record, 48-kHz
- Programmable Microphone Bias
- Programmable PLL for Clock Generation
- I^2C Control Bus
- Audio Serial Data Bus Supports I^2S, Left- and Right-Justified, DSP, PCM, and TDM Modes
- Power Supplies:
  - Analog: 2.7 V to 3.6 V
  - Digital: Core: 1.65 V to 1.95 V, I/O: 1.1 V–3.6 V
- Package: 4-mm × 4-mm, 24-Pin RGE (VQFN)

2 Applications

- Voice-Activated Systems
- Smart Speakers, Voice-Enabled Assistants
- Portable Low-Power Audio Systems
- Noise-Cancellation Systems
- Front-End Voice or Audio Processors for Digital Audio

3 Description

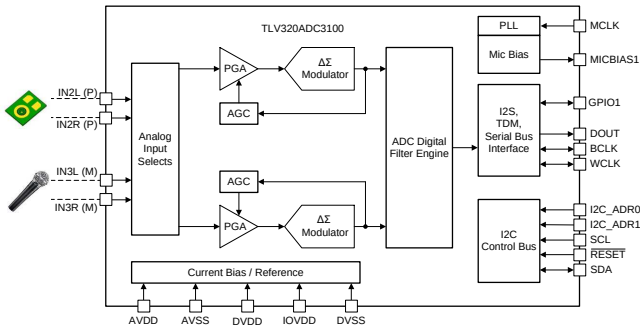
The TLV320ADC3100 is a low-power, stereo audio analog-to-digital converter (ADC) supporting sampling rates from 8 kHz to 96 kHz with an integrated programmable-gain amplifier (PGA) providing up to 40-dB analog gain or automatic gain control (AGC). Front-end input coarse attenuation of 0 dB, –6 dB, or off, is also provided. The inputs are programmable in a combination of single-ended or fully differential configurations. Extensive register-based power control is available via an I^2C interface, enabling mono or stereo recording. The TLV320ADC3100 integrates programable channel gain, digital volume control, a phase-locked loop (PLL), programmable biquad filters, and low latency filter modes. Pre-programmed built-in processing blocks (PRBs) that can be chosen based on the specific application needs, allows optimization of performance and power. Low power consumption coupled with its flexibility make the TLV320ADC3100 ideal for battery-powered portable equipment. The TLV320ADC3100 is form-factor and software compatible with the TLV320ADC3101.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV320ADC3100	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2018	*	Initial release.

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5 Description (continued)

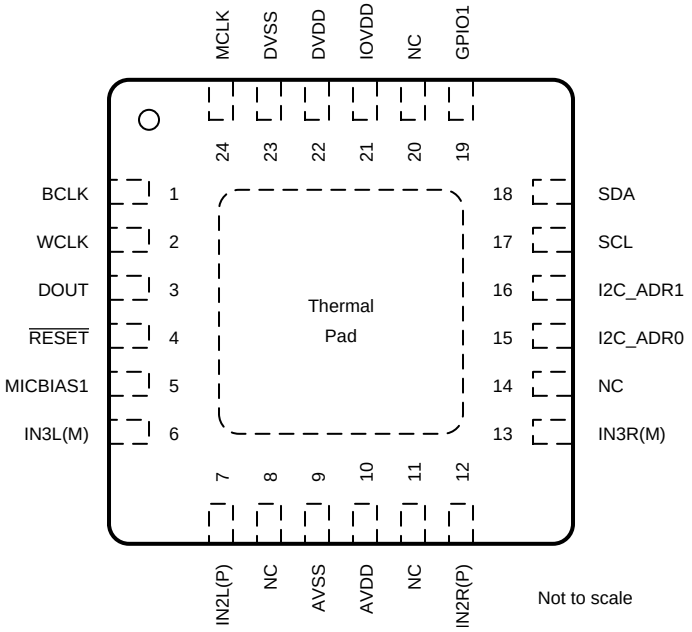
The AGC programs to a wide range of attack (7 ms to 1.4 s) and decay (50 ms to 22.4 s) times. A programmable noise-gate function is included to avoid noise pumping. Low-latency interrupt identification register (IIR) filters optimized for voice and telephony are available, as well as linear-phase finite impulse response (FIR) filters optimized for audio. Programmable IIR filters are also available and can be used for sound equalization, or to remove noise components. The audio serial bus can be programmed to support I^2S, left-justified, right-justified, digital signal processor (DSP), pulse code modulation (PCM), and time-division multiplexing (TDM) modes. The audio bus can be operated in either master or slave mode.

A programmable integrated PLL is included for flexible clock generation and provides support for all standard audio rates from a wide range of available MCLKs, varying from 512 kHz to 50 MHz, including the most popular cases of 12-MHz, 13-MHz, 16-MHz, 19.2-MHz, and 19.68-MHz system clocks.

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6 Pin Configuration and Functions

RGE Package
24-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AVDD	10	P	Analog voltage supply, 2.7 V–3.6 V
AVSS	9	P	Analog ground supply, 0 V
BCLK	1	I/O	Audio serial data bus bit clock
DOUT	3	O	Audio serial data bus data output
DVDD	22	P	Digital core voltage supply, 1.65 V–1.95 V
DVSS	23	P	Digital ground supply, 0 V
GPIO1	19	I/O	General-purpose input/output 1, multifunction pin based on register programming
I2C_ADR0	15	I	LSB of I^2C bus address
I2C_ADR1	16	I	LSB + 1 of I^2C bus address
IN2L(P)	7	I	Microphone or line analog input (left-channel single-ended or differential plus)
IN2R(P)	12	I	Microphone or line analog input (right-channel single-ended or differential plus)
IN3L(M)	6	I	Microphone or line analog input (left-channel single-ended or differential minus)
IN3R(M)	13	I	Microphone or line analog input (right-channel single-ended or differential minus)
IOVDD	21	P	I/O voltage supply, 1.1 V–3.6 V
MCLK	24	I	Master clock input
MICBIAS1	5	O	MICBIAS1 bias voltage output
NC	8, 11, 14, 20	—	No connection
$\overline{\text{RESET}}$	4	I	Reset
SCL	17	I/O	I^2C serial clock
SDA	18	I/O	I^2C serial data input/output
WCLK	2	I/O	Audio serial data bus word clock
Thermal pad	Pad	—	Connect the thermal pad to AVSS.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
	AVDD to AVSS	–0.3	3.9	V
	IOVDD to DVSS	–0.3	3.9	V
	DVDD to DVSS	–0.3	2.5	V
	Digital input voltage to DVSS	–0.3	IOVDD + 0.3	V
	Analog input voltage to AVSS	–0.3	AVDD + 0.3	V
	Operating temperature	–40	85	°C
T_J Max	Junction temperature		105	°C
	Power dissipation		$(T_J \text{ Max} – T_A) / \theta_{JA}$	W
T_{stg}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ESD complacence tested to EIA/JESD22-A114-B and passed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage(1)	2.7	3.3	3.6	V
DVDD	Digital core supply voltage(1)	1.65	1.8	1.95	V
IOVDD	Digital I/O supply voltage(1)	1.1	1.8	3.6	V
V_I	Analog full-scale, 0-dB input voltage (AVDD = 3.3 V)		0.707		Vrms
	Digital output load capacitance		10		pF
T_A	Operating free-air temperature	–40		85	°C

(1) Analog voltage values are with respect to AVSS; digital voltage values are with respect to DVSS.

7.4 Thermal Information

THERMAL METRIC(1)		TLV320ADC3100 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

at 25°C, AVDD = 3.3 V, IOVDD = 1.8 V, DVDD = 1.8 V, f_S = 48-kHz, and 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO ADC						
	Input signal level (0-dB)	Single-ended input		0.707		Vrms
	Input common-mode voltage	Single-ended input		1.35		Vrms
SNR	Signal-to-noise ratio, A-weighted(1)(2)	f_S = 48 kHz, 0-dB PGA gain, IN1 inputs selected and AC-shorted to ground	80	92		dB
	Dynamic range, A-weighted(1)(2)	f_S = 48 kHz; 1-kHz, –60-dB, full-scale input applied at IN1 inputs; 0-dB PGA gain		92		dB
THD	Total harmonic distortion	f_S = 48 kHz; 1-kHz, –2-dB, full-scale input applied at IN1 inputs; 0-dB PGA gain		–90	–75	dB
				0.003%	0.017%	
PSRR	Power-supply rejection ratio	234 Hz, 100 mV_{PP} on AVDD, single-ended input		46		dB
		234 Hz, 100 mV_{PP} on AVDD, differential input		68		
	ADC channel separation	1 kHz, –2-dB IN2L to IN2R		–73		dB
	ADC gain error	1 kHz input, 0-dB PGA gain		0.7		dB
	ADC programmable-gain amplifier maximum gain	1-kHz input tone, R_{SOURCE} < 50 Ω		40		dB
	ADC programmable-gain amplifier step size			0.502		dB
	Input resistance	IN1 inputs, routed to single ADC, input mix attenuation = 0 dB		35		kΩ
		IN2 inputs, input mix attenuation = 0 dB		35		
		IN1 inputs, input mix attenuation = –6 dB		62.5		
		IN2 inputs, input mix attenuation = –6 dB		62.5		
	Input capacitance			10		pF
	Input level control minimum attenuation setting			0		dB
	Input level control maximum attenuation setting			6		dB
	Input level control attenuation step size			6		dB

(1) Ratio of output level with 1-kHz, full-scale, sine-wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz, low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD and lower SNR and dynamic range readings than shown in the *Electrical Characteristics* table. The low-pass filter removes out-of-band noise that, although not audible, may affect dynamic specification values.

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Electrical Characteristics (continued)

at 25°C, AVDD = 3.3 V, IOVDD = 1.8 V, DVDD = 1.8 V, f_S = 48-kHz, and 16-bit audio data (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC DIGITAL DECIMATION FILTER (f_S = 48 kHz)							
	Filter gain from 0 f_S to 0.39 f_S	Filter A, AOSR = 128 or 64			±0.1		dB
	Filter gain from 0.55 f_S to 64 f_S	Filter A, AOSR = 128 or 64			–73		dB
	Filter group delay	Filter A, AOSR = 128 or 64			17 / f_S		s
	Filter gain from 0 f_S to 0.39 f_S	Filter B, AOSR = 64			±0.1		dB
	Filter gain from 0.60 f_S to 32 f_S	Filter B, AOSR = 64			–46		dB
	Filter group delay	Filter B, AOSR = 64			11 / f_S		s
	Filter gain from 0 f_S to 0.39 f_S	Filter C, AOSR = 32			±0.033		dB
	Filter gain from 0.28 f_S to 16 f_S	Filter C, AOSR = 32			–60		dB
	Filter group delay	Filter C, AOSR = 32			11 / f_S		s
MICROPHONE BIAS							
	Bias voltage	Programmable settings, load = 750 Ω			2		V
				2.25	2.5	2.75	
					AVDD – 0.2		
	Current sourcing	2.5-V setting				4	mA
	Integrated noise	BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AGND			3.3		µV rms
DIGITAL I/O							
V_{IL}	Input low level	I_{IL} = 5 µA		–0.3		0.3 × IOVDD	V
V_{IH}	Input high level(3)	I_{IH} = 5 µA		0.7 × IOVDD			V
V_{OL}	Output low level	I_{IH} = 2 TTL loads				0.1 × IOVDD	V
V_{OH}	Output high level	I_{OH} = 2 TTL loads		0.8 × IOVDD			V
SUPPLY CURRENT (f_S = 48 kHz, AVDD = 3.3 V, DVDD = IOVDD = 1.8 V)							
	Mono record	AVDD	PLL and AGC off		2		mA
		DVDD			1.9		
	Stereo record	AVDD	PLL and AGC off		4		mA
		DVDD			2.1		
	PLL	AVDD	Additional power consumed when PLL is powered		1.1		mA
		DVDD			0.8		
	Power down	AVDD	All supply voltages applied, all blocks programmed in lowest power state		0.04		µA
		DVDD			0.7		

(3) When IOVDD < 1.6 V, the minimum V_{IH} is 1.1 V.

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7.6 Timing Requirements: I²S, LJF, RJF Timing in Master Mode

specified at 25°C, DVDD = 1.8 V, all timing specifications are measured at characterization; see Figure 1 for a timing diagram

		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	BCLK, WCLK delay time		20		15	ns
t_d(DO-WS)	BCLK, WCLK to DOUT delay time		25		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		20		15	ns
t_r	Rise time		20		15	ns
t_f	Fall time		20		15	ns

7.7 Timing Requirements: DSP Timing in Master Mode

specified at 25°C, DVDD = 1.8 V, all timing specifications are measured at characterization; see Figure 2 for a timing diagram

		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	BCLK, WCLK delay time		25		15	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		25		15	ns
t_r	Rise time		20		15	ns
t_f	Fall time		20		15	ns

7.8 Timing Requirements: I²S, LJF, RJF Timing in Slave Mode

specified at 25°C, DVDD = 1.8 V, all timing specifications are measured at characterization; see Figure 3 for a timing diagram

		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	BCLK, WCLK setup time	10		6		ns
t_h(WS)	BCLK, WCLK hold time	10		6		ns
t_d(DO-WS)	BCLK, WCLK to DOUT delay time (for LJF mode only)		30		30	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		25		20	ns
t_r	Rise time		16		8	ns
t_f	Fall time		16		8	ns

7.9 Timing Requirements: DSP Timing in Slave Mode

specified at 25°C, DVDD = 1.8 V, all timing specifications are measured at characterization; see Figure 4 for a timing diagram

		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	BCLK, WCLK setup time	10		8		ns
t_h(WS)	BCLK, WCLK hold time	10		8		ns
t_d(DO-BCLK)	BCLK to DOUT delay time		25		20	ns
t_r	Rise time		15		8	ns
t_f	Fall time		15		8	ns

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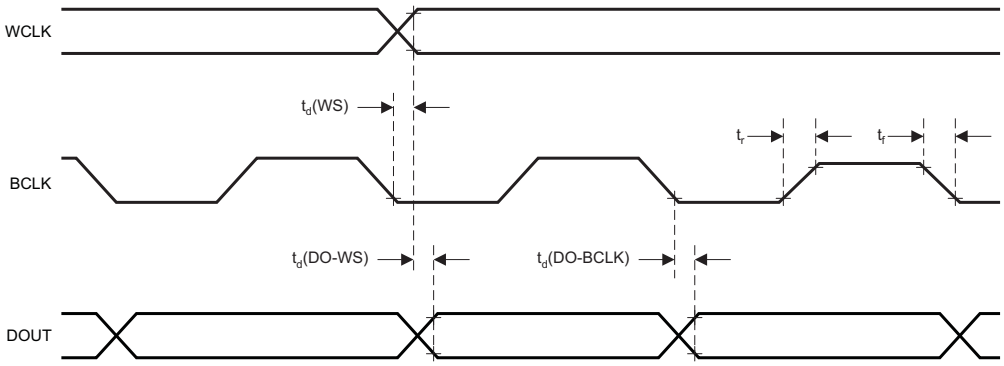


Figure 1. I²S, LJF, RJF Timing in Master Mode

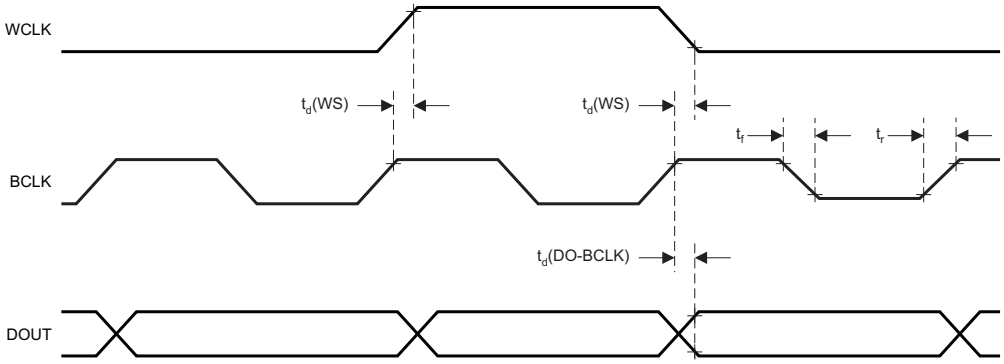


Figure 2. DSP Timing in Master Mode

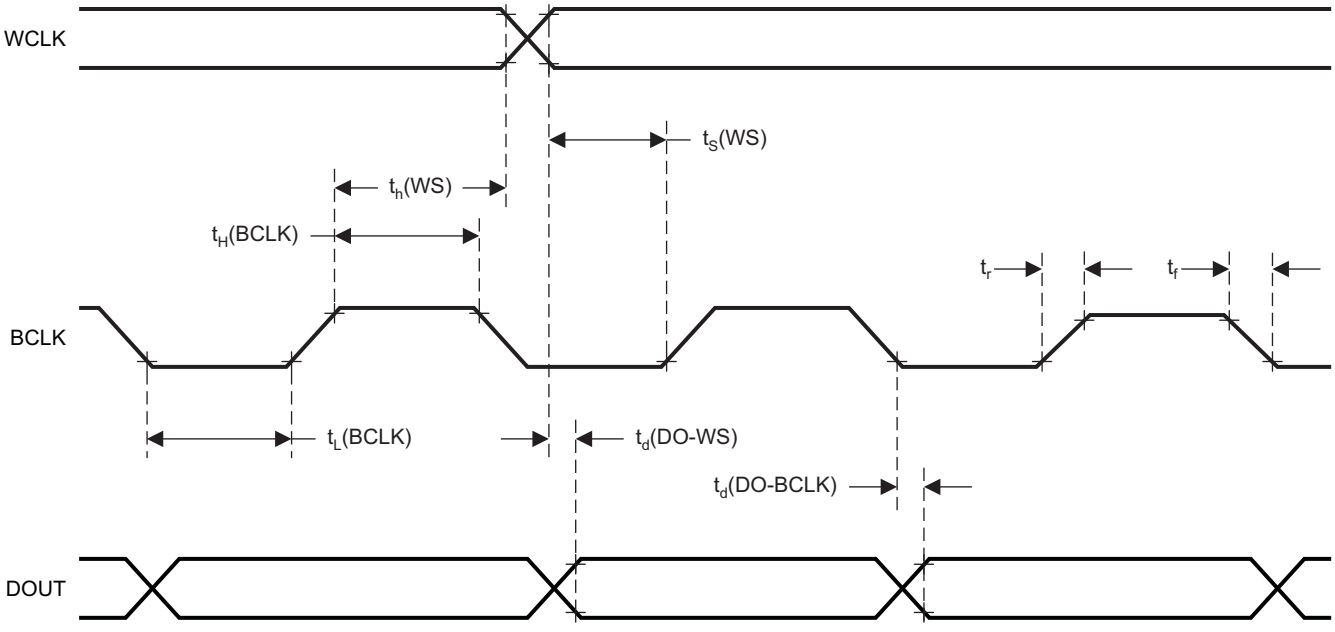
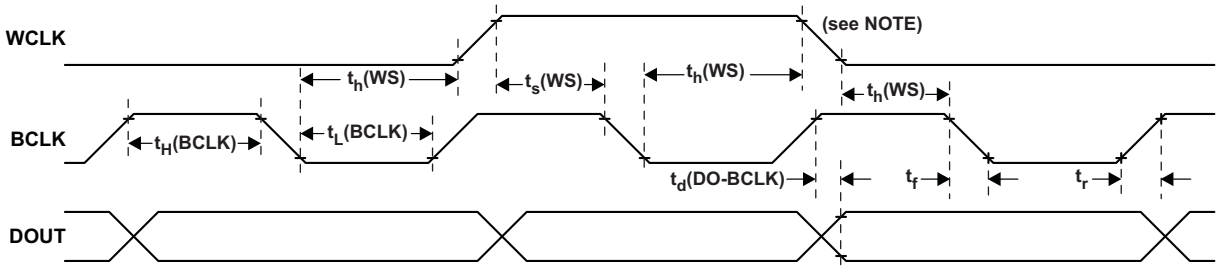


Figure 3. I²S, LJF, RJF Timing in Slave Mode



NOTE: The WCLK falling edge is arbitrary inside a frame.

Figure 4. DSP Timing in Slave Mode

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7.10 Typical Characteristics

at 25°C, AVDD = 3.3 V, IOVDD = 1.8 V, DVDD = 1.8 V, f_S = 48-kHz, and 16-bit audio data (unless otherwise noted)

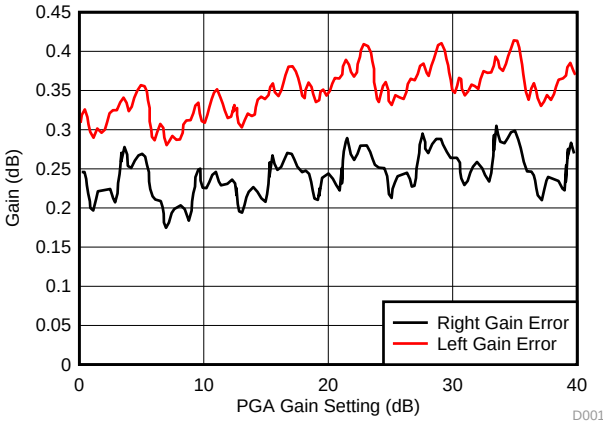


Figure 5. Single-Ended Gain Error

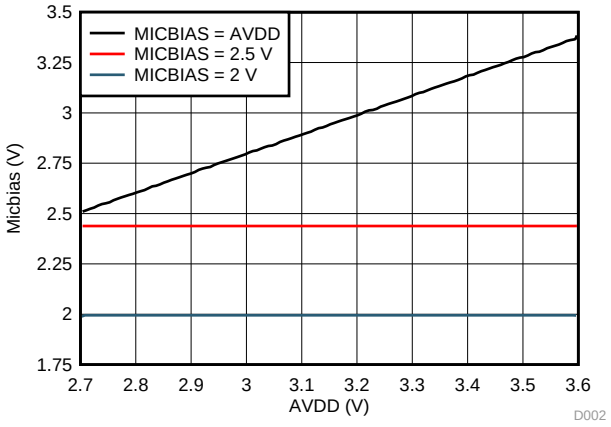


Figure 6. MICBIAS Output Voltage vs AVDD

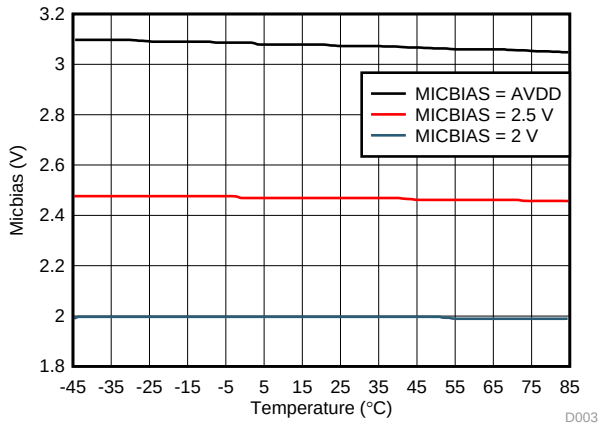


Figure 7. MICBIAS Output Voltage vs Ambient Temperature

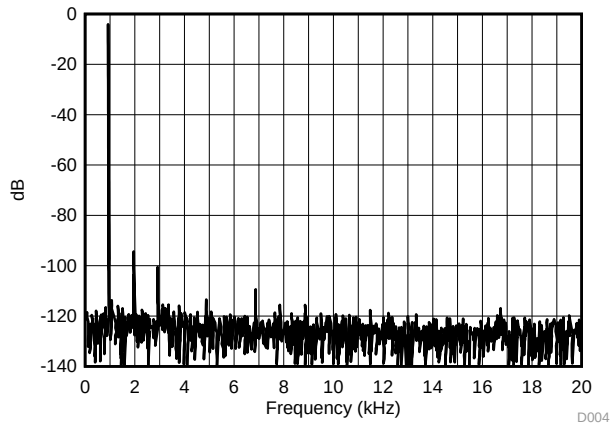


Figure 8. Line Input to ADC FFT Plot

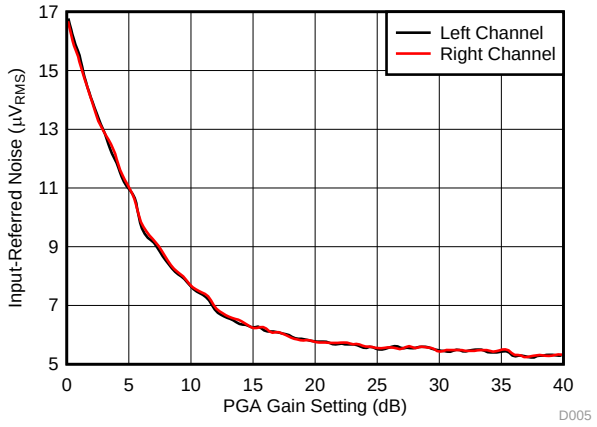


Figure 9. Input-Referred Noise vs PGA Gain

8 Detailed Description

8.1 Overview

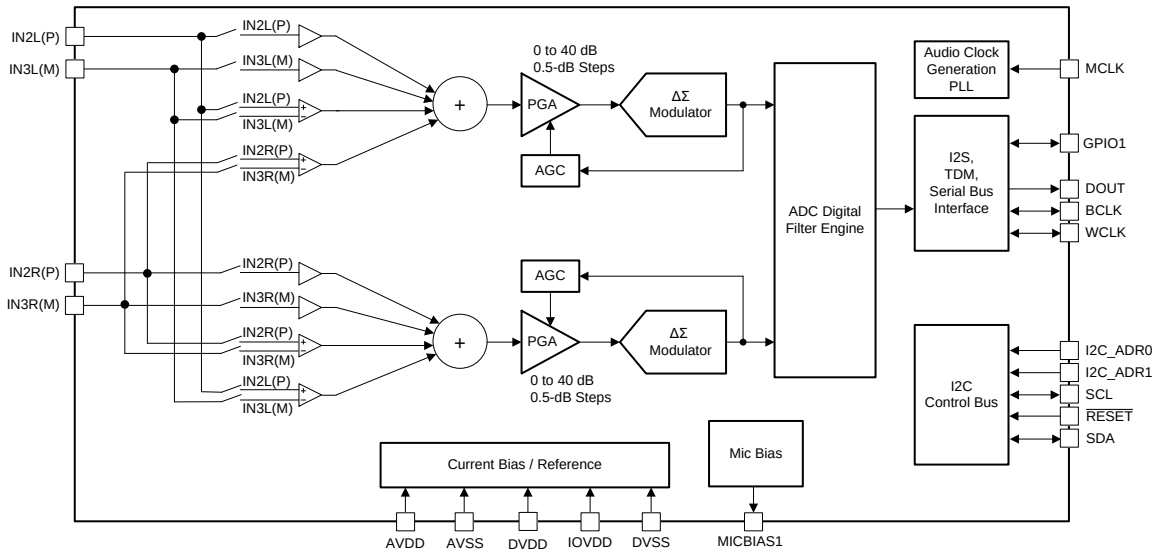
The TLV320ADC3100 is a flexible, low-power, stereo audio analog-to-digital converter (ADC) with extensive feature integration, intended for applications in voice-activated systems, portable computing, communication, and entertainment applications. The device integrates a host of features to reduce cost, board space, and power consumption in space-constrained, battery-powered, portable applications. The TLV320ADC3100 is form-factor and software compatible with the more feature-rich TLV320ADC3101, which has additional features such as a programmable miniDSP.

The TLV320ADC3100 consists of the following blocks:

- Stereo audio multibit delta-sigma ADC (8 kHz–96 kHz)
- Programmable digital filter engines including biquads
- Register-configurable combinations of up to four single-ended or two differential audio inputs
- Fully programmable phase-locked loop (PLL) with extensive ADC clock-source and divider options for maximum end-system design flexibility

Communication to the TLV320ADC3100 for control is via a two-wire I^2C interface. The I^2C interface supports both standard and fast communication modes.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Hardware Reset

The TLV320ADC3100 requires a hardware reset after power up for proper operation. After all power supplies are at their specified values, the $\overline{\text{RESET}}$ pin must be driven low for at least 10 ns. If this reset sequence is not performed, the TLV320ADC3100 may not respond properly to register reads or writes.

8.3.2 PLL Start-up

When the PLL is powered on, a start-up delay of approximately 10 ms occurs after the power-up command of the PLL and before the clocks are available to the TLV320ADC3100. This delay is to ensure stable operation of the PLL and clock-divider logic.

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Feature Description (continued)

8.3.3 Software Power Down

By default, all circuit blocks are powered down following a reset condition. Hardware power up of each circuit block can be controlled by writing to the appropriate control register. This approach allows the lowest power-supply current for the functionality required. However, when a block is powered down, all register settings are maintained as long as power is applied to the device.

8.3.4 Audio Data Converters

The TLV320ADC3100 supports the following standard audio sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz. The converters can also operate at different sampling rates in various combinations, as described in this section.

The TLV320ADC3100 supports a wide range of options for generating clocks for the ADC section as well as the digital interface section and the other control blocks; see Figure 27. The ADC clocks require a source reference clock. The clock can be provided on the device pins MCLK and BCLK. The source reference clock for the ADC section can be chosen by programming the ADC_CLKIN value on page 0, register 4, bits 1:0. The ADC_CLKIN can then be routed through highly flexible clock dividers (see Figure 27) to generate various clocks required for the ADC and programmable digital filter sections. In the event that the desired audio or programmable digital filter clocks cannot be generated from the external reference clocks on MCLK and BCLK, the TLV320ADC3100 also provides the option of using an on-chip PLL that supports a wide range of fractional multiplication values to generate the required system clocks. Starting from ADC_CLKIN, the TLV320ADC3100 provides several programmable clock dividers to support a variety of sampling rates for the ADC and the clocks for the programmable digital filter section.

8.3.5 Digital Audio Data Serial Interface

Audio data are transferred between the host processor and the TLV320ADC3100 via the digital-audio serial-data interface, or audio bus. The audio bus on this device is flexible, including left- or right-justified data options, support for I^2S or pulse code modulation (PCM) protocols, programmable data-length options, a time-division multiplexing (TDM) mode for multichannel operation, flexible master and slave configurability for each bus clock line, and the ability to directly communicate with multiple devices within a system.

The audio serial interface on the TLV320ADC3100 has an extensive I/O control for communication with two independent processors for audio data. The processors can communicate with the device one at a time. This feature is enabled by register programming of the various pin selections.

The audio bus of the TLV320ADC3100 can be configured for left- or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with the data width programmable in 16, 20, 24, or 32 bits by configuring page 0, register 27, bits 5:4. In addition, the word clock and bit clock can be independently configured in either master or slave mode for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and can be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum-selected ADC sampling frequency.

The bit clock is used to clock in and out the digital audio data across the serial bus. When in master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in page 0, register 30; see Figure 27. Accommodating various word lengths as well as supporting the case when multiple TLV320ADC3100s share the same audio bus may require that the number of bit-clock pulses in a frame be adjusted.

The TLV320ADC3100 also includes a feature to offset the position of the start of a data transfer with respect to the word clock. There are two configurations that allow using either a single offset for both channels or to use separate offsets. The Ch_Offset_1 reference represents the value in page 0, register 28 and Ch_Offset_2 represents the value in page 0, register 37. When page 0, register 38, bit 0 is set to zero (time-slot-based channel assignment is disabled), the offset of both channels is controlled, in terms of number of bit clocks, by the programming in page 0, register 28 (Ch_Offset_1). When page 0, register 38, bit 0 = 1 (time-slot-based channel assignment enabled), the first channel is controlled, in terms of number of bit clocks, by the programming in page 0, register 28 (Ch_Offset_1), and the second channel is controlled, in terms of number of bit clocks, by the programming in page 0, register 37 (Ch_Offset_2), where register 37 programs the delay between the first word and the second word. Also, the relative order of the two channels can be swapped, depending on the programmable register bit (page 0, register 38, bit 4) that enables swapping of the channels.

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Feature Description (continued)

The TLV320ADC3100 also supports a feature for inverting the bit clock polarity used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the audio interface mode chosen. The bit clock polarity can be configured by writing to page 0, register 29, bit 3.

The TLV320ADC3100 further includes programmability (page 0, register 27, bit 0) to place DOUT in the high-impedance state at the end of data transfer (that is, at the end of the bit cycle corresponding to the LSB of a channel). By combining this capability with the ability to program at what bit clock in a frame the audio data begins, TDM can be accomplished, resulting in multiple ADCs able to use a single audio serial data bus. To further enhance the tri-state capability, the TLV320ADC3100 can be put in a high-impedance state a half bit cycle earlier by setting page 0, register 38, bit 1 to 1. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a high-impedance output state.

Either or both of the two channels can be disabled in LJF, I^2S, and DSP modes by using page 0, register 38, bits 3:2. Figure 10 shows the interface timing when both channels are enabled and early tri-stating is enabled. Figure 11 shows the effect of setting page 0, register 38, bit 2, first channel disabled, and setting page 0, register 38, bit 2 to 1, which enables placing DOUT in the high-impedance state. If placing DOUT in the high-impedance state is disabled, then the DOUT signal is driven to logic level 0.

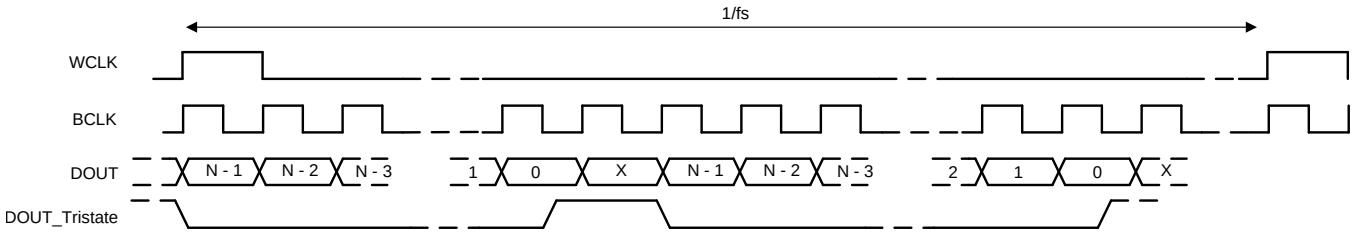


Figure 10. Both Channels Enabled, Early Tri-Stating Enabled

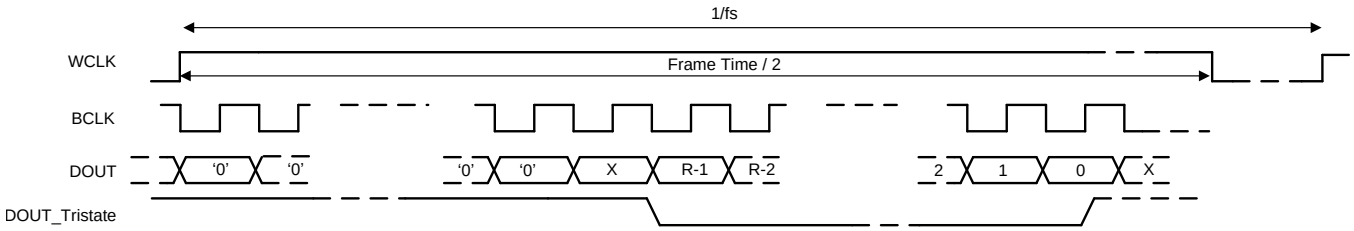


Figure 11. First Channel Disabled, Second Channel Enabled, Tri-Stating Enabled

The sync signal for the ADC filter is not generated based on the disabled channel. The sync signal for the filter corresponds to the beginning of the earlier of the two channels. If the first channel is disabled, the filter sync is generated at the beginning of the second channel, if enabled. If both channels are disabled, there is no output to the serial bus, and the filter sync corresponds to the beginning of the frame.

By default, when the word clocks and bit clocks are generated by the TLV320ADC3100, these clocks are active only when the ADC is powered up within the device. This internal clock gating is done to save power. However, the internal clock gating architecture also supports a feature wherein both the word clocks and bit clocks can be active even when the codec in the device is powered down. This feature is useful when using the TDM mode with multiple codecs on the same bus or when word clocks or bit clocks are used in the same system as general-purpose clocks.

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Feature Description (continued)

8.3.5.1 Right-Justified Mode

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock. Figure 12 shows the right-justified mode timing.

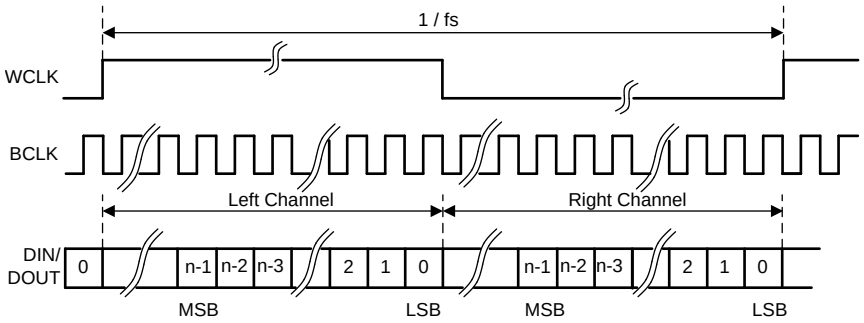


Figure 12. Right-Justified Mode Timing Diagram

For right-justified mode, the number of bit clocks per frame must be greater than twice the programmed word-length of the data.

NOTE

The time-slot-based mode is not available in the right-justified mode.

8.3.5.2 Left-Justified Mode

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly, the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock. Figure 13 shows the standard timing of the left-justified mode.

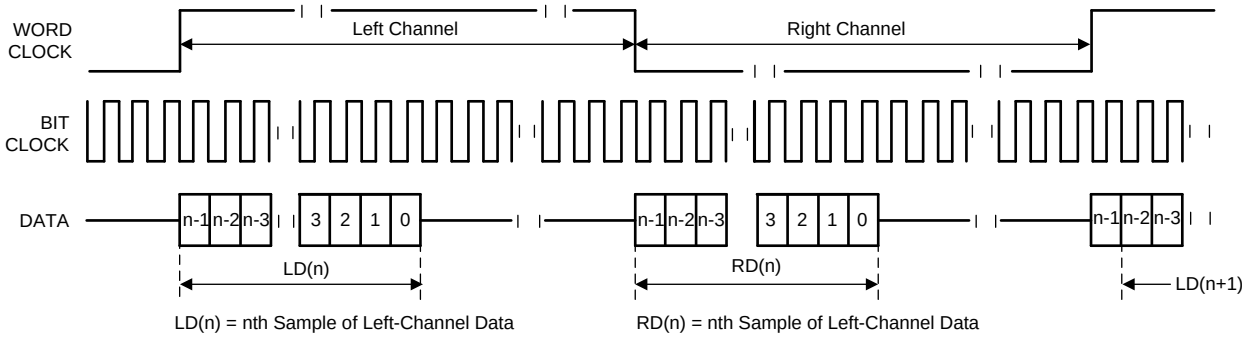


Figure 13. Left-Justified Mode (Standard Timing)

Feature Description (continued)

Figure 14 shows the left-justified mode with Ch_Offset_1 = 1.

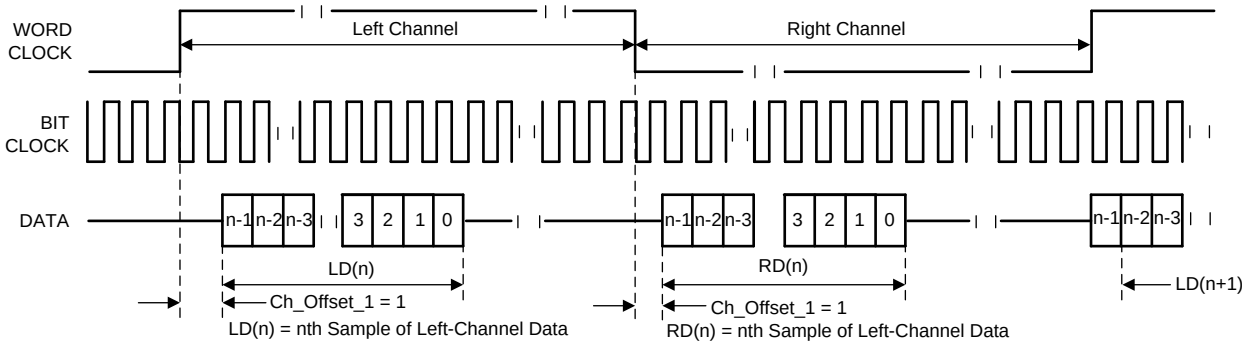


Figure 14. Left-Justified Mode With Ch_Offset_1 = 1

Figure 15 shows the left-justified mode with Ch_Offset_1 = 0 and bit clock inverted.

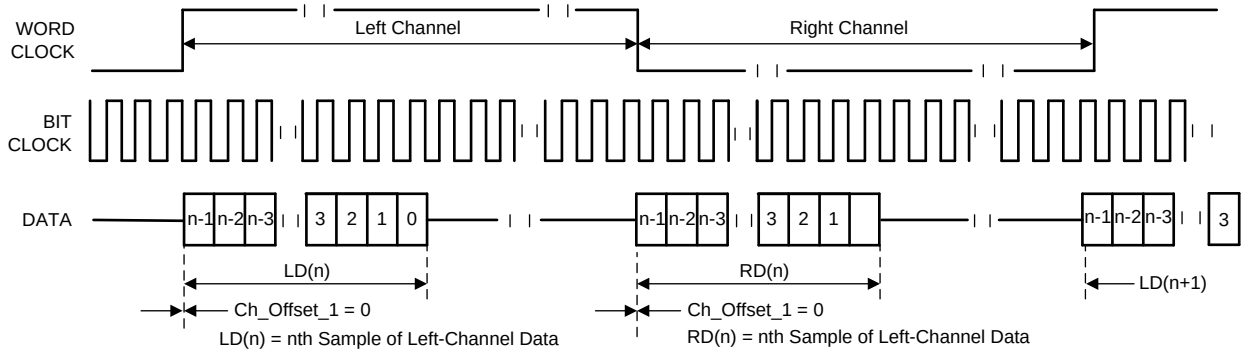


Figure 15. Left-Justified Mode With Ch_Offset_1 = 0, Bit Clock Inverted

For left-justified mode, the number of bit clocks per frame must be greater than twice the programmed word length of the data. Also, the programmed offset value must be less than the number of bit clocks per frame by at least the programmed word length of the data.

When the time-slot-based channel assignment is disabled (page 0, register 38, bit 0 = 0), the left and right channels have the same offset Ch_Offset_1 (page 0, register 28), and each edge of the word clock starts data transfer for one of the two channels, depending on whether or not channel swapping is enabled. Data bits are valid on the rising edges of the bit clock. With the time-slot-based channel assignment enabled (page 0, register 38, bit 0 = 1), the left and right channels have independent offsets (Ch_Offset_1 and Ch_Offset_2). The rising edge of the word clock starts data transfer for the first channel after a delay of its programmed offset (Ch_Offset_1) for this channel. Data transfer for the second channel starts after a delay of its programmed offset (Ch_Offset_2) from the LSB of the first-channel data. The falling edge of the word clock is not used.

With no channel swapping, the MSB of the left channel is valid on the (Ch_Offset_1 + 1)th rising edge of the bit clock following the rising edge of the word clock. Consequently, the MSB of the right channel is valid on the (Ch_Offset_1 + 1)th rising edge of the bit clock following the falling edge of the word clock. The timing diagram of Figure 14 illustrates the operation in this case, with an offset of 1. Because channel swapping is not enabled, the left-channel data are before the right-channel data. With channel swapping enabled, the MSB of the right channel is valid on the (Ch_Offset_1 + 1)th rising edge of the bit clock following the rising edge of the word clock. Thus, the MSB of the left channel is valid on the (Ch_Offset_1 + 1)th rising edge of the bit clock following the falling edge of the word clock. The timing diagram of Figure 16 depicts the operation in this case, with an offset of 1. As shown in the diagram, the right-channel data of a frame are before the left-channel data of that frame because of channel swapping. Otherwise, the behavior is similar to the case where channel swapping is disabled. The MSB of the right-channel data is valid on the second rising edge of the bit clock after the rising edge of the word clock, as a result of an offset of 1. Similarly, the MSB of the left-channel data is valid on the second rising edge of the bit clock after the falling edge of the word clock.

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Feature Description (continued)

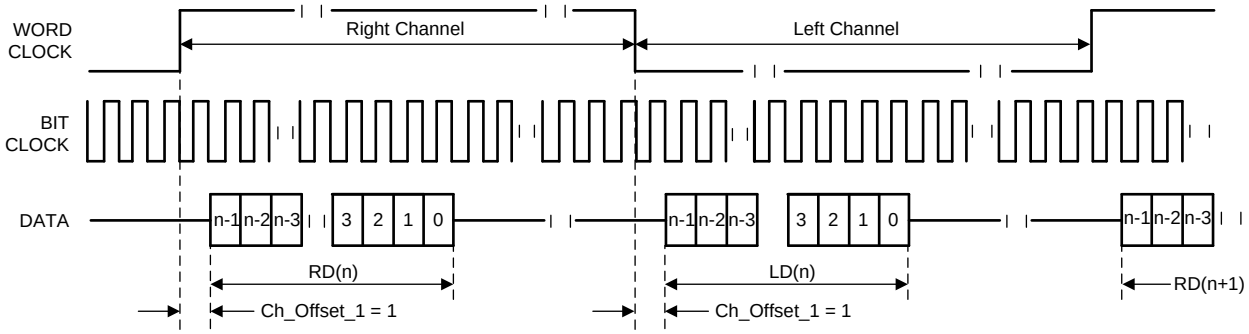


Figure 16. Left-Justified Mode With Ch_Offset_1 = 1, Channel Swapping Enabled

When the time-based-slot mode is enabled with no channel swapping, the MSB of the left channel is valid on the (Offset1 + 1)th rising edge of the bit clock following the rising edge of the word clock. Thus, the MSB of the right channel is valid on the (Ch_Offset_2 + 1)th rising edge of the bit clock following the LSB of the left channel.

Figure 17 shows the operation with time-based-slot mode enabled, Ch_Offset_1 = 0, and Ch_Offset_2 = 1. The MSB of the left channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Data transfer for the right channel does not wait for the falling edge of the word clock, and the MSB of the right channel is valid on the second rising edge of the bit clock after the LSB of the left channel.

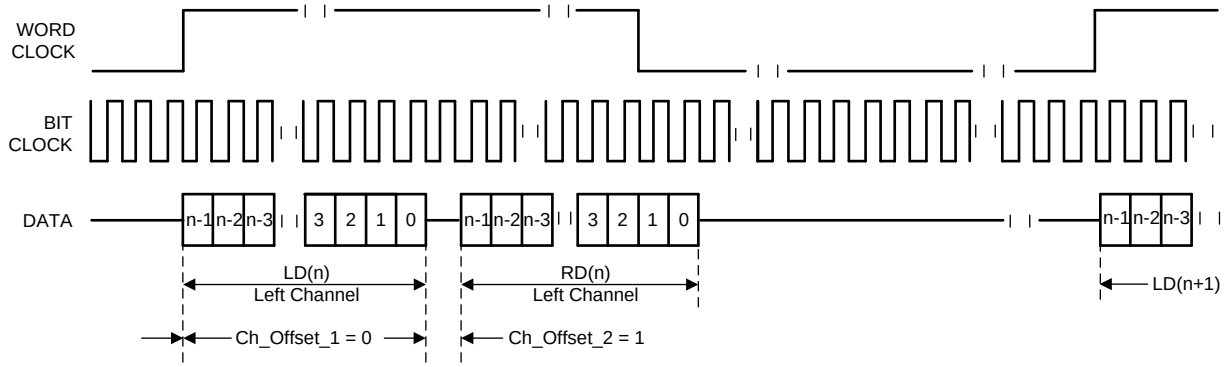


Figure 17. Left-Justified Mode, Time-Based-Slot Mode Enabled, Ch_Offset_1 = 0, Ch_Offset_2 = 1

When the time-based-slot mode is enabled and channel swapping is enabled, the MSB of the right channel is valid on the (Ch_Offset_1 + 1)th rising edge of the bit clock following the rising edge of the word clock. Thus, the MSB of the left channel is valid on the (Ch_Offset_2 + 1)th rising edge of the bit clock following the LSB of the right channel. Figure 18 illustrates the operation in this mode with Ch_Offset_1 = 0 and Ch_Offset_2 = 1. The MSB of the right channel is valid on the first rising edge of the bit clock after the rising edge of the word clock. Data transfer for the left channel starts following the completion of data transfer for the right channel without waiting for the falling edge of the word clock. The MSB of the left channel is valid on the second rising edge of the bit clock after the LSB of the right channel.

Feature Description (continued)

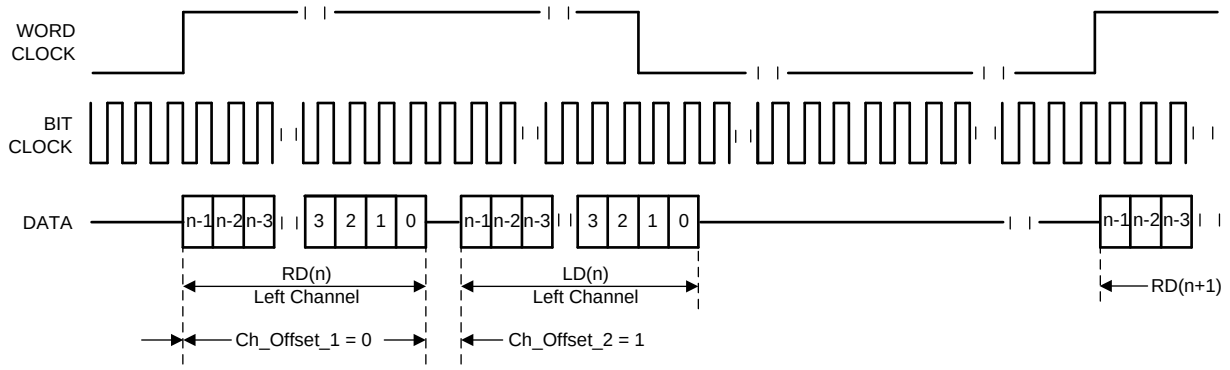


Figure 18. Left-Justified Mode, Time-Based-Slot Mode Enabled, Ch_Offset_1 = 0, Ch_Offset_2 = 1, Channel Swapping Enabled

8.3.5.3 I²S Mode

In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock. Figure 19 shows the standard I²S timing.

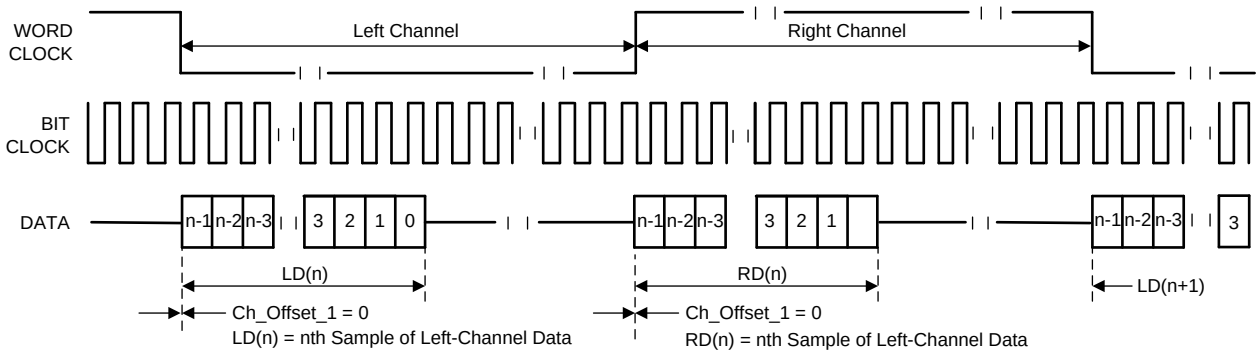


Figure 19. I²S Mode (Standard Timing)

Figure 20 shows the I²S mode timing with Ch_Offset_1 = 2.

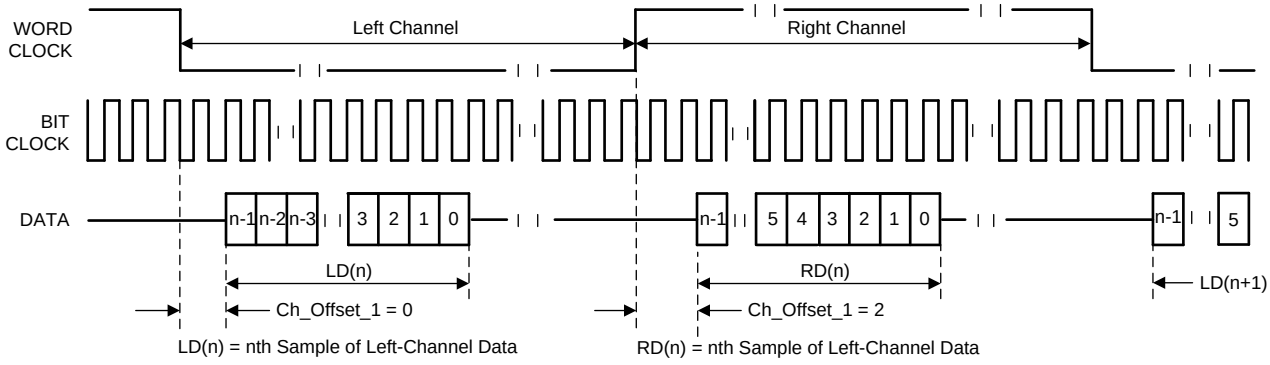


Figure 20. I²S Mode With Ch_Offset_1 = 2

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Feature Description (continued)

Figure 21 shows the I²S mode timing with Ch_Offset_1 = 0 and the bit clock inverted.

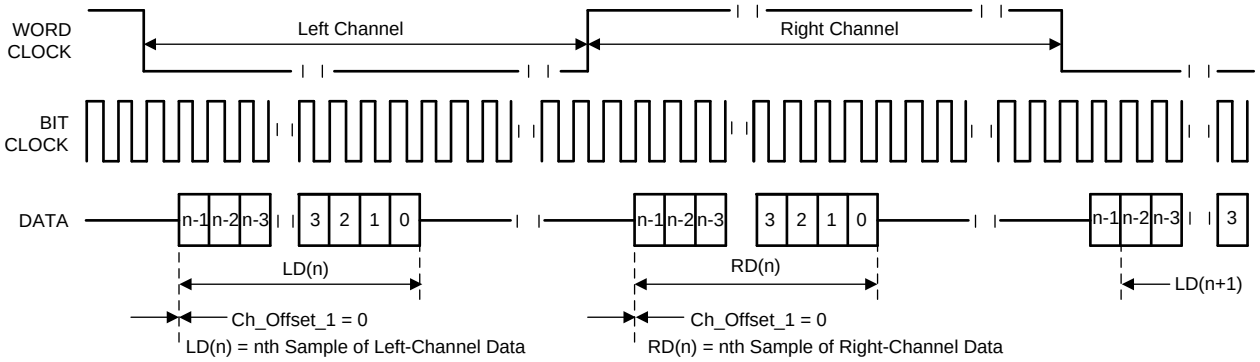


Figure 21. I²S Mode With Ch_Offset_1 = 0, Bit Clock Inverted

For the I²S mode, the number of bit clocks per channel must be greater than or equal to the programmed word length of the data. Also, the programmed offset value must be less than the number of bit clocks per frame by at least the programmed word length of the data.

8.3.5.4 DSP Mode

In DSP mode, the rising edge of the word clock starts the data transfer with the left-channel data first and is immediately followed by the right-channel data. Each data bit is valid on the falling edge of the bit clock. Figure 22 shows the standard timing for the DSP mode.

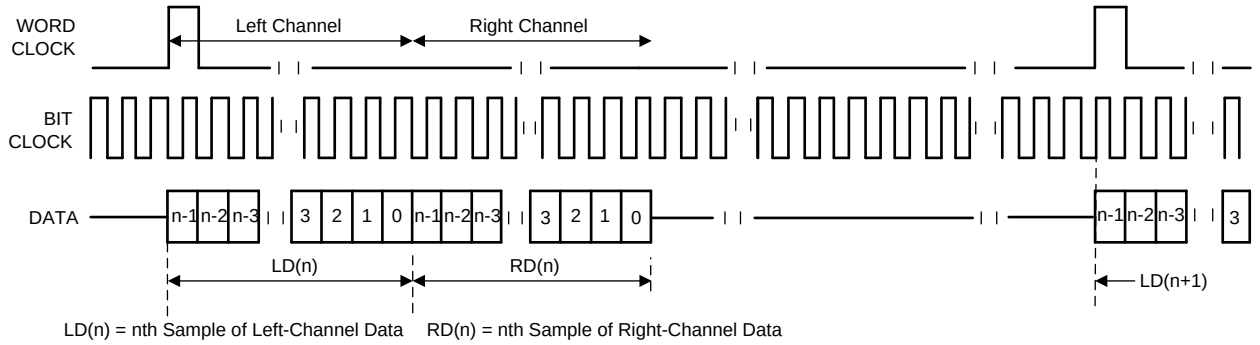


Figure 22. DSP Mode (Standard Timing)

Figure 23 shows the DSP mode timing with Ch_Offset_1 = 1.

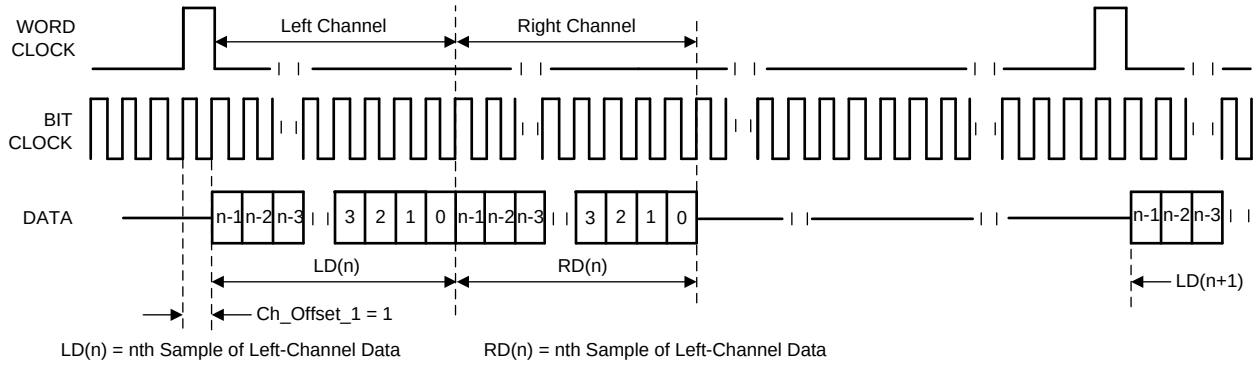


Figure 23. DSP Mode With Ch_Offset_1 = 1

Feature Description (continued)

Figure 24 shows the DSP mode timing with Ch_Offset_1 = 0 and the bit clock inverted.

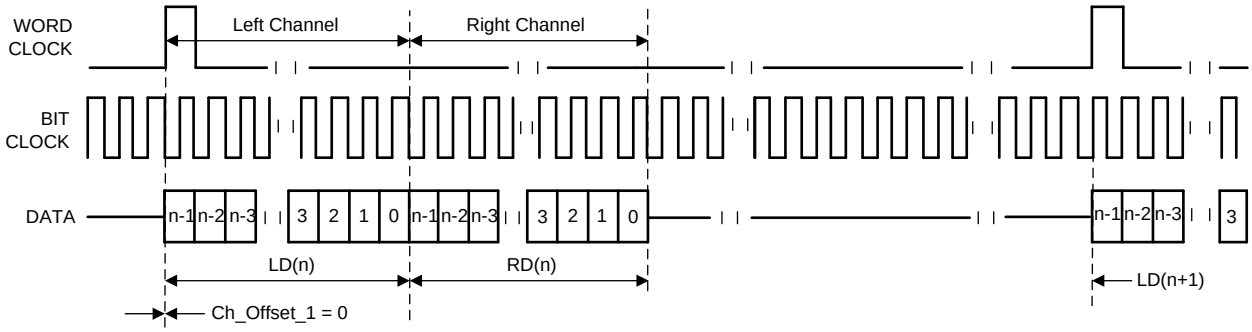


Figure 24. DSP Mode With Ch_Offset_1 = 0, Bit Clock Inverted

For DSP mode, the number of bit clocks per frame must be greater than twice the programmed word length of the data. Also, the programmed offset value must be less than the number of bit clocks per frame by at least the programmed word length of the data.

Figure 25 shows the DSP time-slot-based mode without channel swapping, and with Ch_Offset_1 = 0 and Ch_Offset_2 = 3. The MSB of the left channel data is valid on the first falling edge of the bit clock after the rising edge of the word clock. Because the right channel has an offset of 3, the MSB of its data is valid on the third falling edge of the bit clock after the LSB of the left-channel data. As in the case of other modes, the serial output bus is put in the high-impedance state, if tri-stating of the output is enabled, during all extra bit-clock cycles in the frame.

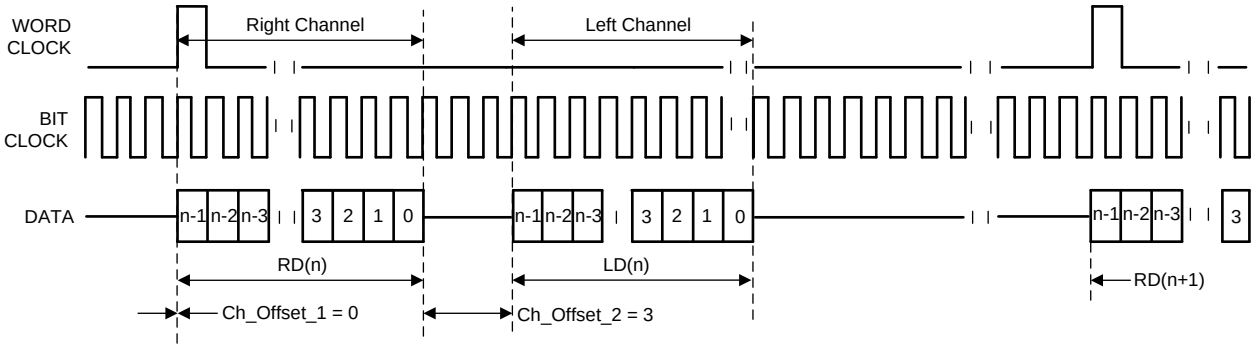


Figure 25. DSP Mode, Time-Slot-Based Mode Enabled, Ch_Offset_1 = 0, Ch_Offset_2 = 3

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Feature Description (continued)

Figure 26 shows the timing diagram for the DSP mode with left and right channels swapped, Ch_Offset_1 = 0, and Ch_Offset_2 = 3. The MSB of the right channel is valid on the first falling edge of the bit clock after the rising edge of the word clock. Similarly, the MSB of the left channel is valid three bit-clock cycles after the LSB of right channel because the offset for the left channel is 3.

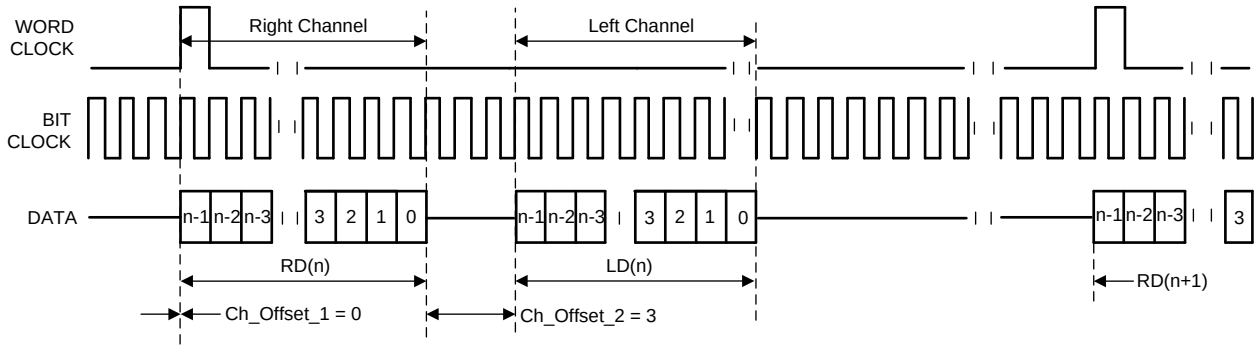


Figure 26. DSP Mode, Time-Slot-Based Mode Enabled, Ch_Offset_1 = 0, Ch_Offset_2 = 3, Channel Swap Enabled

8.3.6 Audio Clock Generation

The audio converters in the fully programmable filter mode of the TLV320ADC3100 require an internal audio master clock at a frequency of ≥ N × f_S, where N = IADC (page 0, register 21) when filter mode (page 0, register 61) equals zero; otherwise, N equals the instruction count from the ADC processing blocks (see Table 6). The master clock is obtained from an external clock signal applied to the device.

The device can accept an MCLK input from 512 kHz to 50 MHz, which can then be passed through either a programmable divider or a PLL to get the proper internal audio master clock required by the device. The BCLK input can also be used to generate the internal audio master clock.

A primary concern is proper operation of the TLV320ADC3100 at various sample rates with the limited MCLK frequencies available in the system. This device includes a programmable PLL to accommodate such situations. The integrated PLL can generate audio clocks from a wide variety of possible MCLK inputs, with particular focus paid to the standard MCLK rates already widely used.

When the PLL is enabled:

$$f_S = (PLLCLK_IN \times K \times R) / (NADC \times MADC \times AOSR \times P)$$

where

- P = 1, 2, 3,…, 8
- R = 1, 2, …, 16
- K = J.D
- J = 1, 2, 3, …, 63
- D = 0000, 0001, 0002, 0003, …, 9998, 9999
- PLLCLK_IN can be MCLK or BCLK, selected by page 0, register 4, bits 3:2 (1)

P, R, J, and D are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), whereas D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

Examples:

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

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Feature Description (continued)

When the PLL is enabled and D = 0000, the following conditions must be satisfied to meet specified performance:

512 kHz ≤ (PLLCLK_IN / P) ≤ 20 MHz
80 MHz ≤ (PLLCLK _IN × K × R / P) ≤ 110 MHz
4 ≤ J ≤ 55

When the PLL is enabled and D ≠ 0000, the following conditions must be satisfied to meet specified performance:

10 MHz ≤ PLLCLK _IN / P ≤ 20 MHz
80 MHz ≤ PLLCLK _IN × K × R / P ≤ 110 MHz
4 ≤ J ≤ 11
R = 1

Example:

For MCLK = 12 MHz, f_S = 44.1 kHz, NADC = 8, MADC = 2, and AOSR = 128:
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example:

For MCLK = 12 MHz, f_S = 48 kHz , NADC = 8, MADC = 2, and AOSR = 128:
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

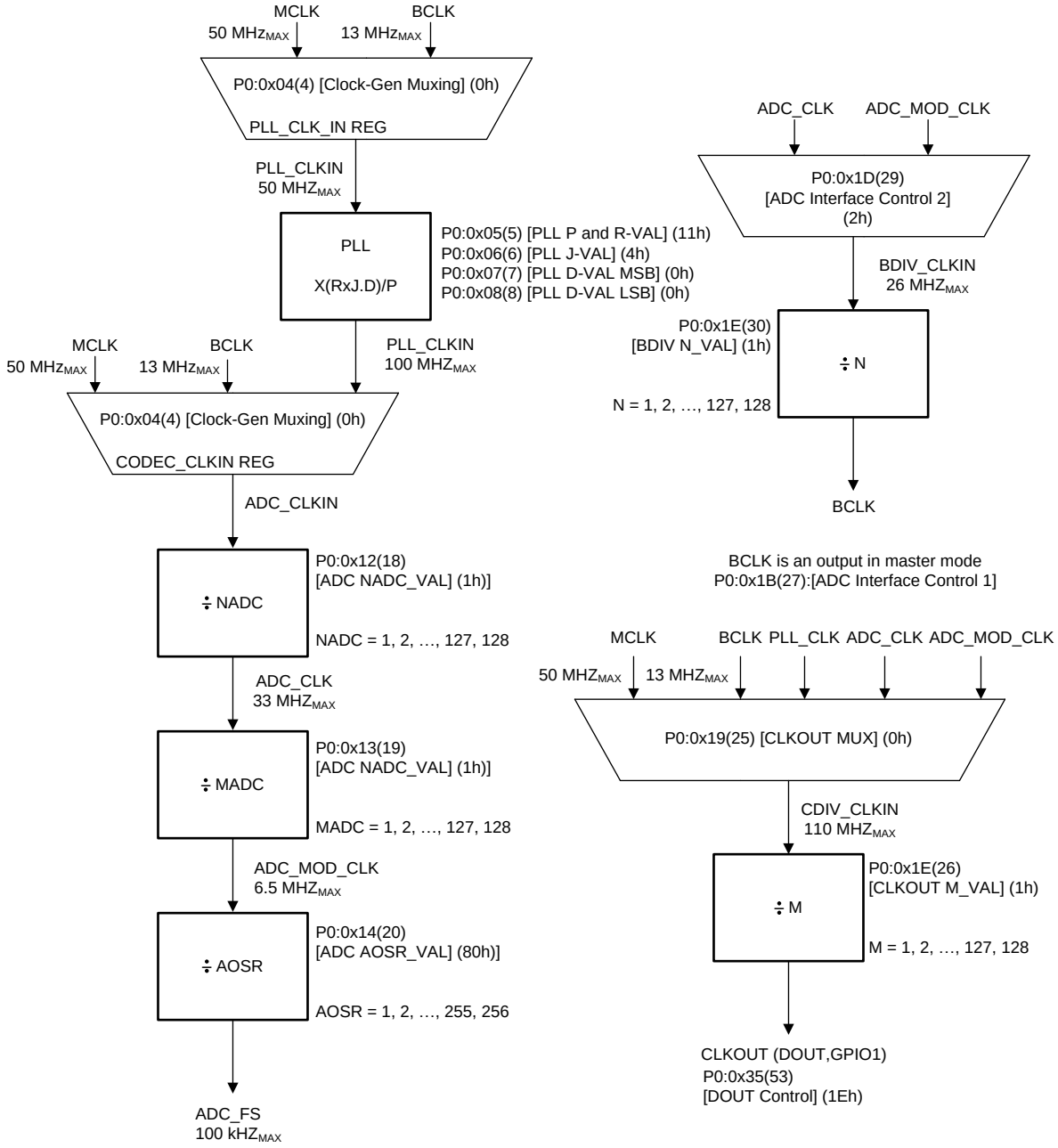
Table 1 lists several example cases of typical MCLK rates and how to program the PLL to achieve sample rates of f_S = 44.1 kHz or 48 kHz with NADC = 8, MADC = 2, and AOSR = 128.

Table 1. Typical MCLK Rates

MCLK (MHz)	P	R	J	D	ACHIEVED f_S	% ERROR
f_S = 44.1 kHz						
2.8224	1	1	32	0	44,100.00	0.0000
5.6448	1	1	16	0	44,100.00	0.0000
12.0	1	1	7	5264	44,100.00	0.0000
13.0	1	1	6	9474	44,099.71	–0.0007
16.0	1	1	5	6448	44,100.00	0.0000
19.2	1	1	4	7040	44,100.00	0.0000
19.68	1	1	4	5893	44,100.30	0.0007
48.0	4	1	7	5264	44,100.00	0.0000
f_S = 48 kHz						
2.048	1	1	48	0	48,000.00	0.0000
3.072	1	1	32	0	48,000.00	0.0000
4.096	1	1	24	0	48,000.00	0.0000
6.144	1	1	16	0	48,000.00	0.0000
8.192	1	1	12	0	48,000.00	0.0000
12.0	1	1	8	1920	48,000.00	0.0000
13.0	1	1	7	5618	47,999.71	–0.0006
16.0	1	1	6	1440	48,000.00	0.0000
19.2	1	1	5	1200	48,000.00	0.0000
19.68	1	1	4	9951	47,999.79	–0.0004
48.0	4	1	8	1920	48,000.00	0.0000

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Figure 27 shows a detailed diagram of the audio clock section of the TLV320ADC3100.



NOTE: MADC × AOSR ≥ IADC, where IADC is the number of instructions (instruction count) for the ADC MAC engine. IADC is programmable from 2, 4,…, 510. The convention used in this figure is page number: register number (reset value).

Figure 27. Audio Clock Generation Processing

8.3.7 Stereo Audio ADC

The TLV320ADC3100 includes a stereo audio ADC that uses a delta-sigma modulator with 128-times oversampling in single-rate mode, followed by a digital decimation filter. The ADC supports sampling rates from 8 kHz to 48 kHz in single-rate mode, and up to 96 kHz in dual-rate mode. Whenever the ADC is in operation, the device requires that an audio master clock be provided and appropriate audio clock generation be set up within the device.

In order to provide optimal system power dissipation, the stereo ADC can be powered one channel at a time, to support when only mono record capability is required. In addition, both channels can be fully or partially powered down.

The integrated digital decimation filter removes high-frequency content and down-samples the audio data from an initial sampling rate of 128 f_S to the final output sampling rate of f_S. The decimation filter provides a linear phase output response with a group delay of 17 / f_S. The –3-dB bandwidth of the decimation filter extends to 0.45 f_S and scales with the sample rate (f_S). The filter has a minimum 73-dB attenuation over the stop band from 0.55 f_S to 64 f_S. Independent digital high-pass filters are also included with each ADC channel, with a corner frequency that can be set independently by programmable coefficients or can be disabled entirely.

Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog antialiasing filtering are relaxed. The TLV320ADC3100 integrates a second-order analog antialiasing filter with 20-dB attenuation at 1 MHz. This filter, combined with the digital decimation filter, provides sufficient antialiasing filtering without requiring additional external components.

The ADC is preceded by a programmable gain amplifier (PGA) that allows analog gain control from 0 dB to 40 dB in steps of 0.5 dB. The PGA gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register programming (see register page 0, register 81). This soft-stepping specifies that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and upon power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag is set whenever the gain applied by the PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming a register bit.

8.3.8 Audio Analog Inputs

8.3.8.1 Digital Volume Control

The TLV320ADC3100 also has a digital volume-control block with a range from –12 dB to 20 dB (as shown in Table 2) in steps of 0.5 dB. This block is set by programming page 0, registers 83 and 84 for the left and right channels, respectively.

Table 2. Digital Volume Control for the ADC

DESIRED GAIN (dB)	LEFT, RIGHT CHANNEL PAGE 0, REGISTERS 83 AND 84, BITS 6:0
–12	110 1000
–11.5	110 1001
–11	110 1010
...	...
–0.5	111 1111
0	000 0000 (default)
0.5	000 0001
...	...
19.5	010 0111
20	010 1000

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During volume control changes, the soft-stepping feature is used to avoid audible artifacts. The soft-stepping rate can be set to either 1 or 2 gain steps per sample. Soft-stepping can also be entirely disabled. This soft-stepping is configured via page 0, register 81, bits 1:0, and is common to soft-stepping control for the analog PGA. During power-down of an ADC channel, this volume control soft-steps down to –12 dB before powering down. Resulting from the soft-stepping control, soon after changing the volume control setting or powering down the ADC channel, the actual applied gain may be different from the one programmed through the control register. The TLV320ADC3100 provides feedback through the read-only flags in page 0, register 36, bit 7 for the left channel and page 0, register 36, bit 3 for the right channel.

8.3.8.2 Fine Digital Gain Adjustment

Additionally, the gain in each channel is finely adjustable in steps of 0.1 dB. This feature is useful when trying to match the gain between channels. By programming page 0, register 82, the gain can be adjusted from 0 dB to –0.4 dB in steps of 0.1 dB. This feature, in combination with the regular digital volume control, allows the gains through the left and right channels be matched in the range of –0.5 dB to 0.5 dB with a resolution of 0.1 dB.

8.3.8.3 AGC

The TLV320ADC3100 includes automatic gain control (AGC) for ADC recording. AGC can be used to maintain a nominally constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer to or farther from the microphone. The AGC algorithm has several programmable parameters (including target gain, attack and decay time constants, noise threshold, and maximum PGA applicable) that allow the algorithm to be fine-tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Because the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate.

- **Target level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320ADC3100 allows programming of eight different target levels that can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Because the TLV320ADC3100 reacts to the signal absolute average and not to peak levels, TI recommends that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.
- **Attack time** determines how quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level resulting from an increase in input signal level. A wide range of attack-time programmability is supported in terms of number of samples (that is, the number of ADC sample-frequency clock cycles).
- **Decay time** determines how quickly the PGA gain is increased when the output signal level falls below the target level resulting from a reduction in input signal level. A wide range of decay-time programmability is supported in terms of number of samples (that is, the number of ADC sample-frequency clock cycles).
- **Noise threshold**. If the input signal level falls below the noise threshold, the AGC considers the duration that the signal level remains below the threshold as silence, and thus brings down the gain to 0 dB in steps of 0.5 dB every sample period and sets the noise-threshold flag. The gain stays at 0 dB unless the input signal average rises above the noise threshold setting, thus preventing noise from being amplified in the absence of a signal. The noise threshold level in the AGC algorithm is programmable from –30 dB to –90 dB of full-scale. When the AGC noise threshold is set to –70 dB, –80 db, or –90 dB, the maximum applicable microphone input PGA setting must be greater than or equal to 11.5 dB, 21.5 dB, or 31.5 dB, respectively. This operation includes hysteresis and debounce to prevent the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. The noise (or silence) detection feature can also be entirely disabled.
- **Maximum applicable PGA** allows the maximum gain applied by the AGC to be restricted. This restriction can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input maximum PGA can be programmed from 0 dB to 40 dB in steps of 0.5 dB.
- **Hysteresis**, as the name suggests, determines a window around the noise threshold that must be exceeded to detect if the recorded signal is indeed either noise or signal. If the energy of the recorded signal is initially greater than the noise threshold, then the AGC recognizes the signal as noise only when the energy of the recorded signal falls below the noise threshold by a value given by hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize the sound as a signal, its energy must exceed the noise threshold by a value given by the hysteresis setting. In order to prevent the AGC from jumping between noise and signal states (which can happen when the energy of the recorded signal is very close to the noise

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threshold), a non-zero hysteresis value must be chosen. The hysteresis feature can also be disabled.

- **Debounce time (noise and signal)** determines the hysteresis in time domain for noise detection. The AGC continuously calculates the energy of the recorded signal. If the calculated energy is less than the set noise threshold, then the AGC does not increase the input gain to achieve the target level. However, to handle audible artifacts that can occur when the energy of the input signal is very close to the noise threshold, the AGC checks if the energy of the recorded signal is less than the noise threshold for a duration greater than the noise debounce time. Similarly, the AGC starts increasing the input-signal gain to reach the target level when the calculated energy of the input signal is greater than the noise threshold. Again, to avoid audible artifacts when the input-signal energy is very close to noise threshold, the energy of the input signal must continuously exceed the noise threshold value for the signal debounce time. If the debounce times are kept very small, then audible artifacts can result by rapidly enabling and disabling the AGC function. At the same time, if the debounce time is kept too large, then the AGC can take more time to respond to changes in input signal levels with respect to the noise threshold. Both noise and signal debounce time can be disabled.
- The **AGC noise threshold flag** is a read-only flag indicating that the input signal has levels lower than the noise threshold, and thus is detected as noise (or silence). In such a condition, the AGC applies a gain of 0 dB.
- **Gain applied by the AGC** is a read-only register setting that gives a real-time feedback to the system on the gain applied by the AGC to the recorded signal. This setting, along with the target setting, can be used to determine the input signal level. In a steady state situation:

  Target level (dB) = gain applied by AGC (dB) + input signal level (dB)

  When the AGC noise threshold flag is set, then the status of the gain applied by the AGC is not valid.
- **The AGC saturation flag** is a read-only flag indicating that the ADC output signal has not reached its target level. However, the AGC is unable to increase the gain further because the required gain is higher than the maximum allowed PGA gain. Such a situation can happen when the input signal has very low energy and the noise threshold is also set very low. When the AGC noise threshold flag is set, the status of the AGC saturation flag must be ignored.
- **The ADC saturation flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This distortion typically happens when the AGC target level is kept very high and the energy in the input signal increases faster than the attack time.
- **An AGC low-pass filter** is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low-pass filter is in the form of a first-order IIR filter. Two 8-bit registers are used to form the 16-bit digital coefficient, as shown in the *Register Maps* section. In this way, a total of six registers are programmed to form the three IIR coefficients. Equation 2 shows how the transfer function of the filter is implemented for signal-level detection:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (2)$$

where

  - Coefficient N0 can be programmed by writing into page 4, registers 2 and 3
  - Coefficient N1 can be programmed by writing into page 4, registers 4 and 5
  - Coefficient D1 can be programmed by writing into page 4, registers 6 and 7
  - N0, N1, and D1 are 16-bit, 2s-complement numbers, and their default values implement a low-pass filter with cutoff at $0.002735 \times \text{ADC_f}_S$

Table 3 lists various AGC programming options. The AGC can be used only if the analog microphone input is routed to the ADC channel.

Figure 28 illustrates the input and output signals along with the decay and attack times of the AGC.

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Table 3. AGC Parameter Settings

FUNCTION	CONTROL REGISTER LEFT ADC	CONTROL REGISTER RIGHT ADC	BIT
AGC enable	Page 0, register 86	Page 0, register 94	7
Target level	Page 0, register 86	Page 0, register 94	6:4
Hysteresis	Page 0, register 87	Page 0, register 95	7:6
Noise threshold	Page 0, register 87	Page 0, register 95	5:1
Maximum applicable PGA	Page 0, register 88	Page 0, register 96	6:0
Time constants (attack time)	Page 0, register 89	Page 0, register 97	7:0
Time constants (decay time)	Page 0, register 90	Page 0, register 98	7:0
Debounce time (noise)	Page 0, register 91	Page 0, register 99	4:0
Debounce time (signal)	Page 0, register 92	Page 0, register 100	3:0
Gain applied by the AGC	Page 0, register 93	Page 0, register 101	7:0 (read-only)
AGC noise-threshold flag	Page 0, register 45 (sticky flag), Page 0, register 47 (non-sticky flag)	Page 0, register 45 (sticky flag), Page 0, register 47 (non-sticky flag)	6:5 (read-only)
AGC saturation flag	Page 0, register 36 (sticky flag)	Page 0, register 36 (sticky flag)	5, 1 (read-only)
ADC saturation flag	Page 0, register 42 (sticky flag), Page 0, register 43 (non-sticky flag)	Page 0, register 42 (sticky flag), Page 0, register 43 (non-sticky flag)	3:2 (read-only)

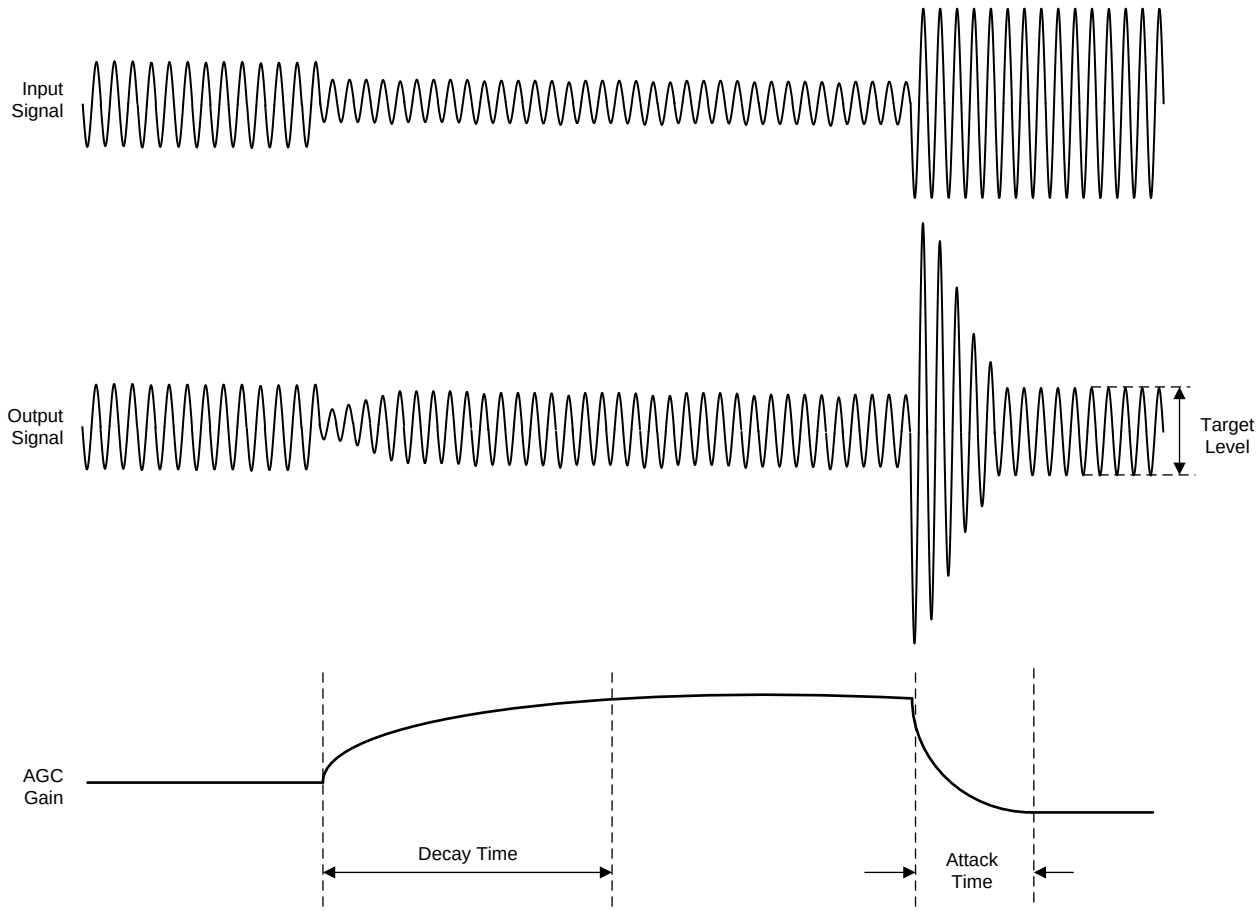


Figure 28. AGC Characteristics

The TLV320ADC3100 includes two analog audio input pins, which can be configured as one fully-differential pair and one single-ended input, or as three single-ended audio inputs. These pins connect through series resistors and switches to the virtual ground terminals of two fully differential operational amplifiers (one per ADC and PGA channel). By selecting to turn on only one set of switches per operational amplifier at a time, the inputs can be effectively multiplexed to each ADC PGA channel.

By selecting to turn on multiple sets of switches per operational amplifier at a time, mixing can also be achieved. Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal operational amplifiers, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, take adequate precautions to avoid such a saturation case from occurring. In general, the mixed signal must not exceed 2 V_{PP} (single-ended) or 4 V_{PP} (differential).

In most mixing applications, there is also a general requirement to adjust the levels of the individual signals being mixed. For example, if a soft signal and a large signal are to be mixed and played together, the soft signal generally must be amplified to a level comparable to the large signal before mixing. In order to accommodate this requirement, the TLV320ADC3100 includes an input level control on each of the individual inputs before they are mixed or multiplexed into the ADC PGAs, with programmable attenuation at 0 dB, –6 dB, or off.

NOTE

This input-level control is not intended to be a volume control, but instead used for coarse level setting. Finer soft-stepping of the input level is implemented in this device by the ADC PGA.

Figure 29 shows various available configurations for the audio input.

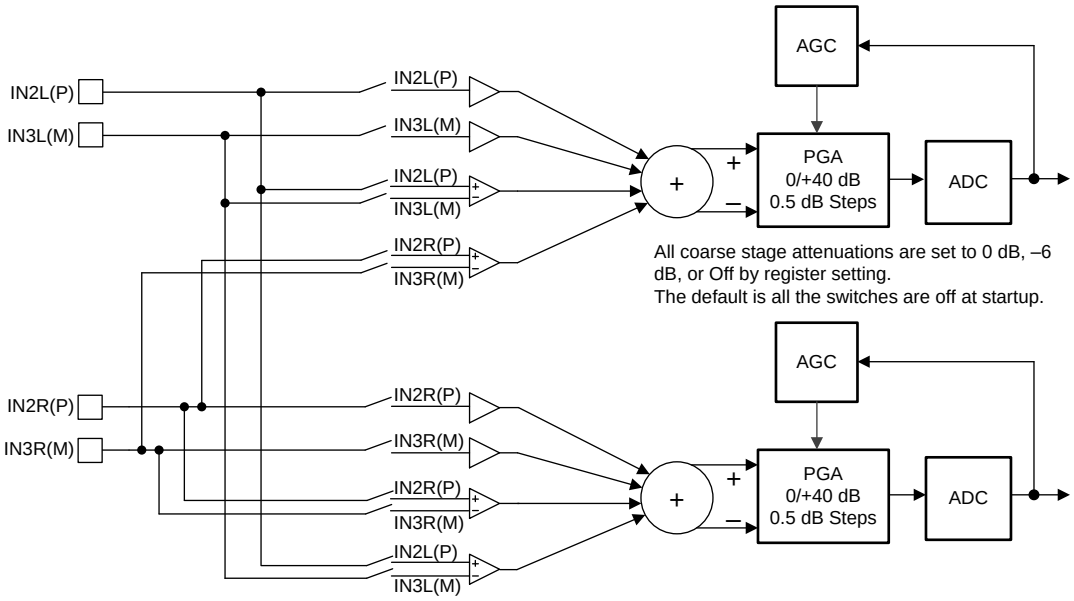


Figure 29. TLV320ADC3100 Available Audio Input Path Configurations

Table 4 lists the available routing configurations for the audio signals on the TLV320ADC3100.

Table 4. TLV320ADC3100 Audio Signals

AUDIO SIGNALS AVAILABLE TO THE LEFT ADC		AUDIO SIGNALS AVAILABLE TO THE RIGHT ADC	
SINGLE-ENDED INPUTS	DIFFERENTIAL INPUTS	SINGLE-ENDED INPUTS	DIFFERENTIAL INPUTS
IN2L(P)	IN2L(P), IN3L(M)	IN2R(P)	IN2R(P), IN3R(M)
IN3L(M)	IN2R(P), IN3R(M)	IN3R(M)	IN2L(P), IN3L(M)

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Inputs can be selected as single-ended instead of fully differential, and mixing or multiplexing into the ADC PGAs is also possible in this mode. However, an input pair cannot be selected as fully differential for connection to one ADC PGA and simultaneously selected as single-ended for connection to the other ADC PGA channel. However, an input can be selected or mixed into both the left and right channel PGAs, as long as the PGA has the same configuration for both channels (either both single-ended or both fully differential).

8.3.9 Input Impedance and VCM Control

The TLV320ADC3100 includes several programmable settings to control the analog input pins, particularly when the pins are not selected for connection to an ADC PGA. The default option allows unselected inputs to be put into a high-impedance state. However, the pins on the device do include protection diode circuits connected to AVDD and AVSS. Thus, if any voltage is driven onto a pin approximately one diode drop (~0.6 V) above AVDD or one diode drop below AVSS, these protection diodes begin conducting current, resulting in an effective impedance that no longer appears as a high-impedance state.

Another programmable option for unselected analog inputs is to weakly hold those inputs at the common-mode input voltage of the ADC PGA (determined by an internal band-gap voltage reference). This feature is useful to keep the AC-coupling capacitors connected to the analog inputs biased up at a normal DC level, thus avoiding the need for them to charge up suddenly when the input is changed from being unselected to selected for connection to an ADC PGA. This option is controlled in page 1, register 52 through page 1, register 57. This option must be disabled when an input is selected for connection to an ADC PGA or selected for the analog input bypass path, because the input can corrupt the recorded input signal if left operational when an input is selected.

In most cases, the analog input pins on the TLV320ADC3100 must be AC-coupled to analog input sources, the only exception generally being if an ADC is used for DC voltage measurement. The AC-coupling capacitor causes a high-pass filter pole to be inserted into the analog signal path, so the size of the capacitor must be chosen to move that filter pole sufficiently low in frequency to cause minimal effect on the processed analog signal. The input impedance of the analog inputs, when selected for connection to an ADC PGA, varies with the setting of the input-level control, starting at approximately 35 kΩ with an input-level control setting of 0 dB, and 62.5-kΩ when the input-level control is set at –6 dB. For example, using a 0.1-µF, AC-coupling capacitor at an analog input results in a high-pass filter pole of 45.5 Hz when the 0-dB, input-level control setting is selected. Table 5 lists various mixer gains and microphone PGA ranges to set a high-pass corner for the application.

Table 5. Single-Ended Input Impedance vs PGA Ranges(1)

MIXER GAIN (dB)	MICROPHONE PGA RANGE (dB)	INPUT IMPEDANCE (Ω)
0	0–5.5	35,000
0	6–11.5	38,889
0	12–17.5	42,000
0	18–23.5	44,074
0	24–29.5	45,294
0	30–35.5	45,960
0	36–40	46,308
–6	0–5.5	62,222
–6	6–11.5	70,000
–6	12–17.5	77,778
–6	18–23.5	84,000
–6	24–29.5	88,148
–6	30–35.5	90,588
–6	36–40	91,919

(1) Valid when only one input is enabled.

8.3.10 MICBIAS Generation

The TLV320ADC3100 includes a programmable microphone bias output (MICBIAS1) capable of providing output voltages of 2 V or 2.5 V (both derived from the on-chip, band-gap voltage) with 4-mA, output-current drive capability. In addition, the MICBIAS output can be programmed to switch to AVDD directly through an on-chip switch, or powered down completely when not needed, for power savings. This function is controlled by register programming in page 1, register 51.

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8.3.11 ADC Decimation Filtering and Signal Processing

The TLV320ADC3100 ADC channel includes a built-in digital decimation filter to process the oversampled data from the delta-sigma modulator to generate digital data at the Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay, and sampling rate.

8.3.11.1 Processing Blocks

The TLV320ADC3100 offers a range of processing blocks that implement various signal processing capabilities along with decimation filtering. These processing blocks provide a choice of how much and what type of signal processing is used and which decimation filter is applied.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high antialias filtering or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR, biquad, and FIR filters have fully user-programmable coefficients. The ADC processing blocks can be selected by writing to page 0, register 61. The default (reset) processing block is PRB_R1. Table 6 lists the available processing blocks for the ADC.

Table 6. ADC Processing Blocks

PROCESSING BLOCKS	CHANNEL	DECIMATION FILTER	FIRST-ORDER IIR AVAILABLE	NUMBER OF BIQUADS	FIR	REQUIRED AOSR VALUE	INSTR CTR
PRB_R1	Stereo	A	Yes	0	No	128, 64	188
PRB_R2	Stereo	A	Yes	5	No	128, 64	240
PRB_R3	Stereo	A	Yes	0	25-tap	128, 64	236
PRB_R4	Right	A	Yes	0	No	128, 64	96
PRB_R5	Right	A	Yes	5	No	128, 64	120
PRB_R6	Right	A	Yes	0	25-tap	128, 64	120
PRB_R7	Stereo	B	Yes	0	No	64	88
PRB_R8	Stereo	B	Yes	3	No	64	120
PRB_R9	Stereo	B	Yes	0	20-tap	64	128
PRB_R10	Right	B	Yes	0	No	64	46
PRB_R11	Right	B	Yes	3	No	64	60
PRB_R12	Right	B	Yes	0	20-tap	64	64
PRB_R13	Right	C	Yes	0	No	32	70
PRB_R14	Stereo	C	Yes	5	No	32	124
PRB_R15	Stereo	C	Yes	0	25-tap	32	120
PRB_R16	Right	C	Yes	0	No	32	36
PRB_R17	Right	C	Yes	5	No	32	64
PRB_R18	Right	C	Yes	0	25-tap	32	62

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8.3.11.2 Processing Blocks: Details

Figure 30 shows the signal chain for a first-order IIR with AGC gain compensation, using filter A.

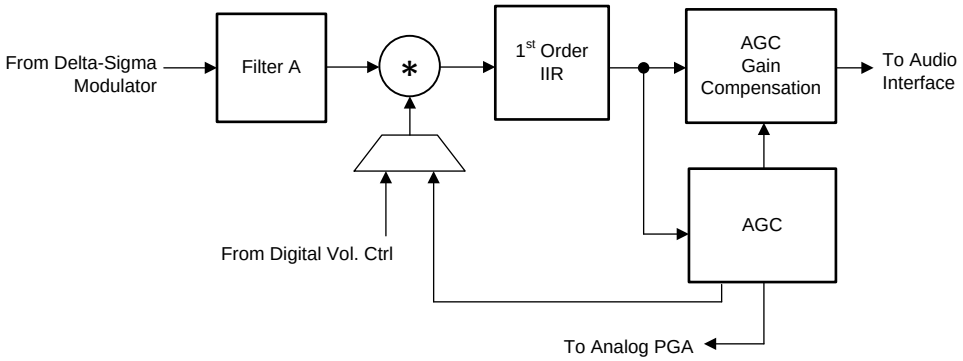


Figure 30. Signal Chain for PRB_R1 and PRB_R4

Figure 31 shows the signal chain for a five-biquad, first-order IIR with AGC gain compensation, using filter A.

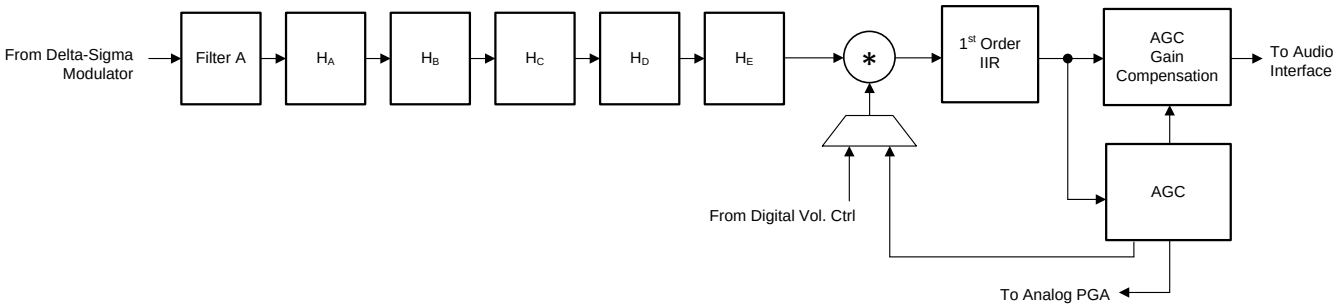


Figure 31. Signal Chain for PRB_R2 and PRB_R5

Figure 32 shows the signal chain for a 25-tap FIR, first-order IIR with AGC gain compensation, using filter A.

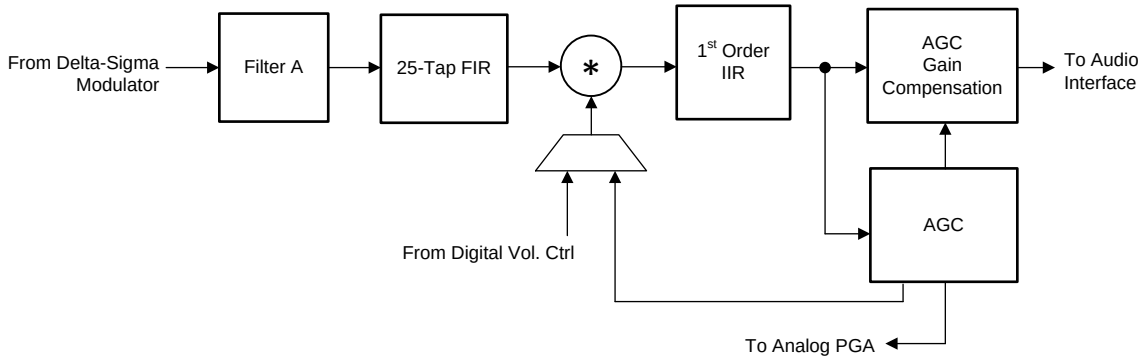


Figure 32. Signal Chain for PRB_R3 and PRB_R6

Figure 33 shows the signal chain for a first-order IIR with AGC gain compensation, using filter B.

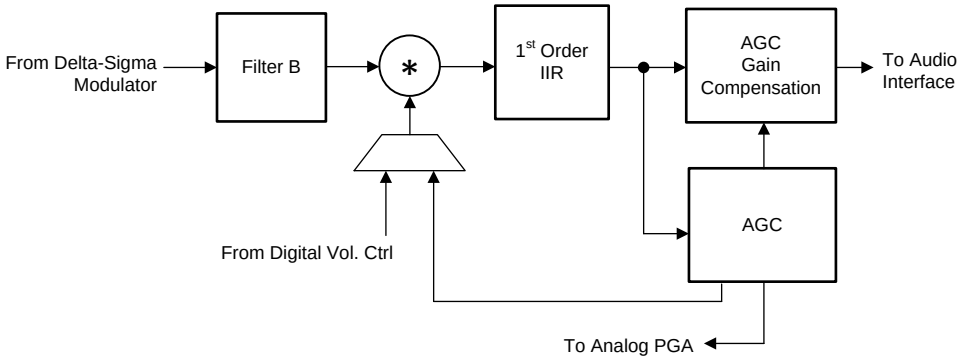


Figure 33. Signal Chain for PRB_R7 and PRB_R10

Figure 34 shows the signal chain for a three-biquad, first-order IIR with AGC gain compensation, using filter B.

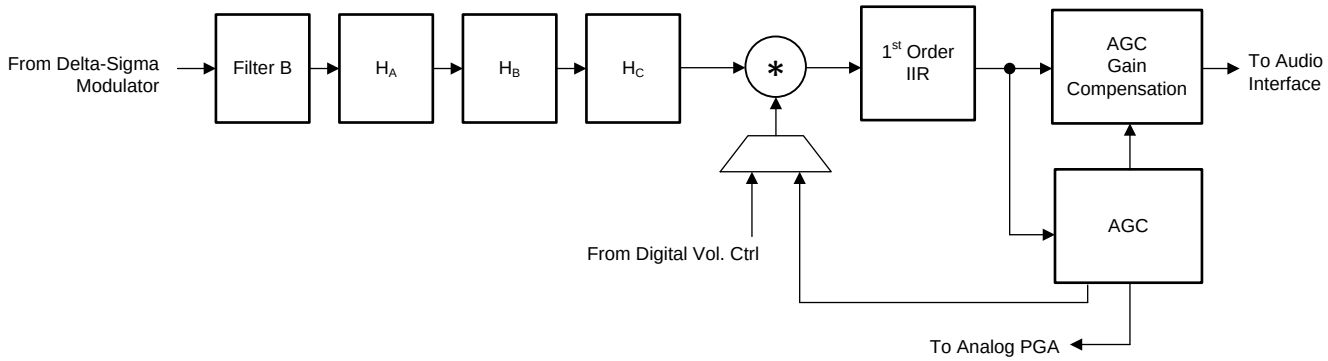


Figure 34. Signal Chain for PRB_R8 and PRB_R11

Figure 35 shows the signal chain for a 20-tap FIR, first-order IIR with AGC gain compensation, using filter B.

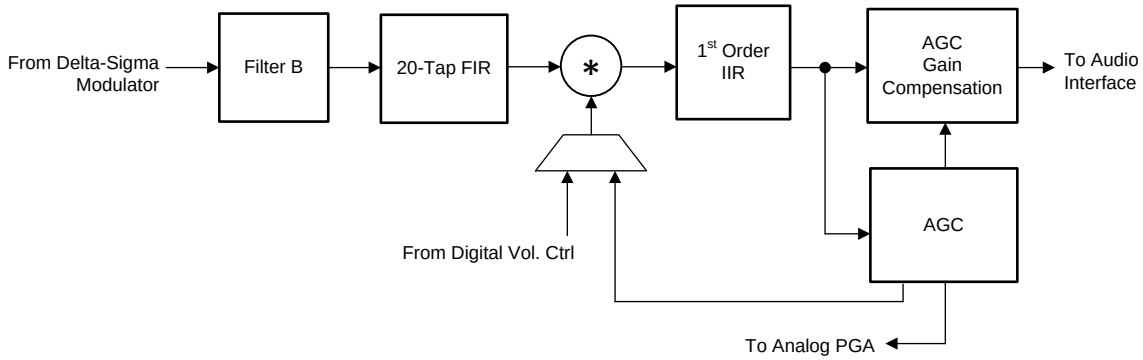


Figure 35. Signal Chain for PRB_R9 and PRB_R12

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Figure 36 shows the signal chain for a first-order IIR with AGC gain compensation, using filter C.

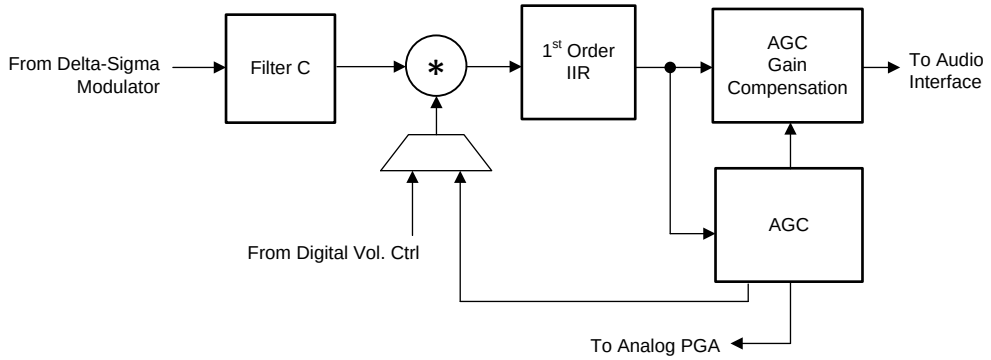


Figure 36. Signal Chain for PRB_R13 and PRB_R16

Figure 37 shows the signal chain for a five-biquad, first-order IIR with AGC gain compensation, using filter C.

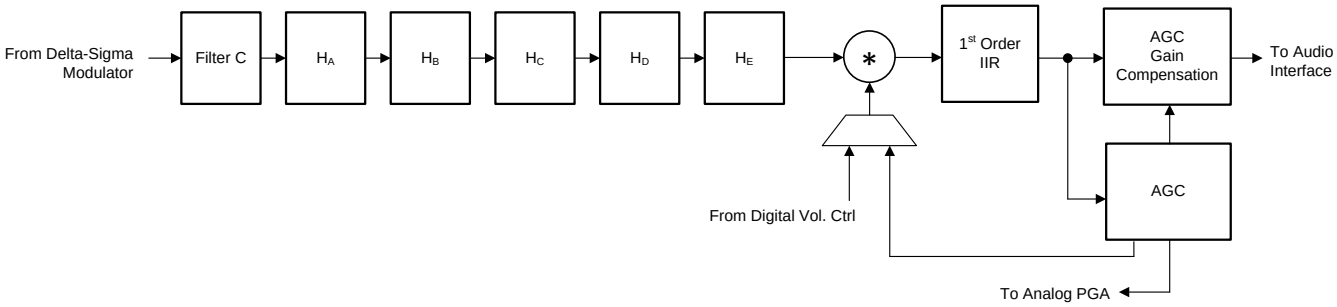


Figure 37. Signal Chain for PRB_R14 and PRB_R17

Figure 38 shows the signal chain for a 25-tap FIR, first-order IIR with AGC gain compensation, using filter C.

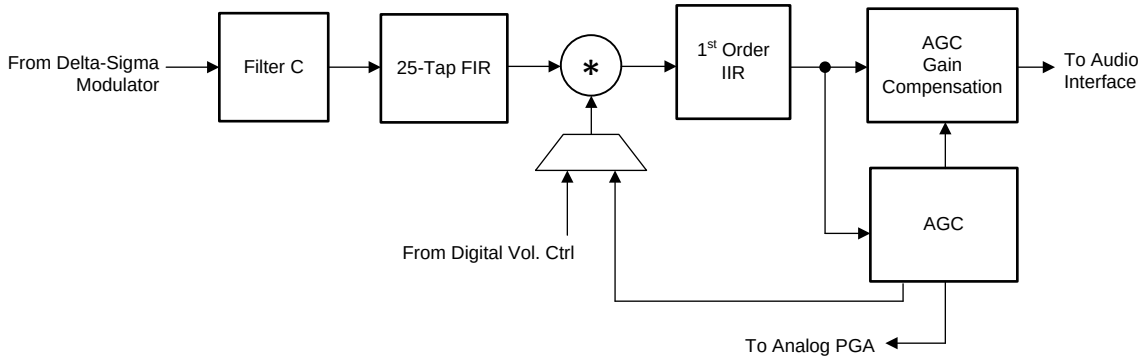


Figure 38. Signal for PRB_R15 and PRB_R18

8.3.11.3 User-Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. A first-order IIR filter is always available, and is useful to filter out possible DC components of the signal efficiently. Up to five biquad sections, or alternatively up to 25-tap FIR filters, are available for specific processing blocks. The coefficients of the available filters are arranged as sequentially indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched while the processor is running.

The coefficients of these filters, as shown in Table 7, are each 16 bits wide, in 2s-complement format, and occupy two consecutive 8-bit registers in the register space. Specifically, the filter coefficients, shown in Figure 39, are in 1.15 (one dot 15) format with a range from –1.0 (0x8000) to 0.999969482421875 (0x7FFF).

Table 7. ADC First-Order IIR Filter Coefficients

FILTER	FILTER COEFFICIENT	ADC COEFFICIENT, LEFT CHANNEL	ADC COEFFICIENT, RIGHT CHANNEL
First-order IIR	N0	C4 (page 4, registers 8, 9)	C36 (page 4, registers 72, 73)
	N1	C5 (page 4, registers 10, 11)	C37 (page 4, registers 74, 75)
	D1	C6 (page 4, registers 12, 13)	C38 (page 4, registers 76, 77)

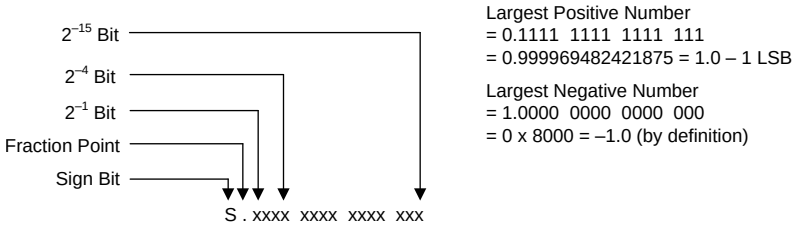


Figure 39. 2s-Complement Coefficient Format

8.3.11.3.1 First-Order IIR Section

Equation 3 gives the transfer function for the first-order IIR filter.

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (3)$$

The frequency response for the first-order IIR section with default coefficients is flat at a gain of 0 dB.

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8.3.11.3.2 Biquad Section

Equation 4 gives the transfer function of each biquad filter.

$$H(z) = \frac{N_0 + 2 \times N_1 z^{-1} + N_2 z^{-2}}{2^{15} - 2 \times D_1 z^{-1} - D_2 z^{-2}} \quad (4)$$

The frequency response for each of the biquad sections with default coefficients is flat at a gain of 0 dB. Table 8 lists the available coefficients for the five biquad filters.

Table 8. ADC Biquad Filter Coefficients

FILTER	FILTER COEFFICIENT	ADC COEFFICIENT, LEFT CHANNEL	ADC COEFFICIENT, RIGHT CHANNEL
BIQUAD A	N0	C7 (page 4, registers 14, 15)	C39 (page 4, registers 78, 79)
	N1	C8 (page 4, registers 16, 17)	C40 (page 4, registers 80, 81)
	N2	C9 (page 4, registers 18, 19)	C41 (page 4, registers 82, 83)
	D1	C10 (page 4, registers 20, 21)	C42 (page 4, registers 84, 85)
	D2	C11 (page 4, registers 22, 23)	C43 (page 4, registers 86, 87)
BIQUAD B	N0	C12 (page 4, registers 24, 25)	C44 (page 4, registers 88, 89)
	N1	C13 (page 4, registers 26, 27)	C45 (page 4, registers 90, 91)
	N2	C14 (page 4, registers 28, 29)	C46 (page 4, registers 92, 93)
	D1	C15 (page 4, registers 30, 31)	C47 (page 4, registers 94, 95)
	D2	C16 (page 4, registers 32, 33)	C48 (page 4, registers 96, 97)
BIQUAD C	N0	C17 (page 4, registers 34, 35)	C49 (page 4, registers 98, 99)
	N1	C18 (page 4, registers 36, 37)	C50 (page 4, registers 100, 101)
	N2	C19 (page 4, registers 38, 39)	C51 (page 4, registers 102, 103)
	D1	C20 (page 4, registers 40, 41)	C52 (page 4, registers 104, 105)
	D2	C21 (page 4, registers 42, 43)	C53 (page 4, registers 106, 107)
BIQUAD D	N0	C22 (page 4, registers 44, 45)	C54 (page 4, registers 108, 109)
	N1	C23 (page 4, registers 46, 47)	C55 (page 4, registers 110, 111)
	N2	C24 (page 4, registers 48, 49)	C56 (page 4, registers 112,113)
	D1	C25 (page 4, registers 50, 51)	C57 (page 4, registers 114, 115)
	D2	C26 (page 4, registers 52, 53)	C58 (page 4, registers 116, 117)
BIQUAD E	N0	C27 (page 4, registers 54, 55)	C59 (page 4, registers 118, 119)
	N1	C28 (page 4, registers 56, 57)	C60 (page 4, registers 120, 121)
	N2	C29 (page 4, registers 58, 59)	C61 (page 4, registers 122,123)
	D1	C30 (page 4, registers 60, 61)	C62 (page 4, registers 124, 125)
	D2	C31 (page 4, registers 62, 63)	C63 (page 4, registers 126, 127)

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8.3.11.3.3 FIR Section

Six of the available ADC processing blocks offer FIR filters for signal processing. PRB_R9 and PRB_R12 feature a 20-tap FIR filter, whereas the processing blocks PRB_R3, PRB_R6, PRB_R15, and PRB_R18 feature a 25-tap FIR filter. Equation 5 gives the transfer function of the Mth order FIR filter that is reconfigurable based on the processing block chosen.

$$H(z) = \sum_{n=0}^{M} FIR_n z^{-n}$$

$$M = 24 \text{ for PRB_R3, PRB_R6, PRB_R15, and PRB_R18}$$

$$M = 19 \text{ for PRB_R9 and PRB_R12} \quad (5)$$

The coefficients of the FIR filters correspond to the ADC coefficient space as listed in Table 9 and are 16-bit, 2s-complement format. There is no default transfer function for the FIR filter. When the FIR filter is used, all applicable coefficients must be programmed.

Table 9. ADC FIR Filter Coefficients

FILTER COEFFICIENT	ADC COEFFICIENT, LEFT CHANNEL	ADC COEFFICIENT, RIGHT CHANNEL
FIR0	C7 (page 4, registers 14, 15)	C39 (page 4, registers 78, 79)
FIR1	C8 (page 4, registers 16, 17)	C40 (page 4, registers 80, 81)
FIR2	C9 (page 4, registers 18, 19)	C41 (page 4, registers 82, 83)
FIR3	C10 (page 4, registers 20, 21)	C42 (page 4, registers 84, 85)
FIR4	C11 (page 4, registers 22, 23)	C43 (page 4, registers 86, 87)
FIR5	C12 (page 4, registers 24, 25)	C44 (page 4, registers 88, 89)
FIR6	C13 (page 4, registers 26, 27)	C45 (page 4, registers 90, 91)
FIR7	C14 (page 4, registers 28, 29)	C46 (page 4, registers 92, 93)
FIR8	C15 (page 4, registers 30, 31)	C47 (page 4, registers 94, 95)
FIR9	C16 (page 4, registers 32, 33)	C48 (page 4, registers 96, 97)
FIR10	C17 (page 4, registers 34, 35)	C49 (page 4, registers 98, 99)
FIR11	C18 (page 4, registers 36, 37)	C50 (page 4, registers 100, 101)
FIR12	C19 (page 4, registers 38, 39)	C51 (page 4, registers 102, 103)
FIR13	C20 (page 4, registers 40, 41)	C52 (page 4, registers 104, 105)
FIR14	C21 (page 4, registers 42, 43)	C53 (page 4, registers 106, 107)
FIR15	C22 (page 4, registers 44, 45)	C54 (page 4, registers 108, 109)
FIR16	C23 (page 4, registers 46, 47)	C55 (page 4, registers 110, 111)
FIR17	C24 (page 4, registers 48, 49)	C56 (page 4, registers 112, 113)
FIR18	C25 (page 4, registers 50, 51)	C57 (page 4, registers 114, 115)
FIR19	C26 (page 4, registers 52, 53)	C58 (page 4, registers 116, 117)
FIR20	C27 (page 4, registers 54, 55)	C59 (page 4, registers 118, 119)
FIR21	C28 (page 4, registers 56, 57)	C60 (page 4, registers 120, 121)
FIR22	C29 (page 4, registers 58, 59)	C61 (page 4, registers 122, 123)
FIR23	C30 (page 4, registers 60, 61)	C62 (page 4, registers 124, 125)
FIR24	C31 (page 4, registers 62, 63)	C63 (page 4, registers 126, 127)

8.3.11.4 Decimation Filter

The TLV320ADC3100 offers three different types of decimation filters. The integrated digital decimation filter removes high-frequency content and downsamples the audio data from an initial sampling rate of AOSR × f_S to the final output sampling rate of f_S. Decimation filtering is achieved using a higher-order cascaded integrator-comb (CIC) filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself; this filter is implicitly set through the chosen processing block.

This section describes the properties of the available filters A, B, and C.

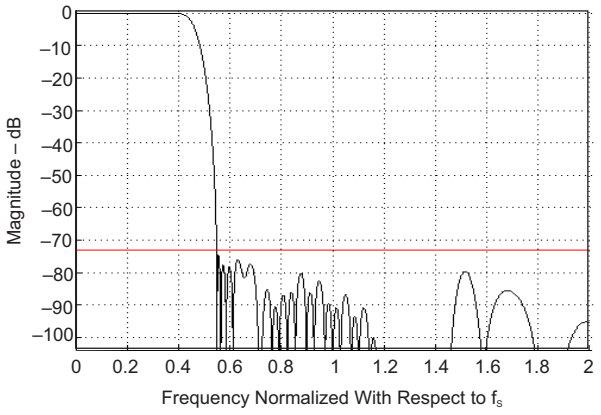
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8.3.11.4.1 Decimation Filter A

This filter is intended for use at sampling rates up to 48 kHz. When configuring this filter, the oversampling ratio of the ADC can either be 128 or 64. For highest performance, the oversampling ratio must be set to 128. Filter A can also be used for 96 kHz at an AOSR of 64. Table 10 specifies the performance of filter A. Figure 40 shows the frequency response for filter A.

Table 10. Specification for ADC Decimation Filter A

PARAMETER	CONDITION	VALUE (Typical)	UNIT
AOSR = 128			
Filter gain pass band	0 f_S–0.39 f_S	0.062	dB
Filter gain stop band	0.55 f_S–64 f_S	–73	dB
Filter group delay		17 / f_S	s
Pass-band ripple, 8 kSPS	0 f_S–0.39 f_S	0.062	dB
Pass-band ripple, 44.18 kSPS	0 f_S–0.39 f_S	0.05	dB
Pass-band ripple, 48 kSPS	0 f_S–0.39 f_S	0.05	dB
AOSR = 64			
Filter gain pass band	0 f_S–0.39 f_S	0.062	dB
Filter gain stop band	0.55 f_S–32 f_S	–73	dB
Filter group delay		17 / f_S	s
Pass-band ripple, 8 kSPS	0 f_S–0.39 f_S	0.062	dB
Pass-band ripple, 44.18 kSPS	0 f_S–0.39 f_S	0.05	dB
Pass-band ripple, 48 kSPS	0 f_S–0.39 f_S	0.05	dB
Pass-band ripple, 96 kSPS	0 kHz–20 kHz	0.1	dB



ADC channel response for decimation filter A
(red line corresponds to –73 dB)

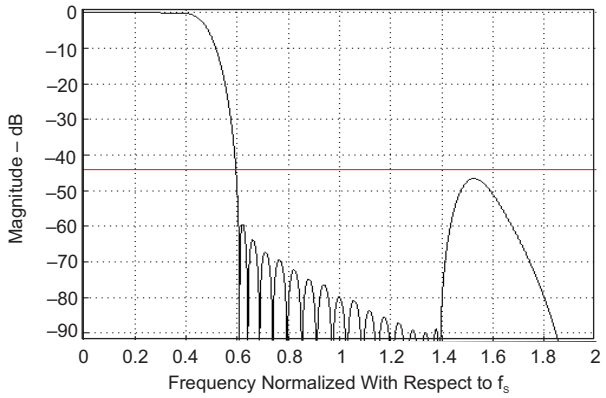
Figure 40. ADC Decimation Filter A, Frequency Response

8.3.11.4.2 Decimation Filter B

Filter B is intended to support sampling rates up to 96 kHz at an oversampling ratio of 64. Table 11 specifies the performance of filter B. Figure 41 shows the frequency response for filter B.

Table 11. Specification for ADC Decimation Filter B

PARAMETER	CONDITION	VALUE (Typical)	UNIT
AOSR = 64			
Filter gain pass band	0 f_S–0.39 f_S	±0.077	dB
Filter gain stop band	0.6 f_S–32 f_S	–46	dB
Filter group delay		11 / f_S	s
Pass-band ripple, 8 kSPS	0 f_S–0.39 f_S	0.076	dB
Pass-band ripple, 44.18 kSPS	0 f_S–0.39 f_S	0.06	dB
Pass-band ripple, 48 kSPS	0 f_S–0.39 f_S	0.06	dB
Pass-band ripple, 96 kSPS	0 kHz–20 kHz	0.11	dB



ADC channel response for decimation filter B
(red line corresponds to –44 dB)

Figure 41. ADC Decimation Filter B, Frequency Response

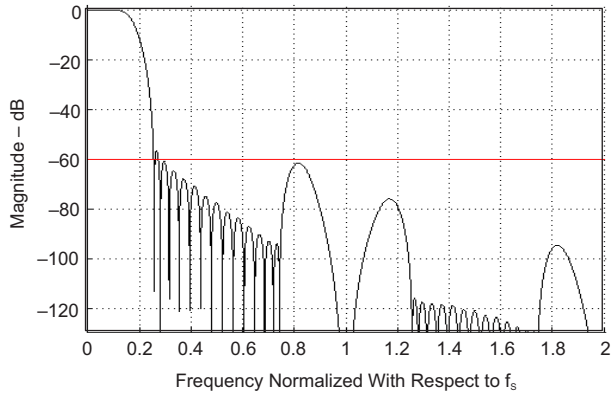
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8.3.11.4.3 Decimation Filter C

Filter type C, along with an AOSR of 32, is specially designed for 192-kSPS operation of the ADC. The pass band, which extends up to 0.11 × f_S (corresponds to 21 kHz), is suited for audio applications. Table 12 specifies the performance of filter C. Figure 42 shows the frequency response for filter C.

Table 12. Specifications for ADC Decimation Filter C

PARAMETER	CONDITION	VALUE (Typical)	UNIT
Filter gain from 0 f_S to 0.11 f_S	0 f_S–0.11 f_S	±0.033	dB
Filter gain from 0.28 f_S to 16 f_S	0.28 f_S–16 f_S	–60	dB
Filter group delay		11 / f_S	s
Pass-band ripple, 8 kSPS	0 f_S–0.11 f_S	0.033	dB
Pass-band ripple, 44.18 kSPS	0 f_S–0.11 f_S	0.033	dB
Pass-band ripple, 48 kSPS	0 f_S–0.11 f_S	0.032	dB
Pass-band ripple, 96 kSPS	0 f_S–0.11 f_S	0.032	dB
Pass-band ripple, 192 kSPS	0 kHz–20 kHz	0.086	dB



ADC channel response for decimation filter C
(red line corresponds to –60 dB)

Figure 42. ADC Decimation Filter C, Frequency Response

8.3.11.5 ADC Data Interface

The decimation filter and signal processing block in the ADC channel passes 32-bit data words to the audio serial interface one time every frame (WCLK). During each frame (WCLK), a pair of data words (for the left and right channels) is passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data per the different modes for audio serial interface.

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8.3.12 TLV320ADC3100 Comparison

Table 13 lists a comparison between the TLV320ADC3100, TLV320ADC3101, and TLV320ADC3001. The TLV320ADC3100 is form-factor and software compatible with the TLV320ADC3101.

Table 13. Device Comparison Table

FEATURES	TLV320ADC3101	TLV320ADC3001	TLV320ADC3100
Number of ADCs	2	2	2
Number of inputs/outputs	6, digital I / f	3, digital I / f	4, digital I / f
Resolution (bits)	24	24	24
Control interface	I^2C	I^2C	I^2C
Digital audio interface	LJ, RJ, I2S, DSP, TDM	LJ, RJ, I2S, DSP, TDM	LJ, RJ, I2S, DSP, TDM
Digital microphone support	Yes	No	No
Number of GPIOs	2	0	1
Number of Microphone bias	2	1	1
Package	4-mm × 4-mm, 24-pin QFN	2.24-mm × 2.16-mm, 16-pin DSBGA (WCSP)	4-mm × 4-mm, 24-pin QFN

8.4 Device Functional Modes

8.4.1 Recording Mode

The recording mode is activated when the ADC blocks are enabled. The record path operates from 8 kHz to 48 kHz in single-rate mode and up to 96 kHz in dual-rate mode. This mode contains programmable input channel configurations supporting single-ended and differential setups. In order to provide optimal system power management, the stereo recording path can be powered up one channel at time, to support when only mono record capability is required. Digital signal processing blocks can remove audible noise that may be introduced by mechanical coupling. The TLV320ADC3100 includes automatic gain control (AGC).

8.5 Programming

8.5.1 Digital Control Serial Interface

8.5.1.1 I^2C Control Mode

The TLV320ADC3100 supports the I^2C control protocol and is capable of both standard and fast modes. Standard mode is up to 100 kHz and fast mode is up to 400 kHz. When in I^2C control mode, the TLV320ADC3100 can be configured for one of four different addresses, using the I2C_ADR1 and I2C_ADR0 pins, which control the two LSBs of the device address. The five MSBs of the device address are fixed as 0011 0 and cannot be changed, whereas the two LSBs are given by I2C_ADR1:I2C_ADR0. Table 14 lists the four possible device addresses resulting from this configuration.

Table 14. I^2C Slave Device Addresses for I2C_ADR1, I2C_ADR0 Settings

I2C_ADR1	I2C_ADR0	DEVICE ADDRESS
0	0	0011 000
0	1	0011 001
1	0	0011 010
1	1	0011 011

I^2C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^2C bus only drive the bus lines low by connecting them to ground; they never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors, so the bus wires are high when no device is driving them low. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the TLV320ADC3100 can only act as a slave device.

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An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level when SCL is low (a low on SDA indicates the bit is 0; a high indicates the bit is 1). When the SDA line has settled, the SCL line is brought high, then low. This pulse on SCL clocks the SDA bit into the receiver shift register.

The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. Under normal circumstances, the master drives the clock line.

Most of the time the bus is idle, no communication is taking place, and both lines are high. When communication is taking place, the bus is active. Only master devices can start a communication by causing a START condition on the bus. Normally, the data line is only allowed to change state when the clock line is low. If the data line changes state when the clock line is high, the state is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is high and the data line goes from high to low. A STOP condition is when the clock line is high and the data line goes from low to high.

After the master issues a START condition, the master sends a byte indicating the slave device to communicate with. This byte is called the *address byte*. Each device on an I^2C bus has a unique 7-bit address that is used to respond with. (Slaves can also have 10-bit addresses; see the I^2C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether the slave device is to be read from or written to.

Every byte transmitted on the I^2C bus, whether address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, the master stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA low. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, the master pulls SDA low to acknowledge this read to the slave. The master then sends a clock pulse to clock the bit.

A not-acknowledge is performed by leaving SDA high during an acknowledge cycle. If the master attempts to address a device not present on the bus, then the master receives a not-acknowledge because no device is present at that address to pull the line low.

When a master has finished communicating with a slave, the master may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. If a START condition is issued when the bus is active, this condition is called a *repeated START condition*.

The TLV320ADC3100 also responds to and acknowledges a general call, which consists of the master issuing a command with a slave address byte of 00h. Figure 43 and Figure 44 show timing diagrams for I^2C write and read operations, respectively.

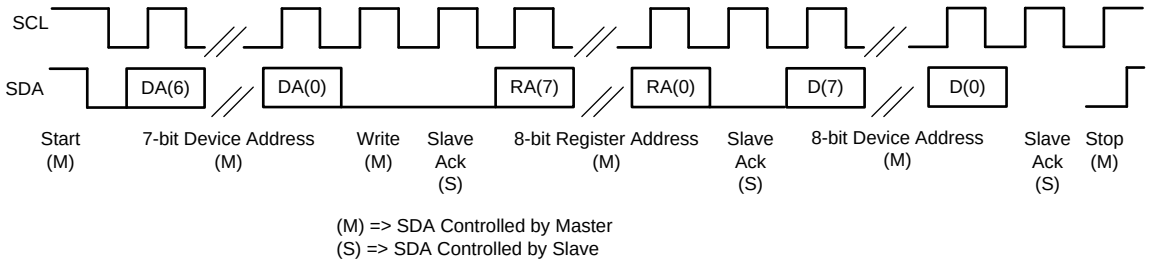


Figure 43. I^2C Write

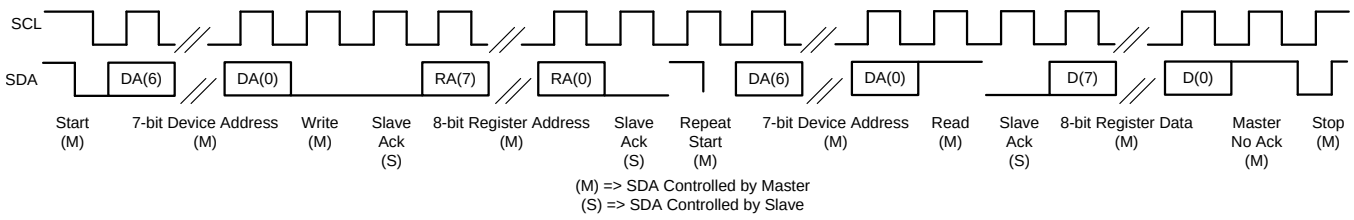


Figure 44. I^2C Read

In the case of an I^2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA are treated as the data for the next incremental register.

Similarly, after the device has transmitted the 8-bit data from the addressed register for an I^2C register read, and if the master issues an acknowledge, the slave then takes control of the SDA bus and transmits the next eight clocks of data for the next incremental register.

8.6 Register Maps

8.6.1 Control Registers

This section describes the control registers for the TLV320ADC3100 in detail. All registers are eight bits in width, with bit 7 referring to the most-significant bit of each register and bit 0 referring to the least-significant bit.

Pages 0, 1, 4, 5, and 32–47 are available. All other pages are reserved. Do not read from or write to reserved pages.

The procedure for register access is:

- Select page N (write data *N* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

Table 15. Page, Register Map

REGISTER NO.	REGISTER NAME
PAGE 0: (Clock Multipliers and Dividers, Serial Interfaces, Flags, GPIO Interrupts and Programming)	
0	Page Control Register
1	S/W RESET
2	Reserved
3	Reserved
4	Clock-Gen Multiplexing
5	PLL P and R-VAL
6	PLL J-VAL
7	PLL D-VAL MSB
8	PLL D-VAL LSB
9–17	Reserved
18	ADC NADC
19	ADC MADC
20	ADC AOSR
21	ADC IADC
22	ADC Digital Engine Decimation
23–24	Reserved
25	CLKOUT MUX
26	CLKOUT M Divider
27	ADC Audio Interface Control 1
28	Data Slot Offset Programmability 1 (Ch_Offset_1)
29	ADC Interface Control 2
30	BCLK N Divider
31	Secondary Audio Interface Control 1
32	Secondary Audio Interface Control 2
33	Secondary Audio Interface Control 3
34	I^2S Sync

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Register Maps (continued)

Table 15. Page, Register Map (continued)

REGISTER NO.	REGISTER NAME
35	Reserved
36	ADC Flag Register
37	Data Slot Offset Programmability 2 (Ch_Offset_2)
38	I^2S TDM Control Register
39–41	Reserved
42	Interrupt Flags (Overflow)
43	Interrupt Flags (Overflow)
44	Reserved
45	Interrupt Flags–ADC
46	Reserved
47	Interrupt Flags–ADC
48	INT1 Interrupt Control
49	INT2 Interrupt Control
50	Reserved
51	Reserved
52	GPIO1 Control
53	DOUT (Out Pin) Control
54–56	Reserved
57	ADC Sync Control 1
58	ADC Sync Control 2
59	ADC CIC Filter Gain Control
60	Reserved
61	ADC Processing Block Selection
62	Programmable Instruction Mode Control Bits
63–79	Reserved
80	Reserved
81	ADC Digital
82	ADC Fine Volume Control
83	Left ADC Volume Control
84	Right ADC Volume Control
85	ADC Phase Compensation
86	Left AGC Control 1
87	Left AGC Control 2
88	Left AGC Maximum Gain
89	Left AGC Attack Time
90	Left AGC Decay Time
91	Left AGC Noise Debounce
92	Left AGC Signal Debounce
93	Left AGC Gain
94	Right AGC Control 1
95	Right AGC Control 2
96	Right AGC Maximum Gain
97	Right AGC Attack Time
98	Right AGC Decay Time
99	Right AGC Noise Debounce
100	Right AGC Signal Debounce

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Register Maps (continued)

Table 15. Page, Register Map (continued)

REGISTER NO.	REGISTER NAME
101	Right AGC Gain
102–127	Reserved
PAGE1: (ADC Routing, PGA, Power-Controls, and so forth)	
0	Page Control Register
1–25	Reserved
26	Dither Control
27–50	Reserved
51	MICBIAS Control
52	Left ADC Input Selection for Left PGA
53	Reserved
54	Left ADC Input Selection for Left PGA
55	Right ADC Input Selection for Right PGA
56	Reserved
57	Right ADC Input Selection for Right PGA
58	Reserved
59	Left Analog PGA Setting
60	Right Analog PGA Setting
61	ADC Low-Current Modes
62	ADC Analog PGA Flags
63–127	Reserved
PAGE 2: Reserved. Do not read or write to this page.	
PAGE 3: Reserved. Do not read or write to this page.	
PAGE 4: ADC Programmable Coefficients RAM (1:63)	
PAGE 5: ADC Programmable Coefficients RAM (65:127)	
PAGES 6–31: Reserved. Do not read from or write to these pages.	
PAGES 32-47: ADC DSP Instruction RAM (Inst_0–Inst_511)	
Page 32 Instructions Inst_0–Inst_31	
Page 33 Instructions Inst_32–Inst_63	
Page 34 Instruction Inst_64–Inst_95 through Page 47 Instruction Inst_480–Inst_511	
PAGES 48–255: Reserved. Do not read from or write to these pages.	

Table 16 lists the access codes for the TLV320ADC3100 registers.

Table 16. TLV320ADC3100 Access Type Codes

Access Type	Code	Description
R	R	Read
R-W	R/W	Read or write
W	W	Write
-n		Value after reset or the default value

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8.6.2 Control Registers, Page 0: Clock Multipliers and Dividers, Serial Interfaces, Flags, Interrupts and Programming of GPIOs

NOTE

Valid pages are 0, 1, 4, 5, 32-47. All other pages are reserved (do not access).

8.6.2.1 Register 0: Page Control Register (address = 0d) [reset = 0000 0000b], Page 0

Figure 45. Register 0: Page Control

7	6	5	4	3	2	1	0
PAGE SEL							
R/W-0000 0000h							

Table 17. Register 0: Page Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE SEL	R/W	0h	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected (reserved) 1111 1111: Page 255 selected (reserved)

8.6.2.2 Register 1: Software Reset (address = 01d) [reset = 00h], Page 0

Figure 46. Register 1: Software Reset

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SW_RST
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	W-0h

Table 18. Register 1: Software Reset Field Descriptions

Bit	Field	Type	Reset	Description
7:1	Reserved	R	0h	Reserved. Write only zeros to these bits.
0	SW_RST	W	0h	0: Don't care 1: Self-clearing software reset for control register

8.6.2.3 Register 2: Reserved (address = 02d) [reset = 00h], Page 0

Figure 47. Register 2: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 19. Register 2: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

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8.6.2.4 Register 3: Reserved (address = 03d) [reset = XXh], Page 0

Figure 48. Register 3: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 20. Register 3: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

8.6.2.5 Register 4: Clock-Gen Multiplexing (address = 04d) [reset = 00h], Page 0

Figure 49. Register 4: Clock-Gen Multiplexing (1)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	PLL_CLKIN		CODEC_CLKIN	
R-0h	R-0h	R-0h	R-0h	R/W-00h		R/W-00h	

(1) See Figure 27 for more details on clock generation multiplexing and dividers.

Table 21. Register 4: Clock-Gen Multiplexing Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved. Do not write any value other than reset value.
3:2	PLL_CLKIN	R/W	00h	00: PLL_CLKIN = MCLK (device pin) 01: PLL_CLKIN = BCLK (device pin) 10: Reserved. Do not use. 11: PLL_CLKIN = logic level 0
1:0	CODEC_CLKIN	R/W	00h	00: CODEC_CLKIN = MCLK (device pin) 01: CODEC_CLKIN = BCLK (device pin) 10: Reserved. Do not use. 11: CODEC_CLKIN = PLL_CLK (generated on-chip)

8.6.2.6 Register 5: PLL P and R-VAL (address = 05d) [reset = 11h], Page 0

Figure 50. Register 5: PLL P and R-VAL

7	6	5	4	3	2	1	0
PLL ON	PLL DIV			PLL MULT R			
R/W-0h	R/W-001h			R/W-0001h			

Table 22. Register 5: PLL P and R-VAL Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL ON	R/W	0h	0: PLL is powered down 1: PLL is powered up
6:4	PLL DIV	R/W	001h	000: PLL divider P = 8 001: PLL divider P = 1 010: PLL divider P = 2 ... 110: PLL divider P = 6 111: PLL divider P = 7
3:0	PLL MULT R	R/W	0001h	0000: PLL multiplier R = 16 0001: PLL multiplier R = 1 0010: PLL multiplier R = 2 ... 1110: PLL multiplier R = 14 1111: PLL multiplier R = 15

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8.6.2.7 Register 6: PLL J-VAL (address = 06d) [reset = 0000 0100b], Page 0

Figure 51. Register 6: PLL J-VAL

7	6	5	4	3	2	1	0
Reserved	Reserved	PLL J-VAL					
R/W-0h	R/W-0h	R/W-00 0100h					

Table 23. Register 6: PLL J-VAL Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	0h	Reserved. Write only zeros to these bits.
5:0	PLL J-VAL	R/W	00 0100h	00 0000: Do not use (reserved) 00 0001: PLL multiplier J = 1 00 0010: PLL multiplier J = 2 00 0011: PLL multiplier J = 3 00 0100: PLL multiplier J = 4 (default) ... 11 1110: PLL multiplier J = 62 11 1111: PLL multiplier J = 63

8.6.2.8 Register 7: PLL D-VAL MSB (address = 07d) [reset = 00h], Page 0

This register is updated when page 0, register 8 is written immediately after page 0, register 7 is written.

Figure 52. Register 7: PLL D-VAL MSB

7	6	5	4	3	2	1	0
Reserved	Reserved	PLL D-VAL MSB					
R/W-0h	R/W-0h	R/W-00 0000h					

Table 24. Register 7: PLL D-VAL MSB Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R/W	0h	Reserved. Write only zeros to these bits.
5:0	PLL D-VAL MSB	R/W	00 0000h	PLL fractional multiplier bits 13:8.

8.6.2.9 Register 8: PLL D-VAL LSB (address = 08d) [reset = 00h], Page 0

This register must be written immediately after writing to page 0, register 7.

Figure 53. Register 8: PLL D-VAL LSB

7	6	5	4	3	2	1	0
PLL D-VAL LSB							
R/W-0000 0000h							

Table 25. Register 8: PLL D-VAL LSB Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL D-VAL LSB	R/W	0h	PLL fractional multiplier bits 7:0.

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8.6.2.10 Registers 9–17: Reserved (addresses = 09d, 10d, 11d, 12d, 13d, 14d, 15d, 16d, 17d) [reset = XXh], Page 0

Figure 54. Registers 9–17: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 26. Registers 9–17: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

8.6.2.11 Register 18: ADC NADC Clock Divider (address = 18d) [reset = 0000 0001b], Page 0

Figure 55. Register 18: ADC NADC Clock Divider

7	6	5	4	3	2	1	0
NADC CLK PWR	NADC CLK DIV						
R/W-0h	R/W-000 0001h						

Table 27. Register 18: ADC NADC Clock Divider Field Descriptions

Bit	Field	Type	Reset	Description
7	NADC CLK PWR	R/W	0h	NADC clock divider power control: 0: NADC clock divider is powered down 1: NADC clock divider is powered up
6:0	NADC CLK DIV	R/W	000 0001h	NADC value: 000 0000: NADC clock divider = 128 000 0001: NADC clock divider = 1 000 0010: NADC clock divider = 2 ... 111 1110: NADC clock divider = 126 111 1111: NADC clock divider = 127

8.6.2.12 Register 19: ADC MADC Clock Divider (address = 19d) [reset = 0000 0001b], Page 0

Figure 56. Register 19: ADC MADC Clock Divider

7	6	5	4	3	2	1	0
MADC CLK PWR	MADC CLK DIV						
R/W-0h	R/W-000 0001h						

Table 28. Register 19: ADC MADC Clock Divider Field Descriptions

Bit	Field	Type	Reset	Description
7	MADC CLK PWR	R/W	0h	0: ADC MADC clock divider is powered down 1: ADC MADC clock divider is powered up
6:0	MADC CLK DIV	R/W	000 0001h	000 0000: MADC clock divider = 128 000 0001: MADC clock divider = 1 000 0010: MADC clock divider = 2 ... 111 1110: MADC clock divider = 126 111 1111: MADC clock divider = 127

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8.6.2.13 Register 20: ADC AOSR (address = 20d) [reset = 1000 0000b], Page 0

Figure 57. Register 20: ADC AOSR(1)

7	6	5	4	3	2	1	0
ADC AOSR							
R/W-1000 0000h							

(1) The AOSR must be an integral multiple of the ADC decimation factor.

Table 29. Register 20: ADC AOSR Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ADC AOSR	R/W	1000 0000h	ADC oversampling value (AOSR): 0000 0000: AOSR = 256 0000 0001: AOSR = 1 0000 0010: AOSR = 2 ... 1111 1110: AOSR = 254 1111 1111: AOSR = 255

8.6.2.14 Register 21: ADC IADC (address = 21d) [reset = 1000 0000b], Page 0

Figure 58. Register 21: ADC IADC(1)

7	6	5	4	3	2	1	0
ADC IADC							
R/W-1000 0000h							

(1) The IADC must be an integral multiple of the ADC decimation factor.

Table 30. Register 21: ADC IADC Field Descriptions

Bit	Field	Type	Reset	Description
7:0	ADC IADC	R/W	1000 0000h	0000 0000: Reserved. Do not use. Number of instructions for the ADC digital filter engine (IADC): 0000 0001: IADC = 2 0000 0010: IADC = 4 ... 1011 1111: IADC = 382 1100 0000: IADC = 384 1100 0001–1111 1111: IADC = Up to 510

8.6.2.15 Register 22: ADC Digital Filter Engine Decimation (address = 22d) [reset = 0000 0100b], Page 0

Figure 59. Register 22: ADC Digital Filter Engine Decimation

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	DEC RATIO			
R-0h	R-0h	R-0h	R-0h	R/W- 01000h			

Table 31. Register 22: ADC Digital Filter Engine Decimation Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved. Do not write any value other than reset value.
3:0	DEC RATIO	R/W	0100h	0000: Decimation ratio in the ADC digital filter engine = 16 0001: Decimation ratio in the ADC digital filter engine = 1 0010: Decimation ratio in the ADC digital filter engine = 2 ... 1101: Decimation ratio in the ADC digital filter engine = 13 1110: Decimation ratio in the ADC digital filter engine = 14 1111: Decimation ratio in the ADC digital filter engine = 15

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8.6.2.16 Registers 23–24 (addresses) = 23d, 24d) [reset = XXh], Page 0

Figure 60. Registers 23–24

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 32. Registers 23–24 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

8.6.2.17 Register 25: CLKOUT MUX (address = 25d) [reset = 00h], Page 0

Figure 61. Register 25: CLKOUT MUX

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	CDIV_CLKIN		
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-000h		

Table 33. Register 25: CLKOUT MUX Field Descriptions

Bit	Field	Type	Reset	Description
7:3	Reserved	R	0h	Reserved. Do not write any value other than reset value.
2: 0	CDIV_CLKIN	R/W	000h	000: CDIV_CLKIN = MCLK (device pin) 001: CDIV_CLKIN = BCLK (device pin) 010: Reserved. Do not use. 011: CDIV_CLKIN = PLL_CLK (generated on-chip) 100: Reserved. Do not use. 101: Reserved. Do not use. 110: CDIV_CLKIN = ADC_CLK (generated on-chip) 111: CDIV_CLKIN = ADC_MOD_CLK (generated on-chip)

8.6.2.18 Register 26: CLKOUT M Divider (address = 26d) [reset = 0000 0001b], Page 0

Figure 62. Register 26: CLKOUT M Divider

7	6	5	4	3	2	1	0
CLKOUT M DIV PWR	CLKOUT M DIV						
R/W-0h	R/W-000 0001h						

Table 34. Register 26: CLKOUT M Divider Field Descriptions

Bit	Field	Type	Reset	Description
7	CLKOUT M DIV PWR	R/W	0h	0: CLKOUT M divider is powered down 1: CLKOUT M divider is powered up
6:0	CLKOUT M DIV	R/W	000 0001h	000 0000: CLKOUT divider M = 128 000 0001: CLKOUT divider M = 1 000 0010: CLKOUT divider M = 2 ... 111 1110: CLKOUT divider M = 126 111 1111: CLKOUT divider M = 127

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8.6.2.19 Register 27: ADC Audio Interface Control 1 (address = 27d) [reset = 00h], Page 0

Figure 63. Register 27: ADC Audio Interface Control 1

7	6	5	4	3	2	1	0
ADC interface		ADC interface word length		BCLK	WCLK	Reserved	Tri-State DOUT
R/W-00h		R/W-00h		R/W-0h	R/W-0h	R-0h	R/W-0h

Table 35. Register 27: ADC Audio Interface Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	ADC interface	R/W	00h	00: ADC interface = I^2S 01: ADC interface = DSP 10: ADC interface = RJF 11: ADC interface = LJF
5:4	ADC interface word length	R/W	00h	00: ADC interface word length = 16 bits 01: ADC interface word length = 20 bits 10: ADC interface word length = 24 bits 11: ADC interface word length = 32 bits
3	BCLK	R/W	0h	0: BCLK is input 1: BCLK is output
2	WCLK	R/W	0h	0: WCLK is input 1: WCLK is output
1	Reserved	R	0h	Reserved. Do not write any value other than reset value.
0	Tri-State DOUT	R/W	0h	0: Tri-stating of DOUT: disabled 1: Tri-stating of DOUT: enabled

8.6.2.20 Register 28: Data Slot Offset Programmability 1 (Ch_Offset_1) (address = 28d) [reset = 00h], Page 0

Figure 64. Register 28: Data Slot Offset Programmability 1 (Ch_Offset_1)

7	6	5	4	3	2	1	0
CH_OFFSET_1							
R/W-0000 0000h							

Table 36. Register 28: Data Slot Offset Programmability 1 (Ch_Offset_1) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CH_OFFSET_1	R/W	0h	0000 0000: Offset = 0 BCLKs. Offset is measured with respect to WCLK rising edge in DSP mode.(1) 0000 0001: Offset = 1 BCLKs 0000 0010: Offset = 2 BCLKs ... 1111 1110: Offset = 254 BCLKs 1111 1111: Offset = 255 BCLKs

(1) Usage controlled by page 0, register 38, bit 0.

8.6.2.21 Register 29: ADC Interface Control 2 (address = 29d) [reset = 0000 0010b], Page 0

Figure 65. Register 29: ADC Interface Control 2

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	BCLK_INVERT	BWCLK_PWR codec inactive	BDIV_CLKIN	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-10h	

Table 37. Register 29: ADC Interface Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R/W	0h	Reserved. Do not write any value other than reset value.
3	BCLK_INVERT	R/W	0h	0: BCLK is not inverted (valid for both primary and secondary BCLK) 1: BCLK is inverted (valid for both primary and secondary BCLK)
2	BWCLK_PWR codec inactive	R/W	0h	0: BCLK and WCLK are active even with the codec powered down: disabled (valid for both primary and secondary BCLK) 1: BCLK and WCLK are active even with the codec powered down: enabled (valid for both primary and secondary BCLK)
1:0	BDIV_CLKIN	R/W	10h	00: Reserved. Do not use. 01: Reserved. Do not use. 10: BDIV_CLKIN = ADC_CLK (generated on-chip) 11: BDIV_CLKIN = ADC_MOD_CLK (generated on-chip)

8.6.2.22 Register 30: BCLK N Divider (address = 30d) [reset = 0000 0001b], Page 0

Figure 66. Register 30: BCLK N Divider

7	6	5	4	3	2	1	0
BCLK N PWR	BCLK N DIV						
R/W-0h	R/W-000 0001h						

Table 38. Register 30: BCLK N Divider Field Descriptions

Bit	Field	Type	Reset	Description
7	BCLK N PWR	R/W	0h	0: BCLK N divider is powered down 1: BCLK N divider is powered up
6:0	BCLK N DIV	R/W	000 0001h	000 0000: CLKOUT divider N = 128 000 0001: CLKOUT divider N = 1 000 0010: CLKOUT divider N = 2 ... 111 1110: CLKOUT divider N = 126 111 1111: CLKOUT divider N = 127

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8.6.2.23 Register 31: Secondary Audio Interface Control 1 (address = 31d) [reset = 00h], Page 0

Figure 67. Register 31: Secondary Audio Interface Control 1

7	6	5	4	3	2	1	0
Reserved	Sec BCLK from GPIO1		Sec BCLK from GPIO1		Reserved	Reserved	Reserved
R-0h	R/W-00h		R/W-00h		R/W-0h	R/W-0h	R-0h

Table 39. Register 31: Secondary Audio Interface Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved. Do not write any value other than reset value.
6:5	Sec BCLK from GPIO1	R/W	00h	00: Secondary BCLK is obtained from the GPIO1 pin 01, 10, 11: Reserved. Do not use.
4:3	Sec WCLK from GPIO1	R/W	00h	00: Secondary WCLK is obtained from the GPIO1 pin 01, 10, 11: Reserved. Do not use.
2:1	Reserved	R/W	0h	Reserved. Do not use.
0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

8.6.2.24 Register 32: Secondary Audio Interface Control 2 (address = 32d) [reset = 00h], Page 0

Figure 68. Register 32: Secondary Audio Interface Control 2

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Choice of BCLK	Choice of WCLK	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R-0h	R-0h

Table 40. Register 32: Secondary Audio Interface Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved. Do not write any value other than reset value.
3	Choice of BCLK	R/W	0h	0: Primary BCLK is used for audio interface and clocking 1: Secondary BCLK is used for audio interface and clocking
2	Choice of WCLK	R/W	0h	0: Primary WCLK is used for audio interface and clocking 1: Secondary WCLK is used for audio interface and clocking
1:0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

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8.6.2.25 Register 33: Secondary Audio Interface Control 3 (address = 33d) [reset = 0001 0000b], Page 0

Figure 69. Register 33: Secondary Audio Interface Control 3

7	6	5	4	3	2	1	0
Source of Primary BCLK	Source of Secondary BCLK	Source of Primary WCLK		Source of Secondary WCLK		Reserved	Reserved
R/W-0h	R/W-0h	R/W-01h		R/W-00h		R-0h	R-0h

Table 41. Register 33: Secondary Audio Interface Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	Source of Primary BCLK	R/W	0h	0: Primary BCLK output = internally generated BCLK clock 1: Primary BCLK output = secondary BCLK
6	Source of Secondary BCLK	R/W	0h	0: Secondary BCLK output = primary BCLK 1: Secondary BCLK output = internally generated BCLK clock
5:4	Source of Primary WCLK	R/W	01h	00: Reserved. Do not use. 01: Primary WCLK output = internally generated ADC_f_S clock (default) 10: Primary WCLK output = secondary WCLK 11: Reserved. Do not use.
3:2	Source of Secondary WCLK	R/W	00h	00: Secondary WCLK output = primary WCLK 01: Reserved. Do not use. 10: Secondary WCLK output = internally generated ADC_f_S clock 11: Reserved. Do not use.
1:0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

8.6.2.26 Register 34: I^2S Sync (address = 34d) [reset = 00h], Page 0

Figure 70. Register 34: I^2S Sync

7	6	5	4	3	2	1	0
I2C hang detect	I2C hang detect flag	I2C general-call accept	Reserved	Reserved	Reserved	Re-sync logic disabled	Re-sync without soft-muting
R/W-0h	R-0h	R/W-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h

Table 42. Register 34: I^2S Sync Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C hang detect	R/W	0h	0: Internal logic is enabled to detect the I^2C hang and react accordingly 1: Internal logic is disabled to detect the I^2C hang
6 (1)	I2C hang detect flag	R	0h	0: I^2C hang is not detected 1: I^2C hang detected flag; when set, this bit is cleared only after reading this register
5	I2C general-call accept	R/W	0h	0: I^2C general-call address is ignored 1: Device accepts I^2C general-call address
4:2	Reserved	R	0h	Reserved. Do not write any value other than reset value.
1	Re-sync logic disabled	R/W	0h	0: Re-sync logic is disabled for the ADC 1: Re-sync stereo ADC with codec interface if the group delay changed by more than ±ADC_f_S / 4
0	Re-sync without soft-muting	R/W	0h	0: Re-sync is done without soft-muting the channel for the ADC 1: Re-sync is done by internally soft-muting the channel for the ADC

(1) Read-only bit. Writes to this bit are not used anywhere.

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8.6.2.27 Register 35: Reserved (address = 35d) [reset = XXh], Page 0

Figure 71. Register 35: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 43. Register 35: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

8.6.2.28 Register 36: ADC Flag Register (address = 36d) [reset = 00h], Page 0

Figure 72. Register 36: ADC Flag Register

7	6	5	4	3	2	1	0
L-ADC PGA gain	L-ADC powered up	L-AGC not saturated	Reserved	R-ADC PGA gain	R-ADC powered up	R-AGC not saturated	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 44. Register 36: ADC Flag Register Field Descriptions

Bit	Field	Type	Reset	Description
7(1)	L-ADC PGA gain	R	0h	0: Left ADC PGA, applied gain ≠ programmed gain 1: Left ADC PGA, applied gain = programmed gain
6(1)	L-ADC powered up	R	0h	0: Left ADC powered down 1: Left ADC powered up
5(1)	L-AGC not saturated	R	0h	0: Left AGC not saturated 1: Left AGC applied gain = maximum applicable gain by the left AGC
4	Reserved	R	0h	Reserved. Do not write any value other than reset value.
3(1)	R-ADC PGA gain	R	0h	0: Right ADC PGA, applied gain ≠ programmed gain 1: Right ADC PGA, applied gain = programmed gain
2(1)	R-ADC powered up	R	0h	0: Right ADC powered down 1: Right ADC powered up
1(1)	R-AGC not saturated	R	0h	0: Right AGC not saturated 1: Right AGC applied gain = maximum applicable gain by the right AGC
0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

(1) Read-only bits. Writes to this bit are not used anywhere.

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8.6.2.29 Register 37: Data Slot Offset Programmability 2 (Ch_Offset_2) (address = 37d) [reset = 00h], Page 0

Figure 73. Register 37: Data Slot Offset Programmability 2 (Ch_Offset_2)

7	6	5	4	3	2	1	0
CH OFFSET 2							
R/W-0000 0000h							

Table 45. Register 37: Data Slot Offset Programmability 2 (Ch_Offset_2) Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CH OFFSET 2	R/W	0h	0000 0000: Offset = 0 BCLKs. Offset is measured with respect to the end of the first channel(1) 0000 0001: Offset = 1 BCLKs 0000 0010: Offset = 2 BCLKs ... 1111 1110: Offset = 254 BCLKs 1111 1111: Offset = 255 BCLKs

(1) Usage is controlled by page 0, register 38, bit 0, TIME_SLOT_MODE_ENABLE.

8.6.2.30 Register 38: I^2S TDM Control Register (address = 38d) [reset = 0000 0010b], Page 0

Figure 74. Register 38: I^2S TDM Control Register

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Channel swap disable	Channel disable		EARLY_3-STATE	TIME_SLOT_MODE
R-0h	R-0h	R-0h	R/W-0h	R/W-00h		R/W-1h	R/W-0h

Table 46. Register 38: I^2S TDM Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved. Do not write any value other than reset value.
4	Channel swap disable	R/W	0h	0: Channel swap disabled 1: Channel swap enabled
3:2	Channel disable	R/W	00h	00: Both left and right channels enabled 01: Left channel enabled 10: Right channel enabled 11: Both left and right channels disabled
1	EARLY_3-STATE	R/W	1h	0: EARLY_3-STATE disabled 1: EARLY_3-STATE enabled
0	TIME_SLOT_MODE	R/W	0h	0: TIME_SLOT_MODE disabled – both channel offsets controlled by Ch_Offset_1 (page 0, register 28) 1: TIME_SLOT_MODE enabled – channel-1 offset controlled by Ch_Offset_1 (page 0, register 28) and channel-2 offset controlled by Ch_Offset_2 (page 0, register 37)

8.6.2.31 Registers 39–41 (addresses) = 39d, 40d, 41d) [reset = XXh], Page 0

Figure 75. Registers 39–41

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 47. Registers 39–41 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

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8.6.2.32 Register 42: Interrupt Flags (Overflow) (address = 42d) [reset = 00h], Page 0

Figure 76. Register 42: Interrupt Flags (Overflow)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Left ADC overflow flag	Right ADC overflow flag	ADC barrel-shifter overflow flag	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 48. Register 42: Interrupt Flags (Overflow) Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved
3(1)	Left ADC overflow flag	R	0h	Left ADC overflow flag
2(1)	Right ADC overflow flag	R	0h	Right ADC overflow flag
1(1)	ADC barrel-shifter overflow flag	R	0h	ADC barrel-shifter output-overflow flag
0	Reserved	R	0h	Reserved

(1) Sticky flag bits. These are read-only bits. These bits are automatically cleared when read and are set only if a new source trigger occurs.

8.6.2.33 Register 43: Interrupt Flags (Overflow) (address = 43d) [reset = 00h], Page 0

Figure 77. Register 43: Interrupt Flags (Overflow)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	L-ADC Overflow	R-ADC Overflow	ADC barrel-shifter overflow flag	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 49. Register 43: Interrupt Flags (Overflow) Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved
3	L-ADC Overflow	R	0h	Left ADC overflow flag
2	R-ADC Overflow	R	0h	Right ADC overflow flag
1	ADC barrel-shifter overflow flag	R	0h	ADC barrel-shifter output-overflow flag
0	Reserved	R	0h	Reserved

8.6.2.34 Register 44: Reserved (address = 44d) [reset = XXh], Page 0

Figure 78. Register 44: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 50. Register 44: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

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8.6.2.35 Register 45: Interrupt Flags—ADC (address = 45d) [reset = 00h], Page 0

Figure 79. Register 45: Interrupt Flags—ADC

7	6	5	4	3	2	1	0
Reserved	Left AGC Noise Threshold Flag	Right AGC Noise Threshold Flag	ADC digital filter engine standard interrupt-port output	ADC digital filter engine auxiliary interrupt-port output	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 51. Register 45: Interrupt Flags—ADC Field Descriptions

Bit	Field	Type	Reset	Description(1)
7	Reserved	R	0h	Reserved
6	Left AGC Noise Threshold Flag	R	0h	0: Left ADC signal power is greater than the noise threshold for the left AGC 1: Left ADC signal power is less than the noise threshold for the left AGC
5	Right AGC Noise Threshold Flag	R	0h	0: Right ADC signal power is greater than the noise threshold for the right AGC 1: Right ADC signal power is less than the noise threshold for the right AGC
4	ADC digital filter engine standard interrupt-port output	R	0h	ADC digital filter engine standard interrupt-port output
3	ADC digital filter engine auxiliary interrupt-port output	R	0h	ADC digital filter engine auxiliary interrupt-port output
2:0	Reserved	R	0h	Reserved

(1) Sticky flag bits. These are read-only bits. These bits are automatically cleared when read and are set only if a new source trigger occurs.

8.6.2.36 Register 46: Reserved (address = 46d) [reset = XXh], Page 0

Figure 80. Register 46: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 52. Register 46: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

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8.6.2.37 Register 47: Interrupt Flags—ADC (address = 47d) [reset = 00h], Page 0

Figure 81. Register 47: Interrupt Flags—ADC

7	6	5	4	3	2	1	0
Reserved	L-ADC power status	R-ADC power status	ADC Filt Std-Out Instantaneous Value	ADC Filt Aux-Out Instantaneous Value	Reserved	Reserved	Reserved
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 53. Register 47: Interrupt Flags—ADC Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	L-ADC power status	R	0h	0: Left ADC signal power is greater than the noise threshold for the left AGC 1: Left ADC signal power is less than the noise threshold for the left AGC
5	R-ADC power status	R	0h	0: Right ADC signal power is greater than the noise threshold for the right AGC 1: Right ADC signal power is less than the noise threshold for the right AGC
4	ADC Filt Std-Out Instantaneous Value	R	0h	ADC digital filter engine standard interrupt-port output. This bit indicates the instantaneous value of the interrupt port at the time of reading the register.
3	ADC Filt Aux-Out Instantaneous Value	R	0h	ADC digital filter engine auxiliary interrupt-port output. This bit indicates the instantaneous value of the interrupt port at the time of reading the register.
2:0	Reserved	R	0h	Reserved

8.6.2.38 Register 48: INT1 Interrupt Control (address = 48d) [reset = 00h], Page 0

Figure 82. Register 48: INT1 Interrupt Control

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	INT1 uses ADC AGC noise	Reserved	INT1 uses Engine interrupts	INT1 uses ADC data-ready interrupts	No. of INT1 Pulses
R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

Table 54. Register 48: INT1 Interrupt Control Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved. Do not write any value other than reset value.
4	INT1 uses ADC AGC noise	R/W	0h	0: ADC AGC noise interrupt is not used in the generation of INT1 interrupt 1: ADC AGC noise interrupt is used in the generation of INT1 interrupt
3	Reserved	R	0h	Reserved. Do not write any value other than reset value.
2	INT1 uses Engine interrupts	R/W	0h	0: Engine-generated interrupts and overflow flags are not used in the generation of INT1 interrupt 1: Engine-generated interrupts and overflow flags are used in the generation of INT1 interrupt
1	INT1 uses ADC data-ready interrupts	R/W	0h	0: ADC data-available interrupt is not used in the generation of INT1 interrupt 1: ADC data-available interrupt is used in the generation of INT1 interrupt
0	No. of INT1 Pulses	R/W	0h	0: INT1 is only one pulse (active high) of duration typical 2 ms 1: INT1 is multiple pulses (active high) of duration typical 2 ms and period 4 ms, until flag register 42 or 45 is read

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8.6.2.39 Register 49: INT2 Interrupt Control (address = 49d) [reset = 00h], Page 0

Figure 83. Register 49: INT2 Interrupt Control

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	INT2 Uses ADC AGC Noise	Reserved	INT2 Uses Engine Interrupts	INT2 Uses ADC Data-Ready Interrupts	No. of INT2 Pulses
R-0h	R-0h	R-0h	R/W-0h	R-0h	R/W-0h	R/W-0h	R/W-0h

Table 55. Register 49: INT2 Interrupt Control Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved. Do not write any value other than reset value.
4	INT2 Uses ADC AGC Noise	R/W	0h	0: ADC AGC noise interrupt is not used in the generation of INT2 interrupt 1: ADC AGC noise interrupt is used in the generation of INT2 interrupt
3	Reserved	R	0h	Reserved. Do not write any value other than reset value.
2	INT2 Uses Engine Interrupts	R/W	0h	0: Engine-generated interrupts and overflow flags are not used in the generation of INT2 interrupt 1: Engine-generated interrupts and overflow flags are used in the generation of INT2 interrupt
1	INT2 Uses ADC Data-Ready Interrupts	R/W	0h	0: ADC data-available interrupt is not used in the generation of INT2 interrupt 1: ADC data-available interrupt is used in the generation of INT2 interrupt
0	No. of INT2 Pulses	R/W	0h	0: INT2 is only one pulse (active high) of duration typical 2 ms 1: INT2 is multiple pulses (active high) of duration typical 2 ms and period 4 ms, until flag register 42 or 45 is read

8.6.2.40 Register 50: Reserved (address = 50d) [reset = XXh], Page 0

Figure 84. Register 50: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 56. Register 50: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

8.6.2.41 Register 51: Reserved (address = 51d) [reset = 00h], Page 0

Figure 85. Register 51: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 57. Register 51: Reserved

Bit	Field	Type	Reset	Description
7:0	Reserved	R/W	0h	Reserved. Do not write any value other than reset value.

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8.6.2.42 Register 52: GPIO1 Control (address = 52d) [reset = 00h], Page 0

Figure 86. Register 52: GPIO1 Control

7	6	5	4	3	2	1	0
Reserved	Reserved	GPIO1 SEL				GPIO1 IN BUF VAL	GPIO1 VAL
R-0h	R-0h	R/W-0000h				R-0h	R/W-0h

Table 58. Register 52: GPIO1 Control Field Descriptions

Bit	Field	Type	Reset	Description
7:6	Reserved	R	0h	Reserved. Do not write any value other than reset value.
5:2	GPIO1 SEL	R/W	0000h	0000: GPIO1 disabled (input and output buffers powered down) 0001: GPIO1 is in input mode (can be used as secondary BCLK input, secondary WCLK input, or in ClockGen block) 0010: GPIO1 is used as general-purpose input (GPI) 0011: GPIO1 output = general-purpose output 0100: GPIO1 output = CLKOUT output (source determined by CDIV_CLKIN_REG; page 0, register 25) 0101: GPIO1 output = INT1 output 0110: GPIO1 output = INT2 output 0111: Reserved. Do not use. 1000: GPIO1 output = secondary BCLK output for codec interface 1001: GPIO1 output = secondary WCLK output for codec interface 1010: DMDIN output = ADC_MOD_CLK output for the digital microphone 1011–1111: Reserved. Do not use.
1	GPIO1 IN BUF VAL	R	0h	GPIO1 input buffer value
0	GPIO1 VAL	R/W	0h	0: GPIO1 value = 0 when bits 5:2 are programmed to 0011 (general-purpose output) 1: GPIO1 value = 1 when bits 5:2 are programmed to 0011 (general-purpose output)

8.6.2.43 Register 53: DOUT (OUT Pin) Control (address = 53d) [reset = 0001 0010b], Page 0

Figure 87. Register 53: DOUT (OUT Pin) Control

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	DOUT bus-keeper EN	DOUT FUNC SEL			DOUT VAL
R-0h	R-0h	R-0h	R/W-1h	R/W-001h			R/W-0h

Table 59. Register 53: DOUT (OUT Pin) Control Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved. Do not write any value other than reset value.
4	DOUT bus-keeper EN	R/W	1h	0: DOUT bus keeper enabled 1: DOUT bus keeper disabled
3:1	DOUT FUNC SEL	R/W	001h	000: DOUT disabled (output buffer powered down) 001 DOUT = primary DOUT output for codec interface 010: DOUT = general-purpose output 011: DOUT = CLKOUT output 100: DOUT = INT1 output 101: DOUT = INT2 output 110: DOUT = secondary BCLK output for codec interface 111: DOUT = secondary WCLK output for codec interface
0	DOUT VAL	R/W	0h	DOUT value = 0 when bits 3:1 are programmed to 010 (general-purpose output) DOUT value = 1 when bits 3:1 are programmed to 010 (general-purpose output)

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8.6.2.44 Registers 54–56 (addresses) = 54d, 55d, 56d) [reset = XXh], Page 0

Figure 88. Registers 54–56

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 60. Registers 54–56 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

8.6.2.45 Register 57: ADC Sync Control 1 (address = 57d) [reset = 00h], Page 0

Figure 89. Register 57: ADC Sync Control 1

7	6	5	4	3	2	1	0
SYNC SEL	CUSTOM SYNC SETTING						
R/W-0h	R/W-000 0000h						

Table 61. Register 57: ADC Sync Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC1 SEL	R/W	0h	0: Default synchronization 1: Custom synchronization
6:0	CUSTOM SYNC1 SETTING	R/W	000 0000h	000 0000: Custom synchronization window size = 0 instructions 000 0001: Custom synchronization window size = 2 instructions (±1 instruction) 000 0010: Custom synchronization window size = 4 instructions (±2 instructions) ... 111 1111: Custom synchronization window size = 254 instructions (±127 instructions)

8.6.2.46 Register 58: ADC Sync Control 2 (address = 58d) [reset = 00h], Page 0

Figure 90. Register 58: ADC Sync Control 2

7	6	5	4	3	2	1	0
CUSTOM SYNC2 TARGET							
R/W-0000 0000h							

Table 62. Register 58: ADC Sync Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CUSTOM SYNC2 TARGET	R/W	0h	0000 0000: Custom synchronization target = instruction 0 0000 0001: Custom synchronization target = instruction 2 0000 0010: Custom synchronization target = instruction 4 ... 1111 1111: Custom synchronization target = instruction 510

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8.6.2.47 Register 59: ADC CIC Filter Gain Control (address = 59d) [reset = 0100 0100h], Page 0

Figure 91. Register 59: ADC CIC Filter Gain Control

7	6	5	4	3	2	1	0
L-CIC FILT GAIN				R-CIC FILT GAIN			
R/W-0100h				R/W-0100h			

Table 63. Register 59: ADC CIC Filter Gain Control Field Descriptions

Bit	Field	Type	Reset	Description
7:4	L-CIC FILT GAIN	R/W	0100h	Left CIC filter gain(1)
3:0	R-CIC FILT GAIN	R/W	0100h	Right CIC filter gain(1)

(1) For proper operation, the CIC gain must be ≤ 1.
If AOSR (page 0, register 20) = 64 and [1 ≤ Filter Mode (page 0, register 61) ≤ 6], then the reset value of 4 results in CIC gain = 1.
Otherwise, the CIC gain = [AOSR / (64 × Digital Filter Engine Decimation)]^4 × 2 $^{(\text{CIC Filter Gain Control})}$ for 0 ≤ CIC Filter Gain Control ≤ 12, and if CIC Filter Gain Control = 15, CIC gain is automatically set such that for 7 ≤ (AOSR / Digital Filter Engine Decimation) ≤ 64, 0.5 < CIC gain ≤ 1.

8.6.2.48 Register 60: Reserved (address = 60d) [reset = 00h], Page 0

Figure 92. Register 60: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 64. Register 60: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R/W	0h	Reserved. Do not write to this register.

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8.6.2.49 Register 61: ADC Processing Block Selection (address = 61d) [reset = 0000 0001h], Page 0

Figure 93. Register 61: ADC Processing Block Selection

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	PRB SEL				
R/W-0h	R/W-0h	R/W-0h	R/W-0 0001h				

Table 65. Register 61: ADC Processing Block Selection Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R/W	0h	Reserved. Do not write any value other than reset value.
4:0	PRB SEL	R/W	0 0001h	0 0000: Reserved. Do not use. 0 0001: Select ADC signal processing block PRB_R1 0 0010: Select ADC signal processing block PRB_R2 0 0011: Select ADC signal processing block PRB_R3 0 0100: Select ADC signal processing block PRB_R4 0 0101: Select ADC signal processing block PRB_R5 0 0110: Select ADC signal processing block PRB_R6 0 0111: Select ADC signal processing block PRB_R7 0 1000: Select ADC signal processing block PRB_R8 0 1001: Select ADC signal processing block PRB_R9 0 1010: Select ADC signal processing block PRB_R10 0 1011: Select ADC signal processing block PRB_R11 0 1100: Select ADC signal processing block PRB_R12 0 1101: Select ADC signal processing block PRB_R13 0 1110: Select ADC signal processing block PRB_R14 0 1111: Select ADC signal processing block PRB_R15 1 0000: Select ADC signal processing block PRB_R16 1 0001: Select ADC signal processing block PRB_R17 1 0010: Select ADC signal processing block PRB_R18 1 0011–1 1111: Reserved. Do not use.

8.6.2.50 Register 62: Programmable Instruction-Mode Control Bits (address = 62d) [reset = 00h], Page 0

Figure 94. Register 62: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 66. Register 62: Reserved

Bit	Field	Type	Reset	Description
7:0	Reserved	R/W	0h	Reserved. Do not write any value other than reset value.

8.6.2.51 Registers 63–79: Reserved (address = 63d - 79d) [reset = XXh], Page 0

Figure 95. Registers 63–79: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 67. Registers 63–79: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

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8.6.2.52 Register 80: Reserved (address = 80d) [reset = 00h], Page 0

Figure 96. Register 80: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 68. Register 80: Reserved

Bit	Field	Type	Reset	Description
7:0	Reserved	R/W	0h	Reserved. Do not write any value other than reset value.

8.6.2.53 Register 81: ADC Digital (address = 81d) [reset = 00h], Page 0

Figure 97. Register 81: ADC Digital

7	6	5	4	3	2	1	0
L-ADC PWR EN	R-ADC PWR EN	Reserved				ADC SOFT-STEP	
R/W-0h	R/W-0h	R/W-0000h				R/W-00h	

Table 69. Register 81: ADC Digital Field Descriptions

Bit	Field	Type	Reset	Description
7	L-ADC PWR EN	R/W	0h	0: Left-channel ADC is powered down 1: Left-channel ADC is powered up
6	R-ADC PWR EN	R/W	0h	0: Right-channel ADC is powered down 1: Right-channel ADC is powered up
5:2	Reserved	R/W	0000h	Reserved. Do not write any value other than reset value.
1:0	ADC SOFT-STEP	R/W	00h	00: ADC channel volume control soft-stepping is enabled for one step / f_S 01: ADC channel volume control soft-stepping is enabled for one step / 2 f_S 10: ADC channel volume control soft-stepping is disabled 11: Reserved. Do not use.

8.6.2.54 Register 82: ADC Fine Volume Control (address = 82d) [reset = 1000 1000h], Page 0

Figure 98. Register 82: ADC Fine Volume Control

7	6	5	4	3	2	1	0
L-ADC MUTE	L-ADC FINE GAIN			R-ADC MUTE	R-ADC FINE GAIN		
R/W-1h	R/W-000h			R/W-1h	R/W-000h		

Table 70. Register 82: ADC Fine Volume Control Field Descriptions

Bit	Field	Type	Reset	Description
7	L-ADC MUTE	R/W	1h	0: Left ADC channel not muted 1: Left ADC channel muted
6:4	L-ADC FINE GAIN	R/W	000h	000: Left ADC channel fine gain = 0 dB 001: Left ADC channel fine gain = –0.1 dB 010: Left ADC channel fine gain = –0.2 dB 011: Left ADC channel fine gain = –0.3 dB 100: Left ADC channel fine gain = –0.4 dB 101–111: Reserved. Do not use.
3	R-ADC MUTE	R/W	1h	0: Right ADC channel not muted 1: Right ADC channel muted
2:0	R-ADC FINE GAIN	R/W	000h	000: Right ADC channel fine gain = 0 dB 001: Right ADC channel fine gain = –0.1 dB 010: Right ADC channel fine gain = –0.2 dB 011: Right ADC channel fine gain = –0.3 dB 100: Right ADC channel fine gain = –0.4 dB 101–111: Reserved. Do not use.

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8.6.2.55 Register 83: Left ADC Volume Control (address = 83d) [reset = 00h], Page 0

Figure 99. Register 83: Left ADC Volume Control

7	6	5	4	3	2	1	0
Reserved	L-ADC CH VOL						
R-0h	R/W-000 0000h						

Table 71. Register 83: Left ADC Volume Control Field Descriptions

Bit	Field	Type	Reset(1)	Description
7	Reserved	R	0h	Reserved. Do not write any value other than reset value.
6:0	L-ADC CH VOL	R/W	000 0000h	100 0000 – 110 1000: Left ADC channel volume = 0 dB 110 1000: Left ADC channel volume = –12 dB 110 1001: Left ADC channel volume = –11.5 dB 110 1010: Left ADC channel volume = –11.0 dB ... 111 1111: Left ADC channel volume = –0.5 dB 000 0000: Left ADC channel volume = –0.0 dB 000 0001: Left ADC channel volume = 0.5 dB ... 010 0110: Left ADC channel volume = 19.0 dB 010 0111: Left ADC channel volume = 19.5 dB 010 1000: Left ADC channel volume = 20 dB 010 1001– 011 1111 : Reserved. Do not use.

(1) Values in 2s-complement decimal format.

8.6.2.56 Register 84: Right ADC Volume Control (address = 84d) [reset = 00h], Page 0

Figure 100. Register 84: Right ADC Volume Control

7	6	5	4	3	2	1	0
Reserved	R-ADC CH VOL						
R-0h	R/W-000 0000h						

Table 72. Register 84: Right ADC Volume Control Field Descriptions

Bit	Field	Type	Reset(1)	Description
7	Reserved	R	0h	Reserved. Do not write any value other than reset value.
6:0	R-ADC CH VOL	R/W	000 0000h	100 0000 – 110 1000: Right ADC channel volume = 0 dB 110 1000: Right ADC channel volume = –12 dB 110 1001: Right ADC channel volume = –11.5 dB 110 1010: Right ADC channel volume = –11.0 dB ... 111 1111: Right ADC channel volume = –0.5 dB 000 0000: Right ADC channel volume = –0.0 dB 000 0001: Right ADC channel volume = 0.5 dB ... 010 0110: Right ADC channel volume = 19.0 dB 010 0111: Right ADC channel volume = 19.5 dB 010 1000: Right ADC channel volume = 20 dB 010 1001– 011 1111 : Reserved. Do not use.

(1) Values in 2s-complement decimal format.

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8.6.2.57 Register 85: Left ADC Phase Compensation (address = 85d) [reset = 00h], Page 0

Figure 101. Register 85: Left ADC Phase Compensation

7	6	5	4	3	2	1	0
L-ADC PHASE COMP							
R/W-0000 0000h							

Table 73. Register 85: Left ADC Phase Compensation Field Descriptions

Bit	Field	Type	Reset	Description
7:0	L-ADC PHASE COMP	R/W	0h	1000 0000: Left ADC has a phase shift of –128 ADC_MOD_CLK cycles with respect to right ADC 1000 0001: Left ADC has a phase shift of –127 ADC_MOD_CLK cycles with respect to right ADC ... 1111 1110: Left ADC has a phase shift of –2 ADC_MOD_CLK cycles with respect to right ADC 1111 1111: Left ADC has a phase shift of –1 ADC_MOD_CLK cycles with respect to right ADC 0000 0000: No phase shift between stereo ADC channels 0000 0001: Left ADC has a phase shift of 1 ADC_MOD_CLK cycles with respect to right ADC 0000 0010: Left ADC has a phase shift of 2 ADC_MOD_CLK cycles with respect to right ADC ... 0111 1110: Left ADC has a phase shift of 126 ADC_MOD_CLK cycles with respect to right ADC 0111 1111: Left ADC has a phase shift of 127 ADC_MOD_CLK cycles with respect to right ADC

8.6.2.58 Register 86: Left AGC Control 1 (address = 86d) [reset = 00h], Page 0

Figure 102. Register 86: Left AGC Control 1

7	6	5	4	3	2	1	0
L-AGC EN	L-AGC TARGET			Reserved	Reserved	Reserved	Reserved
R/W-0h	R/W-000h			R/W-0h	R/W-0h	R/W-0h	R-0h

Table 74. Register 86: Left AGC Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	L-AGC EN	R/W	0h	0: Left AGC disabled 1: Left AGC enabled
6:4	L-AGC TARGET	R/W	000h	000: Left AGC target level = –5.5 dB 001: Left AGC target level = –8 dB 010: Left AGC target level = –10 dB 011: Left AGC target level = –12 dB 100: Left AGC target level = –14 dB 101: Left AGC target level = –17 dB 110: Left AGC target level = –20 dB 111: Left AGC target level = –24 dB
3:0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

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8.6.2.59 Register 87: Left AGC Control 2 (address = 87d) [reset = 00h], Page 0

Figure 103. Register 87: Left AGC Control 2

7	6	5	4	3	2	1	0
L-AGC HYST		L-AGC NOISE THRESHOLD					AGC CLIP STEPPING EN
R/W-00h		R/W- 0 0000h					R/W-0h

Table 75. Register 87: Left AGC Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	L-AGC HYST	R/W	0h	00: Left AGC hysteresis setting of 1 dB 01: Left AGC hysteresis setting of 2 dB 10: Left AGC hysteresis setting of 4 dB 11: Left AGC hysteresis disabled
5:1	L-AGC NOISE THRESHOLD	R/W	0 0000h	00 000: Left AGC noise or silence detection is disabled 00 001: Left AGC noise threshold = –30 dB 00 010: Left AGC noise threshold = –32 dB 00 011: Left AGC noise threshold = –34 dB ... 11 101: Left AGC noise threshold = –86 dB 11 110: Left AGC noise threshold = –88 dB 11 111: Left AGC noise threshold = –90 dB
0	L-AGC CLIP STEPPING EN	R/W	0h	0: Disable clip stepping for AGC 1: Enable clip stepping for AGC

8.6.2.60 Register 88: Left AGC Maximum Gain (address = 88d) [reset = 0111 1111b], Page 0

Figure 104. Register 88: Left AGC Maximum Gain

7	6	5	4	3	2	1	0
Reserved	L-AGC MAX GAIN						
R-0h	R/W-111 1111h						

Table 76. Register 88: Left AGC Maximum Gain Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved. Do not write any value other than reset value.
6:0	L-AGC MAX GAIN	R/W	111 1111h	000 0000: Left AGC maximum gain = 0 dB 000 0001: Left AGC maximum gain = 0.5 dB 000 0010: Left AGC maximum gain = 1 dB ... 101 0000: Left AGC maximum gain = 40 dB 101 0001 – 111 1111: Reserved. Do not use.

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8.6.2.61 Register 89: Left AGC Attack Time (address = 89d) [reset = 00h], Page 0

Figure 105. Register 89: Left AGC Attack Time

7	6	5	4	3	2	1	0
L-AGC ATTACK TIME					L-AGC ATTACK TIME MULT		
R/W-0000 0h					R/W-000h		

Table 77. Register 89: Left AGC Attack Time Field Descriptions

Bit	Field	Type	Reset	Description
7:3	L-AGC ATTACK TIME	R/W	0000 0h	0000 0: Left AGC attack time = 1 × (32 / f_S) 0000 1: Left AGC attack time = 3 × (32 / f_S) 0001 0: Left AGC attack time = 5 × (32 / f_S) 0001 1: Left AGC attack time = 7 × (32 / f_S) 0010 0: Left AGC attack time = 9 × (32 / f_S) ... 1111 0: Left AGC attack time = 61 × (32 / f_S) 1111 1: Left AGC attack time = 63 × (32 / f_S)
2:0	L-AGC ATTACK TIME MULT	R/W	000h	000: Multiply factor for the programmed left AGC attack time = 1 001: Multiply factor for the programmed left AGC attack time = 2 010: Multiply factor for the programmed left AGC attack time = 4 ... 111: Multiply factor for the programmed left AGC attack time = 128

8.6.2.62 Register 90: Left AGC Decay Time (address = 90d) [reset = 00h], Page 0

Figure 106. Register 90: Left AGC Decay Time

7	6	5	4	3	2	1	0
L-AGC DECAY TIME					L-AGC DECAY TIME MULT		
R/W-0000 0h					R/W-000h		

Table 78. Register 90: Left AGC Decay Time Field Descriptions

Bit	Field	Type	Reset	Description
7:3	L-AGC DECAY TIME	R/W	0000 0h	0000 0: Left AGC decay time = 1 × (512 / f_S) 0000 1: Left AGC decay time = 3 × (512 / f_S) 0001 0: Left AGC decay time = 5 × (512 / f_S) 0001 1: Left AGC decay time = 7 × (512 / f_S) 0010 0: Left AGC decay time = 9 × (512 / f_S) ... 1111 0: Left AGC decay time = 61 × (512 / f_S) 1111 1: Left AGC decay time = 63 × (512 / f_S)
2:0	L-AGC DECAY TIME MULT	R/W	000h	000: Multiply factor for the programmed left AGC decay time = 1 001: Multiply factor for the programmed left AGC decay time = 2 010: Multiply factor for the programmed left AGC decay time = 4 ... 111: Multiply factor for the programmed left AGC decay time = 128

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8.6.2.63 Register 91: Left AGC Noise Debounce (address = 91d) [reset = 00h], Page 0

Figure 107. Register 91: Left AGC Noise Debounce

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	L-AGC NOISE DEBOUNCE				
R-0h	R-0h	R-0h	R/W-0 0000h				

Table 79. Register 91: Left AGC Noise Debounce Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved. Do not write any value other than reset value.
4:0	L-AGC NOISE DEBOUNCE	R/W	0 0000h	0 0000: Left AGC noise debounce = 0 / f_S 0 0001: Left AGC noise debounce = 4 / f_S 0 0010: Left AGC noise debounce = 8 / f_S 0 0011: Left AGC noise debounce = 16 / f_S 0 0100: Left AGC noise debounce = 32 / f_S 0 0101: Left AGC noise debounce = 64 / f_S 0 0110: Left AGC noise debounce = 128 / f_S 0 0111: Left AGC noise debounce = 256 / f_S 0 1000: Left AGC noise debounce = 512 / f_S 0 1001: Left AGC noise debounce = 1024 / f_S 0 1010: Left AGC noise debounce = 2048 / f_S 0 1011: Left AGC noise debounce = 4096 / f_S 0 1100: Left AGC noise debounce = 2 × 4096 / f_S 0 1101: Left AGC noise debounce = 3 × 4096 / f_S 0 1110: Left AGC noise debounce = 4 × 4096 / f_S ... 1 1110: Left AGC noise debounce = 20 × 4096 / f_S 1 1111: Left AGC noise debounce = 21 × 4096 / f_S

8.6.2.64 Register 92: Left AGC Signal Debounce (address = 92d) [reset = 00h], Page 0

Figure 108. Register 92: Left AGC Signal Debounce

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	L-AGC SIGNAL DEBOUNCE			
R-0h	R-0h	R-0h	R-0h	R/W-0000h			

Table 80. Register 92: Left AGC Signal Debounce Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved. Do not write any value other than reset value.
3:0	L-AGC SIGNAL DEBOUNCE	R/W	0000h	0000: Left AGC signal debounce = 0 / f_S 0001: Left AGC signal debounce = 4 / f_S 0010: Left AGC signal debounce = 8 / f_S 0011: Left AGC signal debounce = 16 / f_S 0100: Left AGC signal debounce = 32 / f_S 0101: Left AGC signal debounce = 64 / f_S 0110: Left AGC signal debounce = 128 / f_S 0111: Left AGC signal debounce = 256 / f_S 1000: Left AGC signal debounce = 512 / f_S 1001: Left AGC signal debounce = 1024 / f_S 1010: Left AGC signal debounce = 2048 / f_S 1011: Left AGC signal debounce = 2 × 2048 / f_S 1100: Left AGC signal debounce = 3 × 2048 / f_S 1101: Left AGC signal debounce = 4 × 2048 / f_S 1110: Left AGC signal debounce = 5 × 2048 / f_S 1111: Left AGC signal debounce = 6 × 2048 / f_S

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8.6.2.65 Register 93: Left AGC Gain Applied (address = 93d) [reset = 00h], Page 0

Figure 109. Register 93: Left AGC Gain Applied

7	6	5	4	3	2	1	0
L-AGC GAIN APPL							
R-0000 0000h							

Table 81. Register 93: Left AGC Gain Applied Field Descriptions

Bit	Field	Type	Reset	Description
7:0(1)	L-AGC GAIN APPL	R	0h	Left AGC Gain Value Status: 1110 1000: Gain applied by left AGC = –12 dB 1110 1001: Gain applied by left AGC = –11.5 dB ... 1111 1111: Gain applied by left AGC = –0.5 dB 0000 0000: Gain applied by left AGC = 0 dB 0000 0001: Gain applied by left AGC = 0.5 dB ... 0100 1111: Gain applied by left AGC = 39.5 dB 0101 0000: Gain applied by left AGC = 40 dB 0101 0001 – 1111 1111: Reserved. Do not use.

(1) These bits are read-only.

8.6.2.66 Register 94: Right AGC Control 1 (address = 94d) [reset = 00h], Page 0

Figure 110. Register 94: Right AGC Control 1

7	6	5	4	3	2	1	0
R-AGC EN	R-AGC TARGET			Reserved	Reserved	Reserved	Reserved
R/W-0h	R/W-000h			R-0h	R-0h	R-0h	R-0h

Table 82. Register 94: Right AGC Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	R-AGC EN	R/W	0h	0: Right AGC disabled 1: Right AGC enabled
6:4	R-AGC TARGET	R/W	000h	000: Right AGC target level = –5.5 dB 000: Right AGC target level = –8 dB 001: Right AGC target level = –10 dB 010: Right AGC target level = –12 dB 011: Right AGC target level = –14 dB 100: Right AGC target level = –17 dB 101: Right AGC target level = –20 dB 111: Right AGC target level = –24 dB
3:0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

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8.6.2.67 Register 95: Right AGC Control 2 (address = 95d) [reset = 00h], Page 0

Figure 111. Register 95: Right AGC Control 2

7	6	5	4	3	2	1	0
R-AGC HYST		R-AGC NOISE THRESHOLD					R-AGC CLIP STEPPING
R/W-00h		R/W-00 000h					R/W-0h

Table 83. Register 95: Right AGC Control 2 Field Descriptions

Bit	Field	Type	Reset(1)	Description
7:6	R-AGC HYST	R/W	00h	00: Right AGC hysteresis setting of 1 dB 01: Right AGC hysteresis setting of 2 dB 10: Right AGC hysteresis setting of 4 dB 11: Right AGC hysteresis disabled.
5:1	R-AGC NOISE THRESHOLD	R/W	00 000h	00 000: Right AGC noise or silence detection is disabled 00 001: Right AGC noise threshold = –30 dB 00 010: Right AGC noise threshold = –32 dB 00 011: Right AGC noise threshold = –34 dB ... 11 101: Right AGC noise threshold = –86 dB 11 110: Right AGC noise threshold = –88 dB 11 111: Right AGC noise threshold = –90 dB
0	R-AGC CLIP STEPPING	R/W	0h	0: Disable clip stepping for right AGC 1: Enable clip stepping for right AGC

(1) Values in 2s-complement decimal format.

8.6.2.68 Register 96: Right AGC Maximum Gain (address = 96d) [reset = 0111 1111b], Page 0

Figure 112. Register 96: Right AGC Maximum Gain

7	6	5	4	3	2	1	0
Reserved	R-AGC MAX GAIN						
R-0h	R/W-111 1111h						

Table 84. Register 96: Right AGC Maximum Gain Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved. Do not write any value other than reset value.
6:0	R-AGC MAX GAIN	R/W	111 1111h	000 0000: Right AGC maximum gain = 0 dB 000 0001: Right AGC maximum gain = 0.5 dB 000 0010: Right AGC maximum gain = 1 dB ... 101 0000: Right AGC maximum gain = 40 dB 101 0001–111 1111: Not used.

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8.6.2.69 Register 97: Right AGC Attack Time (address = 97d) [reset = 00h], Page 0

Figure 113. Register 97: Right AGC Attack Time

7	6	5	4	3	2	1	0
R-AGC ATTACK TIME					R-AGC ATTACK TIME MULT		
R/W-0000 0h					R/W-000h		

Table 85. Register 97: Right AGC Attack Time Field Descriptions

Bit	Field	Type	Reset	Description
7:3	R-AGC ATTACK TIME	R/W	0000 0h	0000 0: Right AGC attack time = 1 × (32 / f_S) 0000 1: Right AGC attack time = 3 × (32 / f_S) 0001 0: Right AGC attack time = 5 × (32 / f_S) 0001 1: Right AGC attack time = 7 × (32 / f_S) 0010 0: Right AGC attack time = 9 × (32 / f_S) ... 1111 0: Right AGC attack time = 61 × (32 / f_S) 1111 1: Right AGC attack time = 63 × (32 / f_S)
2:0	R-AGC ATTACK TIME MULT	R/W	000h	000: Multiply factor for the programmed right AGC attack time = 1 001: Multiply factor for the programmed right AGC attack time = 2 010: Multiply factor for the programmed right AGC attack time = 4 ... 111: Multiply factor for the programmed right AGC attack time = 128

8.6.2.70 Register 98: Right AGC Decay Time (address = 98d) [reset = 00h], Page 0

Figure 114. Register 98: Right AGC Decay Time

7	6	5	4	3	2	1	0
R-AGC DECAY TIME					R-AGC DECAY TIME MULT		
R/W-0000 0h					R/W-000h		

Table 86. Register 98: Right AGC Decay Time Field Descriptions

Bit	Field	Type	Reset	Description
7:3	R-AGC DECAY TIME	R/W	0000 0h	0000 0: Right AGC decay time = 1 × (512 / f_S) 0000 1: Right AGC decay time = 3 × (512 / f_S) 0001 0: Right AGC decay time = 5 × (512 / f_S) 0001 1: Right AGC decay time = 7 × (512 / f_S) 0010 0: Right AGC decay time = 9 × (512 / f_S) ... 1111 0: Right AGC decay time = 61 × (512 / f_S) 1111 1: Right AGC decay time = 63 × (512 / f_S)
2:0	R-AGC DECAY TIME MULT	R/W	000h	000: Multiply factor for the programmed right AGC decay time = 1 001: Multiply factor for the programmed right AGC decay time = 2 010: Multiply factor for the programmed right AGC decay time = 4 111: Multiply factor for the programmed right AGC decay time = 128

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8.6.2.71 Register 99: Right AGC Noise Debounce (address = 99d) [reset = 00h], Page 0

Figure 115. Register 99: Right AGC Noise Debounce

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	R-AGC NOISE DEBOUNCE				
R-0h	R-0h	R-0h	R/W-0 0000h				

Table 87. Register 99: Right AGC Noise Debounce Field Descriptions

Bit	Field	Type	Reset	Description
7:5	Reserved	R	0h	Reserved. Do not write any value other than reset value.
4:0	R-AGC NOISE DEBOUNCE	R/W	0 0000h	0 0000: Right AGC noise debounce = 0 / f_S 0 0001: Right AGC noise debounce = 4 / f_S 0 0010: Right AGC noise debounce = 8 / f_S 0 0011: Right AGC noise debounce = 16 / f_S 0 0100: Right AGC noise debounce = 32 / f_S 0 0101: Right AGC noise debounce = 64 / f_S 0 0110: Right AGC noise debounce = 128 / f_S 0 0111: Right AGC noise debounce = 256 / f_S 0 1000: Right AGC noise debounce = 512 / f_S 0 1001: Right AGC noise debounce = 1024 / f_S 0 1010: Right AGC noise debounce = 2048 / f_S 0 1011: Right AGC noise debounce = 4096 / f_S 0 1100: Right AGC noise debounce = 2 × 4096 / f_S 0 1101: Right AGC noise debounce = 3 × 4096 / f_S 0 1110: Right AGC noise debounce = 4 × 4096 / f_S ... 1 1110: Right AGC noise debounce = 20 × 4096 / f_S 1 1111: Right AGC noise debounce = 21 × 4096 / f_S, right AGC noise debounce = 0 / f_S

8.6.2.72 Register 100: Right AGC Signal Debounce (address = 100d) [reset = 00h], Page 0

Figure 116. Register 100: Right AGC Signal Debounce

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	R-AGC SIGNAL DEBOUNCE			
R-0h	R-0h	R-0h	R-0h	R/W-0000h			

Table 88. Register 100: Right AGC Signal Debounce Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Reserved	R	0h	Reserved. Do not write any value other than reset value.
3:0	R-AGC SIGNAL DEBOUNCE	R/W	0000h	0000: Right AGC signal debounce = 0 / f_S 0001: Right AGC signal debounce = 4 / f_S 0010: Right AGC signal debounce = 8 / f_S 0011: Right AGC signal debounce = 16 / f_S 0100: Right AGC signal debounce = 32 / f_S 0101: Right AGC signal debounce = 64 / f_S 0110: Right AGC signal debounce = 128 / f_S 0111: Right AGC signal debounce = 256 / f_S 1000: Right AGC signal debounce = 512 / f_S 1001: Right AGC signal debounce = 1024 / f_S 1010: Right AGC signal debounce = 2048 / f_S 1011: Right AGC signal debounce = 2 × 2048 / f_S 1100: Right AGC signal debounce = 3 × 2048 / f_S 1101: Right AGC signal debounce = 4 × 2048 / f_S 1110: Right AGC signal debounce = 5 × 2048 / f_S 1111: Right AGC signal debounce = 6 × 2048 / f_S, right AGC signal debounce = 0 / f_S

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8.6.2.73 Register 101: Right AGC Gain Applied (address = 101d) [reset = 00h], Page 0

Figure 117. Register 101: Right AGC Gain Applied

7	6	5	4	3	2	1	0
R-AGC GAIN APPL							
R-0000 0000h							

Table 89. Register 101: Right AGC Gain Applied Field Descriptions

Bit	Field	Type(1)	Reset	Description
7:0	R-AGC GAIN APPL	R	0h	Right AGC gain value status: 1110 1000: Gain applied by right AGC = –12 dB 1110 1001: Gain applied by right AGC = –11.5 dB ... 1111 1111: Gain applied by right AGC = –0.5 dB 0000 0000: Gain applied by right AGC = 0 dB 0000 0001: Gain applied by right AGC = 0.5 dB ... 0100 1111: Gain applied by right AGC = 39.5 dB 0101 0000: Gain applied by right AGC = 40 dB 0101 0001 – 1111 1111: Reserved. Do not use.

(1) These bits are read-only.

8.6.2.74 Register 102–127: Reserved (addresses) = 102d–127d) [reset = XXh], Page 0

Figure 118. Register 102–127: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 90. Register 102–127: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

8.6.3 Control Registers, Page 1: ADC Routing, PGA, Power Controls, and So Forth

NOTE

Valid pages are 0, 1, 4, 5, 32-47. All other pages are reserved (do not access).

8.6.3.1 Register 0: Page Control Register (address = 0d) [reset = 00h], Page 1

Figure 119. Register 0: Page Control Register

7	6	5	4	3	2	1	0
PAGE 0 CTRL							
R/W-0000 0000h							

Table 91. Register 0: Page Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE 0 CTRL	R/W	0h	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected (reserved) 1111 1111: Page 255 selected (reserved)

8.6.3.2 Register 1–25: Reserved (addresses) = 01d–25d) [reset = XXh], Page 1

Figure 120. Register 1–25: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 92. Register 1–25: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

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8.6.3.3 Register 26: Dither Control (address = 26d) [reset = 00h], Page 1

Figure 121. Register 26: Dither Control

7	6	5	4	3	2	1	0
L-ADC DITHER OFFSET				R-ADC DITHER OFFSET			
R/W-0000h				R/W-0000h			

Table 93. Register 26: Dither Control Field Descriptions

Bit	Field	Type	Reset	Description
7:4	L-ADC DITHER OFFSET	R/W	0000h	DC offset into input of left ADC; signed magnitude number in ±15-mV steps. 1111: –105 mV ... 1011: –45 mV 1010: –30 mV 1001: –15 mV 0000: 0 mV 0001: 15 mV 0010: 30 mV 0011: 45 mV ... 0111: 105 mV
3:0	R-ADC DITHER OFFSET	R/W	0000h	DC offset into input of right ADC; signed magnitude number in ±15-mV steps. 1111: –105 mV ... 1011: –45 mV 1010: –30 mV 1001: –15 mV 0000: 0 mV 0001: 15 mV 0010: 30 mV 0011: 45 mV ... 0111: 105 mV

8.6.3.4 Register 27–50: Reserved (addresses) = 27d–50d) [reset = XXh], Page 1

Figure 122. Register 27–50: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 94. Register 27–50: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

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8.6.3.5 Register 51: MICBIAS Control (address = 51d) [reset = 00h], Page 1

Figure 123. Register 51: MICBIAS Control

7	6	5	4	3	2	1	0
Reserved	MICBIAS VALUE		Reserved	Reserved	Reserved	Reserved	Reserved
R-0h	R/W-00h		R/W-0h	R/W-0h	R-0h	R-0h	R-0h

Table 95. Register 51: MICBIAS Control Field Descriptions

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved. Do not write any value other than reset value.
6:5	MICBIAS VALUE	R/W	00h	00: MICBIAS1 is powered down 01: MICBIAS1 is powered to 2 V 10: MICBIAS1 is powered to 2.5 V 11: MICBIAS1 is connected to AVDD
4:3	Reserved	R/W	0h	Reserved. Do not write any value other than reset value.
2:0	Reserved	R	0h	Reserved. Do not write any value other than reset value.

8.6.3.6 Register 52: Left ADC Input Selection for Left PGA (address = 52d) [reset = 0101 0111b], Page 1

Figure 124. Register 52: Left ADC Input Selection for Left PGA

7	6	5	4	3	2	1	0
LCH_SEL4		LCH_SEL3		LCH_SEL2		Reserved	Reserved
R/W-01h		R/W-01h		R/W-01h		R/W-1h	R/W-1h

Table 96. Register 52: Left ADC Input Selection for Left PGA Field Descriptions

Bit	Field	Type	Reset	Description(1)
7:6	LCH_SEL4	R/W	01h	Differential pair using the IN2L(P) as plus and IN3L(M) as minus inputs. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10: Is not connected to the left ADC PGA 11: Is not connected to the left ADC PGA
5:4	LCH_SEL3	R/W	01h	Used for the IN3L(M) pin, which is single-ended. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10: Is not connected to the left ADC PGA 11: Is not connected to the left ADC PGA
3:2	LCH_SEL2	R/W	01h	Used for the IN2L(P) pin, which is single-ended. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10: Is not connected to the left ADC PGA 11: Is not connected to the left ADC PGA
1:0	Reserved	R/W	1h	Reserved. Do not write any value other than reset value.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs have a 2× gain applied.

8.6.3.7 Register 53: Reserved (address = 53d) [reset = XXh], Page 1

Figure 125. Register 53: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 97. Register 53: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

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8.6.3.8 Register 54: Left ADC Input Selection for Left PGA (address = 54d) [reset = 0011 1111h], Page 1

Figure 126. Register 54: Left ADC Input Selection for Left PGA

7	6	5	4	3	2	1	0
L PGA BYPASS	LCH_SELCM	LCH_SEL3X		LCH_SEL2X		Reserved	Reserved
R/W-0h	R/W-0h	R/W-01h		R/W-01h		R/W-1h	R/W-1h

Table 98. Register 54: Left ADC Input Selection for Left PGA Field Descriptions

Bit	Field	Type	Reset	Description(1)
7	L PGA BYPASS	R/W	0h	0: Do not bypass left PGA 1: Bypass left PGA, unbuffered differential pair using the IN2L(P) as plus and IN3L(M) as minus inputs
6	LCH_SELCM	R/W	0h	0: Left ADC channel unselected inputs are not biased weakly to the ADC common-mode voltage 1: Left ADC channel unselected inputs are biased weakly to the ADC common-mode voltage
5:4	LCH_SEL3X	R/W	01h	Differential pair using the IN2L(P) as plus and IN2R(M) as minus inputs. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10–11: Not connected to the left ADC PGA
3:2	LCH_SEL2X	R/W	01h	Differential pair using the IN2R(P) as plus and IN3R(M) as minus inputs. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10–11: Is not connected to the left ADC PGA
1:0	Reserved	R/W	1h	Reserved. Do not write any value other than reset value.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs have a 2× gain applied.

8.6.3.9 Register 55: Right ADC Input Selection for Right PGA (address = 55d) [reset = 0101 0111b], Page 1

Figure 127. Register 55: Right ADC Input Selection for Right PGA

7	6	5	4	3	2	1	0
RCH_SEL4		RCH_SEL3		RCH_SEL2		Reserved	Reserved
R/W-01h		R/W-01h		R/W-01h		R/W-1h	R/W-1h

Table 99. Register 55: Right ADC Input Selection for Right PGA Field Descriptions

Bit	Field	Type	Reset	Description(1)
7:6	RCH_SEL4	R/W	01h	Differential pair using the IN2R(P) as plus and IN3R(M) as minus inputs. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10–11: Not connected to the right ADC PGA
5:4	RCH_SEL3	R/W	01h	Used for the IN3R(M) pin, which is single-ended. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10–11: Not connected to the right ADC PGA
3:2	RCH_SEL2	R/W	01h	Used for the IN2R(P) pin, which is single-ended. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10–11: Not connected to the right ADC PGA
1:0	Reserved	R/W	1h	Reserved. Do not write any value other than reset value.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs have a 2× gain applied.

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8.6.3.10 Register 56: Reserved (address = 56d) [reset = XXh], Page 1

Figure 128. Register 56: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 100. Register 56: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

8.6.3.11 Register 57: Right ADC Input Selection for Right PGA (address = 57d) [reset = 0001 0111b], Page 1

Figure 129. Register 57: Right ADC Input Selection for Right PGA

7	6	5	4	3	2	1	0
R PGA BYPASS	RCH_SELCM	RCH_SEL3X		RCH_SEL2X		Reserved	Reserved
R/W-0h	R/W-0h	R/W-01h		R/W-01h		R/W-1h	R/W-1h

Table 101. Register 57: Right ADC Input Selection for Right PGA Field Descriptions

Bit	Field	Type	Reset	Description(1)
7	R PGA BYPASS	R/W	0h	0: Do not bypass right PGA 1: Bypass right PGA, unbuffered differential pair using the IN2R(P) as plus and IN3R(M) as minus inputs
6	RCH_SELCM	R/W	0h	0: Right ADC channel unselected inputs are not biased weakly to the ADC common-mode voltage 1: Right ADC channel unselected inputs are biased weakly to the ADC common-mode voltage
5:4	RCH_SEL3X	R/W	01h	Differential pair using the IN2L(P) as plus and IN2R(M) as minus inputs. 00: 0-dB setting is chosen 01: –6 dB setting is chosen 10–11: Not connected to the right ADC PGA
3:2	RCH_SEL2X	R/W	01h	Differential pair using the IN2L(P) as plus and IN3L(M) as minus inputs. 00: 0-dB setting is chosen 01: –6-dB setting is chosen 10, 11: Not connected to the right ADC PGA
1:0	Reserved	R/W	1h	Reserved. Do not write any value other than reset value.

(1) To maintain the same PGA output level for both single-ended and differential pairs, the single-ended inputs have a 2× gain applied.

8.6.3.12 Register 58: Reserved (address = 58d) [reset = XXh], Page 1

Figure 130. Register 58: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 102. Register 58: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to this register.

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8.6.3.13 Register 59: Left Analog PGA Settings (address = 59d) [reset = 1000 0000h], Page 1

Figure 131. Register 59: Left Analog PGA Settings

7	6	5	4	3	2	1	0
L PGA MUTE	L-PGA GAIN						
R/W-1h	R/W-000 0000h						

Table 103. Register 59: Left Analog PGA Settings Field Descriptions

Bit	Field	Type	Reset	Description
7	L PGA MUTE	R/W	1h	0: Left PGA is not muted 1: Left PGA is muted
6:0	L-PGA GAIN	R/W	000 0000h	000 0000: Left PGA gain = 0 dB 000 0001: Left PGA gain = 0.5 dB 000 0010: Left PGA gain = 1 dB ... 101 0000: Left PGA gain = 40 dB 101 0001–111 1111: Reserved. Do not use.

8.6.3.14 Register 60: Right Analog PGA Settings (address = 60d) [reset = 1000 0000h], Page 1

Figure 132. Register 60: Right Analog PGA Settings

7	6	5	4	3	2	1	0
R-PGA MUTE	R-PGA GAIN						
R/W-1h	R/W-000 0000h						

Table 104. Register 60: Right Analog PGA Settings Field Descriptions

Bit	Field	Type	Reset	Description
7	R PGA MUTE	R/W	1h	0: Right PGA is not muted 1: Right PGA is muted
6:0	R-PGA GAIN	R/W	000 0000h	000 0000: Right PGA gain = 0 dB 000 0001: Right PGA gain = 0.5 dB 000 010: Right PGA gain = 1 dB ... 101 0000: Right PGA gain = 40 dB 101 0001–111 1111: Reserved. Do not use.

8.6.3.15 Register 61: ADC Low Current Modes (address = 61d) [reset = 00h], Page 1

Figure 133. Register 61: ADC Low Current Modes

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MODULATOR CURRENT
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R/W-0h

Table 105. Register 61: ADC Low Current Modes Field Descriptions

Bit	Field	Type	Reset	Description
7:1	Reserved	R	0h	Reserved. Write only zeros to these bits.
0	MODULATOR CURRENT	R/W	0h	0: 1× ADC modulator current used 1: 0.5× ADC modulator current used

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8.6.3.16 Register 62: ADC Analog PGA Flags (address = 62d) [reset = 00h], Page 1

Figure 134. Register 62: ADC Analog PGA Flags

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	L ADC PGA FLAG	R ADC PGA FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 106. Register 62: ADC Analog PGA Flags Field Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved	R	0h	Reserved. Do not write any value other than reset value
1	L ADC PGA FLAG	R	0h	0: Left ADC PGA , applied gain ≠ programmed gain 1: Left ADC PGA , applied gain = programmed gain
0	R ADC PGA FLAG	R	0h	0: Right ADC PGA , applied gain ≠ programmed gain 1: Right ADC PGA , applied gain = programmed gain

8.6.3.17 Register 63–127: Reserved (addresses) = 63d–127d) [reset = XXh], Page 1

Figure 135. Register 63–127: Reserved

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh	R-Xh

Table 107. Register 63–127: Reserved Field Descriptions

Bit	Field	Type	Reset	Description
7:0	Reserved	R	Xh	Reserved. Do not write to these registers.

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8.6.4 Control Registers, Page 4: ADC Digital Filter Coefficients

Default values shown for this page only become valid 100 µs following a hardware or software reset.

NOTE

Valid pages are 0, 1, 4, 5, 32-47. All other pages are reserved (do not access).

8.6.4.1 Register 0: Page Control (address = 00d) [reset = 00h], Page 4

Figure 136. Register 0: Page Control

7	6	5	4	3	2	1	0
PAGE SELECT							
R/W-0000 0000h							

Table 108. Register 0: Page Control Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PAGE SELECT	R/W	0h	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected (reserved) 1111 1111: Page 255 selected (reserved)

The remaining page 4 registers are either reserved registers or are used for setting coefficients for the various filters in the processing blocks. Reserved registers must not be written to.

The filter coefficient registers are arranged in pairs, with two adjacent 8-bit registers containing the 16-bit coefficient for a single filter. The 16-bit integer contained in the MSB and LSB registers for a coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32,768 to 32,767. When programming any coefficient value for a filter, the MSB register must always be written first, immediately followed by the LSB register. Even if only the MSB or LSB portion of the coefficient changes, both registers must be written in this sequence. Table 109 is a list of the page 4 registers, excluding the previously described register 0.

Table 109. Page 4 Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	XXXX XXXX	Reserved. Do not write to this register.
2	0000 0001	Coefficient N0(15:8) for AGC LPF (first-order IIR) used as averager to detect level(1)
3	0001 0111	Coefficient N0(7:0) for AGC LPF (first-order IIR) used as averager to detect level
4	0000 0001	Coefficient N1(15:8) for AGC LPF (first-order IIR) used as averager to detect level
5	0001 0111	Coefficient N1(7:0) for AGC LPF (first-order IIR) used as averager to detect level
6	0111 1101	Coefficient D1(15:8) for AGC LPF (first-order IIR) used as averager to detect level
7	1101 0011	Coefficient D1(7:0) for AGC LPF (first-order IIR) used as averager to detect level
8	0111 1111	Coefficient N0(15:8) for Left ADC programmable first-order IIR
9	1111 1111	Coefficient N0(7:0) for Left ADC programmable first-order IIR
10	0000 0000	Coefficient N1(15:8) for Left ADC programmable first-order IIR
11	0000 0000	Coefficient N1(7:0) for Left ADC programmable first-order IIR
12	0000 0000	Coefficient D1(15:8) for Left ADC programmable first-order IIR
13	0000 0000	Coefficient D1(7:0) for Left ADC programmable first-order IIR
14	0111 1111	Coefficient N0(15:8) for Left ADC Biquad A or Coefficient FIR0(15:8) for ADC FIR Filter
15	1111 1111	Coefficient N0(7:0) for Left ADC Biquad A or Coefficient FIR0(7:0) for ADC FIR Filter
16	0000 0000	Coefficient N1(15:8) for Left ADC Biquad A or Coefficient FIR1(15:8) for ADC FIR Filter
17	0000 0000	Coefficient N1(7:0) for Left ADC Biquad A or Coefficient FIR1(7:0) for ADC FIR Filter
18	0000 0000	Coefficient N2(15:8) for Left ADC Biquad A or Coefficient FIR2(15:8) for ADC FIR Filter

(1) Rows belonging to the same coefficient are shaded in this table for easier readability.

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Table 109. Page 4 Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
19	0000 0000	Coefficient N2(7:0) for Left ADC Biquad A or Coefficient FIR2(7:0) for ADC FIR Filter
20	0000 0000	Coefficient D1(15:8) for Left ADC Biquad A or Coefficient FIR3(15:8) for ADC FIR Filter
21	0000 0000	Coefficient D1(7:0) for Left ADC Biquad A or Coefficient FIR3(7:0) for ADC FIR Filter
22	0000 0000	Coefficient D2(15:8) for Left ADC Biquad A or Coefficient FIR4(15:8) for ADC FIR Filter
23	0000 0000	Coefficient D2(7:0) for Left ADC Biquad A or Coefficient FIR4(7:0) for ADC FIR Filter
24	0111 1111	Coefficient N0(15:8) for Left ADC Biquad B or Coefficient FIR5(15:8) for ADC FIR Filter
25	1111 1111	Coefficient N0(7:0) for Left ADC Biquad B or Coefficient FIR5(7:0) for ADC FIR Filter
26	0000 0000	Coefficient N1(15:8) for Left ADC Biquad B or Coefficient FIR6(15:8) for ADC FIR Filter
27	0000 0000	Coefficient N1(7:0) for Left ADC Biquad B or Coefficient FIR6(7:0) for ADC FIR Filter
28	0000 0000	Coefficient N2(15:8) for Left ADC Biquad B or Coefficient FIR7(15:8) for ADC FIR Filter
29	0000 0000	Coefficient N2(7:0) for Left ADC Biquad B or Coefficient FIR7(7:0) for ADC FIR Filter
30	0000 0000	Coefficient D1(15:8) for Left ADC Biquad B or Coefficient FIR8(15:8) for ADC FIR Filter
31	0000 0000	Coefficient D1(7:0) for Left ADC Biquad B or Coefficient FIR8(7:0) for ADC FIR Filter
32	0000 0000	Coefficient D2(15:8) for Left ADC Biquad B or Coefficient FIR9(15:8) for ADC FIR Filter
33	0000 0000	Coefficient D2(7:0) for Left ADC Biquad B or Coefficient FIR9(7:0) for ADC FIR Filter
34	0111 1111	Coefficient N0(15:8) for Left ADC Biquad C or Coefficient FIR10(15:8) for ADC FIR Filter
35	1111 1111	Coefficient N0(7:0) for Left ADC Biquad C or Coefficient FIR10(7:0) for ADC FIR Filter
36	0000 0000	Coefficient N1(15:8) for Left ADC Biquad C or Coefficient FIR11(15:8) for ADC FIR Filter
37	0000 0000	Coefficient N1(7:0) for Left ADC Biquad C or Coefficient FIR11(7:0) for ADC FIR Filter
38	0000 0000	Coefficient N2(15:8) for Left ADC Biquad C or Coefficient FIR12(15:8) for ADC FIR Filter
39	0000 0000	Coefficient N2(7:0) for Left ADC Biquad C or Coefficient FIR12(7:0) for ADC FIR Filter
40	0000 0000	Coefficient D1(15:8) for Left ADC Biquad C or Coefficient FIR13(15:8) for ADC FIR Filter
41	0000 0000	Coefficient D1(7:0) for Left ADC Biquad C or Coefficient FIR13(7:0) for ADC FIR Filter
42	0000 0000	Coefficient D2(15:8) for Left ADC Biquad C or Coefficient FIR14(15:8) for ADC FIR Filter
43	0000 0000	Coefficient D2(7:0) for Left ADC Biquad C or Coefficient FIR14(7:0) for ADC FIR Filter
44	0111 1111	Coefficient N0(15:8) for Left ADC Biquad D or Coefficient FIR15(15:8) for ADC FIR Filter
45	1111 1111	Coefficient N0(7:0) for Left ADC Biquad D or Coefficient FIR15(7:0) for ADC FIR Filter
46	0000 0000	Coefficient N1(15:8) for Left ADC Biquad D or Coefficient FIR16(15:8) for ADC FIR Filter
47	0000 0000	Coefficient N1(7:0) for Left ADC Biquad D or Coefficient FIR16(7:0) for ADC FIR Filter
48	0000 0000	Coefficient N2(15:8) for Left ADC Biquad D or Coefficient FIR17(15:8) for ADC FIR Filter
49	0000 0000	Coefficient N2(7:0) for Left ADC Biquad D or Coefficient FIR17(7:0) for ADC FIR Filter
50	0000 0000	Coefficient D1(15:8) for Left ADC Biquad D or Coefficient FIR18(15:8) for ADC FIR Filter
51	0000 0000	Coefficient D1(7:0) for Left ADC Biquad D or Coefficient FIR18(7:0) for ADC FIR Filter
52	0000 0000	Coefficient D2(15:8) for Left ADC Biquad D or Coefficient FIR19(15:8) for ADC FIR Filter
53	0000 0000	Coefficient D2(7:0) for Left ADC Biquad D or Coefficient FIR19(7:0) for ADC FIR Filter
54	0111 1111	Coefficient N0(15:8) for Left ADC Biquad E or Coefficient FIR20(15:8) for ADC FIR Filter
55	1111 1111	Coefficient N0(7:0) for Left ADC Biquad E or Coefficient FIR20(7:0) for ADC FIR Filter
56	0000 0000	Coefficient N1(15:8) for Left ADC Biquad E or Coefficient FIR21(15:8) for ADC FIR Filter
57	0000 0000	Coefficient N1(7:0) for Left ADC Biquad E or Coefficient FIR21(7:0) for ADC FIR Filter
58	0000 0000	Coefficient N2(15:8) for Left ADC Biquad E or Coefficient FIR22(15:8) for ADC FIR Filter
59	0000 0000	Coefficient N2(7:0) for Left ADC Biquad E or Coefficient FIR22(7:0) for ADC FIR Filter
60	0000 0000	Coefficient D1(15:8) for Left ADC Biquad E or Coefficient FIR23(15:8) for ADC FIR Filter
61	0000 0000	Coefficient D1(7:0) for Left ADC Biquad E or Coefficient FIR23(7:0) for ADC FIR Filter
62	0000 0000	Coefficient D2(15:8) for Left ADC Biquad E or Coefficient FIR24(15:8) for ADC FIR Filter
63	0000 0000	Coefficient D2(7:0) for Left ADC Biquad E or Coefficient FIR24(7:0) for ADC FIR Filter
64	0000 0000	Reserved
65	0000 0000	Reserved

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Table 109. Page 4 Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
66	0000 0000	Reserved
67	0000 0000	Reserved
68	0000 0000	Reserved
69	0000 0000	Reserved
70	0000 0000	Reserved
71	0000 0000	Reserved
72	0000 0000	Coefficient N0(15:8) for Right ADC programmable first-order IIR
73	0000 0000	Coefficient N0(7:0) for Right ADC programmable first-order IIR
74	0000 0000	Coefficient N1(15:8) for Right ADC programmable first-order IIR
75	0000 0000	Coefficient N1(7:0) for Right ADC programmable first-order IIR
76	0000 0000	Coefficient D1(15:8) for Right ADC programmable first-order IIR
77	0000 0000	Coefficient D1(7:0) for Right ADC programmable first-order IIR
78	0000 0000	Coefficient N0(15:8) for Right ADC Biquad A or Coefficient FIR0(15:8) for ADC FIR Filter
79	0000 0000	Coefficient N0(7:0) for Right ADC Biquad A or Coefficient FIR0(7:0) for ADC FIR Filter
80	0000 0000	Coefficient N1(15:8) for Right ADC Biquad A or Coefficient FIR1(15:8) for ADC FIR Filter
81	0000 0000	Coefficient N1(7:0) for Right ADC Biquad A or Coefficient FIR1(7:0) for ADC FIR Filter
82	0000 0000	Coefficient N2(15:8) for Right ADC Biquad A or Coefficient FIR2(15:8) for ADC FIR Filter
83	0000 0000	Coefficient N2(7:0) for Right ADC Biquad A or Coefficient FIR2(7:0) for ADC FIR Filter
84	0000 0000	Coefficient D1(15:8) for Right ADC Biquad A or Coefficient FIR3(15:8) for ADC FIR Filter
85	0000 0000	Coefficient D1(7:0) for Right ADC Biquad A or Coefficient FIR3(7:0) for ADC FIR Filter
86	0000 0000	Coefficient D2(15:8) for Right ADC Biquad A or Coefficient FIR4(15:8) for ADC FIR Filter
87	0000 0000	Coefficient D2(7:0) for Right ADC Biquad A or Coefficient FIR4(7:0) for ADC FIR Filter
88	0000 0000	Coefficient N0(15:8) for Right ADC Biquad B or Coefficient FIR5(15:8) for ADC FIR Filter
89	0000 0000	Coefficient N0(7:0) for Right ADC Biquad B or Coefficient FIR5(7:0) for ADC FIR Filter
90	0000 0000	Coefficient N1(15:8) for Right ADC Biquad B or Coefficient FIR6(15:8) for ADC FIR Filter
91	0000 0000	Coefficient N1(7:0) for Right ADC Biquad B or Coefficient FIR6(7:0) for ADC FIR Filter
92	0000 0000	Coefficient N2(15:8) for Right ADC Biquad B or Coefficient FIR7(15:8) for ADC FIR Filter
93	0000 0000	Coefficient N2(7:0) for Right ADC Biquad B or Coefficient FIR7(7:0) for ADC FIR Filter
94	0000 0000	Coefficient D1(15:8) for Right ADC Biquad B or Coefficient FIR8(15:8) for ADC FIR Filter
95	0000 0000	Coefficient D1(7:0) for Right ADC Biquad B or Coefficient FIR8(7:0) for ADC FIR Filter
96	0000 0000	Coefficient D2(15:8) for Right ADC Biquad B or Coefficient FIR9(15:8) for ADC FIR Filter
97	0000 0000	Coefficient D2(7:0) for Right ADC Biquad B or Coefficient FIR9(7:0) for ADC FIR Filter
98	0000 0000	Coefficient N0(15:8) for Right ADC Biquad C or Coefficient FIR10(15:8) for ADC FIR Filter
99	0000 0000	Coefficient N0(7:0) for Right ADC Biquad C or Coefficient FIR10(7:0) for ADC FIR Filter
100	0000 0000	Coefficient N1(15:8) for Right ADC Biquad C or Coefficient FIR11(15:8) for ADC FIR Filter
101	0000 0000	Coefficient N1(7:0) for Right ADC Biquad C or Coefficient FIR11(7:0) for ADC FIR Filter
102	0000 0000	Coefficient N2(15:8) for Right ADC Biquad C or Coefficient FIR12(15:8) for ADC FIR Filter
103	0000 0000	Coefficient N2(7:0) for Right ADC Biquad C or Coefficient FIR12(7:0) for ADC FIR Filter
104	0000 0000	Coefficient D1(15:8) for Right ADC Biquad C or Coefficient FIR13(15:8) for ADC FIR Filter
105	0000 0000	Coefficient D1(7:0) for Right ADC Biquad C or Coefficient FIR13(7:0) for ADC FIR Filter
106	0000 0000	Coefficient D2(15:8) for Right ADC Biquad C or Coefficient FIR14(15:8) for ADC FIR Filter
107	0000 0000	Coefficient D2(7:0) for Right ADC Biquad C or Coefficient FIR14(7:0) for ADC FIR Filter
108	0000 0000	Coefficient N0(15:8) for Right ADC Biquad D or Coefficient FIR15(15:8) for ADC FIR Filter
109	0000 0000	Coefficient N0(7:0) for Right ADC Biquad D or Coefficient FIR15(7:0) for ADC FIR Filter
110	0000 0000	Coefficient N1(15:8) for Right ADC Biquad D or Coefficient FIR16(15:8) for ADC FIR Filter
111	0000 0000	Coefficient N1(7:0) for Right ADC Biquad D or Coefficient FIR16(7:0) for ADC FIR Filter
112	0000 0000	Coefficient N2(15:8) for Right ADC Biquad D or Coefficient FIR17(15:8) for ADC FIR Filter

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Table 109. Page 4 Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
113	0000 0000	Coefficient N2(7:0) for Right ADC Biquad D or Coefficient FIR17(7:0) for ADC FIR Filter
114	0000 0000	Coefficient D1(15:8) for Right ADC Biquad D or Coefficient FIR18(15:8) for ADC FIR Filter
115	0000 0000	Coefficient D1(7:0) for Right ADC Biquad D or Coefficient FIR18(7:0) for ADC FIR Filter
116	0000 0000	Coefficient D2(15:8) for Right ADC Biquad D or Coefficient FIR19(15:8) for ADC FIR Filter
117	0000 0000	Coefficient D2(7:0) for Right ADC Biquad D or Coefficient FIR19(7:0) for ADC FIR Filter
118	0000 0000	Coefficient N0(15:8) for Right ADC Biquad E or Coefficient FIR20(15:8) for ADC FIR Filter
119	0000 0000	Coefficient N0(7:0) for Right ADC Biquad E or Coefficient FIR20(7:0) for ADC FIR Filter
120	0000 0000	Coefficient N1(15:8) for Right ADC Biquad E or Coefficient FIR21(15:8) for ADC FIR Filter
121	0000 0000	Coefficient N1(7:0) for Right ADC Biquad E or Coefficient FIR21(7:0) for ADC FIR Filter
122	0000 0000	Coefficient N2(15:8) for Right ADC Biquad E or Coefficient FIR22(15:8) for ADC FIR Filter
123	0000 0000	Coefficient N2(7:0) for Right ADC Biquad E or Coefficient FIR22(7:0) for ADC FIR Filter
124	0000 0000	Coefficient D1(15:8) for Right ADC Biquad E or Coefficient FIR23(15:8) for ADC FIR Filter
125	0000 0000	Coefficient D1(7:0) for Right ADC Biquad E or Coefficient FIR23(7:0) for ADC FIR Filter
126	0000 0000	Coefficient D2(15:8) for Right ADC Biquad E or Coefficient FIR24(15:8) for ADC FIR Filter
127	0000 0000	Coefficient D2(7:0) for Right ADC Biquad E or Coefficient FIR24(7:0) for ADC FIR Filter

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 137 shows the required external components and system level connections for proper operation of the device in several popular use cases.

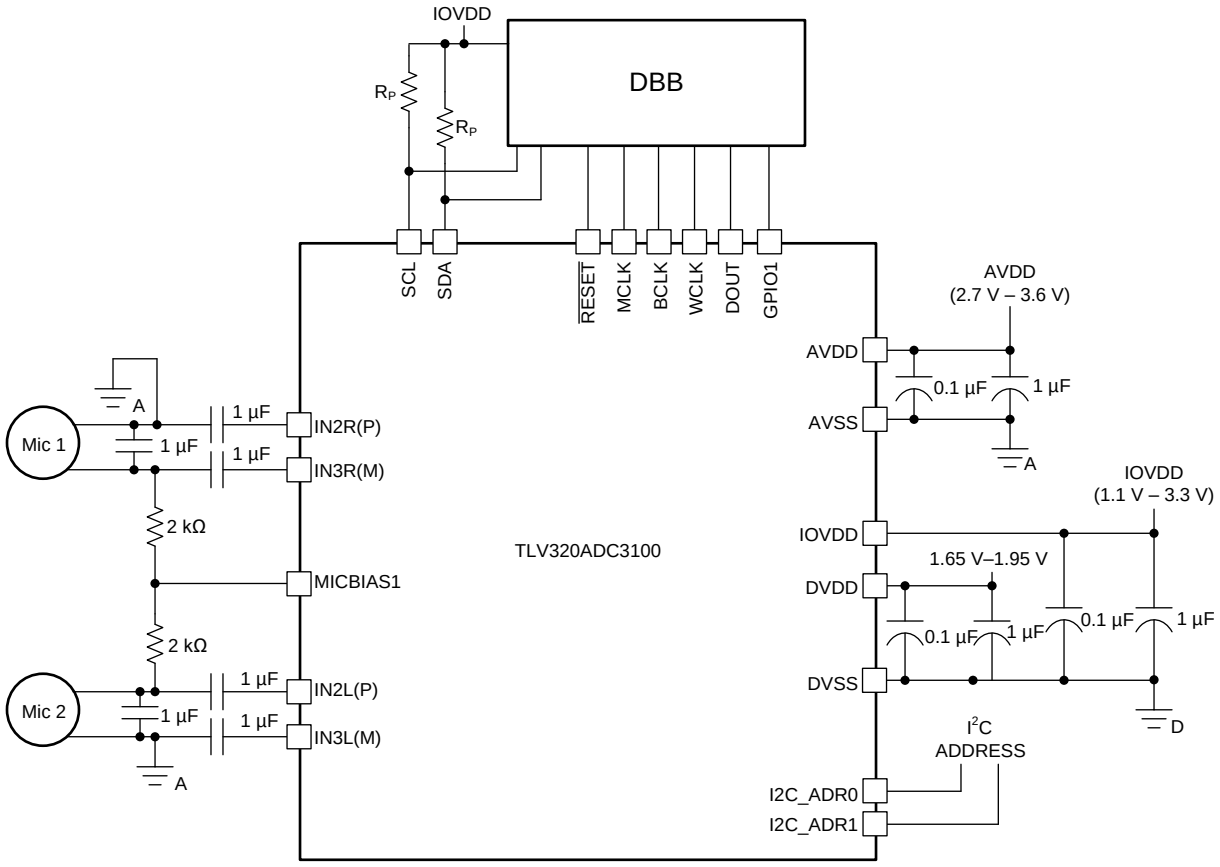


Figure 137. Typical Connections

Each of these configurations can be realized using the evaluation modules (EVMs) for the device. As previously discussed in the *Recording Mode* section, the TLV320ADC3100 is form-factor and software compatible with the TLV320ADC3101. Therefore, both the TLV320ADC3101 and the TLV320ADC3100 use the same EVM, the TLV320ADC3101-K. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

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9.2 Typical Application

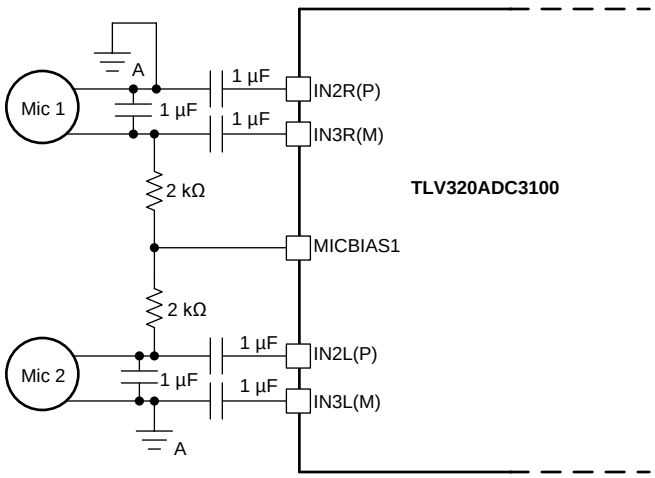


Figure 138. Application With Two Analog Microphones Using a Shared MICBIAS

9.2.1 Design Requirements

Table 110 lists the design parameters for this application.

Table 110. Design Parameters

KEY PARAMETER	SPECIFICATION
AVDD	3.3 V
AVDD supply current	> 6 mA (PLL on, AGC off, digital filter engine off, stereo record, f_S = 48 kHz)
DVDD	1.8 V
DVDD supply current	> 4 mA (PLL on, AGC off, digital filter engine off, stereo record, f_S = 48 kHz)
IOVDD	1.8 V
Maximum MICBIAS current	4 mA (MICBIAS voltage 2.5 V)

9.2.2 Detailed Design Procedure

This section describes the necessary steps to configure the TLV320ADC3100.

9.2.2.1 Step 1

The system clock source (master clock) and the targeted ADC sampling frequency must be identified.

Depending on the targeted performance, the decimation filter type (A, B, or C) and AOSR value can be determined:

- Filter A must be used for 48-kHz high-performance operation; AOSR must be a multiple of 8
- Filter B must be used for up to 96-kHz operations; AOSR must be a multiple of 4
- Filter C must be used for up to 192-kHz operations; AOSR must be a multiple of 2

In all cases, Equation 6 limits the AOSR range:

$$2.8\ \text{MHz} < \text{AOSR} \times \text{ADC_fs} < 6.2\ \text{MHz} \quad (6)$$

Based on the identified filter type and the required signal-processing capabilities, the appropriate processing block can be determined from the list of available processing blocks (PRB_R1 to PRB_R18).

Based on the available master clock, the chosen AOSR and the targeted sampling rate, the clock divider values NADC and MADC can be determined. If necessary, the internal PLL can add a large degree of flexibility.

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Equation 7 describes that, in summary, ADC_CLKIN (derived directly from the system clock source or from the internal PLL) divided by MADC, NADC, and AOSR must be equal to the ADC sampling rate ADC_fs. The ADC_CLKIN clock signal is shared with the DAC clock-generation block.

$$ADC_CLKIN = NADC \times MADC \times AOSR \times ADC_fs \quad (7)$$

To a large degree, NADC and MADC can be chosen independently in the range of 1 to 128. In general, as long as Equation 8 is met, NADC must be as large as possible:

$$MADC \times AOSR \geq INSTR_CTR \quad (8)$$

RC is a function of the chosen processing block and is listed in Table 6.

The common-mode voltage setting of the device is determined by the available analog power supply.

At this point, the PRB_Rx, AOSR, NADC, MADC, and input and output common-mode values device-specific parameters are known. If the PLL is used, the PLL parameters P, J, D, and R are determined as well.

9.2.2.2 Step 2

Setting up the device via register programming:

The following list gives a sequence of items that must be executed in the time between powering the device up and reading data from the device:

1. Define starting point:
   a. Power up applicable external hardware power supplies
   b. Set register page to 0
   c. Initiate SW reset
2. Program clock settings:
   a. Program PLL clock dividers P, J, D, and R (if PLL is used)
   b. Power up PLL (if PLL is used)
   c. Program and power up NADC
   d. Program and power up MADC
   e. Program OSR value
   f. Program I2S word length if required (for example, 20 bits)
   g. Program the processing block to be used
3. Program analog blocks:
   a. Set register page to 1
   b. Program MICBIAS, if applicable
   c. Program MICPGA
   d. Program routing of inputs and common mode to ADC input
   e. Unmute analog PGAs and set analog gain
4. Program ADC:
   a. Set register page to 0
   b. Power up ADC channel
   c. Unmute digital volume control and set gain

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9.2.2.3 Example Register Setup to Record Analog Data Through ADC to Digital Out

A typical EVM I^{2}C register control script follows to show how to set up the TLV320ADC3100 in record mode with f_S = 44.1 kHz and MCLK = 11.2896 MHz.

```
# Key: w 30 XX YY ==> write to I2C address 0x30, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# ADC3101EVM Key Jumper Settings and Audio Connections:
# 1. Remove Jumpers W12 and W13
# 2. Insert Jumpers W4 and W5
# 3. Insert a 3.5mm stereo audio plug into J9 for
#    single-ended input IN1L(P) - left channel and
#    single-ended input IN1R(M) - right channel
#####################################################################
# 1. Define starting point:
#   (a) Power up appicable external hardware power supplies
#   (b) Set register page to 0
#
w 30 00 00
#   (c) Initiate SW Reset
#
w 30 01 01
#
# 2. Program Clock Settings
#   (a) Program PLL clock dividers P,J,D,R (if PLL is necessary)
#
# In EVM, the ADC3001 receives: MCLK = 11.2896 MHz,
# BCLK = 2.8224 MHz, WCLK = 44.1 kHz
#
# Sinve the sample rate is a multiple of the input MCLK then
# no PLL is needed thereby saving power. Use Default (Reset) Settings:
# ADC_CLKIN = MCLK, P=1, R=1, J=4, D=0000
w 30 04 00
w 30 05 11
w 30 06 04
w 30 07 00
w 30 08 00
#
#   (b) Power up PLL (if PLL is necessary) - Not Used in this Example
w 30 05 11
#   (c) Program and power up NADC
#
# NADC = 1, divider powered on
w 30 12 81
#
#   (d) Program and power up MADC
#
# MADC = 2, divider powered on
w 30 13 82
#
#   (e) Program OSR value
#
# AOSR = 128 (default)
w 30 14 80
#
#   (f) Program I2S word length as required (16, 20, 24, 32 bits)
#
# mode is i2s, wordlength is 16, slave mode (default)
w 30 1B 00
#
#   (g) Program the processing block to be used
#
# PRB_P1
w 30 3d 01
#
# 3. Program Analog Blocks
#   (a) Set register Page to 1
#
```


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```
w 30 00 01
#
#   (b) Program MICBIAS if applicable
#
# Not used (default)
w 30 33 00
#
#   (c) Program MICPGA
#
# Left Analog PGA Seeting = 0dB
w 30 3b 00
#
# Right Analog PGA Seeting = 0dB
w 30 3c 00
#
#   (d) Routing of inputs/common mode to ADC input
#   (e) Unmute analog PGAs and set analog gain
#
# Left ADC Input selection for Left PGA = IN1L(P) as Single-Ended
w 30 34 fc
#
# Right ADC Input selection for Right PGA = IN1R(M) as Single-Ended
w 30 37 fc
#
# 4. Program ADC
#
#   (a) Set register Page to 0
#
w 30 00 00
#
#   (b) Power up ADC channel
#
# Power-up Left ADC and Right ADC
w 30 51 c2
#
#   (c) Unmute digital volume control and set gain = 0 dB
#
# UNMUTE
w 30 52 00
#
```

9.2.2.4 MICBIAS

The TLV320ADC3100 has a built-in bias voltage output for the biasing of microphones. No intentional capacitors must be connected directly to the MICBIAS output for filtering.

9.2.2.5 Decoupling Capacitors

The TLV320ADC3100 requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good ceramic capacitor, typically 0.1 µF, placed as close as possible to the device AVDD, IOVDD, and DVDD lead works best. Placing this decoupling capacitor close to the TLV320ADC3100 is important for the performance of the converter. For filtering lower-frequency noise signals, a 1-µF or greater capacitor placed near the device also helps.

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9.2.3 Application Curves

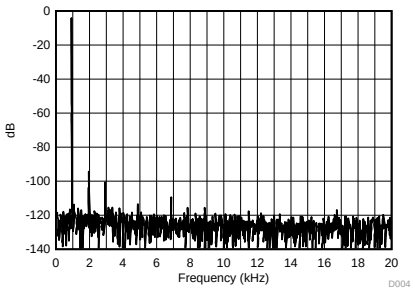


Figure 139. Line Input to ADC FFT Plot

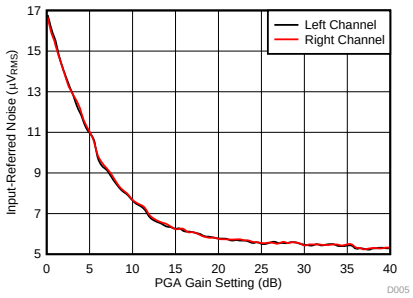


Figure 140. Input-Referred Noise vs PGA Gain

10 Power Supply Recommendations

The power supplies are designed to operate from 2.7 V to 3.6 V for AVDD, from 1.65 V to 1.95 V for DVDD and from 1.1 V to 3.6 V for IOVDD. Any value out of these ranges must be avoided to ensure the correct behavior of the device. The power supplies must be well regulated. Placing a decoupling capacitor close to the TLV320ADC3100 improves the performance of the device. A low equivalent-series-resistance (ESR) ceramic capacitor with a value of 0.1 µF is a typical choice. If the TLV320ADC3100 is used in highly noise-sensitive circuits, TI recommends adding a small LC filter on the VDD connections.

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11 Layout

11.1 Layout Guidelines

Each system design and PCB layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the TLV320ADC3100 performance:

The decoupling capacitors for the power supplies must be placed close to the device terminals. Figure 137 shows the recommended decoupling capacitors for the TLV320ADC3100.

Route analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to avoid undesirable crosstalk.

Analog and digital grounds must be separated to prevent possible digital noise from affecting the analog performance of the board.

11.2 Layout Example

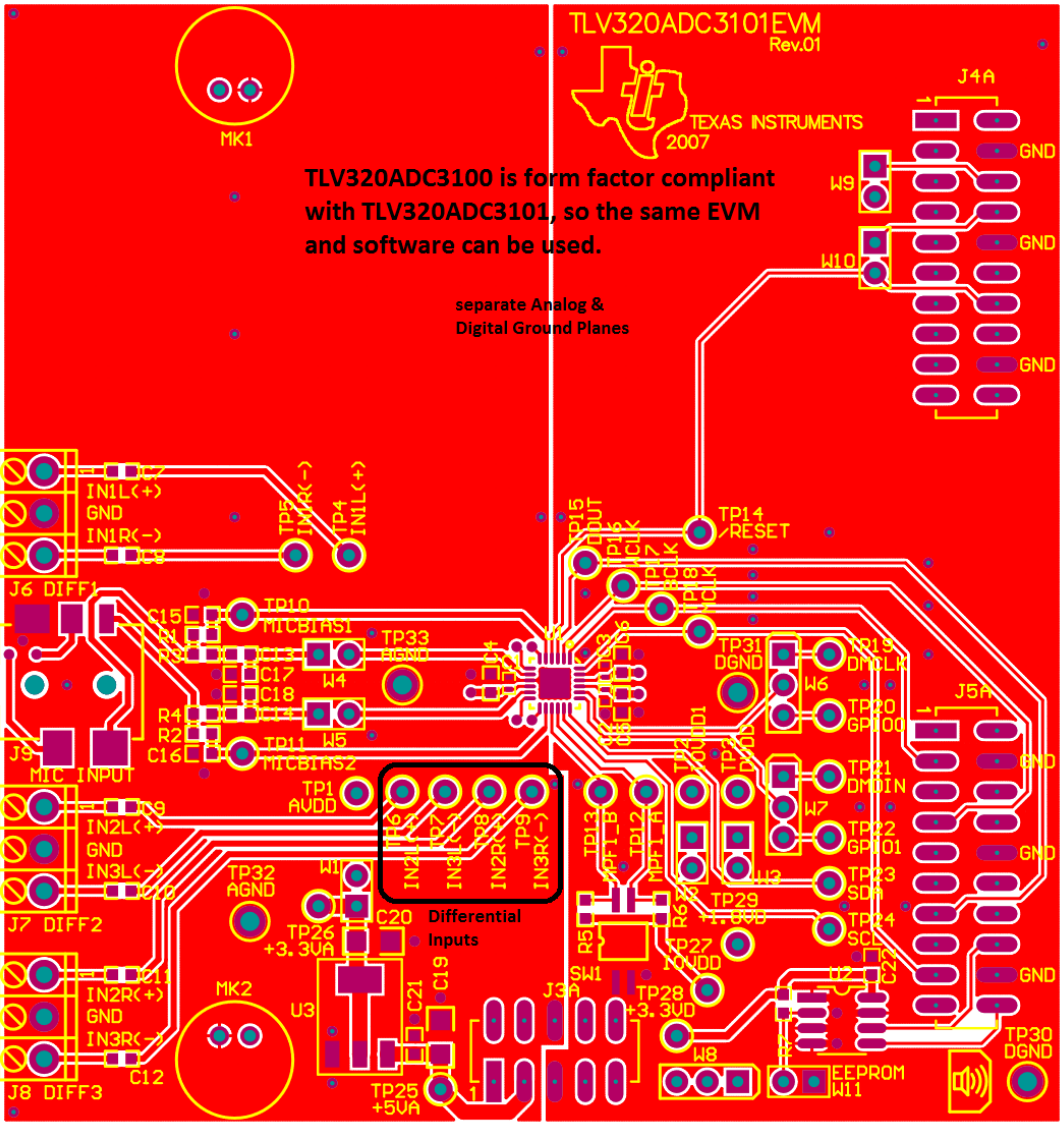


Figure 141. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *TLV320ADC3101 Low-Power Stereo ADC With Embedded miniDSP for Wireless Handsets and Portable Audio*
- *TLV320ADC3001 Low-Power Stereo ADC With Embedded miniDSP for Wireless Handsets and Portable Audio*
- *TLV320ADC3101EVM-K User's Guide*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on www.ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
6PADC3100IRGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADC 3100
6PADC3100IRGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADC 3100
TLV320ADC3100IRGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	ADC 3100
TLV320ADC3100IRGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	ADC 3100
TLV320ADC3100IRGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	ADC 3100
TLV320ADC3100IRGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	ADC 3100

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

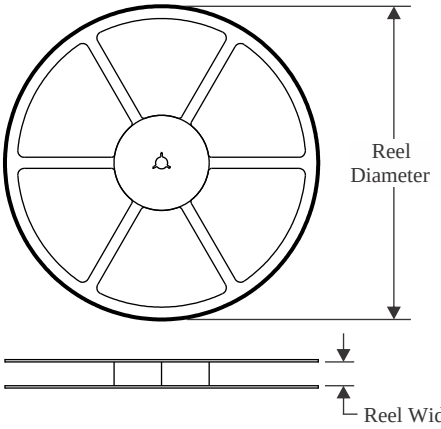
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

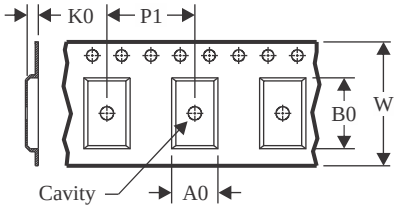
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

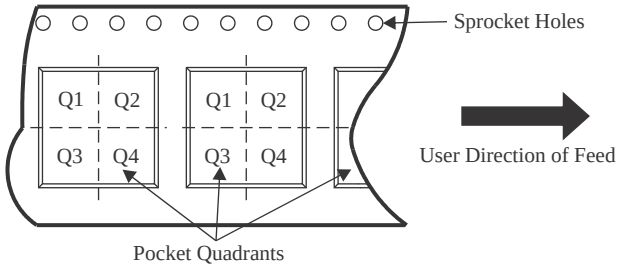


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

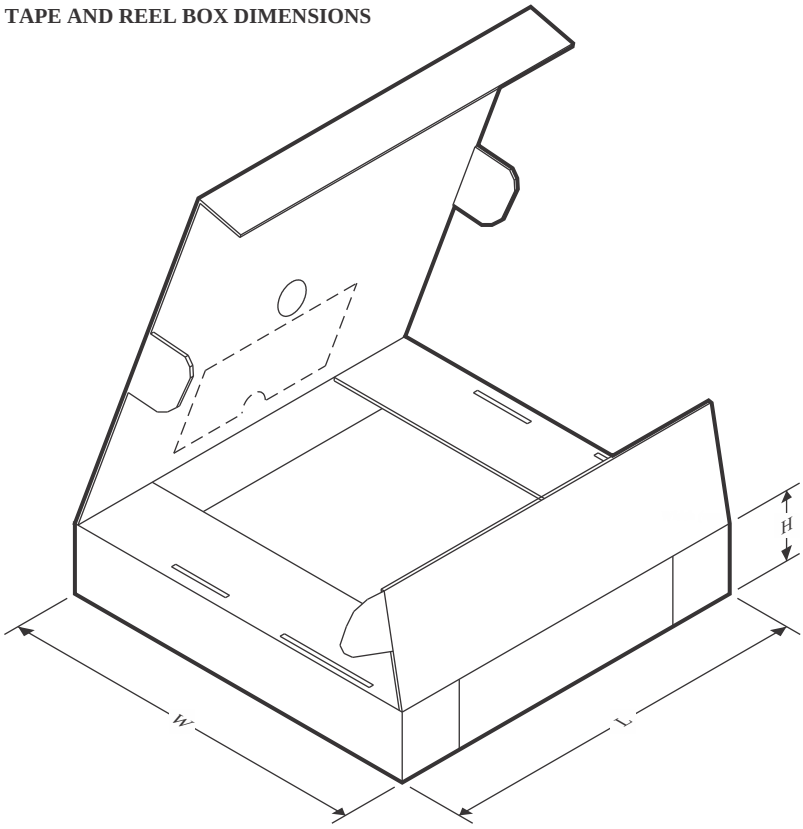
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
6PADC3100IRGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320ADC3100IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLV320ADC3100IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



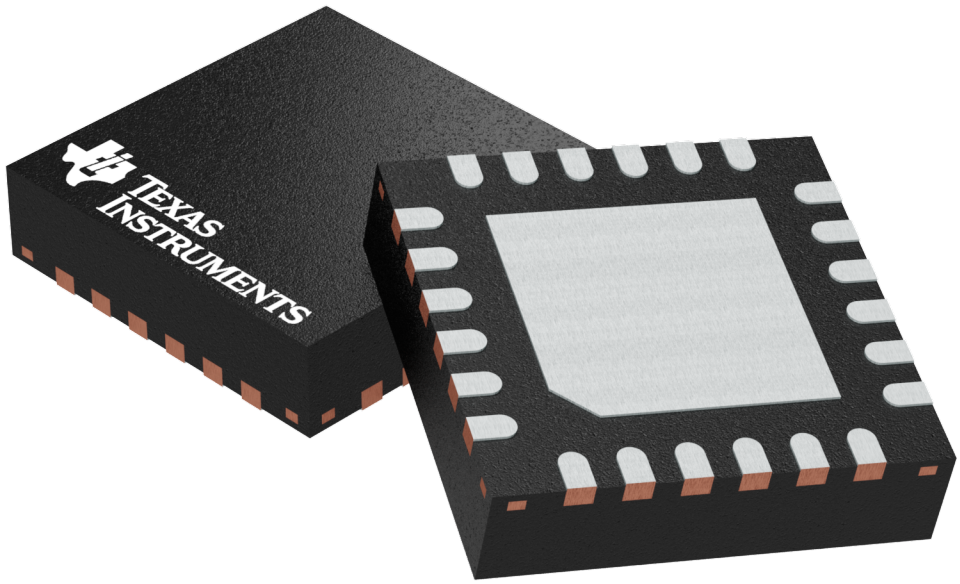
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
6PADC3100IRGERG4	VQFN	RGE	24	3000	367.0	367.0	35.0
TLV320ADC3100IRGER	VQFN	RGE	24	3000	360.0	360.0	36.0
TLV320ADC3100IRGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

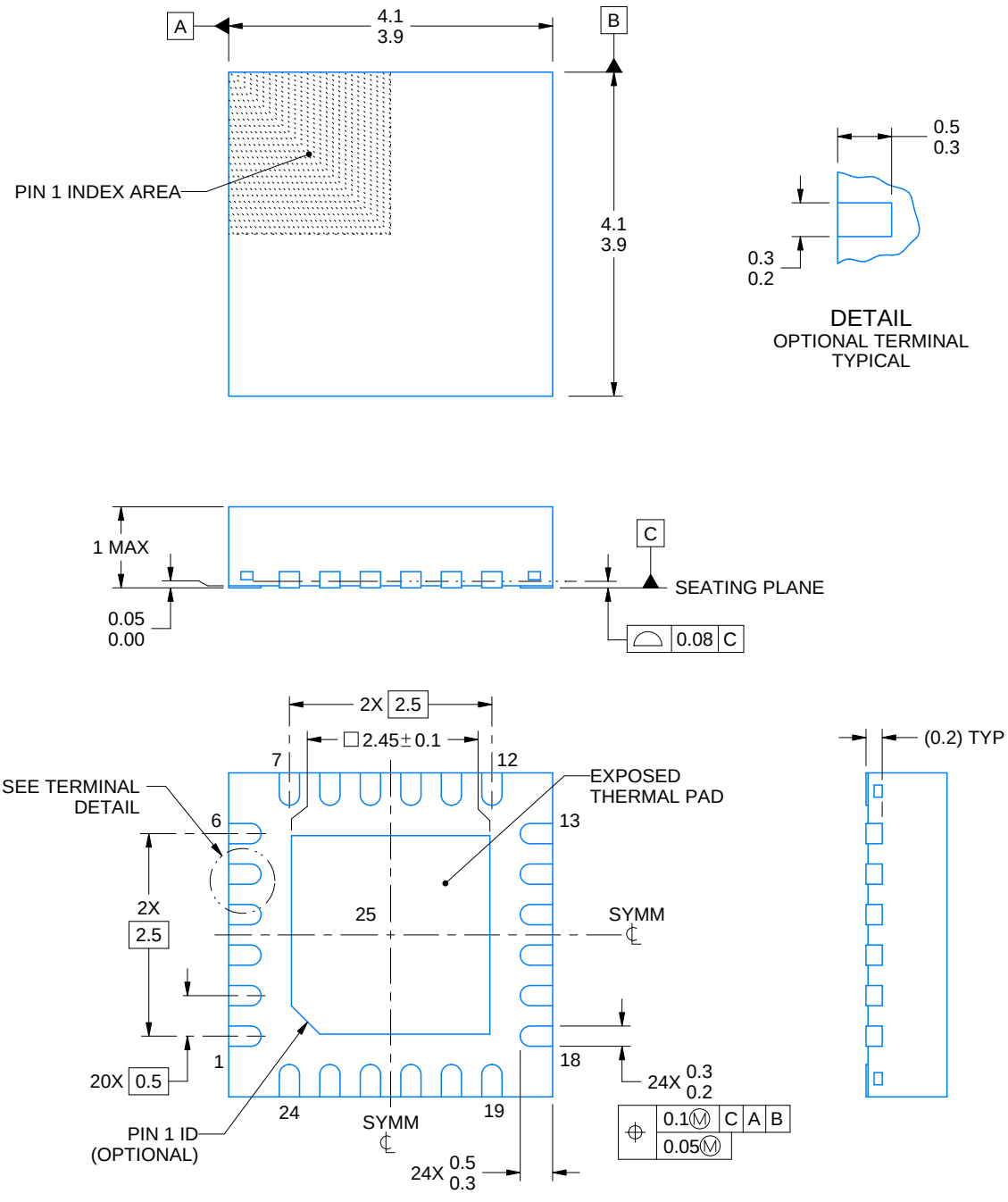
4204104/H

PACKAGE OUTLINE

RGE0024B

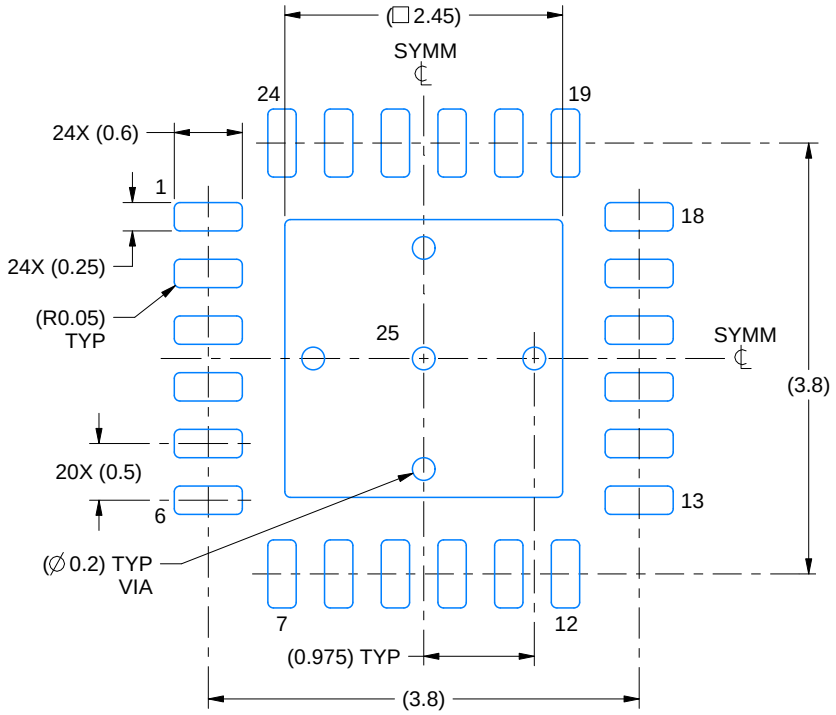
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

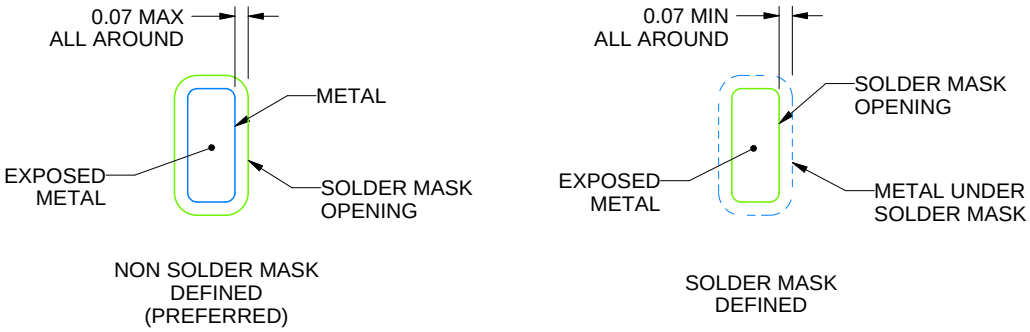


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

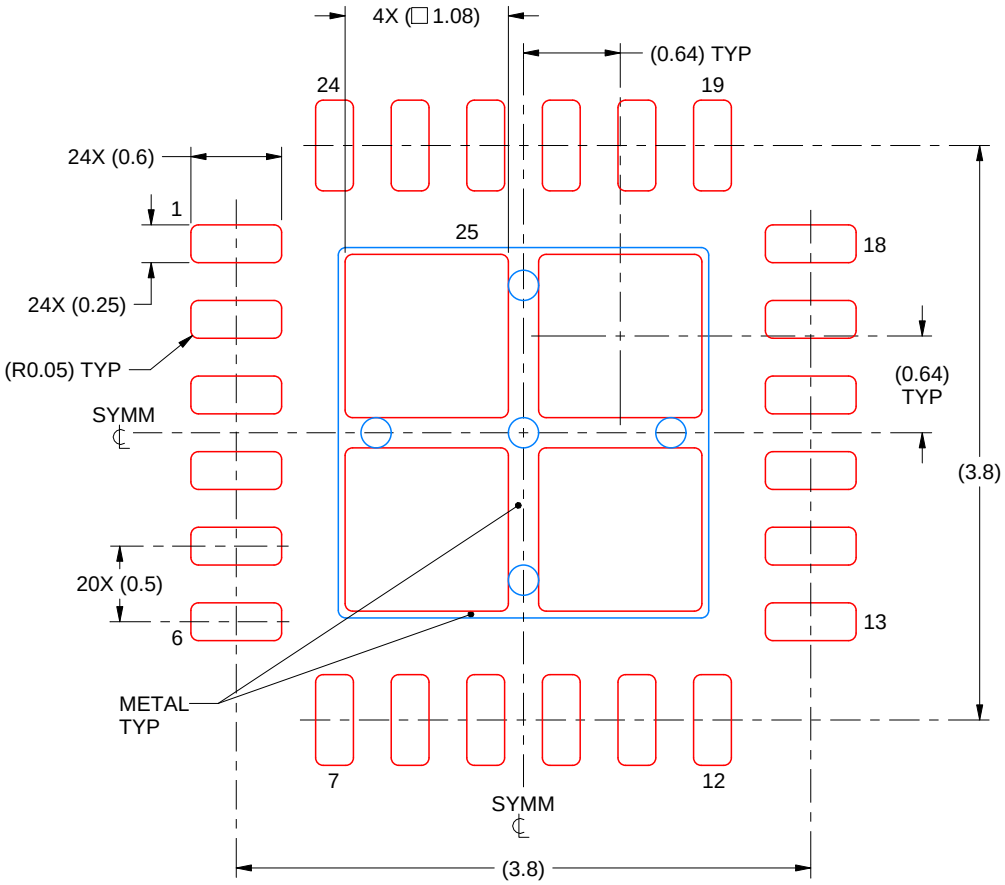


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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