# TLV61047-Q1 Automotive 20$V_{IN}$, 28$V_{OUT}$, 2.2A Non-synchronous Boost Converter

## 1 Features

- AEC-Q100 qualified:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage range: 1.8V to 20V
- Output voltage range: 4.5V to 28V
- Integrated low-side FET: 200mΩ
- High efficiency
  - Up to 89.7% efficiency at $V_{IN}$ = 5V to $V_{OUT}$ = 12V, and $I_{OUT}$ = 0.25A
  - Up to 90.4% efficiency at $V_{IN}$ = 12V to $V_{OUT}$ = 28V, and $I_{OUT}$ = 0.35A
- Peak switch current limit: 2.2A
- Switching frequency: 2.4MHz
- Reference voltage accuracy: ±2.0%
- Typical quiescent current: 25µA
- Typical shutdown current: 0.4µA
- PFM operation mode at light load
- Internal compensation
- Internal soft start time: 2.5ms
- Cycle-by-cycle current limit
- Thermal shutdown protection
- SOT-23-5 DDC package

## 2 Applications

- LED power supply
- Digital still camera
- GPS devices
- Mobile phone
- OLED panel power supply
- USB-powered devices

## 3 Description

The TLV61047-Q1 is a high-voltage, non-synchronous boost converter that integrates a 200mΩ low side power switch to provide an easy use and small size power design. The TLV61047-Q1 has a wide input voltage range from 1.8V to 20V and output voltage covers up to 28V with 2.2A switch current capability.

The TLV61047-Q1 uses adaptive constant off-time peak current control topology to regulate the output voltage. At heavy to light load condition, the TLV61047-Q1 works in pulse width modulation (PWM) mode until trigger the minimum peak current (typical 300mA). At lighter load condition , the devices work in pulse frequency modulation (PFM) mode to improve the efficiency and ripple performance.

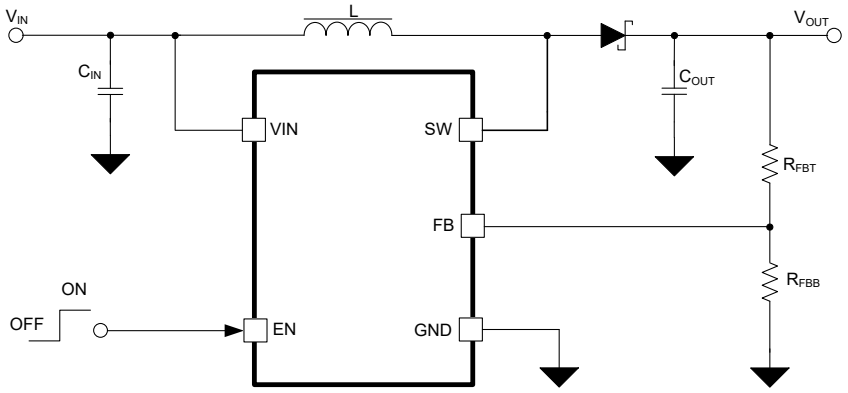
The quasi-constant switching frequency is internally set to 2.4MHz, allowing the use of extremely small surface mount inductor and capacitors. The TLV61047-Q1 has built in 2.5ms soft start to minimize the inrush current during start-up. Additional features include internal compensation, cycle-by-cycle current limit, and thermal shutdown.

The TLV61047-Q1 is available in an SOT-23-5 DDC package.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TLV61047-Q1 | DDC (SOT-23-THN, 5) | 2.9mm × 2.8mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Circuit**

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# 4 Pin Configuration and Functions

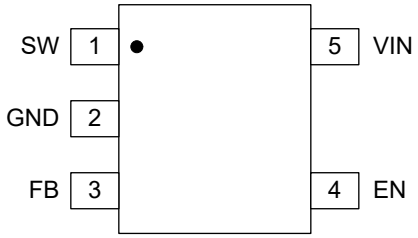



**Figure 4-1. DDC Package 5-Pin SOT-23-THN (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | DDC NO. | | |
| SW | 1 | PWR | The switch pin of the converter. This pin is connected to the drain of the internal power MOSFET. |
| GND | 2 | G | Ground |
| FB | 3 | I | Voltage feedback of output voltage. Connected to the center tap of a resistor divider to program the output voltage. |
| EN | 4 | I | Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns the device into shutdown mode. |
| VIN | 5 | I | IC power supply input |

(1) I = Input, G = Ground, PWR = Power

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range at terminals (2) | VIN,EN | –0.3 | 20.5 | V |
| | SW | –0.3 | 32 | V |
| | FB | –0.3 | 6 | V |
| Operating junction temperature range, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011, all pins | ±750 | V |

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 1.8 | | 20 | V |
| $V_{OUT}$ | Output voltage range | 4.5 | | 28 | V |
| L | Inductance range | 1 | 2.2 | 10 | µH |
| $C_{IN}$ | Effective input capacitance range | 1 | 10 | | µF |
| $C_{OUT}$ | Effective output capacitance range | 1 | 10 | | µF |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TLV61047-Q1 DDC (SOT23) 5 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 145.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 77.6 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 56.5 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 28.5 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 54.9 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | NA | |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

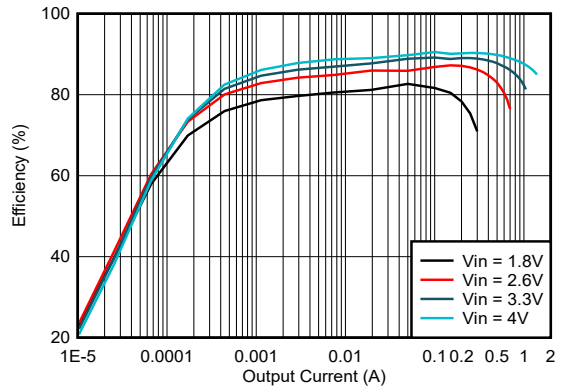
## 5.5 Electrical Characteristics

$T_J$ = –40°C to 150°C, $V_{IN}$ = 5.0V. Typical values are at $T_J$ = 25°C, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | | 1.8 | | 20 | V |
| $V_{IN\_UVLO}$ | Undervoltage lockout threshold | $V_{IN\_UVLO}$ rising | | 1.7 | 1.79 | V |
| | | $V_{IN\_UVLO}$ falling | | 1.55 | 1.64 | |
| $V_{IN\_HYS}$ | $V_{IN\_UVLO}$ hysteresis | | | 150 | | mV |
| $I_{Q\_VIN}$ | Quiescent current into VIN pin | IC enabled, no load, no switching ,$V_{IN}$ = 1.8V to 20V, FB = 1.4V, $T_J$ = –40°C to 125°C | | 25 | 50 | µA |
| $I_{SD}$ | Shutdown current into VIN pin | IC disabled, $V_{IN}$ = 1.8V to 20V, $T_J$ = –40°C to 125°C | | 0.4 | 2.1 | µA |
| $I_{FB\_LKG}$ | Leakage current into FB pin | $T_J$ = –40°C to 125°C | | | 50 | nA |
| $I_{SW\_LKG}$ | Leakage current into SW pin | IC disabled, SW = 28V, $T_J$ = –40°C to 125°C | | | 500 | nA |
| **OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage range | | 4.5 | | 28 | V |
| $V_{REF}$ | Reference Voltage at FB pin | PWM and PFM mode, $T_J$ = –40°C to 125°C | 1.209 | 1.233 | 1.258 | V |
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | Low-side MOSFET on resistance | $V_{IN}$ = 5V, $V_{OUT}$ = 12V | | 200 | | mΩ |
| $F_{SW}$ | Switching frequency | $V_{IN}$ = 5V, $V_{OUT}$ = 12V | | 2.4 | | MHz |
| $t_{OFF\_min}$ | Minimum off time | | | 75 | 150 | ns |
| $t_{ON\_min}$ | Minimum on time | | | 45 | 150 | ns |
| $I_{LIM\_SW}$ | Peak switch current limit | $V_{IN}$ = 5V | 1.9 | 2.2 | 2.5 | A |
| $t_{STARTUP}$ | Soft start-up time | Internal SS ramp time, from 0V to $V_{REF}$ | | 2.5 | | ms |
| **LOGIC INTERFACE** | | | | | | |
| $V_{EN\_H}$ | EN Logic high threshold | | | | 1.2 | V |
| $V_{EN\_L}$ | EN Logic low threshold | | 0.4 | | | V |
| $R_{EN}$ | EN pulldown resistor | | | 1 | | MΩ |
| **PROTECTION** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold | $T_J$ rising | | 170 | | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | $T_J$ falling below $T_{SD}$ | | 20 | | °C |

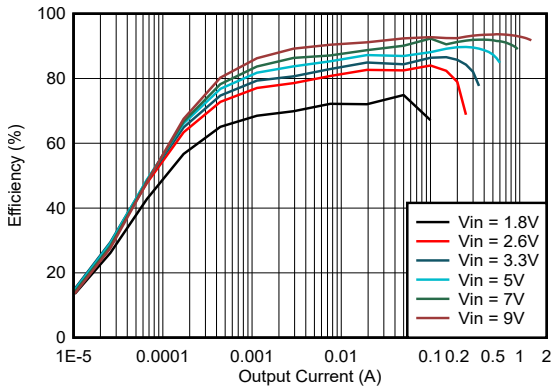
## 5.6 Typical Characteristics

TLV61047-Q1, switching frequency = 2.4MHz (typical), $T_A$ = 25°C, unless otherwise noted



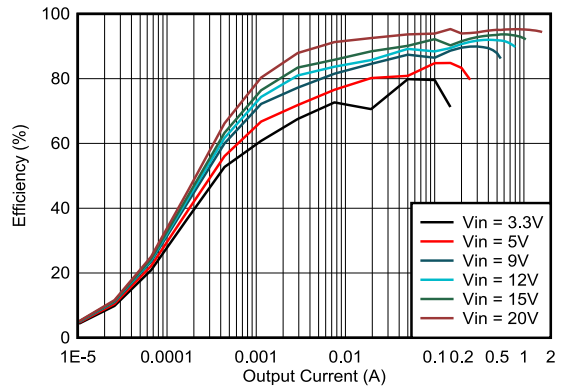

$V_{OUT}$ = 5V L = 1µH

**Figure 5-1. Efficiency vs Output Current, $V_{OUT}$ = 5V**



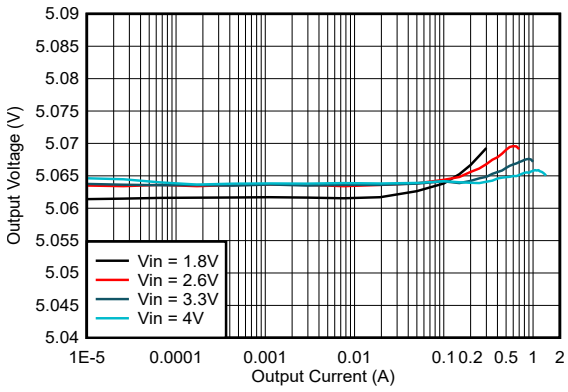

$V_{OUT}$ = 12V L = 2.2µH

**Figure 5-2. Efficiency vs Output Current, $V_{OUT}$ = 12V**



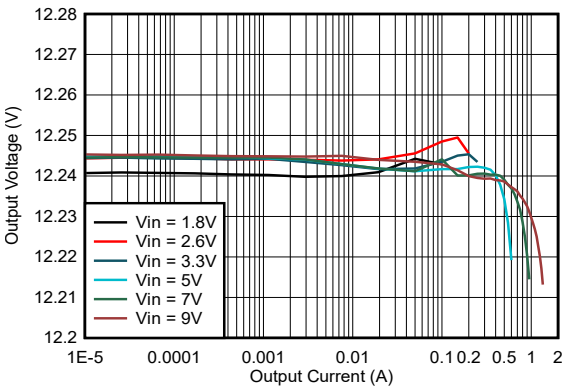

$V_{OUT}$ = 24V L = 4.7µH

**Figure 5-3. Efficiency vs Output Current, $V_{OUT}$ = 24V**



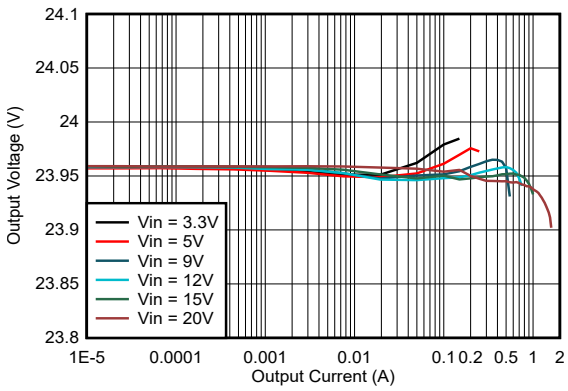

$V_{OUT}$ = 5V L = 1µH

**Figure 5-4. Load regulation, $V_{OUT}$ = 5V**




$V_{OUT}$ = 12V L = 2.2µH

**Figure 5-5. Load regulation, $V_{OUT}$ = 12V**

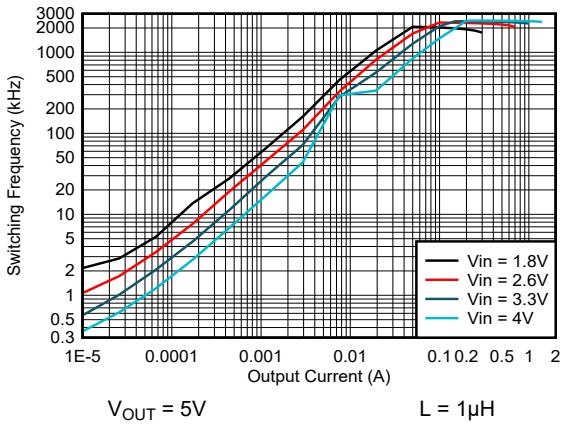



$V_{OUT}$ = 24V L = 4.7µH

**Figure 5-6. Load regulation, $V_{OUT}$ = 24V**

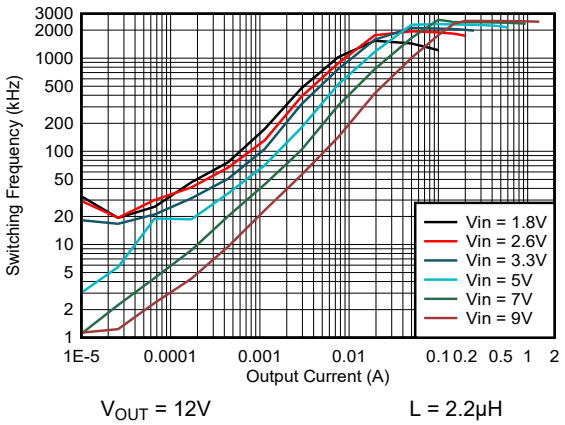
## 5.6 Typical Characteristics (continued)

TLV61047-Q1, switching frequency = 2.4MHz (typical), $T_A$ = 25°C, unless otherwise noted



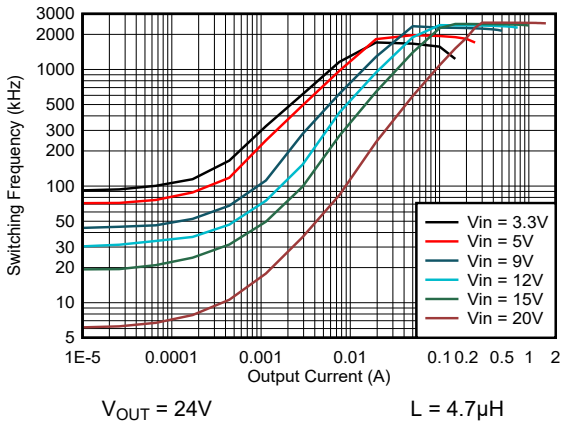

$V_{OUT}$ = 5V L = 1µH

**Figure 5-7. Frequency vs Output Current, $V_{OUT}$ = 5V**




$V_{OUT}$ = 12V L = 2.2µH

**Figure 5-8. Frequency vs Output Current, $V_{OUT}$ = 12V**




$V_{OUT}$ = 24V L = 4.7µH

**Figure 5-9. Frequency vs Output Current, $V_{OUT}$ = 24V**

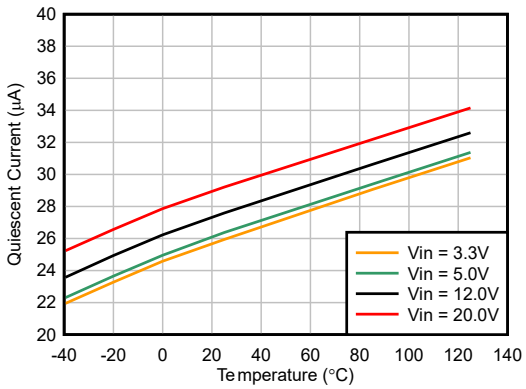



**Figure 5-10. Quiescent Current vs Temperature**

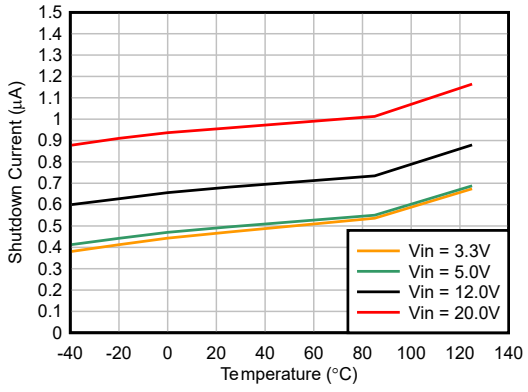



**Figure 5-11. Shutdown Current vs Temperature**

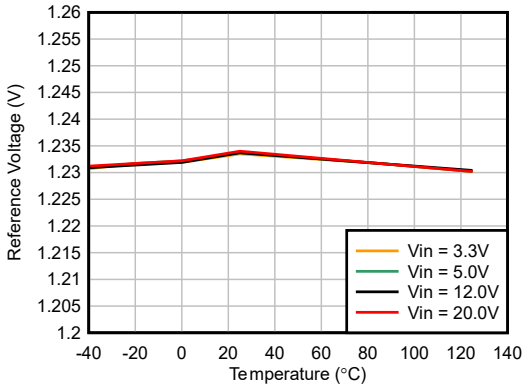



**Figure 5-12. Reference Voltage vs Temperature**

## 5.6 Typical Characteristics (continued)

TLV61047-Q1, switching frequency = 2.4MHz (typical), $T_A$ = 25°C, unless otherwise noted

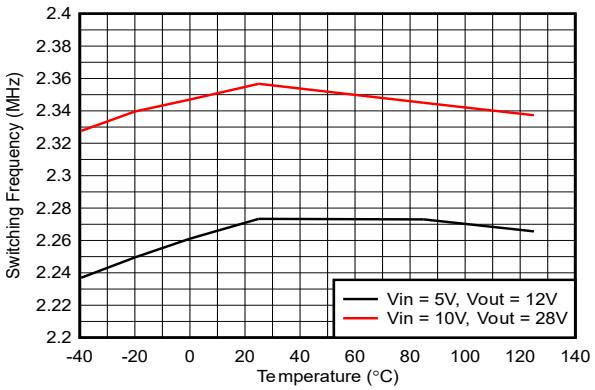



**Figure 5-13. Switching Frequency vs Temperature**

# 6 Detailed Description

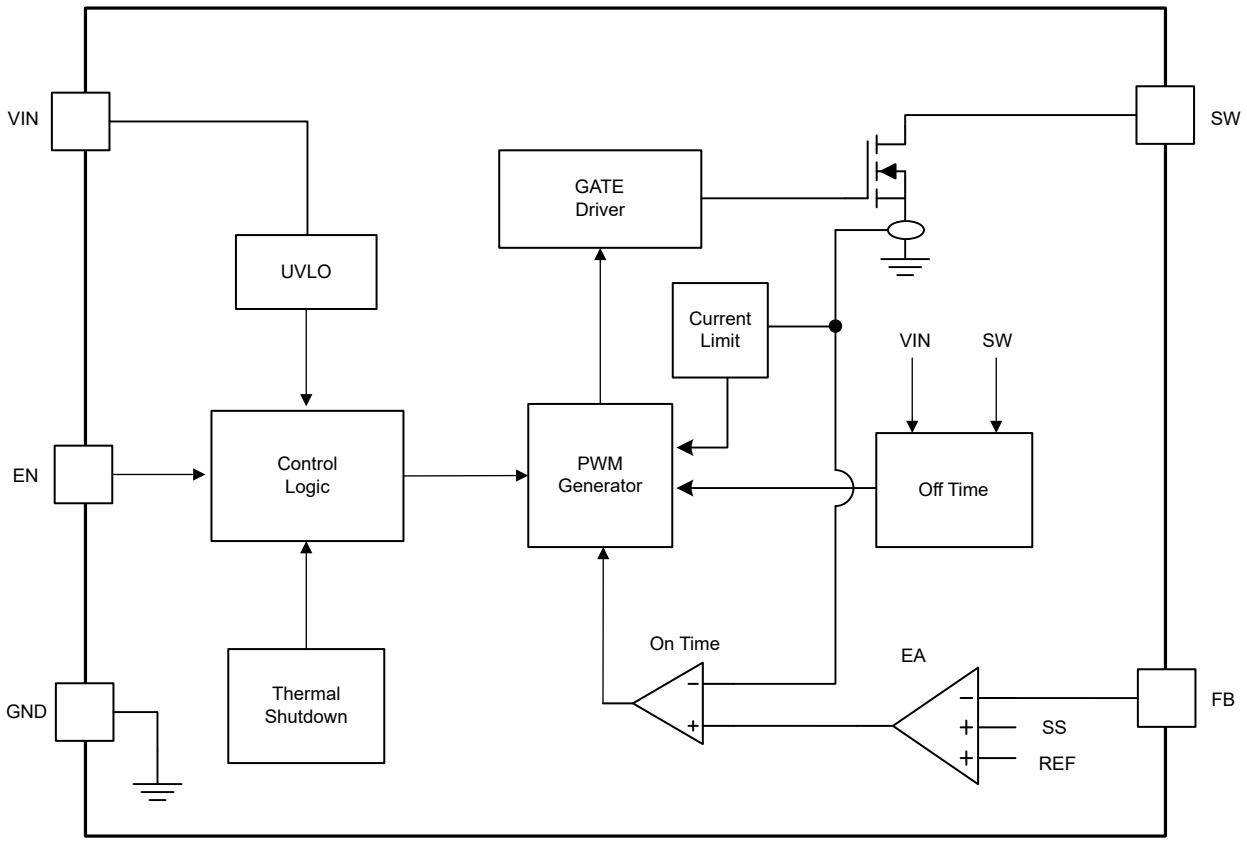
## 6.1 Overview

The TLV61047-Q1 is a non-synchronous boost converter that integrates a 200mΩ low side power switch to provide a easy use and small size power design. The TLV61047-Q1 has a wide input voltage range from 1.8V to 20V and output voltage covers up to 28V with 2.2A switch current capability.

The TLV61047-Q1 uses adaptive constant off-time peak current control topology to regulate the output voltage. At heavy to light load condition, the TLV61047-Q1 works in pulse width modulation (PWM) mode until trigger minimum peak current(typical 300mA). In PWM mode, the quasi-constant switching frequency is internally set to 2.4MHz. At lighter load condition, the devices work in pulse frequency modulation (PFM) mode to improve the efficiency. In PFM mode, the switching frequency decreases lower than 2.4MHz.

The TLV61047-Q1 have built in 2.5ms soft start to minimize the inrush current during start-up. Additional features include internal compensation, cycle-by-cycle current limit, and thermal shutdown.

## 6.2 Functional Block Diagram



## 6.3 Feature Description

### 6.3.1 Undervoltage Lockout

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO falling threshold of 1.6V. A hysteresis of 100mV is added so that the device cannot be enabled again until the input voltage goes up to typical UVLO rising threshold of 1.7V. This function is implemented to prevent malfunctioning of the device when the input voltage is between 1.6V and 1.7V.

### 6.3.2 Enable and Disable

When the input voltage is above typical UVLO rising threshold of 1.7V and the EN pin is pulled high, the TLV61047-Q1 is enabled. When the EN pin is pulled low, the TLV61047-Q1 stops the PWM switch and turns off the low side switch. The EN pin has an internal pulldown resistance of 1MΩ. The device is disabled when the EN pin is floating. In shutdown mode, less than 0.4μA (typical) input current is consumed.

### 6.3.3 Soft Start

The soft-start feature helps the regulator to gradually reach the steady state operating point, therefore reducing start-up stresses and surge. When the input voltage is applied, the output capacitor is charged to VIN through the inductor and high side rectifier diode. After reaching the 1.7V (typical) UVLO rising threshold and EN logic high, the internal soft-start control circuit initiates to ramp the reference voltage with slew rate from 0V to 1.233V within 2.5ms (typical).

### 6.3.4 Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to the excessive heat and power dissipation. Typically, the thermal shutdown occurs at the junction temperature exceeding 170°C (typical). When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 150°C (typical).

## 6.4 Device Functional Modes

The TLV61047-Q1 operates at a quasi-constant frequency pulse width modulation (PWM) under heavy to light load conditions. As the load current decreases, the output of the internal error amplifier also decreases to lower the inductor peak current and delivers less power. The PWM mode can be divided into CCM-PWM mode and DCM-PWM mode based on the load conditions.

- The device operates in CCM-PWM mode with a heavy to moderate load. During this phase, the inductor current valley is always above zero.
- The device operates in DCM-PWM mode as the load continues to decrease from moderate to light. As the name DCM (Discontinuous Current Mode) suggests, an obvious characteristic of this mode is that the inductor current remains at zero for one period in each cycle. During this phase, the inductor peak current can still be reduced by the output of the internal error amplifier to maintain the balance between input and output power. This action allows an excellent off-time of the low-side FET to be worked out internally to keep the switching frequency quasi-constant without pulse skipping. This phase ends when the inductor peak current decreases to $I_{CALMP\_LOW}$, which is typically 300mA.

After the peak inductor current reaches the $I_{CLAMP\_LOW}$ and the load decreases to light or even no load, the peak inductor current cannot be smaller. To balance the input and output energy, the low-side FET is turned off for a prolonged period. The duration of the "zero inductor current" is much longer than in the DCM-PWM phase. This phase is called DCM-PFM mode for features of discontinuous inductor current and significantly reduced frequency. Figure 6-1 shows the three phases of CCM-PWM, DCM-PWM and DCM-PFM.

In work conditions where the $V_{IN}$ is very close to the $V_{OUT}$, the $V_{IN}$ $V_{OUT}$ ratio decided turn on time can be less than the minimum turn on time, the device also enters into the DCM-PFM mode.

At light load, when $T_{ON}$ min is triggered, the device also enters DCM-PFM mode even if the inductor peak current is greater than $I_{CALMP\_LOW}$. When the low-side FET is turned on, the low-side FET remains on for a minimum time, called $T_{ON}$ min. The inductor is energized for at least $T_{ON}$ minimum time when the low-side FET is on. If the $T_{ON}$ minimum is greater than the ideal time required to maintain the quasi-constant frequency,

the device has to extend the off time to balance the input and output energy. So the device is in DCM-PFM mode. Under normal work conditions, the $I_{CALMP\_LOW}$ triggered DCM-PFM mode is much more common than that triggered by $T_{ON}$ min, unless an inductor with extremely small inductance is used.

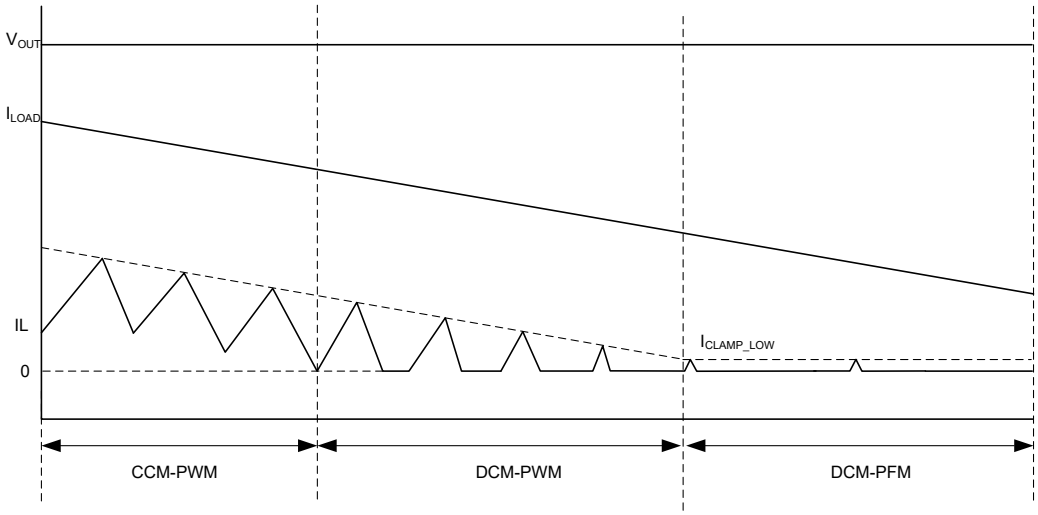



**Figure 6-1. TLV61047-Q1 Functional Modes**

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

TLV61047-Q1 is a boost DC/DC converter integrating a power switch and loop compensation circuits. The device has input range from 1.8V to 20V, with output voltage covers up to 28V. The TLV61047-Q1 adopts the current-mode control with adaptive constant off-time. The switching frequency is quasi-constant and internally set to 2.4MHz allowing the use of extremely small surface mount inductor and capacitors. The following design procedure can be used to select component values for the TLV61047-Q1.

## 7.2 Typical Applications

### *7.2.1 12V Output Boost Converter*

In this design example, TLV61047-Q1 $V_{OUT}$ is configured as 12V with a input source from 1.8V to 9V.

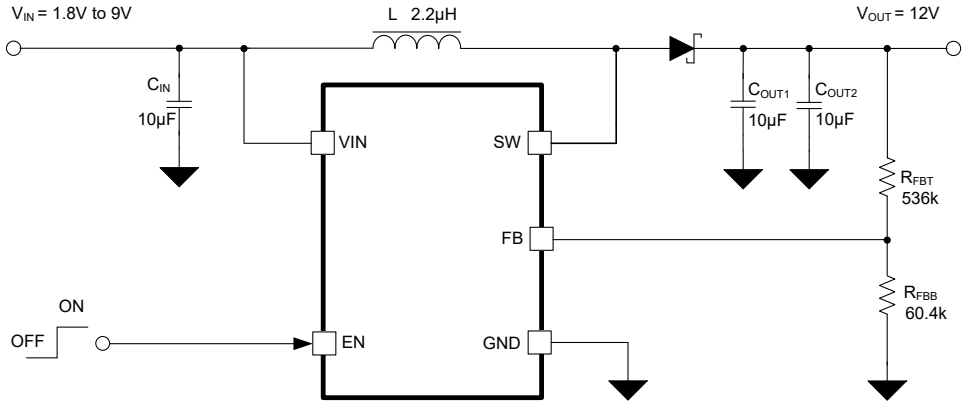



**Figure 7-1. Typical 12V Application**

#### 7.2.1.1 Design Requirements

For this design example, Table 7-1 shows the parameters:

**Table 7-1. Design Requirements**

| PARAMETERS | VALUE |
|---|---|
| Input voltage | 1.8V to 9V |
| Output voltage | 12V |
| Frequency | 2.4MHz |
| Output current | 0mA – 600mA (When $V_{IN}$ >= 5V) |

#### 7.2.1.2 Detailed Design Procedure

##### *7.2.1.2.1 Programming the Output Voltage*

Output voltage is programmed through an external resistor divider. By selecting the external resistor divider $R_{FBT}$ and $R_{FBB}$, as shown in Figure 7-1, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage at the FB pin is $V_{REF}$ of 1.233V.

$$R_{FBT} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_{FBB} \quad (1)$$

where

- $V_{OUT}$ is the desired output voltage
- $V_{REF}$ is the internal reference voltage at the FB pin

For best accuracy, keep $R_{FBB}$ smaller than 150kΩ to make sure the current flowing through $R_{FBB}$ is at least 100 times larger than the FB pin leakage current. Changing $R_{FBB}$ toward a lower value increases the immunity against noise injection. Changing the $R_{FBB}$ toward a higher value reduces the quiescent current for achieving higher efficiency at low load currents.

#### *7.2.1.2.2 Inductor Selection*

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and DC resistance (DCR). The TLV61047-Q1 is designed to work with inductor values between 1µH and 4.7µH. Use Equation 2 to Equation 4 to calculate the peak current of the application inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margin, select the inductor value with –30% tolerance, and a low power-conversion efficiency for the calculation. In a boost regulator, use Equation 2 to calculate the inductor dc current.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (2)$$

where

- $V_{OUT}$ = output voltage
- $I_{OUT}$ = output current
- $V_{IN}$ = input voltage
- η = power conversion efficiency, use 80% for most applications

The inductor ripple current is calculated with the with the equation below for an asynchronous boost converter in continuous conduction mode (CCM).

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} + V_D - V_{IN})}{L \times f_{SW} \times (V_{OUT} + V_D)} \quad (3)$$

where

- $\Delta I_{L(P-P)}$ = inductor ripple current
- L = inductor value
- $f_{SW}$ = switching frequency
- $V_{OUT}$ = output voltage
- $V_{IN}$ = input voltage
- $V_D$ = the forward voltage of the Schottky diode

Therefore, the inductor peak current is calculated with the below equation.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (4)$$

Normally, working with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current is advisable. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. However, in the same way, load transient response time is increased. Table 7-2 lists the recommended inductor for the TLV61047-Q1 in the 2.4MHz configuration.

**Table 7-2. Recommended Inductors for the TLV61047-Q1 at 2.4MHz Configuration**

| PART NUMBER | L (µH) | DCR MAX (mΩ) | SATURATION CURRENT TYPICAL (A) | SIZE (L × W × H) (mm) | VENDOR(1) |
|---|---|---|---|---|---|
| 74438357022 | 2.2 | 26 | 9.2 | 4.1 × 4.1 × 3.1 | Wurth Electronics |
| XAL4020-222ME | 2.2 | 38.7 | 5.6 | 4 × 4 × 2.1 | Coilcraft |
| SWPA5040S4R7NT | 4.7 | 39 | 3.9 | 5 × 5 × 4 | Sunlord |
| XAL4030-472ME | 4.7 | 44.1 | 4.5 | 4 × 4 × 3 | Coilcraft |

(1) See the *Third-party Products Disclaimer*.

#### *7.2.1.2.3 Input and Output Capacitor Selection*

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor capacitance and the equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, use Equation 5 to calculate the minimum capacitance needed for a given ripple:

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (5)$$

where

- $D_{MAX}$ = maximum switching duty cycle
- $V_{RIPPLE}$ = peak to peak output voltage ripple

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used.

Take care when evaluating the derating of a ceramic capacitor under DC bias, aging, and AC signal. For example, the DC bias can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of the capacitance at the rated voltage. Therefore, always leave margin on the voltage rating to make sure of adequate capacitance at the required output voltage.

TI recommends using the output capacitor with effective capacitance 10µF, which covers the major applications. TI also recommends placing a small 1µF capacitor right across the rectifier diode cathode to the GND pin of the TLV61047-Q1 to reduce the high RMS current loop inductance. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output voltage ripple smaller in PWM mode. Table 7-3 lists the recommended capacitor for the TLV61047-Q1.

**Table 7-3. Recommended Output Capacitors for the TLV61047-Q1**

| PART NUMBER | $C_{OUT}$ (µF) | RATING | PACKAGE | VENDOR(1) |
|---|---|---|---|---|
| TMK316BLD106KL | 10 | 25V, X5R | 1206 | Taiyo Yuden |
| CC1206KKX5R8BB106 | 10 | 25V, X5R | 1206 | Yageo |
| CGA5L1X7R1H106K160AC | 10 | 50V, X7R | 1206 | TDK |

(1) See the *Third-party Products Disclaimer*.

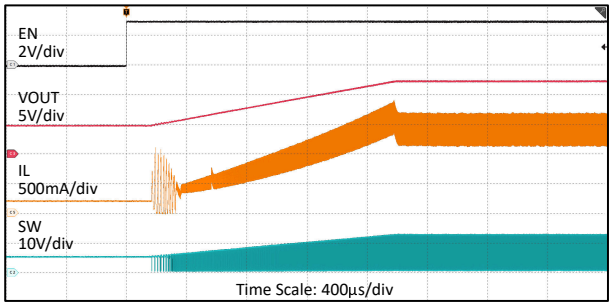
The ceramic capacitors are an excellent choice for the input decoupling of the step-up converter because ceramic capacitors have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 10µF input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the device. Additional "bulk" capacitor (electrolytic or tantalum) in this circumstance, must be placed between $C_{IN}$ and the power source lead to reduce ringing that can occur between the inductance of the power source leads and $C_{IN}$.

#### 7.2.1.2.4 Diode Rectifier Selection

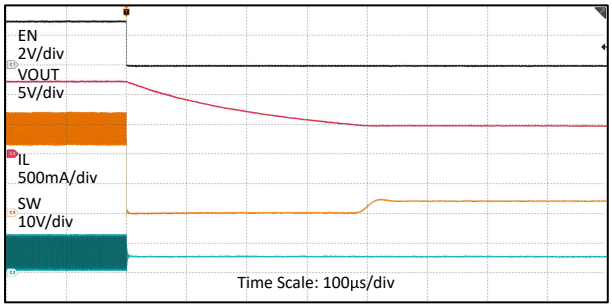
A Schottky diode is the preferred type due to the low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus any switching node ringing. Also, the diode must be able to handle the average output current.

### 7.2.1.3 Application Curves



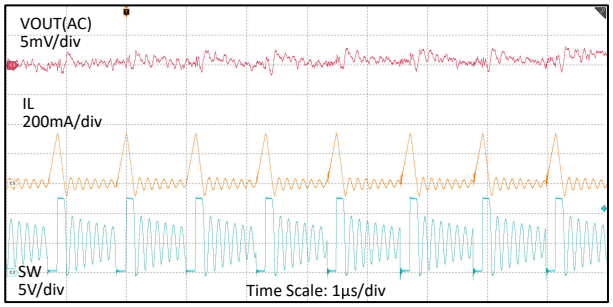

$V_{IN}$ = 5V $V_{OUT}$ = 12V $R_{LOAD}$ = 24Ω

**Figure 7-2. Start-up by EN Waveforms**



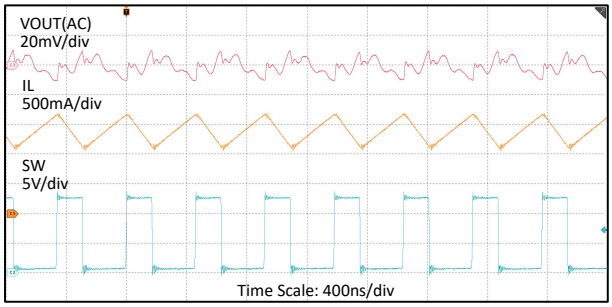

$V_{IN}$ = 5V $V_{OUT}$ = 12V $R_{LOAD}$ = 24Ω

**Figure 7-3. Shutdown by EN Waveforms**



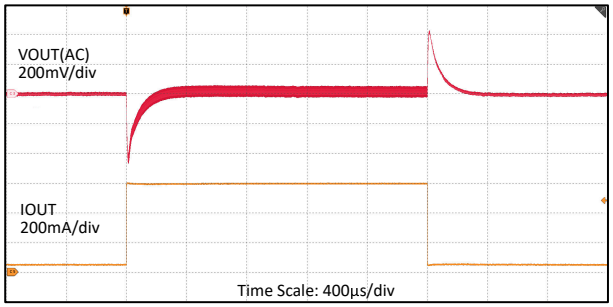

$V_{IN}$ = 5V $V_{OUT}$ = 12V $I_{OUT}$ = 7mA

**Figure 7-4. Switching Waveforms in Steady State**



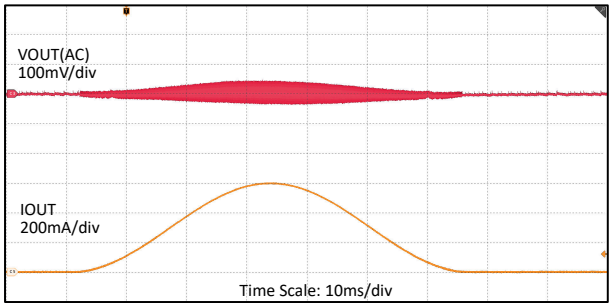

$V_{IN}$ = 5V $V_{OUT}$ = 12V $I_{OUT}$ = 500mA

**Figure 7-5. Switching Waveforms in Steady State**




$V_{IN}$ = 5V $V_{OUT}$ = 12V $I_{OUT}$ = 50mA to 600mA

**Figure 7-6. Load Transient**




$V_{IN}$ = 5V $V_{OUT}$ = 12V $I_{OUT}$ = 0 to 600mA

**Figure 7-7. Load Sweep**

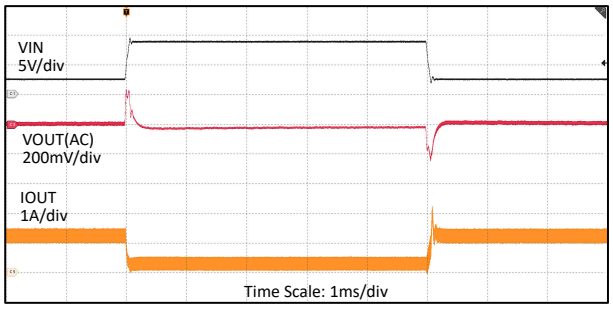



**Figure 7-8. Line Transient**

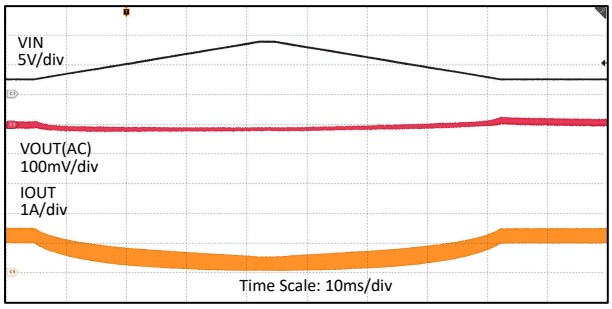



**Figure 7-9. Line Sweep**

### *7.2.2 28V Output Boost Converter*

In this design example, TLV61047-Q1 $V_{OUT}$ is configured as 28V with a input source from 9V to 20V. The principles of the components selection, including the inductor, input and output capacitors diode are the same with those in the example of *12V Output Boost Converter*.

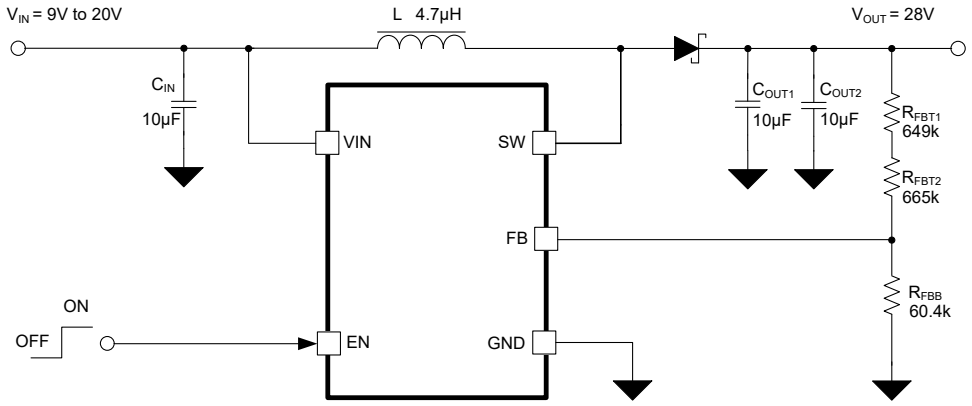


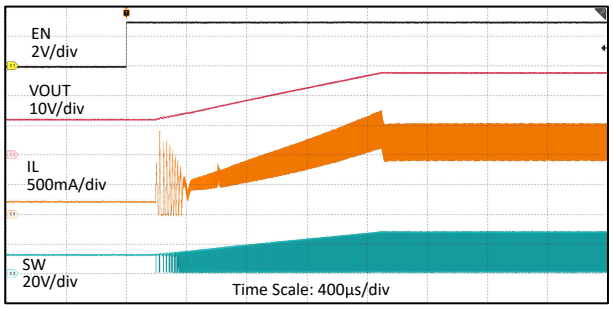

**Figure 7-10. Typical 28V Application**

#### 7.2.2.1 Design Requirements

**Table 7-4. Design Requirements**

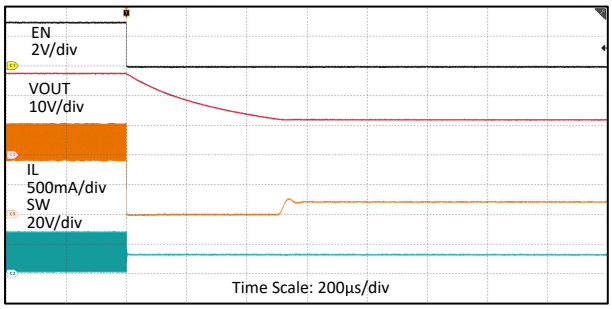
| PARAMETER | VALUE |
|---|---|
| Input voltage | 9V to 20V |
| Output voltage | 28V |
| Frequency | 2.4MHz |
| Output current | 0mA – 600mA (When $V_{IN}$ >= 12V) |

### 7.2.2.2 Application Curves



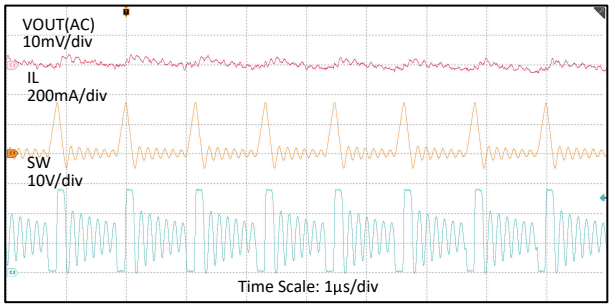

$V_{IN}$ = 12V $V_{OUT}$ = 28V $R_{LOAD}$ = 56Ω

**Figure 7-11. Start-up by EN Waveforms**



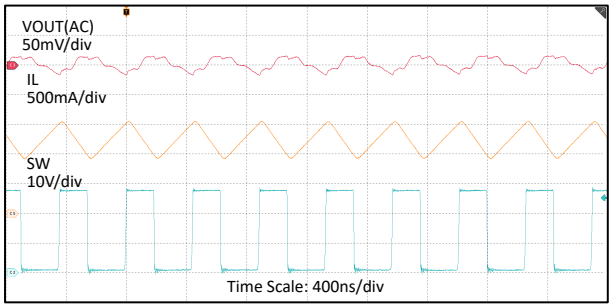

$V_{IN}$ = 12V $V_{OUT}$ = 28V $R_{LOAD}$ = 56Ω

**Figure 7-12. Shutdown by EN Waveforms**



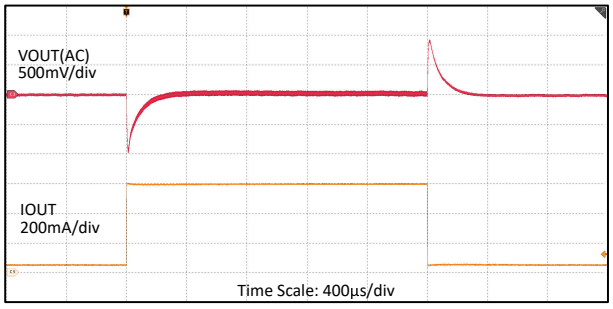

$V_{IN}$ = 12V $V_{OUT}$ = 28V $I_{OUT}$ = 7mA

**Figure 7-13. Switching Waveforms in Steady State**



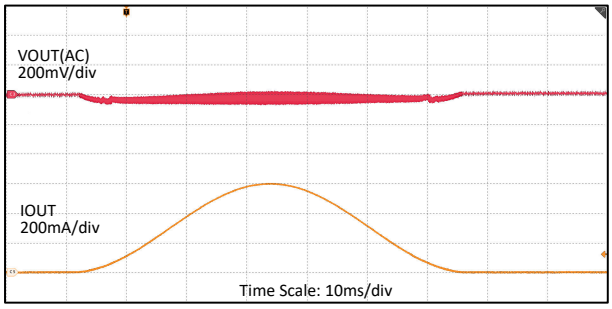

$V_{IN}$ = 12V $V_{OUT}$ = 28V $I_{OUT}$ = 500mA

**Figure 7-14. Switching Waveforms in Steady State**



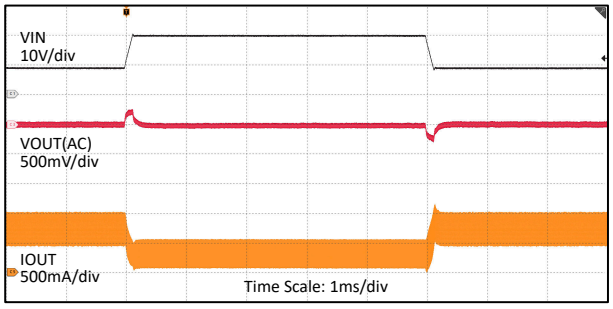

$V_{IN}$ = 12V $V_{OUT}$ = 28V $I_{OUT}$ = 50mA to 600mA

**Figure 7-15. Load Transient**



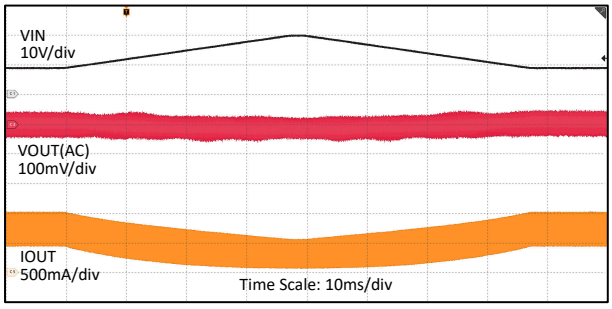

$V_{IN}$ = 12V $V_{OUT}$ = 28V $I_{OUT}$ = 0 to 600mA

**Figure 7-16. Load Sweep**




$V_{IN}$ = 9V to 20V $V_{OUT}$ = 28V $I_{OUT}$ = 200mA

**Figure 7-17. Line Transient**




$V_{IN}$ = 9V to 20V $V_{OUT}$ = 28V $I_{OUT}$ = 200mA

**Figure 7-18. Line Sweep**

## 7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8V to 20V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47µF. Output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TLV61047-Q1.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor must not only to be close to the VIN pin, but also to the GND pin to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier diode, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and must be kept as short as possible. Therefore, the output capacitor must not only to be close to the GND pin, but also to the cathode of the high side rectifier to reduce the overshoot at the SW pin.

### *7.4.2 Layout Example*

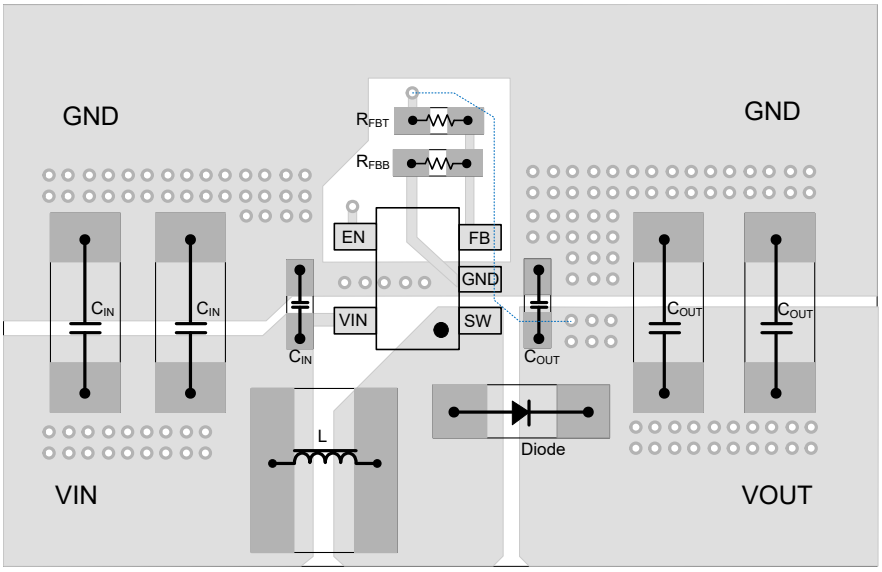



**Figure 7-19. TLV61047-Q1 Layout**

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Third-Party Products Disclaimer*

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## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| March 2026 | * | Initial release |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV61047QDDCRQ1 | Active | Production | SOT-23-THIN (DDC) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 1047Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TLV61047-Q1 :**

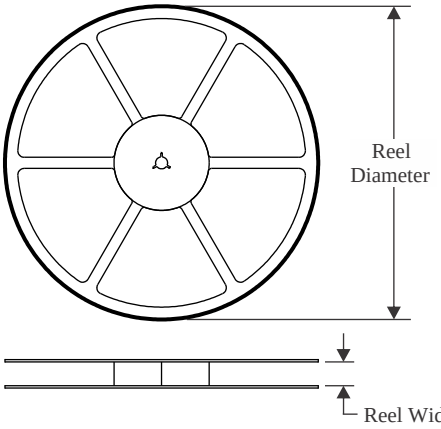
- Catalog : TLV61047

NOTE: Qualified Version Definitions:

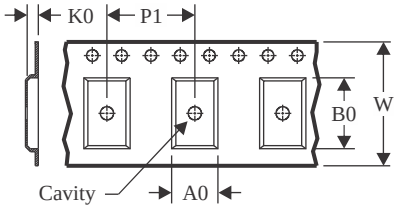
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

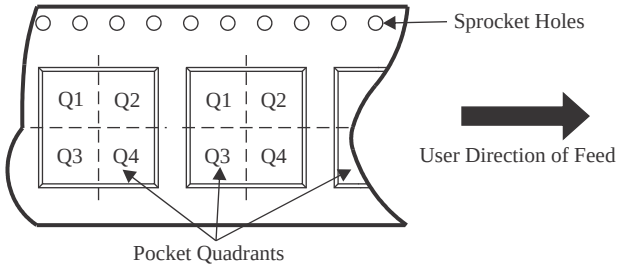



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

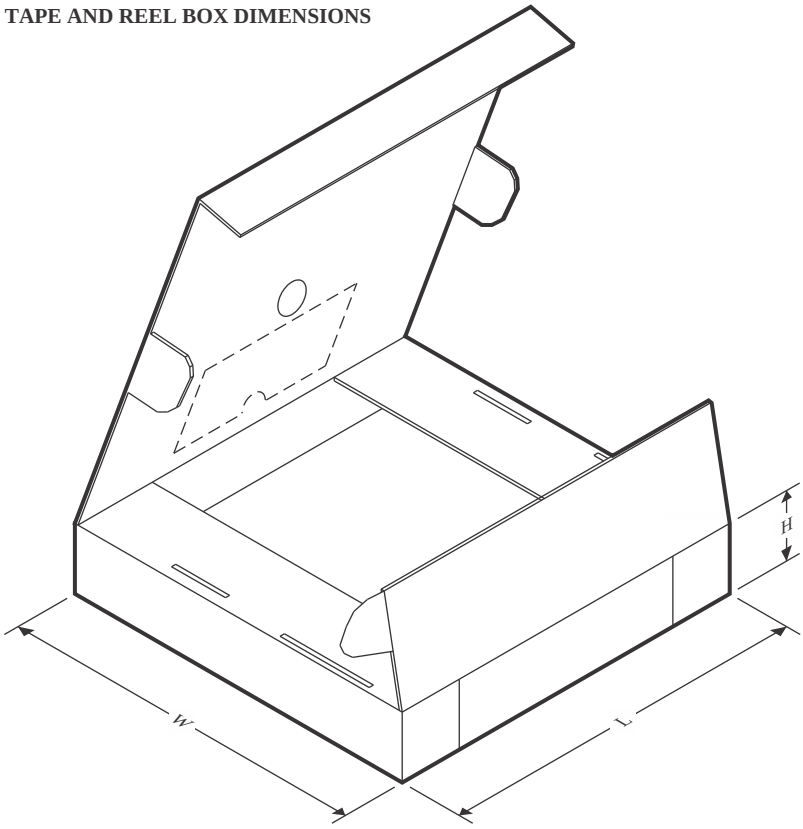
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV61047QDDCRQ1 | SOT-23-THIN | DDC | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

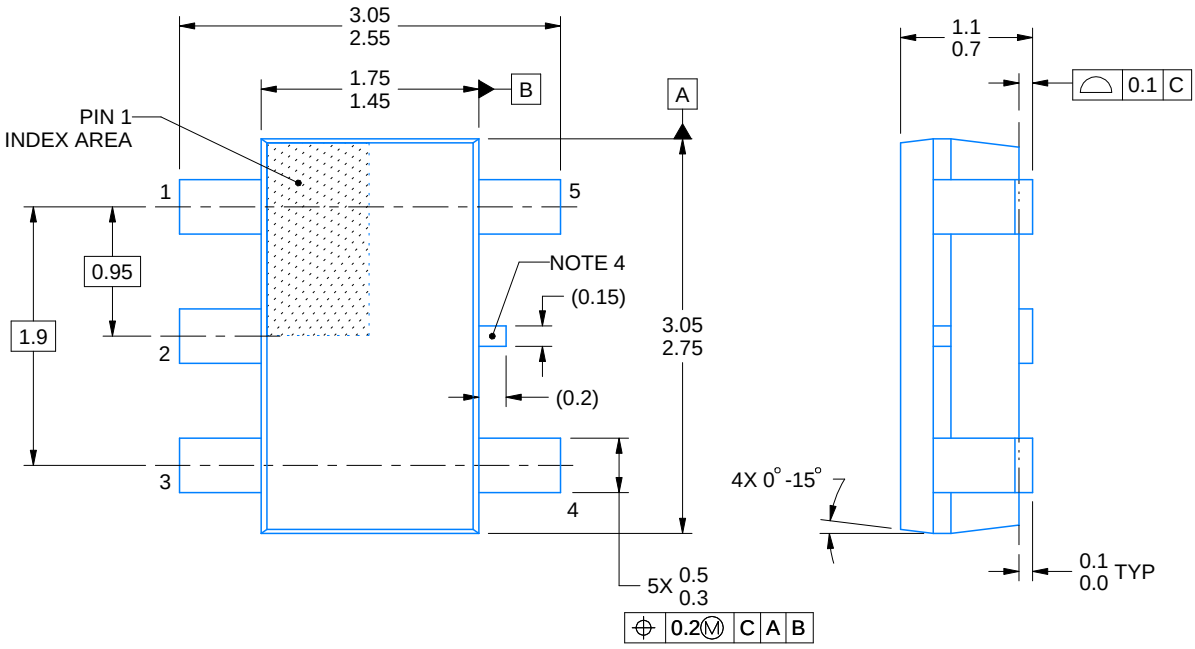
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV61047QDDCRQ1 | SOT-23-THIN | DDC | 5 | 3000 | 210.0 | 185.0 | 35.0 |

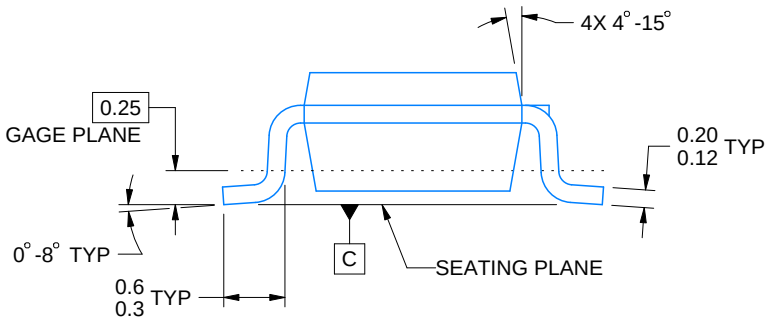
# PACKAGE OUTLINE

## DDC0005A

## SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

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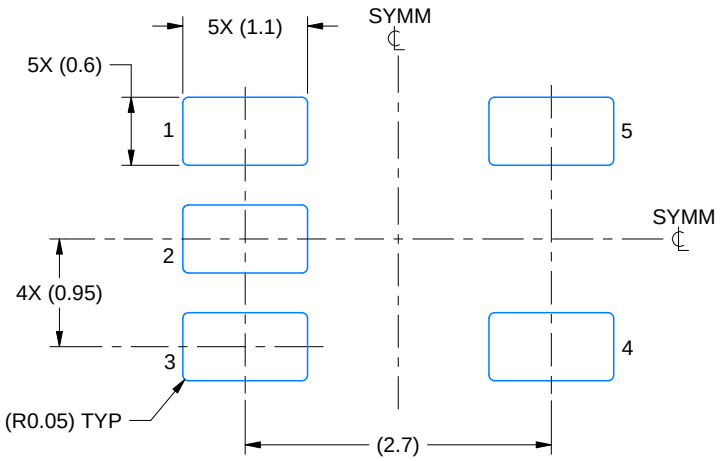
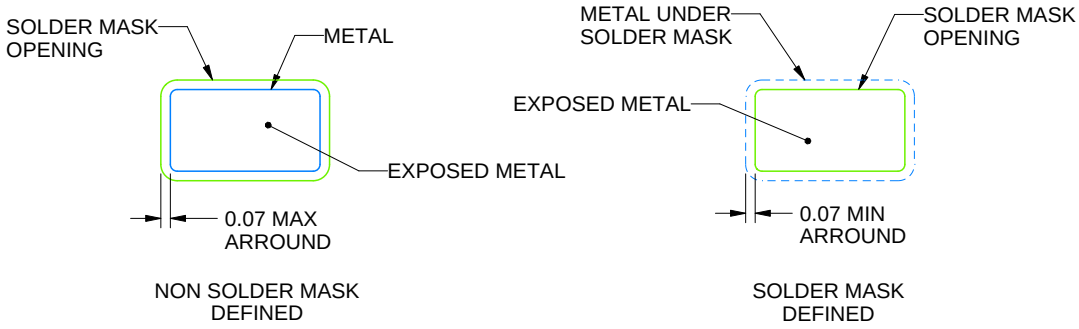
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X




SOLDERMASK DETAILS

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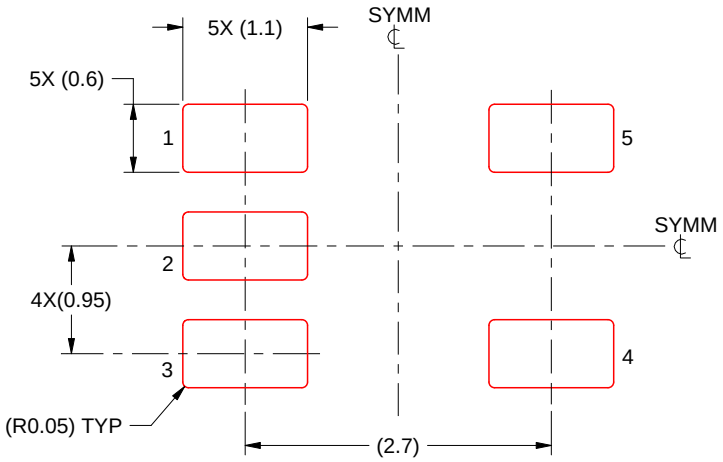
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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