TLV612901 5.5V, 11A Synchronous Boost Converter With Bypass Mode and I²C Interface

1 Features

- 1.8V to 5.5V wide V_{IN} range
  - 2.2V start-up input voltage
- Programmable average input current limit (3.5A to 11A) through I²C, default 8A
- Programmable output voltage (2.35V to 5.5V) through I²C, default 5.0V
- High efficiency and power capability
  - Default 8A average input current limit
  - Two 8mΩ (LS) / 8mΩ (HS) MOSFETs
  - 10mΩ bypass MOSFET
  - 96.3% peak efficiency at V_{IN} = 4.2V, V_{OUT} = 5.0V, and I_{OUT} = 1.5A
  - Up to 94.4% efficiency at V_{IN} = 4.2V, V_{OUT} = 5.0V, and I_{OUT} = 4A
- Auto bypass mode when V_{IN} > V_{OUT}
- Auto PFM, forced PWM or ultrasonic mode selectable at light load
- Output discharge function when EN logic is low
- True disconnection between input and output during shutdown
- Thermal shutdown and overcurrent protection
- Output short-circuit protection
- I²C compatible I/F up to 1Mbps
- 1.2V I/O logic control interface
- 16-ball WCSP package

2 Applications

- Mobile phones
- Tablet
- Optical module
- 4G, 5G mini-module data card
- Satellite communication
- RF power amplifier

3 Description

The TLV612901 is a 5.5V, 11A synchronous boost converter with integrated bypass mode for single-cell battery-powered systems. The device operates over a wide input voltage range and supports startup from 2.2V. The output voltage is programmable through I²C, ranging from 2.35V to 5.5V, with a default value of 5.0V. The TLV612901 is optimized for high power capability, fast transient response, and high efficiency across a wide battery operating range.

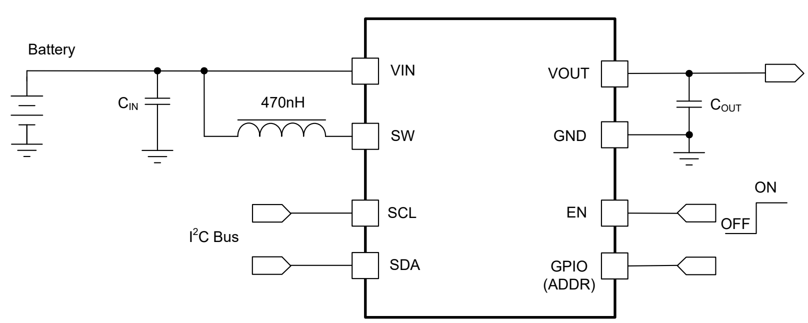
The TLV612901 can be used as a high-power pre-regulator to overcome input voltage droop and input current limitations of the powered system while extending battery run time. When the input voltage is higher than the target output voltage, the device automatically enters bypass mode for maximum efficiency. When the input voltage drops below the target output voltage, the device seamlessly transitions into boost mode to maintain the regulated output voltage and enable full use of the battery capacity. The device also supports forced bypass operation through I²C.

The TLV612901 also supports selectable light-load operating mode, output discharge during shutdown, and true disconnection between input and output. The TLV612901 is available in a 16-ball WCSP package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV612901	YBG (DSBGA, 16)	1.577mm × 1.577mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Circuit

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4 Device Comparison Table

PART NUMBER	DEFAULT OUTPUT VOLTAGE	GPIO FUNCTION	DEFAULT GPIO CONFIGURATION
TLV612901	5.0V	ADDR	Programmable: 75h (ADDR = L), 76h (ADDR = H), 77h (ADDR floating)
TLV612902(1)	3.4V or 3.55V	VSEL	VOUTFLOORSET: (VSEL = Low, 3.4Vout) VOUTROOFSET: (VSEL = High, 3.55Vout)

(1) Product preview (not Production Data). Contact TI factory for more information.

Texas Instruments
www.ti.com

5 Pin Configuration and Functions

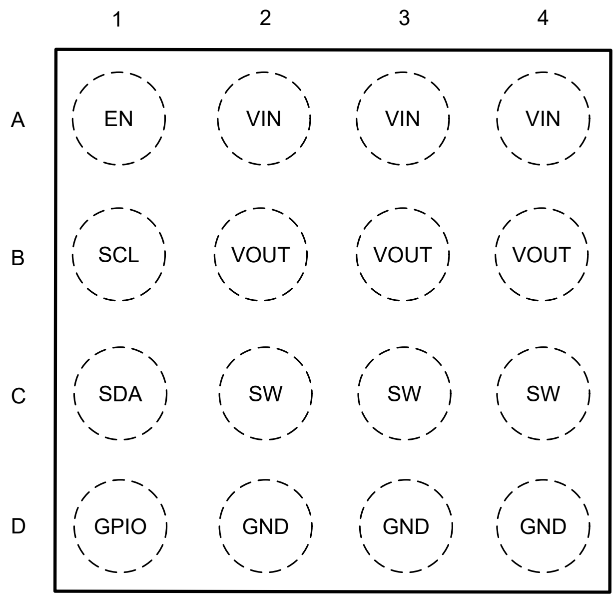


Figure 5-1. TLV612901 YBG Package, 16-Pin DSBGA (Top View)

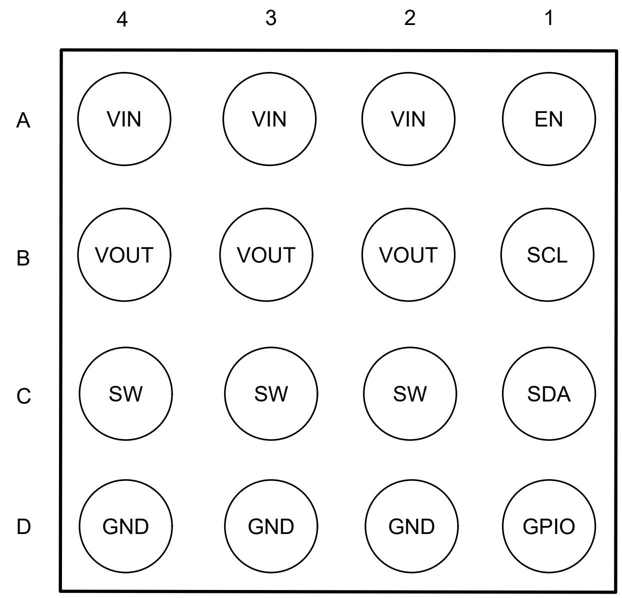


Figure 5-2. TLV612901 YBG Package, 16-Pin DSBGA (Bottom View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	A1	I	Enable logic input. A high logic level enables the device. A low logic level disables the device and places the device in shutdown mode.
VIN	A2, A3, A4	PWR	Power input
SCL	B1	I	Serial interface clock line. Terminate this pin and do not leave this pin floating.
VOUT	B2, B3, B4	PWR	Converter output
SDA	C1	I	Serial interface address/data line. Terminate this pin and do not leave this pin floating.
SW	C2, C3, C4	PWR	Switch node. This pin is connected to the drain of the internal low-side MOSFET and the source of the internal high-side MOSFET.
GPIO	D1	I/O	Configure the pin as ADDR or VSEL function. For TLV612901, the default configuration is ADDR function.
			ADDR: I^2C target address selection. I^2C target address is 75h when ADDR is low, I^2C target address is 76h when ADDR is high, I^2C target address is 77h when ADDR is floating. The address is locked when the start-up sequence is successfully completed. VSEL: output voltage selection. Vout is VOUTFLOOR_TH when VSEL is low. Vout is VOUTROOF_TH when VSEL is high.
GND	D2, D3, D4	PWR	Ground pin of the IC. The GND pad of output capacitor must be close to the GND pin.

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
Input voltage	VIN, SW, EN, VOUT, SCL, SDA, GPIO[2]	DC	–0.3	7	V
Input voltage	SW spike at 10ns[2]	AC	–0.7	8	V
Input voltage	SW spike at 5ns[2]	AC	–0.7	8.5	V
Input current	Continuous average current into SW[3]			6	A
Temperature	Operating junction temperature, T_J		–40	150	°C
Temperature	Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network ground terminal.
(3) Lifetime is reduced when operating continuously at 6A output current and the junction temperature is higher than 85°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions. Pins listed as ±2000V can actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions. Pins listed as ±500V can actually have higher performance.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	1.8		5.5	V
V_{OUT}	Output voltage setting range	2.35		5.5	V
L	Effective inductance range	330	470	560	nH
C_{in}	Effective input capacitance range		5		µF
C_O	Effective output capacitance range, $I_{out} \le 4A$	15	20		µF
	Effective output capacitance range, $4A < I_{out} \le 6A$	20			µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLV612901	TLV612901	UNIT
		YBG (16 PINS)	YBG (16 PINS)	
		Standard	EVM[2]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	78	40.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	0.6	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.4	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13	16.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) Measured on TLV61290EVM-076, 4-layer, 2oz copper 92.2mm × 59.2mm PCB.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 1.8V to 5.5V, V_{OUT} = 3.4V (or V_{IN}, whichever is higher), EN = 1.2V, GPIO= 1.2V. Typical values are at V_{IN} = 3.2V, V_{OUT} = 3.4V, EN = 1.2V, T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		1.8		5.5	V
V_{UVLO}	Undervoltage lockout threshold	Rising		2.1	2.2	V
V_{UVLO}	Undervoltage lockout threshold	Falling		1.7	1.8	V
		Hysteresis		0.4		V
I_Q	Operating quiescent current into V_{IN}	DC/DC boost mode. Device not switching EN = V_{IN}, ENABLE_bit = 01 –40°C ≤ T_J ≤ 85°C		42	57	µA
	Operating quiescent current into V_{OUT}	DC/DC boost mode. Device not switching EN = V_{IN}, ENABLE_bit = 01 2.35V ≤ V_{OUT} ≤ 5.5V –40°C ≤ T_J ≤ 85°C		12	23	µA
	Operating quiescent current in auto bypass mode	True bypass mode (auto) EN = V_{IN}, ENABLE_bit = 01 –40°C ≤ T_J ≤ 85°C		35	49	µA
	Operating quiescent current in forced bypass mode	True bypass mode (forced) EN = V_{IN}, ENABLE_bit = 10 –40°C ≤ T_J ≤ 85°C		35	47	µA
I_{SD}	Shutdown current	Shutdown mode EN = GND, V_{OUT} = GND T_J = 25°C		0.55	2	µA
	Shutdown current	Shutdown mode EN = GND, V_{OUT} = GND –40°C ≤ T_J ≤ 85°C		0.55	11	µA
	Shutdown current	Shutdown mode, but I^2C block is active. EN = V_{IN}, ENABLE_bit = 11 T_J = 25°C		16	23	µA
	Shutdown current	Shutdown mode, but I^2C block is active. EN = V_{IN}, ENABLE_bit = 11 –40°C ≤ T_J ≤ 85°C		16	35	µA
EN, SDA, SCL, GPIO						
V_{IL}	Low-level input voltage		0.33			V
V_{IH}	High-level input voltage				0.82	V
V_{OL}	Low-level output voltage (SDA)	I_{OL} = 8mA			0.36	V
R_{PD}	EN pull-down resistance	Applied voltage < 0.4V		800		kΩ
I_{lkg}	Input leakage current	–40°C ≤ T_J ≤ 85°C			0.1	µA
OUTPUT						
V_{OUT}	Output voltage setting range		2.35		5.5	V
V_{OUT_PWM}	DC voltage accuracy	2.2V ≤ V_{IN} ≤ V_{OUT_TAR} - 150mV PWM operation	–1.5		1.5	%
$V_{OUT\_BP\_ENTER}$	Enter bypass mode threshold	MODE_CTRL = 00, auto PFM		V_{OUT_PWM} × (1 + 0.5%)		V
$V_{OUT\_BP\_ENTER}$	Enter bypass mode threshold	MODE_CTRL = 10, FPWM		V_{OUT_PWM} × (1 + 2%)		V
$V_{OUT\_BP\_EXIT}$	Exit bypass mode threshold	Auto bypass mode		V_{OUT_PWM} × (1 – 3%)		V
V_{OVP}	Output overvoltage protection threshold	VOUT rising	5.45	5.58	5.70	V

6.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 1.8V to 5.5V, V_{OUT} = 3.4V (or V_{IN}, whichever is higher), EN = 1.2V, GPIO= 1.2V. Typical values are at V_{IN} = 3.2V, V_{OUT} = 3.4V, EN = 1.2V, T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DIS_OUT}	Output equivalent discharge impedance			90		Ω
POWER SWITCH						
$R_{DS(on)}$	Low-side switch MOSFET on resistance	V_{OUT} = 5V		8	13.5	mΩ
	High-side rectifier MOSFET on resistance	V_{OUT} = 5V		8	13.5	mΩ
	Low-side switch MOSFET on resistance	V_{OUT} = 3.4V		10	15	mΩ
	High-side rectifier MOSFET on resistance	V_{OUT} = 3.4V		10	15	mΩ
	Bypass MOSFET on resistance	V_{OUT} = 2.35V to 5.5V		10	15	mΩ
I_{LIM_SW}	Average Inductor current limit	ILIM_BOOST = 0110 (default), 1.8V ≤ V_{IN} ≤ 5.5V	6	8	9	A
	Average Inductor current limit adjustable range through I^2C	Typical value, 1.8V ≤ V_{IN} ≤ 5.5V	3.5		11	A
ILIM_REVERSE	Reverse current limit (FPWM operation)	MODE_CTRL = 10		–1		A
I_{LIM_BP}	Bypass mode current limit (Forced)	ENABLE_bit = 10, ILIM_FPT = 010 (default)	6.5	8	11.2	A
	Bypass mode current limit (Auto)	ENABLE_bit = 01, ILIM_APT = 010 (default)	6.5	8	11.2	A
I_{lkg}	Low-side switch MOSFET leakage current	EN = GND, –40°C ≤ T_J ≤ 85°C		0.1	5	µA
	High-side switch MOSFET leakage current	EN = GND, –40°C ≤ T_J ≤ 85°C		0.1	5	µA
	Bypass MOSFET leakage current	EN = GND, –40°C ≤ T_J ≤ 85°C		0.6	5	µA
OSCILLATOR						
T_{ON_MIN}	Minimum On time	PWM mode		80		ns
$F_{sw\_min\_fpwm}$	Minimum switching frequency in FPWM	MODE_CTRL = 10	375	440		kHz
$F_{sw\_min\_pfm}$	Minimum switching frequency in Ultrasonic mode	MODE_CTRL = 01	23			kHz
F_{DITHER}	Spread Spectrum dithering frequency	V_{IN}= 3.2V, V_{OUT}=3.4V, MODE_CTRL = 10, SSFM = 1		±8%		F_{sw}
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown(1)	T_J rising		165		°C
T_{SD_HYS}	Thermal shutdown hysteresis(1)			20		
TIMING						
	Soft start-up time(1)	Internal SS ramp time		400		µs
	Hiccup on time	HICCUP_MODE bit = 1		1		ms
	Hiccup off time	HICCUP_MODE bit = 1		19		ms

(1) Verified by characterization. Not tested in production.

6.6 I²C Interface Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
$f_{(SCL)}$	SCL Clock Frequency	Fast mode		400	kHz
$f_{(SCL)}$	SCL Clock Frequency	Fast mode plus		1	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Fast mode plus	0.5		μs
t_{HD}, t_{STA}	Hold Time (Repeated) START Condition		260		ns
t_{LOW}	LOW Period of the SCL Clock		0.5		μs
t_{HIGH}	HIGH Period of the SCL Clock		260		ns
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition		260		ns
t_{SU}, t_{DAT}	Data Setup Time		50		ns
t_{HD}, t_{DAT}	Data Hold Time		0		μs
t_{RCL}	Rise Time of SCL Signal			120	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT			120	ns
t_{FCL}	Fall Time of SCL Signal			120	ns
t_{RDA}	Rise Time of SDA Signal			120	ns
t_{FDA}	Fall Time of SDA Signal			120	ns
$t_{SU,}$ t_{STO}	Setup Time of STOP Condition		260		ns
C_B	Capacitive Load for SDA and SCL			200	pF

(1) Specified by design. Not tested in production.

6.7 Typical Characteristics

Typical condition V_{IN} = 2.5V to 4.5V, V_{OUT_TAR} = 5.0V, T_J = 25°C, unless otherwise noted

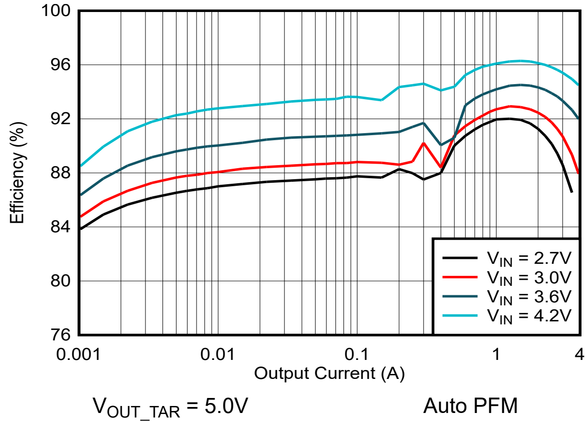


Figure 6-1. Efficiency vs Output Current

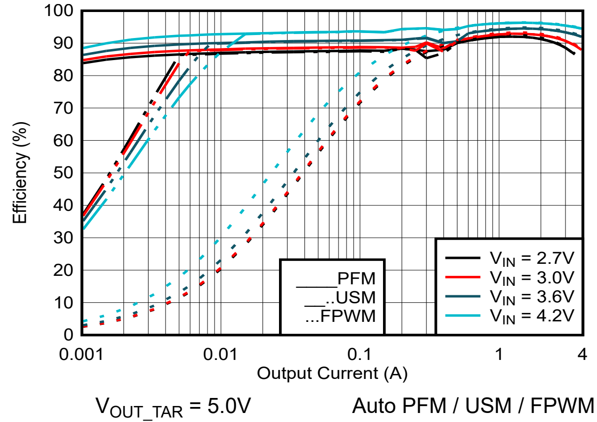


Figure 6-2. Efficiency vs Output Current

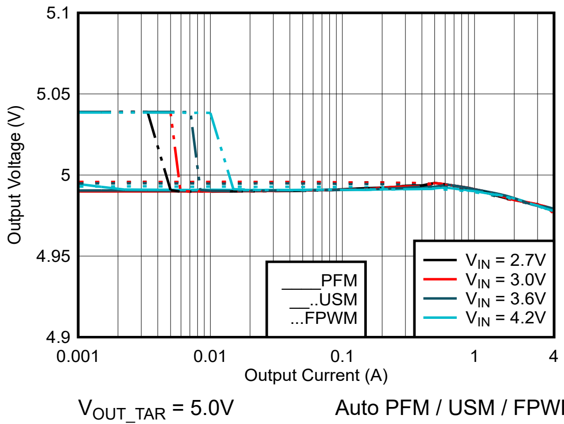


Figure 6-3. DC Output Voltage vs Output Current

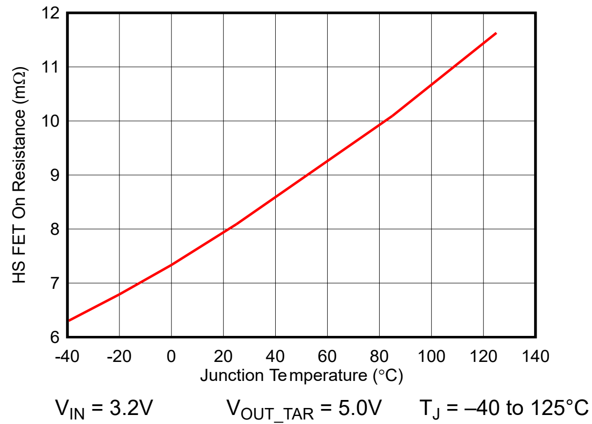


Figure 6-4. High side $R_{ds(on)}$ vs Junction Temperature

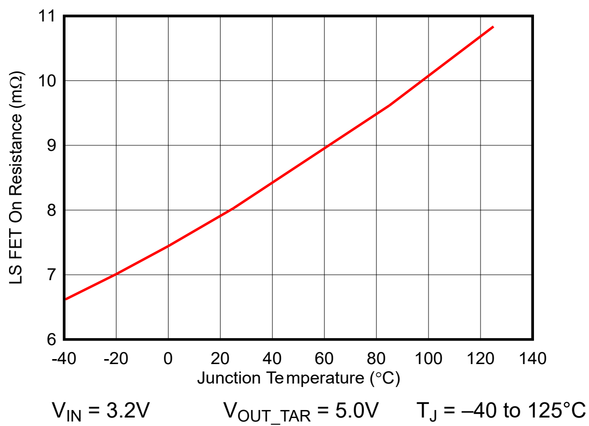


Figure 6-5. Low side $R_{ds(on)}$ vs Junction Temperature

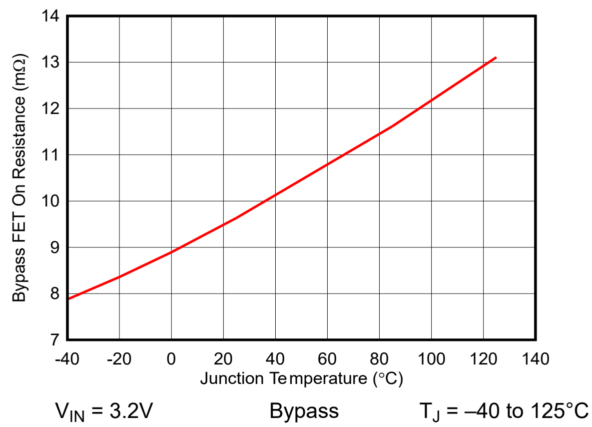
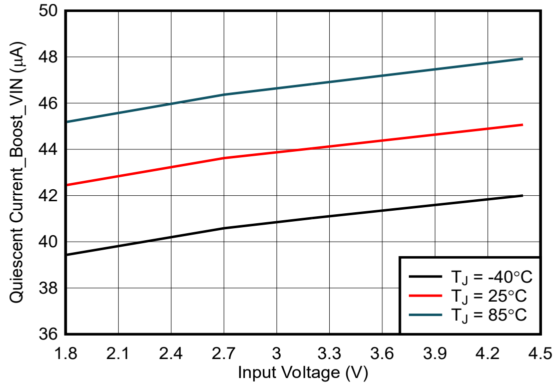


Figure 6-6. Bypass FET $R_{ds(on)}$ vs Junction Temperature

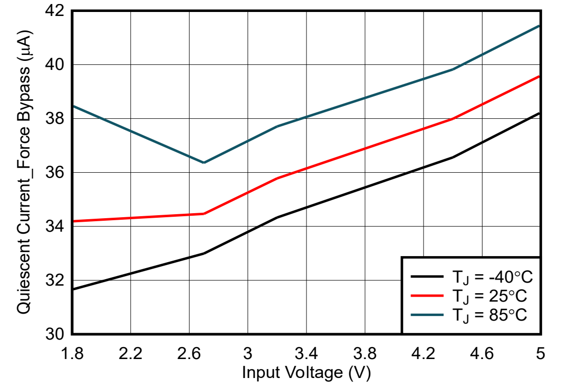
6.7 Typical Characteristics (continued)

Typical condition V_{IN} = 2.5V to 4.5V, V_{OUT_TAR} = 5.0V, T_J = 25°C, unless otherwise noted



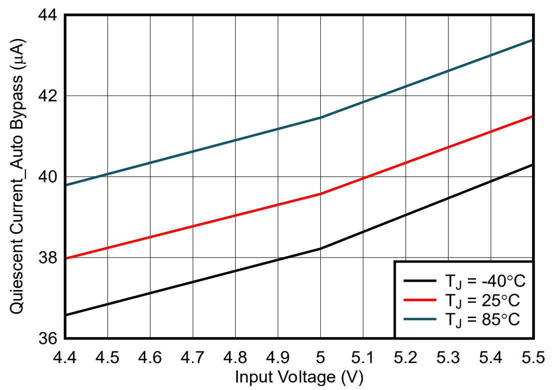
V_{IN} = 1.8V to 4.4V V_{OUT_TAR} = 5.0V I_{OUT} = 0mA
EN = High ENABLE_bit = 01

Figure 6-7. Quiescent Current into V_{IN} at Boost Mode vs Input Voltage



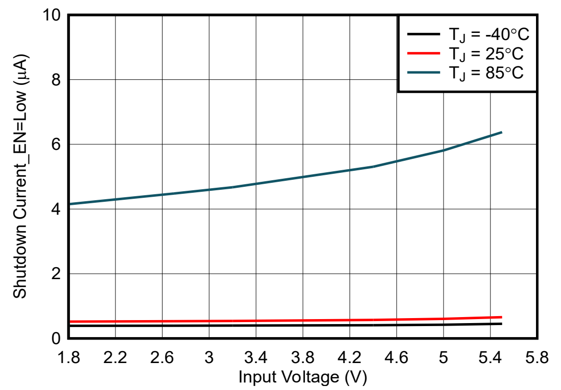
V_{IN} = 1.8 to 5.0V Bypass I_{OUT} = 0mA
EN = High ENABLE_bit = 10

Figure 6-8. Quiescent Current at Forced Bypass Mode vs Input Voltage



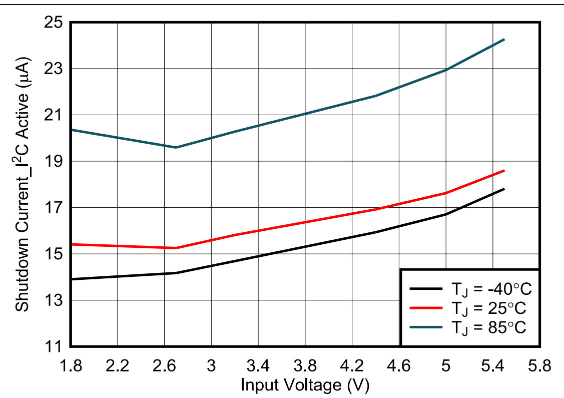
V_{IN} = 4.4 to 5.5V Bypass I_{OUT} = 0mA
EN = High ENABLE_bit = 01 V_{OUT_TAR} = 3.4V

Figure 6-9. Quiescent Current at Auto Bypass Mode vs Input Voltage



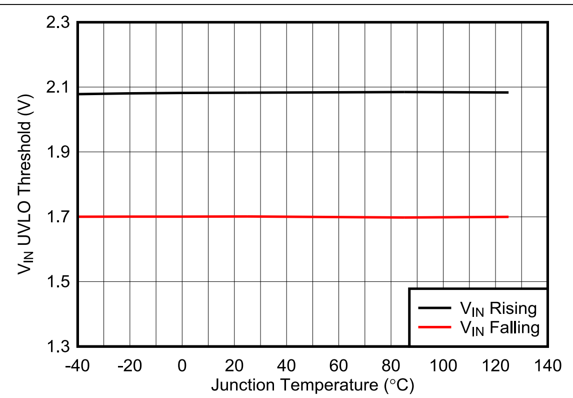
V_{IN} = 1.8 to 5.5V V_{OUT} = GND EN = Low

Figure 6-10. Shutdown Current at EN = Low vs Input Voltage



V_{IN} = 1.8 to 5.5V ENABLE_bit = 11 EN = High

Figure 6-11. Shutdown Current with Active I^2C Block vs Input Voltage



V_{OUT_TAR} = 5.0V T_J = –40 to 125°C

Figure 6-12. V_{IN} UVLO Threshold Rising/Falling vs Junction Temperature

7 Detailed Description

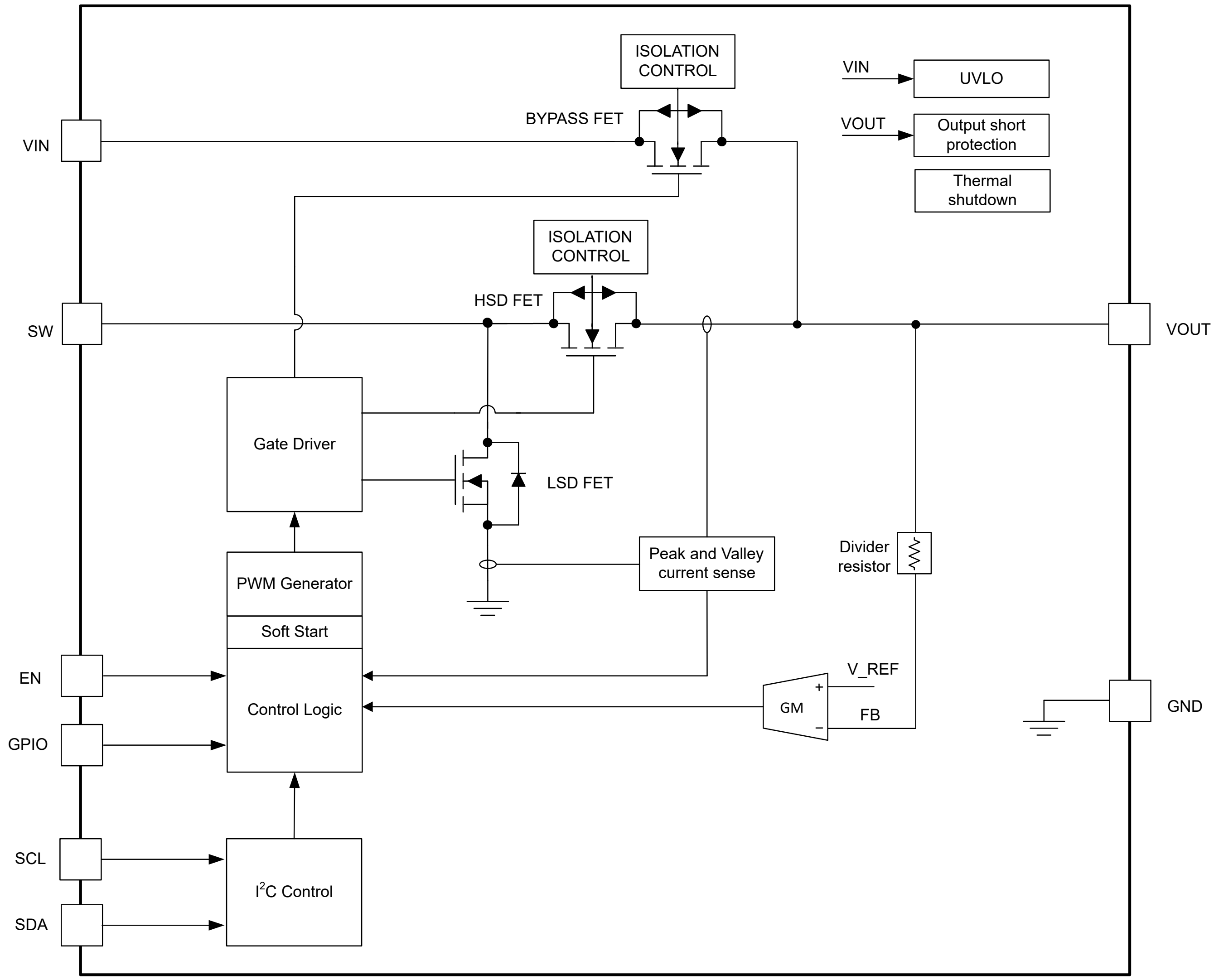
7.1 Overview

The TLV612901 is a high-efficiency, synchronous boost converter with integrated bypass mode optimized for single-cell battery-powered systems. The device includes an 8mΩ low-side power MOSFET, an 8mΩ high-side rectifier MOSFET, and a 10mΩ bypass MOSFET to support high efficiency across a wide input voltage range. With a default 8A average input current limit, the TLV612901 supports high power capability for systems that require a regulated 5.5V supply.

The TLV612901 supports both boost mode and bypass mode operation. When the input voltage is higher than the target output voltage, the device operates in bypass mode to maximize efficiency and minimize the input-to-output voltage drop. When the input voltage drops below the target output voltage, the device transitions to boost mode to maintain the regulated output voltage. This operating scheme allows the system to maintain performance over a wide battery voltage range while extending battery run time.

The TLV612901 uses a hysteretic current-mode control scheme and integrates an I^2C compatible interface allowing transfers up to 1Mbps. Use this communication interface to set the output voltage threshold for switching between boost and bypass mode, reconfigure the mode of operation (auto PFM or forced PWM or Ultrasonic mode), and set the average current limit or the output voltage. These features allow the TLV612901 to support both high-load operation and improved light-load efficiency in portable applications. For TLV612901, the default configuration of GPIO pin is ADDR function, allowing up to three chips to be configured on the same I^2C bus. I^2C target address is 75h when ADDR is low, I^2C target address is 76h when ADDR is high, I^2C target address is 77h when ADDR is floating.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage Setting

To maintain a certain minimum output voltage under heavy load transients, dynamically increase the output voltage set point by I2C register. The functionality also helps to mitigate undershoot during severe line transients, while minimizing the output voltage during more benign operating conditions to save power.

For TLV612901, the GPIO is configured as ADDR function, only set the output voltage by VOUTFLOORSET (default 5.0V).

7.3.2 Switching Frequency and Spread Spectrum Function

The TLV612901 uses a hysteretic control scheme, and TLV612901 maintains a constant inductor ripple current in the range of 1.0A. Therefore, the frequency is not fixed and determined by the operation condition.

In auto PFM operation, the minimum switching frequency is not limited, the switching frequency is approximately 20Hz (or even lower) with open load. In forced PWM operation, minimum switching frequency is limited to approximately 375kHz. In ultrasonic mode, the minimum switching frequency is limited to 23kHz to avoid audio band noise. With this unique feature, the TLV612901 avoids the low frequency switching and prevents the application against the low frequency noise sensitive range.

Switching regulators are particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The TLV612901 provides a spread spectrum feature. The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The result is a spectrum that is continuous and lower in peak amplitude, making complying with electromagnetic interference (EMI) standards and with the power supply ripple requirements in cellular and non-cellular wireless applications easier. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

The spread spectrum architecture varies the switching frequency by ca. ±8% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

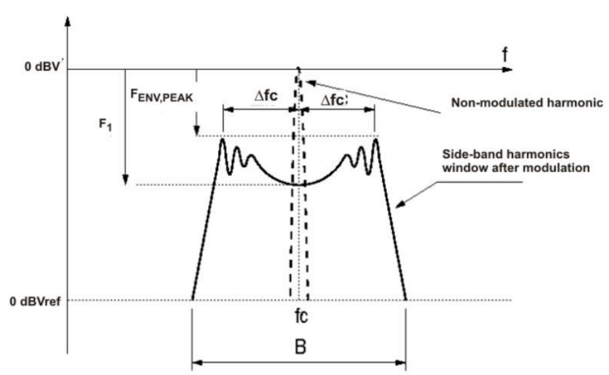


Figure 7-1. Spectrum of a Frequency Modulated Sin - Wave With Sinusoidal Variation in Time

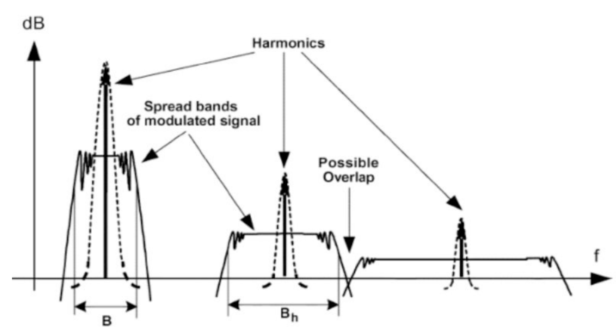


Figure 7-2. Spread Bands of Harmonics in Modulated Square Signals [1]

[1] Spectrum illustrations and formulae (Figure 7-1 and Figure 7-2) copyright IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY, VOL. 47, NO.3, AUGUST 2005.

The above figures show that after modulation the sideband harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \quad (1)$$

where

- f_c is the carrier frequency (switching frequency)
- f_m is the modulating frequency (approximately 0.5% × f_c)
- δ is the modulation ratio (approximately 8%)

$$\delta = \frac{\Delta f_c}{f_c} \quad (2)$$

The maximum switching frequency f_c is limited by the process and finally the parameter modulation ratio (δ), together with f_m, which is the side-band harmonics bandwidth around the carrier frequency f_c. The Carson's rule approximately gives the bandwidth of a frequency modulated waveform. Use Equation 3 to summarize:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \quad (3)$$

f_m < RBW: the receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: the receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

7.4 Device Functional Modes

7.4.1 Enable and Start-Up

The TLV612901 automatically powers-up after an input voltage greater than 2.2V. After start-up, the input voltage can be reduced to 1.8V. The device has an internal soft-start circuit that limits the inrush current during start-up.

The first phase in the start-up procedure is to bias the output node close to the input level (also called down mode pre-charge phase). In this operation mode, when VIN exceeds 2.8V, the TLV612901 has three operating conditions:

- When output voltage is lower than 0.8V, the inductor average current is limited to approximately 0.5A.
- When the output voltage is higher than 0.8V but lower than the input voltage minus 2.0V, the inductor average current limit is increased to approx 1.5A.
- When the output voltage is higher than the input voltage minus 2V but lower than the input voltage, the average inductor current limit is increased to the half of boost current limit (approximately 4A).

When VIN does not exceed 2.8V, the TLV612901 only has two operating conditions during the down mode pre-charge phase. Table 7-1 shows more details for this operation.

The second phase in start-up procedure is boost switching phase. In this operation mode, the output voltage is higher than input voltage, and the average inductor current limit is increased to boost current limit (default 8A).

Using this method, the loading capability during start-up is improved, and this improvement is helpful to reduce the inrush current during start-up. Table 7-1 and Table 7-2 show the relationship between average inductor current limit and output voltage in start-up phase.

Table 7-1. Average Inductor Current Limit Setting During Start-Up (VIN ≤ 2.8V)

PHASE	AVERAGE INDUCTOR CURRENT LIMIT	OUTPUT VOLTAGE
Down mode pre-charge phase	0.5A (typical)	VOUT ≤ 0.8V
	4A (typical)	0.8V < VOUT ≤ VIN
Boost switching phase	8A (typical)	VIN < VOUT

Table 7-2. Average Inductor Current Limit Setting During Start-Up (VIN > 2.8V)

PHASE	INDUCTOR AVERAGE CURRENT LIMIT	OUTPUT VOLTAGE
Down mode pre-charge phase	0.5A (typical)	VOUT ≤ 0.8V
	1.5A (typical)	0.8V < VOUT ≤ VIN – 2.0V
	4A (typical)	VIN – 2.0V < VOUT ≤ VIN
Boost switching phase	8A (typical)	VIN < VOUT

In down mode pre-charge phase, if the output voltage does not reach the input voltage after 1ms, the TLV612901 triggers protection and stops switching. Then the device remains in a waiting state for 19ms before attempting to restart again.

The TLV612901 is able to start up with 2.2V UVLO rising threshold. However, if the load during start-up is so heavy or the output capacitance is so large that the TLV612901 fails to charge the output voltage to target value, the TLV612901 does not start up successfully until the input voltage is increased or the load current is reduced. The total start-up time depends on input voltage, output capacitance and load current.

7.4.2 Operation Mode Setting

The TLV612901 device can be configured (through the Section 8.2) to select the operating mode of the device.

When the EN pin is set to logic high, ENABLE bit (CONFIG[5:6]) = 01 (default value), the device enters normal mode (that is, automatic boost/bypass mode) and enables the output voltage to remain above a pre-defined target voltage.

When the EN pin is set to logic high, ENABLE bit (CONFIG[5:6]) = 10, the device enters forced bypass mode. V_{OUT} follows V_{IN}. The current limit in this mode is defualt 8A (programmable through I^2C). The output voltage is slightly reduced due to voltage drop across the bypass MOSFET. The device consumes only a standby current of 35µA (typical).

When the EN pin is set to logic high, and ENABLE bit (CONFIG[5:6]) = 11 forces the device in shutdown mode, but I^2C block works, with a standby current of typically 16µA. In this mode, true load disconnect between the battery and load prevents current flow from VIN to VOUT, as well as reverse current flow from VOUT to VIN.

When the EN pin is set to logic low forces the device in shutdown mode (regardless of what ENABLE bit is), with a shutdown current of typically 0.55µA. In this mode, true load disconnect between the battery and load prevents current flow from VIN to VOUT, as well as reverse current flow from VOUT to VIN.

Table 7-3. Mode of Operation

EN PIN	ENABLE BIT	OPERATION MODE
Low	xx	Shutdown mode. True load disconnection and output voltage is 0V. The device shutdown current is approximately 0.55µA typical.
High	11	I^2C shutdown mode. Power stage is turned off and output voltage is 0V, but I^2C is active. True load disconnection. The device standby current in this mode is approximately 16µA typical.
High	10	Forced bypass mode. V_{OUT} follows V_{IN}. The device standby current is approximately 35µA typical.
High	00/01 (default 01)	Automatic boost/bypass mode. In boost mode, V_{OUT} = V_{OUT_TAR} (default 5.0V). In bypass mode, V_{OUT} follows V_{IN}.

7.4.3 Bypass Mode

The TLV612901 contains an internal switch for bypassing the DC/DC boost converter during bypass mode. When the input voltage is larger than the preset output voltage, the converter seamlessly transitions into 0% duty cycle operation and the bypass FET is fully turned on.

In auto PFM mode, entry in auto bypass mode is triggered by condition where V_{OUT} > (1 + 0.5%) × V_{OUT_TAR} and V_{IN} > V_{OUT} – 20mV.

In forced PWM mode, the device enters bypass mode when both of the following conditions are met:

- V_{OUT} > (1 + 2%) × V_{OUT_TAR}.
- Seven consecutive cycles of maximum clamped off-time occurs (typical t_{OFF} is 2.25µs of each cycle and total 16µs).

Auto bypass mode exit is triggered by bypass current limit or V_{OUT} < (1 – 3%) × V_{OUT_TAR}.

When ENABLE bit (CONFIG[5:6]) = 10, the device is configured in forced bypass mode. The device enters forced bypass mode when V_{IN} > V_{OUT} + 30mV. And forced bypass mode exit is triggered by the bypass current limit.

In bypass mode, the load (RF PA for instance) is directly supplied from the battery for maximum output power, highest efficiency and lowest possible input-to-output voltage difference. The device consumes only a standby current of 35µA (typical). In bypass mode, the device is protected from short-circuit by a very fast current limit detection scheme.

During this operation, the output voltage follows the input voltage. In bypass mode, due to the presence of the bypass MOSFET, the output voltage drop depends on the input voltage, the R_{DSON} of the bypass MOSFET, and the output current. Use the following equation to calculate the output voltage:

$$V_{OUT} = V_{IN} - \left(R_{DSON(BP)} \times I_{OUT}\right) \quad (4)$$

Conversely, the folloqing equation gives the efficiency in bypass mode:

$$\eta = 1 - R_{DSON(BP)} \frac{I_{OUT}}{V_{IN}} \quad (5)$$

- $R_{DSON(BP)}$ is the typical on-resistance of the bypass FET

During bypass mode, the TLV612901 device has overcurrent and short-circuit protection by a fast current limit detection scheme. If the current in the bypass FET exceeds approximately 8A (programmable through I^2C), the bypass FET is turned off, then the TLV612901 enters into output short-to-ground protection mode. After the overcurrent or short-circuit is released, the TLV612901 goes through the start-up procedure again.

7.4.4 Boost Control Operation

The TLV612901 boost converter is controlled by a hysteretic current mode. This controller regulates the output voltage by keeping the inductor ripple current constant around 1.0A and adjusting the offset of this inductor current depending on the output load. Because the input voltage, output voltage and inductor value all affect the rising and falling slopes of inductor ripple current, the switching frequency is not fixed and is determined by the operation condition.

At light load, the TLV612901 implements three operating modes, auto PFM, forced PWM and ultrasonic mode, to meet different application requirements. The operating mode is set by changing the state of the MODE_CTRL bit through I^2C. When MODE_CTRL = 00, the device operates in auto PFM mode. When MODE_CTRL = 01, the device operates in Ultrasonic mode. When MODE_CTRL = 10 or 11, the device operates in forced PWM mode. For this device, the recommended inductance range is 330nH to 560nH.

7.4.5 Auto PFM Mode

The TLV612901 integrates the power save mode with pulse frequency modulation (auto PFM) to improve the efficiency at the light load. In this mode, if the required average inductor current is lower than the average inductor current defined by this constant ripple, the inductor current goes discontinuously to keep the efficiency high under light load condition. The peak inductor current and the valley inductor current is limited by approximately 1.0A and 0A separately. If the output current in auto PFM mode is no longer supported, the TLV612901 exits auto PFM mode and enters PWM mode.

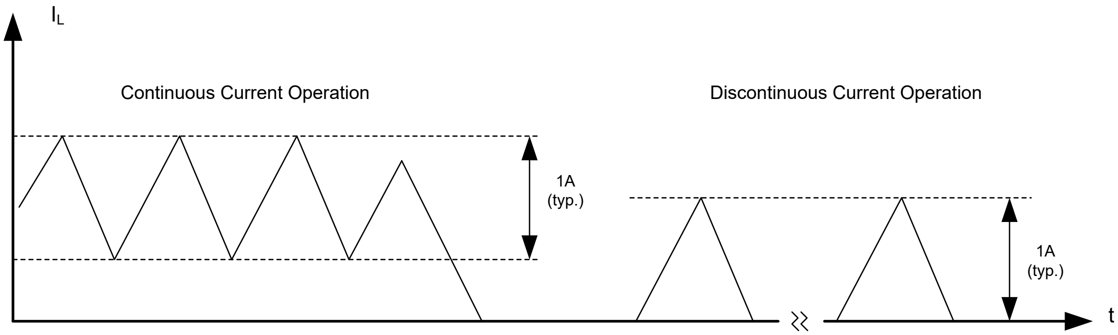


Figure 7-3. Auto PFM Mode

7.4.6 Forced PWM Mode

In forced PWM mode, the TLV612901 keeps the inductor current being continuous for the whole load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and delivers less power from input to output. The high-side FET is not turned off even if the current through the FET goes negative, which makes sure that the inductor current is continuous. Meanwhile, the switching frequency does not change significantly with the load. In this mode, the minimal switching frequency is limited to 375kHz when input voltage is close to output voltage.

7.4.7 Ultrasonic Mode

The ultrasonic mode is a unique control feature that keeps the switching frequency above the acoustic audible frequency toward no load and light load condition. The ultrasonic mode control circuit monitors the switching frequency and keeps the switching frequency above 23kHz to avoid the acoustic band. The output voltage becomes typically 1% higher than PWM operation.

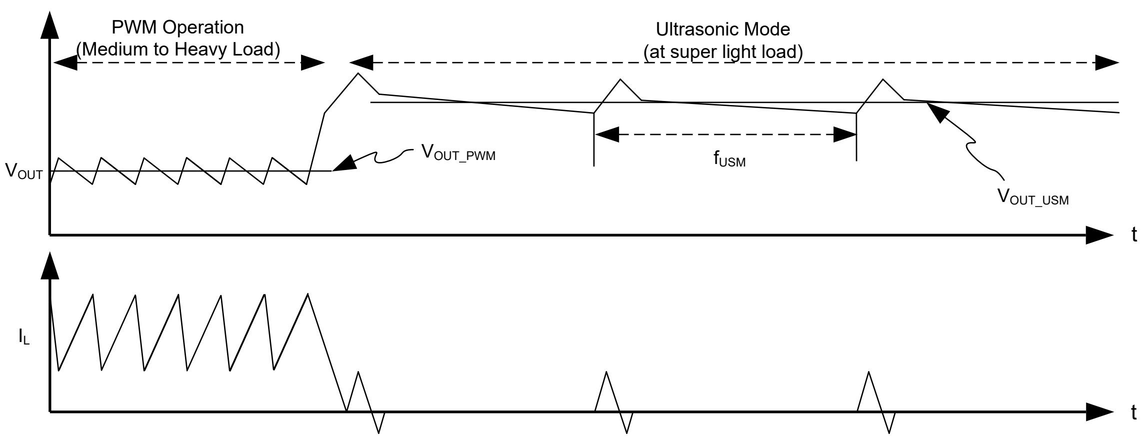


Figure 7-4. Ultrasonic Mode Operation

7.4.8 Output Discharge

The TLV612901 provides an active pulldown resistor to quickly discharge output when the EN is logic low and device in shutdown mode. With this function, the output voltage is connected to ground through internal circuitry, preventing the output from “floating” or entering an undefined state. The output discharge function makes the power on and off sequencing smooth. Pay attention to the output discharge function if use this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground. The output equivalent discharge impedance of TLV612901 is 90Ω (typical).

TLV612901 can modify the status of this function by writing the value of the DISCHG bit through I^2C. When DISCHG = 0, disable output discharge function in I^2C shutdown mode. When DISCHG = 1, enable output discharge function in shutdown mode. The default value of this bit is 1.

7.4.9 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. The I^2C control interface and the output stage of the converter are disabled after the falling V_{IN} trips the undervoltage lockout threshold $V_{UVLO\_falling}$ (1.8V maximum). The device starts operation after the rising V_{IN} trips V_{UVLO_rising} threshold (2.2V maximum).

7.4.10 Current Limit Operation

The TLV612901 device features an average inductor current limit scheme.

In DC/DC boost mode, the TLV612901 device employs an average inductor current limit detection scheme and senses the voltage drop across the synchronous rectifier during the off-time. The average inductor current limit threshold can be set through an I^2C register, and the default value is 8A (typical). When this current limit is reached, if the output current continues to increase, the TLV612901 reduces the output voltage while maintaining the inductor current at the current limit value.

Equation 6 calculates the maximum continuous output current ($I_{OUT(max)}$) before entering current limit (CL).

$$I_{OUT(max)} = I_{LIMIT} \times \left(\frac{V_{IN}}{V_{OUT}}\right) \times \eta \tag{6}$$

where

- η is the efficiency
- $I_{OUT(max)}$ is the maximum output current
- I_{LIMIT} is the current limit of the input side
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

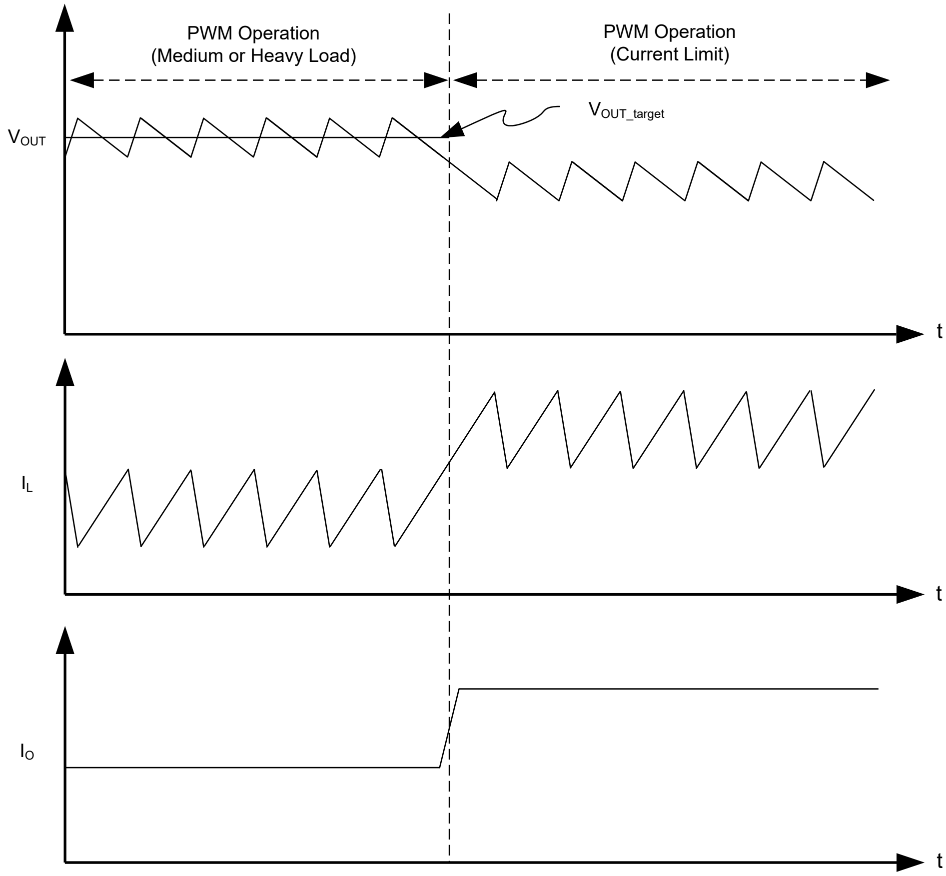


Figure 7-5. Operation Scheme of Current Limit in DC/DC Boost Mode

In bypass mode, the TLV612901 device is protected by a very fast current limit detection scheme. If the current in the bypass FET exceeds approximately 8A, the device turns off the bypass FET after a small delay, ca. 200ns. Then, the device cycles through a start-up procedure.

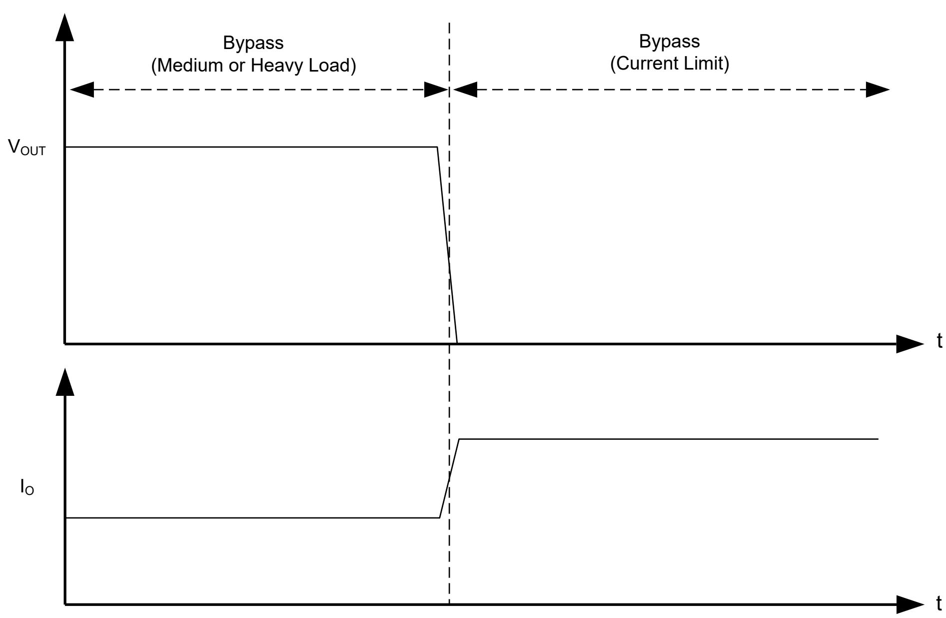


Figure 7-6. Operation Scheme of Current Limit in Bypass Mode

7.4.11 Output Short-to-Ground Protection

The TLV612901 is protected when output is short-to-ground (OSGP). The scheme of output OSGP is same as the scheme in start-up phase.

When output is short, the TLV612901 turns off and cycles through a start-up procedure. After the overcurrent or short circuit is released, the TLV612901 successfully achieves soft start then regulates the output voltage.

The hiccup protection mode can be disabled through I²C.

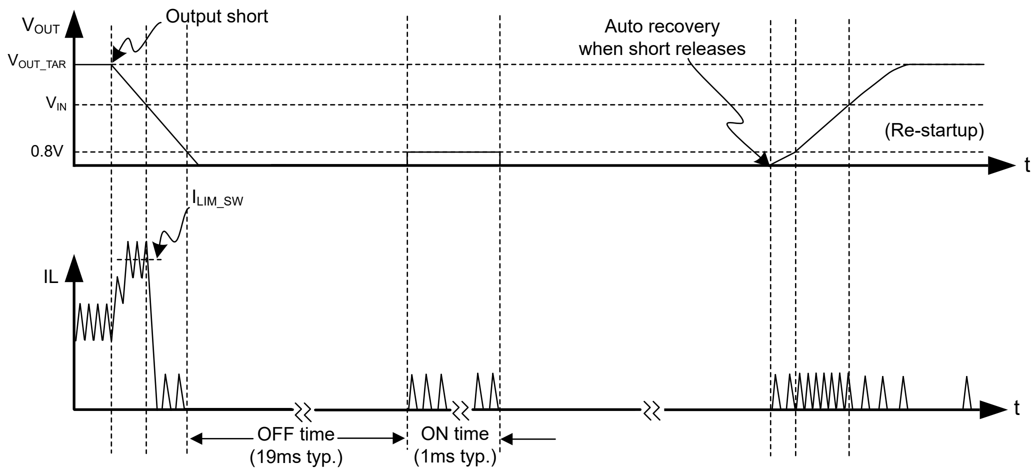


Figure 7-7. Hiccup Mode in OSGP

7.4.12 Overvoltage Protection

The TLV612901 has an output overvoltage protection (OVP). When the output voltage is above 5.58V typically, the device stops switching. After the output voltage falls 0.1V below the OVP threshold, the device resumes operating again.

7.4.13 Thermal Shutdown

The device goes into thermal shutdown once the junction temperaturem (T_J) exceeds 165°C. In this mode, the bypass, high-side, and low-side MOSFETs are turned off and the I²C block is active. When the junction temperature falls below the thermal shutdown minus the hysteresis (20°C typical), the device restarts and regulates the output voltage.

7.4.14 Power-Good Indication Status

The TLV612901 also provides a power-good output bit (PG bit in I²C) for signaling the system when the regulator has successfully completed start-up and no faults have occurred. Power good also functions as an flag for excessive die temperature and overload conditions.

- PG is set (bit = 1) when the start-up sequence is successfully completed.
- PG is reset (bit = 0) when the output voltage falls approximately 50mV below the regulation level in boost mode.
- PG is set (bit = 1) when the device is operating in auto bypass mode (that is ENABLE bit = 00 or 01 and V_{IN} > V_{OUT}).
- PG is not defined when the device is operating in forced bypass mode (that is ENABLE bit = 10).
- PG is reset (bit = 0) when the device is in shutdown mode (that is ENABLE bit = 11).
- PG is reset (bit = 0) when the device is in short protection mode, thermal shutdown mode.

7.5 Programming

The TLV612901 uses I²C interface for flexible converter parameter programming. I²C is a bi-directional 2-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). I²C devices can be considered as controllers or targets when performing data transfers. A controller is the device that initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a target.

The TLV612901 operates as a target device with address 75h when ADDR is logic low. Receiving control inputs from the controller device like a microcontroller or a digital signal processor reads and writes the internal registers 00h through 07h. The I^{2}C interface of the TLV612901 supports both standard mode (up to 100kbit/s) and fast mode plus (up to 1000kbit/s). Both SDA and SCL must be connected to the positive supply voltage through current sources or pullup resistors. When the bus is free, both lines are in high voltage.

7.5.1 Data Validity

The data on the SDA line must be stable during the high level period of the clock. The high-level or low-level state of the data line can only change when the clock signal on the SCL line is low level. One clock pulse is generated for each data bit transferred.

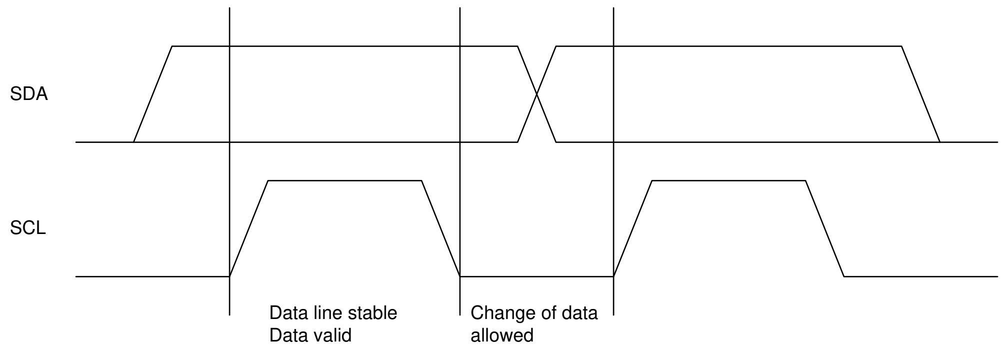


Figure 7-8. I^{2}C Data Validity

7.5.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A high-level to low-level transition on the SDA line while SCL is at high level defines a START condition. A low-level to high-level transition on the SDA line when the SCL is at high level defines a STOP condition.

START and STOP conditions are always generated by the controller. The bus is considered busy after the START condition and free after the STOP condition.

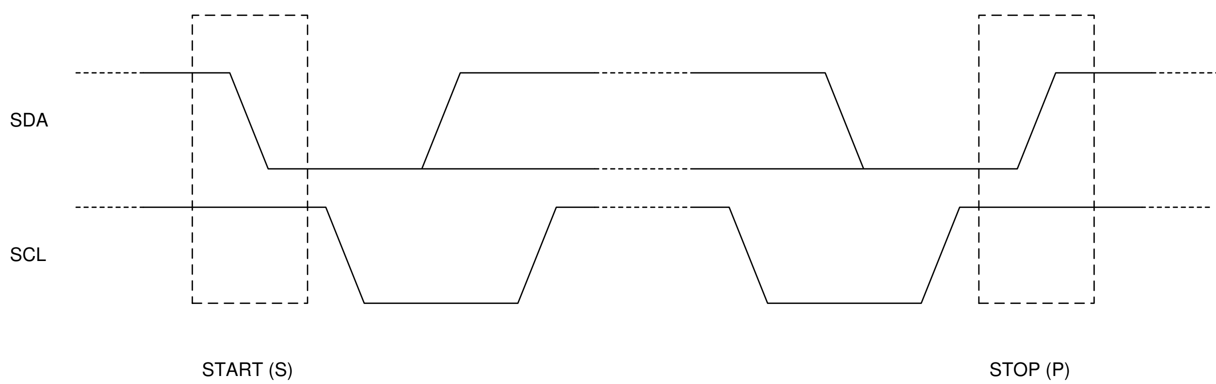


Figure 7-9. I^{2}C START and STOP Conditions

7.5.3 Byte Format

Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a target cannot receive or transmit another complete byte of data until the target has performed some other function, the target can hold the clock line SCL low to force the controller into a wait state (clock stretching). Data transfer then continues when the target is ready for another byte of data and release the clock line SCL.

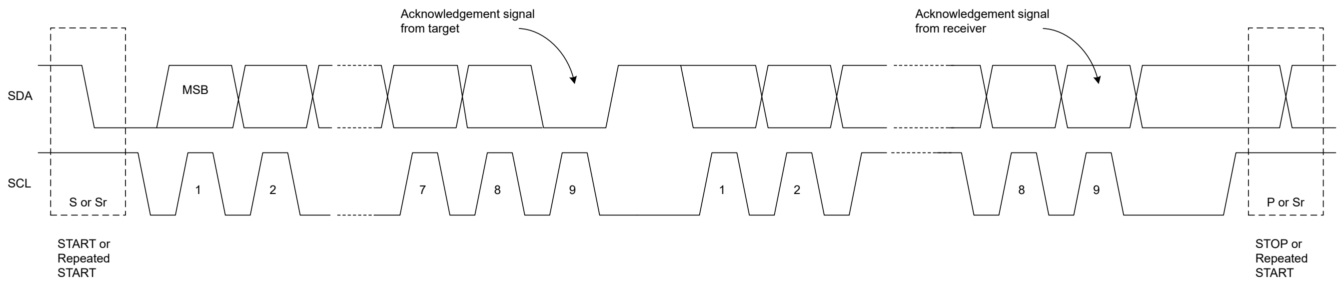


Figure 7-10. Byte Format

7.5.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte is successfully received and another byte can be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the controller.

The transmitter releases the SDA line during the acknowledge clock pulse, allowing the receiver to pull the SDA line low and maintain a stable low level while the clock pulse is high.

The Not Acknowledge signal is when SDA remains high level during the ninth clock pulse. The controller can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.5.5 Target Address and Data Direction Bit

After the START, a target address is sent. This address is seven bits long followed by the eighth bit as a data direction bit (bit R/$\overline{W}$). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

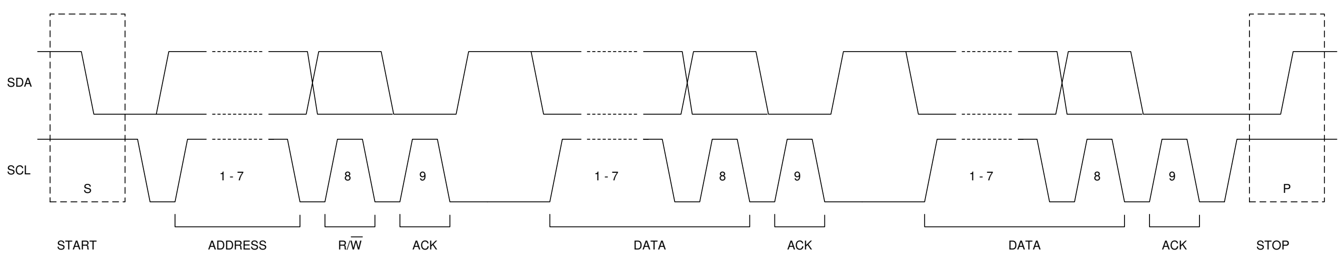


Figure 7-11. Target Address and Data Direction

7.5.6 Single Read and Write

Figure 7-12 and Figure 7-13 show the single-byte write and single-byte read format of the I^{2}C communication.

1	7	1	1	8	1	8	1	1
S	Target Address	0	ACK	Register Address	ACK	Data to Address	ACK	P

Figure 7-12. Single-byte Write

Figure 7-13. Single-byte Read

If the register address is not defined, the TLV612901 sends back NACK and goes back to the idle state.

7.5.7 Multi-Read and Multi-Write

The TLV612901 supports multi-read and multi-write.

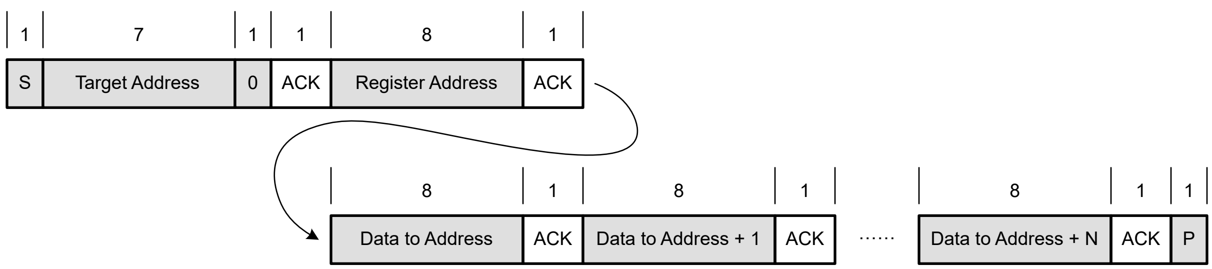


Figure 7-14. Multi-byte Write

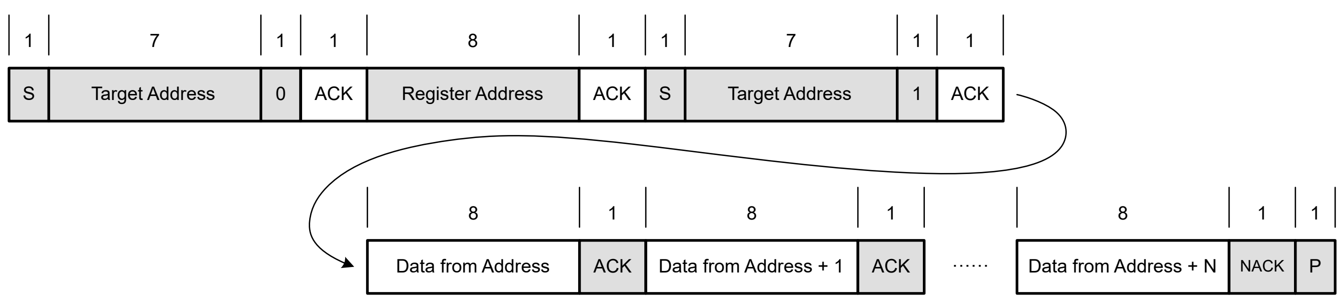


Figure 7-15. Multi-byte Read

8 Register Maps

The Configuration Memory Map lists the memory-mapped registers for the device registers. All register offset addresses not listed in The Configuration Memory Map should be considered as reserved locations, and the register contents should not be modified.

Table 8-1. Device Registers

Register Address	Register Name	Description
00h	DeviceID Register	Sets Manufacturer ID & Device version ID
01h	CONFIG Register	Sets miscellaneous configuration bits
02h	VOUTFLOORSET Register	Sets the floor output voltage threshold boost / bypass mode change
03h	ILIMBSTSET Register	Sets the input current limit in dc/dc boost mode
04h	VOUTROOFSET Register	Sets the roof output voltage threshold boost / bypass mode change (only valid when GPIO is configured as VSEL function)
05h	STATUS Register	Returns status flags
06h	ILIMPTSET Register	Sets the input current limit in bypass mode
07h	BSTLOOP Register	Sets the internal compensation loop

8.1 DeviceID Register

Memory location: 0x00

Table 8-2. VersionID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	Manufacture ID	R	0111	Manufacturer ID.
3:0	Device ID	R	0000	Device version ID.

8.2 CONFIG Register

Memory location: 0x01

Table 8-3. CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0	Device reset bit. 0: Normal operation. 1: Default values are set to all internal registers. The device operation is cycled (ON-OFF-ON), that is, the converter is disabled for a short period of time and the output is reset.
6:5	ENABLE	R/W	01	Device enable bit (refer to Operation Mode Setting). 00 or 01: Device operates in automatic boost or bypass mode. 10: Device forced in forced bypass mode. 11: Device is in shutdown mode but I^2C active.
4	HICCUP_MODE	R/W	1	Hiccup mode enable bit. 0 : Hiccup mode disable 1 : Hiccup mode enable
3	DISCHG	R/W	1	Output discharge enable bit. 0: Disable VOUT discharge when the device is in I^2C shutdown mode. 1: Enable VOUT discharge when the device is in shutdown mode. (refer to Output Discharge)
2	SSFM	R/W	0	Spread modulation control. 0: Spread spectrum modulation is disabled. 1: Spread spectrum modulation is enabled in forced PWM mode
1:0	MODE_CTRL	R/W	00	Device light load functional modes bits. 00: Device operates in Auto PFM Mode. 01: Device operates in Ultrasonic Mode. 10 or 11: Device operates in Forced PWM Mode.

8.3 VOUTFLOORSET Register

Memory location: 0x02

Table 8-4. VOUTFLOORSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	00	Reserved bit. These bits are reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
5:0	VOUTFLOOR_TH	R/W	1	Output voltage threshold, dc/dc boost / bypass mode change.
		R/W	0	
		R/W	1	000000: 2.85V 000001: 2.90V 000010: 2.95V 000011: 3.00V 000100: 3.05V 000101: 3.10V 000110: 3.15V 000111: 3.20V 001000: 3.25V 001001: 3.30V 001010: 3.35V 001011: 3.40V 001100: 3.45V 001101: 3.50V 001110: 3.55V 001111: 3.60V 010000: 3.65V 010001: 3.70V 010010: 3.75V 010011: 3.80V 010100: 3.85V 010101: 3.90V 010110: 3.95V 010111: 4.00V 011000: 4.05V 011001: 4.10V 011010: 4.15V 011011: 4.20V 011100: 4.25V 011101: 4.30V 011110: 4.35V 011111: 4.40V 100000: 4.45V 100001: 4.50V 100010: 4.55V 100011: 4.60V 100100: 4.65V 100101: 4.70V 100110: 4.75V 100111: 4.80V 101000: 4.85V 101001: 4.90V 101010: 4.95V 101011: 5.00V 101100: 5.05V 101101: 5.10V 101110: 5.15V 101111: 5.20V 110000: 5.25V 110001: 5.30V 110010: 5.35V 110011: 5.40V 110100: 5.45V 110101: 5.50V 110110: 2.80V 110111: 2.75V 111000: 2.70V 111001: 2.65V 111010: 2.60V 111011: 2.55V 111100: 2.50V 111101: 2.45V 111110: 2.40V 111111: 2.35V
		R/W	0	
		R/W	1	
		R/W	1	

8.4 ILIMBSTSET Register

Memory location: 0x03

Table 8-5. ILIMBSTSET Register Field Descriptions

<table>
<tr><th>Bit</th><th>Field</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>7</td><td>RESERVED</td><td>R/W</td><td>0</td><td>Reserved bit.
This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.</td></tr>
<tr><td>6</td><td>RESERVED</td><td>R/W</td><td>0</td><td>Reserved bit.
This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.</td></tr>
<tr><td>5</td><td>RESERVED</td><td>R/W</td><td>0</td><td>Reserved bit.
This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.</td></tr>
<tr><td>4</td><td>RESERVED</td><td>R/W</td><td>0</td><td>Reserved bit.
This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.</td></tr>
<tr><td rowspan="4">3:0</td><td rowspan="4">ILIM_BOOST</td><td>R/W</td><td>0</td><td rowspan="4">Inductor average current limit in dc/dc boost mode.
0000: 5A
0001: 5.5A
0010: 6A
0011: 6.5A
0100: 7A
0101: 7.5A
0110: 8A
0111: 8.5A
1000: 9A
1001: 9.5A
1010: 10A
1011: 10.5A
1100: 11A
1101: 3.5A
1110: 4A
1111: 4.5A</td></tr>
<tr><td>R/W</td><td>1</td></tr>
<tr><td>R/W</td><td>1</td></tr>
<tr><td>R/W</td><td>0</td></tr>
</table>

8.5 VOUTROOFSET Register

Memory location: 0x04

Table 8-6. VOUTROOFSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	00	Reserved bit. These bits are reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
5:0	VOUTROOF_TH	R/W	1	Output voltage threshold, dc/dc boost / bypass mode change.
		R/W	0	
		R/W	1	000000: 2.85V 100000: 4.45V 000001: 2.90V 100001: 4.50V 000010: 2.95V 100010: 4.55V 000011: 3.00V 100011: 4.60V 000100: 3.05V 100100: 4.65V 000101: 3.10V 100101: 4.70V 000110: 3.15V 100110: 4.75V 000111: 3.20V 100111: 4.80V 001000: 3.25V 101000: 4.85V 001001: 3.30V 101001: 4.90V 001010: 3.35V 101010: 4.95V 001011: 3.40V 101011: 5.00V 001100: 3.45V 101100: 5.05V 001101: 3.50V 101101: 5.10V 001110: 3.55V 101110: 5.15V 001111: 3.60V 101111: 5.20V 010000: 3.65V 110000: 5.25V 010001: 3.70V 110001: 5.30V 010010: 3.75V 110010: 5.35V 010011: 3.80V 110011: 5.40V 010100: 3.85V 110100: 5.45V 010101: 3.90V 110101: 5.50V 010110: 3.95V 110110: 2.80V 010111: 4.00V 110111: 2.75V 011000: 4.05V 111000: 2.70V 011001: 4.10V 111001: 2.65V 011010: 4.15V 111010: 2.60V 011011: 4.20V 111011: 2.55V 011100: 4.25V 111100: 2.50V 011101: 4.30V 111101: 2.45V 011110: 4.35V 111110: 2.40V 011111: 4.40V 111111: 2.35V
		R/W	1	
		R/W	1	
		R/W	1	

8.6 STATUS Register

Memory location: 0x05

Table 8-7. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TSD	R	0	Thermal shutdown status bit. 0: Normal operation. 1: Thermal shutdown tripped. This flag is reset after readout.
6	CRC_PASS	R	1	OTP test status bit. 0: OTP test failed. This bit is reserved for Test Engineers in TI. 1: Normal operation. This flag is reset after readout.
5	VOUT_START	R	1	Vout status bit. 0: Vout < 0.8V. 1: Vout > 0.8V. This flag is reset after readout.
4	OPMODE	R	1	Device mode of operation status bit. 0: Device operates in bypass mode. 1: Device operates in boost mode.
3	ILIMPT	R	0	Current limit status bit (bypass mode). 0: Normal operation. 1: Indicates that the bypass FET current limit has triggered. This flag is reset after readout.
2	ILIMBST	R	0	Current limit status bit (dc/dc boost mode). 0: Normal operation. 1: Indicates that the average input current limit has triggered for 4ms in dc/dc boost mode. This flag is reset after readout.
1	FL_LD	R	0	Current limit status bit (dc/dc boost mode). 0: Normal operation. 1: Indicates that the average input current limit has triggered in dc/dc boost mode. This flag is reset after readout.
0	PGOOD	R	1	Power Good status bit. 0: Indicates the output voltage is out of regulation. 1: Indicates the output voltage is within its nominal range. This bit is set to 1 if the converter operates in auto bypass mode.

8.7 ILIMPTSET Register

Memory location: 0x06

Table 8-8. ILIMPTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
6	RESERVED	R/W	0	Reserved bit. This bit is reserved for future use. During write operations data intended for this bit is ignored, and during read operations 0 is returned.
5:3	ILIM_FPT	R/W R/W R/W	0 1 0	Current limit in forced bypass mode. 000: 4A 001: 6A 010: 8A 011: 10A 100 to 111: Not Defined.
2:0	ILIM_APT	R/W R/W R/W	0 1 0	Current limit in auto bypass mode. 000: 4A 001: 6A 010: 8A 011: 10A 100 to 111: Not Defined.

8.8 BSTLOOP Register

Memory location: 0x07

Table 8-9. BSTLOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	TI_internal	R/W	01000	TI internal use. Do not read or write.
2:0	RC	R/W	000	Compensation resistor set bit. 000: 200k 001: 250k 010: 100k 011: 150k 100: 400k 101: 450k 110: 300k 111: 350k

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TLV612901 is typically used as a high-power pre-regulator in single-cell battery-powered systems that require a regulated 5.0V output and high output current capability.

In boost applications, the device maintains the regulated output voltage when the input voltage is lower than the target output voltage. The device can also operate in bypass mode to maximize efficiency.

Use the following design procedure to select the external components for the TLV612901.

9.2 Typical Application

9.2.1 TLV612901 With 2.5V – 4.85V V_{IN}, 5.0V V_{OUT}, 3A Output Current

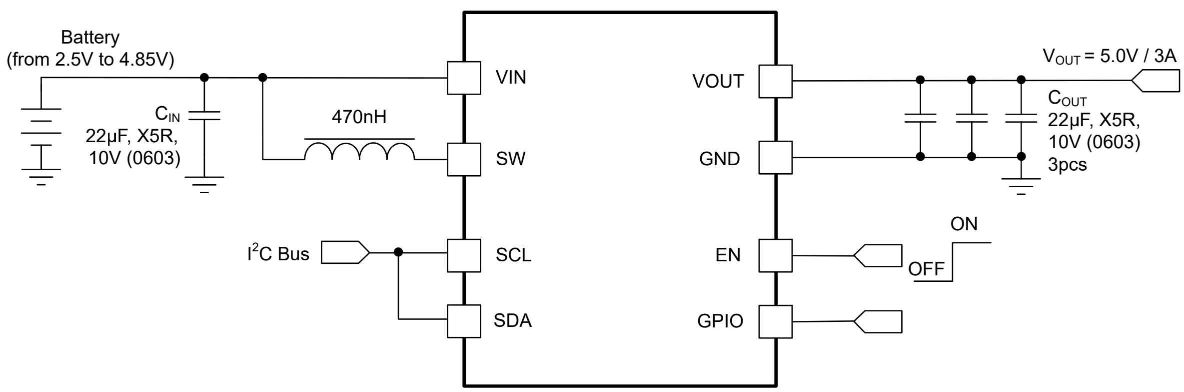


Figure 9-1. TLV612901 With 2.5V – 4.85V V_{IN}, 5.0V V_{OUT}, 3A Output Current

9.2.1.1 Design Requirements

Table 9-1. Design Parameters

REFERENCE	DESCRIPTION	SAMPLE VALUES
V_{IN}	Input voltage range	2.5V – 4.85V
V_{OUT}	Output voltage range at boost mode	V_{OUT} = 5.0V
	Output voltage range bypass mode	$V_{OUT} = V_{IN} – I_{OUT} × R_{DS(ON)\_BYP}$
I_{OUT}	Output current	3A

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor are required. Selecting an inductor with a saturation current rating higher than the possible peak current flowing through the power switches is advisable.

The inductor peak current varies as a function of the load and the input and output voltages. Equation 7 calculates the inductor peak current.

$$I_{L(PEAK)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \text{ with } D = 1 - \frac{V_{IN}}{V_{OUT}} \tag{7}$$

Selecting an inductor with insufficient saturation performance leads to excessive peak current in the converter. This current can eventually harm the device and reduce the reliability of the device.

When selecting the inductor, as well as the inductance, parameters of importance are: maximum current rating, series resistance, and operating temperature. Enable the inductor DC current rating to be greater than the maximum input average current. See also *Current Limit Operation*.

$$I_{L(DC)} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{\eta} \times I_{OUT} \tag{8}$$

The TLV612901 series of step-up converters have been optimized to operate with a effective inductance in the range of 330nH to 560nH. Larger or smaller inductor values are used to optimize the performance of the device for specific operating conditions. See also *Checking Loop Stability*.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

TI recommends the following inductor series from different suppliers with TLV612901.

Table 9-2. List of Inductors

SERIES	L (nH)	DIMENSIONS (in mm)	DC INPUT CURRENT LIMIT SETTING	MANUFACTURER(1)
HTTO32251T-R47MMR	470	3.2 × 2.5 × 1.0 maximum height	≤ 8600mA	Cyntec
744383340047	470	3.4 × 3.4 × 1.2 maximum height	≤ 9400mA	Wurth Elektronik
XGL4012-451	450	4.0 × 4.0 × 1.2 maximum height	≤ 9900mA	Coilcraft
DFE32CAHR47MR0	470	3.2 × 2.5 × 2.0 maximum height	≤ 8700mA	Murata

(1) See the *Third-Party Products Disclaimer*.

9.2.1.2.2 Output Capacitor

For the output capacitor, TI recommends to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If a large capacitor cannot be placed close to the IC, TI strongly recommends to use a small ceramic capacitor in parallel next to the IC. To get an estimate of the recommended minimum output capacitance, use Equation 9.

$$C_{MIN} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \tag{9}$$

where f is the switching frequency and ΔV is the maximum allowed output ripple.

Use an MLCC capacitor with twice the value of the calculated minimum because of the DC bias effects. This capacitor is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

For most of the application cases, TI recommends 3pcs 22µF X5R 10V (0603) MLCC capacitors to use. In applications featuring high (pulsed) load currents (for example: 5V / 3A), TI recommends increasing the output capacitors to ensure sufficient effective output capacitance, such as using 4pcs 22µF X5R 10V (0603) MLCCs.

High cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the effective capacitance of the device. Therefore, the right capacitor value must be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and effective capacitance of the capacitor. For instance, a 22µF X5R 6.3V (0603) MLCC capacitor typically shows an effective capacitance of less than 10µF (under 3.4V DC bias and 20mV AC bias condition).

9.2.1.2.3 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as multilayer ceramic capacitors have extremely low ESR and are available in small footprints. Place capacitors as close as possible to the device. A 22µF input capacitor is sufficient for most applications. To further reduce input current ripple without limitations, use larger values.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output induces ringing at the V_{IN} pin. This ringing couples to the output and be mistaken as loop instability or damage the part. To reduce ringing that occurs between the inductance of the power source leads and C_{IN}, place "bulk" capacitance (electrolytic or tantalum) between C_{IN} and the power source.

9.2.1.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These signals are the basic signals that must be measured when evaluating a switching converter. Signs of instability in the regulation loop include switching waveforms showing large duty cycle jitter or the output voltage or inductor current showing oscillations. This event is often a result of board layout or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the N-channel MOSFET, enable the output capacitor to supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times$ ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to the steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, monitor V_{OUT} for settling time, overshoot or ringing that helps judge the stability of the converter. Without any ringing, the loop has typically more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (that is, MOSFET $r_{DS(on)}$) that are temperature dependent, the loop stability analysis must be done over the input voltage range, load current range, and temperature range.

The TLV612901 series of step-up converters are optimized to operate with a effective inductance in the range of 330nH to 560nH and with the effective output capacitance in the range of 15µF to 100µF. The internal compensation is optimized for an output filter of L = 470nH and effective C_O = 15µF.

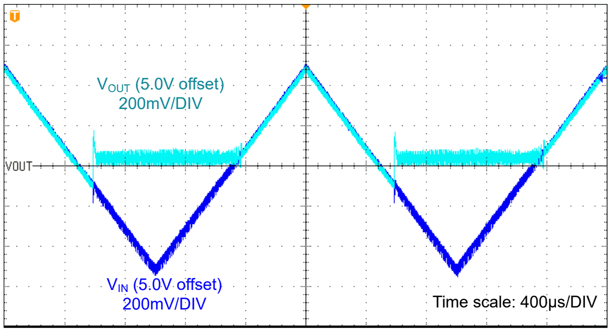
Table 9-3. Component List

REFERENCE	DESCRIPTION	PART NUMBER, MANUFACTURER[1]
C_{IN}	22µF, 10V, 0603, X5R ceramic	GRM187R61A226ME15D
C_{OUT}	3 × 22µF, 10V, 0603, X5R ceramic	3 × GRM187R61A226ME15D
L	450nH, 13.8mΩ, 4.0mm × 4.0mm × 1.2mm	XGL4012-451

(1) See the *Third-Party Products Disclaimer*.

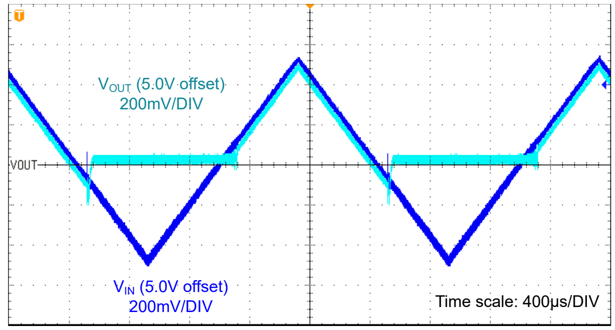
9.2.1.3 Application Curves

Typical condition V_{IN} = 2.5V to 4.85V, V_{OUT_TAR} = 5.0V, T_J = 25°C, unless otherwise noted



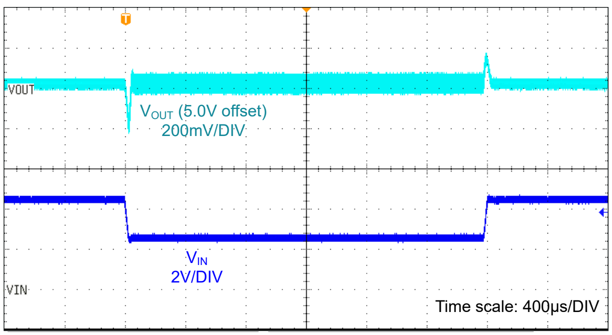
V_{OUT_TAR} = 5.0V T_A = 25°C   Auto PFM   Load = 100mA

Figure 9-2. Boost to Bypass Mode Exit / Entry



V_{OUT_TAR} = 5.0V T_A = 25°C   Auto PFM   Load = 3A

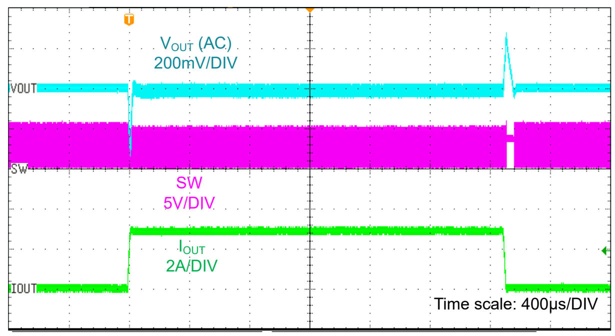
Figure 9-3. Boost to Bypass Mode Exit / Entry



V_{OUT_TAR} = 5.0V T_A = 25°C   Auto PFM   Load = 3A

VIN = 2.7V to 4.5V with 20µs slew rate

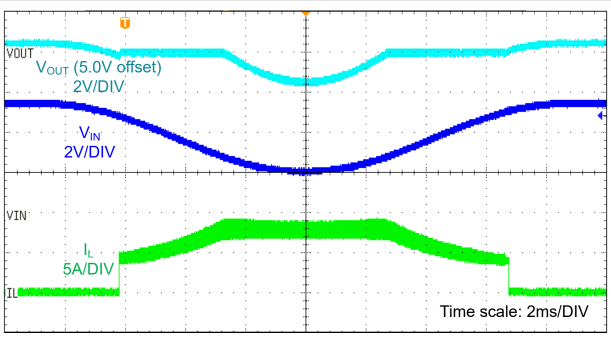
Figure 9-4. Line Transient Response



V_{OUT_TAR} = 5.0V V_{IN} = 3.6V   Auto PFM

Load = 0.1A - 3A, 0.2A/µs slew rate

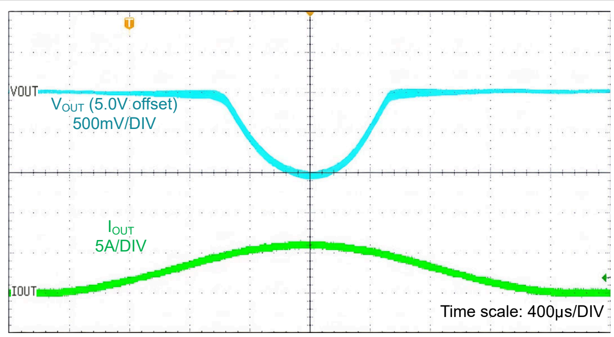
Figure 9-5. Load Transient Response



V_{OUT_TAR} = 5.0V T_A = 25°C   Auto PFM   Load = 4A

VIN = 5.5V to 2.2V sweep

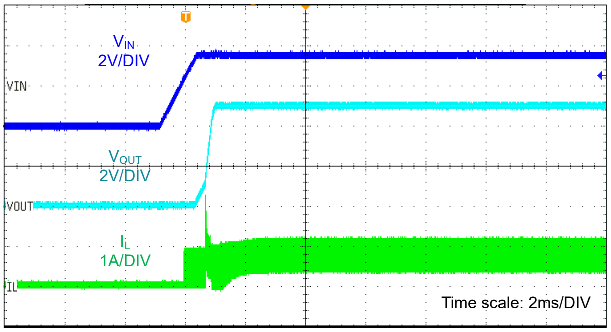
Figure 9-6. Line Sweep



V_{OUT_TAR} = 5.0V V_{IN} = 3.6V   Auto PFM

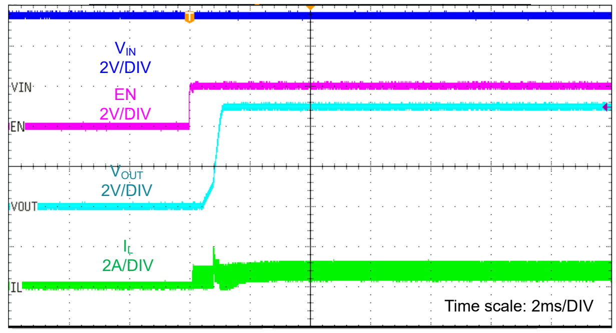
Load = 0A to 6A sweep

Figure 9-7. Load Sweep



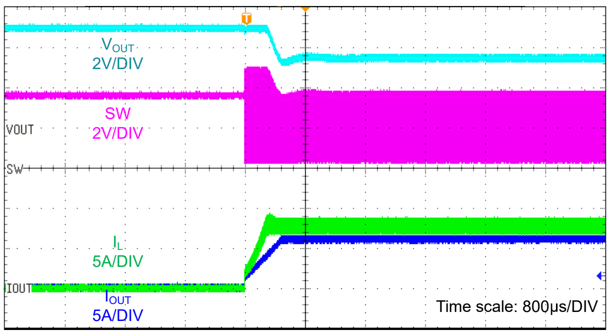
V_{OUT_TAR} = 5.0V V_{IN} = 3.6V Auto PFM 10Ω Load

Figure 9-8. Start-Up by V_{IN}



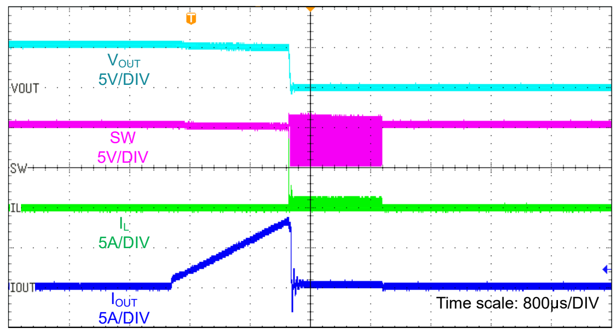
V_{OUT_TAR} = 5.0V V_{IN} = 3.6V Auto PFM 10Ω Load

Figure 9-9. Start-Up by EN



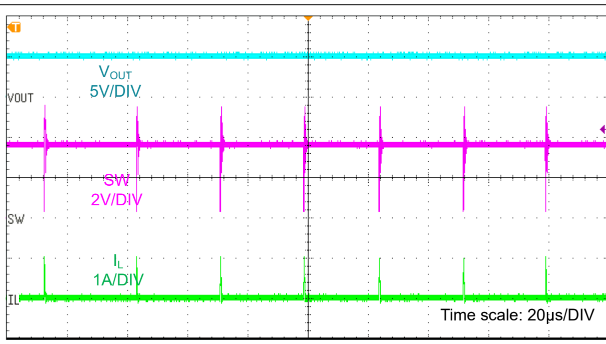
V_{IN} =3.6V Auto PFM Load = 0A to 6A

Figure 9-10. Current Limit Operation at Boost Mode



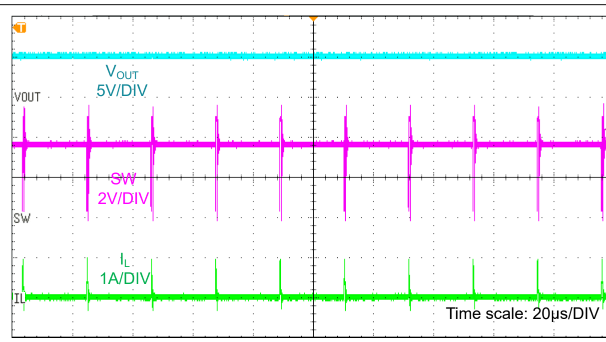
V_{IN} = 5.2V Auto PFM Load = 2A to 10A

Figure 9-11. Current Limit Operation at Bypass Mode



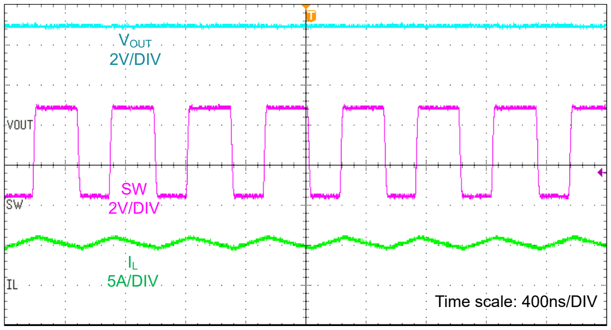
V_{OUT_TAR} = 5.0V V_{IN} = 3.6V Auto PFM Load = 5mA

Figure 9-12. Switching Waveform at Light Load



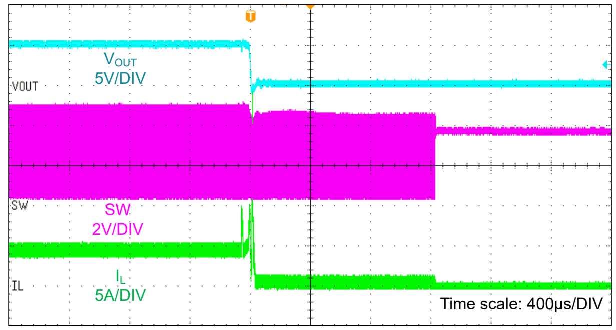
V_{OUT_TAR} = 5.0V V_{IN} = 3.6V USM Load = 5mA

Figure 9-13. Switching Waveform at Light Load



V_{OUT_TAR} = 5.0V V_{IN} = 3.6V Auto PFM Load = 3A

Figure 9-14. Switching Waveform at Heavy Load



V_{OUT_TAR} = 5.0V V_{IN} = 3.6V Auto PFM Load = 3A

Figure 9-15. Output Short to Ground Protection

9.3 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 1.8V and 5.5V. Please ensure the input supply is well regulated. If the input supply is located more than a few inches from the TLV612901 converter, additional bulk capacitance is required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47µF is a typical choice.

9.4 Layout

9.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high current, layout is an important design step. If the layout is not carefully done, the regulator can suffer from instability and noise problems. Because the TLV612901 operates with very fast switching rise and fall times, high-frequency noise radiation (such as EMI) can be generated. Therefore, proper layout of the high-frequency switching path is critical. During layout, minimize the length and area of all traces connected to the SW pin, and use a ground plane under the switching regulator. This action helps minimize interlayer coupling and optimize the high-frequency switching path.

The input capacitor must be close to the VIN pin and PGND pin to reduce the I_{input} supply ripple. The power paths of VOUT, output capacitor and PGND must be as small as possible to reduce parasitic inductance.

Due to the device high power density, thermal management must be carefully considered during layout design. The SW, VOUT, and PGND pins, which improve the thermal capabilities of the package, must be soldered to a large copper polygon. Additionally, using thermal vias underneath the SW pin can further improve thermal performance.

Additionally, consider the effects of PCB parasitics during layout. Figure 9-16 shows the continuous current path and discontinuous current path in TLV612901. The blue solid line represents the continuous current path and the red dashed line represents the discontinuous current path. Figure 9-17 shows the PCB parasitic inductors in discontinuous current path. The loop formed by power MOSFET Q_1, power MOSFET Q_2, output capacitor C_{OUT} must be minimized as short as possible because the PCB parasitic inductors in these high di/dt current paths generate high voltage spikes at output and across power MOSFETs. The spikes and ringing at switch node SW is the source of EMI and can cause power MOSFET overvoltage damage. To minimize the influences of PCB parasitic inductors Lpara1 and Lpara2, a low ESL and ESR X5R or X7R dielectric ceramic capacitor C_{OUT1} is better to be placed as close as possible to the VOUT pin and GND pin of TLV612901.

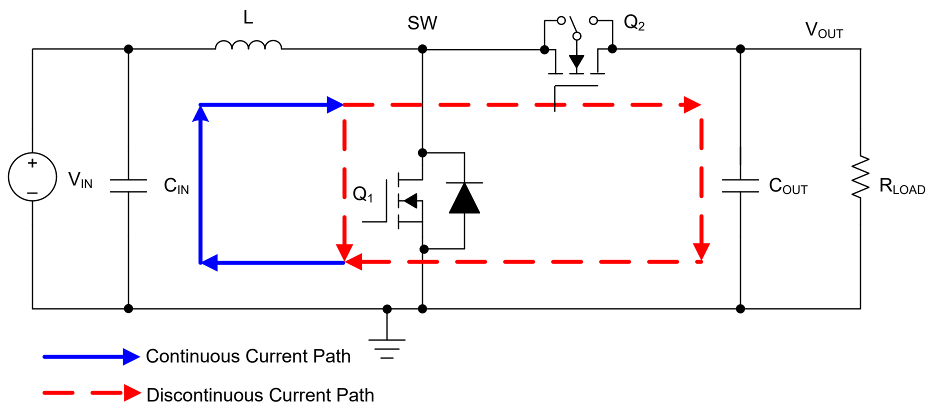


Figure 9-16. Continuous and Discontinuous Current Paths

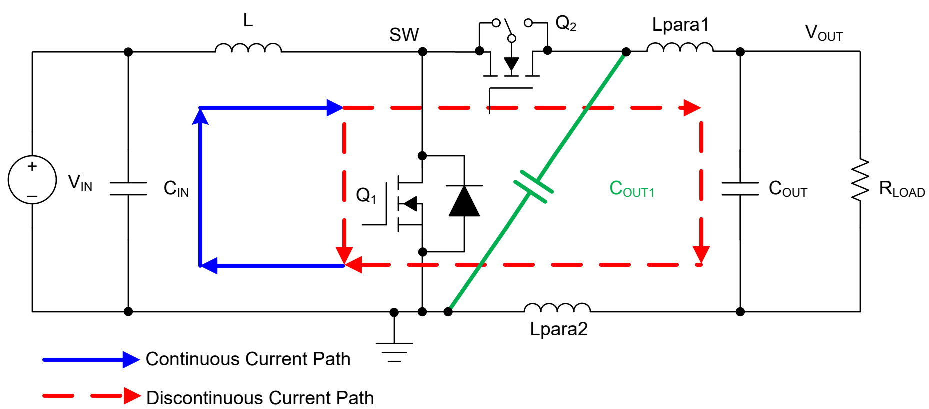


Figure 9-17. PCB Parasitic Inductors in Discontinuous Current Paths

9.4.2 Layout Example

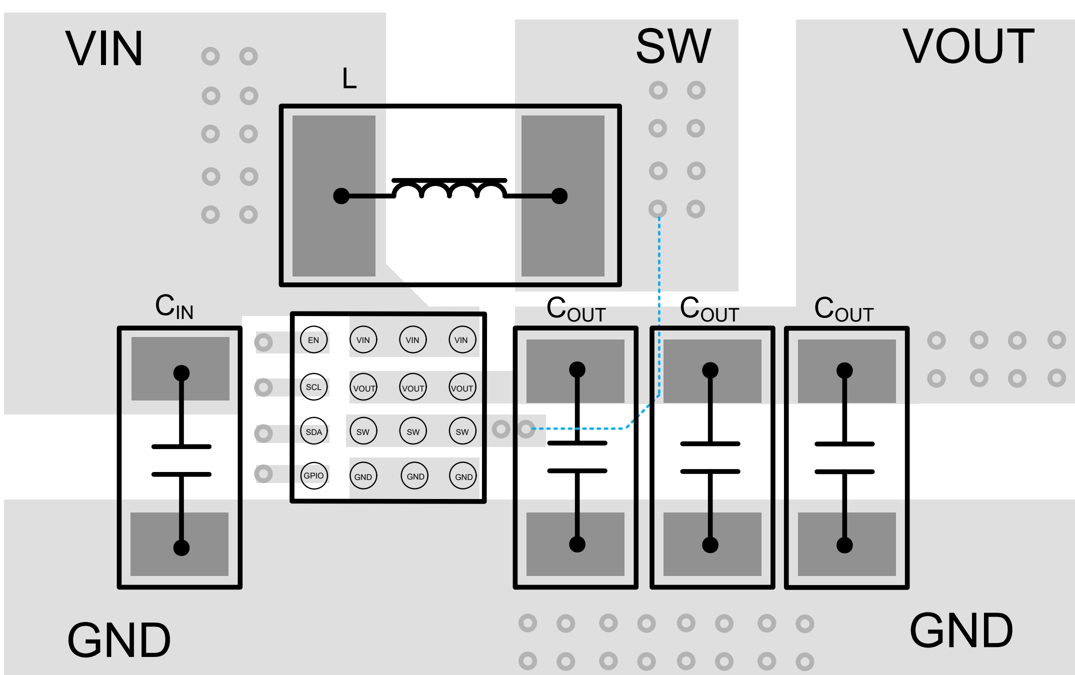


Figure 9-18. Suggested Layout (Top)

9.4.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The following lists three basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The importance of power demand in portable designs is ever-growing, leading designers to select what is best between efficiency, power dissipation, and design size. Due to integration and miniaturization, junction temperature increases significantly which can lead to bad application behaviors (that is, premature thermal shutdown or worst case reduce device reliability).

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, pay special attention to thermal dissipation issues in board design. Keep the device operating junction temperature (T_J) below 125°C.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

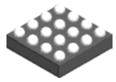
11 Revision History

DATE	REVISION	NOTES
August 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

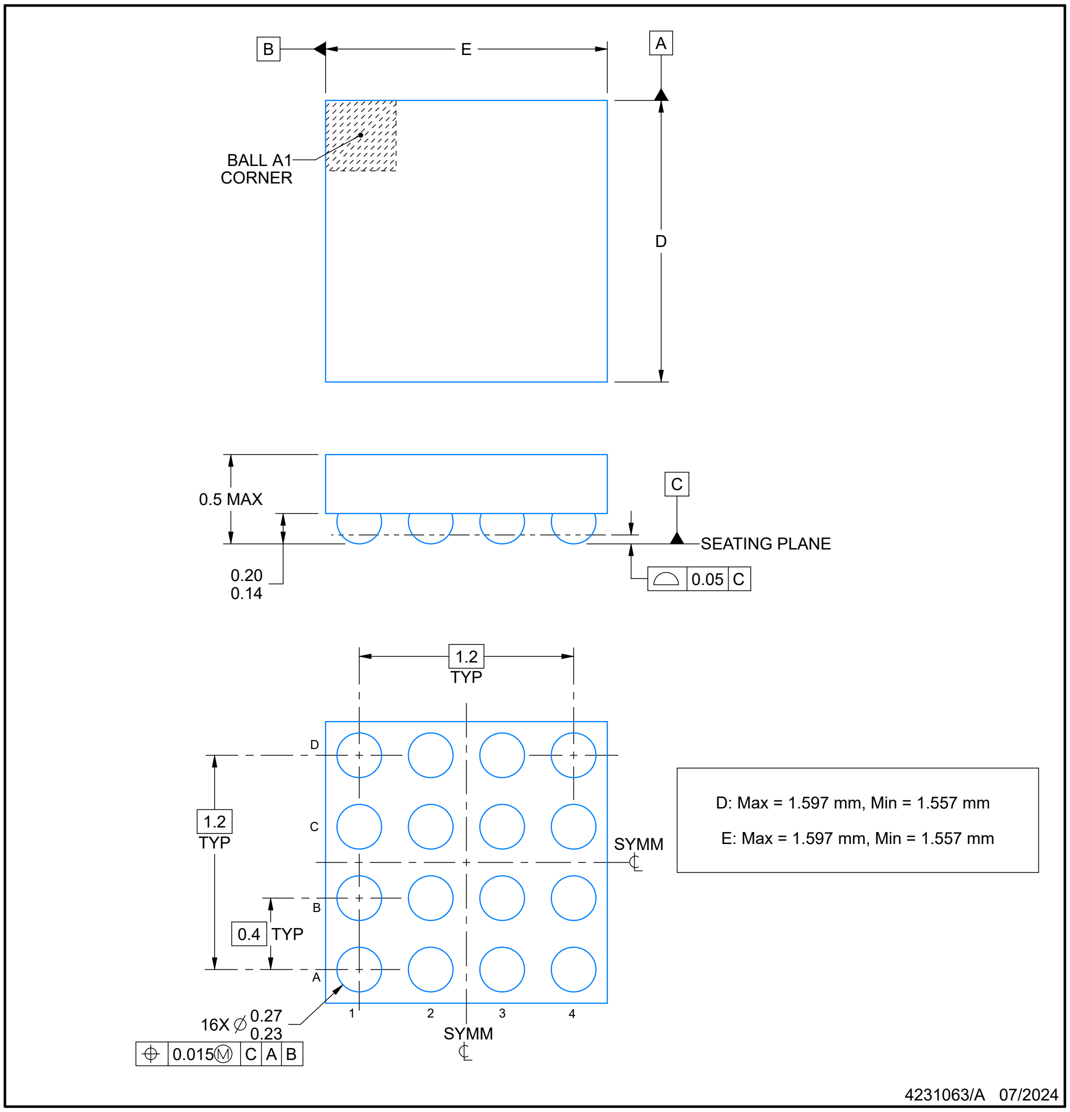
PACKAGE OUTLINE



YBG0016-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



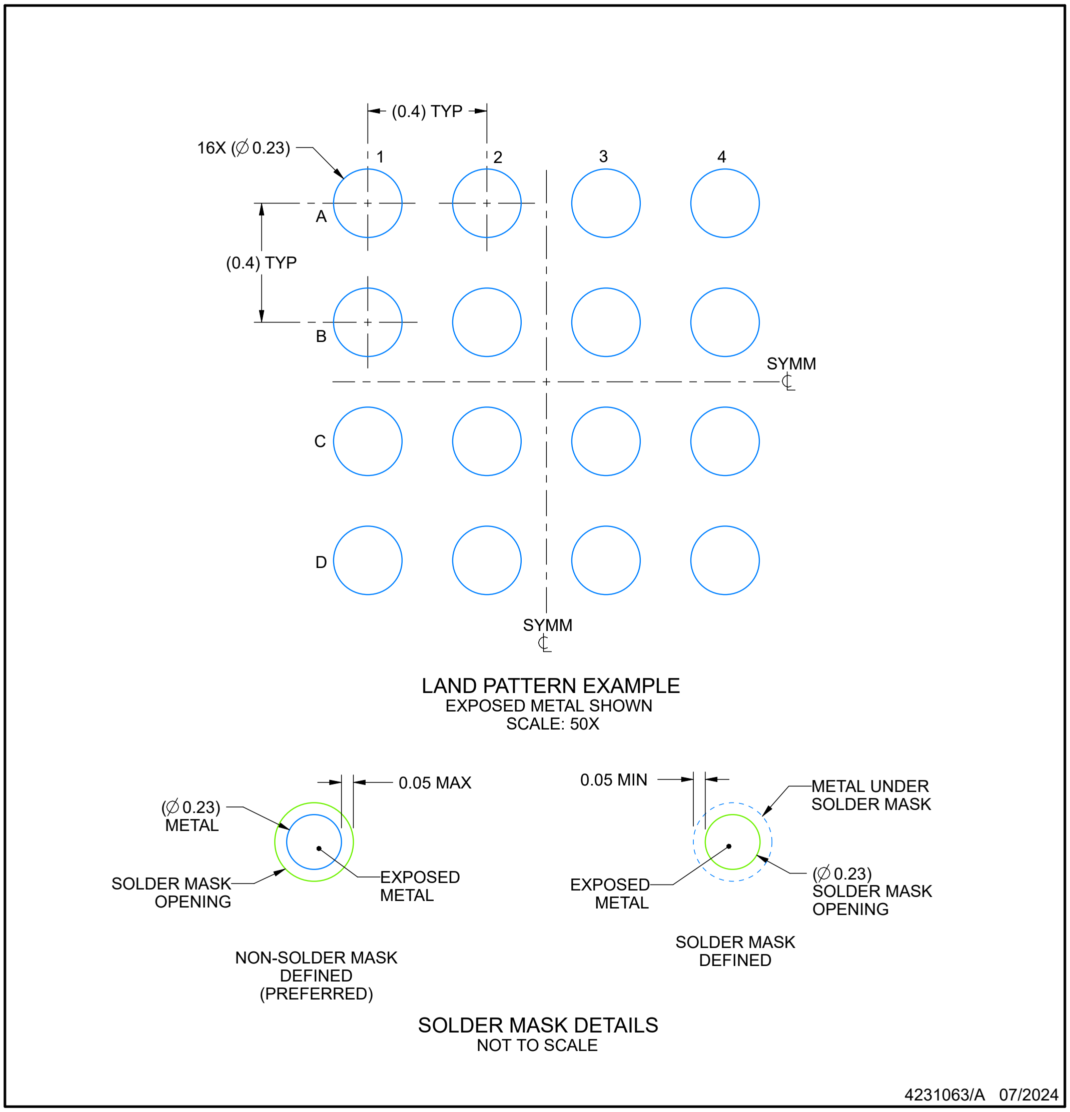
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YBG0016-C01 **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

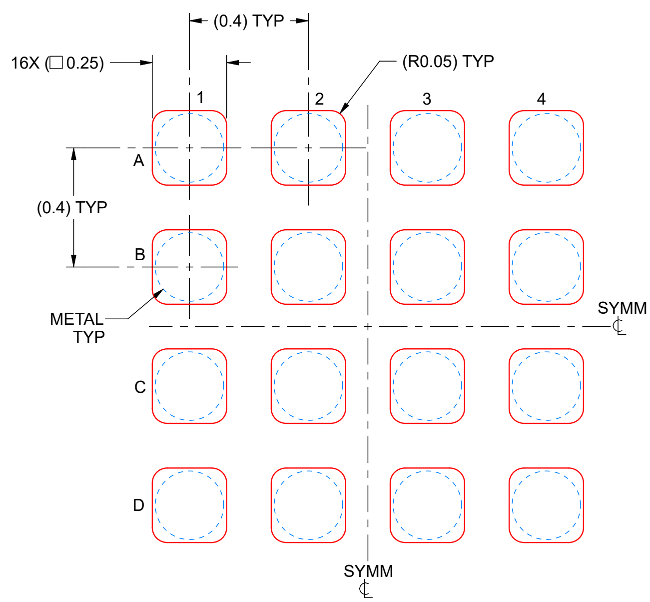
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0016-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 50X

4231063/A 07/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

TEXAS INSTRUMENTS
www.ti.com