TLV9023L-Q1 Automotive Precision, Self-Latching Triple Comparator with AND Gate

1 Features

- Qualified for automotive applications
  AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C
- Output latch with falling-edge triggered clear
- Three individual outputs plus AND output
- AND input for connecting multiple devices
- Power-on Reset (POR) for known start-up
- Latched state on power-up
- 1.65V to 5.5V supply range
- Precision input offset voltage: 300µV
- Rail-to-Rail inputs with fault tolerance
- 95ns typical propagation delay
- Low quiescent current: 22µA per channel
- Low input bias current: 5pA
- open-drain comparator outputs with soft pull-up
- Functional Safety-Capable
  - Documentation available to aid functional safety system design

2 Applications

- Telematics eCall
- Automotive head unit
- Instrument Cluster
- On-board (OBC) and wireless chargers

3 Description

The TLV9023L-Q1 is a triple channel latching comparator with separate outputs and a combined AND output. The family also offers low input offset voltage, power on reset (POR), and fault-tolerant rail-to-rail inputs. These devices have an excellent speed-to-power combination with a propagation delay of 95ns with a quiescent supply current of only 22µA per channel.

The unique feature of the TLV9023L-Q1 is the output latching capability. The output latches upon the first high-to-low threshold crossing, allowing capture of an event or error condition without the full attention of a system controller. This allows events to be captured at start up while the system controller is still initializing or busy with other tasks. The falling-edge triggered clear input allows the system controller to reset the latch after performing any needed tasks and meets safety-critical requirements.

These comparators also feature fault-tolerant inputs that can go up to 6V without damage with no output phase inversion. This makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

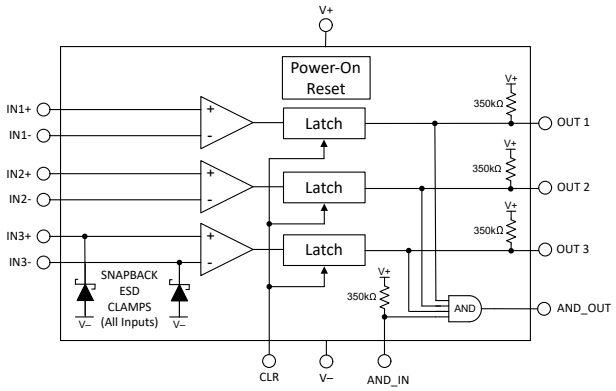
The TLV9023L-Q1 has open-drain outputs that can be pulled-up below or beyond the supply voltage for ORing multiple outputs or level translation. The AND output is push-pull to eliminate the need for a pull-up resistor for a output low start-up state.

The family is specified for the Automotive temperature range of -40°C to +125°C and are available in standard leaded and leadless packages.

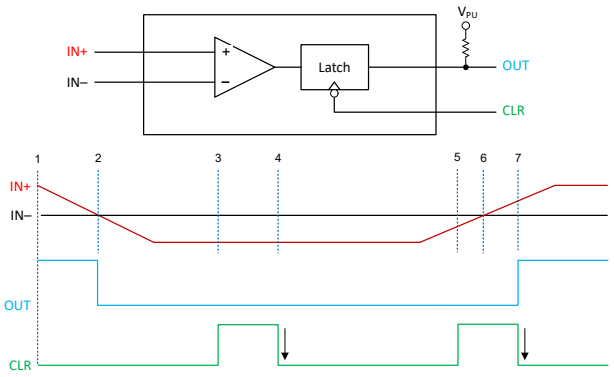
Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)
TLV9023L-Q1	PW (TSSOP 14) (3)	5.00mm × 4.40mm
	RTE (WQFN 16)	3.00mm × 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product preview (not Production Data).



Simplified Block Diagram



Latching Response

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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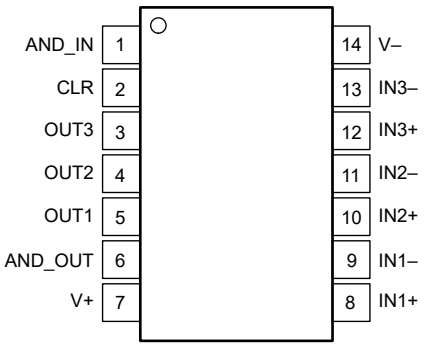
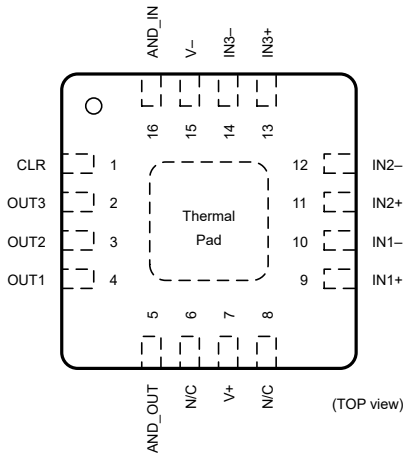
4 Pin Configuration and Functions

Pin Configurations:TLV9023L-Q1



PW Package
14-Pin TSSOP
Top View



RTE Package
16-Pin WQFN
Top View

NOTE: Connect exposed thermal pad directly to V- pin.

Table 4-1. Pin Functions: TLV9023L-Q1

NAME	TLV9023L-Q1		I/O	DESCRIPTION
	14 PINS	16 PINS		
	TSSOP	WQFN		
AND_IN	1	16	I	Input to AND gate (Leave open or tie to VCC)
CLR	2	1	I	Clear input - clears on falling edge
OUT3	3	2	O	Output of comparator 3
OUT2	4	3	O	Output of comparator 2
OUT1	5	4	O	Output of comparator 1
AND_OUT	6	5	O	Output of AND gate
V+	7	7	–	Positive supply voltage
IN1+	8	9	I	Non-Inverting (+) input of comparator 1
IN1–	9	10	I	Inverting (–) input of comparator 1
IN2+	10	11	I	Non-Inverting (+) input of comparator 2
IN2–	11	12	I	Inverting (–) input of comparator 2
IN3+	12	13	I	Non-Inverting (+) input of comparator 3
IN3–	13	14	I	Inverting (–) input of comparator 3
V–	14	15	–	Negative Supply Voltage
NC	–	6, 8	–	No internal connection
Thermal Pad	–	–	–	Connect directly to V-

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) – (V–)	–0.3	6	V
Input pins (IN+, IN–, CLR, AND_IN) from (V–)(2)	–0.3	6	V
Current into Input pins (IN+, IN–, CLR, AND_IN)	–10	10	mA
Output (OUT) from (V–)(3)	–0.3	6	V
Output (AND_OUT) from (V–)	–0.3	(V+) + 0.3	V
Output short circuit duration(4)		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Input terminals are diode-clamped to (V–). Input signals that can swing more than 0.3V beyond (V-) must be current-limited to 10mA or less. Additionally, Inputs (IN+, IN–,CLR) can be greater than (V+) and OUT as long as the voltage is within the –0.3V to 6V range
(3) Output (OUT) for open drain can be greater than (V+)
(4) Short-circuit to (V–) or (V+).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-0111	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage: V_S = (V+) - (V-)	1.65	5.5	V
Input voltage range (IN+, IN–, CLR, AND_IN) from (V–)	–0.2	5.5	V
Input common mode voltage range (IN+, IN–) from (V–)	– 0.2	(V+) + 0.2	V
Output voltage range, open drain output, from (V-)(1)	0	5.5	V
Output voltage range, push-pull output (AND_OUT)	(V-)	(V+)	V
Ambient Temperature, T_A	–40	125	°C

(1) All outputs have a 350k internal pull-up to VCC

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5.4 Thermal Information

THERMAL METRIC (1)		TLV9023L-Q1		UNIT
		PW (TSSOP)	RTE (WQFN)	
		14 PINS	16 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	119.4	53.8	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	53.9	58.6	°C/W
R_{qJB}	Junction-to-board thermal resistance	74.4	29.0	°C/W
y_{JT}	Junction-to-top characterization parameter	12.2	2.2	°C/W
y_{JB}	Junction-to-board characterization parameter	74.0	28.9	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	-	13.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

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5.5 Electrical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V-) = 5V, V_{CM} = (V-) at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 1.8V and 5V	–1.75	±0.3	1.75	mV
V_{OS}	Input offset voltage	V_S = 1.8V and 5V, T_A = –40°C to +125°C	–2.25		2.25	
dV_T/dT	Input offset voltage drift	V_S = 1.8V and 5V, T_A = –40°C to +125°C		±0.5		µV/°C
POWER SUPPLY						
I_Q	Quiescent current per comparator	V_S = 1.8V and 5V, No Load, Output High		22	30	µA
I_Q	Quiescent current per comparator	V_S = 1.8V and 5V, No Load, Output High, T_A = –40°C to +125°C			42	
V_{POR}	Power-On Reset Voltage			1.5		V
PSRR	Power-supply rejection ratio	V_S = 1.8V to 5V, T_A = –40°C to +125°C		95		dB
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S/2		5		pA
I_{OS}	Input offset current	V_{CM} = V_S/2		1		pA
INPUT CAPACITANCE						
C_{ID}	Input Capacitance, Differential	V_{CM} = V_S/2		2		pF
C_{IC}	Input Capacitance, Common Mode	V_{CM} = V_S/2		3		pF
INPUT VOLTAGE RANGE						
V_{IH_CLR}	Voltage input high threshold of CLR		1.2			V
V_{IL_CLR}	Voltage input low of threshold CLR				0.6	V
$V_{CM\text{-}Range}$	Common-mode voltage range	V_S = 1.8V and 5V, T_A = –40°C to +125°C	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 5V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V, T_A = –40°C to +125°C		70		dB
CMRR	Common-mode rejection ratio	V_S = 1.8V, (V–) – 0.2V < V_{CM} < (V+) + 0.2V, T_A = –40°C to +125°C		60		dB
OUTPUT						
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA, T_A = 25°C		75	125	mV
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA, T_A = –40°C to +125°C			175	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 500nA, T_A = 25°C * Internal 350k Pull Up resistor		175	206	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 500nA, T_A = –40°C to +125°C			215	mV
I_{SC}	Short-circuit current	V_S = 5V, Sinking		85		mA
AND GATE CHARACTERISTICS						
V_{IH}	High-Level Input Voltage	V_S = 1.65 to 2.7V	0.55 * (V+)			V
		V_S = 3V to 3.6V	1.8			V
		V_S = 4.5V to 5.5V	0.7 * (V+)			V
V_{IL}	Low-Level Input Voltage	V_S = 1.65 to 2.7V			0.35 * (V+)	V
		V_S = 3V to 3.6V			0.8	V
		V_S = 4.5V to 5.5V			0.3 * (V+)	V
V_{OL}	Voltage swing from (V–)	I_{SINK} = 4mA, T_A = 25°C, V_S = 5V		75	125	mV
V_{OH}	Voltage swing from (V+)	I_{SOURCE} = 1mA, T_A = 25°C, V_S = 5V		175	215	mV
dt/dV	Input transition fall rate	V_S = 1.65V to 5.5V			1	ns/V

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5.6 Switching Characteristics

V_S = 5V, CLR = 5V_{PP}, V_L = 0V, V_H = 5V, 2.5V DC offset, V_{CM} = V_S/2, C_L = 15pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
T_{PD-HL}	Propagation delay time, high-to-low, open-drain only	V_{ID} = –100mV, CLR = 0V, Delay from mid-point of input to mid-point of output		95		ns
T_{PD-LH}	Propagation delay time, low-high	V_{ID} = +100mV, CLR = 0V, Delay from mid-point of input to mid-point of output (Internal R_P = 350KΩ)		4		µs
$T_{PD-CLR-F}$	Clear Fall to Latch Reset propagation delay time	CLR = 1.8V to 5V, Delay from CLR falling edge signal to unlatched output condition		15		ns
CLR_{Min}	Minimum Clear Hold Pulse time to register latch disable and transition output state	CLR = 1.8V to 5V, Minimum CLR pulse size required to register a change of state (latch reset) upon CLR falling edge	10			ns
T_{FALL}	5V Output Fall Time, 80% to 20%	V_{ID} = –100mV		1		ns
AND GATE						
T_{PD-LH}	Propagation delay time, low-to-high	Delay from mid-point of input to mid-point of output			7	ns
T_{PD-HL}	Propagation delay time, high-to-low	Delay from mid-point of input to mid-point of output			7	ns
POWER ON TIME						
P_{ON}	Power on-time			25		µs

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5.7 Typical Characteristics

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

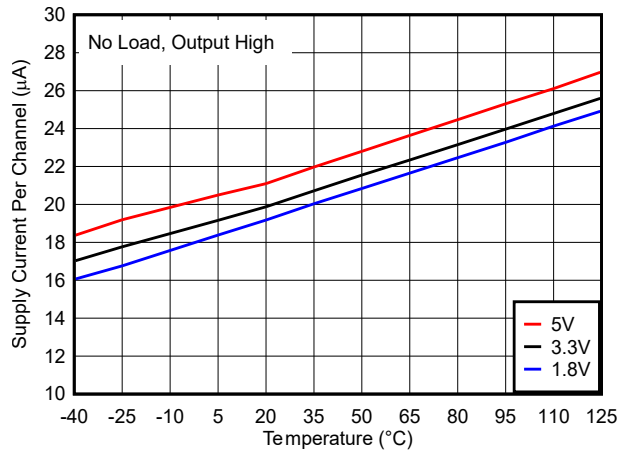

Figure 5-1. Supply Current vs Temperature

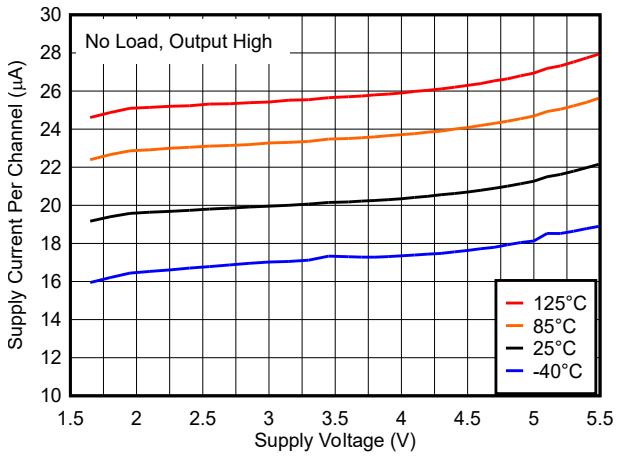

Figure 5-2. Supply Voltage vs Supply Current

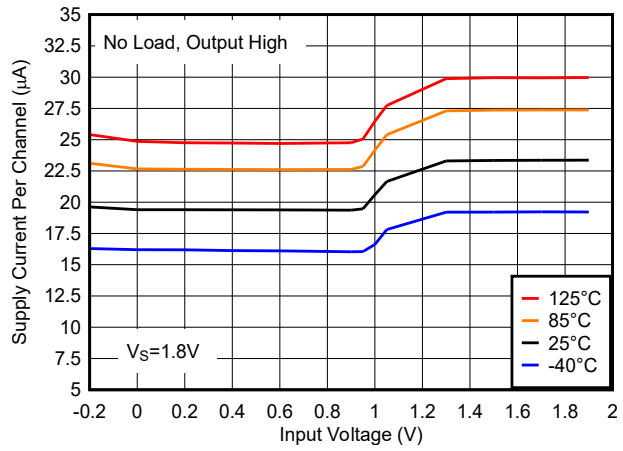

Figure 5-3. Supply Current vs Common Mode Voltage, 1.8V

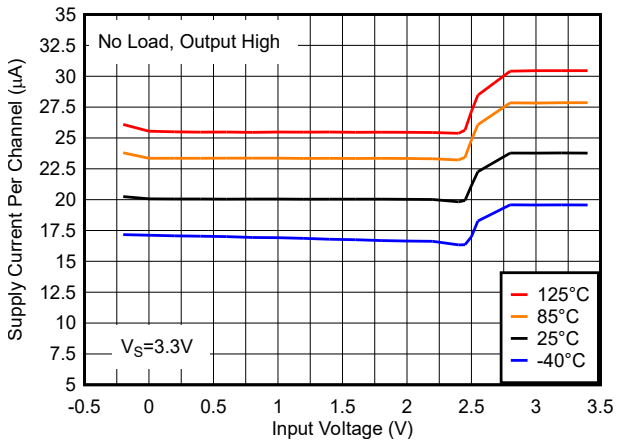

Figure 5-4. Supply Current vs Common Mode Voltage, 3.3V

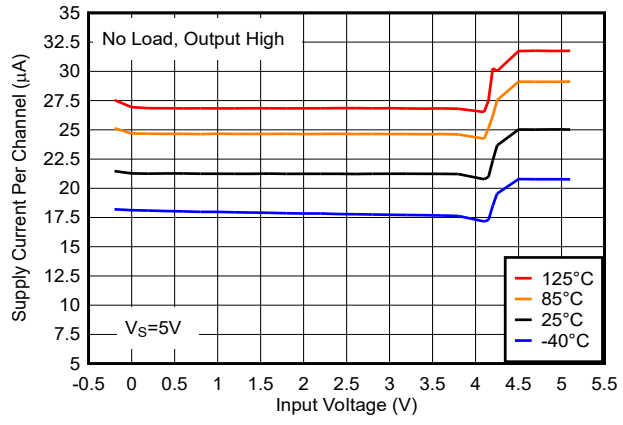

Figure 5-5. Supply Current vs Common Mode Voltage, 5V

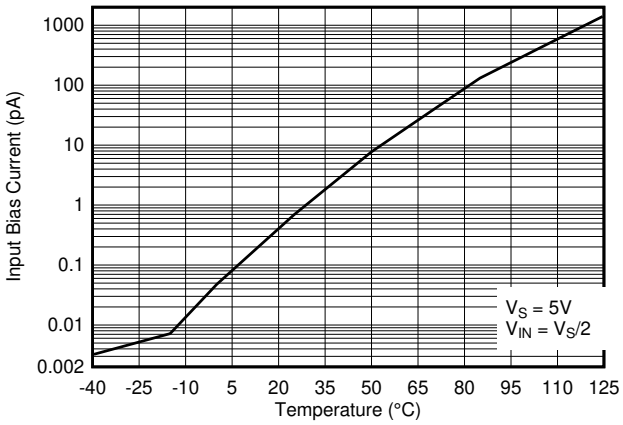

Figure 5-6. Input Bias Current vs Temperature

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

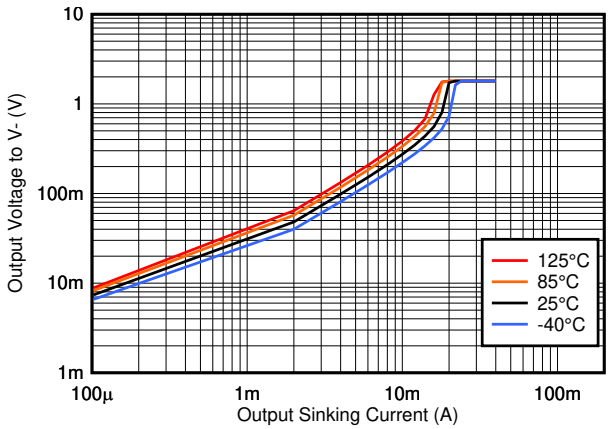

Figure 5-7. Comparator and AND_OUT Output Sinking Current vs Output Voltage, 1.8V

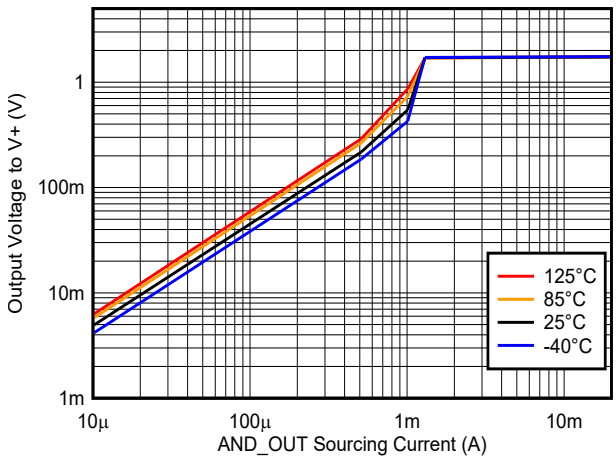

Figure 5-8. AND_OUT Sourcing Current vs Output Voltage, 1.8V

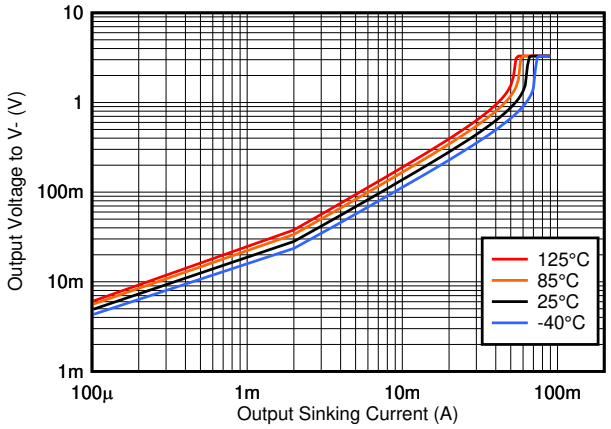

Figure 5-9. Comparator and AND_OUT Output Sinking Current vs Output Voltage, 3.3V

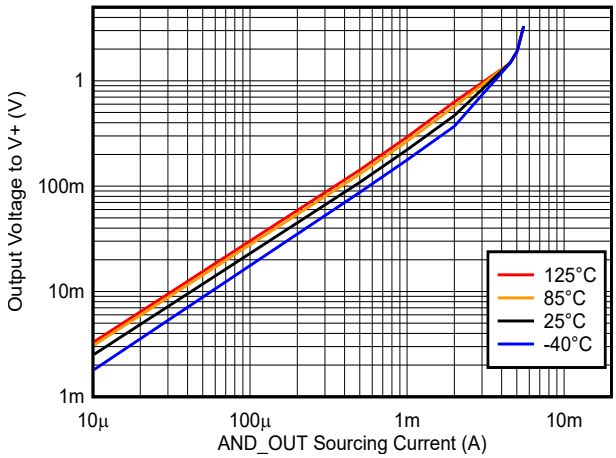

Figure 5-10. AND_OUT Sourcing Current vs Output Voltage, 3.3V

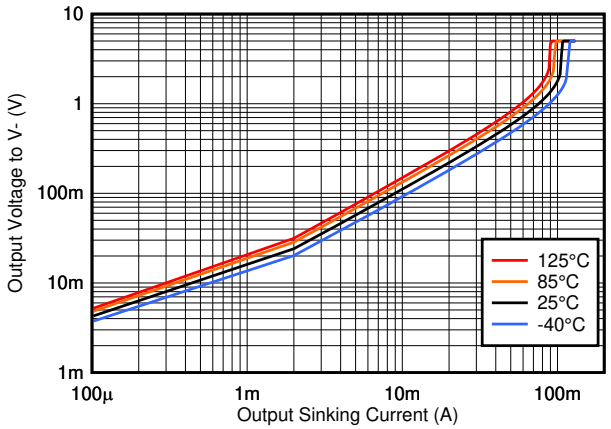

Figure 5-11. Comparator and AND_OUT Output Sinking Current vs Output Voltage, 5V

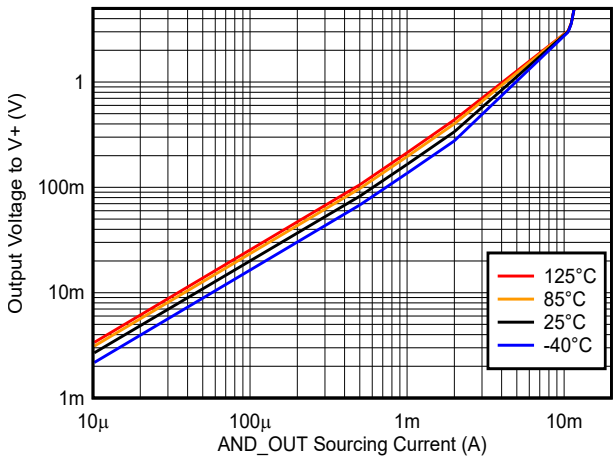

Figure 5-12. AND_OUT Sourcing Current vs Output Voltage, 5V

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

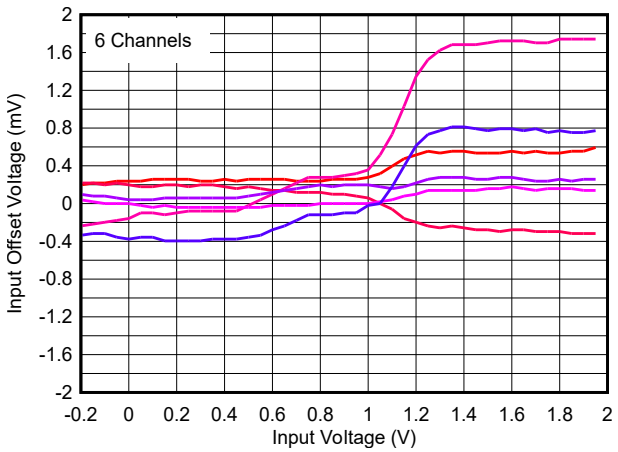

Figure 5-13. Offset Voltage vs Common Mode Voltage, 1.8V, 125°C

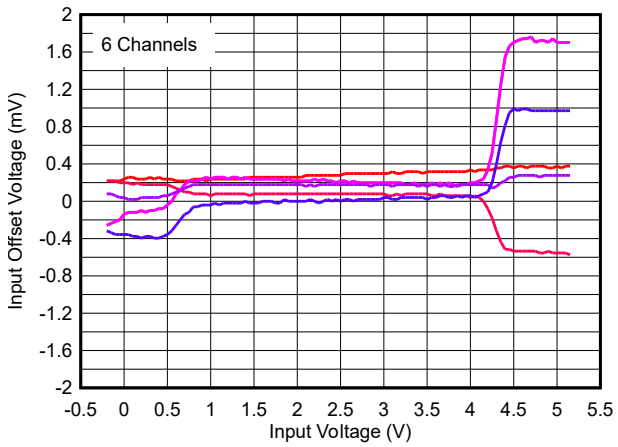

Figure 5-14. Offset Voltage vs Common Mode Voltage, 5V, 125°C

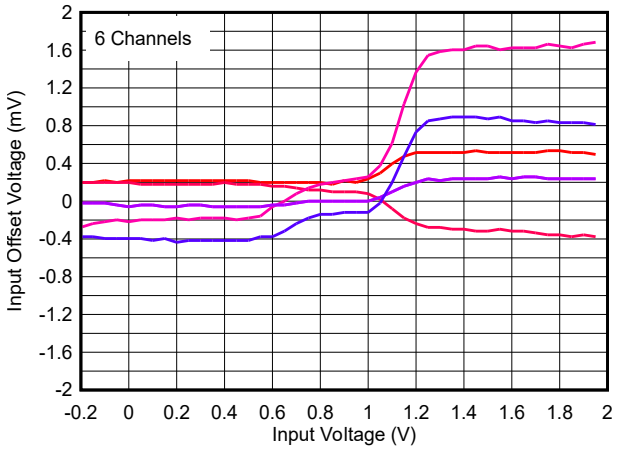

Figure 5-15. Offset Voltage vs Common Mode Voltage, 1.8V, 25°C

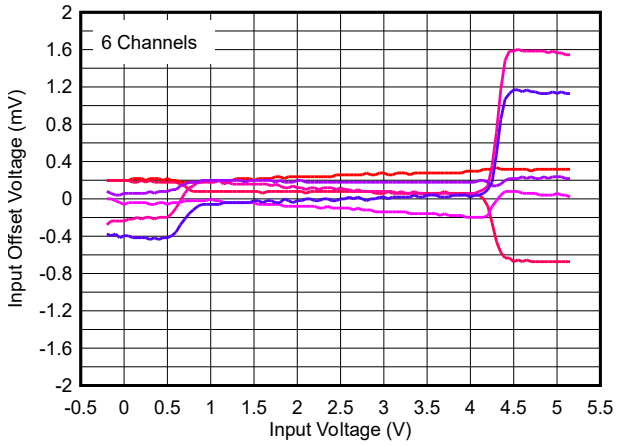

Figure 5-16. Offset Voltage vs Common Mode Voltage, 5V, 25°C

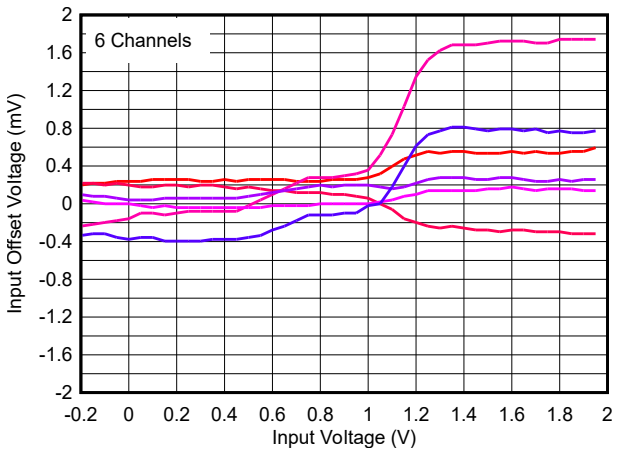

Figure 5-17. Offset Voltage vs Common Mode Voltage, 1.8V, -40°C

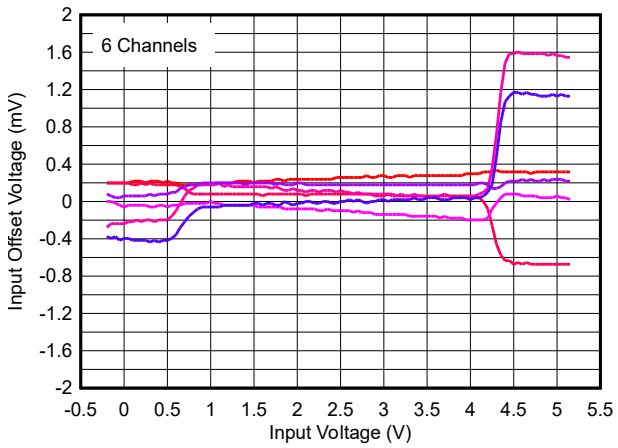

Figure 5-18. Offset Voltage vs Common Mode Voltage, 5V, -40°C

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

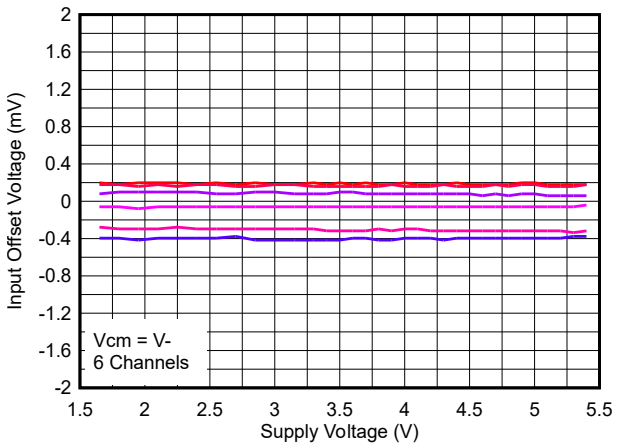

Figure 5-19. Offset Voltage vs Supply Voltage, Low VCM, -40°C

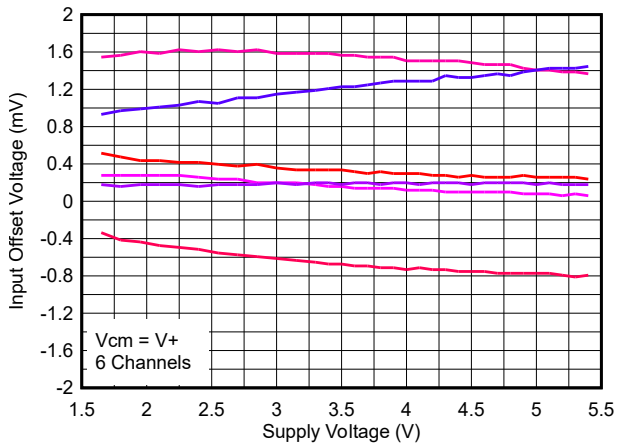

Figure 5-20. Offset Voltage vs Supply Voltage, High VCM, -40°C

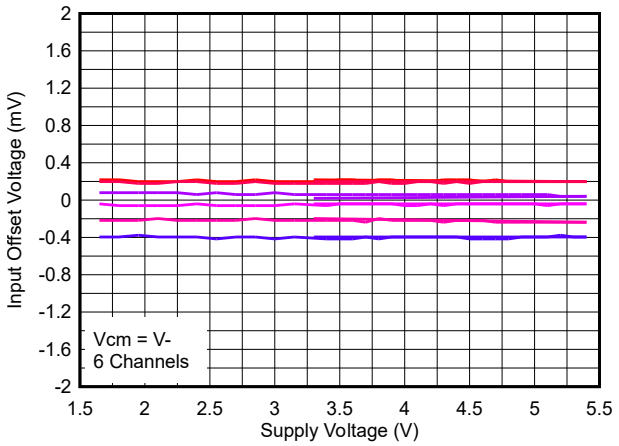

Figure 5-21. Offset Voltage vs Supply Voltage, Low VCM, 25°C

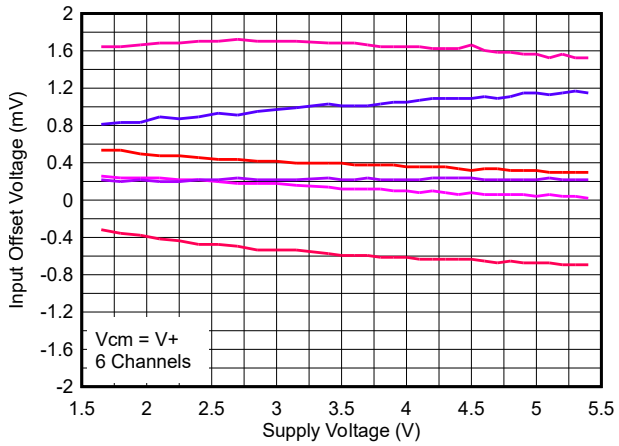

Figure 5-22. Offset Voltage vs Supply Voltage, High VCM, 25°C

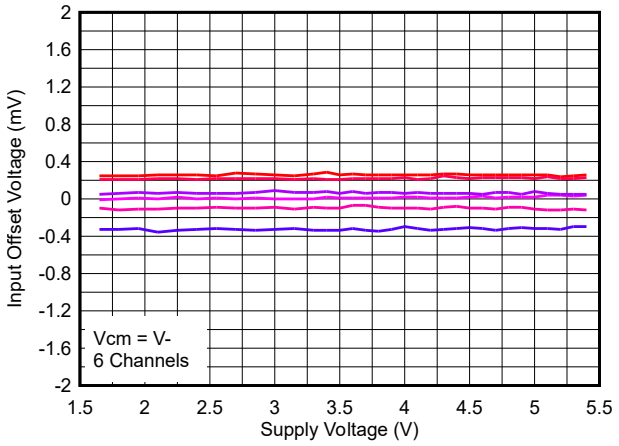

Figure 5-23. Offset Voltage vs Supply Voltage, Low VCM, 125°C

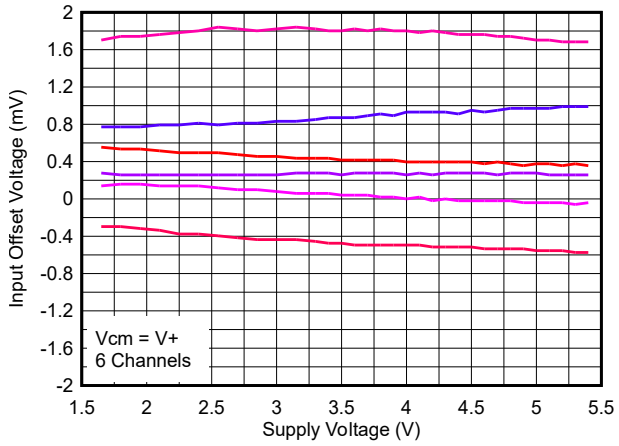

Figure 5-24. Offset Voltage vs Supply Voltage, High VCM, 125°C

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5.7 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, R_{PULLUP} = 2.5k, C_L = 15pF, V_{CM} = 0V, $V_{UNDERDRIVE}$ = 100mV, $V_{OVERDRIVE}$ = 100mV unless otherwise noted.

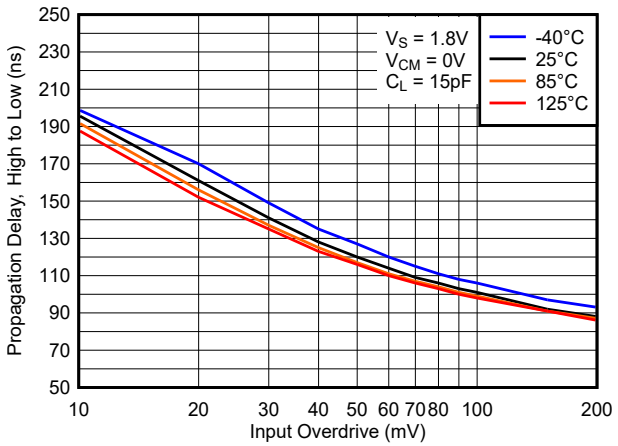

Figure 5-25. Propagation Delay, High to Low, 1.8V

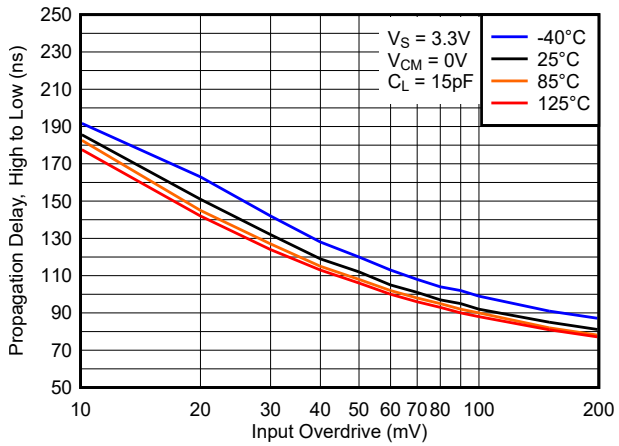

Figure 5-26. Propagation Delay, High to Low, 3.3V

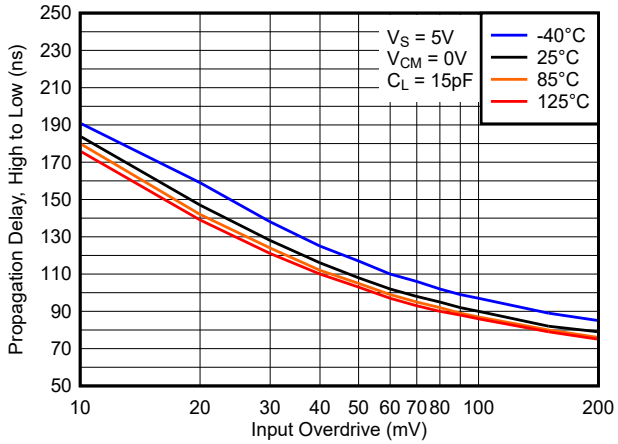

Figure 5-27. Propagation Delay, High to Low, 5V

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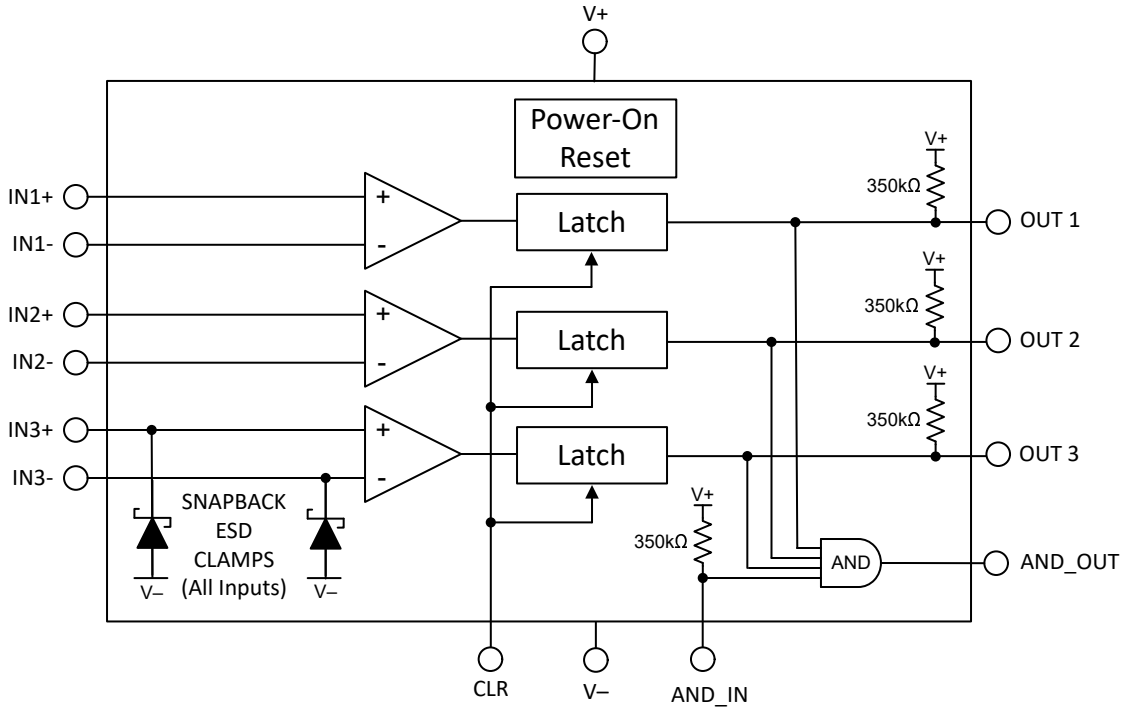
6 Detailed Description

6.1 Overview

The TLV9023L-Q1 is a triple channel latching comparator with a combined AND output. The device offers low input offset voltage, power on reset (POR), fault-tolerant inputs and an excellent speed-to-power combination with a propagation delay of 95ns with a quiescent supply current of 22µA per channel.

6.2 Functional Block Diagram



6.3 Feature Description

The unique feature of the TLV9023L-Q1 is the output latching capability. The output latches upon the first threshold crossing to allow capturing of an event or error condition without the full attention of a system controller. This allows events to be captured at start up while the system controller is still initializing. The system controller can reset the latch after performing any needed tasks. The output is latched at power-up and requires the CLR pin to be pulled low to clear the latch.

The three outputs of the comparators are available individually, and also ANDed together, along with the AND_IN logic input, to the push-pull AND_OUT output. The AND_IN input can be used to dasy-chain multiple TLV9023L-Q1 circuits, or external comparator outputs or error logic lines.

These comparators also feature fault-tolerant inputs that can go up to 6V without damage with no output phase inversion. This makes this family of comparators designed for precision voltage monitoring in harsh, noisy environments.

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6.4 Device Functional Modes

6.4.1 Outputs

6.4.1.1 Comparator Open-Drain Outputs

The TLV9023L-Q1 features an open-drain (also commonly called open collector) sinking-only output stage enabling the output logic levels to be pulled up to any voltage up to 5.5V, independent of the comparator supply voltage (V_S). The open-drain output also allows logical ORing of multiple open-drain outputs and logic level translation.

Each of the outputs also has an internal 350kΩ weak pull-up resistor to V+ to reduce the number of external pull-up resistors. If fast (<100ns) risetimes are required, a lower value external pull-up resistor is required to increase the risetime the expense of power dissipation.

Unused open-drain outputs can be left floating, or can be tied to the V- pin if floating pins are not allowed.

The open-drain output protection consists of a ESD clamp between the output and V- to allow the output to be pulled to any voltage up to a maximum of 5.5V, even if the pull-up voltage exceeds V_S.

6.4.1.2 AND_OUT Output

The TLV9023L-Q1 AND_OUT output is the logical AND of the three internal comparator outputs and the AND_IN input. Any comparator output going low sets the AND_OUT output low.

The AND_OUT output is a push-pull output and does not require an external pull-up resistor and holds the output low during initial power-up.

The AND_OUT output can be connected to the AND_IN of another TLV9023L-Q1 to allow daisy-chaining of the devices. Any comparator going low causes all the AND_OUT outputs to go low in the chained devices.

6.4.2 Power-On Reset (POR)

The TLV9023L-Q1 has a internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V_s) is ramping up or ramping down, the POR circuitry is activated for up to 60µs (over temperature) after the minimum supply voltage threshold of V_{POR} is crossed (typically 1.5V), or immediately when the supply voltage drops below V_{POR}. During the POR period, the input conditions are ignored. When the supply voltage is equal to or greater than the minimum supply voltage, the comparator initially in a latched condition. CLR needs to be asserted after power-up for proper operation.

The input levels must be settled before the end of the POR period to prevent premature latching. Attention must be payed to the time constants of any filtering or RC components on the inputs (references, dividers, bypass capacitors, et cetera).

6.4.2.1 Output POR Behavior

The POR circuit keeps the output **low** during the POR period (t_{on}).

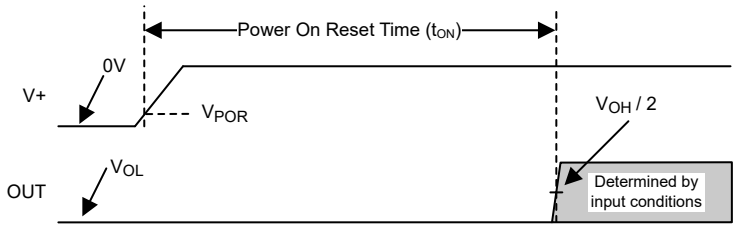

Figure 6-1. Power-On Reset Timing Diagram Example

The POR starts with the output **low** through POR then remains latched **low** post-POR until cleared by the CLR pin. The AND_OUT also holds low during POR.

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6.4.3 Output Latching

The TLV9023L-Q1 has an output that latches upon the first input transition crossing through the input threshold after being armed. The output stays latched until the falling edge of the CLR pin.

6.4.3.1 TLV9023L-Q1 Latch Behavior

The TLV9023L-Q1 output latches **low** during the POR period. Following the POR period, the output is **latched low** and must be cleared with a **high-to-low** transition on the CLR pin. The following is a summary of the latch operation.

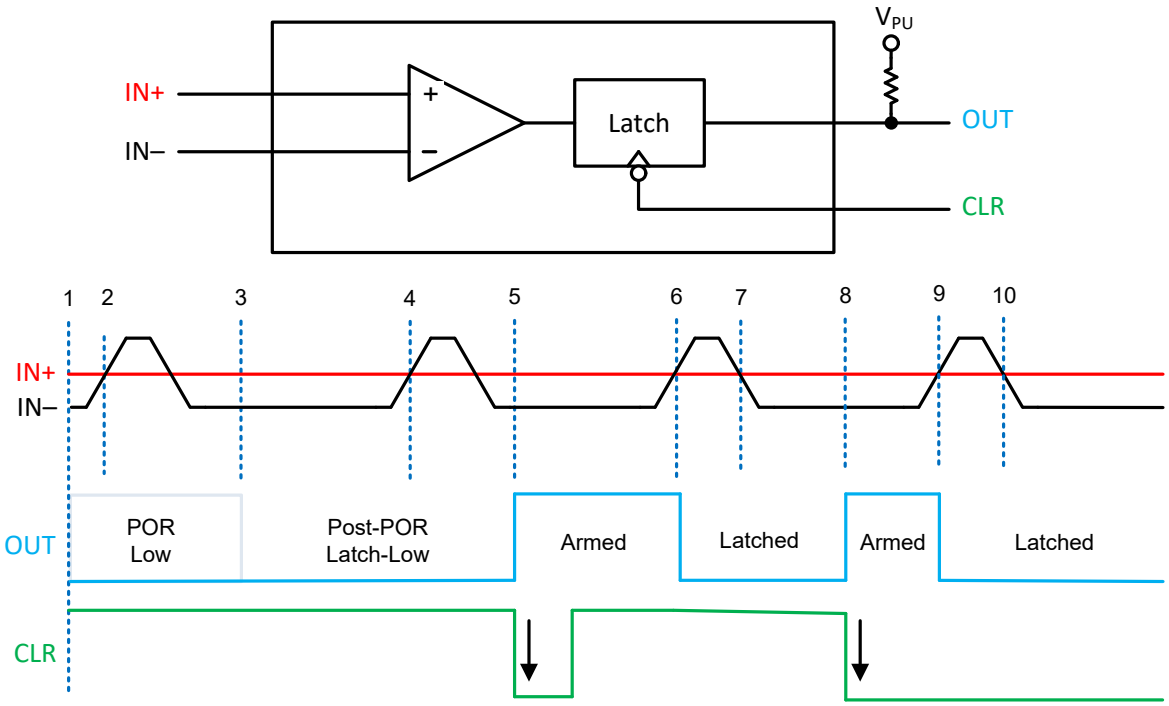

Figure 6-2. Latch Timing Example

The following is a summary of the latch operation.

1. Output is low during the POR period following first power-on.
2. Input transition is ignored during POR period.
3. Following the POR period, the OUT stays latched low.
4. IN- passes IN+, but transition is ignored during latch.
5. CLR falling edge resets and arms latch awaiting next transition.
6. IN- > IN+, so OUT goes low and latches.
7. IN+ > IN-, but OUT remains latched low.
8. CLR falling edge resets and arms latch for next transition.
9. IN- crosses IN+, output goes low and latches again.
10. Output remains latched low even when IN+ > IN-.

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6.4.3.2 Clear (CLR) Input

When CLR is high or low, and the comparator is not in a latched condition, the comparator is active ("armed") and responding to the input conditions, ready for the next qualifying condition to latch.

The CLR input only clears the output latch on the high-to-low (falling) edge of the CLR input. The comparator is then active (armed) after the clear until the next latch condition event.

Using the falling-edge to trigger the reset allows the CLR pin to be either a steady high or low, which prevents a hardware or software failure from locking-up the comparator and allows meeting safety-critical design requirements.

There can be a setup-time contention if the CLR pin is transitioning (falling) at the same time as the comparator output transitions. The output state is indeterminate during the CLR falling edge time. The recommendation is to make the CLR falling-edge as fast as possible to avoid this contention (<100ns fall time).

The CLR pin features a Failsafe, or "5V Compatible" input, accepting logic high levels up to 5V, independent of the comparator supply voltage. The logic high (VOH) threshold is 1.2V.

The CLR input also has a light 200nA active pull-down current to make sure that the CLR pin is low during start-up and the comparator is active. Even with this pull-down, floating the CLR input is not recommended.

6.4.4 Inputs

6.4.4.1 Rail to Rail Input

The TLV9023L-Q1 input voltage range extends from 200mV below V- to 200mV above V+. The differential input voltage (V_{ID}) can be any voltage within these limits. No phase-inversion of the comparator output occurs when the input pins exceed V+ or V-.

6.4.4.2 Fail-Safe Inputs

The inputs are fault tolerant up to 5.5V independent of supply voltage. Fault tolerant is defined as maintaining the same high input impedance when V_S is un-powered or within the recommended operating range.

The fault tolerant inputs can be any value between 0V and 5.5V, even while V_S is zero or ramping up or down. This feature avoids power sequencing issues as long as the input voltage range and supply voltage are within the maximum specified ranges. This is possible since the inputs are not clamped to V+ and the input current maintains high impedance even when a higher voltage is applied to the inputs.

As long as one of the input pins remains within the valid input range, and the supply voltage is valid and not in POR, the output state is correct.

The following is a summary of input voltage excursions and the outcomes:

1. When both IN- and IN+ are within the specified input voltage range:
   a. If IN- is higher than IN+ and the offset voltage, the output is low.
   b. If IN- is lower than IN+ and the offset voltage, the output is high.
2. When IN- is higher than the specified input voltage range and IN+ is within the specified voltage range, the output is low.
3. When IN+ is higher than the specified input voltage range and IN- is within the specified input voltage range, the output is high
4. When IN- and IN+ are both outside the specified input voltage range, the output is **indeterminate** (random). *Do not* operate in this region. The output can randomly flip.

Even with the fault tolerant feature, TI *strongly* recommends keeping the inputs within the specified input voltage range during normal system operation to maintain data sheet specifications. Operating outside the specified input range can cause changes in specifications such as propagation delay and input bias current, which can lead to unpredictable behavior.

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6.4.4.3 Input Protection

The TLV9023L-Q1 incorporates internal ESD protection circuits on all pins. The inputs use a proprietary "snapback" type ESD clamp from each pin to V-. There is no "upper" ESD clamp to V+, which allows the input pins to exceed the supply voltage (V+). During an ESD event, the snapback diodes "short" and go low impedance to V- (like an SCR).

If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct due to transients. The current must be limited 10mA or less. This series resistance can be part of any resistive input dividers or networks.

The ESD diodes cannot clamp on the upper voltages. The ESD clamps do not "hold" at a fixed maximum voltage like a Zener diode. If the inputs are connected to a source that can exceed 5.5V, then external clamping is required to prevent exceeding the maximum input voltage.

The input bias current is typically 5pA for input voltages between V+ and V-. Input bias current typically doubles for each 10°C temperature increase.

6.4.4.4 Internal Hysteresis

The TLV9023L-Q1 does NOT have built-in hysteresis. The latching function negates the need for hysteresis as the output latches upon the first output transition. The reference level must be set to the desired threshold level, and the input signals well filtered to remove any noise or transients that can cause early triggering.

6.4.4.5 AND_IN Input

The AND_IN input allows daisy-chaining multiple devices to expand the number of inputs. The AND_IN input is pass-through and does not trigger any latching.

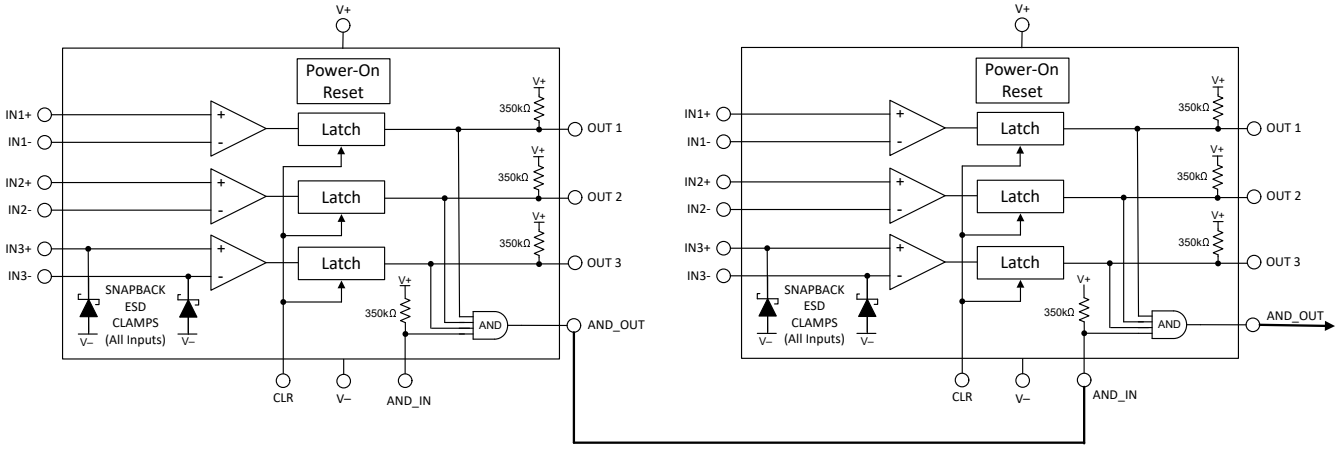

Figure 6-3. Connecting Multiple Devices Together

The AND_OUT pin can be connected to the AND_IN of the next device to create the daisy-chain of multiple devices. The AND_OUT output must be taken from the (rightmost) end of the chain so that all inputs are covered.

The AND_IN input contains a 350kΩ weak pull-up resistor to V+. This eliminates the need for additional pull-up resistors when daisy-chaining several devices. The AND_IN input can be left floating or tied to V+ if not used.

6.4.4.6 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on its own internal wideband noise. Instead, the inputs must be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V+).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The TLV9023L-Q1 compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 7-1 example below, if V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). When V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}) and latches low. Table 7-1 summarizes the output conditions.

Table 7-1. Output Conditions

INPUTS CONDITION	OUTPUT STATE
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (can chatter)
IN+ < IN-	LOW (V_{OL}) (Latches)

7.1.1.2 Propagation Delay

There is a delay between when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. This is shown as t_{pHL} in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output. Because of the latch, the TLV9023L-Q1 does not have a "Low-to high" (t_{pLH}) specification. t_{pLH} is replaced by the "Clear Fall to Latch Reset propagation delay time" ($T_{PD-CLR-F}$) specification, which is the time between the falling edge of the CLR input and the rising edge of the output.

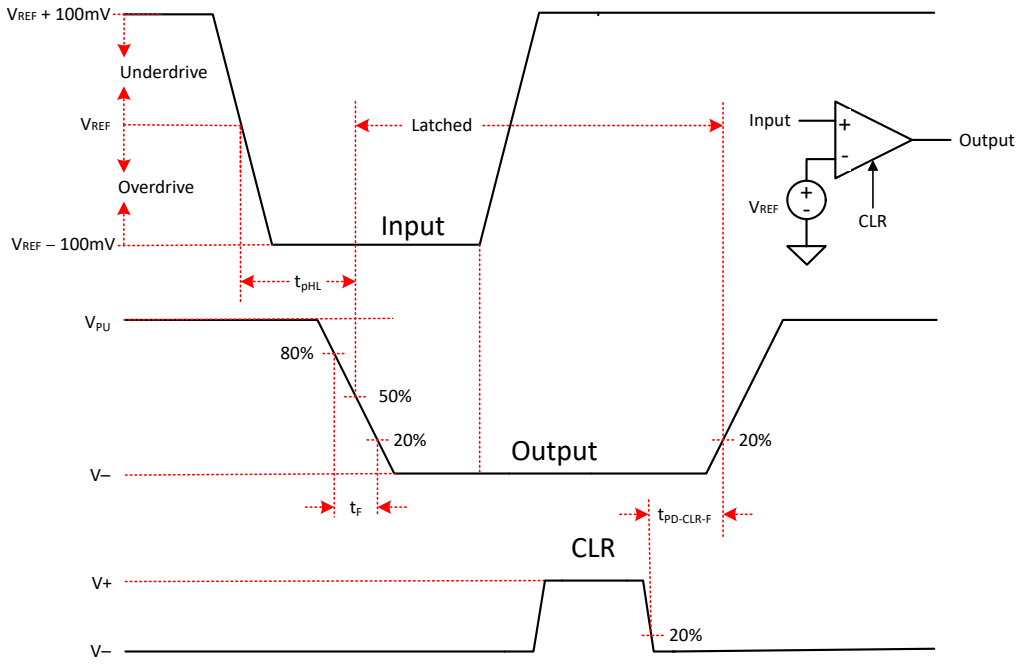

Figure 7-1. Comparator Timing Diagram

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7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage is 100mV as shown in the Figure 7-1 example. The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, apply the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.2 Typical Application

7.2.1 Window Comparator

Window comparators are commonly used to detect undervoltage and overvoltage conditions. Figure 7-2 shows a simple window comparator circuit. Window comparators require open-drain outputs (TLV9023L-Q1) if the outputs are directly connected together.

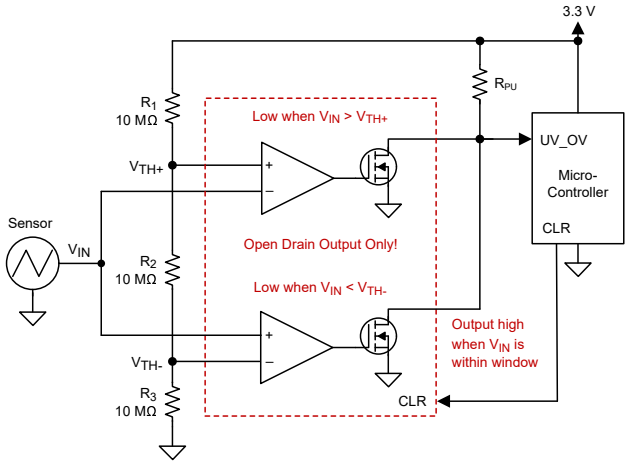

Figure 7-2. Window Comparator Using TLV9023L-Q1

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Latch (logic low output) when an input signal is less than 1.1V
- Latch (logic low output) when an input signal is greater than 2.2V
- Operate from a 3.3V power supply

7.2.1.2 Detailed Design Procedure

Configure the circuit as shown in Figure 7-2. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (V_{TH+} and $V_{TH–}$).

With each resistor being equal, V_{TH+} is 2.2V and V_{TH-} is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The resistor values can be recalculated to provide the desired trip point values.

The sensor output voltage is applied to the inverting and non-inverting inputs of the two comparators. Using two open-drain output comparators allows the two comparator outputs to be Wire-ORed together.

The respective comparator outputs latches low when the sensor is less than 1.1V or greater than 2.2V. The respective comparator outputs are high when the sensor is in the range of 1.1V to 2.2V (within the "window"), as shown in Figure 7-3.

The CLR pin must be toggled high to low to reset the output and arm the comparator.

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7.2.1.3 Application Curve

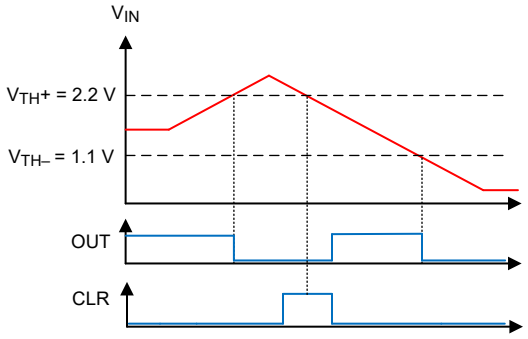

Figure 7-3. Window Comparator Results

For more information, please see Application note SBOA221 "Window comparator circuit".

7.3 Power Supply Recommendations

Due to the fast output edges, bypass capacitors are critical on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents are drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) and (V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

For accurate comparator applications, maintain a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the V+ and V- pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a V+ or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100 ohms) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations must be used when routing long distances.

7.4.2 Layout Example

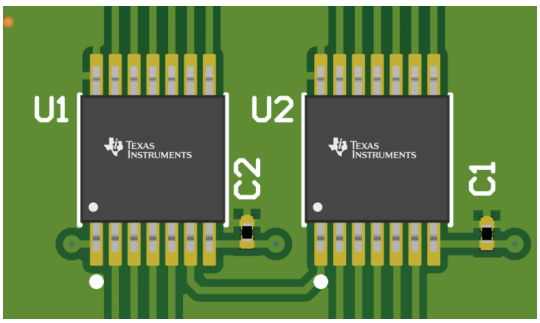

Figure 7-4. Layout Example Showing Dasy-Chained AND_OUT

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Window comparator circuit - SBOA221

Reference Design, Window Comparator Reference Design— TIPD178

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

A Quad of Independently Func Comparators - SNOA654

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2026) to Revision A (November 2026)	Page
• Removed Advance Info for release. PW to preview status	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTLV9023L2WRTERQ1	Active	Preproduction	WQFN (RTE) | 16	5000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TLV9023L-Q1 :

- Catalog : TLV9023L

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

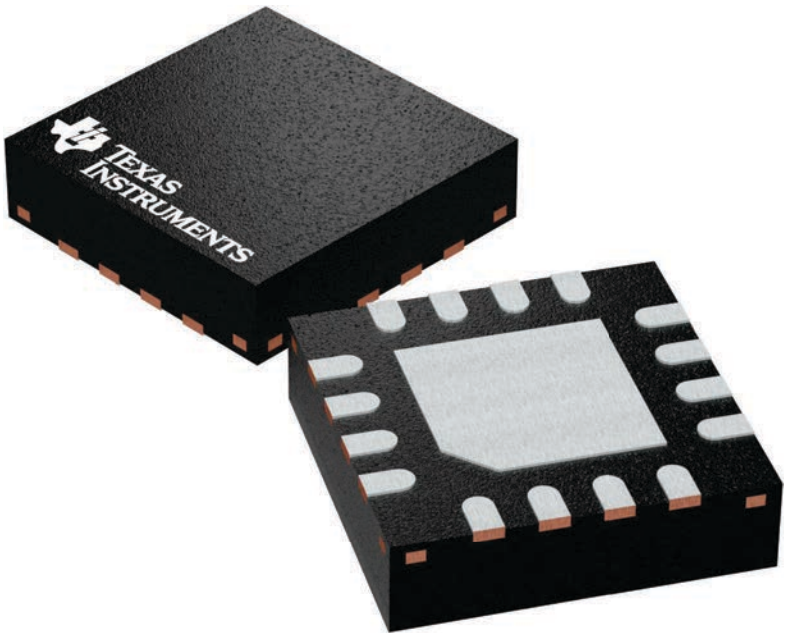
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

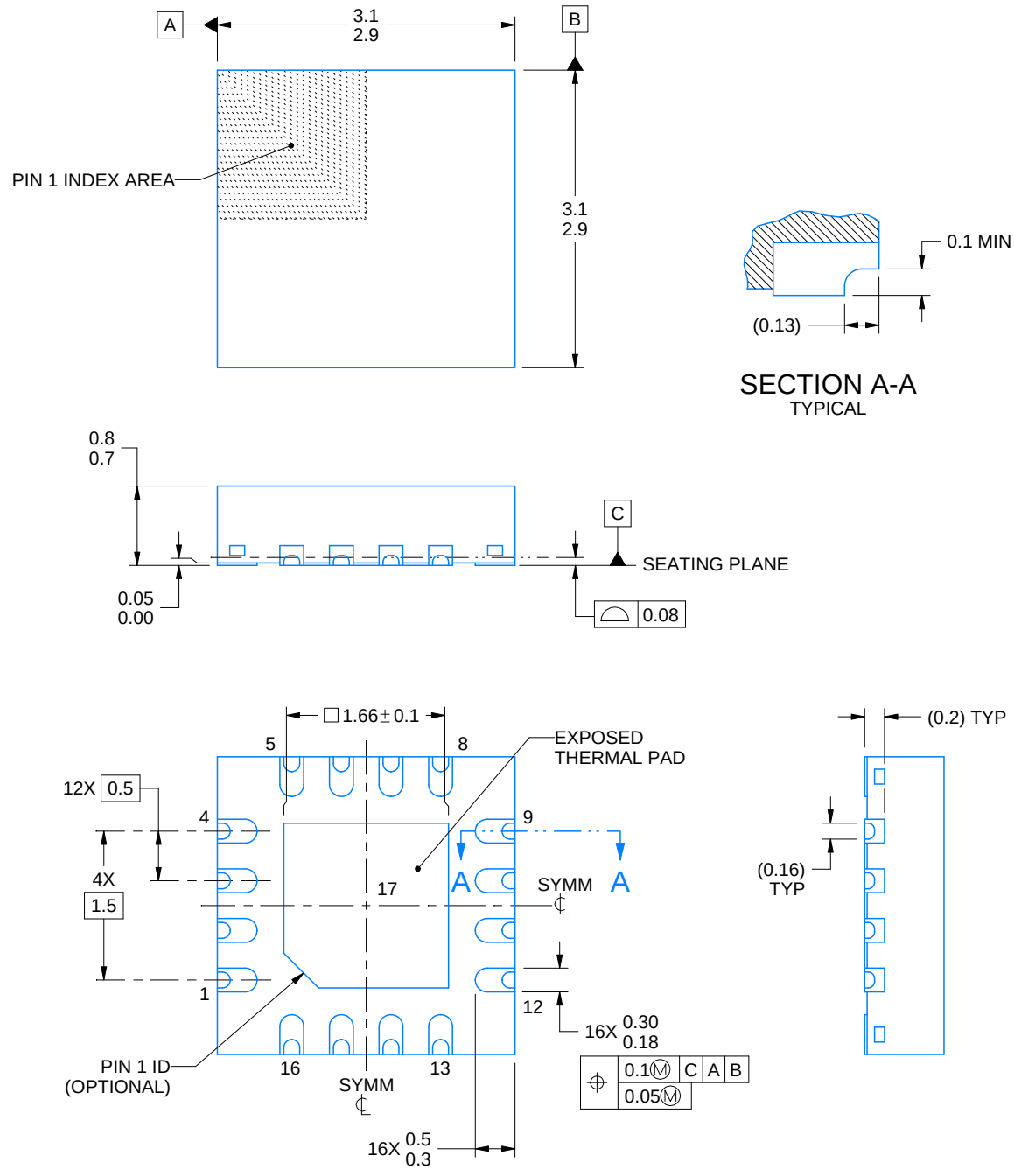


RTE0016K

PACKAGE OUTLINE

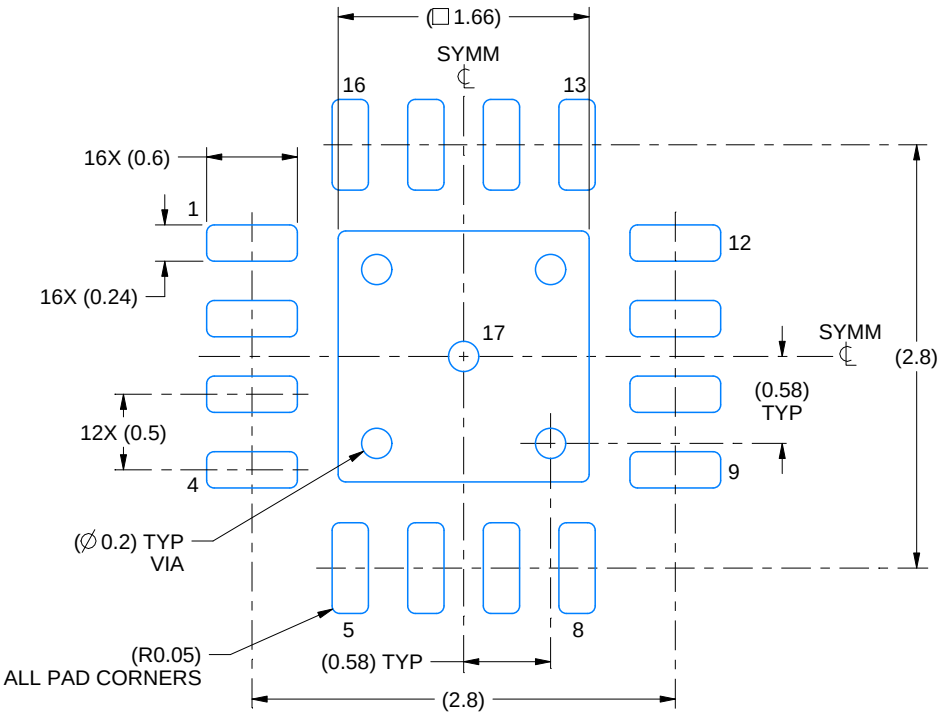
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

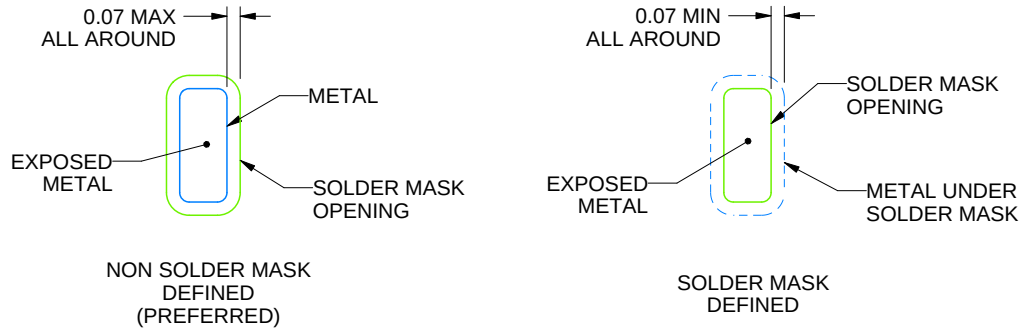


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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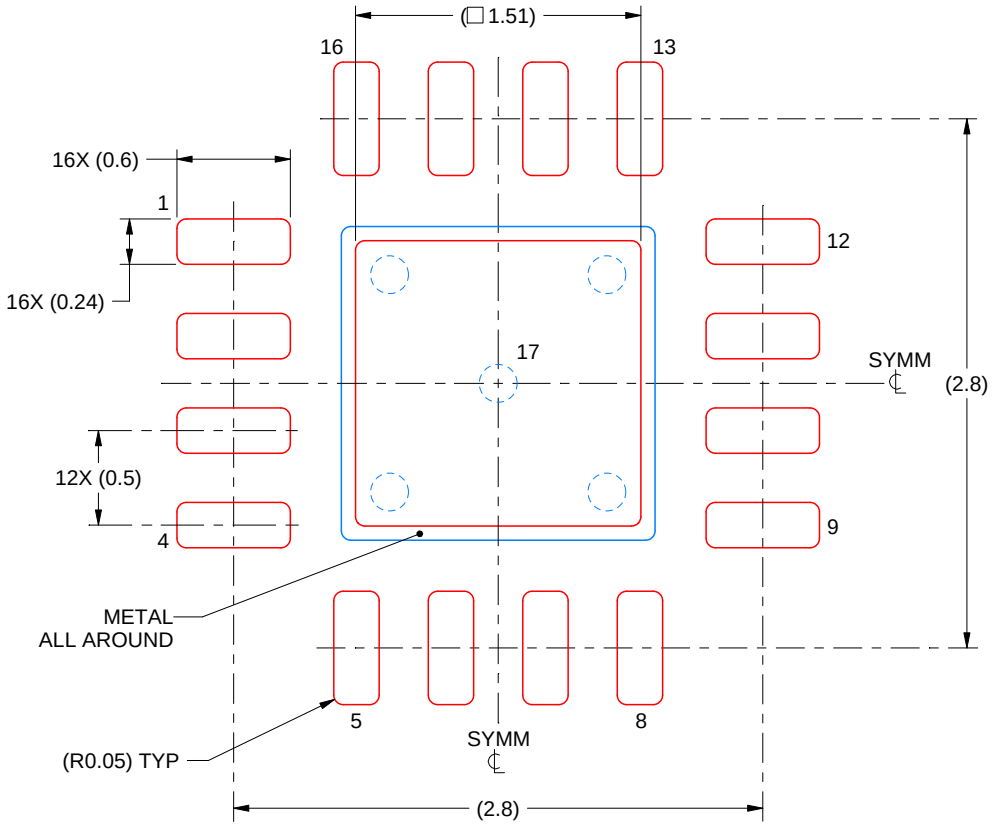
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025