TLVM13630 High-Density, 3-V to 36-V Input, 1-V to 6-V Output, 3-A Power Module With Enhanced HotRod™ QFN Package

1 Features

- Versatile synchronous buck DC/DC module
  - Integrated MOSFETs, inductor, and controller
  - Wide input voltage range of 3 V to 36 V
  - Adjustable output voltage from 1 V to 6 V with 1% setpoint accuracy over temperature
  - 4-mm × 6-mm × 1.8-mm overmolded package
  - –40°C to 125°C junction temperature range
  - Frequency adjustable from 200 kHz to 2.2 MHz
  - Negative output voltage capability
- Ultra-high efficiency across the full load range
  - 93% peak efficiency at 12 V_{IN}, 5 V_{OUT},1 MHz
  - External bias option for improved efficiency
  - Shutdown quiescent current of 0.6 µA (typical)
  - 0.4-V typical dropout voltage at 3-A load
- Ultra-low conducted and radiated EMI signatures
  - Low-noise package with dual input paths and integrated capacitors reduces switch ringing
  - Constant-frequency FPWM mode of operation
  - Meets CISPR 11 and 32 class B emissions
- Suitable for scalable power supplies
  - Pin compatible with the TLVM13620 (36 V, 2 A)
- Inherent protection features for robust design
  - Precision enable input and open-drain PGOOD indicator for sequencing, control, and V_{IN} UVLO
  - Hiccup-mode overcurrent protection
  - Thermal shutdown protection with hysteresis
- Create a custom design using the TLVM13630 with the WEBENCH® Power Designer

2 Applications

- Test and measurement, aerospace and defense
- Factory automation and control
- Buck and inverting buck-boost power supplies

3 Description

The TLVM13630 synchronous buck power module is a highly integrated 36-V, 3-A DC/DC solution that combines power MOSFETs, a shielded inductor, and passives in an Enhanced HotRod™ QFN package. The module has pins for VIN and VOUT located at the corners of the package for optimized input and output capacitor layout placement. Four larger thermal pads beneath the module enable a simple layout and easy handling in manufacturing.

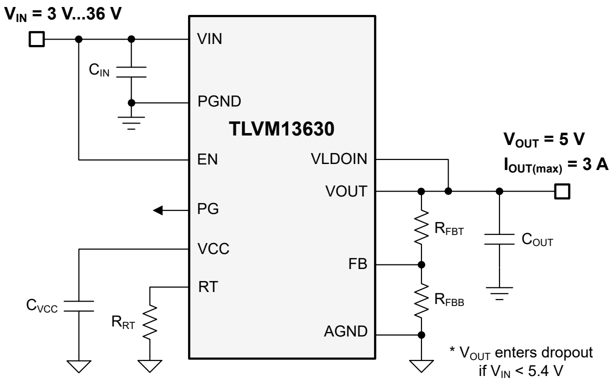
With an output voltage range from 1 V to 6 V, the TLVM13630 is designed to quickly and easily implement a low-EMI design in a small PCB footprint. The total solution requires as few as four external components and eliminates the magnetics and compensation part selection from the design process.

Although designed for small size and simplicity in space-constrained applications, the TLVM13630 module offers many features for robust performance: precision enable with hysteresis for adjustable input-voltage UVLO, integrated VCC, bootstrap and input capacitors for increased reliability and higher density, constant switching frequency over the full load current range for enhanced load transient performance, negative output voltage capability for inverting applications, and a PGOOD indicator for sequencing, fault protection, and output voltage monitoring.

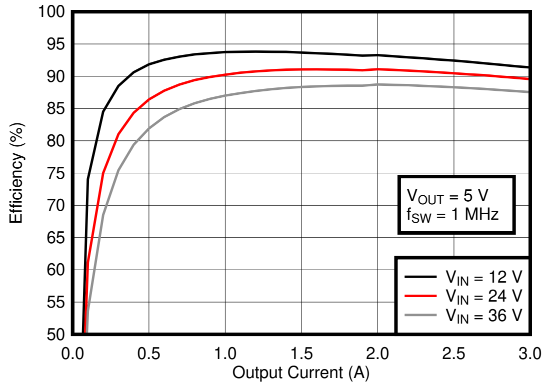
Device Information

PART NUMBER[1]	PACKAGE	BODY SIZE (NOM)
TLVM13630	B0QFN (30)	4.0 mm × 6.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Schematic



Typical Efficiency, V_{OUT} = 5 V, F_{SW} = 1 MHz

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4 Revision History

Changes from Revision * (March 2021) to Revision A (January 2022)	**Page**
• Changed document status from Advance Information to Production Data	1

Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	MODE	SPREAD SPECTRUM	OUTPUT VOLTAGE	EXTERNAL SYNC	JUNCTION TEMPERATURE
TLVM13630	TLVM13630RDHR	FPWM	No	Adjustable	No	–40°C to 125°C

5 Pin Configuration and Functions

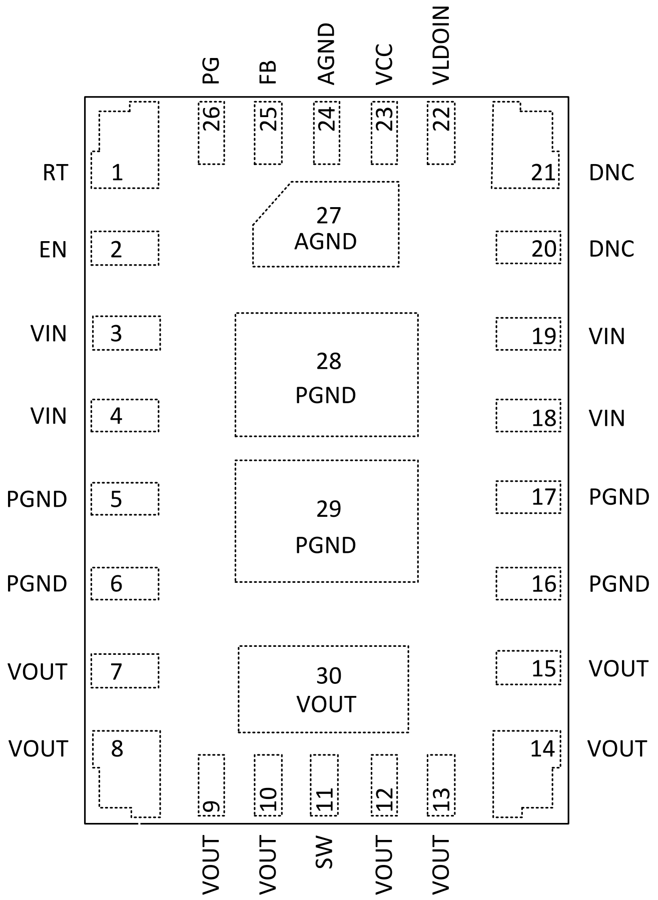


Figure 5-1. 30-Pin QFN, RDH Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	RT	I	Frequency setting pin. This analog pin is used to set the switching frequency between 200 kHz and 2.2 MHz by placing an external resistor from this pin to AGND. Do not leave open or connect to ground.
2	EN	I	Precision enable input pin. High = on, low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Place an external voltage divider between this pin, AGND, and VIN to create an external UVLO.
3, 4, 18, 19	VIN	P	Input supply voltage. Connect the input supply to these pins. Connect input capacitors between these pins and PGND in close proximity to the device. Refer to Section 10.2 for input capacitor placement example.
5, 6, 16, 17, 28, 29	PGND	G	Power ground. This is the return current path for the power stage of the device. Connect this pad to the input supply return, the load return, and the capacitors associated with the VIN and VOUT pins. See Section 10.2 for a recommended layout.
7-10, 12–15, 30	VOUT	P	Output voltage. These pins are connected to the internal output inductor. Connect these pins to the output load and connect external output capacitors between these pins and PGND.
11	SW	O	Switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
20,21	DNC	–	Do Not Connect. Do not connect these pins to ground, to another DNC pin, or to any other voltage. These pins are connected to internal circuitry. Each pin must be soldered to an isolated pad.
22	VLDOIN	P	Optional LDO supply input. Connect to VOUT or to other voltage rail to improve efficiency. Connect an optional high quality 0.1-μF to 1-μF capacitor from this pin to ground for improved noise immunity. Do not connect to a voltage above 12 V or to a voltage greater than VIN. If unused, connect this pin to ground..
23	VCC	O	Internal LDO output. Used as supply to internal control circuits. Do not connect to any external loads. Connect a high-quality 1-μF ceramic capacitor from this pin to PGND.
24, 27	AGND	G	Analog ground. Zero voltage reference for internal references and logic. All electrical parameters are measured with respect to this pin. **This pin must be connected to PGND at a single point.** See Section 10.2 for a recommended layout.
25	FB	I	Feedback input. For the adjustable output version, connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to V_{OUT} at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to AGND. When connecting with feedback resistor divider, keep this FB trace short and as small as possible to avoid noise coupling. See Section 10.2 for a feedback resistor placement.
26	PG	O	Power-good monitor. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required to a suitable pullup voltage. If not used, this pin can be left open or connected to PGND.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Limits apply over T_J = –40°C to 125°C (unless otherwise noted). (1)

		MIN	MAX	UNIT
Input voltage	VIN to AGND, PGND	–0.3	40	V
	VLDOIN to AGND, PGND	–0.3	16	V
	EN to AGND, PGND	–0.3	40	V
	RT to AGND, PGND	–0.3	5.5	V
	FB to AGND, PGND	–0.3	16	V
	PG to AGND, PGND	0	20	V
	PGND to AGND	–1	2	V
Output voltage	VCC to AGND, PGND	–0.3	5.5	V
	SW to AGND, PGND(2)	–0.3	40	V
	VOUT to AGND, PGND	–0.3	6	V
Input current	PG	–	10	mA
T_J	Junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C
T_{stg}	Storage temperature	–55	150	°C
Peak reflow case temperature			260	°C
Maximum number of reflows allowed			3	
Mechanical shock	Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		1500	G
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20 to 2000 Hz		20	G

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) A voltage of 2 V below PGND and 2 V above VIN can appear on this pin for ≤ 200 ns with a duty cycle of ≤ 0.01%.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Limits apply over T_J = –40°C to 125°C (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Input voltage	VIN (Input voltage range after start-up)	3		36	V
Input voltage	VLDOIN			12	V
Output voltage	VOUT(1)	1		6	V
Output current	IOUT(2)	0		3	A
Frequency	F_{SW} set by RT	200		2200	kHz
Input current	PG			2	mA
Output voltage	PG	0		16	V
T_J	Operating junction temperature	–40		125	°C
T_A	Operating ambient temperature	–40		105	°C

(1) Under no conditions should the output voltage be allowed to fall below 0 V.
(2) Maximum continuous DC current may be derated when operating with high switching frequency, high ambient temperature, or both. Refer to the *Typical Characteristics* section for details.

6.4 Thermal Information

THERMAL METRIC(1)		TLVM13630 RDH (QFN) 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (TPSM63603 EVM)	29.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	33.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter(3)	4.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter(4)	21.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The junction-to-ambient thermal resistance, $R_{\theta JA}$, applies to devices soldered directly to a 64-mm x 83-mm four-layer PCB with 2 oz. copper and natural convection cooling. Additional airflow and PCB copper area reduces $R_{\theta JA}$. For more information see the Layout section.
(3) The junction-to-top board characterization parameter, ψ_{JT}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (section 6 and 7). $T_J = \psi_{JT} \times P_{dis} + T_T$; where P_{dis} is the power dissipated in the device and T_T is the temperature of the top of the device.
(4) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature, T_J, of a device in a real system, using a procedure described in JESD51-2A (sections 6 and 7). $T_J = \psi_{JB} \times P_{dis} + T_B$; where P_{dis} is the power dissipated in the device and T_B is the temperature of the board 1mm from the device.

6.5 Electrical Characteristics

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input operating voltage range	Needed to start up (over I_{OUT} range)	3.95		36	V
		Once operating (over I_{OUT} range)	3		36	V
V_{IN_HYS}	Hysteresis(1)			1.0		V
I_{Q_VIN}	Input operating quiescent current (non-switching)	T_A = 25°C, V_{EN} = 3.3 V, V_{FB} = 1.5 V		4		µA
I_{SDN_VIN}	VIN shutdown quiescent current	V_{EN} = 0 V, T_A = 25°C		3		µA
ENABLE						
V_{EN_RISE}	EN voltage rising threshold		1.161	1.263	1.365	V
V_{EN_FALL}	EN voltage falling threshold			0.91		V
V_{EN_HYS}	EN voltage hysteresis		0.275	0.353	0.404	V
V_{EN_WAKE}	EN wake-up threshold		0.4			V
I_{EN}	Input current into EN (non-switching)	V_{EN} = 3.3 V, V_{FB} = 1.5 V		1.65		µA
t_{EN}	EN HIGH to start of switching delay(1)			0.7		ms
INTERNAL LDO VCC						
V_{CC}	Internal LDO VCC output voltage	3.4 V ≤ V_{LDOIN} ≤ 12.5 V		3.3		V
		V_{LDOIN} = 3.1 V, non-switching		3.1		V
V_{CC_UVLO}	VCC UVLO rising threshold	V_{LDOIN} < 3.1 V(1)		3.6		V
		V_{IN} < 3.6 V(2)		3.6		V
$V_{CC\_UVLO\_HYS}$	VCC UVLO hysteresis(2)	Hysteresis below V_{CC_UVLO}		1.1		V
I_{VLDOIN}	Input current into the VLDOIN pin (non-switching, maximum at T_A = 125℃)(3)	V_{EN} = 3.3 V, V_{FB} = 1.5 V		25	31.2	µA
FEEDBACK						
V_{OUT}	Adjustable output voltage range	Over the I_{OUT} range	1		6	V
V_{FB}	Feedback voltage	T_A = 25°C, I_{OUT} = 0 A		1.0		V
V_{FB_ACC}	Feedback voltage accuracy	Over the V_{IN} range, V_{OUT} = 1 V, I_{OUT} = 0 A, F_{SW} = 200 kHz	–1%		+1%	
V_{FB}	Load regulation	T_A = 25°C, 0 A ≤ I_{OUT} ≤ 3 A		0.1%		
V_{FB}	Line regulation	T_A = 25°C, I_{OUT} = 0 A, 4.0 V ≤ V_{IN} ≤ 36 V		0.1%		
I_{FB}	Input current into the FB pin	V_{FB} = 1.0 V		10		nA
CURRENT						
I_{OUT}	Output current	T_A = 25°C	0		3.0	A
I_{OCL}	Output overcurrent (DC) limit threshold			4.9		A
I_{L_HS}	High-side switch current limit	Duty cycle approaches 0%	5.6	6.2	6.8	A
I_{L_LS}	Low-side switch current limit		2.9	3.4	3.8	A
I_{L_NEG}	Negative current limit			–3		A
V_{HICCUP}	Ratio of FB voltage to in-regulation FB voltage to enter hiccup	Not during soft start		40%		
t_W	Short circuit wait time ("hiccup" time before soft start)(1)			80		ms
SOFT START						
t_{SS}	Time from first SW pulse to V_{REF} at 90%	V_{IN} ≥ 4.2 V	3.5	5	7	ms
t_{SS2}	Time from first SW pulse to release of FPWM lockout if output not in regulation(1)	V_{IN} ≥ 4.2 V	9.5	13	17	ms

6.5 Electrical Characteristics (continued)

Limits apply over T_J = –40°C to 125°C, V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{LDOIN} = 5 V, F_{SW} = 800 kHz (unless otherwise noted). Minimum and maximum limits are specified through production test or by design. Typical values represent the most likely parametric norm and are provided for reference only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
PG_{OV}	PG upper threshold – rising	% of V_{OUT} setting	105%	107%	110%	
PG_{UV}	PG lower threshold – falling	% of VOUT setting	92%	94%	96.5%	
PG_{HYS}	PG upper threshold hysteresis (rising and falling)	% of VOUT setting		1.3%		
$V_{IN\_PG\_VALID}$	Input voltage for valid PG output	46-µA pullup, V_{EN} = 0 V	1.0			V
V_{PG_LOW}	Low level PG function output voltage	2-mA pullup to the PG pin, V_{EN} = 3.3 V			0.4	V
I_{PG}	Input current into PG pin when open-drain output is high	V_{PG} = 3.3 V		10		nA
I_{OV}	Pulldown current at the SW node under overvoltage condition			0.5		mA
$t_{PG\_FLT\_RISE}$	Delay time to PG high signal		1.5	2.0	2.5	ms
$t_{PG\_FLT\_FALL}$	Glitch filter time constant for PG function			120		µs
SWITCHING FREQUENCY						
f_{SW_RANGE}	Switching frequency range by R_T or SYNC		200		2200	kHz
f_{SW_RT1}	Default switching frequency by R_T	R_{RT} = 66.5 kΩ	180	200	220	kHz
f_{SW_RT2}	Default switching frequency by R_T	V_{IN} = 12 V, R_{RT} = 5.76 kΩ	1980	2200	2420	kHz
SYNCHRONIZATION						
t_B	Blanking of EN after rising or falling edges(1)		4		28	µs
t_{SYNC_EDGE}	Enable sync signal hold time after edge for edge recognition(1)		100			ns
POWER STAGE						
V_{BOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turn off the high-side switch			2.1		V
t_{ON_MIN}	Minimum ON pulse width(1)	V_{OUT} = 1 V, I_{OUT} = 1 A		55	70	ns
t_{ON_MAX}	Maximum ON pulse width(1)			9		µs
t_{OFF_MIN}	Minimum OFF pulse width	V_{IN} = 4 V, I_{OUT} = 1 A		65	85	ns
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising	158	168	180	°C
T_{HYST}	Thermal shutdown hysteresis (1)			10		°C

(1) Parameter specified by design, statistical analysis and production testing of correlated parameters. Not production tested.
(2) Production tested with V_{IN} = 3 V
(3) This is the current used by the device while not switching, open loop, with FB pulled to +5% of nominal. It does not represent the total input current to the system while regulating. For additional information, reference the *System Characteristics* and the *Input Supply Current* section.

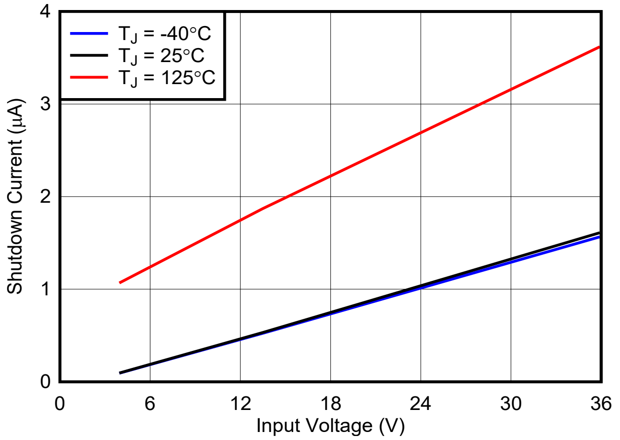
6.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_{IN}	Input supply current when in regulation	V_{IN} = 24 V, V_{OUT} = 3.3 V, V_{EN} = V_{IN}, V_{VLDOIN} = V_{OUT}, F_{SW} = 800 kHz, I_{OUT} = 0 A		10		mA
OUTPUT VOLTAGE						
V_{FB}	Load regulation	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 0.1 A to full load		1		mV
V_{FB}	Line regulation	V_{OUT} = 3.3 V, V_{IN} = 4 V to 36 V, I_{OUT} = 3 A		6		mV
V_{OUT}	Load transient	V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 1 A to 2.5 A at 2 A/µs, $C_{OUT(derated)}$ = 49 µF		50		mV
EFFICIENCY						
η	Efficiency	V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 800 kHz		89.5%		
		V_{OUT} = 3.3 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 800 kHz		87.5%		
		V_{OUT} = 5 V, V_{IN} = 24 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 1 MHz		91%		
		V_{OUT} = 5 V, V_{IN} = 36 V, I_{OUT} = 2.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 1 MHz		88.1%		
		V_{OUT} = 12 V, V_{IN} = 24 V, I_{OUT} = 1.5 A, V_{LDOIN} = V_{OUT}, F_{SW} = 2 MHz		94.1%		

6.7 Typical Characteristics

V_{IN} = 24 V, unless otherwise specified.



V_{EN} = 0 V

Figure 6-1. Shutdown Supply Current

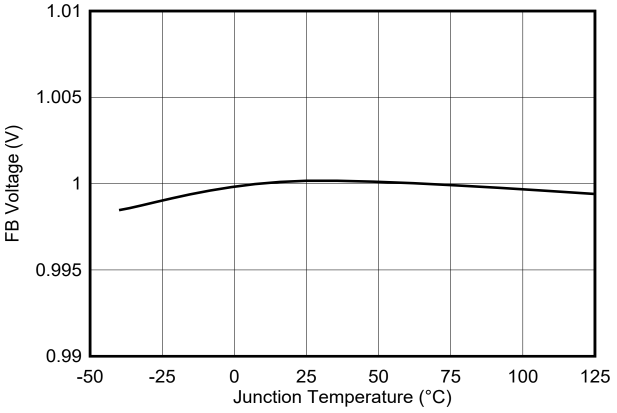


Figure 6-2. Feedback Voltage

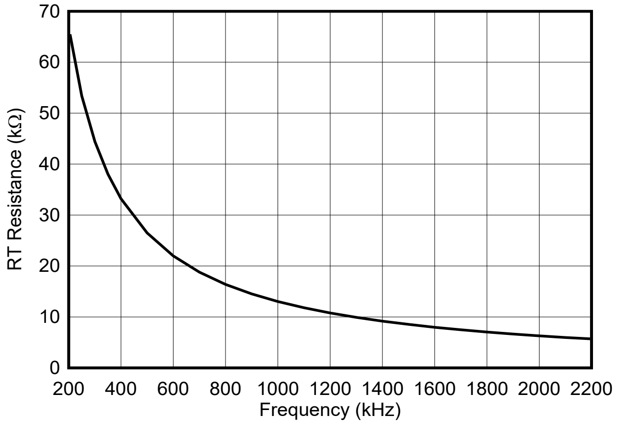


Figure 6-3. Switching Frequency Set by RT Resistor

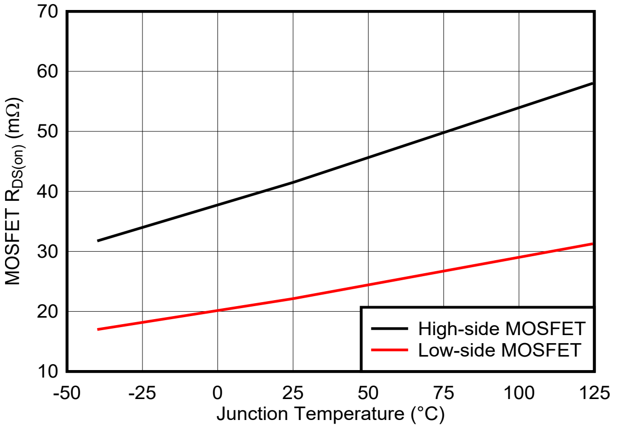


Figure 6-4. High-Side and Low-Side MOSFET $R_{DS(on)}$

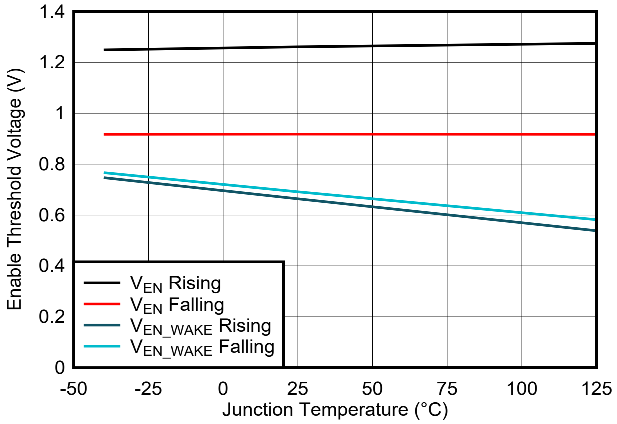


Figure 6-5. Enable Thresholds

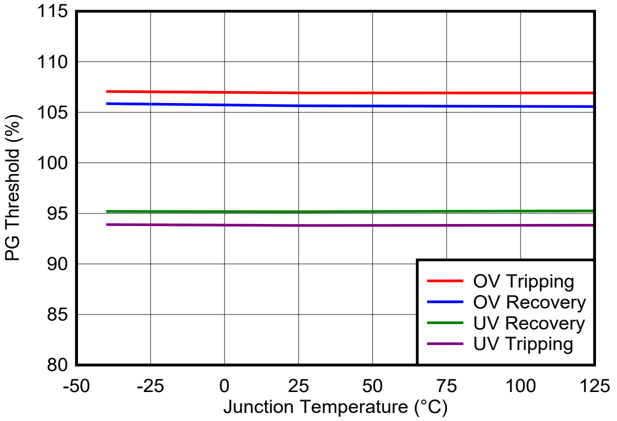
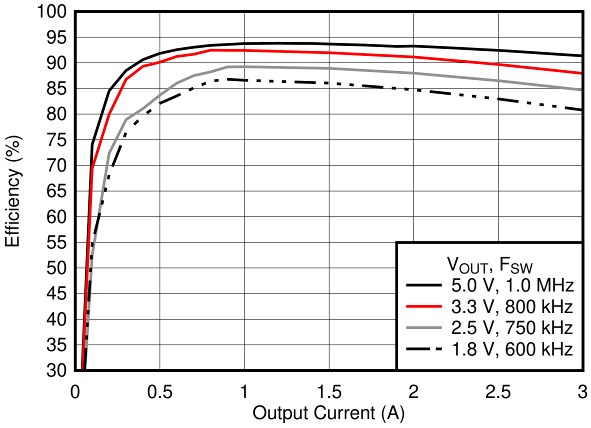


Figure 6-6. Power-Good (PG) Thresholds

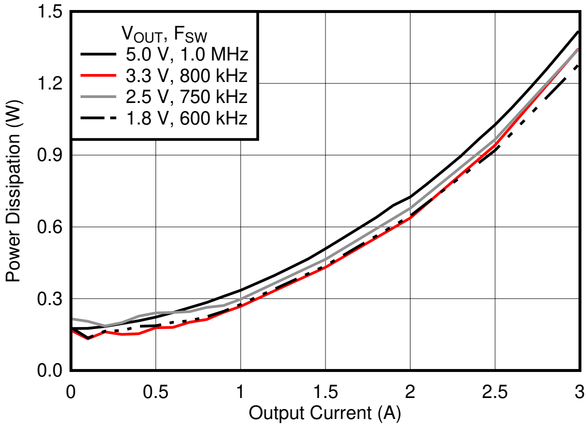
6.8 Typical Characteristics: V_{IN} = 12 V

Refer to Section 8.2 for circuit designs.



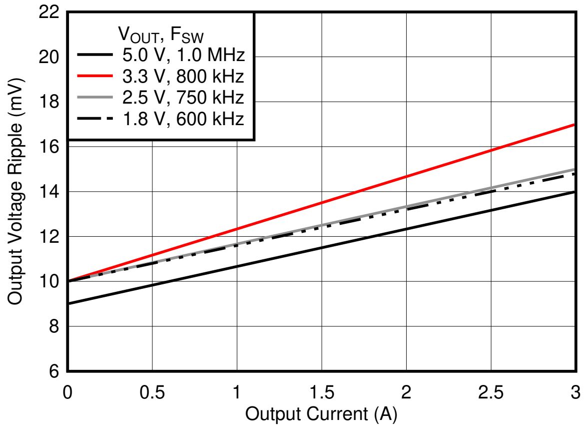
VLDOIN = VOUT

Figure 6-7. Efficiency



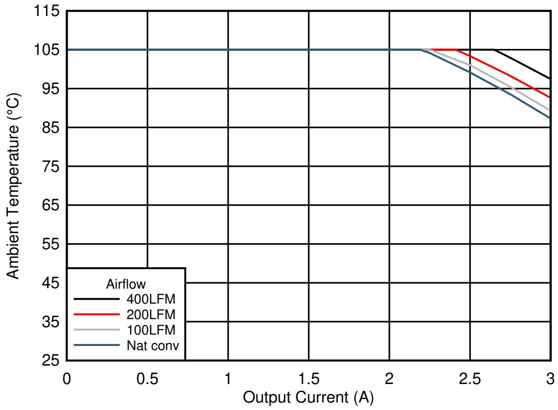
VLDOIN = VOUT

Figure 6-8. Power Dissipation



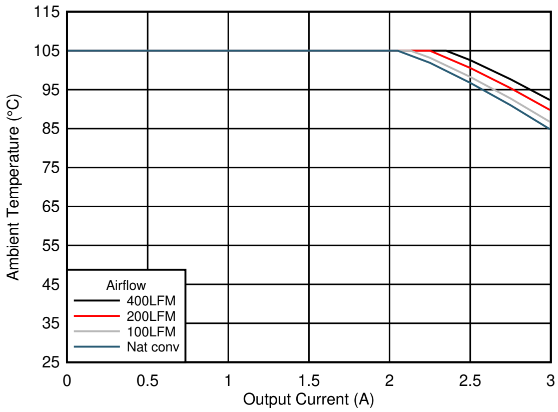
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-9. Output Voltage Ripple



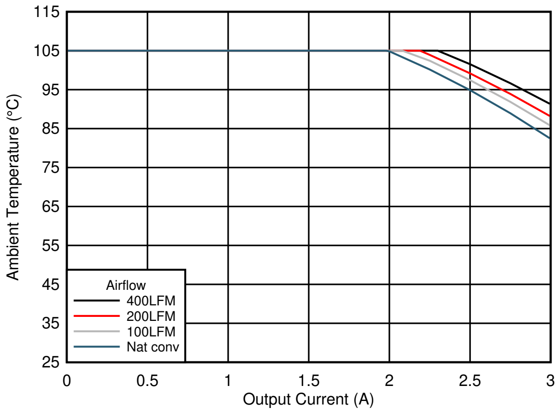
Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-10. Safe Operating Area V_{OUT} = 1.8 V, F_{SW} = 600 kHz



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-11. Safe Operating Area V_{OUT} = 3.3 V, F_{SW} = 800 kHz

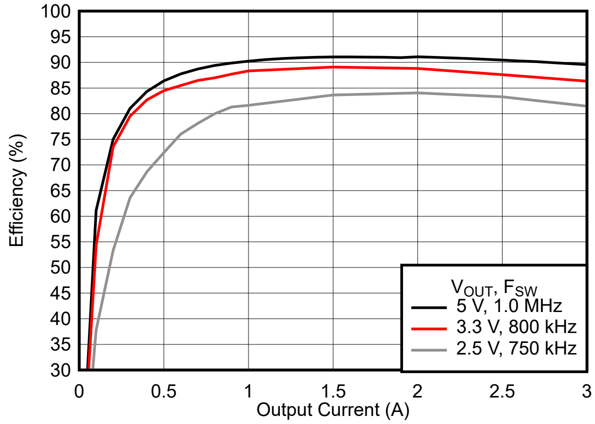


Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-12. Safe Operating Area V_{OUT} = 5.0 V, F_{SW} = 1 MHz

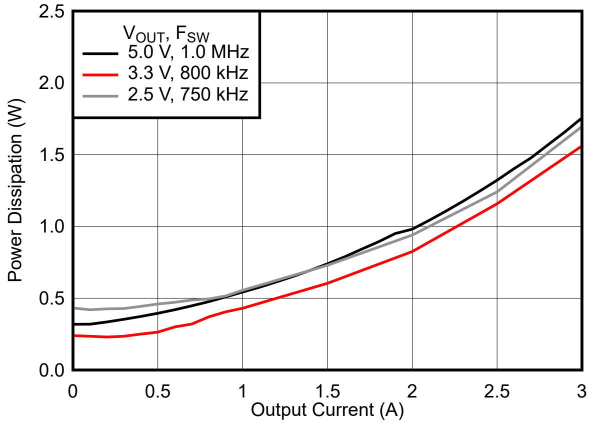
6.9 Typical Characteristics: V_{IN} = 24 V

Refer to Section 8.2 for circuit designs.



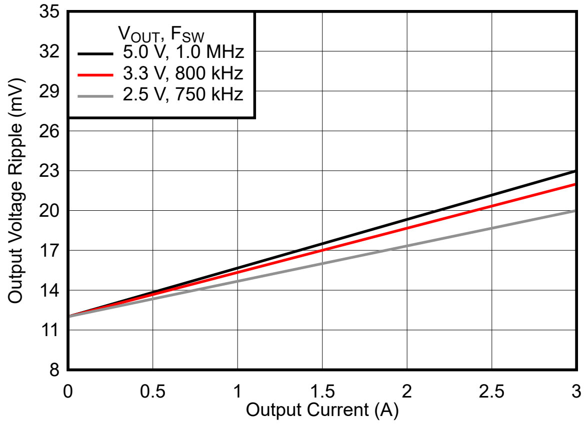
VLDOIN = VOUT

Figure 6-13. Efficiency



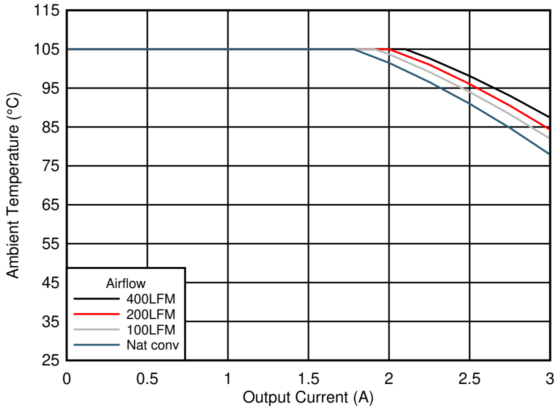
VLDOIN = VOUT

Figure 6-14. Power Dissipation



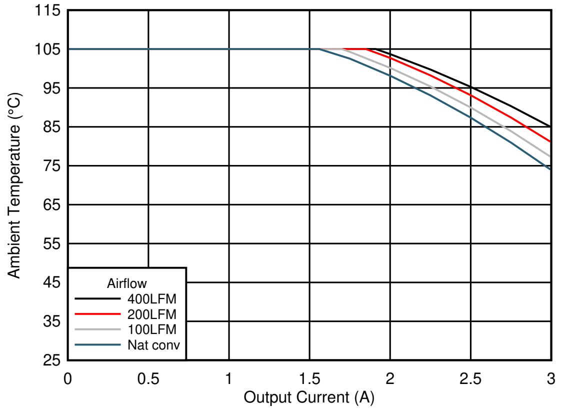
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-15. Output Voltage Ripple



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-16. Safe Operating Area
V_{OUT} = 3.3 V, F_{SW} = 800 kHz

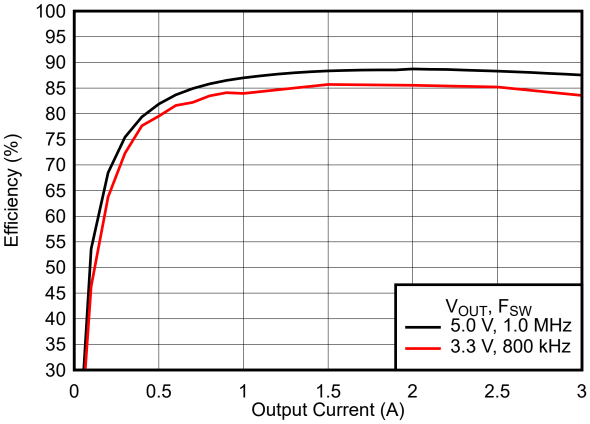


Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-17. Safe Operating Area
V_{OUT} = 5.0 V, F_{SW} = 1 MHz

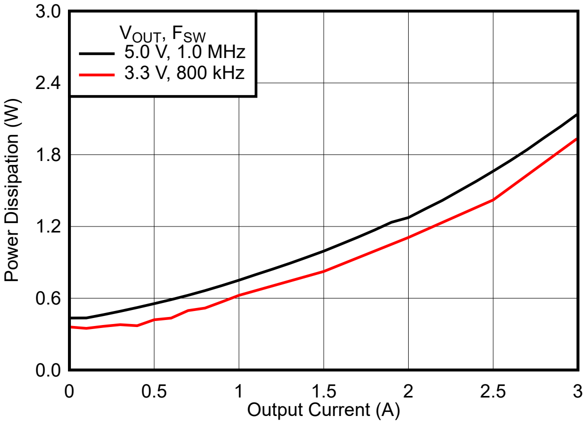
6.10 Typical Characteristics: V_{IN} = 36 V

Refer to Section 8.2 for circuit designs.



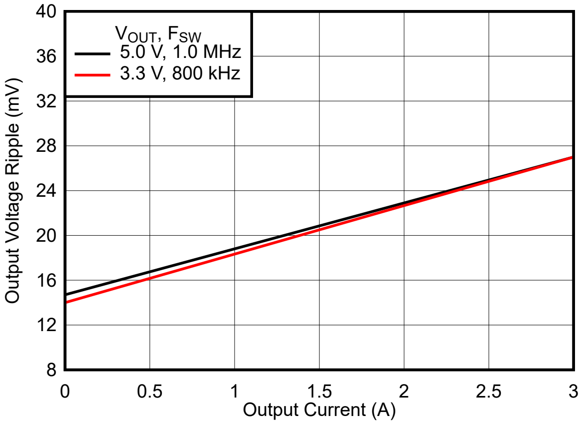
VLDOIN = VOUT

Figure 6-18. Efficiency



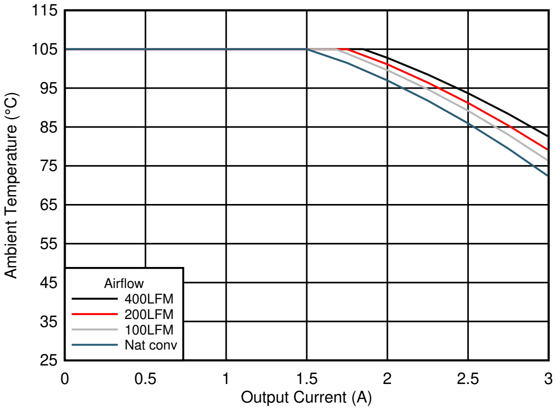
VLDOIN = VOUT

Figure 6-19. Power Dissipation



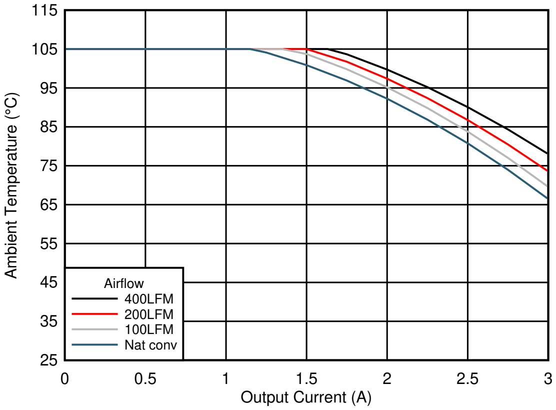
C_{OUT} = 2 × 47-µF ceramic, 25-V, 1206 case size

Figure 6-20. Output Voltage Ripple



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-21. Safe Operating Area
V_{OUT} = 3.3 V, F_{SW} = 800 kHz



Device soldered to a 64-mm × 83-mm, 4-layer PCB

Figure 6-22. Safe Operating Area
V_{OUT} = 5.0 V, F_{SW} = 1 MHz

7 Detailed Description

7.1 Overview

The TLVM13630 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 36-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, and 24-V supply rails. With an integrated power controller, inductor, and MOSFETs, the TLVM13630 delivers up to 3-A DC load current, with high efficiency and ultra-low input quiescent current, in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

With a programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin, the TLVM13630 incorporates specific features to improve EMI performance in noise-sensitive applications:

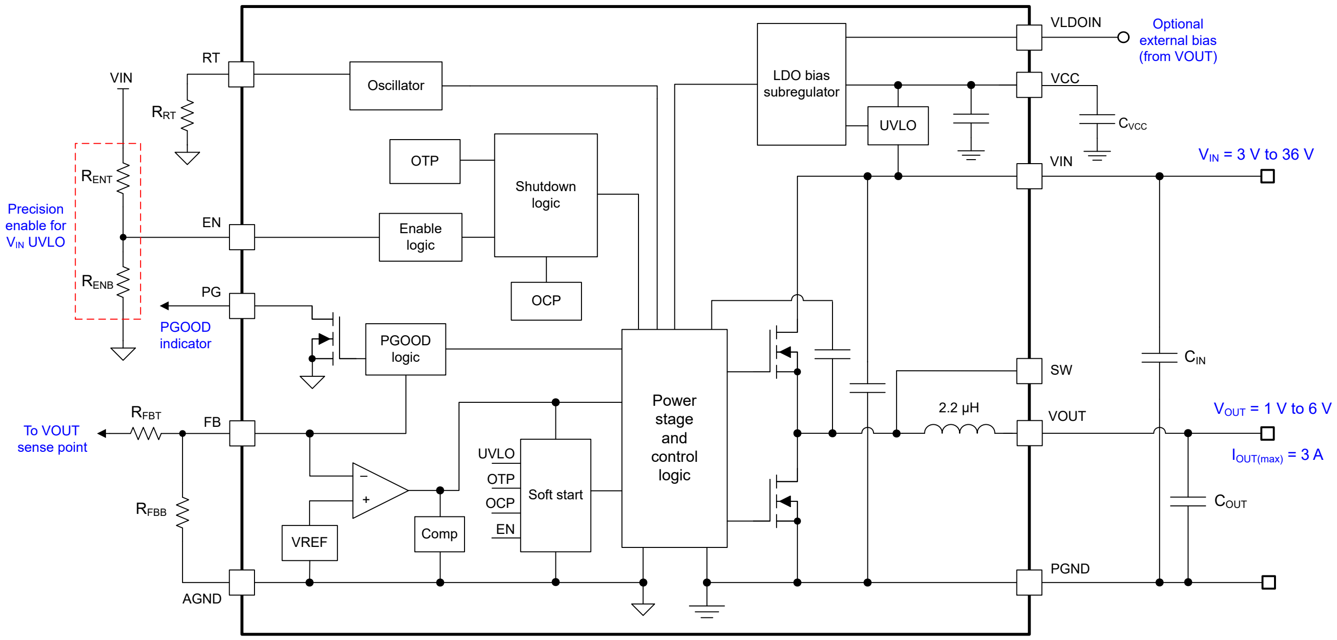
- An optimized package and pinout design enables a shielded switch-node layout that mitigates radiated EMI
- Parallel input and output paths with symmetrical capacitor layouts minimize parasitic inductance, switch-voltage ringing, and radiated field coupling
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range
- Integrated power MOSFETs with enhanced gate drive control enable low-noise PWM switching
- Adjustable switch-node slew rate, which allows optimization of EMI at higher frequency harmonics

The TLVM13630 module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON/OFF capability
- Internally fixed output-voltage soft start with monotonic startup into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery.

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple layout, requiring few external components. See Section 10 for layout example.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Range

With a steady-state input voltage range from 3 V to 36 V, the TLVM13630 module is intended for step-down conversions from typical 12-V, 24-V, and 28-V input supply rails. The schematic circuit in Figure 7-1 shows all the necessary components to implement a TLVM13630-based buck regulator using a single input supply.

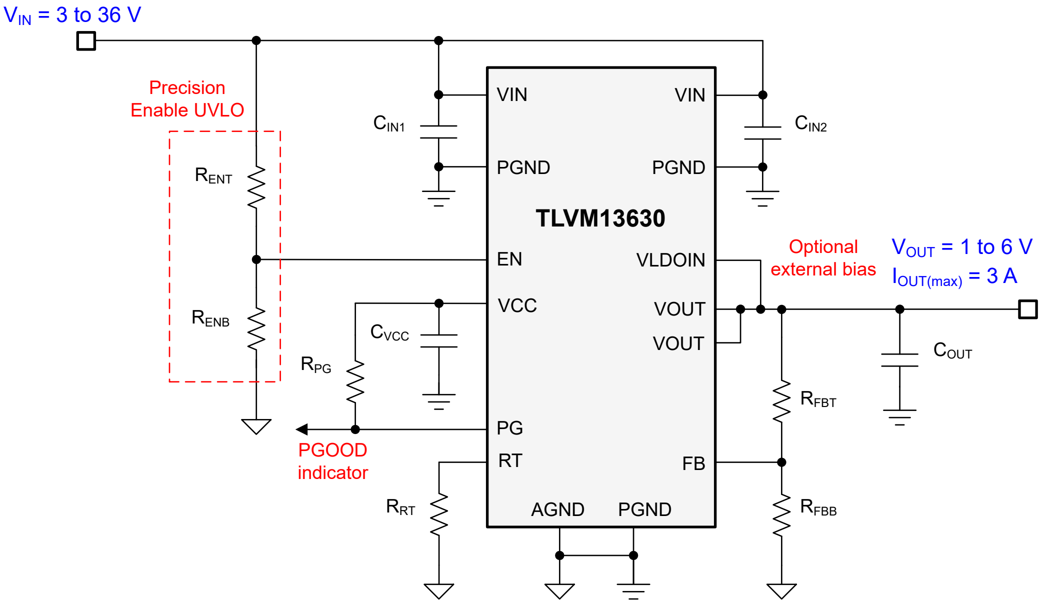


Figure 7-1. TLVM13630 Schematic Diagram with Input Voltage Operating Range of 3 V to 36 V

Take extra care to make sure that the voltage at the VIN pins of the module does not exceed the absolute maximum voltage rating of 40 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.

7.3.2 Adjustable Output Voltage (FB)

The TLVM13630 has an adjustable output voltage range of 1 V to 6 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see Figure 7-2). Connect R_{FBT} between VOUT, at the regulation point, and the FB pin. Connect R_{FBB} between the FB pin and AGND (pin 10). The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be calculated using Equation 1. Table 7-1 lists the standard resistor values for several output voltages and the recommended switching frequency. The minimum required output capacitance for each output voltage is also included in Table 7-1. The capacitance values listed represent the effective capacitance, taking into account the effects of DC bias and temperature variation.

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1\right) \tag{1}$$

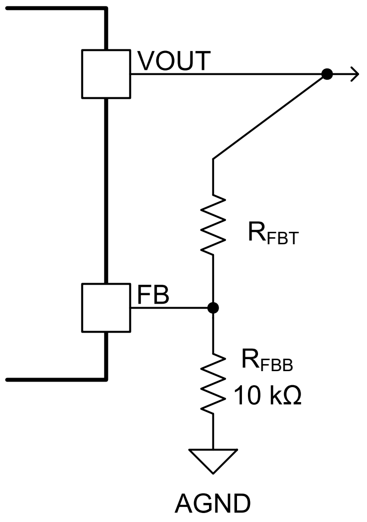


Figure 7-2. FB Resistor Divider

Table 7-1. Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)	V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENDED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)
1.0	Short	400	300	2.5	15	750	65
1.2	2	500	200	3.0	20	750	50
1.5	4.99	500	160	3.3	23.2	800	40
1.8	8.06	600	120	5.0	40.2	1000	25
2.0	10	600	100	6.0	49.9	1000	22

(1) R_{FBB} = 10 kΩ.

Note that higher feedback resistances consume less DC current, which is mandatory if light-load efficiency is critical. However, R_{FBT} larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. It is important to keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see Section 10.

7.3.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. Equation 2 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the capacitors should be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \cdot \left(I_{OUT}{}^{2} \cdot (1 - D) + \frac{\Delta I_L^2}{12} \right)} \tag{2}$$

where

- $D = V_{OUT} / V_{IN}$ = the module duty cycle

Ideally, the DC and AC components of input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} – I_{IN}) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, Equation 3 gives the peak-to-peak ripple voltage amplitude:

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{3}$$

Equation 4 gives the input capacitance required for a particular load current:

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \tag{4}$$

where

- ΔV_{IN} is the input voltage ripple specification.

The TLVM13630 requires a minimum of 2 × 4.7 µF of ceramic type input capacitance. Only use high-quality ceramic type capacitors with sufficient voltage and temperature rating. The ceramic input capacitors provide a low impedance source to the converter in addition to supplying the ripple current and isolating switching noise from other circuits. Additional capacitance can be required for applications with transient load requirements. The voltage rating of input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. Table 7-2 includes a preferred list of capacitors by vendor.

Table 7-2. Recommended Input Capacitors

VENDOR[1]	DIELECTRIC	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE RATING (V)	CAPACITANCE [2] (µF)
TDK	X7R	C3216X7R1H475K160AC	1206	50	4.7
Murata	X7R	GRM31CR71H475KA12L	1206	50	4.7
TDK	X7R	CGA6P3X7R1H475K250AB	1210	50	4.7
Murata	X7S	GCM31CC71H475KA03L	1206	50	4.7

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

7.3.4 Output Capacitors

Table 7-1 lists the TLVM13630 minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(MIN)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See Table 7-3 for a preferred list of output capacitors by vendor.

Table 7-3. Recommended Output Capacitors

VENDOR[1]	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE (V)	CAPACITANCE[2] (µF)
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7S	GCJ31CC71E106KA15L	1206	25	10
Murata	X6S	GRM31CC81E226K	1206	25	22
Murata	X7R	GRM32ER71E226M	1210	25	22

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

7.3.5 Switching Frequency (RT)

The switching frequency range of the TLVM13630 is 200 kHz to 2.2 MHz. The switching frequency can easily be set by connecting a resistor (R_{RT}) between the RT pin and AGND. Use Equation 5 to calculate the R_{RT} value for a desired frequency or simply select from Table 7-4. Note that a resistor value outside of the recommended range can cause the device to shut down. This prevents unintended operation if RT pin is shorted to ground or left open. Do not apply a pulsed signal to this pin to force synchronization.

The switching frequency must be selected based on the output voltage setting of the device. See Table 7-4 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for common input voltages.

$$R_{RT}\left[k\Omega\right]=\frac{13.46}{F_{SW}\left[MHz\right]}-0.44 \tag{5}$$

Table 7-4. Switching Frequency Versus Output Voltage (I_{OUT} = A)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
200	66.5	1.0	2.0	1.0	2.0	1.0	1.5	1.0	1.5
400	33.2	1.0	3.0	1.0	4.0	1.0	3.3	1.2	3.0
600	22.1	1.0	3.5	1.0	6.0	1.5	6.0	1.8	5.0
800	16.5	1.0	3.5	1.0	6.0	1.5	6.0	2.5	6.0
1000	13.0	1.0	3.0	1.0	6.0	2.0	6.0	3.0	6.0
1200	10.7	1.0	3.0	1.5	6.0	2.5	6.0	3.5	6.0
1400	9.09	1.0	3.0	1.5	6.0	3.0	6.0	4.0	6.0
1600	8.06	1.0	3.0	1.5	6.0	3.0	6.0	4.5	6.0
1800	6.98	1.0	3.0	2.0	6.0	3.5	6.0	5.0	6.0
2000	6.34	1.2	2.5	2.0	6.0	4.0	6.0	5.5	6.0
2200	5.626	1.2	2.5	2.0	6.0	4.5	6.0	-	-

7.3.6 Output ON/OFF Enable (EN) and V_{IN} UVLO

The EN pin provides precision ON and OFF control for the TLVM13630. Once the EN/SYNC pin voltage exceeds the threshold voltage and V_{IN} is above the minimum turn-on threshold, the device starts operation. The simplest way to enable the TLVM13630 is to connect EN directly to VIN. This allows the TLVM13630 to start up when V_{IN} is within its valid operating range. However, many applications benefit from the employment of an enable divider network as shown in Figure 7-3, which establishes a precision input undervoltage lockout (UVLO). This can be used for sequencing, to prevent re-triggering the device when used with long input cables, or to reduce the occurrence of deep discharge of a battery power source. An external logic signal can also be used to drive the enable input to toggle the output on and off and for system sequencing or protection.

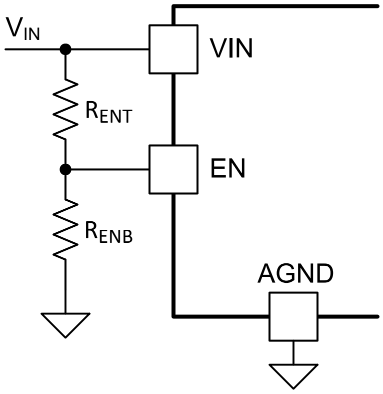


Figure 7-3. VIN UVLO Using the EN Pin

R_{ENB} can be calculated using Equation 6.

$$R_{ENB}\left[k\Omega\right] = R_{ENT}\left[k\Omega\right] \cdot \left(\frac{V_{EN\_RISE}\left[V\right]}{V_{IN(on)}\left[V\right] - V_{EN\_RISE}\left[V\right]}\right) \tag{6}$$

where

- A typical value for R_{ENT} is 100 kΩ.
- V_{EN} is 1.263 V (typical).
- $V_{IN(ON)}$ is the desired start-up input voltage.

7.3.7 Power Good Monitor (PG)

The TLVM13630 provides a PGOOD signal to indicate when the output voltage is within regulation. Use the PGOOD signal for output monitoring, fault protection, or start-up sequencing of downstream converters. The PGOOD pin voltage goes low when the feedback voltage is outside of the PGOOD thresholds. This occurs during the following:

- While the device is disabled
- In current limit
- In thermal shutdown
- During normal start-up, when the output voltage has not reach its regulation value

A glitch filter prevents false flag operation for short excursions (<120 μs typical) of the output voltage, such as during line and load transients.

PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 20 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is above 1 V (typical). Use the PG signal for start-up sequencing of downstream regulators, as shown in Figure 7-4, or for fault protection and output monitoring.

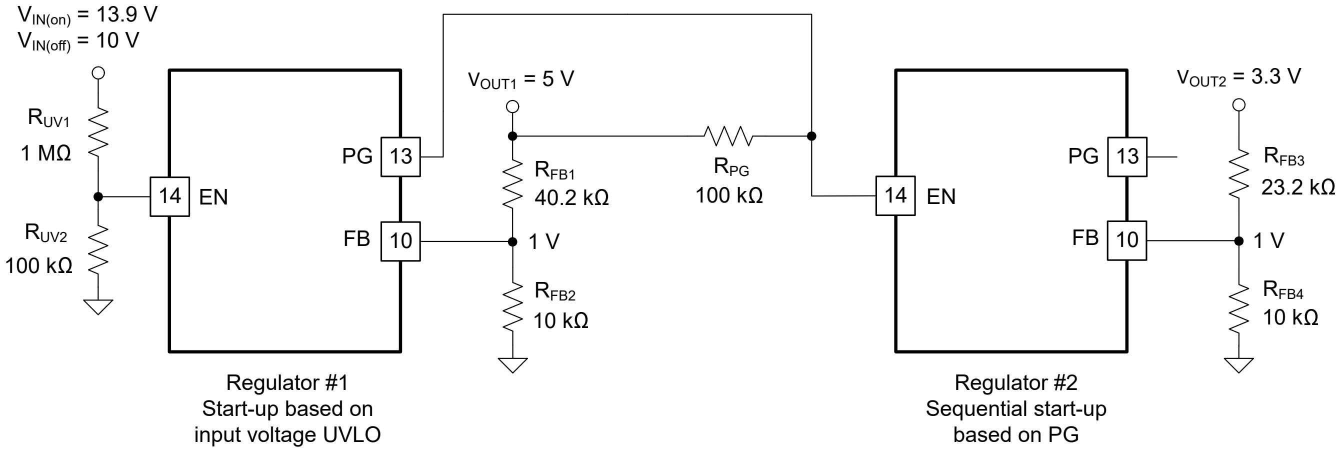


Figure 7-4. TLVM13630 Sequencing Implementation Using PG and EN

7.3.8 Internal LDO, VCC Output, and VLDOIN Input

The TLVM13630 has an internal LDO to power internal circuitry. The VCC pin is the output of the internal LDO. This pin must not be used to power external circuitry. Connect a high-quality, 1-µF capacitor from this pin to AGND, close to the device pins. Do not load the VCC pin or short it to ground.

The VLDOIN pin is an optional input to the internal LDO. Connect an optional high quality 0.1-µF to 1-µF capacitor from this pin to ground for improved noise immunity.

The LDO generates the VCC voltage from one of the two inputs: V_{IN} or the VLDOIN input. When VLDOIN is tied to ground or below 3.1 V, the LDO is powered from V_{IN}. When VLDOIN is tied to a voltage higher than 3.1 V, the LDO input is powered from VLDOIN. VLDOIN voltage must be lower than both V_{IN} and 12.5 V.

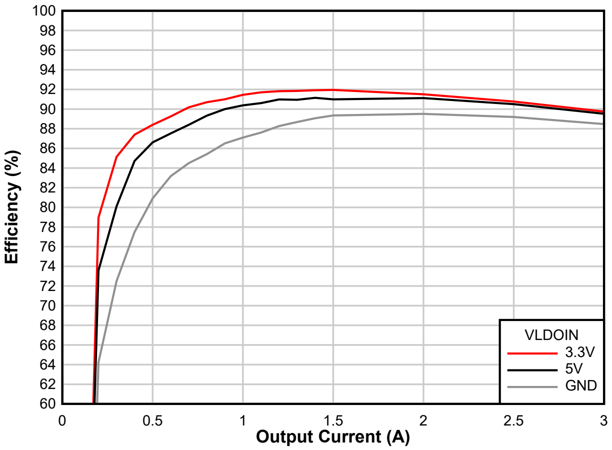
The VLDOIN input is designed to reduce the LDO power loss. The LDO power loss is:

$$P_{LDO\text{-}LOSS} = I_{LDO} \times (V_{IN\_LDO} - V_{VCC}) \quad (7)$$

The higher the difference between the input and output voltages of the LDO, the more loss occurs to supply the same LDO output current. The VLDOIN input provides an option to supply the LDO with a lower voltage than V_{IN}, to reduce the difference of the input and output voltages of the LDO and reduce power loss. For example, if the LDO current is 10 mA at a certain frequency with V_{IN} = 24 V and V_{OUT} = 5 V. The LDO loss with VLDOIN tied to ground is equal to 10 mA × (24 V – 3.3 V) = 207 mW, while the loss with VLDOIN tied to V_{OUT} (5 V) is equal to 10 mA × (5 V – 3.3 V) = 17 mW.

The efficiency improvement is more significant at light and mid loads because the LDO loss is a higher percentage of the total loss. The improvement is more significant with higher switching frequency because the LDO current is higher at higher switching frequency. The improvement is more significant when V_{IN} » V_{OUT} because the voltage difference is higher.

Figure 7-5 shows typical efficiency waveforms with VLDOIN powered by different input voltages.



V_{IN} = 24 V

V_{OUT} = 5 V

F_{SW} = 1 MHz

I_{LDO} = 10 mA

Figure 7-5. Efficiency improvements with VLDOIN (VOUT = 5 V)

7.3.9 Overcurrent Protection (OCP)

The TLVM13630 is protected from overcurrent conditions using cycle-by-cycle current limiting of the peak inductor current. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

The TLVM13630 employs hiccup overcurrent protection if there is an extreme overload. In hiccup mode, the regulator is shut down and kept off for 80 ms (typical) before the TLVM13630 tries to start again. If an overcurrent or short-circuit fault condition still exists, hiccup repeats until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, and prevents overheating and potential damage to the device. Once the fault is removed, the module automatically recovers and returns to normal operation.

7.3.10 Thermal Shutdown

Thermal shutdown is an integrated self-protection used to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 168°C (typical) to prevent further power dissipation and temperature rise. Junction temperature decreases after shutdown, and the TLVM13630 attempts to restart when the junction temperature falls to 158°C (typical).

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN/SYNC pin provides ON and OFF control for the TLVM13630. When V_{EN} is below approximately 0.4 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The input quiescent current in shutdown mode drops to 0.6 µA (typical). The TLVM13630 also employs internal undervoltage protection. If the input voltage is below its UV threshold, the regulator remains off.

7.4.2 Standby Mode

The internal LDO has a lower enable threshold than the regulator itself. When V_{EN} is above 1.1 V (maximum) and below the precision enable threshold of 1.263 V (typical), the internal LDO is on and regulating. The precision enable circuitry is turned on once the internal V_{CC} is above its UVLO threshold. The switching action and voltage regulation are not enabled until $V_{EN/SYNC}$ rises above the precision enable threshold.

7.4.3 Active Mode

The TLVM13630 is in active mode when V_{IN} and V_{EN} are above their relevant thresholds and no fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum start-up voltage.

8 Applications and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLVM13630 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. The following section describes the design procedure to configure the TLVM13630 power module. To expedite and streamline the design process, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases.

As mentioned previously, the TLVM13630 also integrates several optional features to meet system design requirements, including the following:

- Precision enable with hysteresis
- External adjustable UVLO
- Adjustable SW node slew rate
- Power-good indicator

The following application circuit detailed shows the TLVM13630 configuration options suitable for several application use cases.

8.2 Typical Applications

The following are sample typical applications along with design procedure for the implemenation of TLVM13630.

8.2.1 Design 1: 3-A Synchronous Buck Regulator for Industrial Applications

Figure 8-1 shows the schematic diagram of a 5-V, 3-A buck regulator with a switching frequency of 1 MHz. The nominal input voltage for the sample design is 24 V. A resistor R_{RT} of 13 kΩ sets the free-running switching frequency at 1 MHz. An optional SYNC input signal allows adjustment of the switching frequency for this specific application.

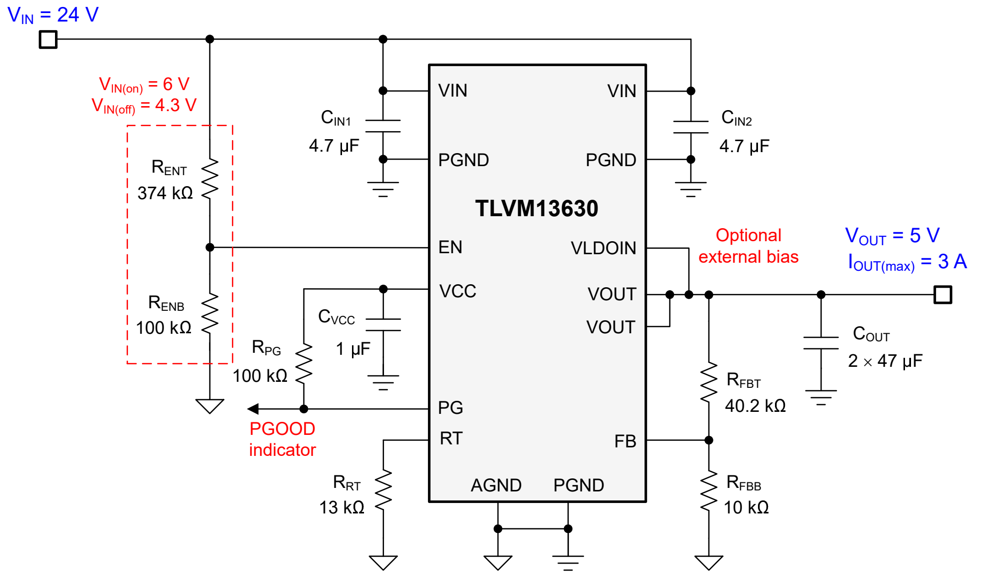


Figure 8-1. Circuit Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters and follow the design procedures in Section 8.2.1.2.

Table 8-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage	24 V
Output voltage	5 V
Output current	0 A to 3 A
Switching Frequency	1 MHz

Table 8-2 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 8-2. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER[1]	PART NUMBER
C_{IN1}, C_{IN2}	2	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 100 V, X7S, 1206, ceramic	Murata	GRM31CC72A475KE11L
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
		1 µF, 16 V, X5R, 0402, ceramic	Taiyo Yuden	EMK105BJ105KVHF
U_1	1	TLVM13630 36-V, 3-A synchronous buck module	Texas Instruments	TLVM13630RDLR

(1) See the *Third-Party Products Disclaimer*.

More generally, the TLVM13630 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63603 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Setpoint

The output voltage of the TLVM13630 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBB} can be selected from Table 7-1 or calculated using Equation 8:

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1\right) \quad (8)$$

For the desired output voltage of 5 V, the formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

8.2.1.2.3 Switching Frequency Selection

The recommended switching frequency for standard output voltages can be found in Table 7-1. For a 5-V output, the recommended switching frequency is 1 MHz. To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND.

8.2.1.2.4 Input Capacitor Selection

The TLVM13630 requires a minimum input capacitance of 2 × 4.7-µF ceramic type. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, select two 4.7-µF, 50-V, 1210 case size, ceramic capacitors.

8.2.1.2.5 Output Capacitor Selection

For a 5-V output, the TLVM13630 requires a minimum of 25 µF of effective output capacitance for proper operation (see Table 7-1). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

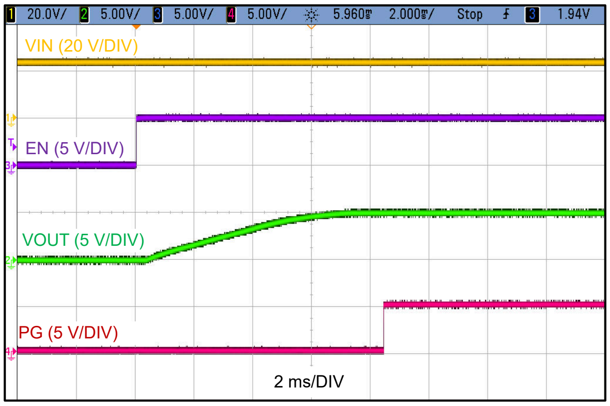
For this design example, select two 47-µF, 10-V, 1210 case size, ceramic capacitors, which have a total effective capacitance of approximately 48 µF at 5 V.

8.2.1.2.6 Other Connections

- Connect VLDOIN to VOUT to improve efficiency.
- Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

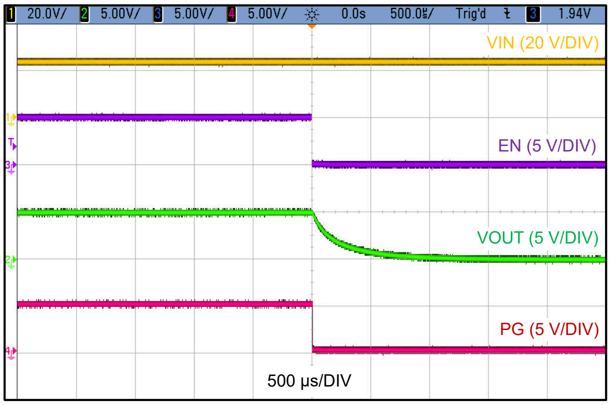
8.2.1.3 Application Curves

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 3 A, and F_{SW} = 1 MHz.



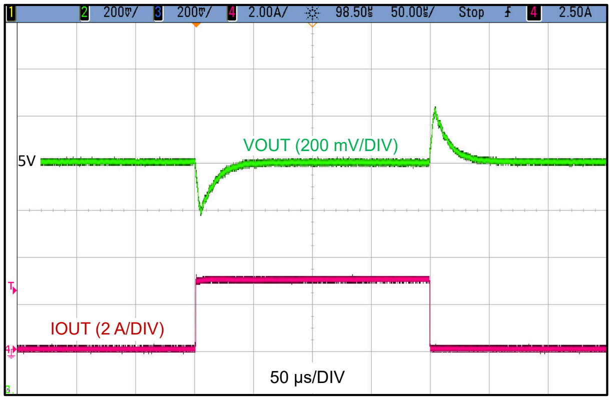
V_{IN} = 24 V V_{OUT} = 5 V

Figure 8-2. Start-Up Waveforms



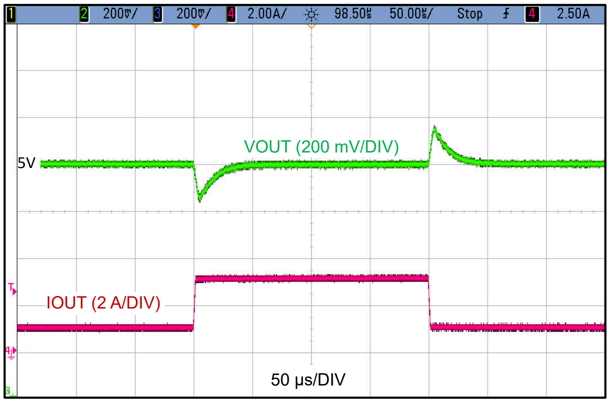
V_{IN} = 24 V V_{OUT} = 5 V

Figure 8-3. Shutdown Waveforms



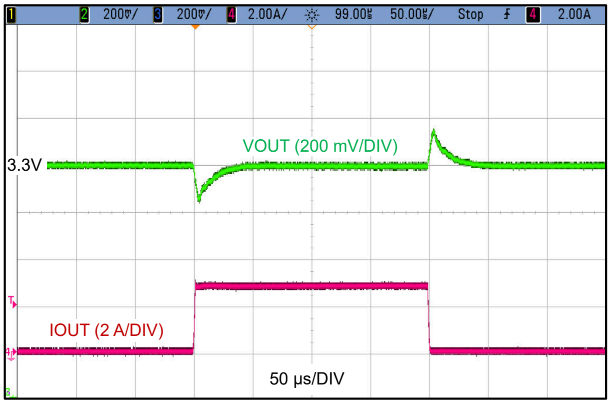
V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-4. Load Transient 0 A to 3 A, 1 A/µs



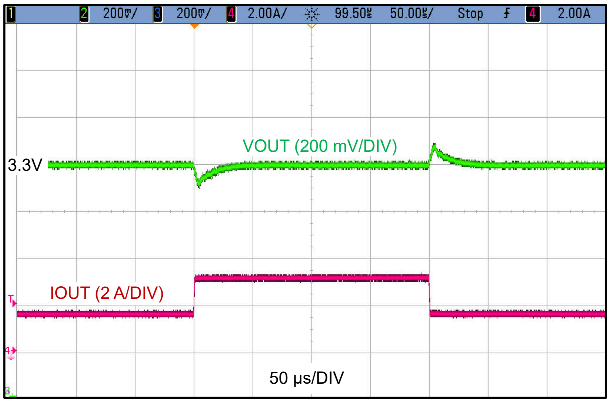
V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-5. Load Transient 1.5 A to 3 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-6. Load Transient 0 A to 3 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 3.3 V F $_{SW}$ = 1 MHz
C_{OUT} = 2 × 47µF

Figure 8-7. Load Transient 1.5 A to 3 A, 1 A/µs

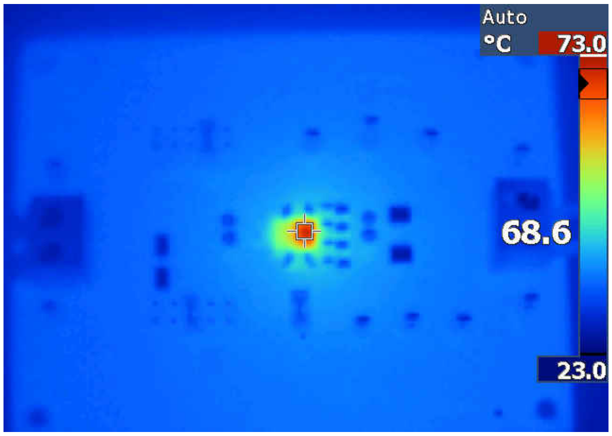


Figure 8-8. Thermal Image V_{IN} = 12 V, V_{OUT} = 3.3 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

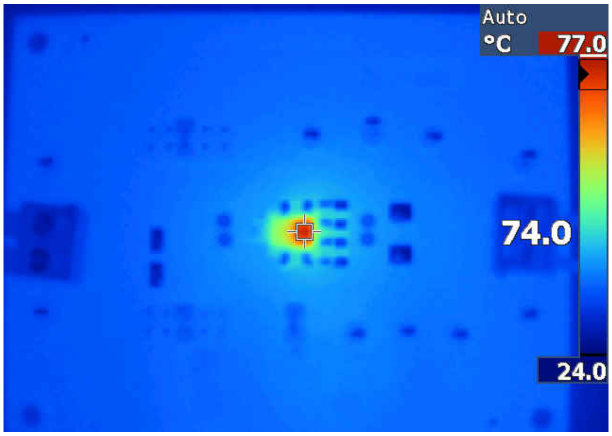


Figure 8-9. Thermal Image V_{IN} = 12 V, V_{OUT} = 5 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

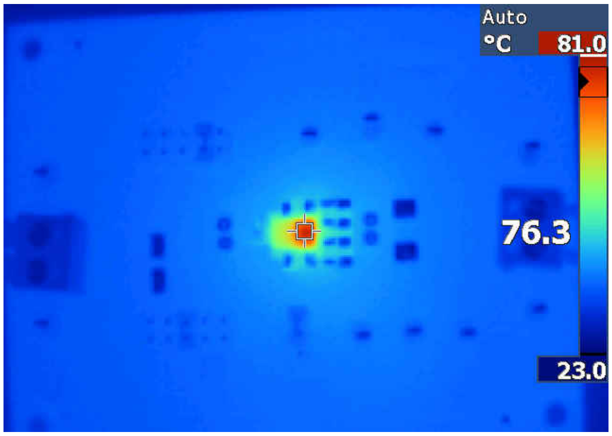


Figure 8-10. Thermal Image V_{IN} = 24 V, V_{OUT} = 3.3 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

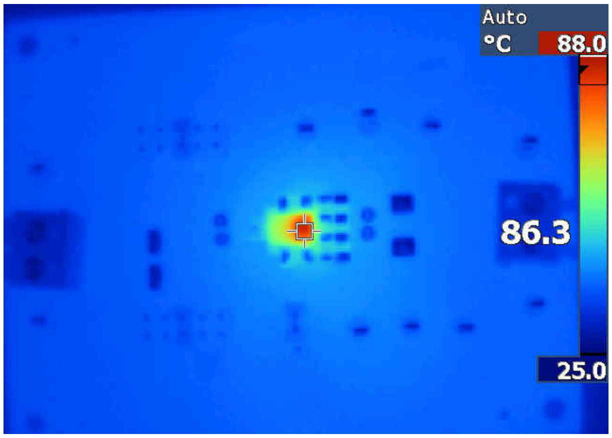


Figure 8-11. Thermal Image V_{IN} = 24 V, V_{OUT} = 5 V, F_{SW} = 1 MHz, I_{OUT} = 3 A

8.2.2 Design 2: Inverting Buck-Boost Regulator with a –5-V Output

Figure 8-12 shows the schematic diagram of a –5-V inverting buck-boost regulator with a switching frequency of 1 MHz. The input voltage range for the sample design is 12 V to 24 V.

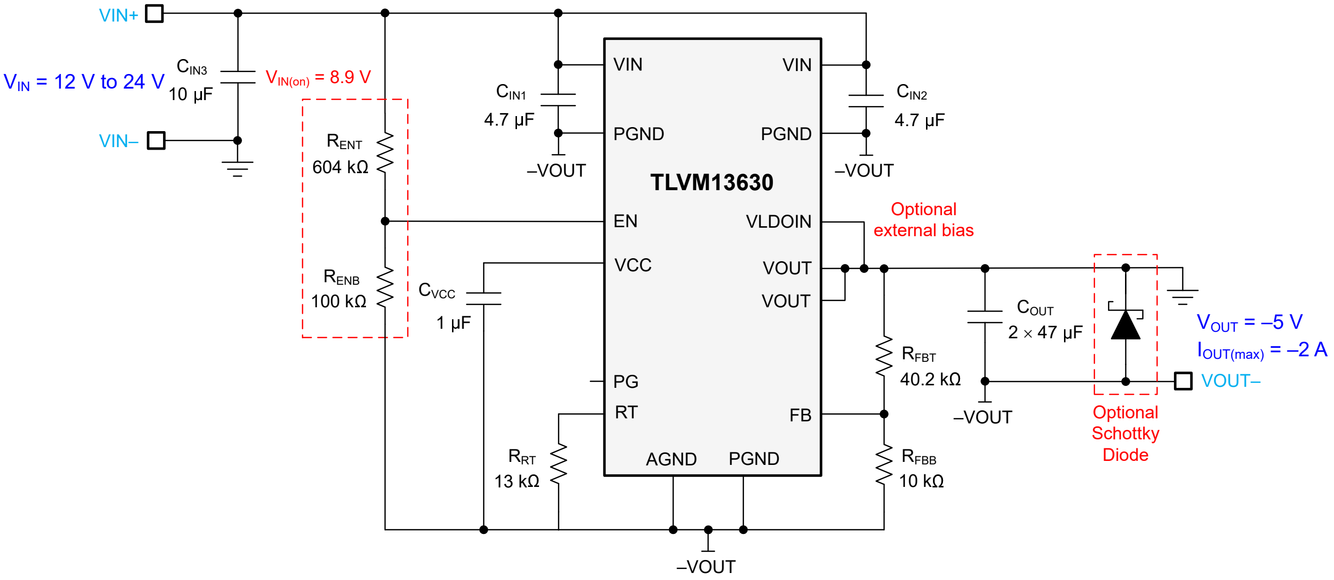


Figure 8-12. Circuit Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-3 as the input parameters and follow the design procedures in Section 8.2.2.2.

Table 8-3. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage	12 to 24 V
Output voltage	–5 V
Output current	0 A to 2 A
Switching frequency	1 MHz

Table 8-4 gives the selected module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 8-4. List of Materials for Application Circuit 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER(1)	PART NUMBER
C_{IN1}, C_{IN2}, C_{IN3}	3	4.7 µF, 50 V, X7R, 1210, ceramic	Taiyo Yuden	UMK325B7475KN-TR
			TDK	CGA6P3X7R1H475K250AB
		4.7 µF, 50 V, X7S, 1206, ceramic	Murata	GCM31CC71H475KA03K
C_{OUT1}, C_{OUT2}	2	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476ME15L
			AVX	1210ZC476MAT2A
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	Murata	GCM188R71C105KA64J
U_1	1	TLVM13630 36-V, 3-A synchronous buck module	Texas Instruments	TLVM13630RDLR

More generally, the TLVM13630 module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Voltage Setpoint

The output voltage of the TLVM13630 device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. Calculate the value for R_{FBT} using Equation 9:

$$R_{FBT}\left[k\Omega\right] = R_{FBB}\left[k\Omega\right] \cdot \left(\frac{V_{OUT}\left[V\right]}{1V} - 1\right) \quad (9)$$

For the desired output voltage of – 5 V, enter the absolute value of 5 V for the V_{OUT} in Equation 9. The formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}.

8.2.2.2.2 IBB Maximum Output Current

The achievable output current with an *IBB topology* using the TLVM13630 is $I_{OUT(max)} = I_{LDC(max)} \times (1 - D)$, where $I_{LDC(max)}$ = 3 A is the rated current of the module and $D = |V_{OUT}| / (V_{IN} + |V_{OUT}|)$ is the module duty cycle. Therefore in the case of V_{IN} = 12 V and the V_{OUT} = –5 V, the maximum output current is 2.1 A.

8.2.2.2.3 Switching Frequency Selection

To set the switching frequency to 1 MHz, connect a 13.0-kΩ resistor between the RT pin and AGND pins of the module based on Equation 5.

8.2.2.2.4 Input Capacitor Selection

The TLVM13630 requires a minimum input capacitance of 2 × 4.7-µF ceramic type between the VIN pins and PGND pins as close as possible to the module. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. In the inverting buck-boost configuration the maximum voltage between VIN and PGND pin of the module is equal to $V_{IN} + |V_{OUT}|$.

For this design, two 4.7-µF, 50-V, 1210 case size, ceramic capacitors are selected.

8.2.2.2.5 Output Capacitor Selection

The TLVM13630 requires a minimum of 25 µF of effective output capacitance for proper operation. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, a two 47-µF, 10-V, 1210 case size, ceramic capacitors are used which have a total effective capacitance of approximately 48 µF at 5 V.

8.2.2.2.6 Other Connections

Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

The right-half-plane zero of an IBB topology is at its lowest frequency at minimum input voltage. However, it does not appear at low frequency for a –5 V output and thus has minimal effect on the loop response for this application.

In the inverting buck-boost configuration, the input capacitor C_{IN} and output capacitor C_{OUT} can formed an AC capacitive divider during a fast V_{IN} transient or hot-plugged event at the input. This event will resulted in a positive voltage spike at the output that may disturb the load. In this case, an optional Schottky diode may be installed between –VOUT and GND as shown in Figure 8-12 to clamp the output spike.

8.2.2.3 Application Curves

Unless otherwise indicated, V_{IN} = 12 V, V_{OUT} = –5 V, and F_{SW} = 1 MHz.

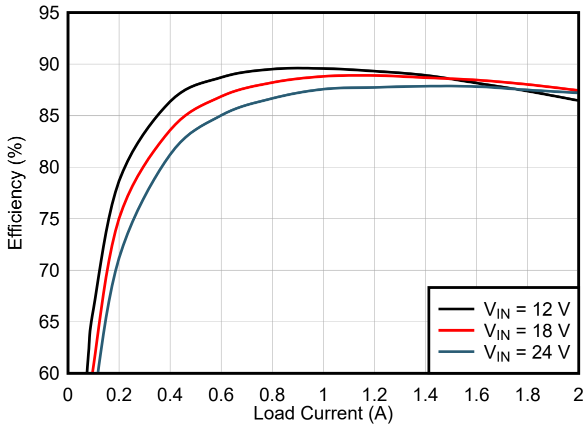


Figure 8-13. Efficiency Curves

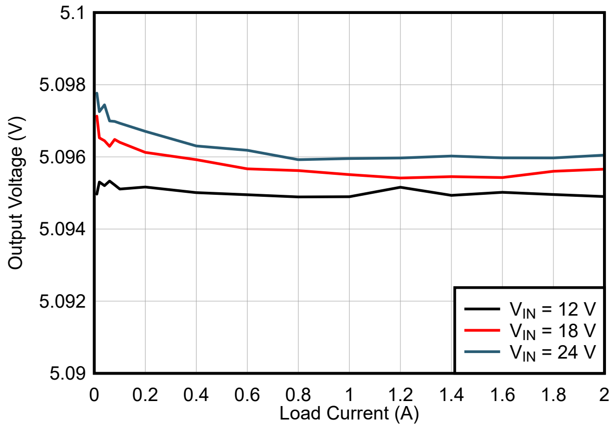
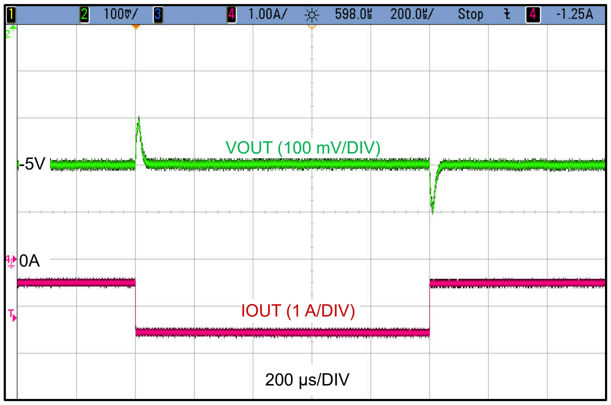
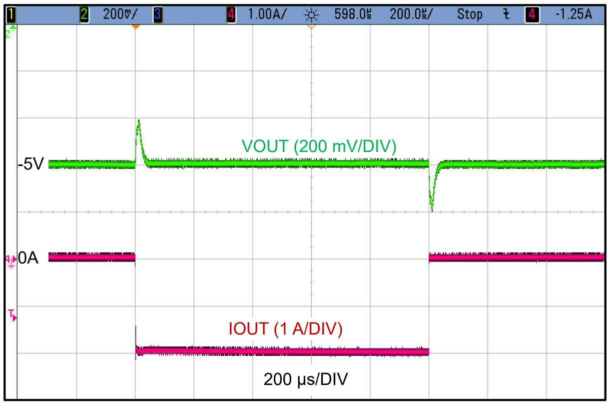


Figure 8-14. Load Regulation



V_{IN} = 12 V V_{OUT} = –5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 8-15. Load Transient –0.5 A to –1.5 A, 1 A/µs



V_{IN} = 12 V V_{OUT} = –5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 47 µF

Figure 8-16. Load Transient 0 A to –2 A, 1 A/µs

8.2.2.3.1 EMI

The TLVM13630 is compliant with EN55011 radiated emissions. Figure 8-17, Figure 8-18, and Figure 8-19 show typical examples of radiated emission plots for the TPSM63603 which is in the same family of parts. The graphs include the plots of the antenna in the horizontal and vertical positions.

8.2.2.3.1.1 EMI Plots

EMI plots were measured using the standard TPSM63603EVM.

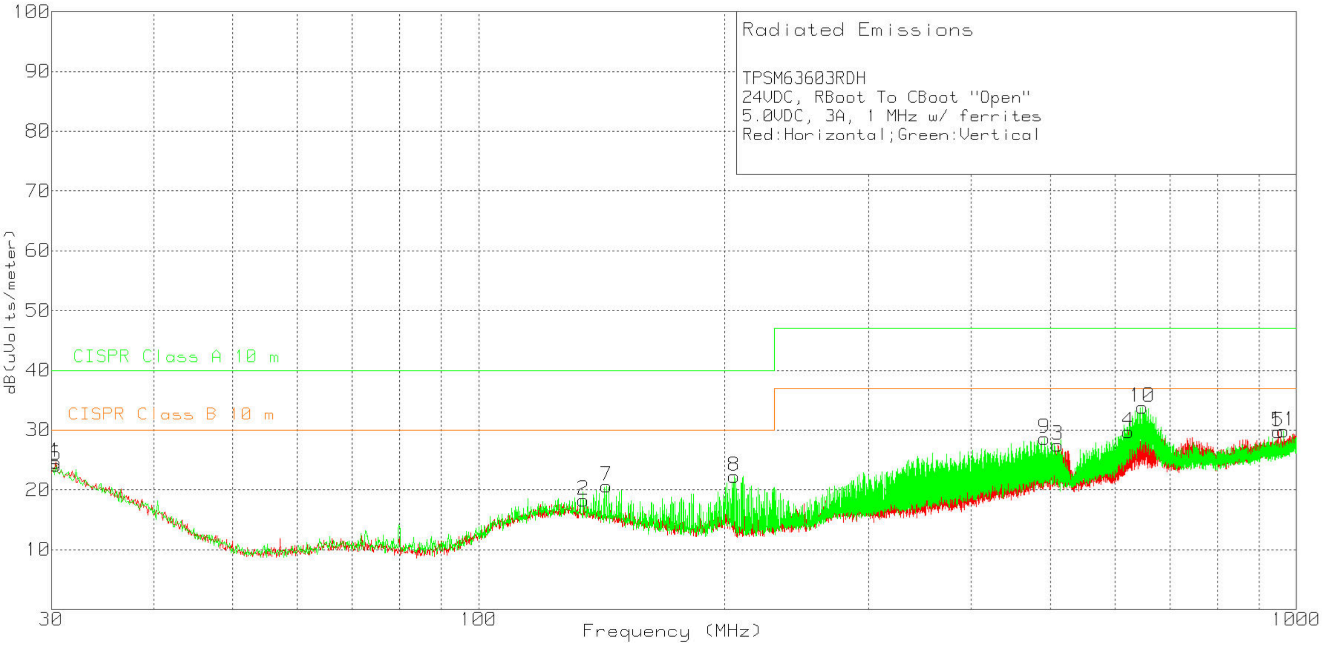


Figure 8-17. Radiated Emissions 24-V Input, 5-V Output, 3-A Load

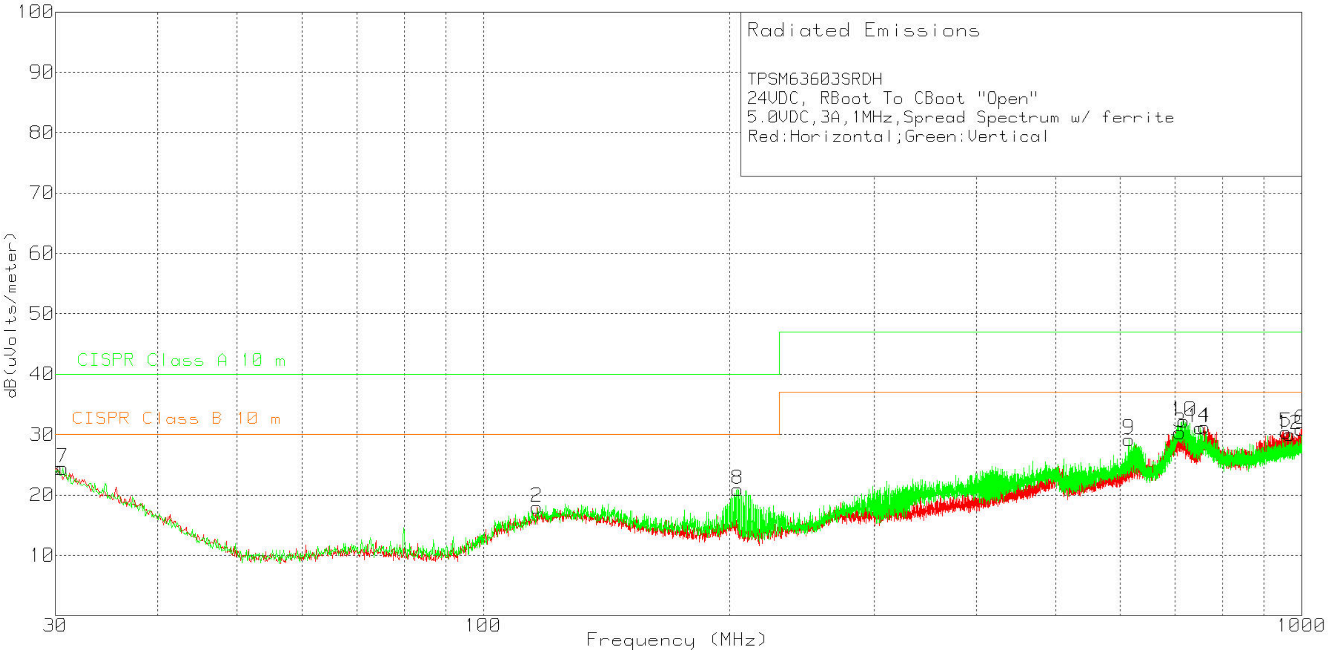


Figure 8-18. Radiated Emissions 24-V Input, 5-V Output, 3-A Load, Spread Spectrum

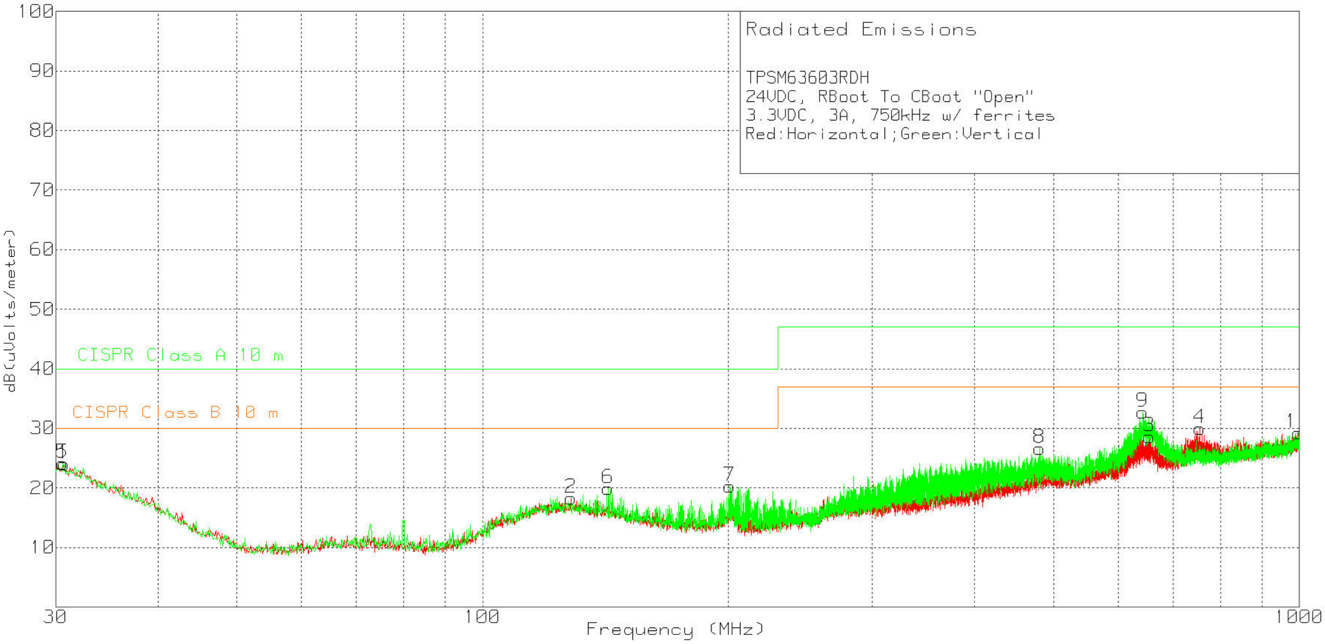


Figure 8-19. Radiated Emissions 24-V Input, 3.3-V Output, 3-A Load

9 Power Supply Recommendations

The TLVM13630 buck module is designed to operate over a wide input voltage range of 3 V to 36 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with Equation 10.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{10}$$

where

- η = efficiency

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

10 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.1 Layout Guidelines

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Figure 10-1 and Figure 10-2 show a typical PCB layout. Some considerations for an optimized layout are:

- Use large copper areas for power planes (VIN, VOUT, and PGND) to minimize conduction loss and thermal stress.
- Place ceramic input and output capacitors close to the device pins to minimize high-frequency noise.
- Locate additional output capacitors between the ceramic capacitors and the load.
- Connect AGND to PGND at a single point.
- Place R_{FBT} and R_{FBB} as close as possible to the FB pin.
- Use multiple vias to connect the power planes to internal layers.

10.2 Layout Example

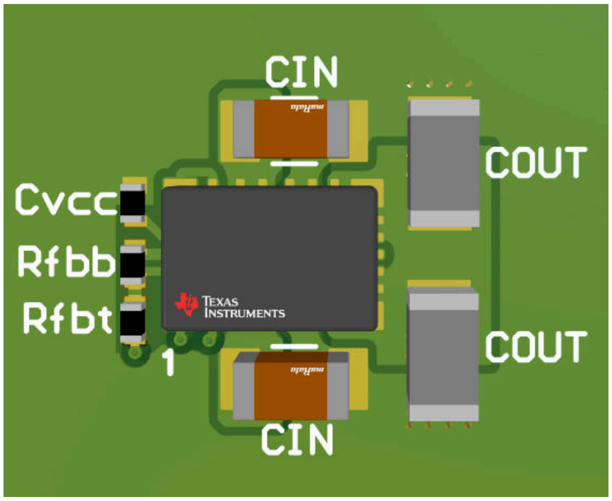


Figure 10-1. Typical Top-Layer Layout

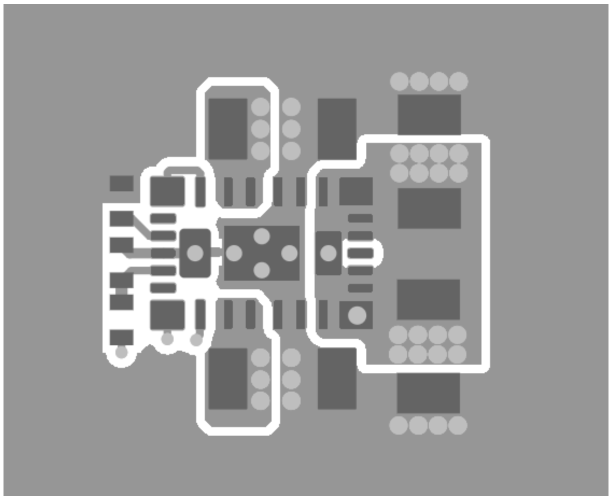


Figure 10-2. Typical Top-Layer

10.2.1 Package Specifications

Table 10-1. Package Specifications Table

TPSM63603		VALUE	UNIT
Weight		123	mg
Flammability	Meets UL 94 V-0		
MTBF calculated reliability	Per Bellcore TR-332, 50% stress, T_A = 40°C, ground benign	84	MHrs

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

With an input operating voltage from 3 V to 36 V and rated output current from 2 A to 6 A, the TLVM13620/30/40/60 family of synchronous buck power modules specified in Table 11-1 provides flexibility, scalability and optimized solution size for a range of applications. These modules enable DC/DC solutions with high density, low EMI and increased flexibility. Available EMI mitigation features include RBOOT-configured switch-node slew rate control, fixed switching frequency, and integrated input bypass capacitors. All modules are rated for an ambient temperature up to 105°C.

Table 11-1. Synchronous Buck DC/DC Power Module Family

DC/DC MODULE	RATED I_{OUT}	PACKAGE	DIMENSIONS	FEATURES	EMI MITIGATION
TLVM13620	2 A	B0QFN (30)	4.0 × 6.0 × 1.8 mm	RT adjustable F_{SW}, precision enable	Integrated BOOT capacitor
TLVM13630	3 A				
TLVM13640	4 A	B3QFN (20)	5.0 × 5.5 × 4.0 mm		Integrated input, VCC and BOOT capacitors
TLVM13660	6 A				

For development support see the following:

- TLVM13630 *Quickstart Calculator*
- TLVM13630 *Simulation Models*
- For TI's reference design library, visit the *TI Reference Design library*.
- For TI's WEBENCH Design Environment, visit the *WEBENCH® Design Center*.
- To design a low-EMI power supply, review TI's comprehensive *EMI Training Series*.
- To design an inverting buck-boost (IBB) regulator, visit *DC/DC inverting buck-boost modules*.
- TI Reference Designs:
  - *Multiple Output Power Solution For Kintex 7 Application*
  - *Arria V Power Reference Design*
  - *Altera Cyclone V SoC Power Supply Reference Design*
  - *Space-optimized DC/DC Inverting Power Module Reference Design With Minimal BOM Count*
  - *3- To 11.5-V_{IN}, –5-V_{OUT}, 1.5-A Inverting Power Module Reference Design For Small, Low-noise Systems*
- Technical Articles:
  - *Powering Medical Imaging Applications With DC/DC Buck Converters*
  - *How To Create A Programmable Output Inverting Buck-boost Regulator*
- To view a related device of this product, see the LM61460 36-V, 6-A synchronous buck converter.

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM63603 device with WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.

- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper
- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- Texas Instruments, *Using the TPSM53602/3/4 for Negative Output Inverting Buck-Boost Applications* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLVM13630RDHR	Active	Production	B0QFN (RDH) | 30	3000 | LARGE T&R	Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 125	13630
TLVM13630RDHR.A	Active	Production	B0QFN (RDH) | 30	3000 | LARGE T&R	Exempt	NIPDAU	Level-3-260C-168 HR	-40 to 125	13630
TLVM13630RDHRG4	Active	Production	B0QFN (RDH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	13630
TLVM13630RDHRG4.A	Active	Production	B0QFN (RDH) | 30	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	13630

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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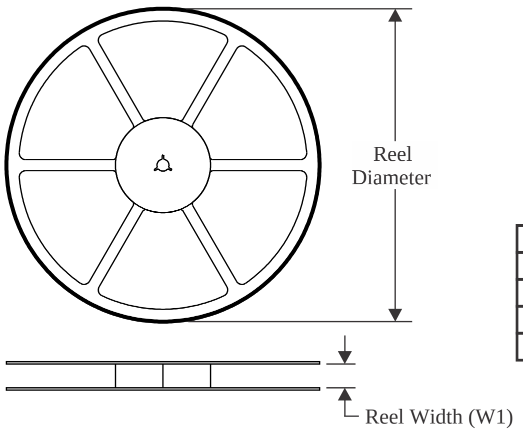
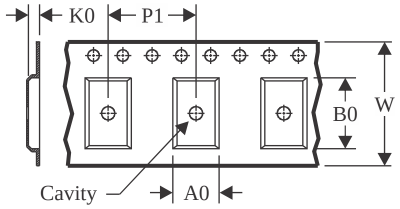
TAPE AND REEL INFORMATION

REEL DIMENSIONS

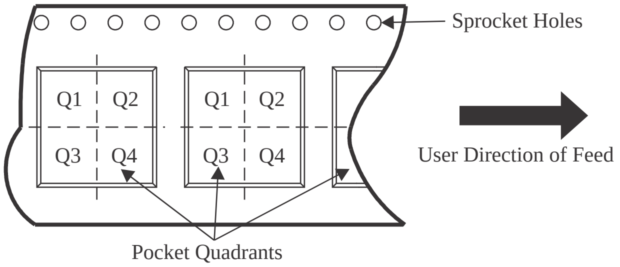


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

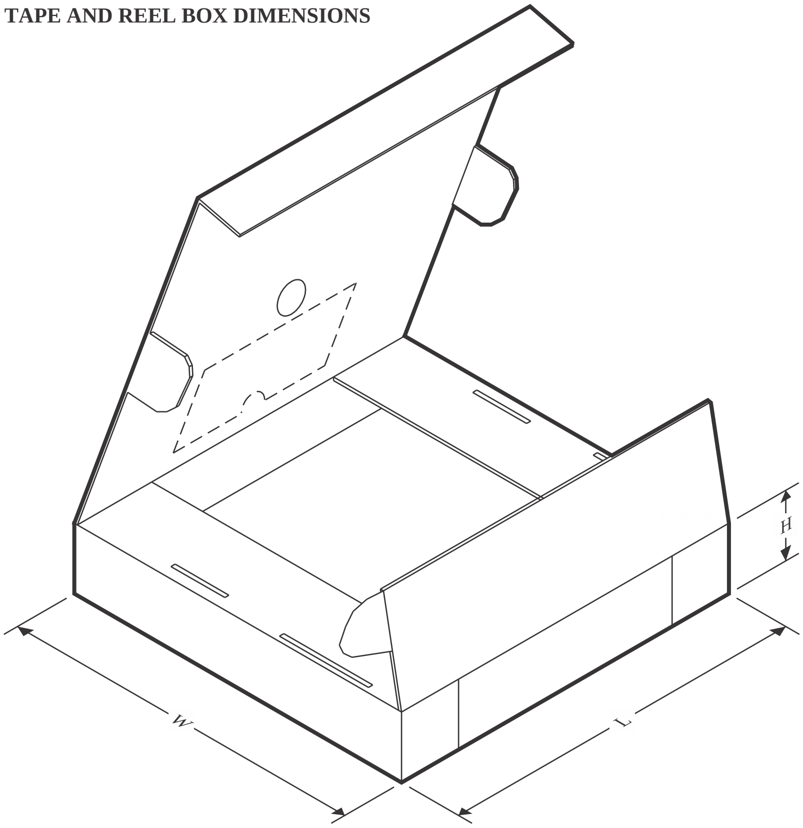
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLVM13630RDHR	B0QFN	RDH	30	3000	330.0	16.4	4.25	6.25	2.1	8.0	16.0	Q1
TLVM13630RDHRG4	B0QFN	RDH	30	3000	330.0	16.4	4.25	6.25	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

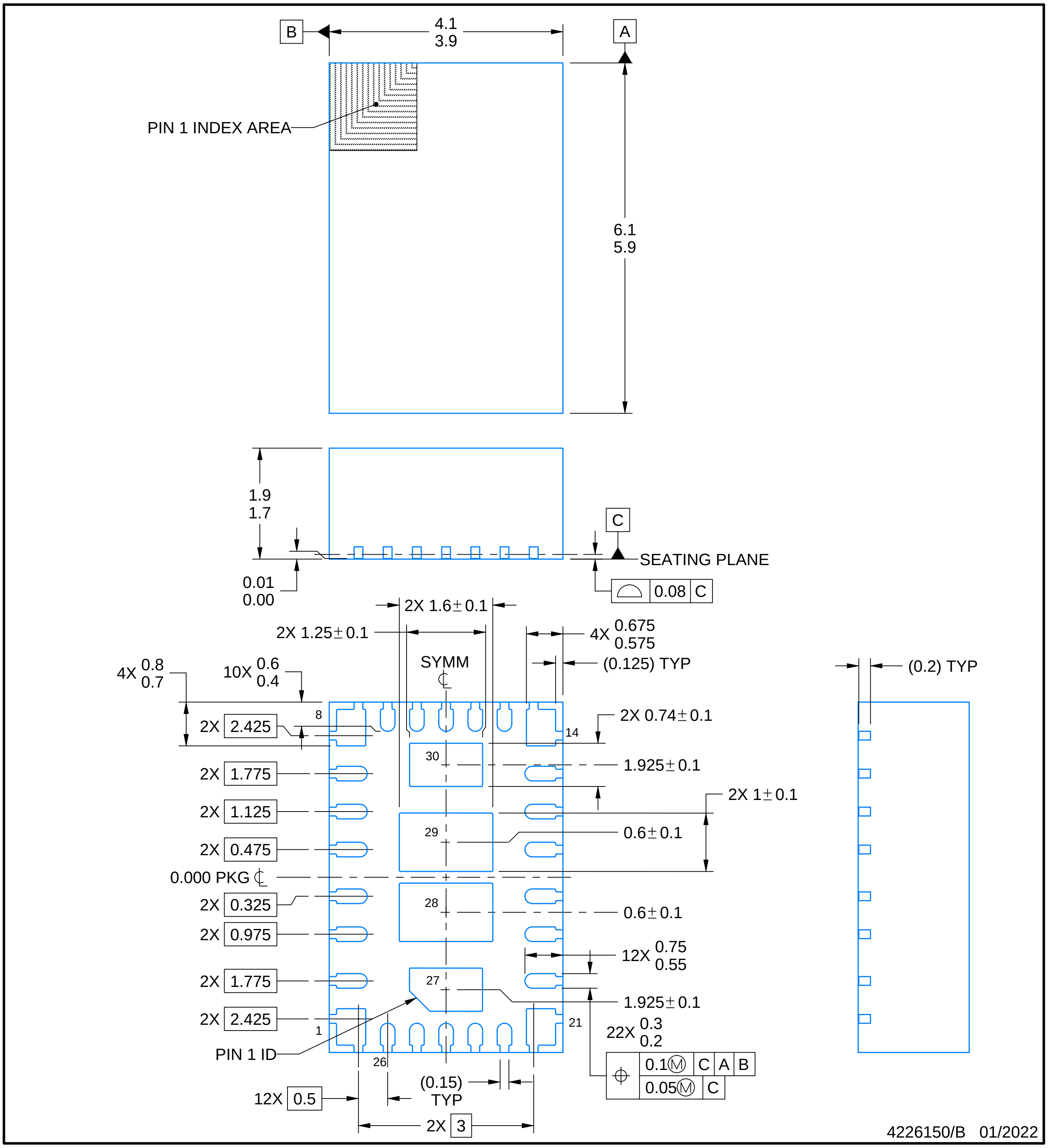
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLVM13630RDHR	B0QFN	RDH	30	3000	336.0	336.0	48.0
TLVM13630RDHRG4	B0QFN	RDH	30	3000	336.0	336.0	48.0

PACKAGE OUTLINE

RDH0030A

B0QFN - 1.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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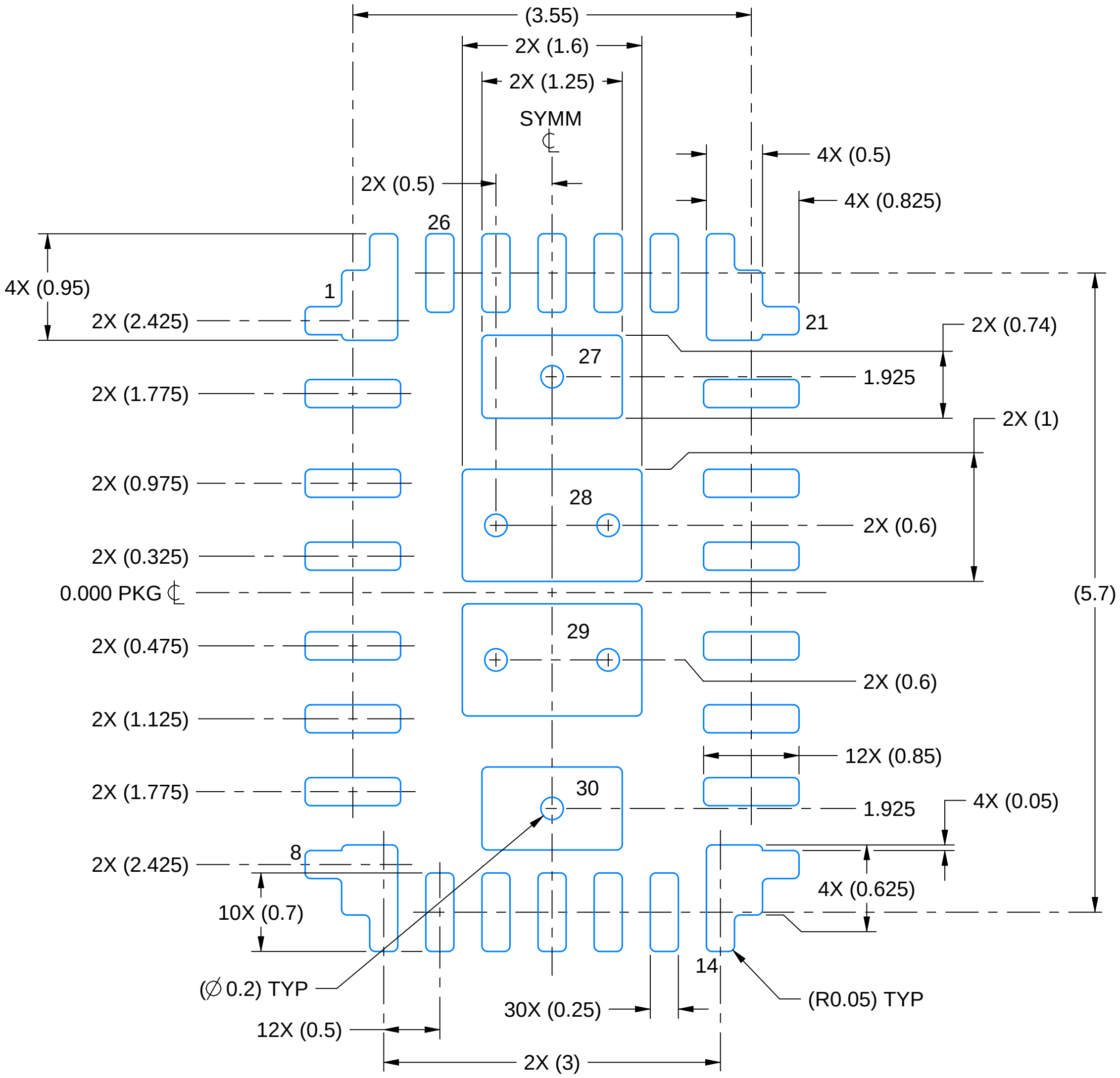
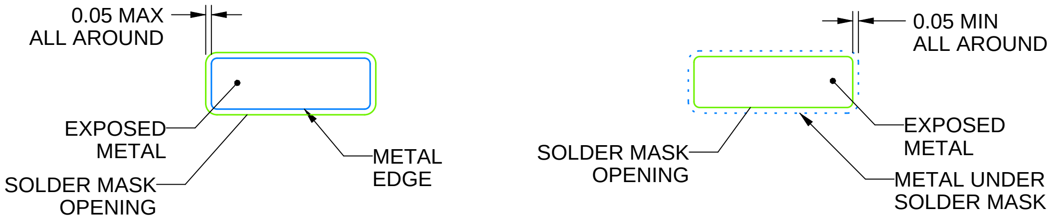
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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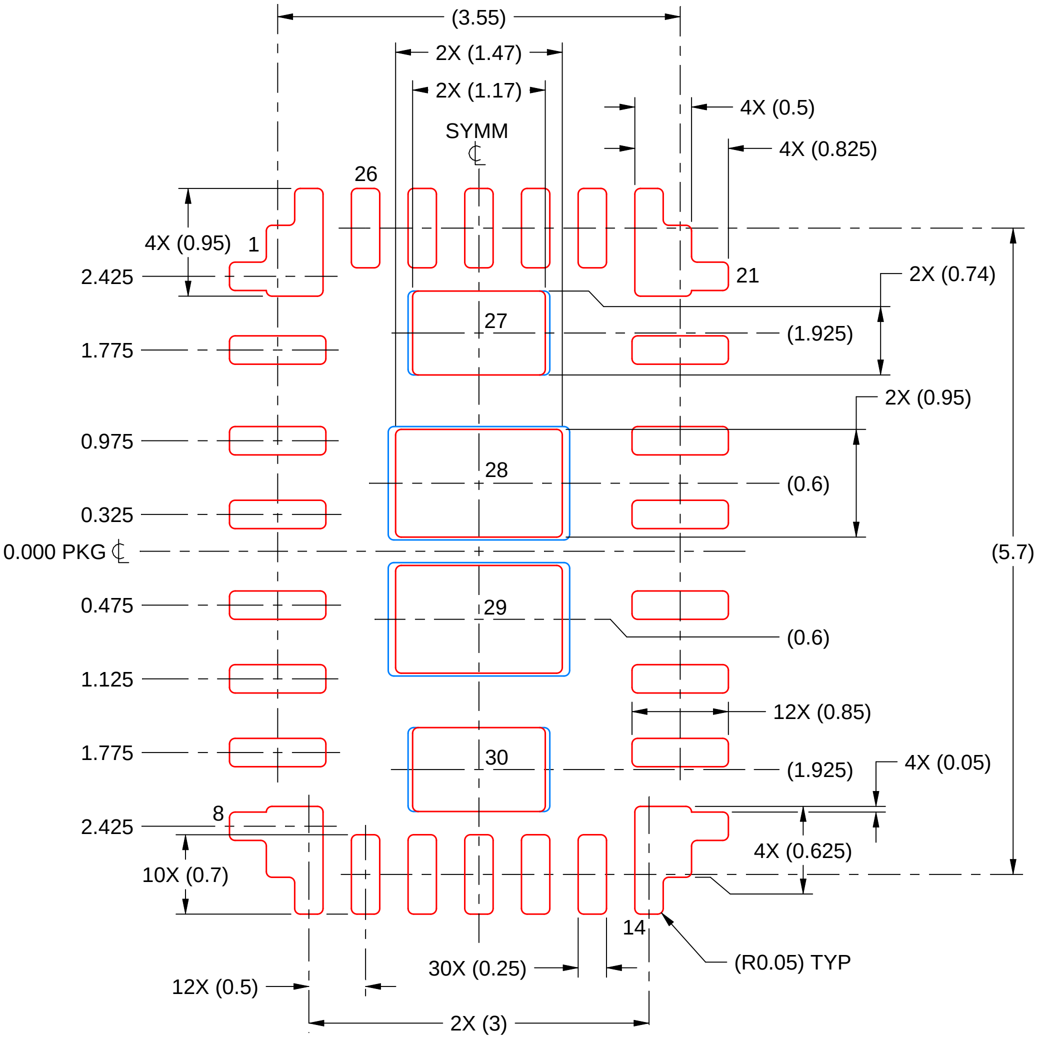
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 27 & 30:
94% PRINTED SOLDER COVERAGE BY AREA

EXPOSED PAD 28 & 29
87% PRINTED SOLDER COVERAGE BY AREA

SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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