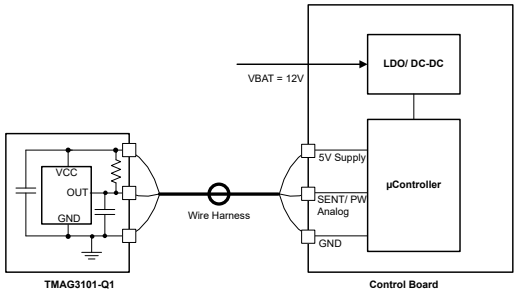
TMAG3101-Q1 Automotive, High-Precision, Linear 3D Hall-Effect Sensor With SENT/ PWM/Analog Interface

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 0: –40°C to 160°C
- 4.5V to 5.5V supply voltage range
- High-precision linear 3D Hall-effect sensor to optimize position sensing speed and accuracy:
  - X-Y angle temperature drift: ±1.0 degree (maximum)
  - Sensitivity mismatch temperature drift: ±2.0% (XY), ±2.5% (XZ, YZ) (maximum)
  - Sensitivity temperature drift for X, Y, Z axes: ±3.0% (maximum)
- Functional Safety-Targeted:
  - Developed for functional safety applications
  - Documentation to aid system design up to ASIL B for single-die TMAG3101-Q1; ASIL D for dual-die TMAG3101D-Q1 (pending review)
- Configurable SENT, Triggered SENT, PWM, and Analog output interfaces
- Programmable full-scale Analog/PWM output ranges
- Built-in temperature sensor with < ±2.5°C error
- 1-wire Single Wire Interface for Test (SWIFT) for end-of-line calibration and programming
- Fixed and variable point linearization for angle or linear magnetic fields
- Integrated angle calculation with offset, gain, and phase correction adjustments

2 Applications

- Steering angle sensing
- Steering torque sensing
- Brake/accelerator pedal position
- Actuator/valve position
- E-shifter position
- Throttle position
- Chassis level sensing



Application Block Diagram

3 Description

The TMAG3101-Q1 is a high-precision linear 3D Hall-effect sensor designed for a wide range of automotive and industrial applications. The high level of integration offers flexibility and accuracy in a variety of position sensing systems. This device features three independent Hall sensors at X, Y, and Z axes. The integrated EEPROM memory enables storage of configuration and linearization data inside the sensor.

A precision signal-chain along with an integrated 20-bit ADC enables high accuracy and low drift magnetic field measurements across a wide ambient temperature range of –40°C to +160°C. The device offers hysteresis, offset, gain, and phase correction options for angle and linear measurement applications. The device also offers up to 32-point linearization scheme to correct system level error sources such as mechanical offset, tilt, and rotation. On-chip temperature sensor data is accessible for system temperature drift compensation.

Integrated angle calculation engine (CORDIC) provides full 360° angular position information for both on-axis and off-axis angle measurement topologies. Several angle calculation schemes are available using user-selected magnetic axes, including 2D or 3D Alpha and Beta angle calculations for joystick or hinge applications.

The TMAG3101-Q1 is calibrated and programmed using the 1-wire SWIFT interface. The device supports user selectable SENT, Triggered SENT, PWM, and Analog output interfaces. TI's unique Triggered SENT interface allows up to four sensors in the same SENT line enabling user selectable addressing scheme.

The TMAG3101-Q1 offers robust diagnostics features to detect and report both system and device-level failures. The SENT communication features a user-enabled cyclic redundancy check to enhance the data integrity. The dual-die variant provides full redundancy, with two identical die in a single package.

The device supports orderable magnetic field ranges of ±50mT, ±100mT, and ±150mT.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMAG3101-Q1	TSSOP (8)	4.40mm × 3.00mm
TMAG3101D-Q1	HTSSOP (16)	4.40mm x 5.00mm

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4 Errata (Pre-Production Material)

Performance deviations of the electrical and magnetic characteristics and behaviors for the pre-production material of TMAG3101-Q1 are at or beyond the deviations documented in Table 4-1 as production material and trim procedures are being finalized. Additional errata not listed here can exist in pre-production material.

Table 4-1. Electrical and Magnetics Characteristics Deviations

PARAMETER	MIN	TYP	MAX	UNIT
$SENS_{ERR}$, X		±0.75	±3	%
$SENS_{ERR}$, Y		±1	±3.5	%
$SENS_{ERR}$, Z		±0.75	±3	%
$SENS_{ERR_DRIFT}$, X		±0.3	±2.5	%
$SENS_{ERR_DRIFT}$, Y		±2	±4.5	%
$SENS_{ERR_DRIFT}$, Z		±2.3	±4.5	%
$SENS_{MIS}$, XY		±0.3	±3	%
$SENS_{MIS}$, XZ		±0.05	±3	%
$SENS_{MIS}$, YZ		±0.4	±3	%
$SENS_{MIS_DRIFT}$, XY		±2	±4	%
$SENS_{MIS_DRIFT}$, XZ		±2.75	±5	%
$SENS_{MIS_DRIFT}$, YZ		±4.2	±5.5	%
B_{OFFSET}, X		±40	±250	µT
B_{OFFSET}, Y		±20	±150	µT
B_{OFFSET}, Z		±36	±150	µT
B_{OFFSET_DRIFT}, X		±1.2	±3	µT/°C
B_{OFFSET_DRIFT}, Y		±1.5	±3	µT/°C
B_{OFFSET_DRIFT}, Z		±1.2	±3	µT/°C
ANG_{ERR}, XY		±0.5	±1.5	°
ANG_{ERR}, XZ		±1.2	±2	°
ANG_{ERR}, YZ		±0.25	±2	°
ANG_{ERR_DRIFT}, XY		±0.7	±2	°
ANG_{ERR_DRIFT}, XZ		±1.0	±3	°
ANG_{ERR_DRIFT}, YZ		±1.2	±3	°
B_{N_XY}		60		LSB (RMS, 1 sigma)
B_{N_Z}		60		LSB (RMS, 1 sigma)
OUT_{OFF}, DAC offset error			±40	mV

Temperature Sensor Characteristics

Temperature sensor error is outside the specified limits in pre-production devices.

PWM Output Frequency Tolerance (f_{PWM})

PWM output frequency tolerance is outside the specified limits in pre-production devices.

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PWM Output With 2D Angle Data

When operating in PWM mode and outputting 2D angle data, the device drives PWM duty cycles outside of 5% to 95% or 10% to 90% according to PWM_DC_SEL

SWIFT_CPU_MAILBOX Signal Path Corrections

When using SWIFT_CPU_MAILBOX to evaluate different device configurations any signal path corrections (ex. x_POL, x_OFFSET, x_GAIN) are applied twice. Recommend using OPERATING_MODE bitfield to see correctly applied signal path corrections. When using OPERATING_MODE for evaluation, re-enter SWIFT programming mode using the procedures shown in Section 7.5.1.4.

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5 Pin Configuration and Functions

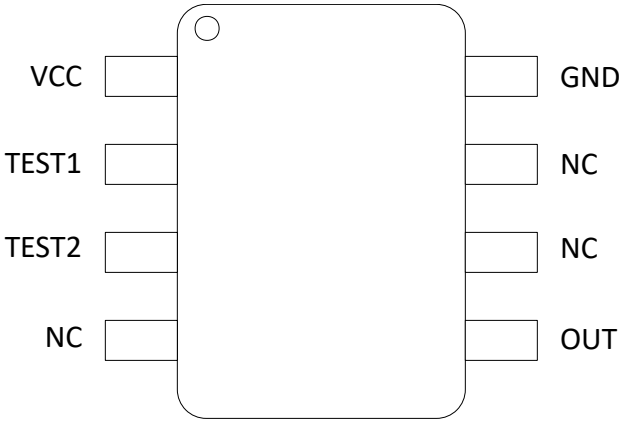


Figure 5-1. PW Package 8-Pin TSSOP Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCC	P	Main power supply, 4.5V to 5.5V. Connect at least a 0.1µF capacitor
2	TEST1	I	TI Factory test pin. Connect to ground
3	TEST2	I	TI Factory test pin. Connect to ground
4	NC	NC	Floating pin. Connect to ground
5	OUT	I/O	Device interface pin
6	NC	NC	Floating pin. Connect to ground
7	NC	NC	Floating pin. Connect to ground
8	GND	G	Ground reference

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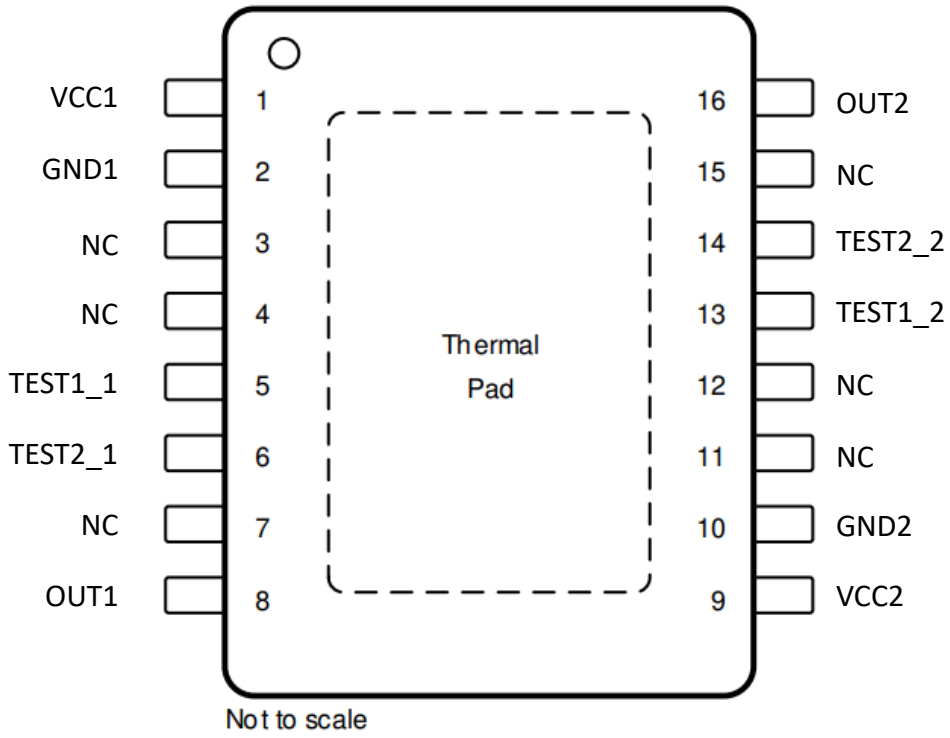


Figure 5-2. PWP Package 16-Pin HTSSOP Top View

Table 5-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VCC1	P	Main power supply for die 1, 4.5V to 5.5V. Connect at least a 0.1µF capacitor
2	GND1	G	Ground reference for die 1
3	NC	NC	Floating pin. Connect to ground
4	NC	NC	Floating pin. Connect to ground
5	TEST1_1	I	TI factory test pin. Connect to ground.
6	TEST2_1	I	TI factory test pin. Connect to ground.
7	NC	NC	Floating pin. Connect to ground
8	OUT1	I/O	Device interface pin for die 1
9	VCC2	P	Main power supply for die 2, 4.5V to 5.5V. Connect at least a 0.1µF capacitor
10	GND2	G	Ground reference for die 2
11	NC	NC	Floating pin. Connect to ground
12	NC	NC	Floating pin. Connect to ground
13	TEST1_2	I	TI factory test pin. Connect to ground.
14	TEST2_2	I	TI factory test pin. Connect to ground.
15	NC	NC	Floating pin. Connect to ground
16	OUT1	I/O	Device interface pin for die 2

(1) I = input, O = output, I/O = input and output, G = ground, P = power, NC = no connect

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{CC}	Main supply voltage	–20	20	V
I_{CC}	Supply current, VCC		±30	mA
I_{OUT}	Output short current, OUT shorted to VCC or GND		±30	mA
V_{OUT}	Output voltage, OUT	–20	20	V
V_{IN}	Input voltage, TEST	–0.3	7	V
B_{MAX}	Magnetic flux density		Unlimited	T
T_J	Junction temperature	–40	175	°C
T_{stg}	Storage temperature	–65	175	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) See *Errata* for pre-production material

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±4000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC(1)		TMAG3101-Q1 PW (TSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5		5.5	V
V_{OUT}	Output voltage, OUT	0		5.5	V
C_{VCC}	VCC bypass capacitance	100		1000	nF
B_{MAX}	Magnetic flux density, TMAG3101-Q1 x1 variant			±50	mT
B_{MAX}	Magnetic flux density, TMAG3101-Q1 x2 variant			±100	mT
B_{MAX}	Magnetic flux density, TMAG3101-Q1 x3 variant			±150	mT

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		MIN	NOM	MAX	UNIT
T_A	Operating free air temperature	–40		160	C

6.5 Electrical Characteristics

Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)[3]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I/O Characteristics						
V_{OH}	Output HIGH voltage, OUT in push-pull mode	I_{OUT} = –1mA	V_{CC} - 0.5			V
V_{OL}	Output LOW voltage, OUT	I_{OUT} = 1mA	0		0.5	V
I_{OZ}	Output leakage current, OUT	Output disabled V_{OZ} < 5.5V			±5	µA
V_{IL}	Input LOW voltage, OUT				35	%VCC
V_{IH}	Input HIGH voltage, OUT		65			%VCC
V_{HYST}	Input hysteresis voltage, OUT		0.5			V
Device Specifications						
$V_{CCPOR(RISE)}$	Power on Reset voltage, rising		2.5	2.7	2.9	V
$V_{CCPOR(HYST)}$	Power on Reset voltage, hysteresis	$V_{CCPOR(RISE)}$ - $V_{CCPOR(FALL)}$	0.02	0.3	0.4	V
$V_{CCOV(RISE)}$	Over voltage threshold at V_{CC}, rising	OV_SEL = 0h	5.9	6.1	6.35	V
		OV_SEL = 1h	6.35	6.5	6.75	V
$V_{CCOV(HYST)}$	Over voltage threshold at V_{CC}, hysteresis	$V_{CCOV(RISE)}$ - $V_{CCOV(FALL)}$	0.09	0.13	0.2	V
$V_{CCUV(RISE)}$	Under voltage threshold at V_{CC}, rising	UV_SEL = 0h	3.6	3.9	4.1	V
		UV_SEL = 1h	2.7	2.9	3.1	V
$V_{CCUV(HYST)}$	Under voltage threshold at V_{CC}, hysteresis	$V_{CCUV(RISE)}$ - $V_{CCUV(FALL)}$	0.02	0.1	0.2	V
LDO_{UV}	Under voltage threshold at internal LDO (AVDD), falling			1.6	1.7	V
$t_{OV_UV_FL}$	Minimum time threshold to stay in over voltage or under voltage condition to set the V_{CC_OV}, V_{CC_UV} bits			35	65	µs
I_{ACTIVE}	Active mode current, SENT/ PWM mode	During continuous conversion	5	7	10	mA
	Active mode current, Analog mode		6	8	11	mA
$I_{STANDBY}$	Stand-by mode current	Device in Standby mode, no active ADC conversion	1	2	3	mA
t_{ACTIVE}	X, Y, or Z axis active conversion time, offset, gain, phase, hysteresis, and linearization corrections disabled[1]	Conversion time for single magnetic channel with FILTER_SEL = 0h		97	103.5	µs
		Conversion time for single magnetic channel with FILTER_SEL = 7h		224	237	µs
t_{ON}	Power on time	Time taken to go to active mode after V_{CC} crossing V_{CC_UV}			450	µs
t_{STAND_ACTIVE}	Time taken to switch from stand-by mode to active mode upon trigger				10	µs

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Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{fall}	Fall time t_{TICK} = 12µs R_{PU} = 12kΩ C_{LOAD} = 0.1nF to 1nF SENT/ PWM/ SWIFT mode	FALL_SLEW = 0h		0.3		µs
		FALL_SLEW = 1h		0.45		µs
		FALL_SLEW = 2h		0.6		µs
		FALL_SLEW = 3h		0.75		µs
	Fall time R_{PU} = 12kΩ C_{LOAD} = 0.1nF to 5nF SENT/ PWM/ SWIFT mode	FALL_SLEW = 4h		1.3		µs
		FALL_SLEW = 5h		2.1		µs
		FALL_SLEW = 6h		3.5		µs
		FALL_SLEW = 7h		5.5		µs
t_{rise}(2)	Rise time t_{TICK} = 12µs R_{PU} = 12kΩ C_{LOAD} = 0.1nF to 1nF Push-pull mode, SENT/ PWM mode	RISE_SLEW = 0h		0.3		µs
		RISE_SLEW = 1h		0.45		µs
		RISE_SLEW = 2h		0.6		µs
		RISE_SLEW = 3h		0.75		µs
	Rise time t_{TICK} = 12µs R_{PU} = 12kΩ C_{LOAD} = 0.1nF to 5nF Push-pull mode, SENT/ PWM mode	RISE_SLEW = 4h		1.3		µs
		RISE_SLEW = 5h		2.1		µs
		RISE_SLEW = 6h		7.0		µs
		RISE_SLEW = 7h		11.0		µs
f_{CLK_HF}	Frequency of high frequency oscillator		30.5	32	33.5	MHz
f_{CLK_LF}	Frequency of low frequency oscillator			100		kHz

(1) t_{ACTIVE} is the total conversion time from start to finish. If the conversion is triggered, t_{ACTIVE} is the time counted from trigger start to data available at result registers. If the conversions are continuous, t_{ACTIVE} is the time from starting a new conversion to data available at the result registers.
(2) Rise time for SENT / PWM output in open-drain mode is not specified as the time depends on the external resistor and capacitor.
(3) See *Errata* for pre-production material

6.6 Magnetic Characteristics

Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Magnetic Channel Specifications						
B_{RANGE}	Linear magnetic range: X, Y, or Z axis	TMAG3101x1		±51.2		mT
		TMAG3101x2		±102.5		
		TMAG3101x3		±153.7		
SENS	Sensitivity, X, Y, or Z axis	±50mT range		639.51		LSB/mT
		±100mT range		319.51		
		±150mT range		213.17		
$SENS_{ERR}$	Sensitivity error T_A =25°C	X, Y, Z axis			±2.5	%
$SENS_{LE}$	Sensitivity Linearity Error T_A =25°C	X, Y, axis		±0.10	±0.3	
		Z axis		±0.10	±0.3	
$SENS_{MIS}$	Sensitivity mismatch T_A = 25°C	X-Y axes			±2.5	
		Y-Z or X-Z axes			±3.5	
B_{OFFSET}	Offset T_A = 25°C	X, Y axis		±100		µT
		Z axis		±100		

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Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
B_{N_XY}	Magnetic sensor noise spectral density X or Y axis T_A = -40°C to 150°C FILTER_SEL = 0 (bandwidth = 45kHz)	±50 mT range		410	647	nT/rtHz
		±100 mT range		432	671	
		±150 mT range		462	695	
B_{N_Z}	Magnetic sensor noise spectral density Z-axis T_A = -40°C to 150°C FILTER_SEL = 0 (bandwidth = 45kHz)	±50 mT range		274	432	
		±100 mT range		296	438	
		±150 mT range		313	460	
Magnetic Channel Drift Specifications						
$SENS_{ERR_DRIFT}$	Sensitivity drift from T_A = 25°C X, Y, Z axis	T_A = -40°C to 150°C			±3	%
		T_A = -40°C to 160°C		±1.5	TBD	
$SENS_{MIS_DRIFT}$	Sensitivity mismatch drift from T_A = 25°C	X-Y axes T_A = -40°C to 150°C			±1.5	
		Y-Z, or X-Z axes T_A = -40°C to 150°C			±2.0	
		X-Y axes T_A = -40°C to 160°C			TBD	
B_{OFFSET_DRIFT}	Offset drift from T_A = 25°C	T_A = -40°C to 150°C			±1.0	µT/°C
		T_A = -40°C to 160°C			TBD	
$B_{SENS_LT_DRIFT}$	Sensitivity Lifetime drift X, Y, Z axes After Q100 qual	T_A = 25°C		±0.5	±2.0	%
$B_{OFFSET_LT_DRIFT}$	Offset Lifetime drift After Q100 qual	T_A = 25°C			±100	µT
STC	Temperature compensation X, Y, Z axes T_A = -40°C to 160°C	TEMPCO_SEL = 2h		0		%/°C
		TEMPCO_SEL = 8h		0.12		
		TEMPCO_SEL = 5h		0.04		
		TEMPCO_SEL = Bh		0.2		
Angle Specifications						
ANG_{ERR}	Angle error in full 360 degree rotation T_A = 25°C Input magnetic field magnitude = 60% * B_{RANGE}	X-Z, Y-Z			±1.0	deg
		X-Y			±0.5	
N_{RMS}	RMS (1 Sigma) angle noise XY	FILTER_SEL = 0h T_A = -40°C to 150°C		0.2	0.4	deg_{rms}
		FILTER_SEL = 6h T_A = -40°C to 150°C		0.02	0.2	
		FILTER_SEL = Ah T_A = -40°C to 150°C		0.02	0.1	
	RMS (1 Sigma) angle noise XZ, YZ	FILTER_SEL = 0h T_A = -40°C to 150°C		0.2	0.4	
		FILTER_SEL = 6h T_A = -40°C to 150°C		0.02	0.2	
		FILTER_SEL = Ah T_A = -40°C to 150°C		0.02	0.1	
Angle Drift Specifications						

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Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANG_{ERR_DRIFT}	Angle temp drift from T_A = 25°C in full 360 degree rotation X-Z. Y-Z Input magnetic field magnitude = 60% * B_{RANGE}	T_A = -40°C to 150°C			±1.0	deg
		T_A = -40°C to 160°C		±0.5		
	Angle temp drift from T_A = 25°C in full 360 degree rotation X-Y Input magnetic field magnitude = 60% * B_{RANGE}	T_A = -40°C to 150°C			±0.8	
		T_A = -40°C to 160°C		±0.25		
ANG_{ELT_DRIFT}	Angle error lifetime drift After Q100 qual	T_A = 25°C			±0.1	deg

(1) See *Errata* for pre-production material

6.7 Temperature Sensor Characteristics

Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{RANGE}	Temperature sensing range		–40		175	℃
T_{RES}	Temperature resolution (LSB) in 16-bit format			7.8125		m°C
T_{ERR}	Temperature accuracy	T_A = –40℃ to 160℃		±0.5	±2.5	℃
T_{NRMS}	RMS (1 Sigma) temperature noise			0.05	0.2	℃

(1) See *Errata* for pre-production material

6.8 PWM Interface Characteristics

for V_{CC} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D_L	Linear duty cycle range	PWM_DC_SEL = 0h	5		95	%D
		PWM_DC_SEL = 1h	10		90	%D
S_A	Full scale range sensitivity A_PWM_OUT_SCALE - 0h ±50 mT Range	PWM_DC_SEL = 0h		0.878		%D/mT
		PWM_DC_SEL = 1h		0.78		%D/mT
	Full scale range sensitivity A_PWM_OUT_SCALE - 0h ±100 mT Range	PWM_DC_SEL = 0h		0.439		%D/mT
		PWM_DC_SEL = 1h		0.39		%D/mT
	Full scale range sensitivity A_PWM_OUT_SCALE - 0h ±150 mT Range	PWM_DC_SEL = 0h		0.293		%D/mT
		PWM_DC_SEL = 1h		0.260		%D/mT
S_A	Full scale angle sensitivity A_PWM_OUT_SCALE = 0h	PWM_DC_SEL = 0h		0.25		%D/deg Angle
		PWM_DC_SEL = 1h		0.222		%D/deg Angle

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for V_{CC} = 4.5 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{QΔL}$	Quiescent duty cycle lifetime drift	High-temperature operating stress for 1000 hours		< 0.5		%
f_{PWM}	PWM output frequency	PWM_FREQ_SEL = 0h	95	100	105	Hz
		PWM_FREQ_SEL = 1h	143	150	158	
		PWM_FREQ_SEL = 2h	195	205	215	
		PWM_FREQ_SEL = 3h	232	244	256	
		PWM_FREQ_SEL = 4h	464	488	512	
		PWM_FREQ_SEL = 5h	742	781	820	
		PWM_FREQ_SEL = 6h	1237	1302	1367	
		PWM_FREQ_SEL = 7h	1855	1953	2051	
V_{PWM_L}	PWM low logic level	IO = 1 mA			0.5	V
V_{PWM_H}	PWM high logic level	IO = -1 mA Push-pull mode	VCC - 0.5			V
OUT_{RES}	PWM output resolution		13			Bit

(1) See *Errata* for pre-production material

6.9 SENT Interface Characteristics

Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SENT/ Trigger SENT Specification						
t_{TICK}	SENT tick time	TICK_SEL = 0h	0.238	0.25	0.263	µs
		TICK_SEL = 1h	0.475	0.5	0.525	
		TICK_SEL = 2h	0.95	1.0	1.05	
		TICK_SEL = 3h	1.9	2.0	2.1	
		TICK_SEL = 4h	2.85	3.0	3.15	
		TICK_SEL = 5h	4.75	5	5.25	
		TICK_SEL = 6h	5.7	6	6.3	
		TICK_SEL = 7h	11.4	12	12.6	
TOL_{TICK}	TICK time tolerance		–5		5	%
RES_{SENT}	SENT output resolution		12		16	bit
C_{LOAD}(1)	Load capacitance				5	nF
R_{PU}(1)	Pull-up resistor		3			kΩ

(1) The output resistive and capacitive load must be carefully selected to match the application tick time to allow appropriate time constant for the transmission of the SENT signal.
(2) See *Errata* for pre-production material

6.10 Analog Output Interface Characteristics

Valid over |B| > 30mT and over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT_{RES}	Analog output Resolution			12		bits
ΔVout	DAC Step Size (LSB)			0.0195		%VCC
OUT_{RANGE}	Linear operating output voltage		10		90	%VCC

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Valid over |B| > 30mT and over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
S_B	Full scale range sensitivity A_PWM_OUT_SCALE = 0h	±50 mT range, V_{CC} = 5V		39.03		mV/mT
		±100 mT range, V_{CC} = 5V		19.5		
		±150 mT range, V_{CC} = 5V		13.01		
S_A	Full scale angle sensitivity	A_PWM_OUT_SCALE = 0h		11.11		mV/deg
DNL	DAC Differential non-linearity	V_{CC} = 5V	-1		1	LSB
INL	DAC Integral non-linearity	V_{CC} = 5V	-4		4	
OUT_{GAIN}	DAC Gain error	T_A = 25°C	-0.2		0.2	%VCC
OUT_{GAIN_DRIFT}	DAC Gain error drift from T_A = 25°C	T_A =-40°C to 150°C	-0.1		0.1	
		T_A =-40°C to 160°C			TBD	
OUT_{OFF}	DAC Offset error		-3		3	mV
OUT_{OFF_DRIFT}	DAC Offset drift			0.05		mV/°C
R_{LOAD}	Output load resistance		3.0			kΩ
C_{LOAD}	Output load capacitance T_A = 25°C	LOAD_SEL = 0h	10		20	nF
		LOAD_SEL = 1h	20		50	
		LOAD_SEL = 2h	50		100	
		LOAD_SEL = 3h	100		330	
V_{DIAG_H}	Diagnostic high voltage		95			%VCC
V_{DIAG_L}	Diagnostic low voltage				5	
$t_{response}$	Analog output sensor response time	Time taken for output to change to 99% of desired output value from the time sensor input reaches 99% of the final value		1.5		ms

(1) See *Errata* for pre-production material

6.11 SWIFT Interface Characteristics

Over free-air temperature range and V_{CC} = 4.5 V to 5.5 V (unless otherwise noted); Typical specification are at T_A = 25°C and V_{CC} = 5.0 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWIFT Specification						
t_T	SWIFT unit time, selectable by microcontroller		0.75		208.4	µs
TOL_T	SWIFT unit time tolerance		–10%		10%	
C_{LOAD}	Load capacitance. This capacitance impacts the rising edge transition timing.				5	nF
R_{PU}	Pull-up resistance. This resistance along with the load capacitance impacts the rising edge transition timing.		3			kΩ
V_{OL}	Output low voltage with 1mA load current				0.5	V
V_{IH}	SWIFT input HIGH voltage		65			%VCC
V_{IL}	SWIFT input LOW voltage				35	%VCC

(1) See *Errata* for pre-production material

6.12 Power up Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{start_power_up}$	Time to go to stand-by mode after V_{CC} supply voltage crossing V_{CC_MIN}	Triggered SENT mode		424		µs

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over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{start_power_up}$	Time to go to active measure mode after V_{CC} supply voltage crossing V_{CC_MIN}	Continuous SENT mode		415		µs
$t_{start_power_up}$	Time to go to active measure mode after V_{CC} supply voltage crossing V_{CC_MIN}	Analog mode, LOCKOUT = 4h		385		µs
$t_{start_power_up}$	Time to go to active measure mode after V_{CC} supply voltage crossing V_{CC_MIN}	PWM mode		385		µs
$t_{start_power_up}$	Time to go to SWIFT mode after V_{CC} supply voltage crossing V_{CC_MIN}	SWIFT mode		385		µs
$t_{fault_recovery}$	Time for OUT pin to transition from high-z mode to active mode after fault condition removed.		125		400	µs

6.13 Typical Characteristics

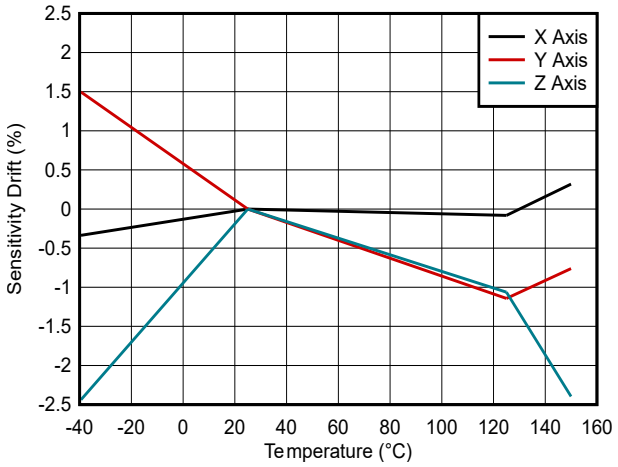


Figure 6-1. Sensitivity Drift vs. Temperature, ±150mT Range (Pre-Production Material)

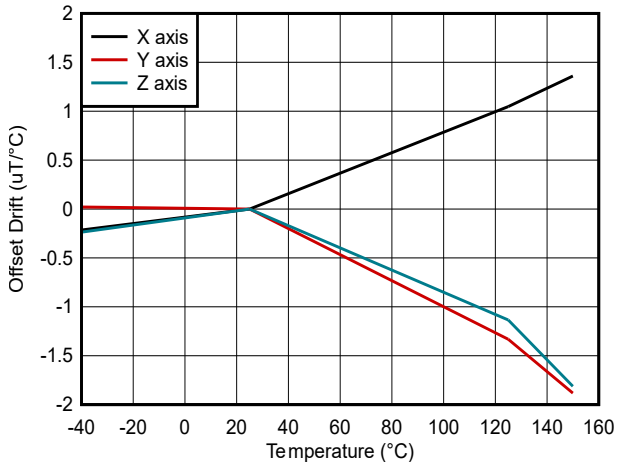


Figure 6-2. Offset Drift vs. Temperature, ±150mT Range (Pre-Production Material)

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7 Detailed Description

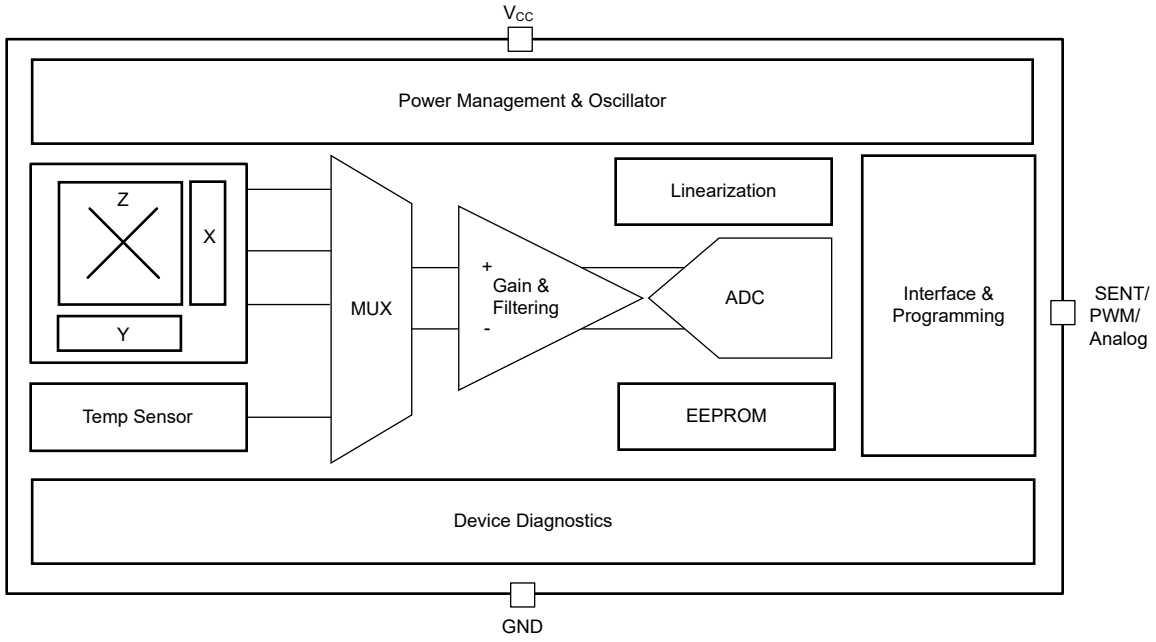
7.1 Overview

The TMAG3101-Q1 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The sensor includes horizontal and vertical Hall-plates capable of sensing magnetic fields in the X, Y, and Z directions. The device offers four user selectable interfaces (SENT, Triggered SENT, PWM, or Analog) which is configured through the SWIFT interface. Linear sensor data (raw X, Y, Z, and temperature channel), along with a number of angle data derived from the linear measurement, are accessible through the device configurations.

The IC consists of the following functional and building blocks:

- The Power Management and Oscillator block contains a low-power oscillator, biasing circuitry, undervoltage and overvoltage detection circuitry, and a fast oscillator
- The sensing and temperature measurement block contains the Hall biasing, Hall sensors with multiplexers, noise filters, integrator circuit, temperature sensor, and the ADC. The Hall sensor data and temperature data are multiplexed through the same ADC.
- The digital core includes the linearization and EEPROM blocks, which handle digital signal processing of the sensor data as well as volatile and nonvolatile memory
- The Interface block contains the SENT/Triggered SENT/PWM/Analog control circuitry, ESD protection circuits, and short-to-VBAT circuits.
- The diagnostic blocks are embedded in the circuitry to enable mandatory and user-enabled diagnostic checks

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Sensor Location

Figure 7-1 shows the location of X, Y, Z Hall elements inside the TMAG3101-Q1.

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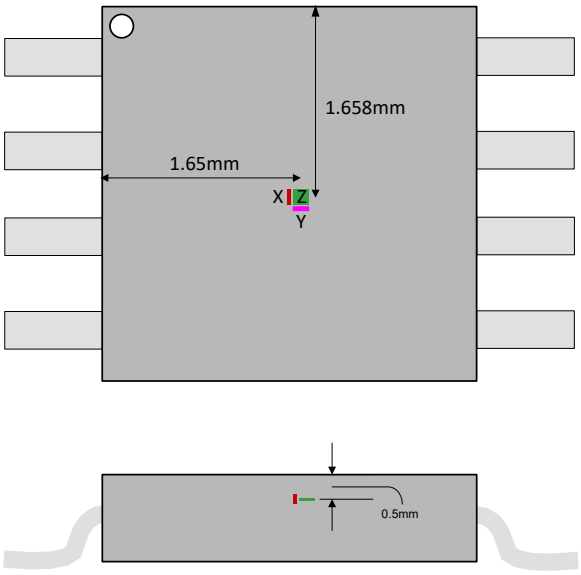


Figure 7-1. Location of X, Y, Z Hall Elements

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7.3.2 Magnetic Range Selection

Table 7-1 shows the mdagnetic range selection for the TMAG3101-Q1 device based on device orderable.

Table 7-1. Magnetic Range Selection

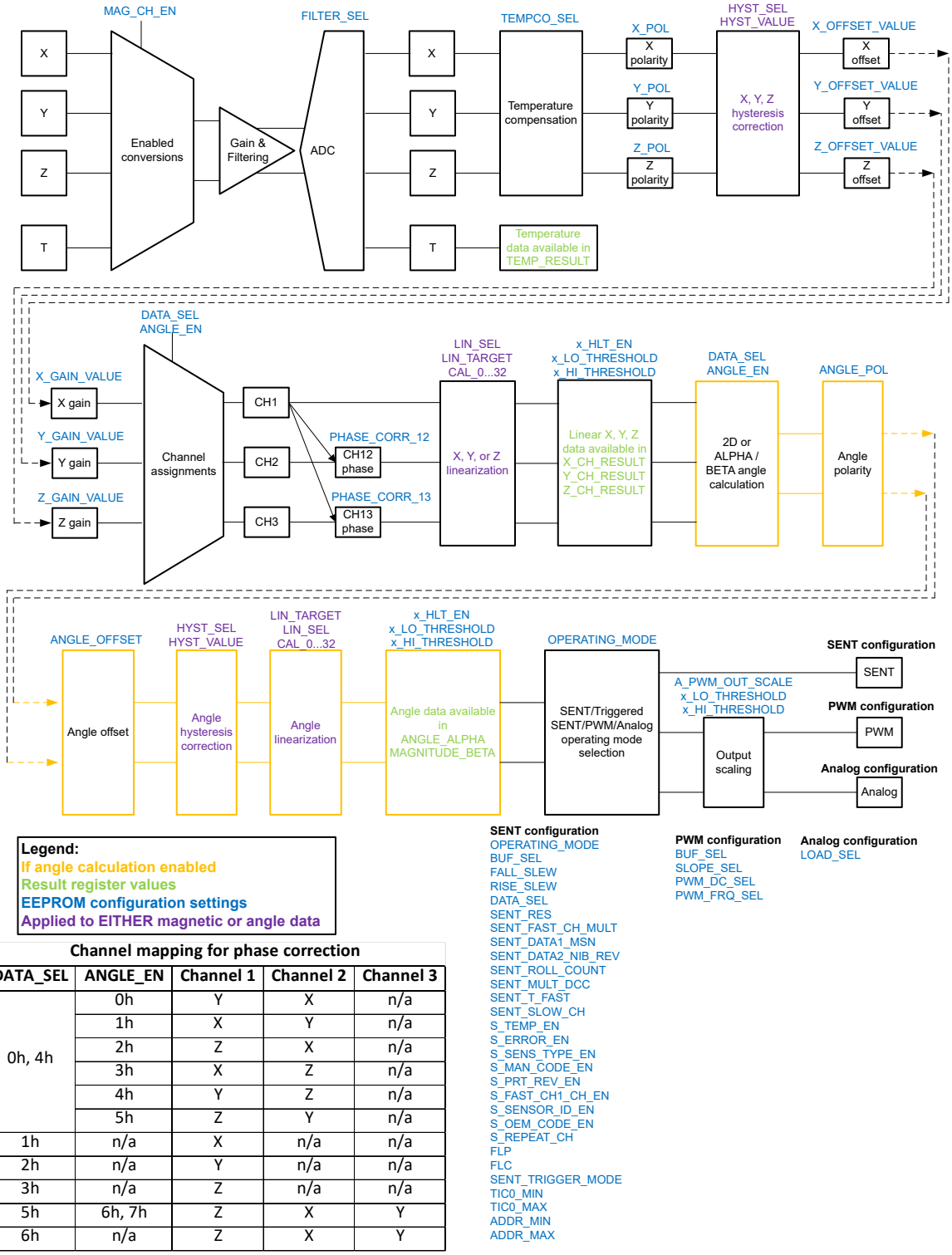
	TMAG3101-Q1 Orderable	Magnetic Sensing Range
X, Y, and Z Axis Field	TMAG3101x1	±50mT
	TMAG3101x2	±100mT
	TMAG3101x3	±150mT

7.3.3 Signal Path

The details of the overall digital signal processing path for the TMAG3101-Q1 are shown in TMAG3101-Q1 Signal Path. Not all functions are available for all measurement modes. Depending on the measurement setup, the signal path is scaled to the needs for the measurement setup.

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Channel mapping for phase correction

DATA_SEL	ANGLE_EN	Channel 1	Channel 2	Channel 3
0h, 4h	0h	Y	X	n/a
	1h	X	Y	n/a
	2h	Z	X	n/a
	3h	X	Z	n/a
	4h	Y	Z	n/a
	5h	Z	Y	n/a
1h	n/a	X	n/a	n/a
2h	n/a	Y	n/a	n/a
3h	n/a	Z	n/a	n/a
5h	6h, 7h	Z	X	Y
6h	n/a	Z	X	Y

Figure 7-2. TMAG3101-Q1 Signal Path

7.3.4 Conversion Time

The TMAG3101-Q1 offers multiple update rates and sensor selection options for system design flexibility. Use the MAG_CH_EN, FILTER_SEL, DIAG_EN, and OPERATING_MODE register bits to select the right conversion setting for a given application. Table 7-2 shows the different conversion times for the TMAG3101-Q1 during

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continuous conversion with DIAG_EN = 0b. During each conversion the temperature sensor measures the die temperature and stores the measurement in the TEMP_RESULT register.

Table 7-2. Conversion Time Settings

FILTER SETTING	CONVERSION TIME			COMMENT
	SINGLE AXIS	TWO AXES	THREE AXES	
FILTER_SEL = 0000b	97µs	180µs	263µs	Fastest update rate
FILTER_SEL = 0001b	98µs	182µs	266µs	
FILTER_SEL = 0010b	100µs	186µs	272µs	
FILTER_SEL = 0011b	104µs	194µs	284µs	
FILTER_SEL = 0100b	112µs	210µs	308µs	
FILTER_SEL = 0101b	128µs	242µs	356µs	
FILTER_SEL = 0110b	160µs	306µs	452µs	
FILTER_SEL = 0111b	224µs	434µs	644µs	
FILTER_SEL = 1000b	352µs	690µs	1.028ms	
FILTER_SEL = 1001b	608µs	1.202ms	1.796ms	
FILTER_SEL = 1010b	1.120ms	2.226ms	3.332ms	
FILTER_SEL = 1011b	2.144ms	4.274ms	6.404ms	
FILTER_SEL = 1100b	4.192ms	8.370ms	12.548ms	
FILTER_SEL = 1101b	8.288ms	16.562ms	24.836ms	
FILTER_SEL = 1110b	16.480ms	32.946ms	49.412ms	
FILTER_SEL = 1111b	32.864ms	65.714ms	98.564ms	Best SNR case

Additional post conversion time can be added when features like diagnostics, linearization, or other signal path correction features are enabled.

7.3.5 Magnetic Flux Direction

The TMAG3101-Q1 is sensitive to the magnetic field component in X, Y, and Z directions. The X and Y fields are in plane with the package. The Z field is perpendicular to the top of the package. The device is sensitive to both magnetic north and south poles in each axis. As shown in Figure 7-3, the device generates positive ADC codes in response to a magnetic south pole in the proximity. Similarly, the device generates negative ADC codes if the magnetic north poles approach from the same directions.

The polarity of each axis can be inverted using the X_POL, Y_POL, and Z_POL bits in EEPROM.

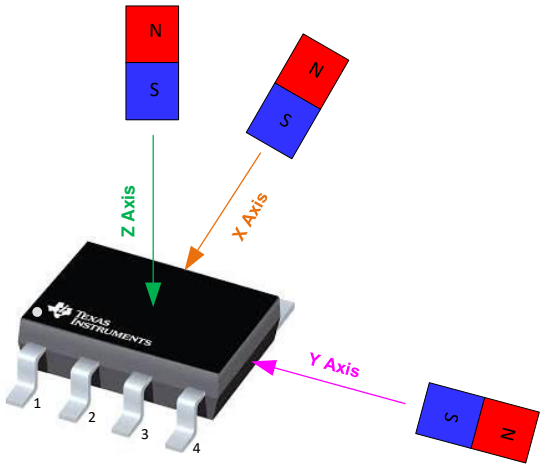


Figure 7-3. Direction of Applied Magnetic South Pole to Generate Positive ADC Codes

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7.3.6 Sensor Conversion Selection

The TMAG3101-Q1 DATA_SEL and ANGLE_EN register bits determine the type of data communicated through the OUT pin. Additional information such as magnetic threshold cross information can be communicated through the status nibble of the SENT frame. Proper sensor channels must be enabled through the MAG_CH_EN register bits to be compatible with the desired data output. Select MAG_CH_EN settings of 8h to Fh if additional averaging for particular channels are required. As an example, the XZX setting enables the average of the two X conversions for each Z conversion. The temperature sensor data is collected with each new conversion irrespective of the conversion settings. The temperature data can be accessed only in the SENT mode. Select SENT_T_FAST bit for temperature data through the SENT fast channel, and S_TEMP_EN bit for temperature data through the SENT slow serial channel. A few examples of the proper EEPROM setting are shown in Table 7-3.

Table 7-3. Sensor Channel Selection Examples

DATA_SEL	ANGLE_EN	x_HLT_EN	MAG_CH_EN
0h or 4h	0h or 1h	T_HLT_EN =1h	Select X and Y channels
	0h or 1h	T_HLT_EN =1h, Z_HLT_EN =1h	Select X, Y, and Z channels
	0h or 1h	MAG_HLT_EN =1h	Select X and Y channels
5h	6h or 7h	Don't care	Select X, Y, and Z channels
1h	Don't care	X_HLT_EN =1h	Select X channel
	Don't care	T_HLT_EN =1h, Z_HLT_EN =1h	Select X and Z channels
2h	Don't care	Z_HLT_EN =1h	Select Y and Z channels
3h	Don't care	T_HLT_EN =1h, Z_HLT_EN =1h	Select Z channel
6h	Don't care	Don't care	Select X, Y, and Z channels

7.3.7 Temperature Coefficient

The TMAG3101-Q1 offers multiple magnetic temperature coefficients to compensate for magnetic temperature characteristics as shown in Table 7-4. The temperature coefficient controls the device sensitivity. As an example, with TEMPCO_SEL of 1011b, at 125C the device sensitivity is 0.2 × (125 – 25) = 20% higher than the sensitivity at 25°C. Use the TEMPCO_SEL EEPROM bits to select the desired temperature coefficient setting for a given magnet.

Table 7-4. Temperature Coefficient

TEMPCO_SEL SETTING	Temperature Coefficient	Comment
TEMPCO_SEL = 0000b	–0.02%/°C	
TEMPCO_SEL = 0001b	–0.01%/°C	
TEMPCO_SEL = 0010b	0.00%/°C	No temperature coefficient
TEMPCO_SEL = 0011b	0.01%/°C	
TEMPCO_SEL = 0100b	0.03%/°C	
TEMPCO_SEL = 0101b	0.04%/°C	SmCo Magnet
TEMPCO_SEL = 0110b	0.05%/°C	
TEMPCO_SEL = 0111b	0.11%/°C	
TEMPCO_SEL = 1000b	0.12%/°C	NdFeB Magnet
TEMPCO_SEL = 1001b	0.13%/°C	
TEMPCO_SEL = 1010b	0.19%/°C	
TEMPCO_SEL = 1011b	0.20%/°C	Ferrite Magnet
TEMPCO_SEL = 1100b	0.21%/°C	

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7.3.8 Hysteresis Function

The TMAG3101-Q1 offers optional hysteresis function to enhance noise immunity. Use the HYST_SEL and HYST_VALUE register bits to select the target channel and the amount of hysteresis. After enabled, the device applies a hysteresis band to the corresponding channel. Hysteresis can be applied to either magnetic field data or angle data, but not both at the same time.

As the magnetic field is moving in a certain direction, the device responds to a change in field in the opposite direction only if the amount of change is larger than the hysteresis band. if the amount of change is less than the hysteresis band, the device maintains the output from the previous conversion. This feature can help eliminate unwanted spikes in the sensor or angle output as demonstrated in Figure 7-4.

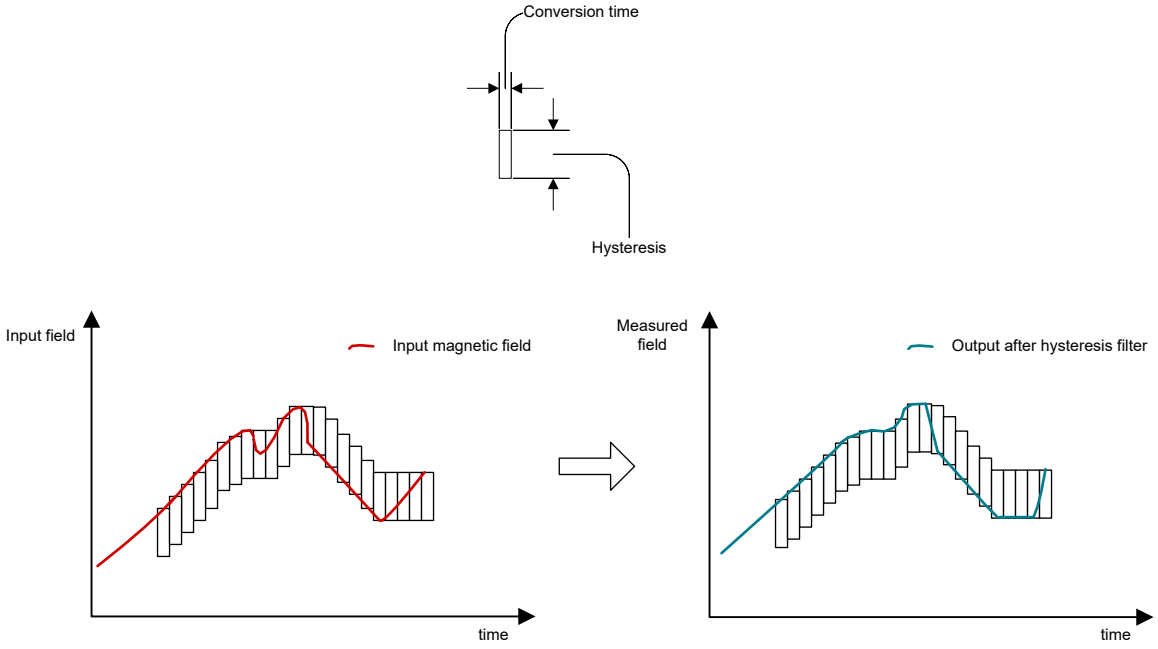


Figure 7-4. TMAG3101-Q1 Hysteresis Function

7.3.9 Magnetic Sensor Offset Correction

As shown in Figure 7-5, the TMAG3101-Q1 supports individual offset correction for all three axes by selecting 16-bit, 2's complement offset values in the X_OFFSET_VALUE, Y_OFFSET_VALUE, and Z_OFFSET_VALUE register bits. The range of possible x_OFFSET_VALUE valid entries can be -32768 to +32767 with a mT resolution of 1/SENS. As an example, the X offset value in mT is calculated as the X_OFFSET_VALUE / SENS. Default offset value is 0.

Note that polarity change is the first operation performed in the signal processing. Set the polarity first to verify the offset programmed has the proper sign. Offset correction is represented by Equation 1, Equation 2, and Equation 3.

$$\mathrm{X_OFFSET_CORR} = \mathrm{X_VALUE} + \mathrm{X_OFFSET_VALUE} \quad (1)$$

$$\mathrm{Y_OFFSET_CORR} = \mathrm{Y_VALUE} + \mathrm{Y_OFFSET_VALUE} \quad (2)$$

$$\mathrm{Z_OFFSET_CORR} = \mathrm{Z_VALUE} + \mathrm{Z_OFFSET_VALUE} \quad (3)$$

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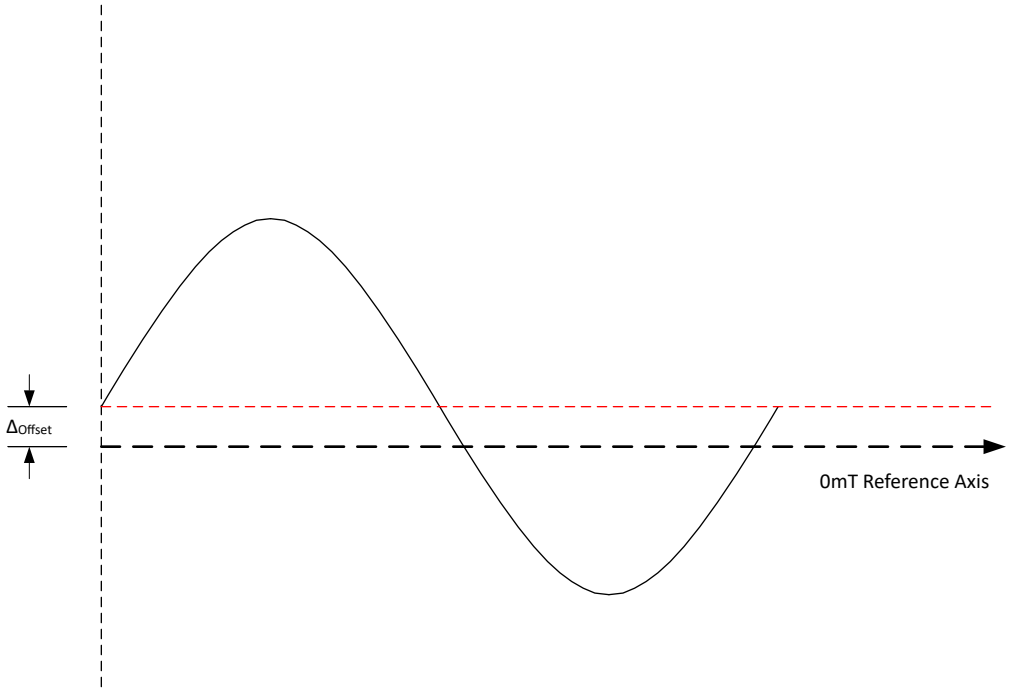


Figure 7-5. Magnetic Sensor Data Offset Correction

7.3.10 Magnetic Sensor Gain Correction

The TMAG3101-Q1 supports gain correction for all the three magnetic axes by selecting 16-bit unsigned gain values in the X_GAIN_VALUE, Y_GAIN_VALUE, and Z_GAIN_VALUE register bits. For polarity correction, use the X_POL, Y_POL, and Z_POL bitfields. The range of possible gain values are within 0 to 15.99976, with a resolution of 0.000244. As an example, with X_GAIN_VALUE set to 0x0800, the X channel measured data is scaled by a factor of 0.5 (2048/65536) times before storing in the X result register. The default gain value of 0x1000 indicates no scaling. Gain correction is implemented after offset correction. The gain correction is particularly helpful during off-axis angle calculation where the two sensor axes data do not have the same peak amplitude.

In the case that phase correction is applied to a specific channel, the desired gain correction value must be adapted by a factor of 1/cos(α), where α represents the phase error corrected. Gain correction is represented by Equation 4, Equation 5, and Equation 6.

$$\mathrm{X_GAIN_CORR} = \mathrm{X_VALUE} \times \mathrm{X_GAIN} \tag{4}$$

$$\mathrm{Y_GAIN_CORR} = \mathrm{Y_VALUE} \times \mathrm{Y_GAIN} \tag{5}$$

$$\mathrm{Z_GAIN_CORR} = \mathrm{Z_VALUE} \times \mathrm{Z_GAIN} \tag{6}$$

7.3.11 Phase Correction

The TMAG3101-Q1 offers optional phase correction for orthogonality errors in 2D-angle calculation, 3D-angle calculation, and SENT fast channel multiplexing modes. Phase correction can be independently applied to Channel 2 and Channel 3 in relation to Channel 1 using the PHASE_CORR_12 and PHASE_CORR_13 coefficients. PHASE_CORR_1x represents the tangent of the orthogonality error between Channel x and Channel 1, $\tan(\alpha_{phase_error})$. When implementing phase correction, the gain correction value for the respective channel must be adapted by a factor of $1 / \cos(\alpha_{phase_error})$.

Channels are assigned as shown in the table below according to DATA_SEL and ANGLE_EN bitfields. Offset and gain correction must be implemented before phase correction to identify the phase error between

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normalized waveforms. PHASE_CORR_12 and PHASE_CORR_13 are 16-bit 2's complement bit fields with a range of -4 to 3.9999, which allows for phase correction of up to ±75 degrees.

Equation 7 and Equation 8 outline the calculations performed in the phase correction block.

$$\text{CHANNEL_2_PHASE_CORR} = \text{CHANNEL_2} + (\text{CHANNEL_1} \times \text{PHASE_CORR_12}) \quad (7)$$

$$\text{CHANNEL_3_PHASE_CORR} = \text{CHANNEL_3} + (\text{CHANNEL_1} \times \text{PHASE_CORR_13}) \quad (8)$$

Table 7-5. Channel Assignments for Phase Correction

DATA_SEL	ANGLE_EN	Channel 1	Channel 2	Channel 3
0h, 4h	0h	Y	X	n/a
	1h	X	Y	n//a
	2h	Z	X	n/a
	3h	X	Z	n/a
	4h	Y	Z	n/a
	5h	Z	Y	n/a
1h	n/a	X	n/a	n/a
2h	n/a	Y	n/a	n/a
3h	n/a	Z	n/a	n/a
5h	6h, 7h	Z	X	Y
6h	n/a	Z	X	Y

Section 7.3.11 shows an example of the phase correction.

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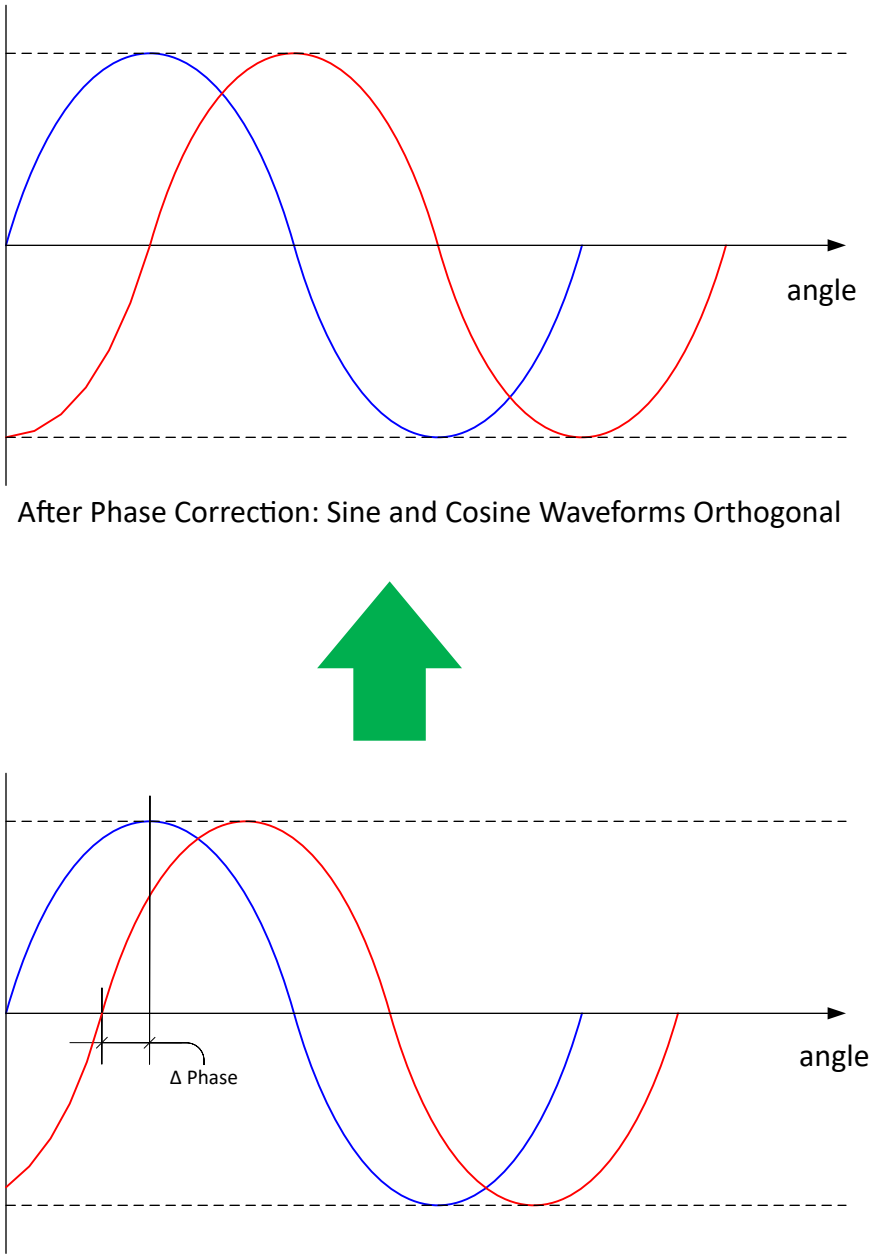


Figure 7-6. TMAG3101-Q1 Phase Correction

7.3.12 2D Angle Definition

The TMAG3101-Q1 supports 2D angle calculation based off two magnetic axes when the ANGLE_EN bits are set between 000b and 101b. As examples the particular 2D angle calculation for ANGLE_EN = 000b and 001b are described in Equation 9 and Equation 10 respectively.

$$\text{2D Angle} = \text{ARCTAN2}\left[\frac{\text{Y}}{\text{X}}\right] \tag{9}$$

$$\text{2D Angle} = \text{ARCTAN2}\left[\frac{\text{X}}{\text{Y}}\right] \tag{10}$$

where

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- X and Y are the linear magnetic field data for the X and Y axes respectively, after polarity, temperature, offset, gain, and phase correction.

7.3.13 Alpha and Beta Angle Definition

The TMAG3101-Q1 supports simultaneous calculations of 2D plane alpha and beta angles when the ANGLE_EN bits are set to 110b. The 2D alpha and beta definitions are explained in Equation 11 and Equation 12.

$$\text{2D ALPHA} = \text{ARCTAN2}\left[\frac{Z}{X}\right] \tag{11}$$

$$\text{2D BETA} = \text{ARCTAN2}\left[\frac{Z}{Y}\right] \tag{12}$$

where

- X, Y, and Z are the linear magnetic field data for the X, Y and Z axes respectively

The TMAG3101-Q1 supports simultaneous calculations of 3D alpha and beta angles when the ANGLE_EN bits are set to 111b. The 3D alpha and beta definitions are explained in Equation 13 and Equation 14.

$$\text{3D ALPHA} = \text{ARCTAN2}\left[\frac{\sqrt{Z^2 + Y^2}}{X}\right] \tag{13}$$

$$\text{3D BETA} = \text{ARCTAN2}\left[\frac{\sqrt{Z^2 + X^2}}{Y}\right] \tag{14}$$

where

- X, Y, and Z are the linear magnetic field data for the X, Y and Z axes respectively after polarity, temperature coefficient, offset, gain, and phase correction.

Figure 7-7 shows the 2D and 3D alpha/ beta angle references.

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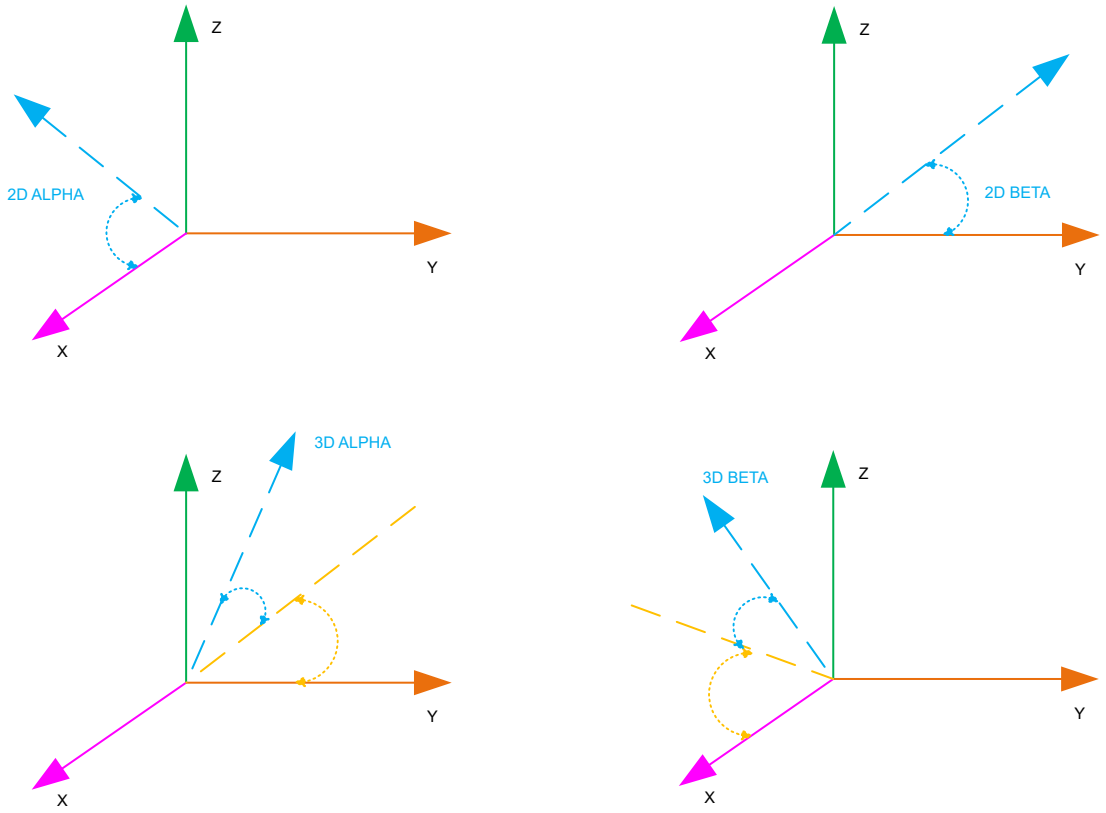


Figure 7-7. Alpha and Beta Angle Definition

7.3.14 Angle Polarity

ANGLE_POL is used to reverse the direction of the rotation reporting for 2D angle calculation, ALPHA angle only, BETA angle only, or ALPHA and BETA angles. Polarity correction is shown in Equation 15 and Equation 16.

$$A_1 = A_0 \; for \; ANGLE_POL = 0h \tag{15}$$

$$A_1 = 360 - A_0 \; for \; ANGLE_POL \; = 1h \tag{16}$$

7.3.15 Angle Offset

ANGLE_OFFSET allows the user to set the zero angle point at the output of the CORDIC angle calculation to align electrical and mechanical angles. ANGLE_OFFSET[15:0] is a 16-bit two's complement bit field with a range of -180° to +179.99° and a resolution of 0.0055°. Angle offset is applied as shown in Equation 17.

$$\mathrm{A_2 = mod(A_1 + ANGLE_OFFSET,\ 360)} \tag{17}$$

7.3.16 Linearization

The TMAG3101-Q1 supports multiple fixed and variable point linearization options for the X, Y, Z, or CORDIC angle output data. Use the LIN_SEL and LIN_TARGET register bits to select a particular option for a given application. Fixed point linearization is performed on the full magnetic or angle data range. The reference points (ref#) for fixed point linearization are factory defined as shown in Fixed Point Linearization. Variable point linearization options allow user defined reference points as shown in Variable Point Linearization.

The linearization scheme starts with storing an offset value against the first reference point (ref#1) as explained in *Detailed Design Procedure*. The linearization coefficients (coeff#) for each reference points are calculated from the slope of the error curve between the two reference points.

The reference points and offset associated with ref#1 follow the same data format as defined in *Data Definition*.

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Store the linearization coefficient values (coeff#) in the Q10p6-format as shown in Figure 7-8.

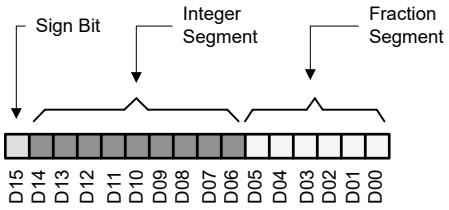


Figure 7-8. Linearization Coefficient Format

Use Equation 18 to calculate the linearization coefficient values. As an example, a coefficient of 25.375 is entered as 0358h.

$$C = (D_{15} \times (-1)) \times \left(\sum_{i=0}^{14} D_i \times 2^{(i-6)}\right) \quad (18)$$

7.3.16.1 Fixed Point Linearization

The TMAG3101-Q1 offers multiple fixed point linearization options based off the LIN_SEL and LIN_TARGET register settings. For 2D angle data the fixed point linearization reference points are shown inTable 7-6. For linear data the fixed point linearization reference points are shown in Table 7-7. ALPHA, BETA angle measurements do not support fixed point linearization.

Table 7-6. 2D Angle Fixed Point Linearization Reference Points (in Degree Angle) (LIN_TARGET = 001b)

EEPROM Bitfield	LIN_SEL = 000b	LIN_SEL = 001b	LIN_SEL = 010b	LIN_SEL = 011b
	32-Point	16-Point	8-Point	4-Point
CAL_00	offset at 0°	offset at 0°	offset at 0°	offset at 0°
CAL_01	0°	0°	0°	0°
CAL_02	11.25°	22.5°	45°	90°
CAL_03	22.5°	45°	90°	180°
CAL_04	33.75°	67.5°	135°	270°
CAL_05	45°	90°	180°	
CAL_06	56.25°	112.5°	225°	
CAL_07	67.5°	135°	270°	
CAL_08	78.75°	157.5°	315°	
CAL_09	90°	180°		
CAL_10	101.25°	202.5°		
CAL_11	112.5°	225°		
CAL_12	123.75°	247.5°		
CAL_13	135°	270°		
CAL_14	146.25°	292.5°		
CAL_15	157.5°	315°		
CAL_16	168.75°	337.5°		
CAL_17	180°			
CAL_18	191.25°			
CAL_19	202.5°			
CAL_20	213.75°			
CAL_21	225°			
CAL_22	236.25°			
CAL_23	247.5°			
CAL_24	258.75°			

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Table 7-6. 2D Angle Fixed Point Linearization Reference Points (in Degree Angle) (LIN_TARGET = 001b) (continued)

EEPROM Bitfield	LIN_SEL = 000b	LIN_SEL = 001b	LIN_SEL = 010b	LIN_SEL = 011b
	32-Point	16-Point	8-Point	4-Point
CAL_25	270°			
CAL_26	281.25°			
CAL_27	292.5°			
CAL_28	303.75°			
CAL_29	315°			
CAL_30	326.25°			
CAL_31	337.5°			
CAL_32	348.75°			

Table 7-7. Linear Field Fixed Point Linearization Reference Points (in mT) (LIN_TARGET = 010b, 011b, or 100b)

EEPROM Bitfield	50mT Range				100mT Range				150mT Range			
	32-Point	16-Point	8-Point	4-Point	32-Point	16-Point	8-Point	4-Point	32-Point	16-Point	8-Point	4-Point
CAL_00	offset at -50mT	offset at -50mT	offset at -50mT	offset at -50mT	offset at -100mT	offset at -100mT	offset at -100mT	offset at -100mT	offset at -150mT	offset at -150mT	offset at -150mT	offset at -150mT
CAL_01	-50mT	-50mT	-50mT	-50mT	-100mT	-100mT	-100mT	-100mT	-150mT	-150mT	-150mT	-150mT
CAL_02	-46.875mT	-43.75mT	-37.5mT	-25mT	-93.75mT	-87.5mT	-75mT	-50mT	-140.625 mT	-131.25m T	-112.5mT	-75mT
CAL_03	-43.75mT	-37.5mT	-25mT	0mT	-87.5mT	-75mT	-50mT	0mT	-131.25m T	-112.5mT	-75mT	0mT
CAL_04	-40.625mT	-31.25mT	-12.5mT	25mT	-81.25mT	-62.5mT	-25mT	50mT	-121.875 mT	-93.75mT	-37.5mT	75mT
CAL_05	-37.5mT	-25mT	0mT		-75mT	-50mT	0mT		-112.5mT	-75mT	0mT	
CAL_06	-34.375mT	-18.75mT	12.5mT		-68.75mT	-37.5mT	25mT		-103.125 mT	-56.25mT	37.5mT	
CAL_07	-31.25mT	-12.5mT	25mT		-62.5mT	-25mT	50mT		-93.75mT	-37.5mT	75mT	
CAL_08	-28.125mT	-6.25mT	37.5mT		-56.25mT	-12.5mT	75mT		-84.375m T	-18.75mT	112.5mT	
CAL_09	-25mT	0mT			-50mT	0mT			-75mT	0mT		
CAL_10	-21.875mT	6.25mT			-43.75mT	12.5mT			-65.625m T	18.75mT		
CAL_11	-18.75mT	12.5mT			-37.5mT	25mT			-56.25mT	37.5mT		
CAL_12	-15.625mT	18.75mT			-31.25mT	37.5mT			-46.875m T	56.25mT		
CAL_13	-12.5mT	25mT			-25mT	50mT			-37.5mT	75mT		
CAL_14	-9.375mT	31.25mT			-18.75mT	62.5mT			-28.125m T	93.75mT		
CAL_15	-6.25mT	37.5mT			-12.5mT	75mT			-18.75mT	112.5mT		
CAL_16	-3.125mT	43.75mT			-6.25mT	87.5mT			-9.375mT	131.25mT		
CAL_17	0mT				0mT				0mT			
CAL_18	3.125mT				6.25mT				9.375mT			
CAL_19	6.25mT				12.5mT				18.75mT			
CAL_20	9.375mT				18.75mT				28.125mT			
CAL_21	12.5mT				25mT				37.5mT			
CAL_22	15.625mT				31.25mT				46.875mT			
CAL_23	18.75mT				37.5mT				56.25mT			
CAL_24	21.875mT				43.75mT				65.625mT			
CAL_25	25mT				50mT				75mT			
CAL_26	28.125mT				56.25mT				84.375mT			
CAL_27	31.25mT				62.5mT				93.75mT			

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Table 7-7. Linear Field Fixed Point Linearization Reference Points (in mT) (LIN_TARGET = 010b, 011b, or 100b) (continued)

EEPROM Bitfield	50mT Range				100mT Range				150mT Range			
	32-Point	16-Point	8-Point	4-Point	32-Point	16-Point	8-Point	4-Point	32-Point	16-Point	8-Point	4-Point
CAL_28	34.375mT				68.75mT				103.125mT			
CAL_29	37.5mT				75mT				112.5mT			
CAL_30	40.625mT				81.25mT				121.875mT			
CAL_31	43.75mT				87.5mT				131.25mT			
CAL_32	46.875mT				93.75mT				140.625mT			mT

7.3.16.2 Variable Point Linearization

The TMAG3101-Q1 offers multiple variable point linearization options based off the LIN_SEL and LIN_TARGET register settings. In variable point linearization, the linearization reference points are user-defined. The references must be entered in ascending order. Several EEPROM mapping examples are described in Table 7-8.

Table 7-8. Variable Point Linearization Mapping in EEPROM

EEPROM Bitfield	LIN_TARGET = 001b, 010b, 011b, or 100b			LIN_TARGET = 101b	
	LIN_SEL = 100b	LIN_SEL = 101b	LIN_SEL = 110b	LIN_SEL = 101b	LIN_SEL = 110b
	16-Point X, Y, Z, or 2D-Angle	8-Point X, Y, Z, or 2D-Angle	4-Point X, Y, Z, or 2D-Angle	7-Point ALPHA-BETA	3-Point ALPHA-BETA
CAL_00	offset	offset	offset	ALPHA_offset	ALPHA_offset
CAL_01	ref#1	ref#1	ref#1	ALPHA_ref#1	ALPHA_ref#1
CAL_02	coeff#1	coeff#1	coeff#1	ALPHA_coeff#1	ALPHA_coeff#1
CAL_03	ref#2	ref#2	ref#2	ALPHA_ref#2	ALPHA_ref#2
CAL_04	coeff#2	coeff#2	coeff#2	ALPHA_coeff#2	ALPHA_coeff#2
CAL_05	ref#3	ref#3	ref#3	ALPHA_ref#3	ALPHA_ref#3
CAL_06	coeff#3	coeff#3	coeff#3	ALPHA_coeff#3	ALPHA_coeff#3
CAL_07	ref#4	ref#4	ref#4	ALPHA_ref#4	RESERVED
CAL_08	coeff#4	coeff#4	coeff#4	ALPHA_coeff#4	BETA_offset
CAL_09	ref#5	ref#5		ALPHA_ref#5	BETA_ref#1
CAL_10	coeff#5	coeff#5		ALPHA_coeff#5	BETA_coeff#1
CAL_11	ref#6	ref#6		ALPHA_ref#6	BETA_ref#2
CAL_12	coeff#6	coeff#6		ALPHA_coeff#6	BETA_coeff#2
CAL_13	ref#7	ref#7		ALPHA_ref#7	BETA_ref#3
CAL_14	coeff#7	coeff#7		ALPHA_coeff#7	BETA_coeff#3
CAL_15	ref#8	ref#8		RESERVED	
CAL_16	coeff#8	coeff#8		BETA_offset	
CAL_17	ref#9			BETA_ref#1	
CAL_18	coeff#9			BETA_coeff#1	
CAL_19	ref#10			BETA_ref#2	
CAL_20	coeff#10			BETA_coeff#2	
CAL_21	ref#11			BETA_ref#3	
CAL_22	coeff#11			BETA_coeff#3	
CAL_23	ref#12			BETA_ref#4	
CAL_24	coeff#12			BETA_coeff#4	
CAL_25	ref#13			BETA_ref#5	

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Table 7-8. Variable Point Linearization Mapping in EEPROM (continued)

EEPROM Bitfield	LIN_TARGET = 001b, 010b, 011b, or 100b			LIN_TARGET = 101b	
	LIN_SEL = 100b	LIN_SEL = 101b	LIN_SEL = 110b	LIN_SEL = 101b	LIN_SEL = 110b
	16-Point X, Y, Z, or 2D-Angle	8-Point X, Y, Z, or 2D-Angle	4-Point X, Y, Z, or 2D-Angle	7-Point ALPHA-BETA	3-Point ALPHA-BETA
CAL_26	coeff#13			BETA_coeff#5	
CAL_27	ref#14			BETA_ref#6	
CAL_28	coeff#14			BETA_coeff#6	
CAL_29	ref#15			BETA_ref#7	
CAL_30	coeff#15			BETA_coeff#7	
CAL_31	ref#16				
CAL_32	coeff#16				

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7.3.17 Threshold Check

The TMAG3101-Q1 enables magnetic, angle, angle magnitude, and temperature threshold checks through the selection of the corresponding x_THRESHOLD EEPROM bits. Multiple thresholds can be enabled at the same time, and the first threshold cross triggers the response through the OUT pin. The default factory setting for all the thresholds checks are disabled. For a ±50mT magnetic field range Table 7-9 shows examples of threshold selections.

Table 7-9. Threshold Setting Examples

Threshold Type	Threshold Setting	Threshold Checks
2D Angle	A_HLT_EN = 0h	No angle threshold enabled
	A_HLT_EN = 1h, 2D_A_LO_THRESHOLD = 4000h, 2D_A_HI_THRESHOLD = FFFFh	Angle lower threshold is enabled at 90°. For example, threshold cross is detected if angle is measured at 45°
	A_HLT_EN = 1h, 2D_A_LO_THRESHOLD = 4000h, 2D_A_HI_THRESHOLD = A000h	Both angle lower threshold (90°) and upper threshold (225°) are enabled. For example, threshold cross is detected if angle is measured at 45° or 280°.
	A_HLT_EN = 1h, 2D_A_LO_THRESHOLD =0000h, 2D_A_HI_THRESHOLD =A000h	Angle upper threshold is enabled at 225°. For example, threshold cross is detected if angle is measured at 280°
Z Sensor Data	Z_HLT_EN = 0h	No magnetic threshold enabled
	Z_HLT_EN = 1h, Z_LO_THRESHOLD = C000h, Z_HI_THRESHOLD = 7FFFh	Z axis lower threshold is enabled at –25.62mT. For example, threshold cross is detected if Z magnetic field is measured at –26mT.
	Z_HLT_EN = 1h, Z_LO_THRESHOLD = C000h, Z_HI_THRESHOLD = 3000h	Both Z axis lower threshold (–25.62mT) and upper threshold (19.21mT) are enabled. For example, threshold cross is detected if Z magnetic field is measured at –26mT or 19.5mT.
	Z_HLT_EN = 1h, Z_LO_THRESHOLD = FFFFh, Z_HI_THRESHOLD =3000h	Z axis upper threshold is enabled at 19.21mT. For example, threshold cross is detected if Z magnetic field is measured at 19.5mT.
Temperature data	T_HLT_EN = 1h, T_LO_THRESHOLD = FFFFh, T_HI_THRESHOLD = 2F00h	Temperature upper threshold is enabled at 94°C. For example, threshold cross is detected if temperature is measured at 100°C
	T_HLT_EN = 1h, T_LO_THRESHOLD = F880h, T_HI_THRESHOLD = 2F00h	Both temperature lower threshold (–15°C) and upper threshold (94°C) are enabled. For example, threshold cross is detected if temperature is measured at –17°C or 100°C

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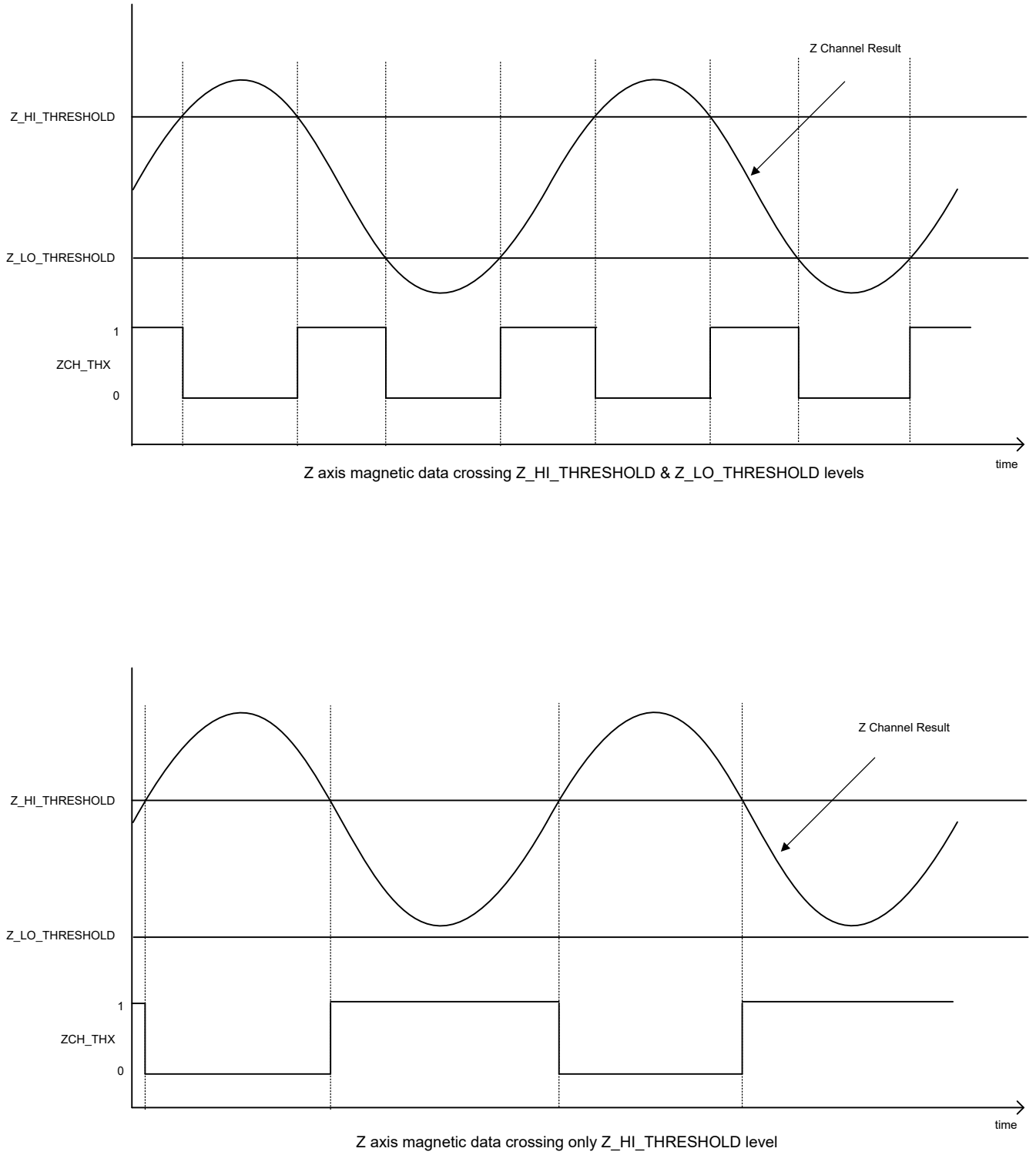


Figure 7-9. Z Channel Magnetic Threshold Examples When Z_HLT_EN = 1h, Z_LO_THRESHOLD = C000h, Z_HI_THRESHOLD = 3000h

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7.3.18 Analog/PWM Output Range Scaling

During Analog or PWM mode the TMAG3101-Q1 output full-scale range can be adjusted by setting the A_PWM_OUT_SCALE bit. This scaling feature helps enhance the output range for Analog or PWM signal in applications where full magnetic or angle ranges are not required. The Analog or PWM mode supports only one set of data to be transmitted based off the DATA_SEL and ANGLE_EN bits selections. With A_PWM_OUT_SCALE bit set, the device looks into corresponding *_THRESHOLD fields for the lower and upper limits to adjust the output full-scale range. Note that the scaling can degrade when the thresholds are too close together. Recommend at least 4096LSB difference between high and low thresholds. For the ±50mT magnetic field range, Table 7-10 shows examples of output full-scale range adjustments.

Table 7-10. Analog/PWM Output Range Scaling Examples

Analog/ PWM Output Type	A_PWM_OUT_SCALE	Threshold Setting	Output Full-Scale Range
2D Angle	0h	2D_A_LO_THRESHOLD =xxxxh, 2D_A_HI_THRESHOLD =xxxxh	0° to 360°
	1h	2D_A_LO_THRESHOLD =4000h, 2D_A_HI_THRESHOLD =FFFFh	90° to 360°
	1h	2D_A_LO_THRESHOLD =4000h, 2D_A_HI_THRESHOLD =A000h	90° to 225°
	1h	2D_A_LO_THRESHOLD =0000h, 2D_A_HI_THRESHOLD =A000h	0° to 225°
Z Sensor Data	0h	Z_LO_THRESHOLD =xxxxh, Z_HI_THRESHOLD =xxxxh	–51.24mT to 51.24mT
	1h	Z_LO_THRESHOLD =C000h, Z_HI_THRESHOLD =7FFFh	–25.62mT to 51.24mT
	1h	Z_LO_THRESHOLD =C000h, Z_HI_THRESHOLD =3000h	–25.62mT to 19.21mT
	1h	Z_LO_THRESHOLD =FFFFh, Z_HI_THRESHOLD =3000h	–51.24mT to 19.21mT

Figure 7-10 and Figure 7-11 show examples of Analog and PWM output scaling examples with 2D angle data respectively.

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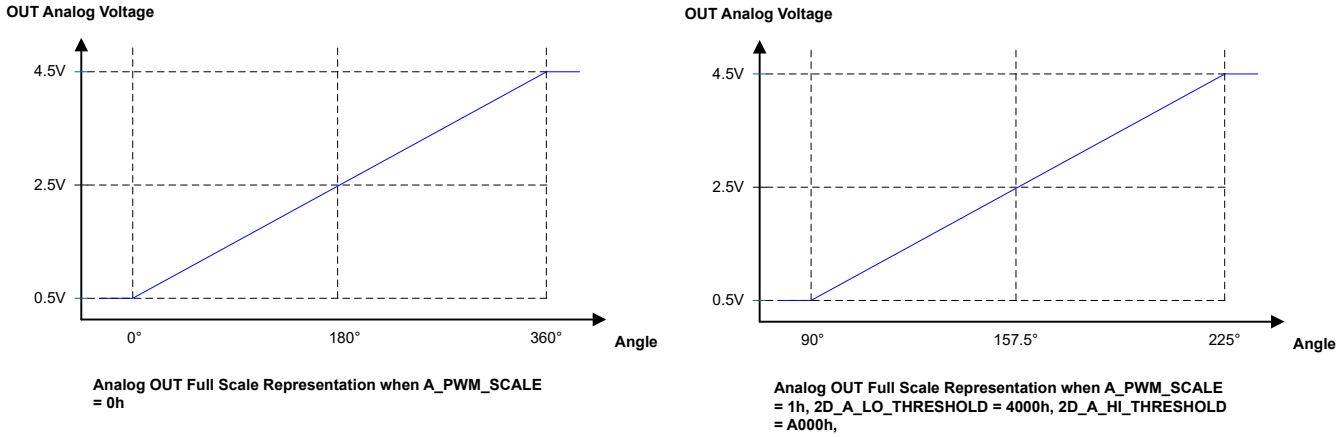
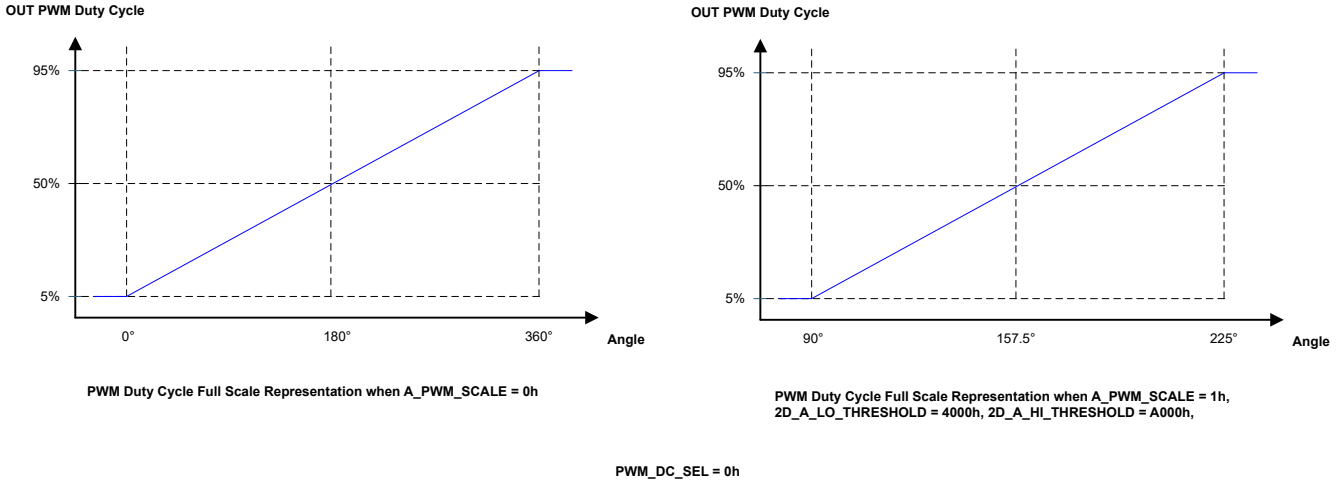


Figure 7-10. Analog Output Scaling Example



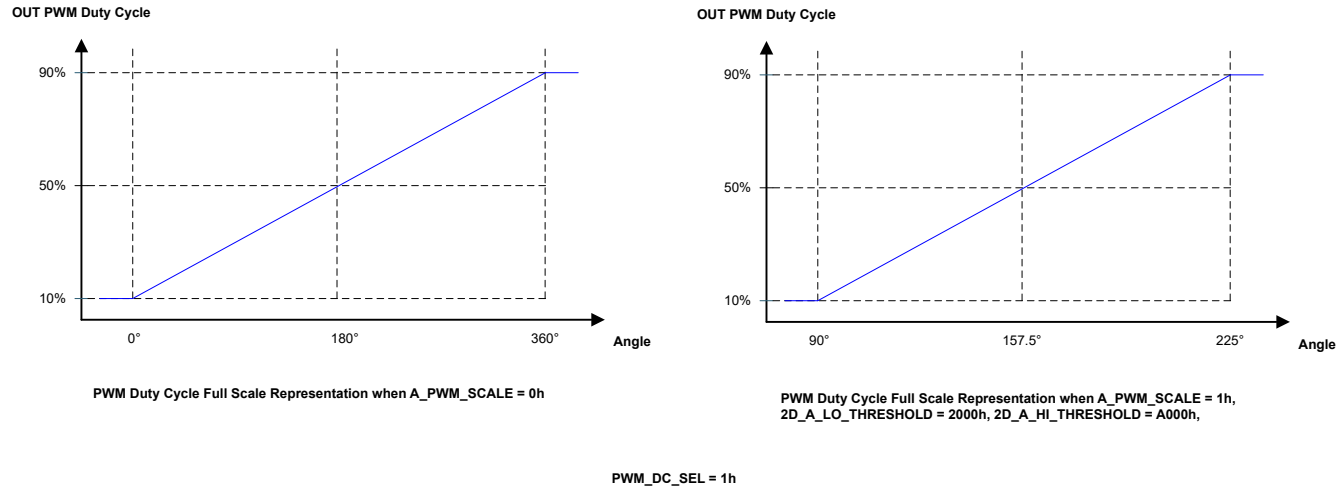


Figure 7-11. PWM Output Scaling Example

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7.3.19 Diagnostics

The TMAG3101-Q1 supports several device and system level diagnostics features to detect, monitor, and report failures during the device operation.

In the event of a failure, the TMAG3101-Q1 reports back to the controller through the following mechanisms:

- Status bits or high impedance during the SENT communications
- OUT pin high impedance during PWM and Analog mode communications; external pull up resistor pulls OUT into diagnostic range (Vout > 0.95*VCC in Analog mode or output duty cycle > 97% in PWM mode)
- No response through the OUT line, or CRC error during SENT communication

The TMAG3101-Q1 performs the following device and system level checks:

7.3.19.1 EEPROM Power Fault Check

This diagnostic mechanism verifies power is good during EEPROM programming. EEPROM programming operation is initiated by SWIFT Copy Scratchpad command. Following the start of programming, the Host issues SWIFT Read strobes. While programming is in progress, the reads return 1's. When programming completes, 0's are returned. If there is an EEPROM programming voltage fault, 0's are never returned and the E2P_PWRF flag is set. The flag can be cleared by writing 1 to E2P_PWRF or power cycling the device.

Item	Description
Run mode	Continuous during EEPROM Programming
Fault response	SWIFT read strobes during EEPROM programming never returns a 0. E2P_PWRF bit is set.
Fault register bit	E2P_PWRF
Impact if disabled	Cannot be disabled
Fault recovery	Write 1 to clear E2P_PWRF bit or device power cycle

7.3.19.2 EEPROM ECC Check

The EEPROM ECC checks the content of the internal EEPROM to correct any single error occurrence. In case any double error occurrence, the device OUT pin goes to high impedance state and flags the EEPROM_DED bit. EEPROM_DED cannot be read by the SWIFT interface as the interface immediately triggers the output to be disabled when set. Device power cycle is required for recovery.

Item	Description
Run mode	Continuous
Fault response	SENT - high impedance PWM - high impedance Analog - high impedance
Fault register bit	EEPROM_DED
Impact if disabled	Cannot be disabled
Fault recovery	Power cycle

7.3.19.3 VCC Check

This diagnostic mechanism continuously checks the external voltage supply on VCC pin and flags a fault if the supply is out of range. VCC_OV and VCC_UV cannot be read by the SWIFT interface as the interface immediately triggers the device output to be disabled when set. The processor clears these bits when the over- or under-voltage condition is removed.

Item	Description
Run mode	Continuous
Datasheet parameters	V_{VCC_UV}, V_{VCC_OV}
Fault register bit	VCC_UV and VCC_OV

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Item	Description
Fault response	SENT - high impedance followed by error communication via status bit 0 (S0) once error is removed PWM - high impedance Analog - high impedance
Fault recovery	The device goes to normal operating mode with the VCC returning within V_{VCC_UV} and V_{VCC_OV}. For SENT interface the VCC_UV and VCC_OV flags removed after the completion of the slow serial message containing the corresponding flag.

7.3.19.4 OUT Overcurrent Protection

This diagnostic mechanism continuously monitors the current through the OUT pin and disables the output to protect the device in case of an overcurrent condition.

Item	Description
Run mode	Continuous
Datasheet parameters	I_{OUT}, Absolute Maximum Ratings
Fault register bit	N/A
Fault response	SENT - high impedance PWM - high impedance Analog - high impedance
Fault recovery	Power cycle after fault cleared when LOCKOUT = Eh. When LOCKOUT ≠ Eh, device can recover without power cycle when condition removed.

7.3.19.5 Oscillator Integrity Check

This diagnostic mechanism allows the controller to check any hardware fault or drift of the internal oscillators. OSC_ERR cannot be read by the SWIFT interface as OSC_ERR immediately triggers the device output to be disabled when set. Device power cycle is required for recovery.

Item	Description
Run mode	Continuous
Datasheet parameters	f_{CLK_HF}, f_{CLK_LF}
Fault register bit	OSC_ERR
Impact if disabled	Cannot be disabled.
Fault response	SENT - high impedance PWM - high impedance Analog - high impedance
Fault recovery	Power cycle

7.3.19.6 Internal LDO Under Voltage Check

This diagnostic mechanism continuously monitors the internal regulator that supplies the critical analog blocks and Hall sensor biasing, and flags a fault if the internal regulator falls below a threshold after which the accuracy of the magnetic field measurement cannot be guaranteed. LDO_STAT cannot be read by the SWIFT interface as LDO_STAT immediately triggers the device output to be disabled when set. The processor clears this bit when the LDO undervoltage condition is removed.

Item	Description
Run mode	Continuous
Datasheet parameters	N/A
Fault register bit	LDO_STAT
Impact if disabled	Cannot be disabled

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Item	Description
Fault response	SENT - Error communication using the status bit 0 (S0). PWM - high impedance Analog - high impedance
Fault recovery	The device goes to normal operating mode with the internal LDO returning to normal voltage. For SENT interface the LDO_STAT flag is removed after the completion of the slow serial message containing the corresponding flag.

7.3.19.7 Power-On Reset (POR) Check

This diagnostic mechanism continuously monitors the supply rail, and puts the device OUT pin in high impedance state if the digital core cannot function reliably. The occurrence of the fault is detected when VCC goes below VCC_{POR}.

Item	Description
Run mode	Continuous
Datasheet parameter	VCC_{POR}
POR register bit	None
POR communication	SENT - null frame (all zeros) PWM - none Analog - none

7.3.19.8 Magnetic Field Threshold Check

This diagnostic mechanism allows the controller to monitor the external applied field. The controller can use this check to determine if a magnetic field is present within specified thresholds. This check, though used as check at system level, can also indicate any gross problems with the signal path if a field outside the expected range is detected and reported. The threshold checks are independent of any particular magnetic channel being enabled or disabled. Threshold checks for all axes can be enabled even when those axes are not currently being used in the signal datapath. XCH_THX, YCH_THX, and ZCH_THX can all be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic measurement is initiated and completed
Fault configuration registers	X_HLT_EN, Y_HLT_EN, Z_HLT_EN to enable test. X_HI_THRESHOLD, X_LO_THRESHOLD, Y_HI_THRESHOLD, Y_LO_THRESHOLD, Z_HI_THRESHOLD, Z_LO_THRESHOLD to set threshold.
Fault register bits	XCH_THX, YCH_THX, ZCH_THX
Fault response	SENT - communication via status bit 1 (S1) PWM - high impedance Analog - high impedance
Fault recovery	The XCH_THX, YCH_THX, ZCH_THX bits are reset at the beginning of each new conversion

7.3.19.9 Temperature Threshold Check

This diagnostic mechanism allows the controller to monitor the junction temperature of the die, which is also an indication of the ambient temperature as the device does not generate significant self-heating. This is useful to monitor the temperature at the system level accurately and alert the controller if the temperature is exceeded. The diagnostic mechanism can also be used to warn the controller if the die temperature has increased beyond the expected range due to some internal failure. TEMP_THX can be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic conversion is initiated and completed
Configuration registers	T_HLT_EN to enable test. T_HI_THRESHOLD, T_LO_THRESHOLD to set thresholds

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Item	Description
Fault register bit	TEMP_THX
Threshold check communication	SENT - communication via status bit 1 (S1) PWM - high impedance Analog - high impedance
Threshold check recovery	The TEMP_THX bit is reset at the beginning of each conversion

7.3.19.10 Analog Front-End (AFE) Check

This diagnostic mechanism allows the controller to check the performance of the analog signal path. In this check, the device disconnects the Hall sensor from the signal path and uses an alternate resistance bridge to create a known, predetermined signal as an input to the signal path. This mechanism then checks if the measured digital value compared to a fixed value from the factory is within a pre-programmed, factory-determined value. This mechanism can detect issues with multiplexers, offset cancellation mechanism, the gain stages, the low-pass filter, and the ADC, as well. AFE_FAIL can be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic measurement is initiated and completed
Configuration registers	DIAG_EN to enable test
Fault register bit	AFE_FAIL
Fault communication	SENT - communication via status bit 0 (S0) PWM - high impedance Analog - high impedance
Fault recovery	Power cycle required to clear

7.3.19.11 Hall Resistance and Switch Matrix Check

This diagnostic mechanism allows the controller to check if the sensitivity of the Hall sensor is within the factory-determined limits by checking the resistance of the Hall-effect sensor. In this check, the biasing and multiplexing control of all directions of the Hall sensor (X, Y and Z) are also checked. ZHS_STAT, YHS_STAT, XHS_STAT can all be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic measurement is initiated and completed
Configuration registers	DIAG_EN to enable test
Fault register bits	ZHS_STAT, YHS_STAT, XHS_STAT
Fault communication	SENT - communication via status bit 0 (S0) PWM - high impedance Analog - high impedance
Fault recovery	Power cycle required to clear

7.3.19.12 Hall Offset Check

This diagnostic mechanism allows the controller to check if the offset of the Hall sensor is within the factory-determined limits and the offset cancellation circuitry is working properly. HS_OFFSET_STAT can be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic measurement is initiated and completed
Configuration registers	DIAG_EN to enable test

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Item	Description
Fault communication	SENT - communication via status bit 0 (S0) PWM - high impedance Analog - high impedance
Fault register bit	HS_OFFSET_STAT
Fault recovery	Power cycle required to clear

7.3.19.13 ADC Check

This diagnostic mechanism checks ADC functionality and conversion. This check is done by converting a known bandgap voltage, which is completely independent of the ADC reference, and comparing the voltage against the factory-determined tolerance limits. ADC_FAIL can be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic measurement is initiated and completed
Configuration registers	DIAG_EN to enable test
Fault register bit	ADC_FAIL
Fault communication	SENT - communication via status bit 0 (S0) PWM - high impedance Analog - high impedance
Fault recovery	Power cycle required to clear

7.3.19.14 2D Angle or Alpha Angle Threshold Check

This diagnostic mechanism allows the controller to monitor the 2D angle or alpha angle threshold checks. Select 0h or 4h settings in the DATA_SEL for 2D angle threshold and 5h for alpha angle threshold. With each new conversion both high and low thresholds are checked. The device indicates threshold cross if the measured angle is below the low threshold or above the high threshold. 2D_A_THX can be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic measurement is initiated and completed
Configuration registers	2D_A_HLT_EN to enable test. 2D_A_HI_THRESHOLD and 2D_A_LO_THRESHOLD to set the upper and lower thresholds.
Fault register bit	2D_A_THX
Threshold check communication	SENT - communication via status bit 1 (S1) PWM - high impedance Analog - high impedance
Threshold check recovery	The 2D_A_THX bit is reset at the beginning of each new conversion

7.3.19.15 Magnitude or Beta Angle Threshold Check

This diagnostic mechanism allows the controller to monitor the magnitude or beta angle threshold checks. Select 0h or 4h settings in the DATA_SEL for magnitude threshold and 5h for beta angle threshold. With each new conversion both high and low thresholds are checked. The device indicates threshold cross if the measured value is below the low threshold or above the high threshold. MAG_B_THX can be read by the SWIFT interface when set.

Item	Description
Run mode	Every time a magnetic measurement is initiated and completed
Configuration registers	MAG_B_HLT_EN to enable test. MAG_B_HI_THRESHOLD, MAG_B_LO_THRESHOLD to set the upper and lower thresholds respectively.

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Item	Description
Fault register bit	MAG_B_THX
Threshold check communication	SENT - communication via status bit 1 (S1) PWM - high impedance Analog - high impedance
Threshold check recovery	The MAG_B_THX bit is reset at the beginning of each new conversion

7.3.19.16 Memory (RAM/ROM) Check

This diagnostic mechanism checks the content of the RAM and ROM to correct any single error occurrence. In case any double error occurrence, the device OUT pin goes to high impedance state and flag the MEM_ERR register bit. MEM_ERR cannot be read by the SWIFT interface as the interface immediately triggers the device output to be disabled when set. Device power cycle is required for recovery.

Item	Description
Run mode	Continuous
Fault response	SENT - high impedance PWM - high impedance Analog - high impedance
Fault register bit	MEM_ERR
Impact if disabled	Cannot be disabled
Fault recovery	Power cycle

7.3.19.17 Configuration Register Check

This diagnostic mechanism checks the content of the trim and device configuration hardware registers to detect a single error (SED) or double error (DED). In case any SED or DED is detected, the device OUT pin goes to high impedance state and flag the CONF_ERR register bit. CONF_ERR cannot be read by the SWIFT interface as the interface immediately triggers the device output to be disabled when set. Device power cycle is required for recovery.

Item	Description
Run mode	Continuous
Fault response	SENT - high impedance PWM - high impedance Analog - high impedance
Fault register bit	CONF_ERR
Impact if disabled	Cannot be disabled
Fault recovery	Power cycle

7.3.19.18 Stack Overflow Check

This diagnostic mechanism detects access to SRAM that is outside the memory space allocated for the stack. In case of error occurrence, the device OUT pin goes to high impedance state. STCKOVF is an internal only register, STCKOVF cannot be read by the SWIFT interface. A device power cycle is required for recovery.

Item	Description
Run mode	Continuous
Fault response	SENT - high impedance PWM - high impedance Analog - high impedance
Fault register bit	STCKOVF (internal)
Impact if disabled	Cannot be disabled
Fault recovery	Power cycle

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7.3.19.19 Watchdog Timer Check

This diagnostic mechanism verifies that the device is operating within expected timing constraints. In case a watchdog timer error occurs, the device output goes into a high impedance state. WDT_STAT is an internal only register. The register cannot be read using the SWIFT interface. Device power cycle is required for recovery.

Item	Description
Run mode	Continuous
Fault response	SENT - high impedance PWM - high impedance Analog - high impedance
Fault register bit	WDT_STAT (internal only)
Impact if disabled	Cannot be disabled
Fault recovery	Power cycle

7.3.19.20 Response to Diagnostic Error During SENT Output Modes

Table 7-11 describes the TMAG3101-Q1 response to different diagnostic failures during SENT communication.

Table 7-11. Response to Diagnostic Error During SENT Communication

Diagnostic	OUT status during fault	Reporting through SENT	Fault recovery	Fault communication through SENT fast channel
VCC under POR event	Hi-Z	First SENT fast channel frame data all zeros. Also reported through SENT slow serial message when enabled.	Power cycle	First SENT frame after power-up data all zeros
VCC under-voltage threshold cross	Hi-Z	Report fault during the first SENT frame after returning to normal VCC. Fault reporting happens through status nibble and the slow serial message. If error code ($1) is enabled, the fault condition is latched until the diagnostic message ($01) is complete. If $01 is not enabled, fault flag is cleared after the S0 is set and reported once	VCC rises above VCC_UV. The fault flag clears after successful SENT communication if no new fault is detected	Bit-0 (S0) of status nibble is set after VCC rises above VCC_UV
VCC over-voltage threshold cross	Hi-Z	Report fault during the first SENT frame after returning to normal VCC. Fault reporting happens through status nibble and the slow serial message. If error code ($1) is enabled, the fault condition is latched until the diagnostic message ($01) is complete. If $01 is not enabled, fault flag is cleared after the S0 of the status nibble is set and reported once.	VCC lowers below VCC_OV. The fault flag clears after successful SENT communication if no new fault is detected	Bit-0 (S0) of status nibble is set after VCC lowers below VCC_OV
OUT overcurrent protection	Hi-Z	SENT communication failure	Power cycle after fault cleared when LOCKOUT = Eh. When LOCKOUT ≠ Eh, device can recover without power cycle when condition removed.	First SENT frame after power-up data all zeros
Magnetic field threshold cross	Active	Report fault through status nibble and the slow serial message. If error code ($01) is enabled, the fault condition is latched until the diagnostic message ($01) is complete. If $01 is not enabled, fault flag is cleared after the S1 is set and reported once	The _THX bits are reset at the beginning of each new conversion	Bit-1 (S1) of status nibble is set
Angle or magnitude threshold cross	Active			
Temperature threshold cross	Active			
AFE diagnostic fail	Active	Report fault through status nibble bit 0 and the slow serial message if error code $01 is enabled.	Power cycle	Bit-0 (S0) of status nibble is set
Sensor offset/ resistance threshold cross	Active			
ADC check	Active			

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Table 7-11. Response to Diagnostic Error During SENT Communication (continued)

Diagnostic	OUT status during fault	Reporting through SENT	Fault recovery	Fault communication through SENT fast channel
EEPROM check	Hi-Z		Power cycle	First SENT frame after power-up data all zeros
SRAM check				
ROM check				
Stack Overflow check				
Oscillator check				
OUT short to VCC	Hi-Z if overcurrent occurs	SENT communication failure	Power cycle after fault cleared if overcurrent occurs when LOCKOUT = Eh. When LOCKOUT ≠ Eh, device can recover without power cycle when condition removed.	
OUT short to GND				

7.3.19.21 Response to Diagnostic Error During Analog/PWM Output Modes

Table 7-12 describes the TMAG3101-Q1 response to different diagnostic failures during Analog or PWM output modes.

Table 7-12. Response to Diagnostic Error During Analog/ PWM Communication

Diagnostic	Analog Mode		PWM Mode	
	OUT status during fault	Fault recovery	OUT status during fault?	Fault recovery
VCC under POR event	Hi-Z	Power cycle	Hi-Z	Power cycle
VCC under-voltage threshold cross	Hi-Z	OUT active after VCC rises above VCC_UV	Hi-Z	OUT active after VCC rises above VCC_UV
VCC over-voltage threshold cross	Hi-Z	OUT active after VCC lowers below VCC_OV	Hi-Z	OUT active after VCC lowers below VCC_OV
OUT overcurrent protection	Hi-Z	Power cycle after condition cleared	Hi-Z	Power cycle after condition cleared when LOCKOUT = Eh. When LOCKOUT ≠ Eh, device can recover without power cycle when condition removed.
Magnetic field threshold cross	Hi-Z	Fault cleared during new conversion if condition cleared	Hi-Z	Fault cleared during new conversion if condition cleared
Angle or magnitude threshold cross				
Temperature threshold cross				
AFE diagnostic fail	Hi-Z	Power cycle	Hi-Z	Power cycle
Sensor offset/resistance threshold cross				
ADC check				
EEPROM check	Hi-Z	Power cycle after condition cleared	Hi-Z	Power cycle after condition cleared
SRAM check				
ROM check				
Stack Overflow check				
Oscillator check				

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Table 7-12. Response to Diagnostic Error During Analog/ PWM Communication (continued)

Diagnostic	Analog Mode		PWM Mode	
	OUT status during fault	Fault recovery	OUT status during fault?	Fault recovery
OUT short to VCC	OUT in diagnostic band, or Hi-Z if overcurrent occurs	Power cycle after condition cleared if overcurrent occurs	OUT inside diagnostic band, or Hi-Z if overcurrent occurs	Power cycle after condition cleared if overcurrent occurs when LOCKOUT = Eh. When LOCKOUT ≠ Eh, device can recover without power cycle when condition removed.
OUT short to GND				

7.4 Device Functional Modes

7.4.1 Operating Modes

The TMAG3101-Q1 supports multiple operating modes selectable through the OPERATING_MODE register bits.

7.4.1.1 Single Wire Interface for Test (SWIFT) Mode (OPERATING_MODE = 0h)

Single Wire Interface for Test (SWIFT) mode is the programming mode and factory default mode for the TMAG3101-Q1. The device enters SWIFT mode during the first power up after the device is shipped from the factory with the OPERATING_MODE set at 0h. From SWIFT mode, the device can be configured to operate in any given mode, perform conversions, and store the calibration data in the device EEPROM. After the calibration and configuration are completed, power cycle the device to start operating at the desired mode.

The SWIFT_CPU_MAILBOX bitfield can be used to evaluate device configuration settings and operating modes without programming the OPERATING_MODE bitfield. When using SWIFT_CPU_MAILBOX commands 81h through 86h, the user is responsible for programming the relevant EEPROM bitfields for the desired operating mode.

SWIFT mode is available in open-drain output mode only. See Section 7.5.1 for more information.

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7.4.1.2 SENT and Triggered SENT Operating Modes

7.4.1.2.1 Synchronous Triggered SENT Mode (Triggered Conversions) (OPERATING_MODE = 1h)

The TMAG3101-Q1 supports synchronous trigger conversion and triggered SENT mode when the OPERATING_MODE is set to 1h. Synchronous triggered SENT mode is available in open-drain output mode only (BUF_SEL = 0h). In this mode a host triggers the device to start a new conversion and receives the result data through SENT interface from the previous conversion. If the host trigger intervals are slower than the device conversion time, the conversion and the SENT frames are synchronized properly without any missing or repeated frames as shown in Figure 7-12. If the host trigger intervals are faster than the device conversion time, data can repeat in the SENT frames and the device ignores a conversion trigger while another conversion is ongoing. Figure 7-13 shows this scenario. In this mode the SENT rolling counter follows the conversion data sequence count. Verify that the pause pulse is enabled (FLC = 1h) when using OPERATING_MODE = 1h.

In FEFE trigger mode, data is latched from the result registers just after the rising edge of the TIC0 command pulse. The new conversion sequence begins 1 unit tick + 3us after the rising edge of the TIC0 command pulse. This time varies based on TICK_SEL configuration.

In FERE trigger mode, data is latched at the end of the full 90-tick trigger pulse. The new conversion sequence begins 3us after the falling edge that ends the valid 90 tick FERE trigger pulse.

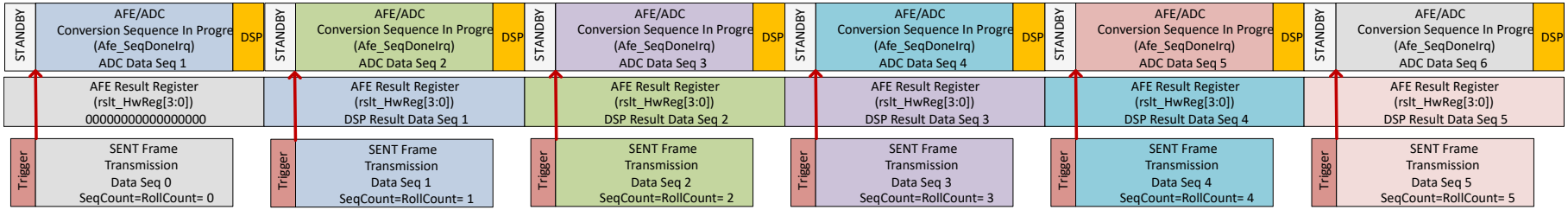


Figure 7-12. TMAG3101-Q1 Conversion Time Less Than SENT Frame Interval Time in Synchronous Triggered SENT Mode

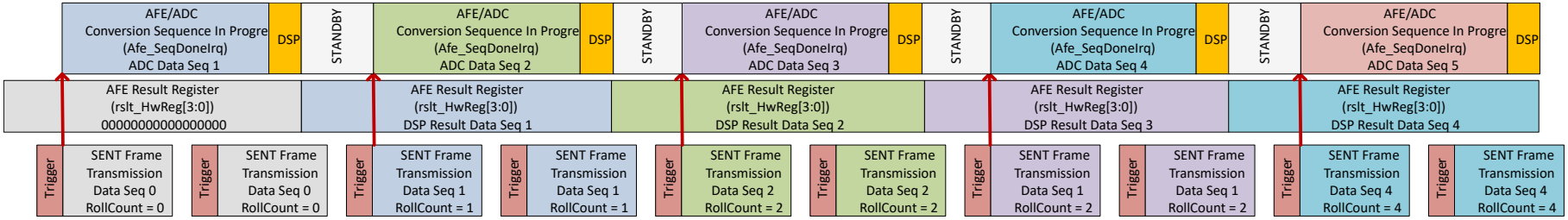


Figure 7-13. TMAG3101-Q1 Conversion Time Greater Than SENT Frame Interval Time in Synchronous Triggered SENT Mode

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7.4.1.2.2 Synchronous SENT Mode (Synchronized Conversions and SENT Frames) (OPERATING_MODE = 2h)

The TMAG3101-Q1 supports continuous conversion and triggered SENT mode when the OPERATING_MODE is set to 2h. Synchronous SENT mode is available in open-drain or push-pull output mode (BUF_SEL = 0h or 1h). In this mode the device initiates back-back continuous conversions. At the end of each new conversion the device triggers a new SENT frame to transmit the latest result. If the conversion time is slower than the SENT frame length, the conversion and the SENT frames are synchronized properly without any missing results as shown in Figure 7-14. If the conversion time is faster than the SENT frame length, results can be missed as the device ignores a new SENT frame trigger while the conversion is ongoing. This scenario is shown in Figure 7-15. In this mode the SENT rolling counter follows the conversion data sequence count. Verify that the pause pulse is enabled (FLC = 1h) when using OPERATING_MODE = 2h.

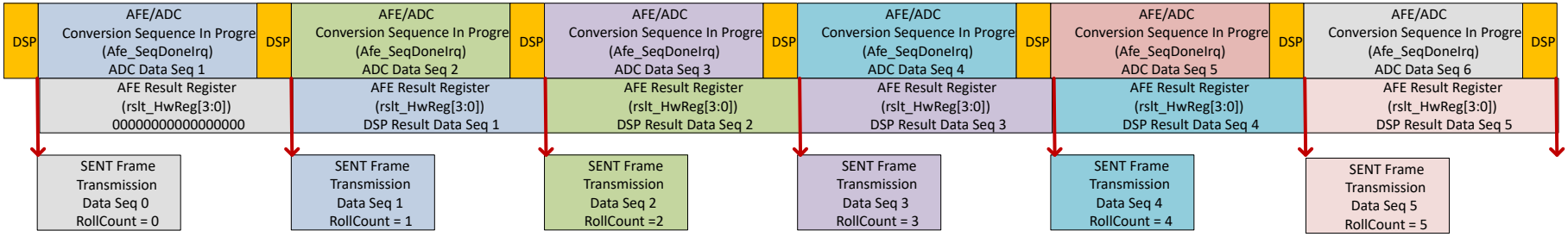


Figure 7-14. TMAG3101-Q1 Conversion Time Longer Than SENT Frame Length in Synchronous SENT Mode

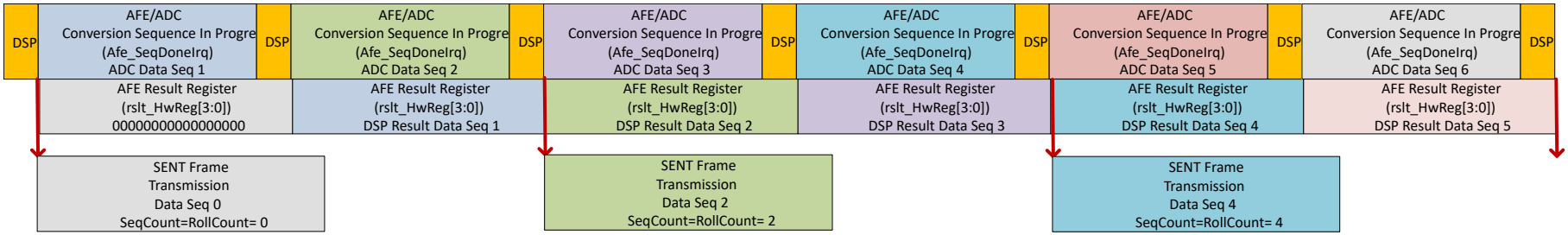


Figure 7-15. TMAG3101-Q1 Conversion Time Shorter Than SENT Frame Length in Synchronous SENT Mode

7.4.1.2.3 Asynchronous Triggered SENT Mode (Continuous Conversions) (OPERATING_MODE = 3h)

The TMAG3101-Q1 supports asynchronous continuous conversion and triggered SENT mode when the OPERATING_MODE is set to 3h. Asynchronous triggered SENT mode is available in open-drain output mode only (BUF_SEL = 0h). In this mode the device initiates back-back continuous conversions and a host triggers the device to send the most updated result through SENT frame asynchronously. If the host trigger intervals are slower than the device conversion time, there is possibility to miss some conversion results as shown in Figure 7-16. If the host trigger intervals are faster than the device conversion time, there is a possibility to transmit the same result data in the successive SENT frames as shown in Figure 7-17. In this mode the SENT rolling counter follows the SENT frame count. verify that the pause pulse is enabled (FLC = 1h) when using OPERATING_MODE = 3h.

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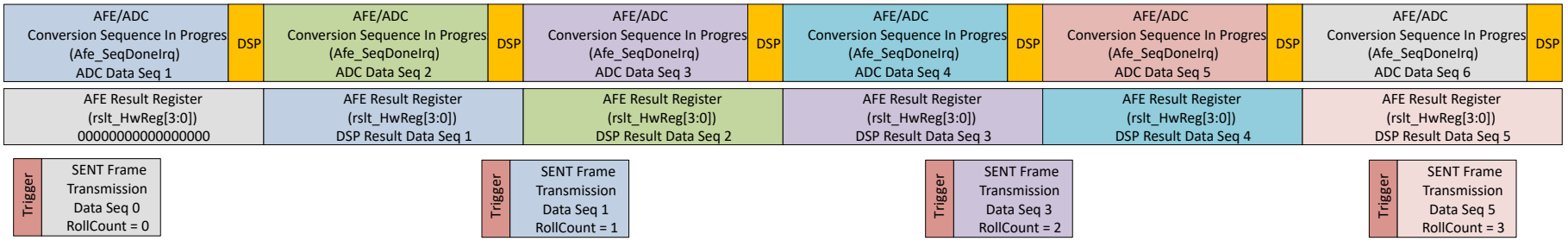


Figure 7-16. TMAG3101-Q1 Conversion Time Less Than SENT Frame Interval Time in Asynchronous Triggered SENT Mode

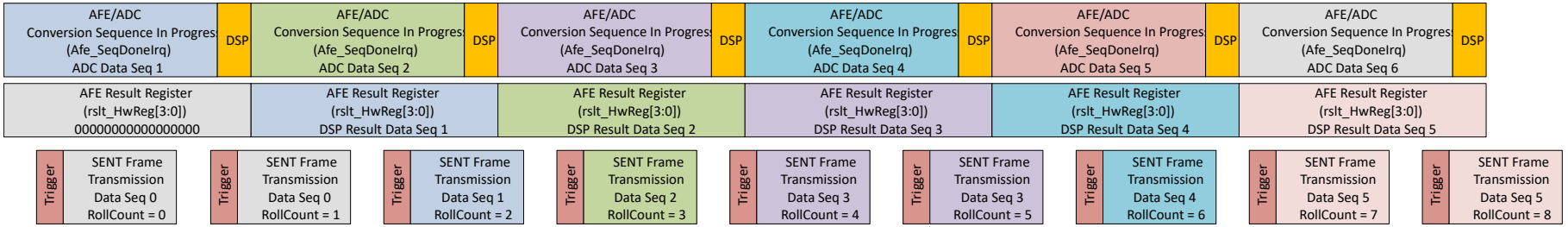


Figure 7-17. TMAG3101-Q1 Conversion Time Greater Than SENT Frame Interval Time in Asynchronous Triggered SENT Mode

7.4.1.2.4 Asynchronous SENT Mode (Continuous Conversion) (OPERATING_MODE = 4h)

The TMAG3101-Q1 supports asynchronous continuous conversion and continuous SENT mode when the OPERATING_MODE is set to 4h. Asynchronous SENT mode is available in open-drain or push-pull output mode (BUF_SEL = 0h or 1h). In this mode the device initiates back-back continuous conversions and send back-back SENT frames with the latest result available in the result registers. The AFE and ADC are running continuously. SENT frame frequency is set by user configured SENT settings. If the conversion time is slower than the SENT frame length, there is possibility of sending the same result through successive SENT frames as shown in Figure 7-18. If the conversion time is faster than the SENT frame length, there is possibility of missing results as the device does not initiate a new SENT frame until the old frame is complete. This scenario is shown in Figure 7-19. In this mode the SENT rolling counter follows the SENT frame count.

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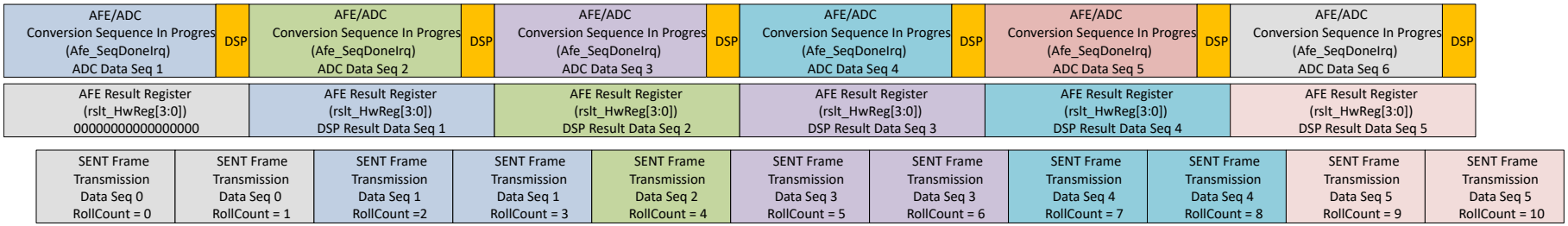


Figure 7-18. TMAG3101-Q1 Conversion Time Longer Than SENT Frame Length in Asynchronous SENT Mode

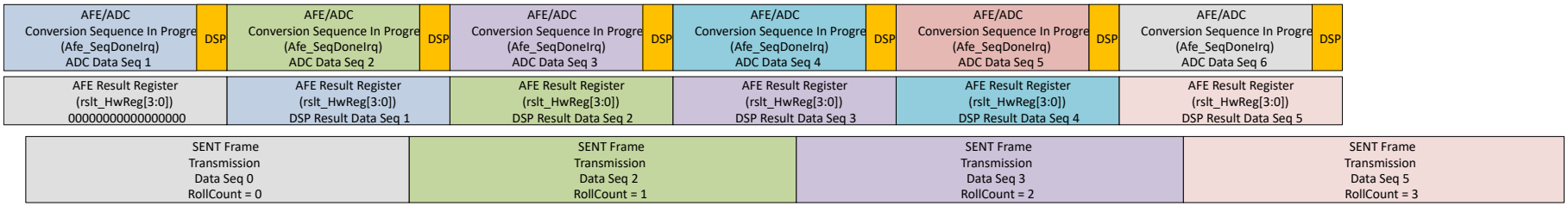


Figure 7-19. TMAG3101-Q1 Conversion Time Shorter Than SENT Frame Length in Asynchronous SENT Mode

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7.4.1.2.5 Triggered SENT Trigger Pulses

Host triggered SENT operating modes are available in open-drain output mode only (BUF_SEL = 0h).

7.4.1.2.5.1 Falling Edge, Falling Edge (FEFE) Trigger Pulse

When OPERATING_MODE = 1h or 3h and TRIGMODE = 0h, the Falling Edge, Falling Edge (FEFE) trigger pulse is enabled in host triggered SENT modes. The host drives the SENT line low to initiate communication of commands and device address. The duration of the low pulse is decoded as the command. The host then releases the SENT line before driving the line low a second time. The duration of the interval between the two falling edges is decoded as the target device address. The addressed device starts driving the SENT line low when a valid command and address are received. The host releases the SENT line and the target device continues to hold the SENT line low for the 6-ticks of the Sync Pulse of the data frame transmission.

The command and address duration boundaries are programmed in terms of unit ticks using the ADDR_MIN, ADDR_MAX bitfields and the TIC0_MIN and TIC0_MAX bitfields. As a result, trigger pulse timing varies depending on the configured TICK_SEL.

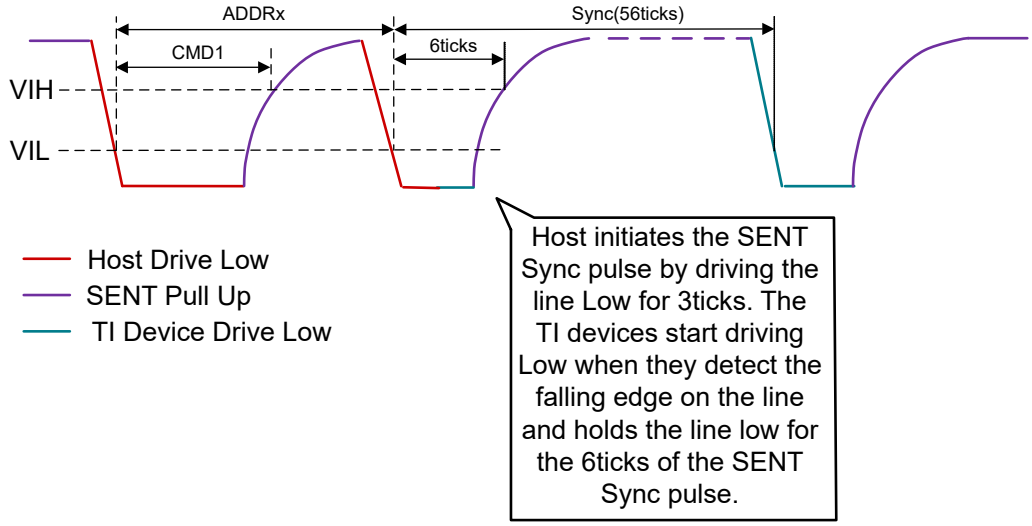


Figure 7-20. Falling Edge, Falling Edge Triggered SENT pulse

7.4.1.2.5.2 Falling Edge, Rising Edge (FERE) Trigger Pulse

When OPERATING_MODE = 1h or 3h and TRIGMODE = 1h, the Falling Edge, Rising Edge (FERE) trigger pulse is enabled in host triggered SENT modes. The host drives the SENT line low to initiate communication of the device address. The host then releases the SENT line. The duration of the interval between the falling edge and the rising edge is decoded as the target device address. 90 ticks after the falling edge, the addressed device starts driving the SENT line low for the 6-ticks of the Sync Pulse of the data frame transmission.

The address duration boundaries of the device are programmed in units of ticks can be configured by programming the ADDR_MIN and ADDR_MAX bitfields. As a result, the trigger pulse timing varies depending on the configured TICK_SEL setting.

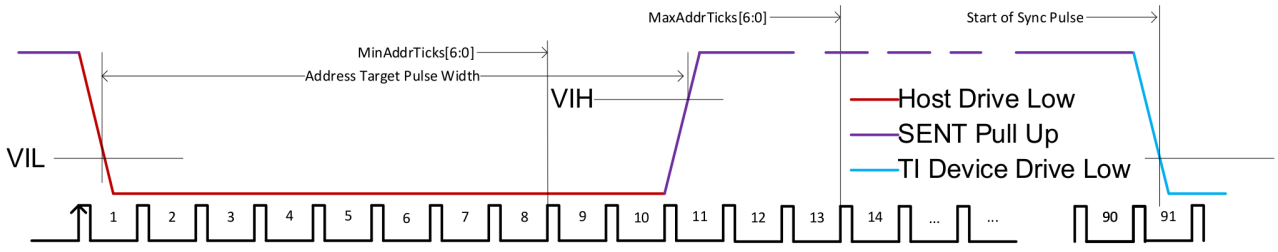


Figure 7-21. Falling Edge, Rising Edge Triggered SENT pulse

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7.4.1.2.6 SENT Data Formats

Each single-edge nibble transmission (SENT) frame contains a series of pulses consisting of a low interval and high interval. Each data pulse contains a nibble (4 bits) of data. The duration of each pulse is measured from falling edge to falling edge and has units of ticks. Use the TICK_SEL bitfield to select the SENT tick time. The high interval time is variable and indicates the data value of the nibble, described in Table 7-13. Each SENT frame consists of the following pulses:

1. Sync: 56 ticks, indicates the beginning of a SENT frame
2. Status: indicates TMAG3101-Q1 status and communicates slow channel data (if enabled)
3. Data: output magnetic channel, angle, and other optional data nibbles
4. CRC (Cyclical Redundancy Check): error checking
5. Pause Pulse: optional, can be used to enable constant frame length

Table 7-13. SENT Nibble Values

Nibble Duration (Total Ticks)	Hexadecimal Value
12	0h
13	1h
14	2h
15	3h
. . .	. . .
26	Eh
27	Fh

The TMAG3101-Q1 supports multiple SENT data outputs selectable from the DATA_SEL register bits. The output data is mapped as shown in Table 7-14 for 12-bit data, and Table 7-15 for 16-bit data.

Table 7-14. 12-Bit SENT Data Mapping (SENT_RES = 0b)

Data Type	MSN Nibble, N2	N1	LSN Nibble, N0
X_CH_RESULT, ANGLE_ALPHA	Data1_N3	Data1_N2	Data1_N1
Y_CH_RESULT, MAGNITUDE_BETA	Data2_N3	Data2_N2	Data2_N1
Z_CH_RESULT	Data3_N3	Data3_N2	Data3_N1
TEMP_RESULT (12-bit)	Data4_N3	Data4_N2	Data4_N1

Table 7-15. 16-Bit SENT Data Mapping (SENT_RES = 1b)

Data Type	MSN Nibble, N3	N2	N1	LSN Nibble, N0
X_CH_RESULT, ANGLE_ALPHA	Data1_N3	Data1_N2	Data1_N1	Data1_N0
Y_CH_RESULT, MAGNITUDE_BETA	Data2_N3	Data2_N2	Data2_N1	Data2_N0
Z_CH_RESULT	Data3_N3	Data3_N2	Data3_N1	Data3_N0
TEMP_RESULT (8-bit)			Data4_N3	Data4_N2

7.4.1.2.6.1 SENT Fast Frame Examples

Table 7-16 and Table 7-17 show SENT frame examples for the TMAG3101-Q1.

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Table 7-16. SENT Fast Channel Configuration Settings

Position Data 1				Position Data 2				Temperature Data			Rolling Counter		Inverted Data 1 MSN
Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat2_N3	Dat2_N2	Dat2_N1	Dat2_N0	T_N2	T_N1	T_N0	RC_N1	RC_N0	DAT1_N3_INV
Present when DATA_SEL = 0h to 5h 12-bit data if SENT_RES = 0h 16-bit data if SENT_RES = 1h				Present when DATA_SEL = 4h, 5h 12-bit data if SENT_RES = 0h 16-bit data if SENT_RES = 1h Nibble order reversed if DAT2_REV = 1h				Present when T_FAST = 1h 12-bit data if SENT_RES = 0h 8-bit data if SENT_RES = 1h Nibble order reversed if DATA_SEL = 0h to 3h and DAT2_REV = 1h			Present when ROLLC = 1h		Present when DAT1_MSN = 1h

Table 7-17. SENT Frame Examples for 2D Angle and Magnitude

SENT frame format	12-bit Data (SENT_RES = 0h)	16-bit Data (SENT_RES = 1h)	2D Angle (DATA_SEL = 0h)	2D Angle & Magnitude (DATA_SEL = 4h)	8- or 12-bit Temperature (T_FAST = 1h)	8-bit Rolling Counter (ROLL_C = 1h)	Data1 MSN Inverted Nibble (DATA1_MSN = 1h)	Data2 Nibble Order Reversed (DAT2_REV = 1h)	SYNC	STATUS	N1	N2	N3	N4	N5	N6	N7	N8	N9
H.2	x		x								Dat1_N3	Dat1_N2	Dat1_N1	CRC					
	x		x			x					Dat1_N3	Dat1_N2	Dat1_N1	ROLLC_N1	ROLLC_N0	CRC			
	x		x				x				Dat1_N3	Dat1_N2	Dat1_N1	DAT1_MSN	CRC				
	x		x			x	x				Dat1_N3	Dat1_N2	Dat1_N1	ROLLC_N1	ROLLC_N0	DAT1_MSN	CRC		
		x	x								Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	CRC				
		x	x			x					Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	ROLLC_N1	ROLLC_N0	CRC		
		x	x				x				Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	DAT1_MSN	CRC			
H.4		x	x			x	x				Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	ROLLC_N1	ROLLC_N0	DAT1_MSN	CRC	
H.1	x			x				x			Dat1_N3	Dat1_N2	Dat1_N1	Dat2_N1	Dat2_N2	Dat2_N3	CRC		
	x			x		x		x			Dat1_N3	Dat1_N2	Dat1_N1	Dat2_N1	Dat2_N2	Dat2_N3	ROLLC_N1	ROLLC_N0	CRC

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Table 7-17. SENT Frame Examples for 2D Angle and Magnitude (continued)

SENT frame format	12-bit Data (SENT_RES = 0h)	16-bit Data (SENT_RES = 1h)	2D Angle (DATA_SEL = 0h)	2D Angle & Magnitude (DATA_SEL = 4h)	8- or 12-bit Temperature (T_FAST = 1h)	8-bit Rolling Counter (ROLL_C = 1h)	Data1 MSN Inverted Nibble (DATA1_MSN = 1h)	Data2 Nibble Order Reversed (DAT2_REV = 1h)	SYNC	STATUS	N1	N2	N3	N4	N5	N6	N7	N8	N9
	x			x			x	x			Dat1_N3	Dat1_N2	Dat1_N1	Dat2_N1	Dat2_N2	Dat2_N3	DAT1_MSN	CRC	
	x			x							Dat1_N3	Dat1_N2	Dat1_N1	Dat2_N3	Dat2_N2	Dat2_N1	CRC		
	x			x		x					Dat1_N3	Dat1_N2	Dat1_N1	Dat2_N3	Dat2_N2	Dat2_N1	ROLLC_N1	ROLLC_N0	CRC
	x			x			x				Dat1_N3	Dat1_N2	Dat1_N1	Dat2_N3	Dat2_N2	Dat2_N1	DAT1_MSN	CRC	
		x		x							Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat2_N3	Dat2_N2	Dat2_N1	Dat2_N0	CRC
		x		x				x			Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat2_N0	Dat2_N1	Dat2_N2	Dat2_N3	CRC
	x		x		x						Dat1_N3	Dat1_N2	Dat1_N1	Dat4_N3	Dat4_N2	Dat4_N1	CRC		
	x		x		x	x					Dat1_N3	Dat1_N2	Dat1_N1	Dat4_N3	Dat4_N2	Dat4_N1	ROLLC_N1	ROLLC_N0	CRC
	x		x		x		x				Dat1_N3	Dat1_N2	Dat1_N1	Dat4_N3	Dat4_N2	Dat4_N1	DAT1_MSN	CRC	
H.1	x		x		x			x			Dat1_N3	Dat1_N2	Dat1_N1	Dat4_N1	Dat4_N2	Dat4_N3	CRC		
	x		x		x	x		x			Dat1_N3	Dat1_N2	Dat1_N1	Dat4_N1	Dat4_N2	Dat4_N3	ROLLC_N1	ROLLC_N0	CRC
	x		x		x		x	x			Dat1_N3	Dat1_N2	Dat1_N1	Dat4_N1	Dat4_N2	Dat4_N3	DAT1_MSN	CRC	
		x	x		x						Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat4_N3	Dat4_N2	CRC		
		x	x		x	x					Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat4_N3	Dat4_N2	ROLLC_N1	ROLLC_N0	CRC
		x	x		x		x				Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat4_N3	Dat4_N2	DAT1_MSN	CRC	
H.7		x	x		x			x			Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat4_N2	Dat4_N3	CRC		

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Table 7-17. SENT Frame Examples for 2D Angle and Magnitude (continued)

SENT frame format	12-bit Data (SENT_RES = 0h)	16-bit Data (SENT_RES = 1h)	2D Angle (DATA_SEL = 0h)	2D Angle & Magnitude (DATA_SEL = 4h)	8- or 12-bit Temperature (T_FAST = 1h)	8-bit Rolling Counter (ROLL_C = 1h)	Data1 MSN Inverted Nibble (DATA1_MSN = 1h)	Data2 Nibble Order Reversed (DAT2_REV = 1h)	SYNC	STATUS	N1	N2	N3	N4	N5	N6	N7	N8	N9
		x	x		x	x		x			Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat4_N2	Dat4_N3	ROLLC_N1	ROLLC_N0	CRC
		x	x		x		x	x			Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	Dat4_N2	Dat4_N3	DAT1_MSN	CRC	

SENT fast channel multiplexing mode enables X, Y, and Z magnetic data in sequential SENT frames. The Frame Control (FC) nibble indicates the data represented in the frame. For example, FC = 0h indicates X axis data, FC = 1h indicates Y axis data, FC = 2h indicates Z axis data, and FC = 3h indicates temperature data. A Data Consistency Counter (DCC) nibble can also be enabled, and indicates that the data with the same DCC value is from the same conversion set. The DCC is incremented with each recurrence of the Frame Control sequence.

Table 7-18. SENT Frame Examples for Fast Channel Multiplexing

12-bit data (SENT_RES = 0b)	16-bit data (SENT_RES = 1b)	Temperature (T_FAST = 1h)	3-axis linear Fast Channel Multiplexing (DATA_SEL = 110b)	Data Consistency Counter (DCC	SYNC	STATUS	N1	N2	N3	N4	N5	N6	N7
X			X				FC = 0	Dat1_N3	Dat1_N2	Dat1_N1	CRC		
							FC = 1	Dat2_N3	Dat2_N2	Dat2_N1	CRC		
							FC = 2	Dat3_N3	Dat3_N2	Dat3_N1	CRC		

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Table 7-18. SENT Frame Examples for Fast Channel Multiplexing (continued)

12-bit data (SENT_RES = 0b)	16-bit data (SENT_RES = 1b)	Temperature (T_FAST = 1h)	3-axis linear Fast Channel Multiplexing (DATA_SEL = 110b)	Data Consistency Counter (DCC	SYNC	STATUS	N1	N2	N3	N4	N5	N6	N7
X		X	X				FC = 0	Dat1_N3	Dat1_N2	Dat1_N1	CRC		
							FC = 1	Dat2_N3	Dat2_N2	Dat2_N1	CRC		
							FC = 2	Dat3_N3	Dat3_N2	Dat3_N1	CRC		
							FC = 3	Dat4_N3	Dat4_N2	Dat4_N1	CRC		
X			X	X			FC = 0	DC = n	Dat1_N3	Dat1_N2	Dat1_N1	CRC	
							FC = 1	DC = n	Dat2_N3	Dat2_N2	Dat2_N1	CRC	
							FC = 2	DC = n	Dat3_N3	Dat3_N2	Dat3_N1	CRC	
X		X	X	X			FC = 0	DC = n	Dat1_N3	Dat1_N2	Dat1_N1	CRC	
							FC = 1	DC = n	Dat2_N3	Dat2_N2	Dat2_N1	CRC	
							FC = 2	DC = n	Dat3_N3	Dat3_N2	Dat3_N1	CRC	
							FC = 3	DC = n	Dat4_N3	Dat4_N2	Dat4_N1	CRC	
	X		X				FC = 0	Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	CRC	
							FC = 1	Dat2_N3	Dat2_N2	Dat2_N1	Dat2_N0	CRC	
							FC = 2	Dat3_N3	Dat3_N2	Dat3_N1	Dat3_N0	CRC	

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Table 7-18. SENT Frame Examples for Fast Channel Multiplexing (continued)

12-bit data (SENT_RES = 0b)	16-bit data (SENT_RES = 1b)	Temperature (T_FAST = 1h)	3-axis linear Fast Channel Multiplexing (DATA_SEL = 110b)	Data Consistency Counter (DCC	SYNC	STATUS	N1	N2	N3	N4	N5	N6	N7
	X	X	X				FC = 0	Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	CRC	
							FC = 1	Dat2_N3	Dat2_N2	Dat2_N1	Dat2_N0	CRC	
							FC = 2	Dat3_N3	Dat3_N2	Dat3_N1	Dat3_N0	CRC	
							FC = 3	Dat4_N3	Dat4_N2	Dat4_N1	Dat4_N0	CRC	
	X		X	X			FC = 0	DC = n	Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	CRC
							FC = 1	DC = n	Dat2_N3	Dat2_N2	Dat2_N1	Dat2_N0	CRC
							FC = 2	DC = n	Dat3_N3	Dat3_N2	Dat3_N1	Dat3_N0	CRC
	X	X	X	X			FC = 0	DC = n	Dat1_N3	Dat1_N2	Dat1_N1	Dat1_N0	CRC
							FC = 1	DC = n	Dat2_N3	Dat2_N2	Dat2_N1	Dat2_N0	CRC
							FC = 2	DC = n	Dat3_N3	Dat3_N2	Dat3_N1	Dat3_N0	CRC
							FC = 3	DC = n	Dat4_N3	Dat4_N2	Dat4_N1	Dat4_N0	CRC

7.4.1.2.6.2 SENT CRC Calculation

The TMAG3101-Q1 performs mandatory 4-bit CRC for SENT fast frame. The status nibble is not included in the CRC calculation. The data integrity is maintained for the SENT output by a 4-bit CRC covering the content of the outgoing SENT frames. The 4-bit CRC code is generated by the polynomial:

$$x^4 + x^3 + x^2 + 1 \quad (19)$$

There is a separate 6-bit CRC for the enhanced serial message. The 6-bit CRC code is generated by the polynomial:

$$x^6 + x^4 + x^3 + 1 \quad (20)$$

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7.4.1.2.6.3 SENT Slow Channel Data

The TMAG3101-Q1 supports the slow serial message through the status nibble of the fast channel communication. The slow serial message channel is particularly useful to send error diagnostics and other status signals that do not require as fast update as the sensor conversion data. The following slow serial messages can be selected through SENT_SLOW_CH register bits.

7.4.1.2.6.3.1 Short Serial Message

Short Serial Message Format shows the Short Serial Message Format for transmitting 8 bits of slow channel data when SENT_SLOW_CH = 1h. For this format, bit 3 in the status nibble of the fast channel frame starts at logic 1 and then stays at logic 0 for the next 15 frames. This fixed code of logic 1 followed by 15 logic 0s indicates where each slow channel message starts and ends. The message ID, 8-bit slow channel data word, and 4-bit CRC are contained in status bit 2 transmitted one bit at a time over multiple fast channel frames. The device requires 16 fast channel message frames to send one Short Serial Message.

Table 7-19. Short Serial Message Format

Received Status Nibble	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
S[3]	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S[2]	4-bit ID				8-bit data								4-bit CRC			

7.4.1.2.6.3.2 Enhanced Serial Message

The Enhanced Serial Message Format transmits slow channel data in either 12 or 16 bit format. A configuration bit is used to indicate 12-bit or 16-bit format. Table 7-20 shows the 12-bit data with an 8-bit message ID when SENT_SLOW_CH = 2h. Table 7-21 shows the 16-bit data with a 4-bit message ID when SENT_SLOW_CH = 3h. Sending a message using the Enhanced Serial Messaging Format requires 18 fast channel message frames. Similar to the Short Serial Message, the Enhanced Serial Messaging data are sent 2 bits at a time and comprise bit 3 and bit 2 of the status nibble.

Table 7-20. 12-bit Enhanced Serial Message

Received Status Nibble	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
S[3]	1	1	1	1	1	1	0	0	8-bit ID[7:4]				0	8-bit ID[3:0]				0
S[2]	6-bit CRC						12-bit data											

Table 7-21. 16-bit Enhanced Serial Message

Received Status Nibble	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
S[3]	1	1	1	1	1	1	0	1	4-bit ID				0	16-bit data[15:12]				0
S[2]	6-bit CRC						16-bit data[11:0]											

7.4.1.2.6.3.3 Slow Serial Message Data

The TMAG3101-Q1 offers an array of slow serial data as described in EEPROM_CONFG2. Table 7-22 explains different options to send slow serial messages along with the mapping message IDs and data locations.

Table 7-22. Slow Serial Message IDs

Short-serial Message 4 bit ID	Enhanced Message 8 bit ID	Enhanced Message 4 bit ID	EEPROM_CONFG2 Bit	Data Source	Comments
$0-$1	$23	$0	S_TEMP_EN	TEMP_RESULT	For short serial message, $0 and $1 corresponds to 8MSB and 8LSB bits respectively
$F	$01	$01	S_ERROR_EN		Error code communication

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Table 7-22. Slow Serial Message IDs (continued)

Short-serial Message 4 bit ID	Enhanced Message 8 bit ID	Enhanced Message 4 bit ID	EEPROM_CONFG2 Bit	Data Source	Comments
	$03		S_SENS_TYPE_EN	SENSOR_TYPE[11:0]	Describes the type of sensor
	$05		S_MAN_CODE_EN	TI_MAN_CODE[11:0]	TI manufacturer code
	$06		S_PROT_REV_EN	PROTOCOL_REV[11:0]	SENT protocol revision
	$07		S_FAST_CH1_CH_EN	FAST_CH_CHR_X1[11:0]	Fast channel 1 Characteristic X1
	$08		S_FAST_CH1_CH_EN	FAST_CH_CHR_X2[11:0]	Fast channel 1 Characteristic X2
	$09		S_FAST_CH1_CH_EN	FAST_CH_CHR_Y1[11:0]	Fast channel 1 Characteristic Y1
	$0A		S_FAST_CH1_CH_EN	FAST_CH_CHR_Y2[11:0]	Fast channel 1 Characteristic Y2
	$29		S_SENSOR_ID_EN	{DIE_ID_LOT[4:0], 3'b000, DIE_ID_WAFER[4:0]}	Sensor ID #1
	$2A		S_SENSOR_ID_EN	{DIE_ID_LOT[11:8], 5'b00000, DIE_ID_FAB[2:0]}	Sensor ID #2
	$2B		S_SENSOR_ID_EN	{DIE_ID_LOT[19:16], DIE_ID_X[7:0]}	Sensor ID #3
	$2C		S_SENSOR_ID_EN	{DIE_ID_LOT[27:24], DIE_ID_Y[7:0]}	Sensor ID #4
	$90		S_OEM_CODE_EN	ASCII_OEM_1[11:0]	ASCII character OEM codes
	$91		S_OEM_CODE_EN	ASCII_OEM_2[11:0]	ASCII character OEM codes
	$92		S_OEM_CODE_EN	ASCII_OEM_3[11:0]	ASCII character OEM codes
	$93		S_OEM_CODE_EN	ASCII_OEM_4[11:0]	ASCII character OEM codes
	$94		S_OEM_CODE_EN	ASCII_OEM_5[11:0]	ASCII character OEM codes
	$95		S_OEM_CODE_EN	ASCII_OEM_6[11:0]	ASCII character OEM codes
	$96		S_OEM_CODE_EN	ASCII_OEM_7[11:0]	ASCII character OEM codes
	$97		S_OEM_CODE_EN	ASCII_OEM_8[11:0]	ASCII character OEM codes

7.4.1.2.6.3.4 Slow Serial Message Error Code

The TMAG3101-Q1 offers flexible error code communications as described in Table 7-23.

Table 7-23. Slow Serial Message IDs

Short-serial Message 8-bit	Enhanced Message 12-bit	Enhanced Message 16-bit	Diagnostic	Comments
0	0	0	Power on reset event	
1	1	1	Under-voltage threshold cross	VCC_UV
2	2	2	Over-voltage threshold cross	VCC_OV

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Table 7-23. Slow Serial Message IDs (continued)

Short-serial Message 8-bit	Enhanced Message 12-bit	Enhanced Message 16-bit	Diagnostic	Comments
3	3	3	Magnetic field threshold cross	XCH_THX YCH_THX ZCH_THX
4	4	4	Angle magnitude threshold cross	2DA_THX MAG_B_THX
5	5	5	Temperature threshold cross	TEMP_THX
6	6	6	AFE diagnostic fail	AFE_FAIL
7	7	7	ADC check fail	ADC_FAIL
	8	8	Hall offset check fail	HS_OFFSET_STAT
	9	9	Hall resistance check fail	XHS_STAT YHS_STAT ZHS_STAT
	10	10	LDO undervoltage check fail	LDO_STAT
	11	11	Reserved	
		12	Reserved	
		13	Reserved	
		14	Reserved	
		15	Reserved	

7.4.1.3 Analog Continuous Conversion Mode (OPERATING_MODE = 6h)

With OPERATING_MODE set at 6h, the TMAG3101-Q1 goes into the active ratiometric analog output mode with an output range of $0.1\times V_{CC}$ to $0.9\times V_{CC}$. In this mode the device performs continuous conversions according to MAG_CH_EN. The selected sensor data is transferred to a primary after converting the data stream in analog form. X axis magnetic data, Y axis magnetic data, Z axis magnetic data, or a 2D angle calculation are data output options in analog mode. In this mode, only one sensor can be active in the same analog line.

If LOCKOUT ≠ Eh, there is a 40ms timeout at power up before entering analog mode to allow the user to re-enter SWIFT programming mode. When LOCKOUT = Eh, the device enters directly into analog mode.

Set LOAD_SEL to the appropriate value depending on the capacitive load being driven on the OUT pin in Analog mode.

7.4.1.4 PWM Continuous Conversion Mode (OPERATING_MODE = 7h)

With OPERATING_MODE set at 7h, the TMAG3101-Q1 goes into the active PWM output mode. In this mode the device performs continuous conversions according to MAG_CH_EN. The selected sensor data is transferred to a primary after converting the data stream in PWM form. X axis magnetic data, Y axis magnetic data, Z axis magnetic data, or a 2D angle calculation are data output options in PWM mode. In this mode only one sensor can be active in the same PWM line. PWM cycles must be read from falling edge to falling edge.

PWM is available in open-drain or push-pull output mode (BUF_SEL = 0h or 1h). PWM_FREQ_SEL sets the PWM carrier frequency. PWM_DC_SEL sets the PWM full scale duty cycle range to either 5% to 95% or 10% to 90%.

7.5 Programming

7.5.1 Single Wire Interface for Test (SWIFT) Protocol Overview

The TMAG3101-Q1 supports the SWIFT interface for the device calibration and programming. SWIFT timing and data transfer protocol is based on the TI SDQ interface. The SWIFT features that are common to SDQ include open-drain drivers, the capability to host multiple devices on a single wire, to enumerate the connected devices without prior knowledge of the unique device IDs. SWIFT extends the capability of SDQ by enabling a flexible timing regime which is driven by the SWIFT host during initialization of a command sequence.

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The following symbols are defined on the SWIFT bus:

- Timing Reset Pulse – Driven by the host to reinitialize SWIFT timing regime.
- Standard Reset Pulse – Driven by Host to initiate each SWIFT command sequence and sets the timing range for bit transactions.
- Presence Pulse – Response from SWIFT devices to acknowledge receipt of a Standard Reset and to confirm the received timing range is accepted.
- Host Write One, Host Write Zero – Driven by Host with timing aligned to the Synchronization Nibble to transfer data to the SWIFT devices.
- Host Read One, Host Read Zero – Host initiates Read One/Zero transfers with a Read-Slot Pulse. For One-bits to be transferred, the SWIFT device allows the line to return to High. For Zero-bits to be transferred, the SWIFT device pulls the line Low for the duration of the Read Zero timing.
- Synchronization Nibble – The set of four bits that are driven by Host as part of the Command Byte following receipt of a Presence Pulse.

The flexible timing regime of SWIFT allows communication timing to be set relative to the minimum reliable Low pulse that can be reliably transferred based on the electrical characteristics of the application. Alternatively, SWIFT timing can be set by the minimum time that the Host interface hardware can drive the SWIFT timing regime. In Figure 7-22 below, T defines time of the minimum pulse duration.

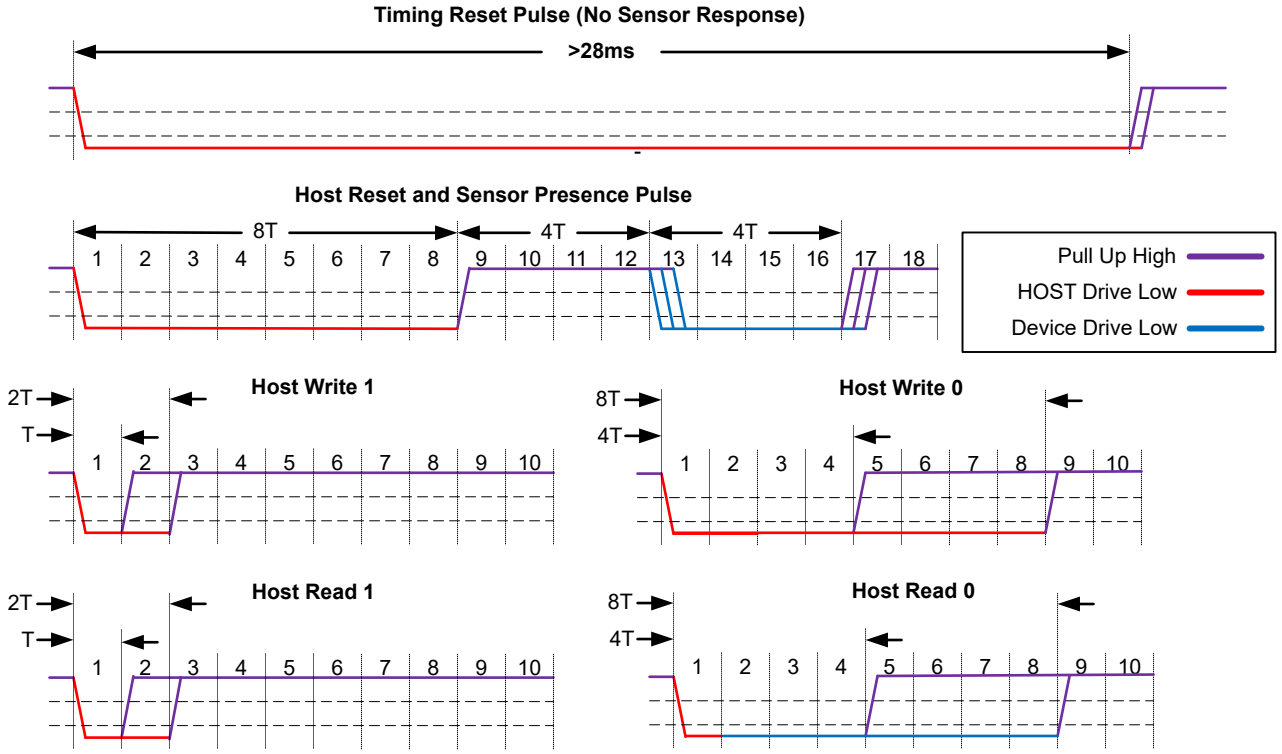


Figure 7-22. SWIFT Symbol Timing Requirements

SWIFT timing is designed to enable use of a standard UART to handle the communication protocol. The host SWIFT driver is required to be open-drain. Consequently, a discrete component with open-drain drive can be required between the host and the SWIFT devices. A difference between the Host interface voltage and the pull up voltage (VPU) can exist and require level translation. Slow slew rates that are tolerated by SWIFT can require a hysteresis buffer to drive the Host input.

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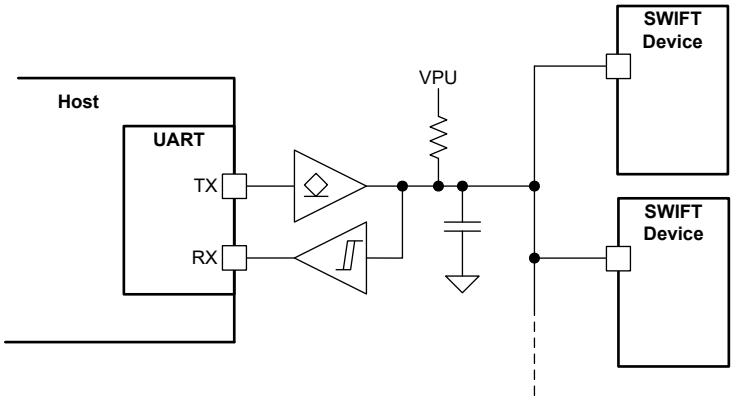


Figure 7-23. UART Controlling Multiple SWIFT Device

Figure 7-22 shows idealized SWIFT timing aligned into a UART Tx/Rx 8-bit frame with Start and Stop bits included. Note that Baud setting changes are required between the Reset and Presence Pulse symbols and the Host bit transactions. The time T represents the minimum Low pulse width transmitted on the SWIFT wire. The minimum value of T can be limited by the electrical characteristics of SWIFT wire and drivers or limited by the capability of the host to generate the minimum pulse timing.

Several SWIFT commands involve an 8-bit CRC for data integrity. The SWIFT CRC8 is generated by the polynomial $x^8 + x^5 + x^4 + 1$.

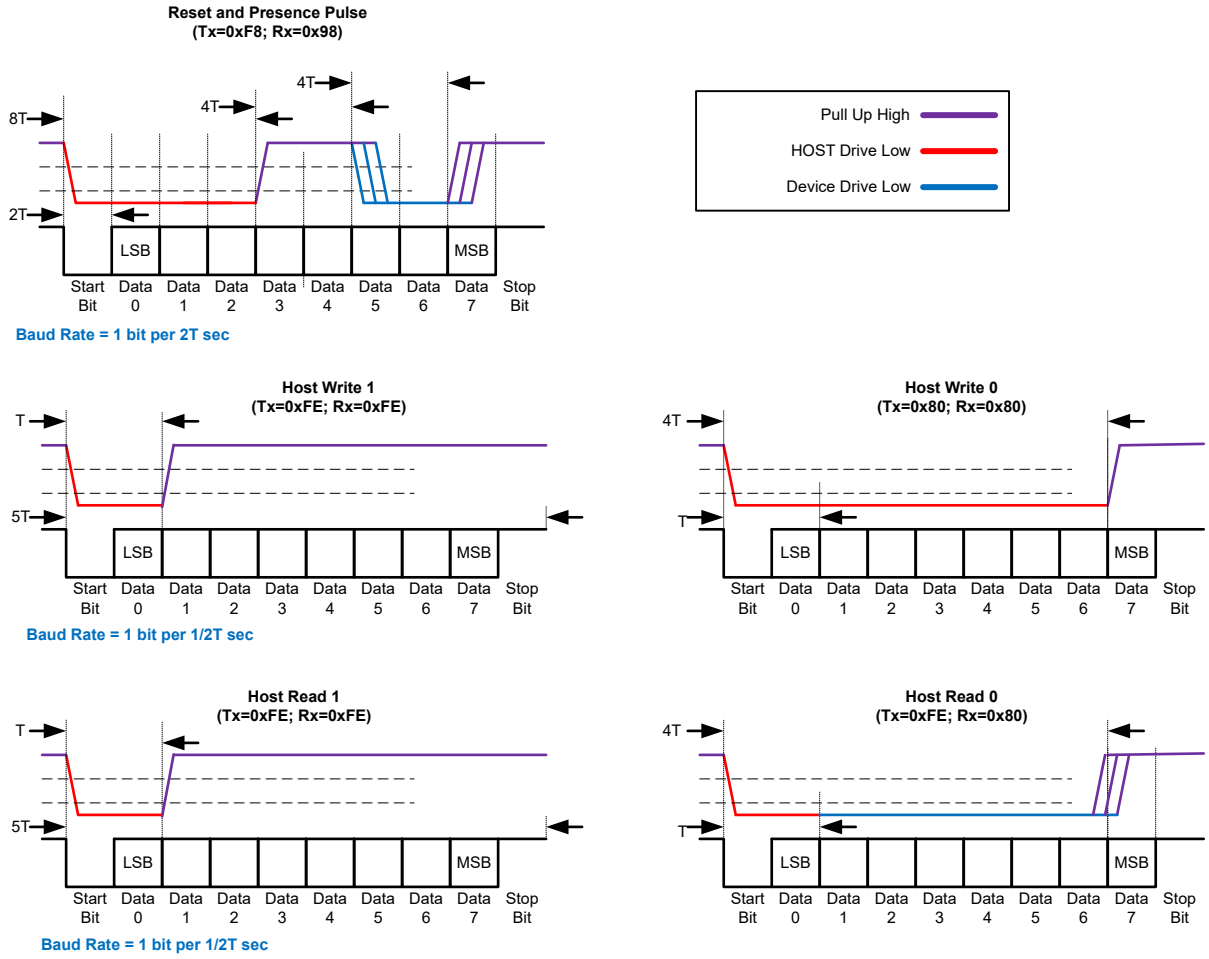


Figure 7-24. SWIFT Timing With an UART

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7.5.1.1 UART Implementation of SWIFT Symbols

The TMAG3101-Q1 SWIFT timing symbols are defined in a way that there is a direct mapping to standard UART driven timing.

7.5.1.1.1 Timing Reset Pulse

When the TMAG3101-Q1 SWIFT Timing Reset Pulse is received, the connected SWIFT devices resets a timing regime that has been previously been established. The next Standard Reset pulse width sets the new range for the timing regime that the reset pulse intended to establish. The Timing Reset can be issued at any time to interrupt a command sequence and restart SWIFT communication with a new timing regime.

The SWIFT Timing Reset requires a minimum Low interval of greater than 28ms. The Timing Reset Pulse can be implemented with a standard UART set to 300 Baud transmitting 0x00.

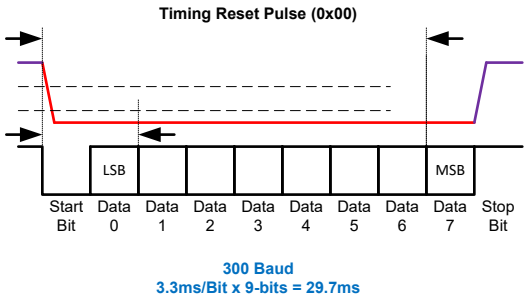


Figure 7-25. UART Driven SWIFT RESET Pulse

7.5.1.1.2 Standard Reset and Presence Pulse

When the Host driven Standard Reset is issued after initial power up or after a Timing Reset, the width of the pulse sets the range for SWIFT communication timing regime. The Presence Pulse response by the connected SWIFT devices confirms the presence of a client on the line and that the timing range has been accepted.

The Host driven Standard Reset and the SWIFT clients driven Presence Pulse response is transmitted and received in a single UART Tx/Rx byte at base Baud rate. The value received for the Standard Reset and Presence pulse can vary.

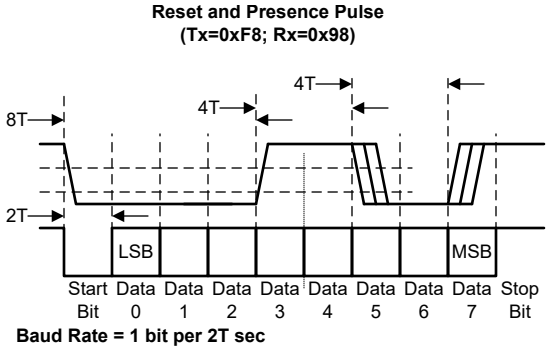


Figure 7-26. Standard Reset and Presence Pulse

7.5.1.1.3 Host Write 1/0

The Host Write 1/0 bit waveforms are generated by the Host Pulling the SWIFT line Low. The Host transmits logic 1s by holding the line Low for time T. The Host transmits logic 0s by holding the line Low for time 4T. Implementations using UARTs have a Baud setting that is one-half the Baud rate used for transmitting the Standard Reset Pulse. The same byte that is transmitted by the Host is also received by the Host UART.

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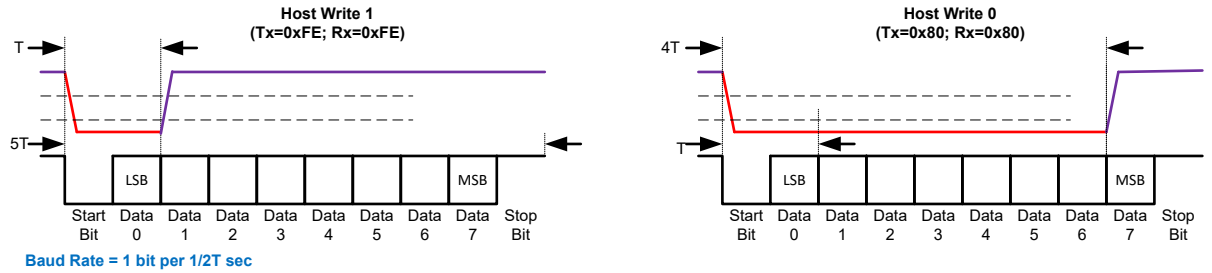


Figure 7-27. Host Write 1/0

7.5.1.1.4 Host Read 1/0

The Host Read 1/0 bit transfers are initiated by the Host by issuing a Read Pulse which is the minimum pulse of time T. The SWIFT device responds by allowing the line to return High to transmit a logic 1 or the SWIFT device responds by holding the line Low (after the Host has released it) for a total time of 4T. Implementations using UARTs have a Baud setting that are one-half the Baud rate used for transmitting the Standard Reset Pulse. For Host Read 1 transmissions, the same pulse that is transmitted by the Host is also received by the Host UART. The Host transmits 0xFE and ideally receives 0x80. Due to timing uncertainty inherent with asynchronous communication, the value received for the Standard Reset and Presence pulse can vary.

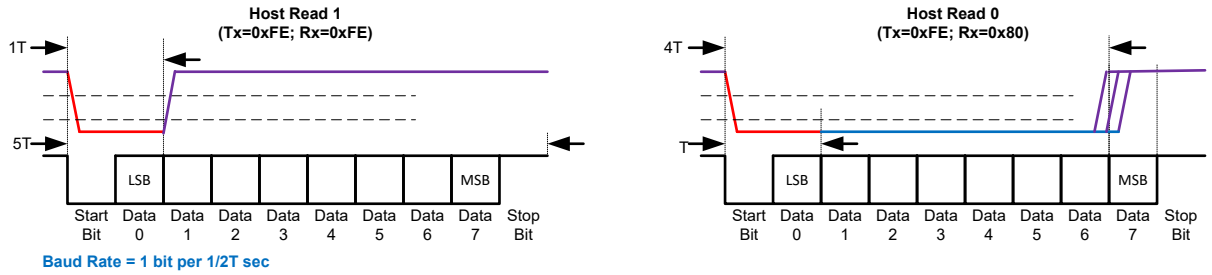


Figure 7-28. Host Read 1/0

7.5.1.1.5 Alternative UART Byte to SWIFT Bit Mapping

An alternative mapping of UART bytes to SWIFT bit communication enables 2-SWIFT bits to be transferred in a single UART byte. The mapping is illustrated in the figure below.

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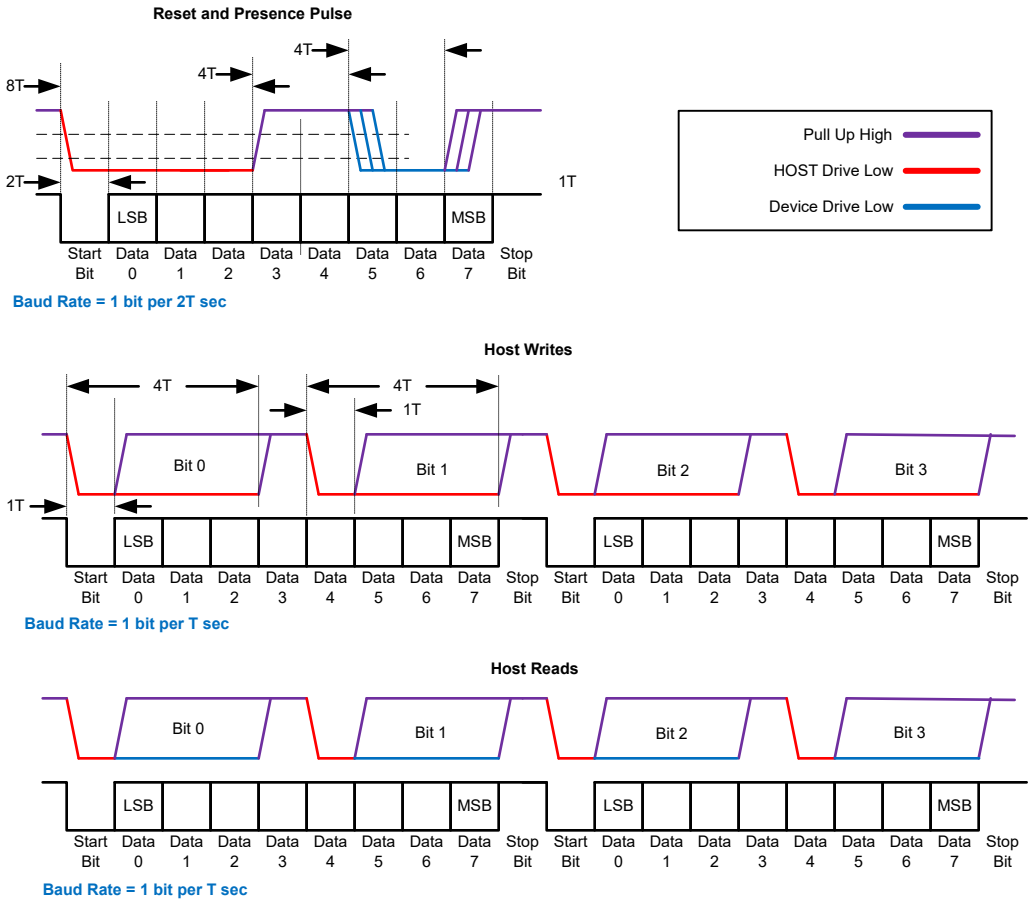


Figure 7-29. Two SWIFT Bits in a Single UART Byte

7.5.1.2 SWIFT Signaling

The SWIFT communication line is pulled up to the interface voltage source. All connected devices are open-drain. Consequently, the connected devices can only pull down the line and there is no electrical contention when multiple devices pull down the line.

The host initiates all SWIFT signaling. The Standard Reset pulse initiates all command sequences. All connected SWIFT clients respond with a Presence Pulse. The Presence Pulse confirms to the Host that there are one or more SWIFT devices connected to the line.

The SWIFT selection command following the Standard Reset Pulse and Presence Pulse contains the Synchronization Nibble (0x3).

7.5.1.3 SWIFT Command Sequences

All SWIFT command sequences are initiated with the Standard Reset and Presence pulse transactions. The Standard Reset can be initiated at any point to interrupt and reinitialize command sequences. Global or Selection Commands containing the Synchronization Nibble follow initialization of the command sequence.

Global Commands end a command sequence leaving no SWIFT device selected for further communication.

Completion of Selection Commands enable further communication with the selected SWIFT client. That communication can be response from the client with information such as its unique 48-bit SWIFT ID. More commonly further communication initiates a Functional Command to execute a Memory Function or Sensor Function.

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The SWIFT protocol supports single-drop and multi-drop applications. SWIFT commands that support multi-drop applications can also be used in single-drop applications. Two of the available Selection Commands are reserved for single-drop applications.

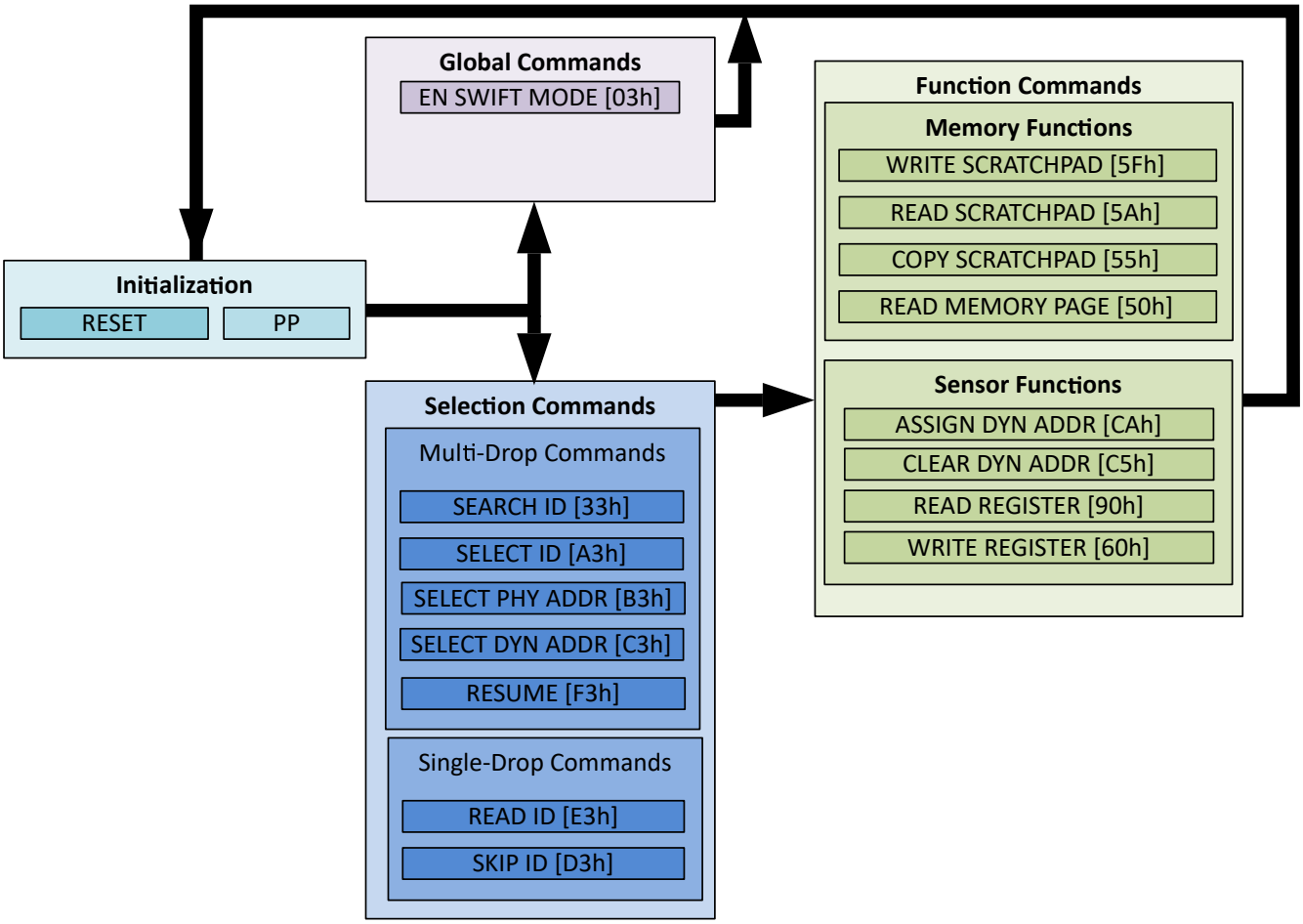


Figure 7-30. TMAG3101-Q1 SWIFT Command Sequences

In this section, the electrical signaling of the protocol is represented by named blocks as shown in the following figures.

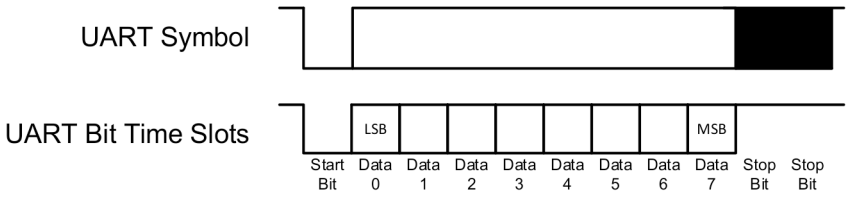


Figure 7-31. UART Symbol

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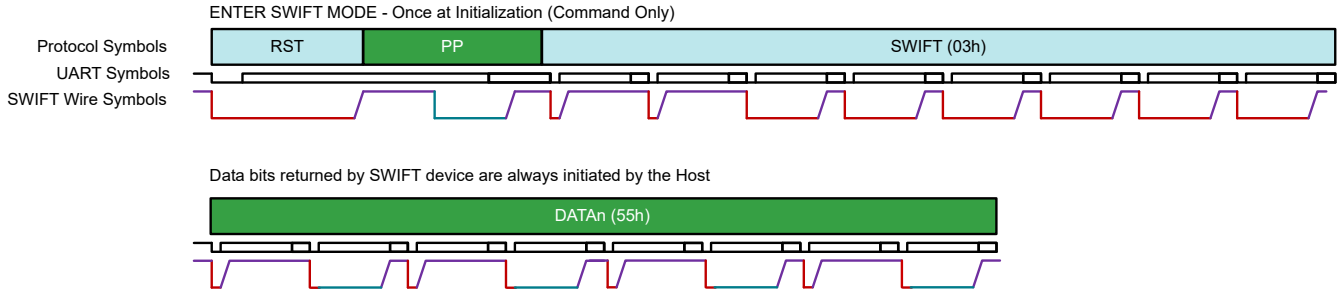


Figure 7-32. Example SWIFT Signaling

7.5.1.3.1 Global Commands

Global Commands follow the Standard Reset and Presence Pulse sequence. All connected SWIFT devices can implement all of the Global Commands. All connected SWIFT clients which can execute the Global Command do so.

7.5.1.3.1.1 Enable SWIFT Mode [0x03]

The Enable Swift Mode (ENSWIFT) command is required as the first command in a SWIFT communication session to be started after initial power up or after a transition into SWIFT communication from another device operating mode.



Figure 7-33. Enable SWIFT Mode

7.5.1.3.2 Selection Commands

Completion of the SWIFT Selection Commands results in a single connected SWIFT client being selected for a functional command sequence.

7.5.1.3.2.1 Single-Drop Commands

The SWIFT Single-Drop commands allow more efficient client selection for application when only one client is present in the application.

7.5.1.3.2.1.1 Read ID [0xE3]

The Read ID (RDID) command returns the 56-bit SWIFT ID and ECC8 from the client. After the SWIFT ID is delivered by the client, the client is selected for a subsequent function command sequence.

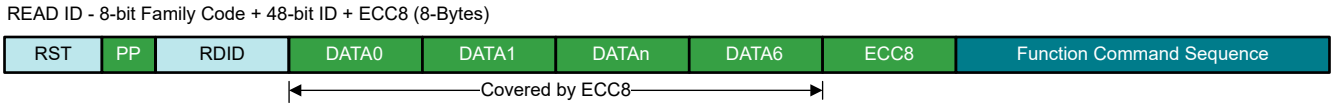


Figure 7-34. Read ID

7.5.1.3.2.1.2 Skip ID [0xD3]

The Skip ID (SKIPID) command selects the connected SWIFT client for a subsequent function command sequence.



Figure 7-35. Skip ID

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7.5.1.3.2.2 Multi-Drop Commands

The SWIFT Multi-Drop Commands enable enumeration of clients when the system configuration is dynamic or unknown to the Host. These commands provide a means of selecting clients with known SWIFT IDs or Physical IDs or with a dynamically assigned ID. Once a client is selected, the client can remain selected for execution of additional function commands by issuing the Resume Multi-drop command after a Standard Reset and Presence Pulse sequence.

7.5.1.3.2.2.1 Search Die ID [0x33]

Execution of the Search Die ID (SRCHID) command sequence enables the Host to enumerate the set of connected SWIFT clients by using the unique, 48-bit factory programmed SWIFT ID stored in each SWIFT client. After completion of the Search ID command, a single SWIFT client is enumerated and selected for execution of a functional command sequence.



Figure 7-36. Search ID

After the Search ID command code is issued by the Host, each bit of the 48-bit ID (plus 8-bit CRC) is determined for a single connected client with a sequence that includes three bit value transfers between the Host and the connected clients for each ID bit. The SWIFT ID for one connected client is determined with each Search ID command until the command sequence enumerates all connected clients. As each client is enumerated, the client is selected for a subsequent execution of a function command.

The following diagram provides an example of a system containing three devices with unknown SWIFT IDs. In this example, the SWIFT IDs are three bits (and not the standard 48-bits plus CRC). To determine the bit values that exist for the value of the least significant bit (lsb) of the SWIFT ID (bit[0]), the Host issues two Read Slot pulses and the connected devices respond with the Read values of the lsb (bit[0]) and the complement (cbit[0]). Since all three devices have Zero as the value of bit[0], the Host makes the Bit0 Decision when the host sees no contention for the bit[0] value. The Host issues a Write Zero to confirm that the host intends to proceed enumeration with all clients with bit[0]=0.

The Host proceeds by issuing two Read Slots prior to the Bit1 Decision. In that round, contention for the value of bit[1] ID detected. That informs the Host that there are at least two connected clients. The Host must then choose which branch to interrogate and must remember that the other branch must be integrated in a future Search ID session. In this example, the Host chooses to acknowledge with a Write 0 (b.). When, the Host acknowledges bit[1]=0, all devices with bit[1]=1 must not respond to Read Slots until a Standard Reset is issued. This behavior removes those clients from completion for enumeration in the current Search ID session.

The Host proceeds by issuing two Read Slots prior to the Bit2 Decision. In that round, contention for the value of bit[2] id detected. That informs the Host that there are at least three connected clients. The Host must then choose which branch to interrogate and must remember that the other branch must be integrated in another Search ID session. In this example, the Host chooses to acknowledge with a Write 0 (c.). When, the Host acknowledges bit[2]=0, the client with ID 000b has been selected for subsequent functional command execution.

To compete enumeration of connected clients, the Host issues a Standard Reset and Presence Pulse sequence ahead of again issuing the Search ID command. In the example below, the sequence of choices the Host makes to enumerate the client with ID 110b is shown to be Bit0 Choice is 0 (a.). Bit1 Choice is 1 (d.). Bit2 Choice is 1 (e.).

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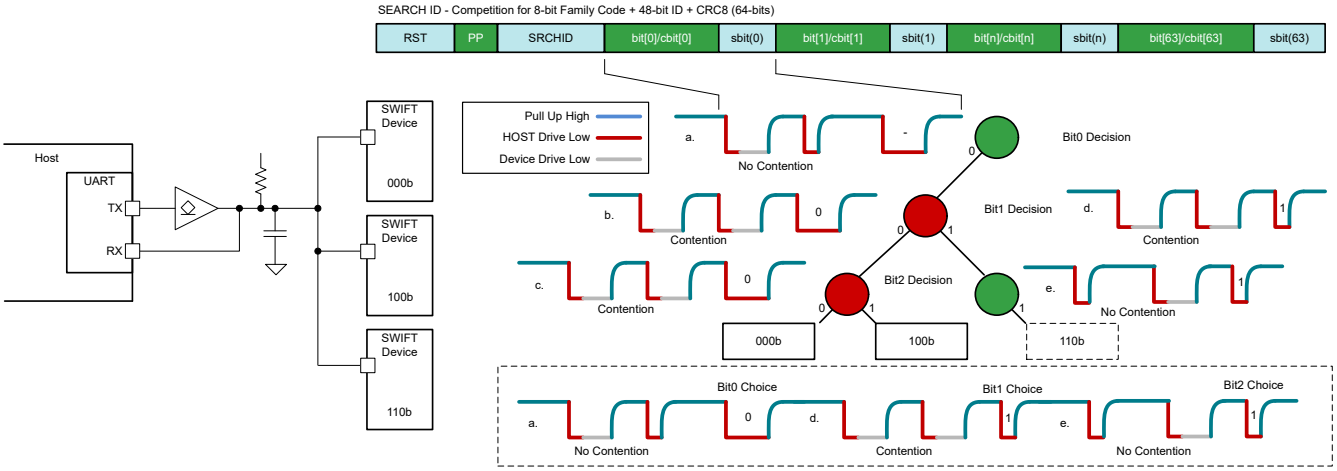


Figure 7-37. Search ID Example

7.5.1.3.2.2.2 Select SWIFT ID [0xA3]

The Select ID (SELSID) command is issued to select a client by the 48-bit (plus 8-bit CRC) SWIFT ID that is known to the Host. The SWIFT ID can be determined by the Search ID or Read ID commands.

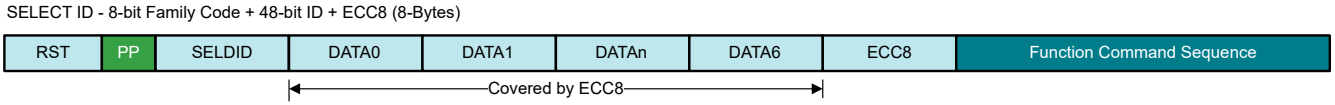


Figure 7-38. Select SWIFT ID

7.5.1.3.2.2.3 Select Physical ID [0xB3]

The Select Physical ID (SELPID) is used for clients which have pin-strapping available which identify the physical location of the client with the end equipment. The Physical ID is 4-bits. The Select Physical IC command requires the Physical ID and the complement to follow the command.



Figure 7-39. Select Physical ID

7.5.1.3.2.2.4 Select Dynamic ID [0xC3]

The Select Dynamic ID (SELDID) command selects a client which as been assigned a 4-bit Dynamic Device ID (DynID) by execution of the Assign Dynamic ID command.

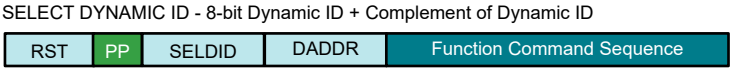


Figure 7-40. Select Dynamic ID

7.5.1.3.2.2.5 Resume [0xF3]

The Resume (RESUME) Command is issued to keep a previously selected client selected for execution of a functional command sequence.



Figure 7-41. Resume

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7.5.1.3.3 Function Commands

Functional commands execute operations that alter the NVM of the client or enable Read/Write access the client specific hardware registers.

7.5.1.3.3.1 Memory Function Commands

7.5.1.3.3.1.1 Write Scratch Pad [0x5F]

The Write Scratch Pad (WRSP64) command loads the Scratch Pad Registers with the address and data of 64-bits of data to be programmed into the on-chip NVM of the client. The Scratch Pad CRC (SP_CRC8) covers the command code as well as the address and data values of the transaction. The SP_CRC8 is subsequently used as the value used to confirm execution of NVM programming with the Copy Scratch Pad command.

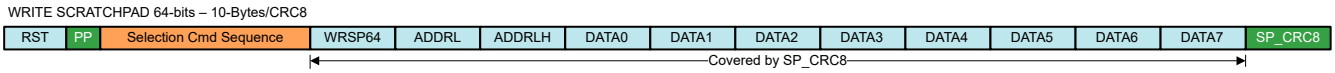


Figure 7-42. Write Scratch Pad

7.5.1.3.3.1.2 Read Scratch Pad [0x5A]

The Read Scratch Pad (RDSP64) command returns the contents of the address and data stored in the Scratch Pad Register. The CRC8 returned covers the command and transmitted data. The CRC8 with is returned is not the SP_CRC8 that is stored with the Scratch Pad address and data.

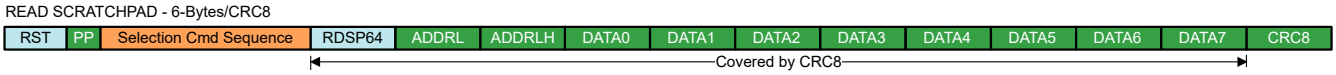


Figure 7-43. Read Scratch Pad

7.5.1.3.3.1.3 Copy Scratch Pad [0x55]

The Copy Scratch Pad (CPYSP) command accompanied with the SP_CRC8 value, initiates the programming steps required for the on-chip NVM of the client.

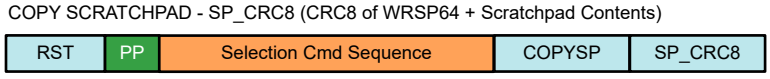


Figure 7-44. Copy Scratch Pad

7.5.1.3.3.1.4 Read Memory Page [0x50]

The Read Memory Page (RDPAGE) command return the contents of the selected NVM address. A CRC8 for the command and requested address is returned by the client to confirm the proper command and address are being used. CRC8 bytes are returned by the client at the end of transmission of each set of 33-bytes. The Host can continue to read NVM data after the first page while the client continues to increment the internal address. At the end of the internal NVM address, the internal address of the client wraps around and continues providing new data.



Figure 7-45. Read Memory Page

7.5.1.3.3.2 Sensor Function Commands

The Sensor Function commands provide Read/Write access to client specific hardware register resources. This set of commands includes management of the dynamically assigned SWIFT addresses.

7.5.1.3.3.2.1 Assign Dynamic ID [0xCA]

The Assign Dynamic ID (ASSA8) is used to reduce the overhead of addressing devices with known SWIFT IDs. For systems with unknown connected clients, after completion of each round of Search ID commands, the

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selected client can be assigned a Dynamic Address. In future transactions the Dynamic Address can be used to address that client instead of the 48-bit (plus 8-bit CRC).

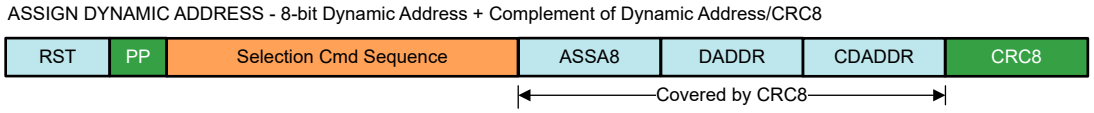


Figure 7-46. Assign Dynamic ID

7.5.1.3.3.2.2 Clear Dynamic ID [0xC5]

The Clear Dynamic ID (CLRAA) command is provided to allow re-assignment of Dynamic ID for cases when disturbance of the SWIFT communication has led to uncertainty of the Dynamic ID assignments.

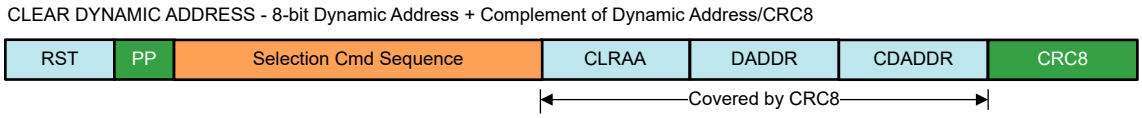


Figure 7-47. Clear Dynamic ID

7.5.1.3.3.2.3 Read 32-bit Register [0x90]

The Read 32-bit Register (RDREG32) command provides read access to the client specific hardware registers in 32-bit segments. The first CRC8 of the response covers the command address and first 32-bits of data. If the Host continues to Read hardware register data, the subsequent sets of 32-bit data are covered by a CRC8 byte.

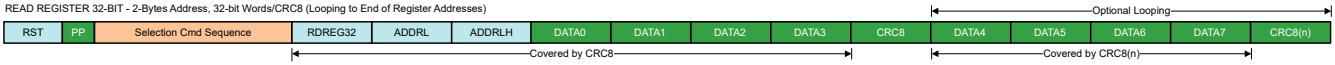


Figure 7-48. Read 32-bit Register

7.5.1.3.3.2.4 Write 32-bit Register [0x60]

The Write 32-bit Register (WRREG32) command sequence provides address and data values to be written in to the client specific hardware registers. The client responds with a CRC8 that covers the command address and data of the first 32-bit write transaction. Subsequent transmission of 32-bits causes the internal address to increment followed by the return of a CRC8 which covers those 32-bits of data.

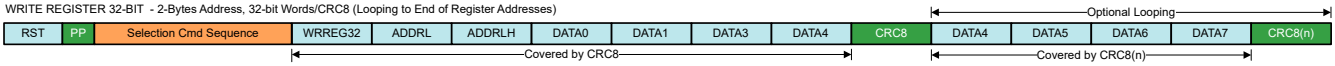


Figure 7-49. Write 32-bit Register

7.5.1.4 Entering SWIFT Mode Through Operating Modes

After the TMAG3101-Q1 has been programmed into the desired operating mode using the OPERATING_MODE bit, re-entering the SWIFT programming mode is possible using an external trigger from the host. This allows the user to read or write EEPROM or User Registers depending on the state of the LOCKOUT bitfield. When LOCKOUT = Eh, the interrupt pulses and the ability to re-enter SWIFT programming mode is fully disabled.

To re-enter SWIFT programming mode when in a SENT or Triggered SENT operating mode (OPERATING_MODE = 1h through 4h) or PWM operating mode (OPERATING_MODE = 7h):

1. At any time after POR, create the interrupt pulse condition by driving the OUT pin low for a minimum of 300 ticks (SENT) or minimum of 3 full PWM cycles (PWM), then release the line or drive the line high. The line must be pulled high at least once after power-up to detect the interrupt pulse.
   a. The interrupt pulse can trigger the OUT overcurrent detection of the device. In this case, the OUT pin is still monitored for a valid interrupt pulse. If a valid interrupt pulse is not detected, a power cycle is required for recovery.
2. If a valid interrupt pulse is detected, the output is now disabled and a 5ms timer starts

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3. Write the complete enable SWIFT command (03h) before the 5ms timeout expires
4. If the command is incorrect or aborted, the device re-enters SENT, Triggered SENT, or PWM operating mode
5. If the command is correct, the device remains in SWIFT mode until a power cycle or until writing CDh to the SWIFT_CPU_MAILBOX bitfield

To re-enter SWIFT programming when in Analog operating mode (OPERATING_MODE = 6h)

1. After POR and device registers have been loaded, there is a 40ms timer to enter SWIFT mode. If this timer expires before fully unlocking the device, the device enters analog mode and the only way to try to enter SWIFT mode again is through a POR event.
2. Write the complete enable SWIFT command (03h) before the 40ms timer expires.
3. If the command is wrong or aborted, the device enters Analog output mode.
4. If the command is correct, the output is disabled and the device remains in SWIFT mode until a power cycle or until writing CDh to the SWIFT_CPU_MAILBOX bitfield.

7.5.1.5 Register Lockout Modes

The LOCKOUT[3:0] bitfield is used to enable different levels of programming lockout modes for the device. Once the LOCKOUT bitfield is programmed and the device is reset or power cycled, the LOCKOUT bitfield is permanently set.

- When LOCKOUT[3:0] = 0h, no lockout is enabled.
- When LOCKOUT[3:0] = 7h, all EEPROM programming via SWIFT is locked. SWIFT writes to the User Registers and SWIFT reads of EEPROM and User Registers are enabled.
- When LOCKOUT[3:0] = Bh, all SWIFT writes to the complete memory map (EEPROM and User Registers), except the SWIFT_CPU_MAILBOX, are locked. SWIFT reads of EEPROM and User Registers are enabled.
- When LOCKOUT[3:0] = Dh, all SWIFT reads and writes to the complete memory map (EEPROM and User Registers), except the SWIFT_CPU_MAILBOX are locked. The SWIFT Read ID command can still be used to read the device ID.
- When LOCKOUT[3:0] = Eh, SWIFT access is completely locked. Only device functional mode is available (SENT, Triggered SENT, PWM, Analog). Re-entering SWIFT mode is disabled and the device does not respond to interrupt pulses from the host.

7.5.2 Data Definition

7.5.2.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in the X_CH_RESULT, Y_CH_RESULT, and Z_CH_RESULT registers, respectively. The ADC output is stored in 16-bit result registers in 2's complement format. To calculate magnetic field in mT, use Equation 21 for 16-bit SENT data or when reading the X/Y/Z_CH_RESULT registers using SWIFT.

$$B = \frac{x_CH_RESULT}{SENS} \quad (21)$$

where

- B is magnetic field in mT
- x_CH_RESULT is the magnetic channel result in 16-bit 2's complement format
- SENS is the sensitivity in LSB/mT from the magnetic characteristics table

In analog output mode, calculate the magnetic output data output before any signal path corrections using Equation 22.

$$B = \frac{V_{OUT} - V_Q}{0.8 \times V_{CC}} \times \frac{2^{16}}{SENS} \quad (22)$$

where:

- B is magnetic field in mT
- V_{OUT} is the measured voltage on the OUT pin

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- V_Q is V_{CC} / 2
- SENS is the sensitivity in LSB/mT from the magnetic characteristics table

In PWM output mode, calculate the magnetic output data before any signal path corrections using Equation 23.

$$B = \frac{D_{OUT} - D_Q}{D_L} \times \frac{2^{16}}{SENS} \quad (23)$$

where:

- B is magnetic field in mT
- D_{OUT} is the % duty cycle measured on the output
- D_Q is 50%
- D_L is the linear duty cycle range; 90% when PWM_DC_SEL = 0h and 80% when PWM_DC_SEL = 1h
- SENS is the sensitivity in LSB/mT from the magnetic characteristics table

7.5.2.2 Temperature Sensor Data

The TMAG3101-Q1 temperature sensor measures temperature from –40°C to 170°C. Temperature data is stored in the TEMP_RESULT register in signed 16-bit two's complement Q9p7 format. The temperature data can be output in 16-bit format in SWIFT mode, or in 16-bit, 12-bit, or 8-bit format in SENT operating mode. The table below shows example temperature data out for TEMP_RESULT[15:0].

Table 7-24. 16-bit Temperature data format

Temperature (°C)	TEMP_RESULT[15:0]	
	BINARY	HEX
-40	1110 1100 0000 0000	EC00h
-25	1111 0011 1000 0000	F380h
-0.0078125	1111 1111 1111 1111	FFFFh
0	0000 0000 0000 0000	0000h
0.0078125	0000 0000 0000 0001	0001h
25	0000 1100 1000 0000	0C80h
125	0011 1110 1000 0000	3E80h
150	0100 1011 0000 0000	4B00h
170	0101 0101 0000 0000	5500h

7.5.2.3 Angle and Magnitude Data Definition

The TMAG3101-Q1 enables angle calculations based off the ANGLE_EN register bit settings. The angle output is stored in 16-bit result registers in unsigned format. To calculate angle in degree use Equation 24 for 16-bit SENT frame data and Equation 25 for 12-bit SENT frame data. If Alpha and Beta angle calculation is enabled, the Beta angle result is stored in MAGNITUDE_BETA.

$$A = ANGLE_ALPHA \times \left(\frac{360}{2^{16}}\right) \quad (24)$$

$$A = ANGLE_ALPHA \times \left(\frac{360}{2^{12}}\right) \quad (25)$$

where

- A is the angle in degrees

In analog output mode, calculate the angle output data before any signal path corrections using Equation 26.

$$A = \frac{V_{OUT} - V_Q}{0.8 \times V_{CC}} \times 360 \quad (26)$$

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where:

- A is the angle in degrees
- V_{OUT} is the measured voltage on the OUT pin
- V_Q is 0.1×V_{CC}

In PWM output mode, calculate the angle output data before any signal path corrections using Equation 27.

$$A = \frac{D_{OUT} - D_Q}{D_L} \times 360 \quad (27)$$

where:

- A is the angle in degrees
- D_{OUT} is the measured duty cycle on the OUT pin
- D_Q is 5% when PWM_DC_SEL = 0h and 10% when PWM_DC_SEL = 1h
- D_L is the linear duty cycle range; 90% when PWM_DC_SEL = 0h and 80% when PWM_DC_SEL = 1h

During the angle calculation, use Equation 28 to calculate the resultant vector magnitude.

$$\mathrm{M} = \sqrt{\mathrm{MADC_{Ch1}}^2 + \mathrm{MADC_{Ch2}}^2} \quad (28)$$

where

- $\mathrm{MADC_{Ch1}}$, $\mathrm{MADC_{Ch2}}$ are the ADC codes of the two magnetic channels selected for the angle calculation.

The magnitude data can be accessed as 16-bit or 12-bit format. To calculate magnitude in mT use Equation 29 for 16-bit SENT data and Equation 30 for 12-bit SENT data.

$$\mathrm{M} = \frac{\sum_{i=0}^{15} \mathrm{D}_i \times 2^i}{2^{16}} \times 2|\mathrm{B_R}| \quad (29)$$

$$\mathrm{M} = \frac{\sum_{i=0}^{11} \mathrm{D}_i \times 2^i}{2^{12}} \times 2|\mathrm{B_R}| \quad (30)$$

where

- M is magnitude data in mT.
- D_i is the data bit
- B_R is the magnetic range in mT for the corresponding channel.

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8 Register Map

8.1 TMAG3101-Q1 Registers

Table 8-1. TMAG3101-Q1 Registers

Offset	Acronym	Register Name	Section
0h	EEPROM_CONFIG0	Magnetic sensor, operating mode, device output, SENT fast and slow serial channel configurations	Section 8.1.1
8h	EEPROM_CONFIG1	SENT fast channel, diagnostics, and output slew rate settings	Section 8.1.2
10h	EEPROM_CONFIG2	Triggered SENT config and X and Y channel offset	Section 8.1.3
18h	EEPROM_CONFIG3	X gain, angle, Z, and Y offset	Section 8.1.4
20h	EEPROM_CONFIG4	Z gain, Y gain, and phase correction	Section 8.1.5
28h	EEPROM_CONFIG5	Phase correction, 2D angle thresholds, temperature threshold	Section 8.1.6
30h	EEPROM_CONFIG6	Temperature, X, and Y thresholds	Section 8.1.7
38h	EEPROM_CONFIG7	Y and Z thresholds	Section 8.1.8
40h	EEPROM_CONFIG8	Magnitude and linearization config	Section 8.1.9
48h	EEPROM_CONFIG9	Linearization coefficients	Section 8.1.10
50h	EEPROM_CONFIG10	Linearization coefficients	Section 8.1.11
58h	EEPROM_CONFIG11	Linearization coefficients	Section 8.1.12
60h	EEPROM_CONFIG12	Linearization coefficients	Section 8.1.13
68h	EEPROM_CONFIG13	Linearization coefficients	Section 8.1.14
70h	EEPROM_CONFIG14	Linearization coefficients	Section 8.1.15
78h	EEPROM_CONFIG15	Linearization coefficients	Section 8.1.16
80h	EEPROM_CONFIG16	Linearization coefficients	Section 8.1.17
88h	EEPROM_CONFIG17	Linearization coefficients	Section 8.1.18
90h	EEPROM_CONFIG18	Linearization coefficients, SENT protocol revision and fast channel characteristics	Section 8.1.19
98h	EEPROM_CONFIG19	SENT fast channel characteristics and OEM codes	Section 8.1.20
A0h	EEPROM_CONFIG20	OEM codes	Section 8.1.21
A8h	EEPROM_CONFIG21	OEM codes	Section 8.1.22
B0h	EEPROM_CONFIG22	Manufacturer code, sensor type, and device lockout bits	Section 8.1.23
200h	USER_REG0	Status register	Section 8.1.24
204h	USER_REG1	X and Y results	Section 8.1.25
208h	USER_REG2	Z and temperature results	Section 8.1.26
20Ch	USER_REG3	Angle and magnitude results	Section 8.1.27
210h	USER_REG4	Swift CPU mailbox and device version	Section 8.1.28
214h	USER_REG5	ADC result and sequence count	Section 8.1.29
218h	USER_REG6	Sensor configuration and diagnostics and AFE control	Section 8.1.30
21Ch	USER_REG7	Reserved	Section 8.1.31

8.1.1 EEPROM_CONFG0 Register (Offset = 0h) [Reset = 0000000000000000h]

Figure 8-1. EEPROM_CONFG0 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32

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Figure 8-1. EEPROM_CONFG0 Register Field Descriptions (continued)

ECC0	DATA_SEL[2:0]	SENT_SLOW_CH[1:0]	SENT_RES	SENT_MULT	T_FAST	DAT1_MSN	DAT2_REV	ROLLC	MULT_DCC	S_T_EN	S_ERR_EN	S_TYPE	S_MAN	S_PROT	S_CHAR	S_ID	S_OEM	TRIGMODE	S_REPEAT[1:0]	RESERVED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEMPCO_SEL[3:0]				RESERVED	PWM_FREQ_SEL[2:0]			PWM_DC_SEL	A_PWM_OUT_SCALE	ANGLE_POL[2:0]			Z_POL	Y_POL	X_POL	OPERATING_MODE[2:0]			ANGLE_EN[2:0]			DIAG_EN[1:0]		FILTER_SEL[3:0]				MAG_CH_EN[3:0]			

Table 8-2. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC0	R	00h	ECC
55-53	DATA_SEL[2:0]	R/W	0h	Enables the type of position data to be transmitted via the OUT pin 0h = 2D angle for SENT/PWM/Analog 1h = X-axis data for SENT/PWM/Analog 2h = Y-axis data for SENT/PWM/Analog 3h = Z-axis data for SENT/PWM/Analog 4h = 2D angle and magnitude data for SENT only 5h = ALPHA and BETA angle data for SENT only 6h = X, Y, Z data for SENT only (Fast channel multiplexing must be enabled) 7h = Reserved
52-51	SENT_SLOW_CH[1:0]	R/W	0h	Enables SENT slow-serial channel communication via the status nibble 0h = Serial message disabled 1h = Short serial message enabled 2h = Enhanced 12-bit serial message enabled 3h = Enhanced 16-bit serial message enabled
50	SENT_RES	R/W	0h	Selects the resolution of SENT data 0h = 12-bit SENT data 1h = 16-bit SENT data
49	SENT_MULT	R/W	0h	Enables SENT fast channel multiplexing for X, Y, Z and temperature data 0h = Fast channel multiplexing disabled 1h = fast channel multiplexing enabled
48	T_FAST	R/W	0h	Enabled temperature data through the fast SENT channel 0h = No temperature data through the SENT fast channel 1h = Temperature data through SENT fast channel. 12-bit temperature when SENT_RES = 0h, 8-bit temperature when SENT_RES = 1h

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Table 8-2. Register Field Description (continued)

Bit	Field	Type	Reset	Description
47	DAT1_MSN	R/W	0h	Enables SENT transmission of inverted data 1 MSN in fast channel for enhanced data integrity 0h = Inverted data 1 MSN transmission disabled 1h = Inverted data 1 MSN transmission enabled
46	DAT2_REV	R/W	0h	Enables reversal of SENT data 2 nibble order in fast channel 0h = SENT data 2 nibble order MSN to LSN 1h = SENT data 2 nibble order LSN to MSN
45	ROLLC	R/W	0h	Enables SENT 8-bit rolling counter through fast channel0h = SENT rolling counter disabled1h = SENT rolling counter enabled
44	MULT_DCC	R/W	0h	Enables data consistency counter (DCC) during SENT fast channel multiplexing. The DCC nibble is defined as a rolling counter and is incremented with each recurrence of the frame control sequence. 0h = DCC disabled 1h = DCC enabled
43	S_T_EN	R/W	0h	Enables temperature data through SENT slow serial channel 0h = No temperature data through SENT slow serial channel 1h = Enable temperature data through SENT slow serial channel
42	S_ERR_EN	R/W	0h	Enables error communication through SENT slow serial channel 0h = No error data through SENT slow serial channel 1h = Enable error data through SENT slow serial channel
41	S_TYPE	R/W	0h	Enables sensor type communication through SENT slow serial channel 0h = No sensor type communication through SENT slow serial channel 1h = Enable sensor type data through SENT slow serial channel
40	S_MAN	R/W	0h	Enables TI manufacturer code through SENT slow serial channel 0h = Disable TI manufacturer code through SENT slow serial channel 1h = Enable TI manufacturer code through SENT slow serial channel
39	S_PROT	R/W	0h	Enables SENT protocol revision through SENT slow serial channel 0h = Disable SENT protocol revision through SENT slow serial channel 1h = Enable SENT protocol revision through SENT slow serial channel
38	S_CHAR	R/W	0h	Enables SENT fast channel 1 characteristic through SENT slow serial channel 0h = Disable fast channel 1 characteristic through SENT slow serial channel 1h = Enable fast channel 1 characteristic through SENT slow serial channel
37	S_ID	R/W	0h	Enables sensor ID through SENT slow serial channel 0h = Disable sensor ID through SENT slow serial channel 1h = Enable sensor ID through SENT slow serial channel

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Table 8-2. Register Field Description (continued)

Bit	Field	Type	Reset	Description
36	S_OEM	R/W	0h	Enables ASCII character OEM codes through SENT slow serial channel 0h = Disable OEM codes through SENT slow serial channel 1h = Enable OEM codes through SENT slow serial channel
35	TRIGMODE	R/W	0h	Selects the SENT trigger mode 0h = Triggered SENT with falling edge to falling edge addressing (FEFE trigger) 1h = Triggered SENT with falling edge to rising edge addressing (FERE trigger)
34-33	S_REPEAT[1:0]	R/W	0h	Enables repeating specific channels in the SENT slow serial communication. Valid only for SENT_SLOW_CH = 2h. Ensure S_ERR_EN and S_T_EN are appropriately set. 0h = No repeat in SENT slow serial channel 1h = Enable error communication ($01) to repeat between any other message in the format message-error-message-error-message-error and repeat 2h = Enable temperature data ($23) to repeat between any other message in the format message-temperature-message-temperature-message-temperature and repeat 3h = Enable both error communication and temperature data ($01 and $23) to repeat between any other message in the format message-error-temperature-message-error-temperature and repeat
32	RESERVED	R	0h	Reserved
31-28	TEMPCO_SEL[3:0]	R/W	2h	Temperature coefficient of external magnet 0h = -0.02%/°C 1h = -0.01%/°C 2h = 0.00%/°C (No tempco selected) 3h = 0.01%/°C 4h = 0.03%/°C 5h = 0.04%/°C (SmCo) 6h = 0.05%/°C 7h = 0.11%/°C 8h = 0.12%/°C (NdBFe) 9h = 0.13%/°C Ah = 0.19%/°C Bh = 0.20%/°C (Ceramic) Ch = 0.21%/°C Dh = Reserved Eh = Reserved Fh = Reserved
27	RESERVED	R	0h	Reserved

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Table 8-2. Register Field Description (continued)

Bit	Field	Type	Reset	Description
26-24	PWM_FREQ_SEL[2:0]	R/W	0h	Selects the typical PWM frequency. 0h = 100Hz 1h = 150Hz 2h = 205Hz 3h = 244Hz 4h = 488Hz 5h = 781Hz 6h = 1302Hz 7h = 1953Hz
23	PWM_DC_SEL	R/W	0h	Selects the PWM full scale duty cycle range 0h = PWM full scale duty cycle from 5% to 95% 1h = PWM full scale duty cycle from 10% to 90%
22	A_PWM_OUT_SCALE	R/W	0h	Enables the scaling of the Analog or PWM OUT full range according to x_THRESHOLD_VALUE entry for the particular data type 0h = Scaling of the Analog or PWM output is disabled 1h = Scaling of the Analog or PWM output is enabled
21-19	ANGLE_POL[2:0]	R/W	0h	Changes the CORDIC angle output polarity. This effectively reverses the rotation direction. 0h = Default result 1h = Reverses the polarity of the 2D angle 2h = Reverses the polarity of ALPHA angle only 3h = Reverses the polarity of BETA angle only 4h = Reverses the polarity of ALPHA and BETA angle 5h = Reserved 6h = Reserved 7h = Reserved
18	Z_POL	R/W	0h	Selects the polarity of the Z magnetic field 0h = Default result 1h = Reverses the polarity of the Z magnetic field
17	Y_POL	R/W	1h	Selects the polarity of the Y magnetic field 0h = Reverses the polarity of the Y magnetic field 1h = Default result
16	X_POL	R/W	0h	Selects the polarity of the X magnetic field 0h = Default result 1h = Reverses the polarity of the X magnetic field

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Table 8-2. Register Field Description (continued)

Bit	Field	Type	Reset	Description
15-13	OPERATING_MODE[2:0]	R/W	0h	Selects the device operating mode 0h = SWIFT mode 1h = Synchronous TI Triggered SENT mode (Triggered Conversions) 2h = Synchronous SENT Mode (SENT Frames and Conversions are Synchronized) 3h = Asynchronous TI Triggered SENT mode (Continuous Conversions) 4h = Asynchronous SENT mode (Continuous Conversions) 5h = Reserved 6h = Analog Continuous Conversion mode 7h = PWM Continuous Conversion mode
12-10	ANGLE_EN[2:0]	R/W	0h	Enable angle calculation 0h = XY angle calculation enabled 1h = YX angle calculation enabled 2h = XZ angle calculation enabled 3h = ZX angle calculation enabled 4h = ZY angle calculation enabled 5h = YZ angle calculation enabled 6h = 2D ALPHA BETA angle calculation enabled 7h = 3D ALPHA BETA angle calculation enabled
9-8	DIAG_EN[1:0]	R/W	0h	Enables diagnostic selection 0h = Turn off all diagnostics (default) 1h = Turn on all diagnostics 2h = Turn on only active channel diagnostics 3h = reserved

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Table 8-2. Register Field Description (continued)

Bit	Field	Type	Reset	Description
7-4	FILTER_SEL[3:0]	R/W	0h	Enables conversion filter settings to optimize speed versus noise performance 0h = 45kHz, 263us (3 axes), 180us (2 axes), 97us (1 axis) 1h = 22.5kHz, 266us (3 axes), 182us (2 axes), 98us (1 axis) 2h = 11.25kHz, 272us (3 axes), 186us (2 axes), 100us (1 axis) 3h = 5.625kHz, 284us (3 axes), 194us (2 axes), 104us (1 axis) 4h = 2.8125kHz, 308us (3 axes), 210us (2 axes), 112us (1 axis) 5h = 1.4kHz, 356us (3 axes), 242us (2 axes), 128us (1 axis) 6h = 700Hz, 452us (3 axes), 306us (2 axes), 160us (1 axis) 7h = 350Hz, 644us (3 axes), 434us (2 axes), 224us (1 axis) 8h = 175Hz, 1.028ms (3 axes), 690us (2 axes), 352us (1 axis) 9h = 87Hz, 1.796ms (3 axes), 1.202ms (2 axes), 608us (1 axis) Ah = 44Hz, 3.332ms (3 axes), 2.226ms (2 axes), 1.120ms (1 axis) Bh = 22Hz, 6.404ms (3 axes), 4.274ms (2 axes), 2.144ms (1 axis) Ch = 11Hz, 12.548ms (3 axes), 8.370ms (2 axes), 4.192ms (1 axis) Dh = 5.5Hz, 24.836ms (3 axes), 16.562ms (2 axes), 8.288ms (1 axis) Eh = 2.75Hz, 49.412ms (3 axes), 32.946ms (2 axes), 16.480ms (1 axis) Fh = 1.4Hz, 98.564ms (3 axes), 65.714ms (2 axes), 32.864ms (1 axis)
3-0	MAG_CH_EN[3:0]	R/W	0h	Enables data acquisition of the magnetic axis channels 0h = All magnetic channels disabled (default) 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channel enabled 4h = Z channel enabled 5h = Z, X channel enabled 6h = Y, Z channel enabled 7h = X, Y, Z channel enabled 8h = X, Y, X channel enabled 9h = Y, X, Y channel enabled Ah = Y, Z, Y channel enabled Bh = Z, Y, Z channel enabled Ch = Z, X, Z channel enabled Dh = X, Z, X channel enabled Eh = X, Y, Z, Y, X channel enabled Fh = X, Y, Z, Z, Y, X channel enabled

8.1.2 EEPROM_CONFG1 Register (Offset = 8h) [Reset = 0000000000000000h]

Figure 8-2. EEPROM_CONFG1 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32

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Figure 8-2. EEPROM_CONFG1 Register Field Descriptions (continued)

ECC1	FEC[7:0]	FLP[7:0]	FLC[1:0]	RESERVED	TICK_SEL[3:0]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOAD_SEL[2:0]			RISE_SLEW[2:0]			FALL_SLEW[2:0]		BUF_SEL	RESERVED	UV_SEL	OV_SEL	RESERVED			A_HLT_EN	M_HLT_EN	T_HLT_EN	X_HLT_EN	Y_HLT_EN	Z_HLT_EN	HYST_SEL[2:0]			HYST_VALUE[7:0]						

Table 8-3. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC1	R	00h	ECC
55-48	FEC[7:0]	R/W	00h	Number of 32MHz clock cycles for the Host driven SENT Trigger falling edge. Used to adjust the SENT Sync pulse low time duration after the FEFE SENT trigger
47-40	FLP[7:0]	R/W	00h	Adds delay to the SENT frame when additional frame length padding is enabled (FLC = 3h). The additional delay is calculated as FLP × tick time × 4
39-38	FLC[1:0]	R/W	0h	SENT frame length control 0h = No pause pulse enabled 1h = Pause pulse enabled 2h = Pause pulse enabled with constant frame length 3h = Pause pulse enabled with constant frame length and additional frame length padding (FLP)
37-36	RESERVED	R	0h	Reserved
35-32	TICK_SEL[3:0]	R/W	0h	Selects the SENT tick time 0h = 0.25µs 1h = 0.5µs 2h = 1.0µs 3h = 2.0µs 4h = 3.0µs 5h = 5.0µs 6h = 6.0µs 7h = 12.0µs 8h = reserved 9h = reserved Ah = reserved Bh = reserved Ch = reserved Dh = reserved Eh = reserved Fh = reserved

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Table 8-3. Register Field Description (continued)

Bit	Field	Type	Reset	Description
31-30	LOAD_SEL[1:0]	R/W	0h	Selects the drive strength of the analog output depending on the capacitive load. 0h = Up to 20nF load on OUT 1h = 20nF to 50nF load on OUT 2h = 50nF to 100nF load on OUT 3h = 100nF to 330nF load on OUT
29-27	RISE_SLEW[2:0]	R/W	0h	Selects the OUT pin rise slew rate for SENT/PWM output modes when in push-pull mode 0h = 0.3µs 1h = 0.45µs 2h = 0.6µs 3h = 0.75µs 4h = 1.3µs 5h = 2.1µs 6h = 7.0µs 7h = 11.0µs
26-24	FALL_SLEW[2:0]	R/W	0h	Selects the OUT pin fall slew rate for SENT/PWM/SWIFT output modes. Fall time for open drain and push-pull modes. 0h = 0.3µs 1h = 0.45µs 2h = 0.6µs 3h = 0.75µs 4h = 1.3µs 5h = 2.1µs 6h = 3.5µs 7h = 5.5µs
23	BUF_SEL	R/W	0h	Selects the OUT buffer type for SENT and PWM modes 0h = open drain mode 1h = push-pull mode
22	RESERVED	R	0h	Reserved
21	UV_SEL	R/W	0h	Selects the under voltage threshold on Vcc 0h = Under voltage threshold at 4.0V 1h = Under voltage threshold at 3.0V
20	OV_SEL	R/W	0h	Selects the over voltage threshold on Vcc 0h = Over voltage threshold at 6.1V 1h = Over voltage threshold at 6.5V
19-17	RESERVED	R	00h	Reserved
16	A_HLT_EN	R/W	0h	Enables 2D angle or ALPHA limit check 0h = 2D angle or ALPHA limit check disabled 1h = 2D angle or ALPHA limit check enabled
15	M_HLT_EN	R/W	0h	Enables magnitude or BETA limit check 0h = Magnitude or BETA limit check disabled 1h = Magnitude or BETA limit check enabled

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Table 8-3. Register Field Description (continued)

Bit	Field	Type	Reset	Description
14	T_HLT_EN	R/W	0h	Enables temperature limit check 0h = Temperature limit check disabled 1h = Temperature limit check enabled
13	X_HLT_EN	R/W	0h	Enables X magnetic field limit check 0h = X magnetic field limit check disabled 1h = X magnetic field limit check enabled
12	Y_HLT_EN	R/W	0h	Enables Y magnetic field limit check 0h = Y magnetic field limit check disabled 1h = Y magnetic field limit check enabled
11	Z_HLT_EN	R/W	0h	Enables Z magnetic field limit check 0h = Z magnetic field limit check disabled 1h = Z magnetic field limit check enabled
10-8	HYST_SEL[2:0]	R/W	0h	Enables hysteresis on raw magnetic channel data or calculated angle 0h = No hysteresis enabled 1h = Hysteresis for X channel 2h = Hysteresis for Y channel 3h = Hysteresis for Z channel 4h = Hysteresis for enabled channels per MAG_CH_EN 5h = Hysteresis for 2D angle or ALPHA / BETA angles 6h = Reserved 7h = Reserved
7-0	HYST_VALUE[7:0]	R/W	00h	Hysteresis value for linear axis in mT is calculated as HYST_VALUE × 4 / (SENS). Hysteresis value for angle in degrees is calculated as HYST_VALUE × (1/16)

8.1.3 EEPROM_CONFG2 Register (Offset = 10h) [Reset = 00000000x0000000h]

Figure 8-3. EEPROM_CONFG2 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC2								Y_OFFSET_VALUE[7:0]								X_OFFSET_VALUE[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWIFT_PHYID[3:0]				TC0MAX[6:0]							TC0MIN[6:0]							ADRMAX[6:0]							ADRMIN[6:0]					

Table 8-4. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC2	R	00h	ECC
55-48	Y_OFFSET_VALUE[7:0]	R/W	00h	LSB of 16-bit, two's complement offset value for Y axis channel. The offset value in mT can be calculated as Y_OFFSET_VALUE[15:0] / SENS. Default offset is 0.
47-32	X_OFFSET_VALUE[15:0]	R/W	0000h	16-bit, two's complement offset value for X axis channel. The offset value in mT can be calculated as X_OFFSET_VALUE[15:0] / SENS. Default offset is 0.

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Table 8-4. Register Field Description (continued)

Bit	Field	Type	Reset	Description
31-28	SWIFT_PHYID[3:0]	R/W	xh	Indicates the unique device orderable ID for SWIFT addressing purposes
27-21	TIC0MAX[6:0]	R/W	00h	Maximum number of ticks for low pulse in FEFE Triggered SENT mode
20-14	TIC0MIN[6:0]	R/W	00h	Minimum number of ticks for low pulse in FEFE Triggered SENT mode
13-7	ADRMAX[6:0]	R/W	00h	Maximum number of ticks for Triggered SENT addressing
6-0	ADRMIN[6:0]	R/W	00h	Minimum number of ticks for Triggered SENT addressing

8.1.4 EEPROM_CONFG3 Register (Offset = 18h) [Reset = 0010000000000000h]

Figure 8-4. EEPROM_CONFG3 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC3								X_GAIN[15:0]																ANGLE_OFFSET[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ANGLE_OFFSET[7:0]								Z_OFFSET_VALUE[15:0]																Y_OFFSET_VALUE[15:8]							

Table 8-5. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC3	R	00h	ECC
55-40	X_GAIN[15:0]	R/W	1000h	16-bit unsigned gain correction value for X channel data. Gain value is calculated as X_GAIN × (16/65536). Default gain value is 1 (1000h).
39-24	ANGLE_OFFSET[15:0]	R/W	0000h	16-bit two's complement offset value for 2D angle data. Offset angle in degrees is calculated as ANGLE_OFFSET × (360/65536). Default offset value is 0.
23-8	Z_OFFSET_VALUE[15:0]	R/W	0000h	16-bit, two's complement offset value for Z axis channel. The offset value in MT can be calculated as Z_OFFSET_VALUE[15:0] / SENS. Default offset is 0.
7-0	Y_OFFSET_VALUE[15:8]	R/W	00h	MSB of 16-bit, two's complement offset value for Y axis channel. The offset value in mT can be calculated as Y_OFFSET_VALUE[15:0] / SENS. Default offset is 0.

8.1.5 EEPROM_CONFG4 Register (Offset = 20h) [Reset = 0000000010001000h]

Figure 8-5. EEPROM_CONFG4 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC4								PHASE_CORR_13[7:0]								PHASE_CORR_12[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z_GAIN[15:0]																Y_GAIN[15:0]															

Table 8-6. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC4	R	00h	ECC
55-48	PHASE_CORR_13[7:0]	R/W	00h	LSB for 16 bit two's complement phase correction value for Channel 3 in relation to Channel 1. Default value is 0 for no phase correction. Phase correction value is calculated as PHASE_CORR_13 × (4/32768).
47-32	PHASE_CORR_12[15:0]	R/W	0000h	16 bit two's complement phase correction value for Channel 2 in relation to Channel 1. Default value is 0 for no phase correction. Phase correction value is calculated as PHASE_CORR_12 × (4/32768).

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Table 8-6. Register Field Description (continued)

Bit	Field	Type	Reset	Description
31-16	Z_GAIN[15:0]	R/W	1000h	16-bit unsigned gain correction value for Z channel data. Gain value is calculated as Z_GAIN × (16/65536). Default gain value is 1 (1000h).
15-0	Y_GAIN[15:0]	R/W	1000h	16-bit unsigned gain correction value for Y channel data. Gain value is calculated as Y_GAIN × (16/65536). Default gain value is 1 (1000h).

8.1.6 EEPROM_CONFG5 Register (Offset = 28h) [Reset = 0000000000000000h]

Figure 8-6. EEPROM_CONFG5 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC5								T_LO_THRESHOLD_VALUE[15:0]																2D_A_HI_THRESHOLD_VALUE[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2D_A_HI_THRESHOLD_VALUE[7:0]								2D_A_LO_THRESHOLD_VALUE[15:0]																PHASE_CORR_13[15:8]							

Table 8-7. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC5	R	00h	ECC
55-40	T_LO_THRESHOLD_VALUE[15:0]	R/W	0000h	Temperature minimum threshold in degrees Celsius. stored as a 16 bit two's complement value in 9p7 format.
39-24	2D_A_HI_THRESHOLD_VALUE[15:0]	R/W	0000h	2D angle or ALPHA angle maximum threshold in 16-bit unsigned format. Threshold in degrees is calculated as 2D_A_HI_THRESHOLD × (360/65536)
23-8	2D_A_LO_THRESHOLD_VALUE[15:0]	R/W	0000h	2D angle or ALPHA angle minimum threshold in 16-bit unsigned format. Threshold in degrees is calculated as 2D_A_LO_THRESHOLD × (360/65536)
7-0	PHASE_CORR_13[15:8]	R/W	00h	MSB for 16 bit two's complement phase correction value for Channel 3 in relation to Channel 1. Default value is 0 for no phase correction. Phase correction value is calculated as PHASE_CORR_13 × (4/32768).

8.1.7 EEPROM_CONFG6 Register (Offset = 30h) [Reset = 0000000000000000h]

Figure 8-7. EEPROM_CONFG6 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC6								Y_LO_THRESHOLD_VALUE[7:0]								X_HI_THRESHOLD_VALUE[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X_LO_THRESHOLD_VALUE[15:0]																T_HI_THRESHOLD_VALUE[15:0]															

Table 8-8. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC	R	00h	ECC
55-48	Y_LO_THRESHOLD_VALUE[7:0]	R/W	00h	LSB of Y axis minimum magnetic field threshold stored in 16 bit two's complement format. Threshold in mT can be calculated as Y_LO_THRESHOLD_VALUE / SENS
47-32	X_HI_THRESHOLD_VALUE[15:0]	R/W	0000h	X axis maximum magnetic field threshold stored in 16 bit two's complement format. Threshold in mT can be calculated as X_HI_THRESHOLD_VALUE / SENS
31-16	X_LO_THRESHOLD_VALUE[15:0]	R/W	0000h	X axis minimum magnetic field threshold stored in 16 bit two's complement format. Threshold in mT can be calculated as X_LO_THRESHOLD_VALUE / SENS

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Table 8-8. Register Field Description (continued)

Bit	Field	Type	Reset	Description
15-0	T_HI_THRESHOLD_VALUE[15:0]	R/W	0000h	Temperature maximum threshold in degrees Celsius. stored as a 16 bit two's complement value in 9p7 format.

8.1.8 EEPROM_CONFG7 Register (Offset = 38h) [Reset = 0000000000000000h]

Figure 8-8. EEPROM_CONFG7 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC7								Z_HI_THRESHOLD_VALUE[15:0]																Z_LO_THRESHOLD_VALUE[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z_LO_THRESHOLD_VALUE[7:0]								Y_HI_THRESHOLD_VALUE[15:0]																Y_LO_THRESHOLD_VALUE[15:8]							

Table 8-9. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC7	R	00h	ECC
55-40	Z_HI_THRESHOLD_VALUE[15:0]	R/W	0000h	Z axis maximum magnetic field threshold stored in 16 bit two's complement format. Threshold in mT can be calculated as Z_HI_THRESHOLD_VALUE / SENS
39-24	Z_LO_THRESHOLD_VALUE[15:0]	R/W	0000h	Z axis minimum magnetic field threshold stored in 16 bit two's complement format. Threshold in mT can be calculated as Z_LO_THRESHOLD_VALUE / SENS
23-8	Y_HI_THRESHOLD_VALUE[15:0]	R/W	0000h	Y axis maximum magnetic field threshold stored in 16 bit two's complement format. Threshold in mT can be calculated as Y_HI_THRESHOLD_VALUE / SENS
7-0	Y_LO_THRESHOLD_VALUE[15:8]	R/W	0000h	MSB of Y axis minimum magnetic field threshold stored in 16 bit two's complement format. Threshold in mT can be calculated as Y_LO_THRESHOLD_VALUE / SENS

8.1.9 EEPROM_CONFG8 Register (Offset = 40h) [Reset = 0000000000000000h]

Figure 8-9. EEPROM_CONFG8 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC8								CAL_00[15:0]																RESERVED	LIN_TARGET[2:0]			RESERVED	LIN_SEL[2:0]		
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
M_HI_THRESHOLD_VALUE[15:0]																M_LO_THRESHOLD_VALUE[15:0]															

Table 8-10. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC8	R	00h	ECC
55-40	CAL_00[15:0]	R/W	0000h	16 bit calibration input 0
39	RESERVED	R	0h	Reserved

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Table 8-10. Register Field Description (continued)

Bit	Field	Type	Reset	Description
38-36	LIN_TARGET[2:0]	R/W	0h	Selects the linearization target 0h = Linearization is disabled 1h = 2D angle selected by ANGLE_EN 2h = X axis data 3h = Y axis data 4h = Z axis data 5h = ALPHA and BETA, only 7 and 3 point variable point linearization supported 6h = Reserved 7h = Reserved
35	RESERVED	R	0h	Reserved
34-32	LIN_SEL[2:0]	R/W	0h	Selects the linearization scheme. 0h = 32 point fixed point 1h = 16 point fixed point 2h = 8 point fixed point 3h = 4 point fixed point 4h = 16 point variable point 5h = 8 point variable point (7 point for alpha/beta) 6h = 4 point variable point (3 point for alpha/beta) 7h = Reserved
31-16	M_HI_THRESHOLD_VALUE[15:0]	R/W	0000h	Magnitude or BETA angle maximum threshold stored as 16 bit unsigned value. Calculate magnitude threshold in mT as M_HI_THRESHOLD_VALUE × (x_RANGE / 32768) and x_RANGE is the magnetic range of the axes. Calculate BETA angle threshold in degrees as M_HI_THRESHOLD_VALUE × (360/65536).
15-0	M_LO_THRESHOLD_VALUE[15:0]	R/W	0000h	Magnitude or BETA angle minimum threshold stored as 16 bit unsigned value. Calculate magnitude threshold in mT as M_LO_THRESHOLD_VALUE × (x_RANGE / 32768) and x_RANGE is the magnetic range of the axes. Calculate BETA angle threshold in degrees as M_LO_THRESHOLD_VALUE × (360/65536).

8.1.10 EEPROM_CONFG9 Register (Offset = 48h) [Reset = 0000000000000000h]

Figure 8-10. EEPROM_CONFG9 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC9								CAL_04[7:0]								CAL_03[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_02[15:0]																CAL_01[15:0]														

Table 8-11. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC9	R	00h	ECC
55-48	CAL_04[7:0]	R/W	00h	LSB of 16 bit calibration input 4
47-32	CAL_03[15:0]	R/W	0000h	16 bit calibration input 3
31-16	CAL_02[15:0]	R/W	0000h	16 bit calibration input 2
15-0	CAL_01[15:0]	R/W	0000h	16 bit calibration input 1

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8.1.11 EEPROM_CONFG10 Register (Offset = 50h) [Reset = 0000000000000000h]

Figure 8-11. EEPROM_CONFG10 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC10								CAL_07[15:0]																CAL_06[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_06[7:0]								CAL_05[15:0]																CAL_04[15:8]							

Table 8-12. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC10	R	00h	ECC
55-40	CAL_07[15:0]	R/W	0000h	16 bit calibration input 7
39-24	CAL_06[15:0]	R/W	0000h	16 bit calibration input 6
23-8	CAL_05[15:0]	R/W	0000h	16 bit calibration input 5
7-0	CAL_04[15:8]	R/W	0000h	MSB of 16 bit calibration input 4

8.1.12 EEPROM_CONFG11 Register (Offset = 58h) [Reset = 0000000000000000h]

Figure 8-12. EEPROM_CONFG11 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC11								CAL_11[7:0]								CAL_10[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_09[15:0]																CAL_08[15:0]															

Table 8-13. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC11	R	00h	ECC
55-48	CAL_11[7:0]	R/W	00h	LSB of 16 bit calibration input 11
47-32	CAL_10[15:0]	R/W	0000h	16 bit calibration input 10
31-16	CAL_09[15:0]	R/W	0000h	16 bit calibration input 9
15-0	CAL_08[15:0]	R/W	0000h	16 bit calibration input 8

8.1.13 EEPROM_CONFG12 Register (Offset = 60h) [Reset = 0000000000000000h]

Figure 8-13. EEPROM_CONFG12 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC12								CAL_14[15:0]																CAL_13[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_13[7:0]								CAL_12[15:0]																CAL_11[15:8]							

Table 8-14. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC12	R	00h	ECC
55-40	CAL_14[15:0]	R/W	0000h	16 bit calibration input 14
39-24	CAL_13[15:0]	R/W	0000h	16 bit calibration input 13
23-8	CAL_12[15:0]	R/W	0000h	16 bit calibration input 12
7-0	CAL_11[15:8]	R/W	00h	MSB of 16 bit calibration input 11

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8.1.14 EEPROM_CONFG13 Register (Offset = 68h) [Reset = 0000000000000000h]

Figure 8-14. EEPROM_CONFG13 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC13								CAL_18[7:0]								CAL_17[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_16[15:0]																CAL_15[15:0]														

Table 8-15. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC13	R	00h	ECC
55-48	CAL_18[7:0]	R/W	00h	LSB of 16 bit calibration input 18
47-32	CAL_17[15:0]	R/W	0000h	16 bit calibration input 17
31-16	CAL_16[15:0]	R/W	0000h	16 bit calibration input 16
15-0	CAL_15[15:0]	R/W	0000h	16 bit calibration input 15

8.1.15 EEPROM_CONFG14 Register (Offset = 70h) [Reset = 0000000000000000h]

Figure 8-15. EEPROM_CONFG14 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC14								CAL_21[15:0]																CAL_20[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_20[7:0]								CAL_19[15:0]																CAL_18[15:8]							

Table 8-16. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC14	R	00h	ECC
55-40	CAL_21[15:0]	R/W	0000h	16 bit calibration input 21
39-24	CAL_20[15:0]	R/W	0000h	16 bit calibration input 20
23-8	CAL_19[15:0]	R/W	0000h	16 bit calibration input 19
7-0	CAL_18[15:8]	R/W	00h	MSB of 16 bit calibration input 18

8.1.16 EEPROM_CONFG15 Register (Offset = 78h) [Reset = 0000000000000000h]

Figure 8-16. EEPROM_CONFG15 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC15								CAL_25[7:0]								CAL_24[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_23[15:0]																CAL_22[15:0]														

Table 8-17. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC15	R	00h	ECC
55-48	CAL_25[7:0]	R/W	00h	LSB of 16 bit calibration input 25
47-32	CAL_24[15:0]	R/W	0000h	16 bit calibration input 24
31-16	CAL_23[15:0]	R/W	0000h	16 bit calibration input 23
15-0	CAL_22[15:0]	R/W	0000h	16 bit calibration input 22

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8.1.17 EEPROM_CONFG16 Register (Offset = 80h) [Reset = 0000000000000000h]

Figure 8-17. EEPROM_CONFG16 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC16								CAL_28[15:0]																CAL_27[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_27[7:0]								CAL_26[15:0]																CAL_25[15:8]							

Table 8-18. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC16	R	00h	ECC
55-40	CAL_28[15:0]	R/W	0000h	16 bit calibration input 28
39-24	CAL_27[15:0]	R/W	0000h	16 bit calibration input 27
23-8	CAL_26[15:0]	R/W	0000h	16 bit calibration input 26
7-0	CAL_25[15:8]	R/W	00h	MSB 16 bit calibration input 25

8.1.18 EEPROM_CONFG17 Register (Offset = 88h) [Reset = 0000000000000000h]

Figure 8-18. EEPROM_CONFG17 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC17								CAL_32[7:0]								CAL_31[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL_30[15:0]																CAL_29[15:0]															

Table 8-19. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC17	R	00h	ECC
55-48	CAL_32[7:0]	R/W	00h	LSB of 16 bit calibration input 32
47-32	CAL_31[15:0]	R/W	0000h	16 bit calibration input 31
31-16	CAL_30[15:0]	R/W	0000h	16 bit calibration input 30
15-0	CAL_29[15:0]	R/W	0000h	16 bit calibration input 29

8.1.19 EEPROM_CONFG18 Register (Offset = 90h) [Reset = 0000000000000000h]

Figure 8-19. EEPROM_CONFG18 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC18								FAST_CH_CHR_X2[15:0]																FAST_CH_CHR_X1[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAST_CH_CHR_X1[7:0]								PROTOCOL_REV[15:0]																CAL_32[15:8]							

Table 8-20. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC18	R	00h	ECC
55-40	FAST_CH_CHR_X2[15:0]	R/W	0000h	SENT Fast channel characteristics for SENT slow serial communication
39-24	FAST_CH_CHR_X1[15:0]	R/W	0000h	SENT Fast channel characteristics for SENT slow serial communication
23-8	PROTOCOL_REV[15:0]	R/W	0000h	SAE SENT protocol revision.
7-0	CAL_32[15:8]	R/W	00h	MSB of 16 bit calibration input 32

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8.1.20 EEPROM_CONFG19 Register (Offset = 98h) [Reset = 0000000000000000h]

Figure 8-20. EEPROM_CONFG19 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC19								ASCII_OEM_2[7:0]								ASCII_OEM_1[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FAST_CH_CHR_Y2[15:0]																FAST_CH_CHR_Y1[15:0]														

Table 8-21. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC19	R	00h	ECC
55-48	ASCII_OEM_2[7:0]	R/W	00h	OEM information for SENT slow serial communication
47-32	ASCII_OEM_1[15:0]	R/W	0000h	OEM information for SENT slow serial communication
31-16	FAST_CH_CHR_Y2[15:0]	R/W	0000h	SENT fast channel characteristics for SENT slow serial communication
15-0	FAST_CH_CHR_Y1[15:0]	R/W	0000h	SENT fast channel characteristics for SENT slow serial communication

8.1.21 EEPROM_CONFG20 Register (Offset = A0h) [Reset = 0000000000000000h]

Figure 8-21. EEPROM_CONFG20 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC20								ASCII_OEM_5[15:0]																ASCII_OEM_4[15:8]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASCII_OEM_4[7:0]								ASCII_OEM_3[15:0]																ASCII_OEM_2[15:8]							

Table 8-22. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC20	R	00h	ECC
55-40	ASCII_OEM_5[15:0]	R/W	0000h	OEM information for SENT slow serial communication
39-24	ASCII_OEM_4[15:0]	R/W	0000h	OEM information for SENT slow serial communication
23-8	ASCII_OEM_3[15:0]	R/W	0000h	OEM information for SENT slow serial communication
7-0	ASCII_OEM_2[15:8]	R/W	00h	OEM information for SENT slow serial communication

8.1.22 EEPROM_CONFG21 Register (Offset = A8h) [Reset = 0000000000000000h]

Figure 8-22. EEPROM_CONFG21 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC21								RESERVED								ASCII_OEM_8[15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASCII_OEM_7[15:0]																ASCI_OEM_6[15:0]															

Table 8-23. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC21	R	00h	ECC
55-48	RESERVED	R	00h	Reserved.
47-32	ASCII_OEM_8[15:0]	R/W	0000h	OEM information for SENT slow serial communication
31-16	ASCII_OEM_7[15:0]	R/W	0000h	OEM information for SENT slow serial communication
15-0	ASCI_OEM_6[15:0]	R/W	0000h	OEM information for SENT slow serial communication

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8.1.23 EEPROM_CONFG22 Register (Offset = B0h) [Reset = 0000000000000058h]

Figure 8-23. EEPROM_CONFG22 Register Field Descriptions

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
ECC22								RESERVED																							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCKOUT[3:0]				RESERVED				SENSOR_TYPE[11:0]												TI_MAN_CODE[11:0]											

Table 8-24. Register Field Description

Bit	Field	Type	Reset	Description
63-56	ECC22	R	00h	ECC
55-32	RESERVED	R	000000h	Reserved
31-28	LOCKOUT[3:0]	R/W	0h	Enables different programming lockout modes for the device 0h = No lockout enabled 1h = Reserved 2h = Reserved 3h = Reserved 4h = Reserved 5h = Reserved 6h = Reserved 7h = Lock out only SWIFT EEPROM programming 8h = Reserved 9h = Reserved Ah = Reserved Bh = Lock out all SWIFT writes to the memory map except SWIFT mailbox Ch = Reserved Dh = Lock out both SWIFT read and write access to memory map except SWIFT mailbox Eh = Lock out SWIFT access completely Fh = Reserved
27-24	RESERVED	R	0h	Reserved
23-12	SENSOR_TYPE[11:0]	R/W	000h	Sensor type for SENT slow serial communication
11-0	TI_MAN_CODE[11:0]	R/W	058h	TI manufacturer code for SENT slow serial communication

8.1.24 USER_REG0 Register (Offset = 200h) [Reset = 00000000h]

Figure 8-24. USER_REG0 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDY	RESERVED		MAGB_THX	2DA_THX	RESERVED	AFE_FAIL	ADC_FAIL	RESERVED	ZHS_STAT	YHS_STAT	ZHS_STAT	TEMP_THX	ZCH_THX	YCH_THX	XCH_THX	E2P_DED	E2P_PWRF	OSC_ERR	VCC_UV	VCC_OV	CONF_ERR	LDO_STAT	MEM_ERR	A	T	Z	Y	X	SET_COUNT[2:0]		

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Table 8-25. Register Field Description

Bit	Field	Type	Reset	Description
31	RDY	R	0h	Conversion data buffer is ready 0h = Conversion in progress (result registers hold previous result) 1h = Conversion complete
30-29	RESERVED	R	0h	Reserved
28	MAGB_THX	R	0h	Magnitude or BETA angle threshold crossing detected 0h = No magnitude or BETA angle threshold crossing detected 1h = Magnitude or BETA angle threshold crossing detected
27	2DA_THX	R	0h	2D angle or ALPHA angle threshold crossing detected 0h = No 2D angle or ALPHA angle threshold crossing detected 1h = 2D angle or ALPHA angle threshold crossing detected
26	HS_OFFSET_STAT	R	0h	Hall sensor offset diagnostic status 0h = No Hall sensor offset error detected 1h = Hall sensor offset error detected
25	AFE_FAIL	R	0h	Analog front end diagnostic status 0h = No AFE error detected 1h = AFE error detected
24	ADC_FAIL	R	0h	ADC diagnostic status 0h = No ADC error detected 1h = ADC error detected
23	RESERVED	R	0h	Reserved
22	ZHS_STAT	R	0h	Z axis Hall sensor diagnostic status 0h = No Z axis Hall sensor error detected 1h = Z axis Hall sensor diagnostic test failed
21	YHS_STAT	R	0h	Y axis Hall sensor diagnostic status 0h = No Y axis Hall sensor error detected 1h = Y axis Hall sensor diagnostic test failed
20	XHS_STAT	R	0h	X axis Hall sensor diagnostic status 0h = No X axis Hall sensor error detected 1h = X axis Hall sensor diagnostic test failed
19	TEMP_THX	R	0h	Temperature threshold crossing detected 0h = No temperature threshold crossing detected 1h = Temperature threshold crossing detected
18	ZCH_THX	R	0h	Z axis channel threshold crossing detected 0h = No Z axis channel threshold crossing detected 1h = Z axis channel threshold crossing detected
17	YCH_THX	R	0h	Y axis channel threshold crossing detected 0h = No Y axis channel threshold crossing detected 1h = Y axis channel threshold crossing detected
16	XCH_THX	R	0h	X axis channel threshold crossing detected 0h = No X axis channel threshold crossing detected 1h = X axis channel threshold crossing detected

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Table 8-25. Register Field Description (continued)

Bit	Field	Type	Reset	Description
15	E2P_DED	R	0h	EEPROM double error detection. Power cycle the device to clear. 0h = No EEPROM double error detected 1h = EEPROM double error detected
14	E2P_PWRF	R/W	0h	EEPROM power failure during EEPROM write. Write 1 to this bit or power cycle the device to clear. 0h = No EEPROM power failure during write detected 1h = EEPROM power failure during write detected
13	OSC_ERR	R	0h	Oscillator error detected 0h = No oscillator error detected 1h = Oscillator error detected
12	VCC_UV	R	0h	VCC under voltage detection 0h = No VCC under voltage detected 1h = VCC under voltage detected
11	VCC_OV	R	0h	VCC over voltage detection 0h = No VCC over voltage detected 1h = VCC over voltage detected
10	CONF_ERR	R	0h	Configuration register CRC error. Power cycle needed to clear. 0h = No configuration register CRC error detected 1h = Configuration register CRC error detected.
9	LDO_STAT	R	0h	Internal LDO under voltage check 0h = No LDO undervoltage detected 1h = LDO under voltage detected
8	MEM_ERR	R	0h	Memory (RAM or ROM) double error detection 0h = No memory double error detected 1h = Memory double error detected
7	A	R	0h	2D angle/Magnitude/ALPHA/BETA data from current conversion 0h = Data is not current 1h = Data is current
6	T	R	0h	Temperature data from current conversion 0h = Temperature data is not current 1h = Temperature data is current
5	Z	R	0h	Z axis data from current conversion 0h = Z axis data is not current 1h = Z axis data is current
4	Y	R	0h	Y axis data from current conversion 0h = Y axis data is not current 1h = Y axis data is current
3	X	R	0h	X axis data from current conversion 0h = Z axis data is not current 1h = Z axis data is current
2-0	SET_COUNT[2:0]	R	0h	Rolling count of conversion data sets. SET_COUNT is incremented with the completion of each conversion sequence.

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8.1.25 USER_REG1 Register (Offset = 204h) [Reset = 00000000h]

Figure 8-25. USER_REG1 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Y_CH_RESULT[15:0]																X_CH_RESULT[15:0]															

Table 8-26. Register Field Description

Bit	Field	Type	Reset	Description
31-16	Y_CH_RESULT[15:0]	R	0000h	Y channel data conversion result
15-0	X_CH_RESULT[15:0]	R	0000h	Z channel data conversion result

8.1.26 USER_REG2 Register (Offset = 208h) [Reset = 00000000h]

Figure 8-26. USER_REG2 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TEMP_RESULT[15:0]																Z_CH_RESULT[15:0]															

Table 8-27. Register Field Description

Bit	Field	Type	Reset	Description
31-16	TEMP_RESULT[15:0]	R	0000h	Temperature data conversion result. 16 bit two's complement 10p7 format
15-0	Z_CH_RESULT[15:0]	R	0000h	Z channel data conversion result

8.1.27 USER_REG3 Register (Offset = 20Ch) [Reset = 00000000h]

Figure 8-27. USER_REG3 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAGNITUDE_BETA[15:0]																ANGLE_ALPHA[15:0]															

Table 8-28. Register Field Description

Bit	Field	Type	Reset	Description
31-16	MAGNITUDE_BETA[15:0]	R	0000h	Magnitude or BETA angle conversion results
15-0	ANGLE_ALPHA[15:0]	R	0000h	2D angle or ALPHA angle conversion results.

8.1.28 USER_REG4 Register (Offset = 210h) [Reset = 00000000h]

Figure 8-28. USER_REG4 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																					DEV_VER[2:0]			SWIFT_CPU_MAILBOX[7:0]							

Table 8-29. Register Field Description

Bit	Field	Type	Reset	Description
31-11	RESERVED	R	00000h	Reserved
10-8	DEV_VER[2:0]	R	0h	Indicates the version of the device

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Table 8-29. Register Field Description (continued)

Bit	Field	Type	Reset	Description
7-0	SWIFT_CPU_MAILBOX[7:0]	R/W	xxh	Commands to execute SWIFT conversions, transition to operating modes, collect factory measurements, and transfer messages between the SWIFT host and the device. 0h = No command. 30h = Enable AFE in SWIFT mode 31h = Run AFE once to execute only one conversion in SWIFT mode per EEPROM settings. Results are loaded into RESULT registers after conversion is complete 81h = Run the device in Synchronous Trigger Conversion/ Trigger SENT mode (Triggered by Host). Ensure OPERATING_MODE remains at 0h and relevant EEPROM configuration bitfields are programmed. 82h = Run the device in Synchronous Continuous Conversion/ Trigger SENT mode (SENT frame triggered by end of conversion). Ensure OPERATING_MODE remains at 0h and relevant EEPROM configuration bitfields are programmed. 83h = Run the device in Asynchronous Continuous Conversion/ Trigger SENT mode (SENT frame triggered by Host). Ensure OPERATING_MODE remains at 0h and relevant EEPROM configuration bitfields are programmed. 84h = Run the device in Asynchronous Continuous Conversion/ Continuous SENT mode. Ensure OPERATING_MODE remains at 0h and relevant EEPROM configuration bitfields are programmed. 85h = Run the device in PWM mode. Ensure OPERATING_MODE remains at 0h and relevant EEPROM configuration bitfields are programmed. 86h = Run the device in Analog mode. Ensure OPERATING_MODE remains at 0h and relevant EEPROM configuration bitfields are programmed. CDh = Change to SENT / Analog / PWM operating mode. This is a soft reset command that transitions the device into operating mode and starts conversions per EEPROM settings without the requirement of power cycling the device.

8.1.29 USER_REG5 Register (Offset = 214h) [Reset = 00000000h]

Figure 8-29. USER_REG5 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIRST_CONV	RESERVED			CHANNEL_ID[3:0]				SEQUENCE_COUNT[7:0]								ADC_CONV_RESULT[15:0]															

Table 8-30. Register Field Description

Bit	Field	Type	Reset	Description
31	FIRST_CONV	R	0h	First conversion in a multiple conversion sequence is complete 0h = Not the first conversion in a sequence 1h = First conversion in a sequence
30-28	RESERVED	R	0h	Reserved

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Table 8-30. Register Field Description (continued)

Bit	Field	Type	Reset	Description
27-24	CHANNEL_ID[3:0]	R	0h	Identification of the input channel of conversion result data. 0h = No channel 1h = Temperature channel 2h = X channel 3h = Y channel 4h = Z channel 5h = X resistance check 6h = Y resistance check 7h = Z resistance check 8h = Offset check 9h = AFE check Ah = ADC check Bh = Reserved Ch = Reserved Dh = Reserved Eh = Reserved Fh = Reserved
23-16	SEQUENCE_COUNT[7:0]	R	00h	Rolling count of completed conversions within a sequence of conversions. Resets at the beginning of each conversion sequence.
15-0	ADC_CONV_RESULT[15:0]	R	0000h	ADC conversion result. Contains raw ADC conversion data (before any corrections) for system debug purposes.

8.1.30 USER_REG6 Register (Offset = 218h) [Reset = 00000000h]

Figure 8-30. USER_REG6 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																AFE_EN	AFE_STDBY	RESERVED		AFE_1CH	RESERVED	DIAG_EN[1:0]		FILTER_SEL[3:0]				MAG_CH_EN[3:0]			

Table 8-31. Register Field Description

Bit	Field	Type	Reset	Description
31-16	RESERVED	R	0h	Reserved
15	AFE_EN	R/W	0h	Enable for Analog Front End to begin data conversion sequences 0h = AFE disabled 1h = AFE enabled
14	AFE_STDBY	R/W	0h	Suspends data conversion and hold Analog Front End in Standby mode. User can write AFE_STDBY to 0h if continuous AFE conversions are desired. During continuous AFE conversions, data read from the result registers can not all be from the same conversion set. 0h = AFE active 1h = AFE in standby mode
13-12	RESERVED	R	0h	Reserved

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Table 8-31. Register Field Description (continued)

Bit	Field	Type	Reset	Description
11	AFE_1CH	R/W	0h	For TI test. Leave as default value of 0h. Enables single channel conversions.
10	RESERVED	R	0h	Reserved
9-8	DIAG_EN[1:0]	R/W	0h	Diagnostics selection 0h = Turn off all diagnostics (default) 1h = Turn on all diagnostics 2h = Turn on only active channel diagnostics 3h = Reserved
7-4	FILTER_SEL[3:0]	R/W	0h	Enables conversion filter settings to optimize speed versus noise performance 0h = 45kHz, 263us (3 axes), 180us (2 axes), 97us (1 axis) 1h = 22.5kHz, 266us (3 axes), 182us (2 axes), 98us (1 axis) 2h = 11.25kHz, 272us (3 axes), 186us (2 axes), 100us (1 axis) 3h = 5.625kHz, 284us (3 axes), 194us (2 axes), 104us (1 axis) 4h = 2.8125kHz, 308us (3 axes), 210us (2 axes), 112us (1 axis) 5h = 1.4kHz, 356us (3 axes), 242us (2 axes), 128us (1 axis) 6h = 700Hz, 452us (3 axes), 306us (2 axes), 160us (1 axis) 7h = 350Hz, 644us (3 axes), 434us (2 axes), 224us (1 axis) 8h = 175Hz, 1.028ms (3 axes), 690us (2 axes), 352us (1 axis) 9h = 87Hz, 1.796ms (3 axes), 1.202ms (2 axes), 608us (1 axis) Ah = 44Hz, 3.332ms (3 axes), 2.226ms (2 axes), 1.120ms (1 axis) Bh = 22Hz, 6.404ms (3 axes), 4.274ms (2 axes), 2.144ms (1 axis) Ch = 11Hz, 12.548ms (3 axes), 8.370ms (2 axes), 4.192ms (1 axis) Dh = 5.5Hz, 24.836ms (3 axes), 16.562ms (2 axes), 8.288ms (1 axis) Eh = 2.75Hz, 49.412ms (3 axes), 32.946ms (2 axes), 16.480ms (1 axis) Fh = 1.4Hz, 98.564ms (3 axes), 65.714ms (2 axes), 32.864ms (1 axis)

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Table 8-31. Register Field Description (continued)

Bit	Field	Type	Reset	Description
3-0	MAG_CH_EN[3:0]	R/W	0h	Enables data acquisition of the magnetic axis channels 0h = All magnetic channels disabled (default) 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channel enabled 4h = Z channel enabled 5h = Z, X channel enabled 6h = Y, Z channel enabled 7h = X, Y, Z channel enabled 8h = X, Y, X channel enabled 9h = Y, X, Y channel enabled Ah = Y, Z, Y channel enabled Bh = Z, Y, Z channel enabled Ch = Z, X, Z channel enabled Dh = X, Z, X channel enabled Eh = X, Y, Z, Y, X channel enabled Fh = X, Y, Z, Z, Y, X channel enabled

8.1.31 USER_REG7 Register (Offset = 21Ch) [Reset = 00000000h]

Figure 8-31. USER_REG7 Register Field Descriptions

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Table 8-32. Register Field Description

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	00000000h	Reserved

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Selecting the Sensitivity Option

Select the highest TMAG3101-Q1 sensitivity option that can measure the required range of magnetic flux density so that the ADC output range is maximized.

Larger-sized magnets and shorter sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool, TI Magnetic Sense Simulator (TIMSS) to help with simple magnet calculations on ti.com.

9.2 Typical Application

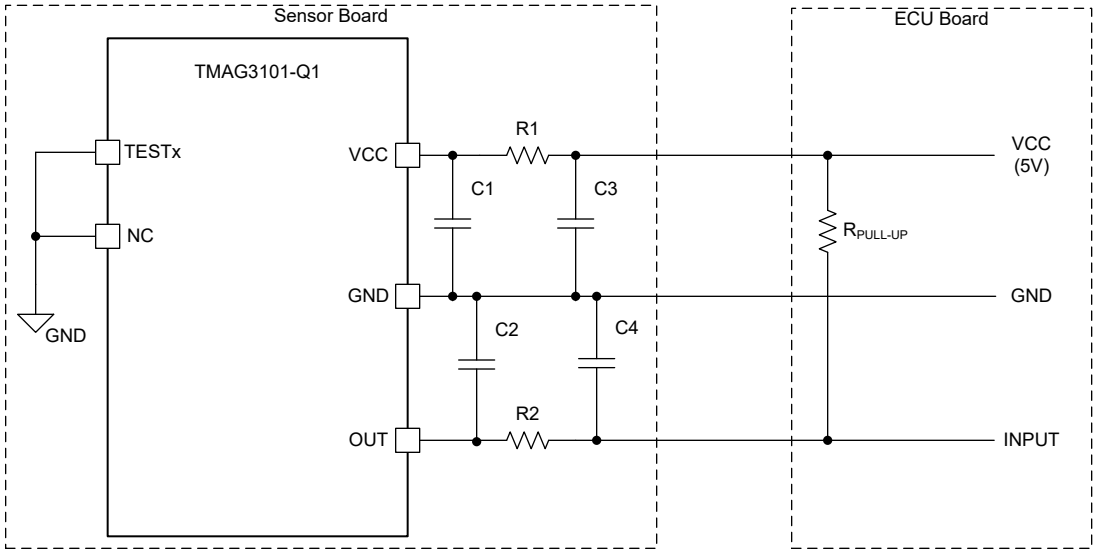


Figure 9-1. TMAG3101-Q1 Recommended Application Circuit

When operating the TMAG3101 in SENT or Triggered SENT mode with open-drain output, select appropriate values for the capacitor and pullup resistor on the OUT pin to provide a suitable RC time constant for the rise time for the selected tick time.

Table 9-1. Recommended RC Time Constants for SENT Mode With Open-drain Output

SENT tick time (µs)	0.25	0.5	1	2	3	5	6	12
Recommended max RC time constant (µs)	0.26	0.56	1.16	2.36	3.56	5.96	7.16	14.36

Table 9-2. Recommended External Components

Component	Min. Value	Typ. Value	Max. Value	Comment
SENT and PWM Output				
C_1	470nF	1µF	-	Place as close to the device as possible

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Table 9-2. Recommended External Components (continued)

Component	Min. Value	Typ. Value	Max. Value	Comment
C_2	-	1nF	5nF	For SENT, select based on tick time
C_3	-	-	1nF	Optional, for improved EMC performance
C_4	-	-	1nF	
R_1	-	-	10Ω	
R_2	-	-	-	
$R_{PULL-UP}$	3kΩ	10kΩ	-	For SENT, select based on tick time
Triggered SENT Output				
C_1	470nF	1µF	-	Place as close to the device as possible
C_2	-	1nF	5nF	Select based on tick time
C_3	-	0nF	1nF	Optional, for improved EMC performance
C_4	-	0nF	1nF	
R_1	-	0Ω	10Ω	
R_2	-	0Ω	-	
$R_{PULL-UP}$	3kΩ	10kΩ	-	Select based on tick time
Analog Output				
C_1	470nF	1µF	-	Place as close to the device as possible
C_2	10nF	10nF	330nF	
C_3	-	-	1nF	Optional, for improved EMC performance
C_4	-	-	1nF	
R_1	-	-	10Ω	
R_2	-	-	-	
$R_{PULL-UP}$	3kΩ	10kΩ	-	

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9.2.1 Design Requirements

Magnetic angle sensors are popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG3101-Q1 offers an on-chip angle calculator that can provide angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE_EN register bits. The device offers an angle output in complete 360 degree scale. The TMAG3101-Q1 supports multiple error correction schemes to enhance system measurement accuracy. In this section the linearization example is described. In the presence of wider mechanical tolerances, in some applications additional pre-linearizations corrections such as gain, offset, and phase corrections can yield the desired system accuracy.

Use the parameters listed in Table 9-3 for this design example

Table 9-3. Design Parameters

DESIGN PARAMETERS	2D ANGLE MEASUREMENT
Linearization Scheme	Variable
VCC	5V
Magnet	Cylinder: 4.7625mm diameter, 12.7mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<1000
Desired Accuracy after Linearization	<0.1° for full 360° rotation (–180° to 180°)

9.2.2 Detailed Design Procedure

The device calibration is performed in the SWIFT mode.

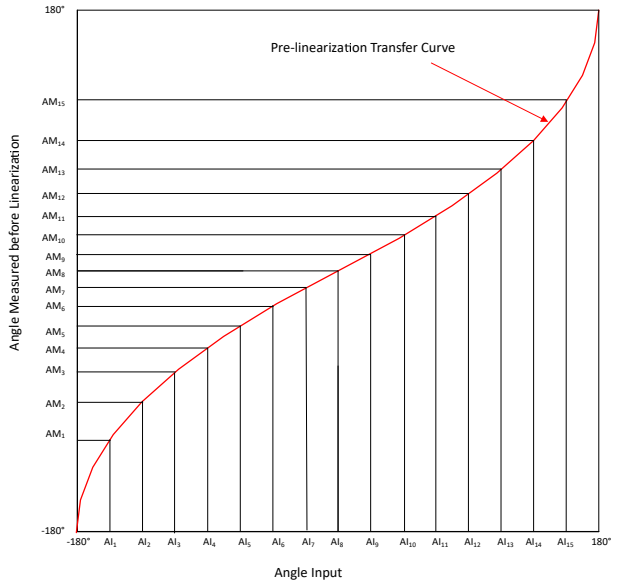


Figure 9-2. TMAG3101-Q1 Pre-Linearization Transfer Curve

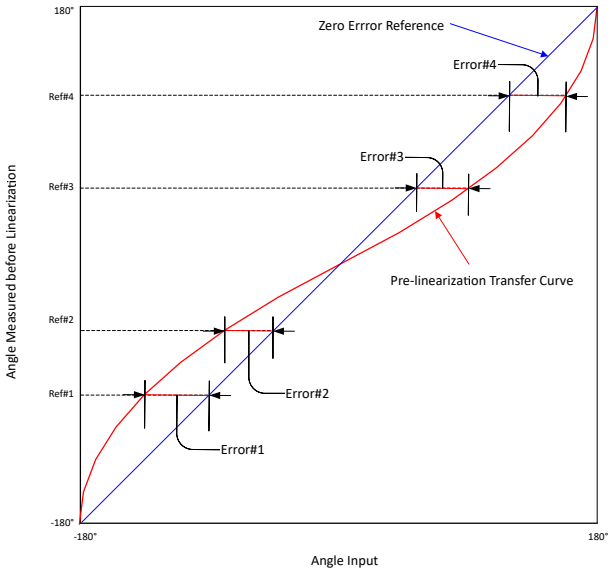


Figure 9-3. TMAG3101-Q1 Variable Point Linearization

1. Set the device for on-axis X-Y angle measurement.
2. Set the MAG_CH_EN = 0011b, FILTER_SEL =1010b.
3. Start with 0 degree angular position of the rotating magnet, and increment the magnet position 1 degree at a time, and measure the device CORDIC angle data for each angular position.

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4. Record the magnet position input angles and corresponding CORDIC angle outputs for full 360 degree. A reduced set of data can be collected if the angle accuracy target is wider, or the angle of interest is less than 360 degree.
5. Wait for the results to generate the 'pre-linearization transfer curve. Figure 9-2 shows an example of transfer curve with reduced set of points for illustrations.
6. Select the first reference point, Ref#1 from the vertical axis of the pre-linearization transfer curve as shown in Figure 9-3. Calculate the offset as the difference between transfer curve and zero error reference line at Ref#1, Offset = Error#1.
7. Select the second reference point, Ref#2 from the vertical axis of the pre-linearization transfer curve as shown in Figure 9-3. Calculate the Error#2 as the difference between transfer curve and zero error reference line at Ref#2. The Ref#1 linearization coefficient, Coeff#1 is calculated as

$$\text{Coeff \# 1} = \frac{\text{Error \# 2} - \text{Error \# 1}}{\text{Ref \# 2} - \text{Ref \# 1}} \times 256 \quad (31)$$

8. Select the third reference point, Ref#3 from the vertical axis of the pre-linearization transfer curve as shown in Figure 9-3. Calculate the Error#3 as the difference between transfer curve and zero error reference line at Ref#3. The Ref#2 linearization coefficient, Coeff#2 is calculated as

$$\text{Coeff \# 2} = \frac{\text{Error \# 3} - \text{Error \# 2}}{\text{Ref \# 3} - \text{Ref \# 2}} \times 256 \quad (32)$$

9. Select the fourth reference point, Ref#4 from the vertical axis of the pre-linearization transfer curve as shown in Figure 9-3. Calculate the Error#4 as the difference between transfer curve and zero error reference line at Ref#4. The Ref#3 linearization coefficient, Coeff#3 is calculated

$$\text{Coeff \# 3} = \frac{\text{Error \# 4} - \text{Error \# 3}}{\text{Ref \# 4} - \text{Ref \# 3}} \times 256 \quad (33)$$

10. Similarly select the successive reference points and calculate the linearization coefficient data as

$$\text{Coeff \# n} = \frac{\text{Error \# (n + 1)} - \text{Error \# n}}{\text{Ref \# (n + 1)} - \text{Ref \# n}} \times 256 \quad (34)$$

11. For variable point linearization store the reference points and the corresponding linearization coefficients in the EEPROM locations as mapped in Table 7-8.
12. For fixed point linearization store the corresponding linearization coefficients in the EEPROM locations as mapped in Table 7-6.
13. After the linearization table is populated with the right coefficient values, if the measured angle A falls in between Ref#n and ref# (n+1), the TMAG3101-Q1 reports the corrected angle, A_L as

$$A_L = A - \left(\text{Offset} + \left(\sum_{i=1}^{n-1} (\text{Ref \# (i + 1)} - \text{Ref \# (i)}) \times \frac{\text{Coeff \# (i)}}{256}\right) + \left((A - \text{Ref \# n}) \times \frac{\text{Coeff \# n}}{256}\right)\right) \quad (35)$$

9.3 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.1µF. Connect the TEST and NC pins to ground.

9.4 Layout

9.4.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall-effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

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9.4.2 Layout Example

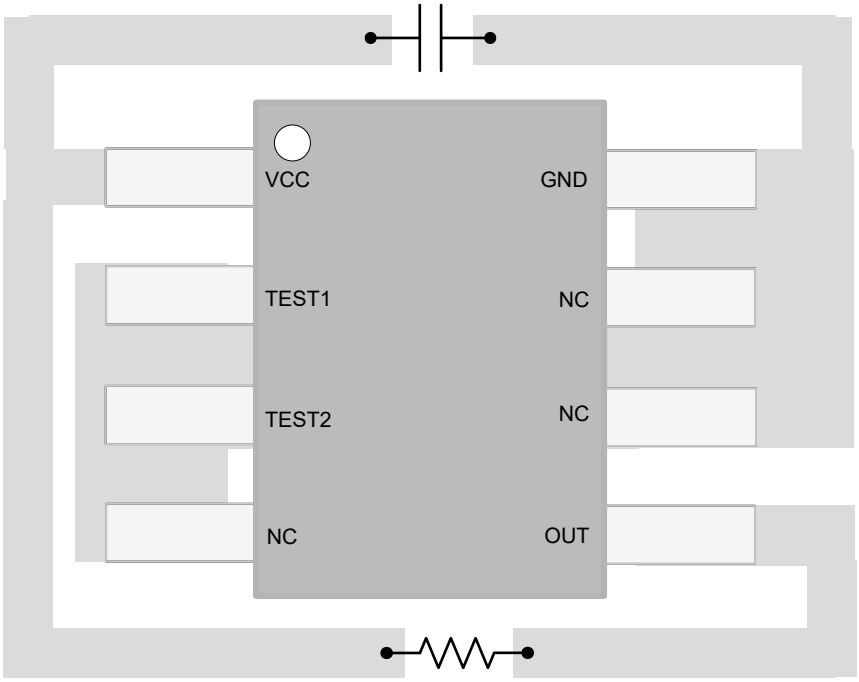


Figure 9-4. Layout Example With TMAG3101-Q1

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10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2026	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.

ADVANCE INFORMATION

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12.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4)(5)
PMAG3101A3A0PWRQ1	PREVIEW	TSSOP	PW	8	2000 | LARGE T&R	RoHS	Sn	Level 3-260C-168 HR	-40°C to 160°C	P1A3A

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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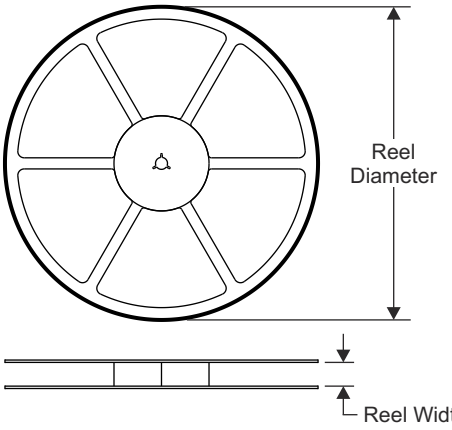
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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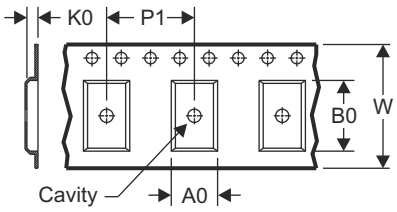
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12.2 Tape and Reel Information

REEL DIMENSIONS

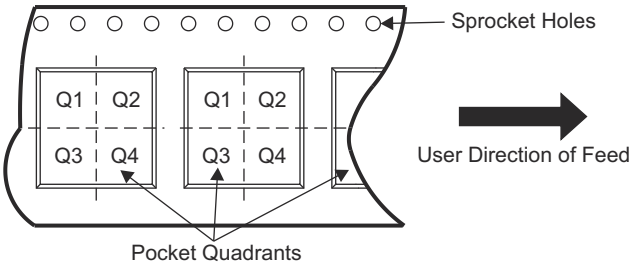


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



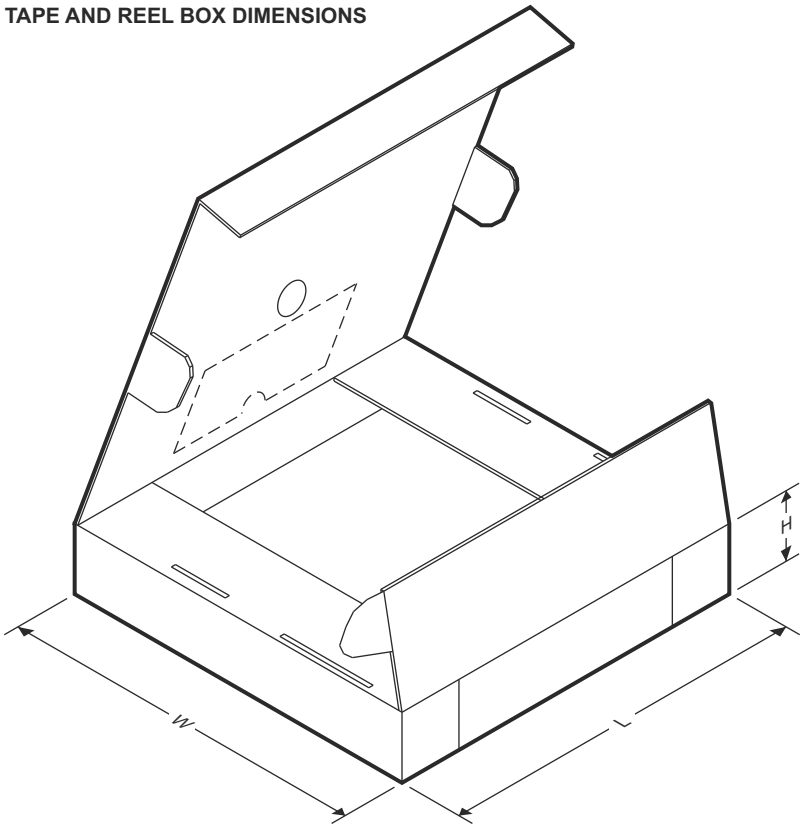
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PMAG3101A3A0PWRQ1	TSSOP	PW	8	2000	330	12.4	6.4	5.2	2.1	8	12	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PMAG3101A3A0PWRQ1	TSSOP	PW	8	2000	367	367	35

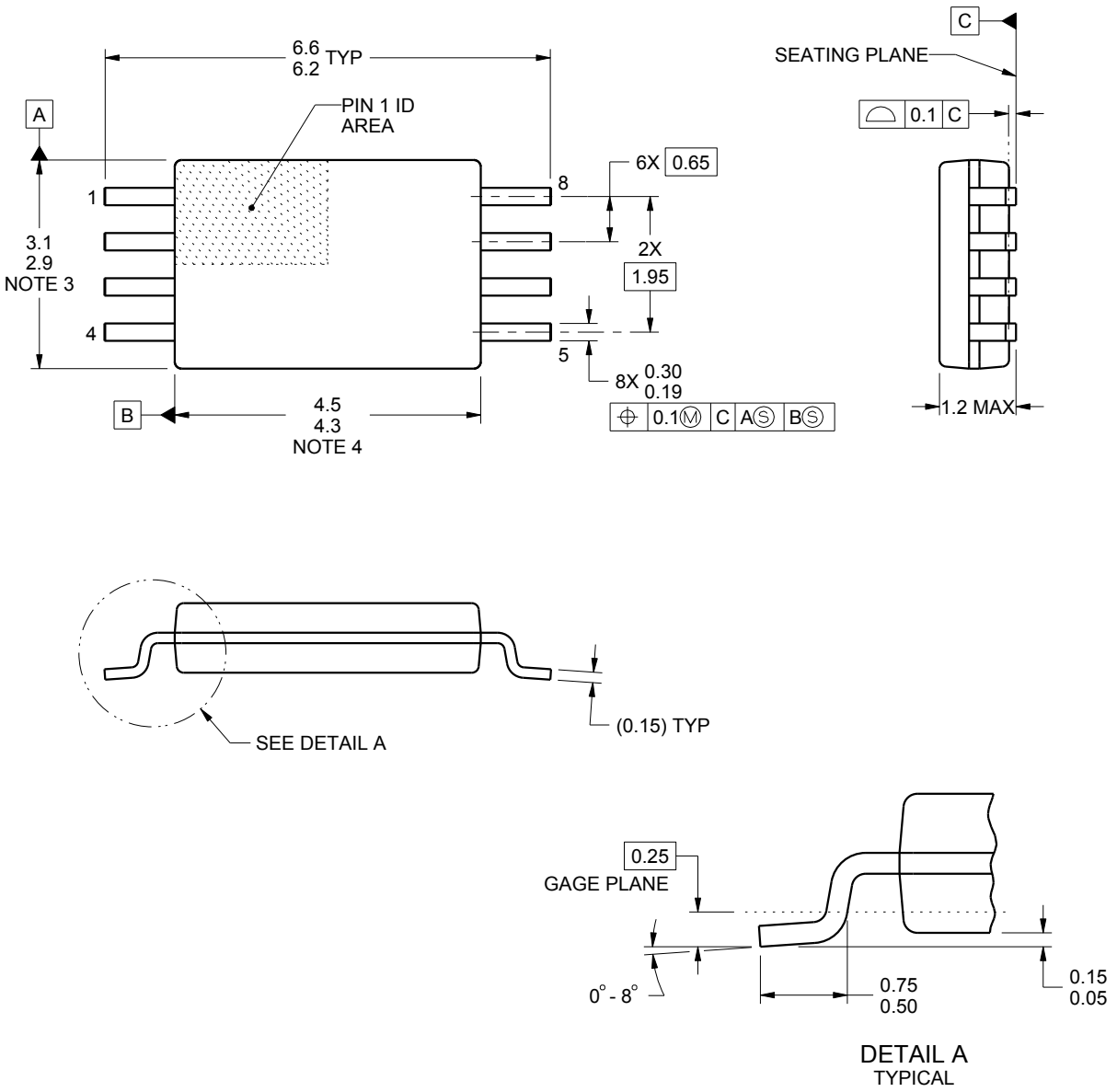
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PACKAGE OUTLINE

PW0008A

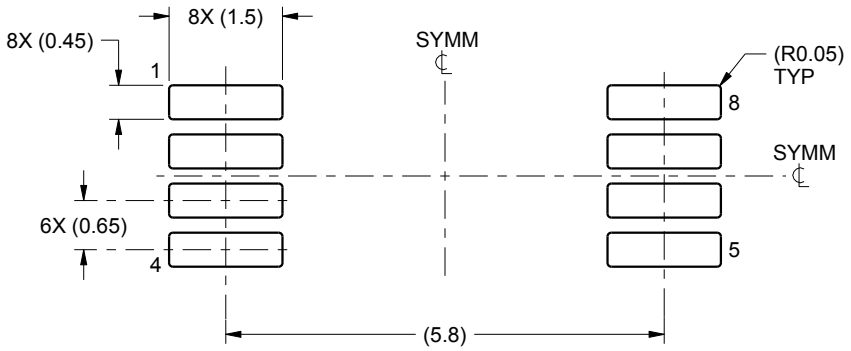
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

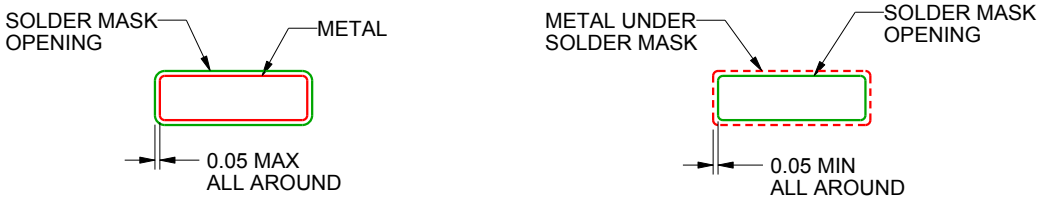


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

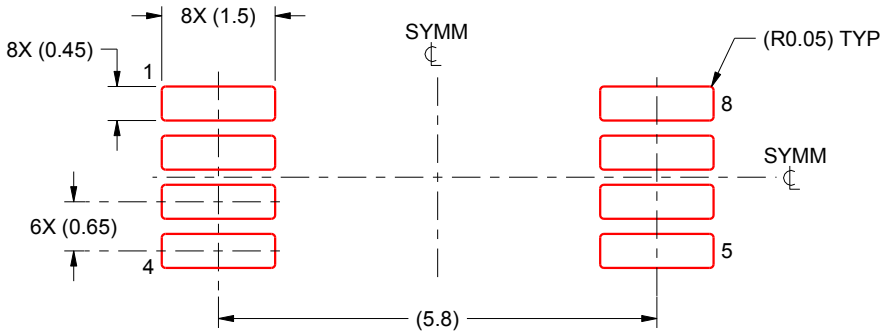


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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