# TMUX1574 Low-Capacitance, 2:1 (SPDT) 4-Channel, Powered-Off Protected Switch with 1.8 V Logic

## 1 Features

- Wide supply range: 1.5 V to 5.5 V
- Low on-capacitance: 7.5 pF
- Low on-resistance: 2 Ω
- High bandwidth: 2 GHz
- -40°C to +125°C operating temperature
- 1.8 V Logic Compatible
- Supports Input Voltage Beyond Supply
- Integrated Pull Down Resistor on Logic Pins
- Bidirectional Signal Path
- Fail-Safe Logic
- Powered-off Protection up to 3.6 V Signals
  - Pinout compatible to SN74CBTLV3257

## 2 Applications

- Flash memory sharing
- JTAG multiplexing
- SPI multiplexing
- eMMC multiplexing
- Servers
- Data center switches & routers
- Wireless infrastructure
- PC & notebooks
- Building automation
- Grid infrastructure
- ePOS
- Appliances

## 3 Description

The TMUX1574 is a complementary metal-oxide semiconductor (CMOS) switch. The TMUX1574 offers 2:1 SPDT switch configuration with 4-channels. Wide operating supply of 1.5 V to 5.5 V allows for use in a broad array of applications from servers and communication equipment to industrial applications. The device supports bidirectional analog and digital signals on the source (SxA, SxB) and drain (Dx) pins and can pass signals above supply up to $V_{DD}$ x 2, with a maximum input/output voltage of 5.5 V.

Powered-off Protection up to 3.6 V on the signal path of the TMUX1574 provides isolation when the supply voltage is removed ($V_{DD}$ = 0 V). Without this protection feature, switches can back-power the supply rail through an internal ESD diode and cause potential damage to the system.

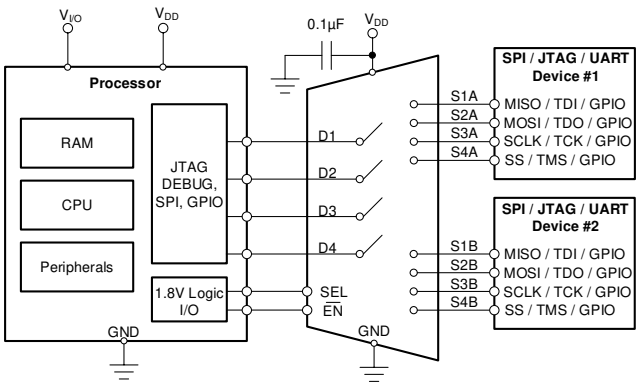
Fail-Safe Logic circuitry allows voltages on the logic control pins to be applied before the supply pin, protecting the device from potential damage. All control inputs have 1.8 V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Integrated pull down resistor on the logic pins removes external components to reduce system size and cost.

**Device Information(1)**

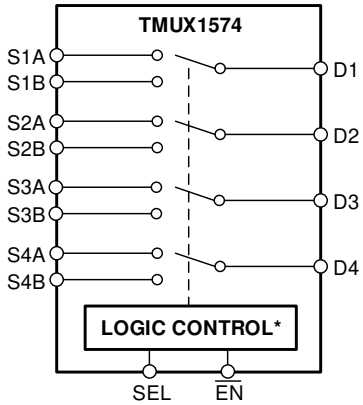
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TMUX1574 | TSSOP (16) | 5.00 mm × 4.40 mm |
| | UQFN (16) | 2.60 mm x 1.80 mm |
| | SOT-23-THIN (16) | 4.20 mm x 2.00 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

**Application Example**




**Block Diagram**




*Internal 6MΩ Pull-Down on Logic Pins

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (September 2019) to Revision C | Page |
|---|---|
| • Added prop delay and skew specs for DYY package | 8 |
| • Changed Figure 20 to include prop. delay and skew for DYY package | 12 |

| Changes from Revision A (December 2018) to Revision B | Page |
|---|---|
| • Added the SOT-23-THIN (DYY) package to the data sheet | 1 |
| • Added thermal information for DYY package. | 5 |

| Changes from Original (October 2018) to Revision A | Page |
|---|---|
| • Changed the document status From: *Advanced Information* To: *Production* data | 1 |


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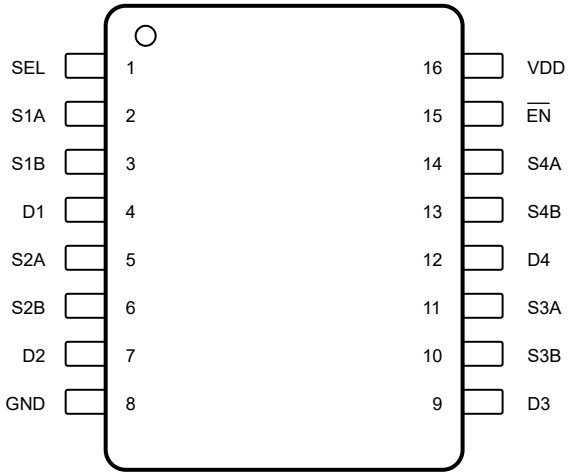
# 5 Pin Configuration and Functions

**PW Package**
**16-Pin TSSOP**
**Top View**

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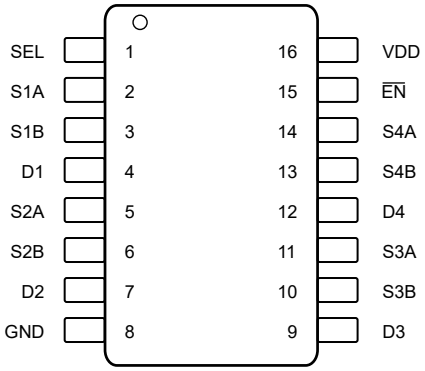
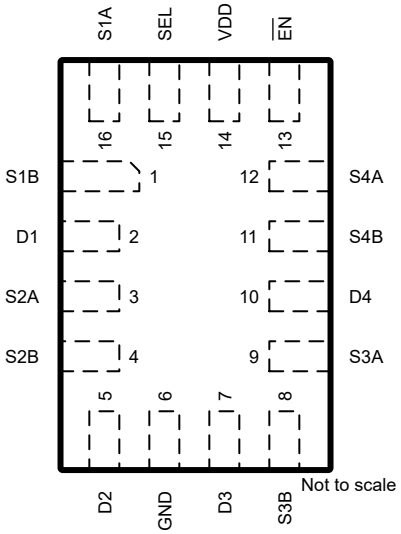
**DYY Package**
**16-Pin SOT-23-THIN**
**Top View**




**RSV Package**
**16-Pin UQFN**
**Top View**

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## Pin Functions

| PIN | | | TYPE(1) | DESCRIPTION(2) |
|---|---|---|---|---|
| NAME | TSSOP / SOT-23-THIN | UQFN | | |
| SEL | 1 | 15 | I | Select pin: controls state of switches according to Table 1. Internal 6 MΩ pull-down to GND. |
| S1A | 2 | 16 | I/O | Source pin 1A. Can be an input or output. |
| S1B | 3 | 1 | I/O | Source pin 1B. Can be an input or output. |
| D1 | 4 | 2 | I/O | Drain pin 1. Can be an input or output. |
| S2A | 5 | 3 | I/O | Source pin 2A. Can be an input or output. |
| S2B | 6 | 4 | I/O | Source pin 2B. Can be an input or output. |
| D2 | 7 | 5 | I/O | Drain pin 2. Can be an input or output. |
| GND | 8 | 6 | P | Ground (0 V) reference |
| D3 | 9 | 7 | I/O | Drain pin 3. Can be an input or output. |
| S3B | 10 | 8 | I/O | Source pin 3B. Can be an input or output. |
| S3A | 11 | 9 | I/O | Source pin 3A. Can be an input or output. |
| D4 | 12 | 10 | I/O | Drain pin 4. Can be an input or output. |
| S4B | 13 | 11 | I/O | Source pin 4B. Can be an input or output. |
| S4A | 14 | 12 | I/O | Source pin 4A. Can be an input or output. |
| $\overline{EN}$ | 15 | 13 | I | Active low enable: When this pin is high, all switches are turned off. When this pin is low, SEL pin controls the signal path selection. Internal 6 MΩ pull-down to GND. |
| VDD | 16 | 14 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{DD}$ and GND. |

(1) I = input, O = output, I/O = input and output, P = power
(2) Refer to Device Functional Modes for what to do with unused pins.


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# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).[1][2][3]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.5 | 6 | V |
| $V_{SEL}$ or $V_{EN}$ | Logic control input pin voltage (SEL or $\overline{EN}$) | –0.5 | 6 | V |
| $I_{SEL}$ or $I_{EN}$ | Logic control input pin current (SEL or $\overline{EN}$) | –30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain pin voltage | –0.5 | 6 | V |
| $I_S$ or $I_{D\ (CONT)}$ | Source and drain pin continuous current: (SxA, SxB, Dx) | –25 | 25 | mA |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.5 | 5.5 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pin), $V_{DD} \geq 1.5$ V[1] | 0 | $V_{DD}$ x 2 | V |
| $V_{S_off}$ or $V_{D_off}$ | Signal path input/output voltage (source or drain pin), $V_{DD} < 1.5$ V[2] | 0 | 3.6 | V |
| $V_{SEL}$ or $V_{EN}$ | Logic control input voltage ($\overline{EN}$, SEL) | 0 | 5.5 | V |
| $T_A$ | Ambient temperature | –40 | 125 | ºC |

(1) Device input and output can operate up to $V_{DD}$ x 2, with a maximum input and output voltage of 5.5 V.
(2) $V_{S_off}$ and $V_{D_off}$ refers to the voltage at the source or drain pins when supply is less than 1.5 V.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | DEVICE PW (TSSOP) 16 PINS | DEVICE DYY (SOT-23) 16 PINS | DEVICE RSV (UQFN) 16 PINS | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 117.4 | 123.0 | 129.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 47.9 | 70.5 | 69.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 63.7 | 50.4 | 58.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 6.9 | 5.0 | 3.6 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 63.1 | 50.3 | 56.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

$V_{DD}$ = 1.5 V to 5.5 V, GND = 0V, $T_A$ = –40°C to +125°C
Typical values are at $V_{DD}$ = 3.3 V, $T_A$ = 25°C, (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{DD}$ | Power supply voltage | | 1.5 | | 5.5 | V |
| $I_{DD}$ | Active supply current | $V_{SEL}$ = 0 V, 1.4V or $V_{DD}$<br>$V_S$ = 0 V to 5.5 V | | 40 | 68 | µA |
| $I_{DD_STANDBY}$ | Supply current when disabled | $V_{EN}$ = 1.4 V or $V_{DD}$<br>$V_S$ = 0 V to 5.5 V | | 7.5 | 15 | µA |
| **DC CHARACTERISTICS** | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$*2<br>$V_{S(max)}$ = 5.5 V<br>$I_{SD}$ = 8 mA<br>Refer to ON-State Resistance Figure | | 2 | 4.5 | Ω |
| $\Delta R_{ON}$ | On-resistance match between channels | $V_S$ = $V_{DD}$<br>$I_{SD}$ = 8 mA<br>Refer to ON-State Resistance Figure | | 0.07 | 0.28 | Ω |
| $R_{ON\ (FLAT)}$ | On-resistance flatness | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 8 mA<br>Refer to ON-State Resistance Figure | | 1 | 1.8 | Ω |
| $I_{POFF}$ | Powered-off I/O pin leakage current | $V_{DD}$ = 0 V<br>$V_S$ = 0 V to 3 V<br>$V_D$ = 0 V<br>$T_A$ = 25℃<br>Refer to Ipoff Leakage Figure | –10 | 0.01 | 10 | nA |
| $I_{POFF}$ | Powered-off I/O pin leakage current | $V_{DD}$ = 0 V<br>$V_S$ = 0 V to 3.6 V<br>$V_D$ = 0 V<br>Refer to Ipoff Leakage Figure | –2 | 0.01 | 2 | µA |
| $I_{S(OFF)}$<br>$I_{D(OFF)}$ | OFF leakage current | Switch Off<br>$V_D$ = 0.8*$V_{DD}$ / 0.2*$V_{DD}$<br>$V_S$ = 0.2*$V_{DD}$ / 0.8*$V_{DD}$<br>Refer to Off Leakage Figure | –100 | 0.03 | 100 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | ON leakage current | Switch On<br>$V_D$ = 0.8*$V_{DD}$ / 0.2*$V_{DD}$, S pins floating<br>or<br>$V_S$ = 0.8*$V_{DD}$ / 0.2*$V_{DD}$, D pins floating<br>Refer to On Leakage Figure | –50 | 0.01 | 50 | nA |
| **LOGIC INPUTS** | | | | | | |
| $V_{IH}$ | Input logic high | | 1.2 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | 0 | | 0.45 | V |
| $I_{IH}$ | Input high leakage current | $V_{SEL}$ = 1.8 V, $V_{DD}$ | | 1 | ±2 | µA |
| $I_{IL}$ | Input low leakage current | $V_{SEL}$ = 0 V | | 0.2 | ±2 | µA |
| $R_{PD}$ | Internal pull-down resistor on logic pins | | | 6 | | MΩ |
| $C_I$ | Logic input capacitance | $V_{SEL}$ = 0 V, 1.8 V or $V_{DD}$<br>f = 1 MHz | | 3 | | pF |


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## 6.6 Dynamic Characteristics

$V_{DD}$ = 1.5 V to 5.5 V, GND = 0V, $T_A$ = –40°C to +125°C
Typical values are at $V_{DD}$ = 3.3 V, $T_A$ = 25°C, (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{OFF}$ | Source and drain off capacitance | $V_S$ = 2.5 V<br>$V_{SEL}$= 0 V<br>f = 1 MHz<br>Refer to Capacitance Figure | Switch OFF | | 3.5 | 6 | pF |
| $C_{ON}$ | Source and drain on capacitance | $V_S$ = 2.5 V<br>$V_{SEL}$= 0 V<br>f = 1 MHz<br>Refer to Capacitance Figure | Switch ON | | 7.5 | 12 | pF |
| $Q_C$ | Charge Injection | $V_S$ = $V_{DD}$/2<br>$R_S$ = 0 Ω, $C_L$ =1 nF<br>Refer to Charge Injection Figure | Switch ON | | 3.5 | | pC |
| $O_{ISO}$ | Off isolation | $R_L$ = 50 Ω<br>f = 100 kHz<br>Refer to Off Isolation Figure | Switch OFF | | –90 | | dB |
| | | $R_L$ = 50 Ω<br>f = 1 MHz<br>Refer to Off Isolation Figure | Switch OFF | | –75 | | dB |
| $X_{TALK}$ | Channel to Channel crosstalk | $R_L$ = 50 Ω<br>f = 100 kHz<br>Refer to Crosstalk Figure | Switch ON | | –90 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω<br>Refer to Bandwidth Figure | Switch ON | | 2 | | GHz |
| $I_{LOSS}$ | Insertion loss | $R_L$ = 50 Ω<br>f = 1 MHz<br>Refer to Bandwidth Figure | Switch ON | | –0.12 | | dB |

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## 6.7 Timing Requirements

$V_{DD}$ = 1.5 V to 5.5 V, GND = 0V, $T_A$ = –40°C to +125°C
Typical values are at $V_{DD}$ = 3.3 V, $T_A$ = 25°C, (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_{DD}$ = 2.5 V to 5.5 V<br>$V_S$ = $V_{DD}$<br>$R_L$ = 200 Ω, $C_L$ = 15pF<br>Refer to Transition Timing Figure | | 160 | 350 | ns |
| $t_{TRAN}$ | Transition time from control input | $V_{DD}$ < 2.5 V<br>$V_S$ = $V_{DD}$<br>$R_L$ = 200 Ω, $C_L$ = 15pF<br>Refer to Transition Timing Figure | | 180 | 580 | ns |
| $t_{ON(EN)}$ | Device turn on time from enable pin | $V_S$ = $V_{DD}$<br>$R_L$ = 200 Ω, $C_L$ = 15pF<br>Refer to Ton(EN) & Toff(EN) Figure | | 12 | 35 | µs |
| $t_{OFF(EN)}$ | Device turn off time from enable pin | $V_S$ = $V_{DD}$<br>$R_L$ = 200 Ω, $C_L$ = 15pF<br>Refer to Ton(EN) & Toff(EN) Figure | | 50 | 95 | ns |
| $t_{ON(VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_S$ = 3.6 V<br>$V_{DD}$ rise time = 1us<br>$R_L$ = 200 Ω, $C_L$ = 15pF<br>Refer to Ton(vdd) & Toff(vdd) Figure | | 20 | 60 | µs |
| $t_{OFF(VDD)}$ | Device turn off time ($V_{DD}$ to output) | $V_S$ = 3.6 V<br>$V_{DD}$ fall time = 1us<br>$R_L$ = 200 Ω, $C_L$ = 15pF<br>Refer to Ton(vdd) & Toff(vdd) Figure | | 1.2 | 2.7 | µs |
| $t_{OPEN\ (BBM)}$ | Break before make time | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15pF<br>Refer to Topen(BBM) Figure | 0.5 | | | ns |
| $t_{SK(P)}$ | Inter - channel skew - QFN (RSV) | Refer to Tsk Figure | | 5 | | ps |
| $t_{SK(P)}$ | Inter - channel skew - DYY (SOT-23) | Refer to Tsk Figure | | 9 | | ps |
| $t_{SK(P)}$ | Inter - channel skew - TSSOP (PW) | Refer to Tsk Figure | | 18 | | ps |
| $t_{PD}$ | Propagation delay - QFN (RSV) | Refer to Tpd Figure | | 50 | | ps |
| $t_{PD}$ | Propagation delay - DYY (SOT-23) | Refer to Tpd Figure | | 75 | | ps |
| $t_{PD}$ | Propagation delay - TSSOP (PW) | Refer to Tpd Figure | | 95 | | ps |


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## 6.8 Typical Characteristics

At $T_A$ = 25°C, $V_{DD}$ = 5 V (unless otherwise noted).

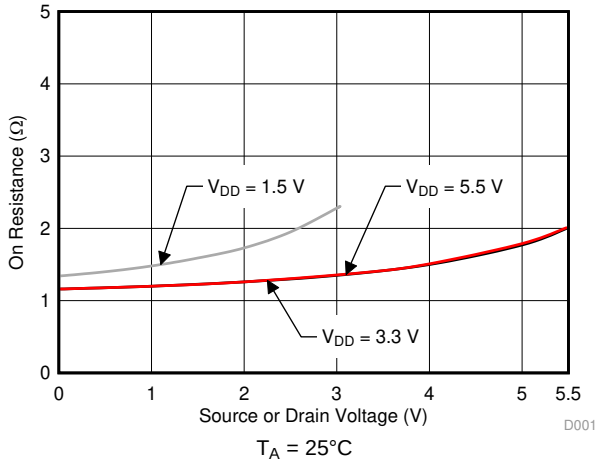



**Figure 1. On-Resistance vs Source or Drain Voltage**

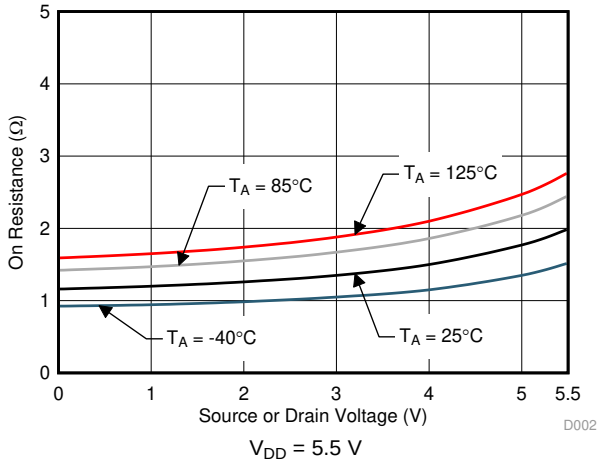



**Figure 2. On-Resistance vs Source or Drain Voltage**

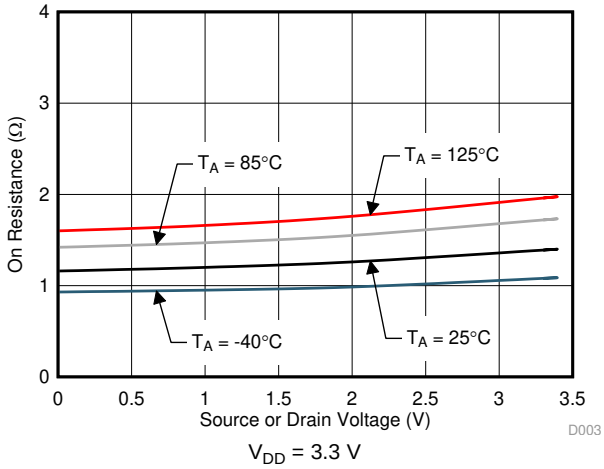



**Figure 3. On-Resistance vs Source or Drain Voltage**

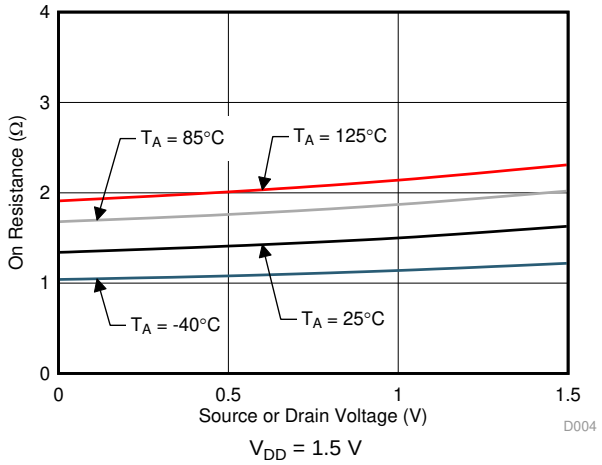



**Figure 4. On-Resistance vs Source or Drain Voltage**

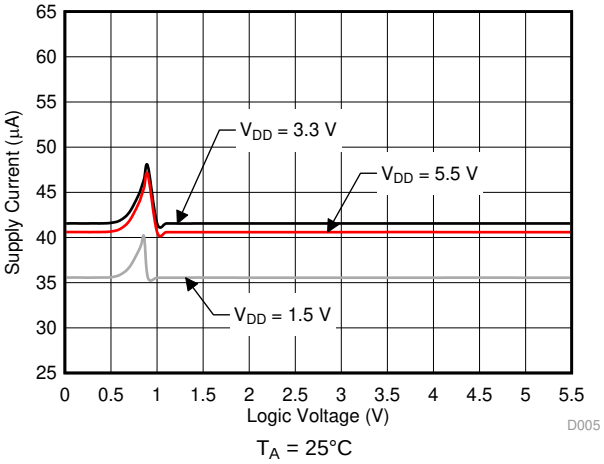



**Figure 5. Supply Current vs Logic Voltage**

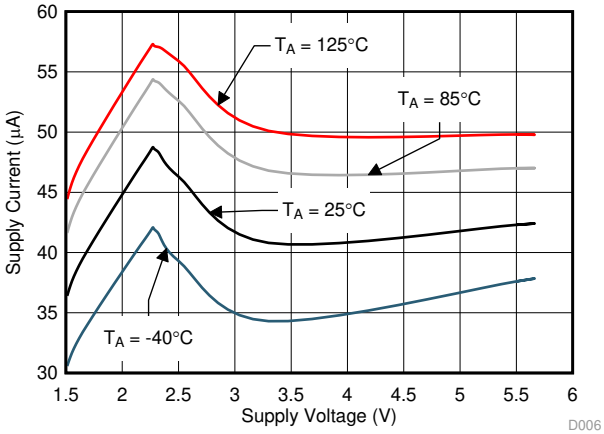
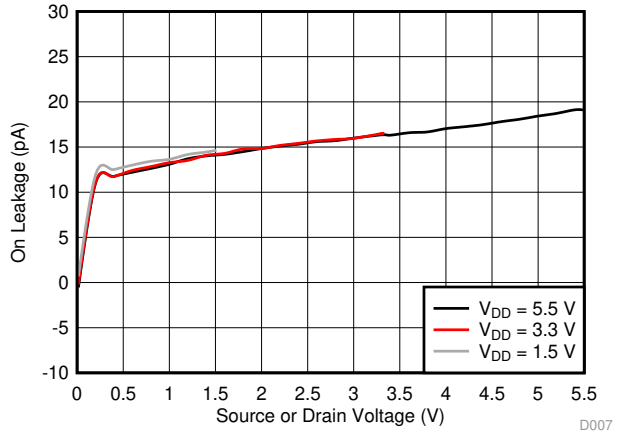



**Figure 6. Supply Current vs Supply Voltage**

## Typical Characteristics (continued)




$T_A$ = 25°C

**Figure 7. On-Leakage vs Source or Drain Voltage**

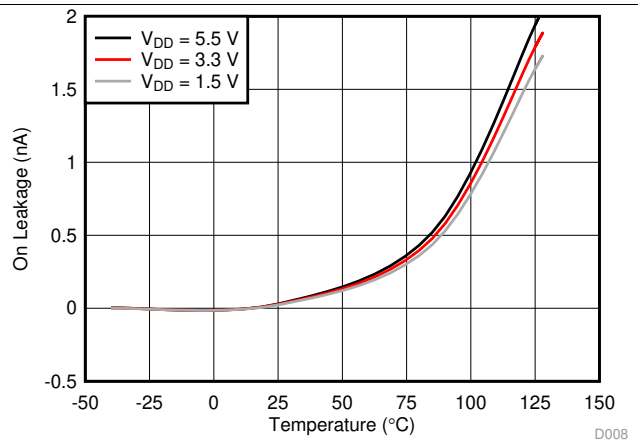
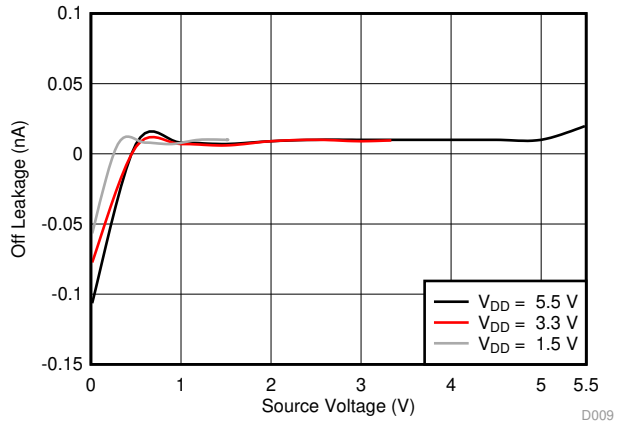



**Figure 8. On-Leakage vs Temperature**




$T_A$ = 25°C

**Figure 9. Off-Leakage vs Source or Drain Voltage**

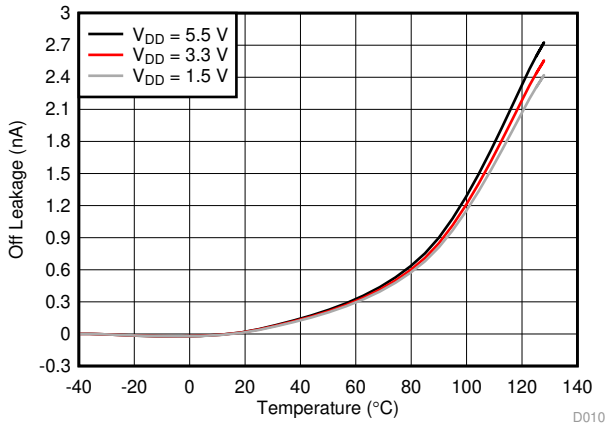
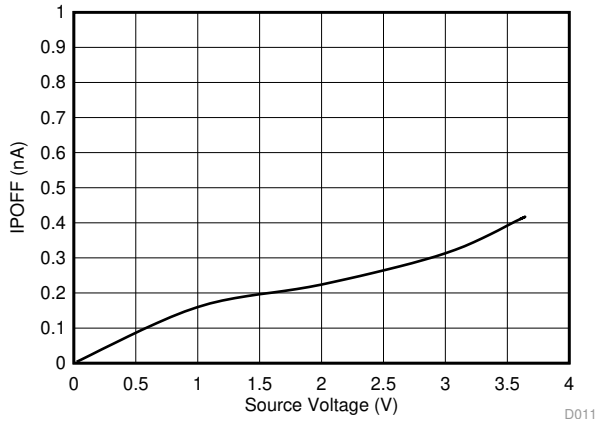
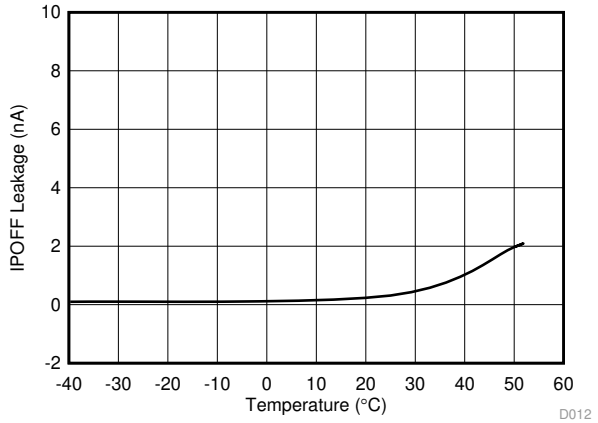



**Figure 10. Off-Leakage vs Temperature**




$T_A$ = 25°C

**Figure 11. IPOFF Leakage vs Source or Drain Voltage**




$V_{Source}$ = 3 V

**Figure 12. IPOFF Leakage vs Temperature**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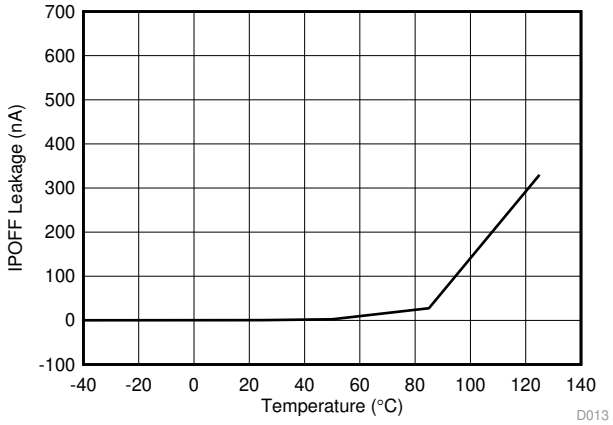
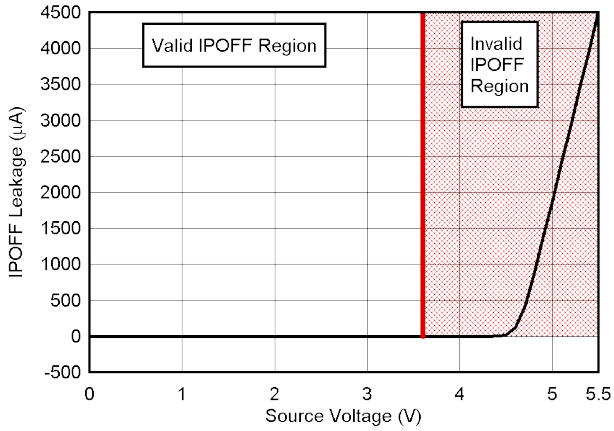
## Typical Characteristics (continued)



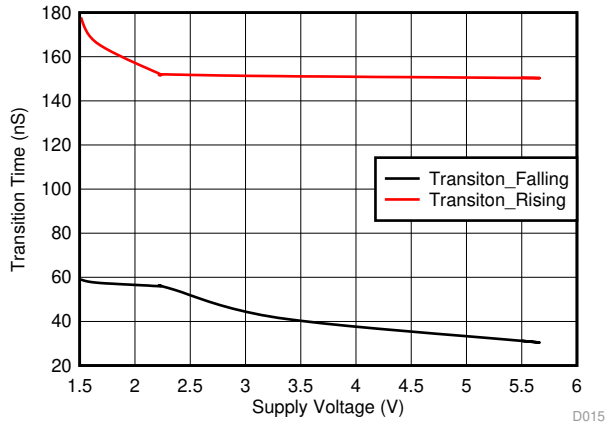

$V_{Source}$ = 3.6 V
$V_{Drain}$ = 0 V

**Figure 13. IPOFF Leakage vs Temperature**



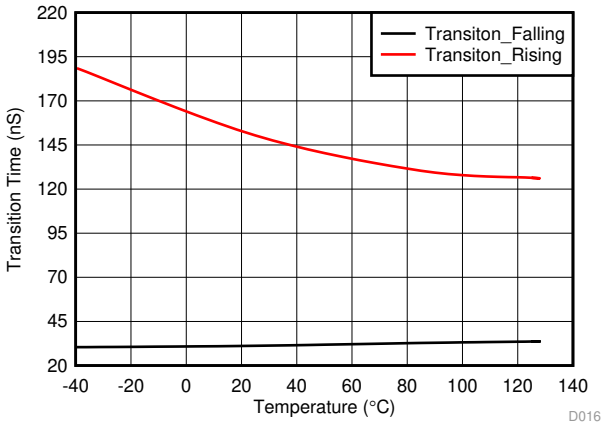

$T_A$ = 25°C
$R_L$ = 200 Ω

**Figure 14. IPOFF Leakage vs Source or Drain Voltage**



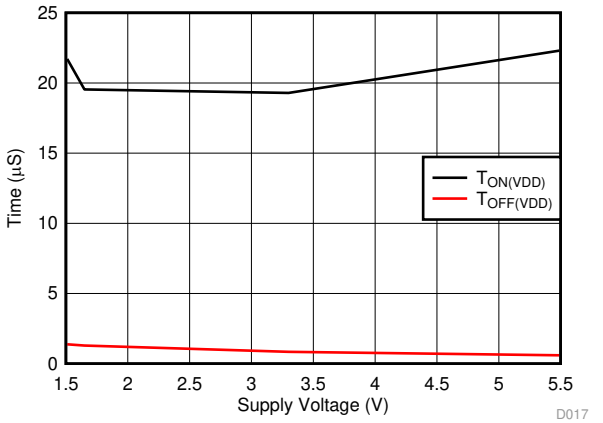

$T_A$ = 25°C

**Figure 15. $T_{TRANSITION}$ vs Supply Voltage**



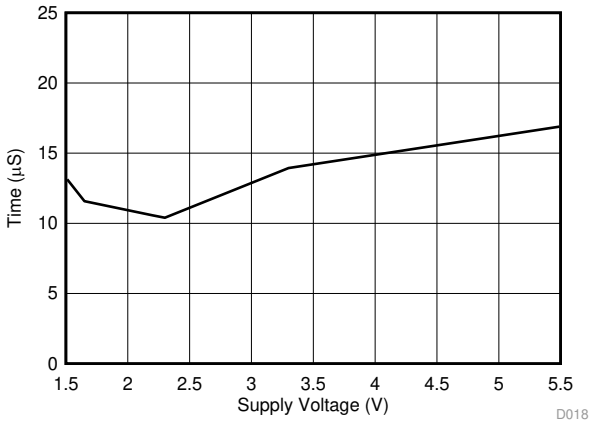

$V_{DD}$ = 5.5 V

**Figure 16. $T_{TRANSITION}$ vs Temperature**




$T_A$ = 25°C

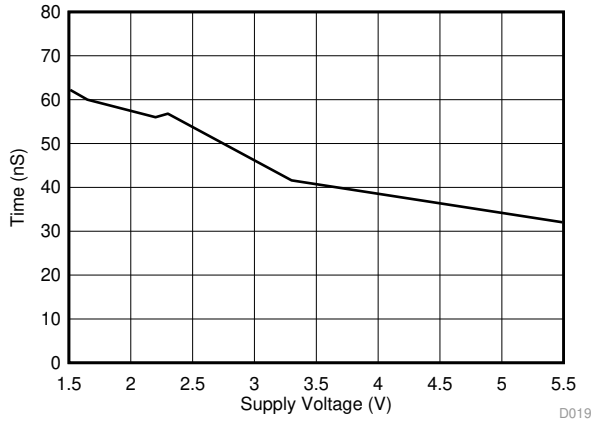
**Figure 17. $T_{ON\ (VDD)}$ and $T_{OFF\ (VDD)}$ vs Supply Voltage**




$T_A$ = 25°C

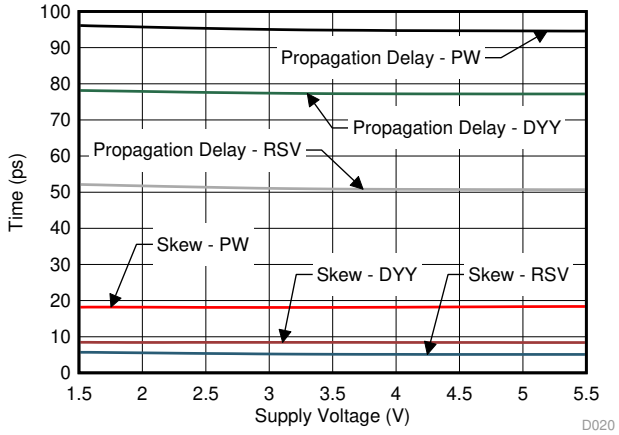
**Figure 18. $T_{ON\ (EN)}$ vs Supply Voltage**

## Typical Characteristics (continued)



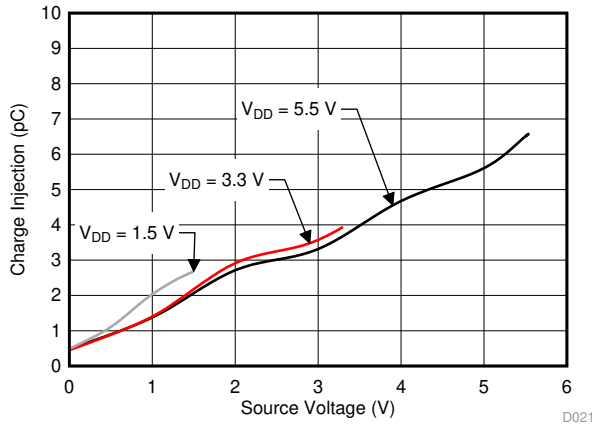

$T_A$ = 25°C

**Figure 19. $T_{OFF\ (EN)}$ vs Supply Voltage**



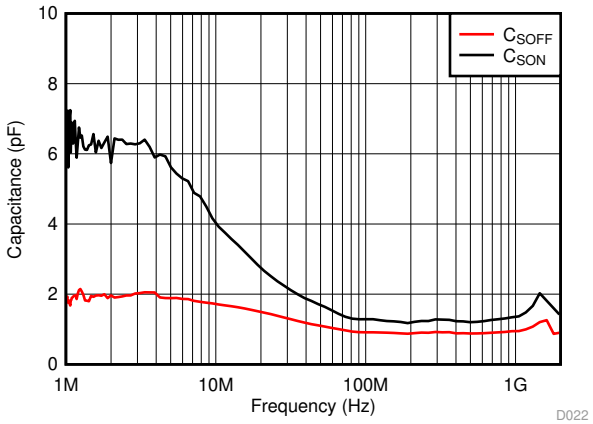

$T_A$ = 25°C

**Figure 20. Skew and Propagation Delay vs Supply Voltage**



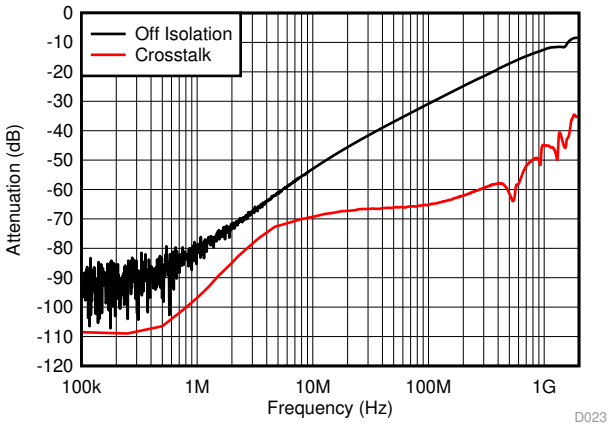

$T_A$ = 25°C

**Figure 21. Charge Injection vs Source Voltage**



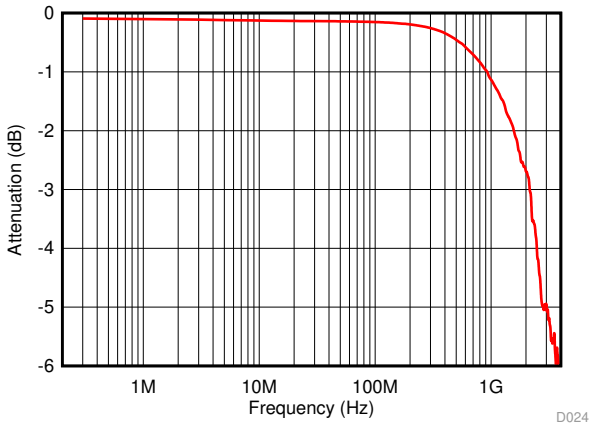

$T_A$ = 25°C
$V_{DD}$ = 1.5 V to 5.5 V

**Figure 22. Capacitance vs Frequency**




$T_A$ = 25°C
$V_{DD}$ = 3.3 V

**Figure 23. Off Isolation and Crosstalk vs Frequency**




$T_A$ = 25°C
$V_{DD}$ = 1.5 V to 5.5 V

**Figure 24. On-Response vs Frequency**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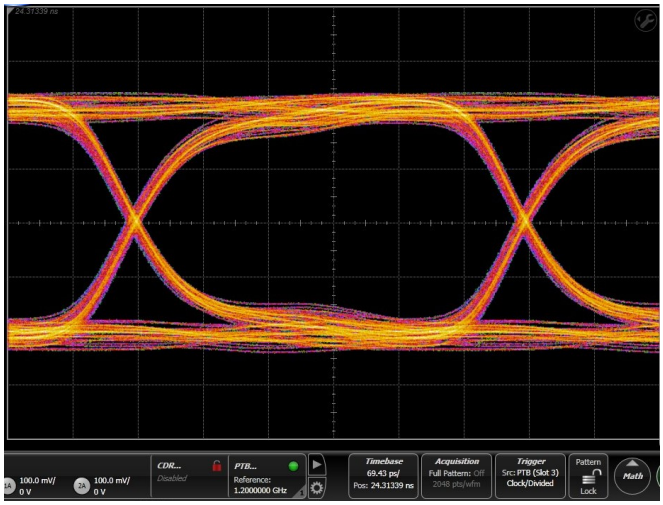
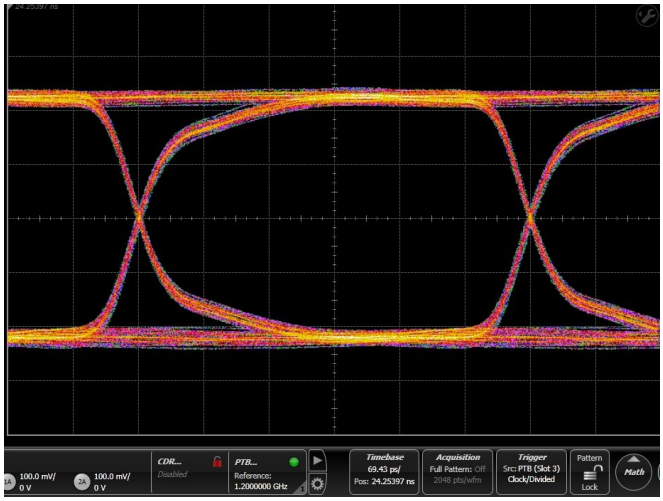
### 6.8.1 Eye Diagrams




$T_A$ = 25°C
Bias = 1.5 V
50 Ω Termination

**Figure 25. Eye Pattern: 2.4 Gbps**




$T_A$ = 25°C
Bias = 1.5 V
50 Ω Termination

**Figure 26. Eye Pattern: 2.4 Gbps Through Path**

# 7 Parameter Measurement Information

## 7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. The measurement setup used to measure $R_{ON}$ is shown in Figure 27. Voltage (V) and current ($I_{SD}$) are measured using this setup, and $R_{ON}$ is computed as shown below with $R_{ON} = V / I_{SD}$:

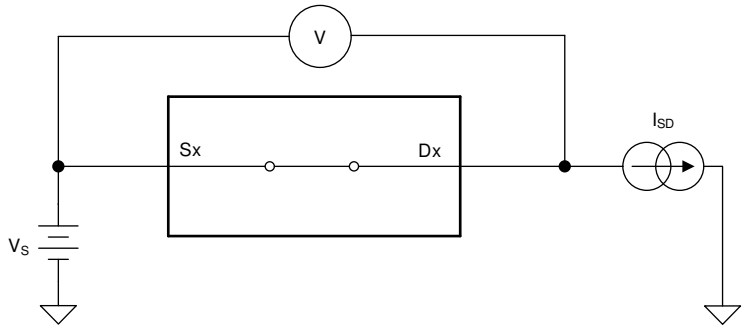



**Figure 27. On-Resistance Measurement Setup**

## 7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S\ (OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D\ (OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 28.

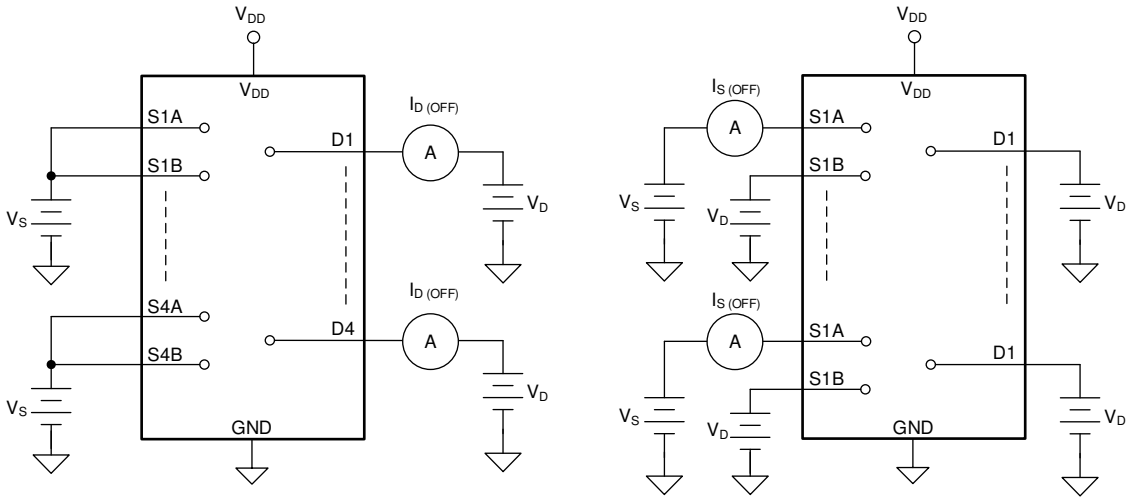



**Figure 28. Off-Leakage Measurement Setup**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## 7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S\ (ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D\ (ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 29 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

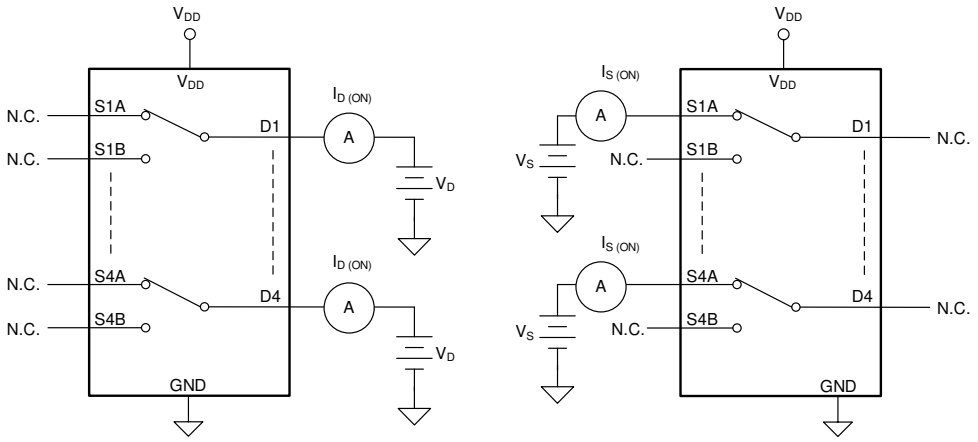


**Figure 29. On-Leakage Measurement Setup**

## 7.4 $I_{POFF}$ Leakage Current

$I_{POFF}$ leakage current is defined as the leakage current flowing into or out of the source pin when the device is powered off. This current is denoted by the symbol $I_{POFF}$.

The setup used to measure both $I_{POFF}$ leakage current is shown in Figure 30.

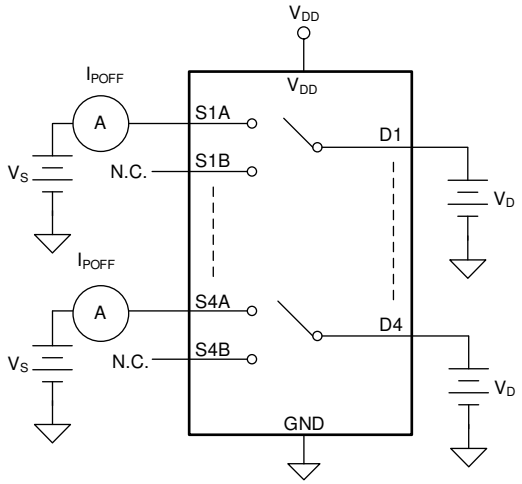


**Figure 30. $I_{POFF}$ Leakage Measurement Setup**

## 7.5 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the select signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. The time constant from the load resistance and load capacitance can be added to the transition time to calculate system level timing. Figure 31 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

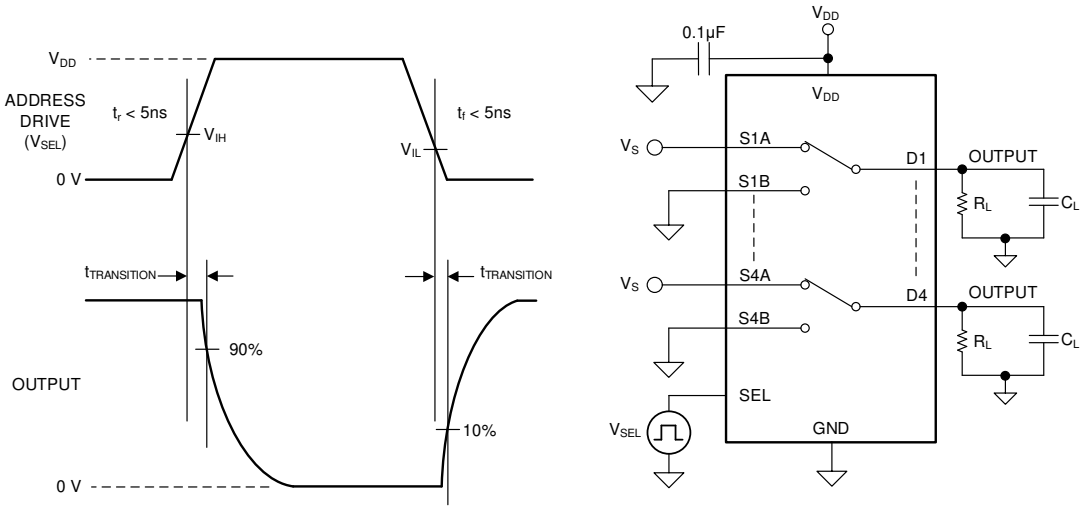


**Figure 31. Transition-Time Measurement Setup**

## 7.6 $t_{ON\ (EN)}$ and $t_{OFF\ (EN)}$ Time

The $t_{ON\ (EN)}$ time is defined as the time taken by the output of the device to rise to 90% after the enable has fallen past the logic threshold. The 90% measurement is used to provide the timing of the device being enabled in the system. Figure 32 shows the setup used to measure the enable time, denoted by the symbol $t_{ON\ (EN)}$.

The $t_{OFF\ (EN)}$ time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the logic threshold. The 90% measurement is used to provide the timing of the device being disabled in the system. Figure 32 shows the setup used to measure enable time, denoted by the symbol $t_{OFF\ (EN)}$.

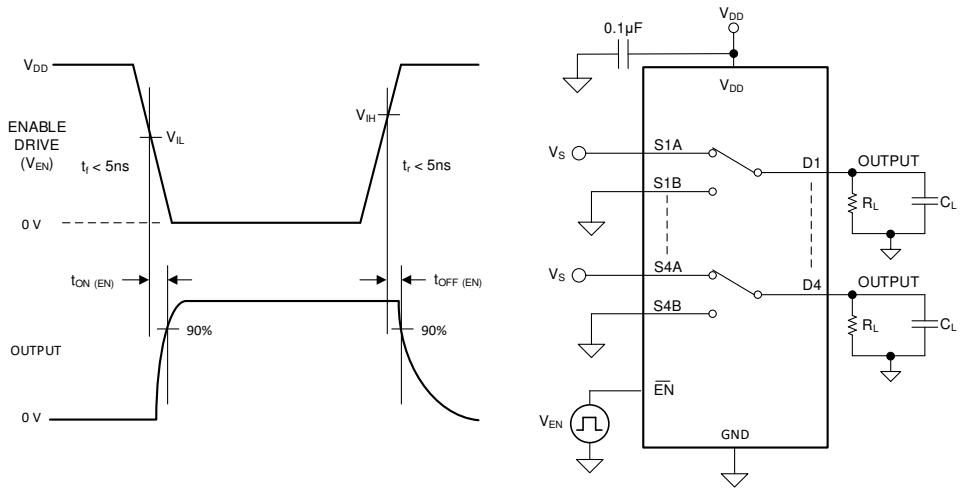


**Figure 32. $t_{ON\ (EN)}$ and $t_{OFF\ (EN)}$ Time Measurement Setup**


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## 7.7 $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 33 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

the $t_{OFF\ (VDD)}$ time is defined as the time taken by the output of the device to fall to 90% after the supply has fallen past the supply threshold. The 90% measurement is used to provide the timing of the device turning off in the system. Figure 33 shows the setup used to measure turn off time, denoted by the symbol $t_{OFF\ (VDD)}$.

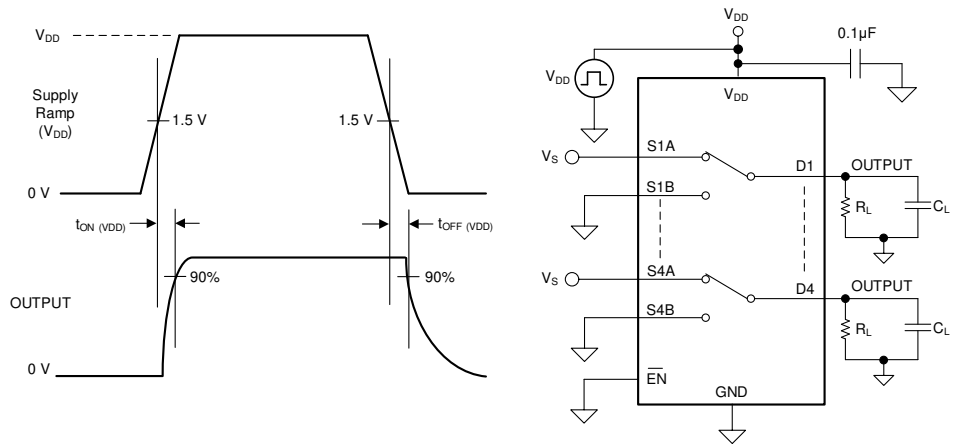


**Figure 33. $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$Time Measurement Setup**

## 7.8 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 34 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

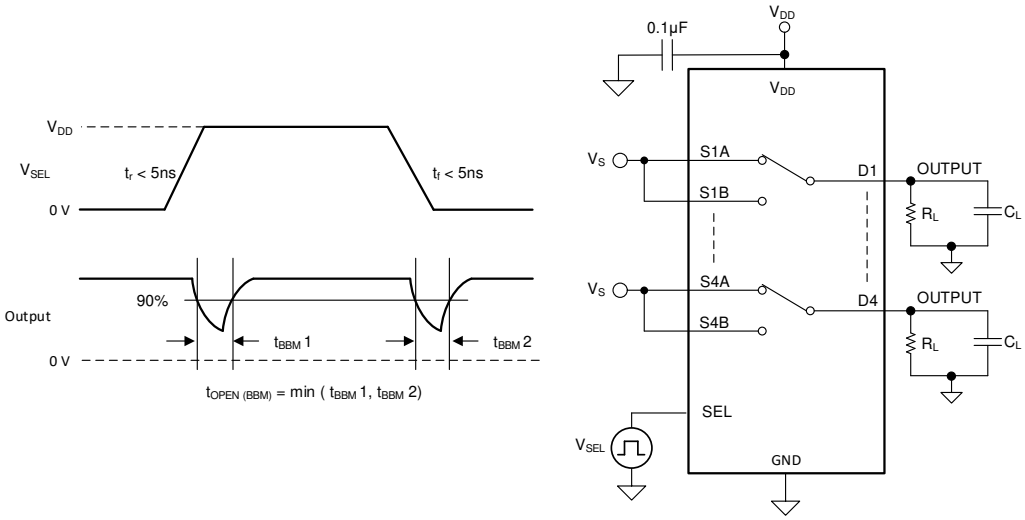


**Figure 34. Break-Before-Make Delay Measurement Setup**

## 7.9 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 35 shows the setup used to measure propagation delay, denoted by the symbol $t_{PD}$.

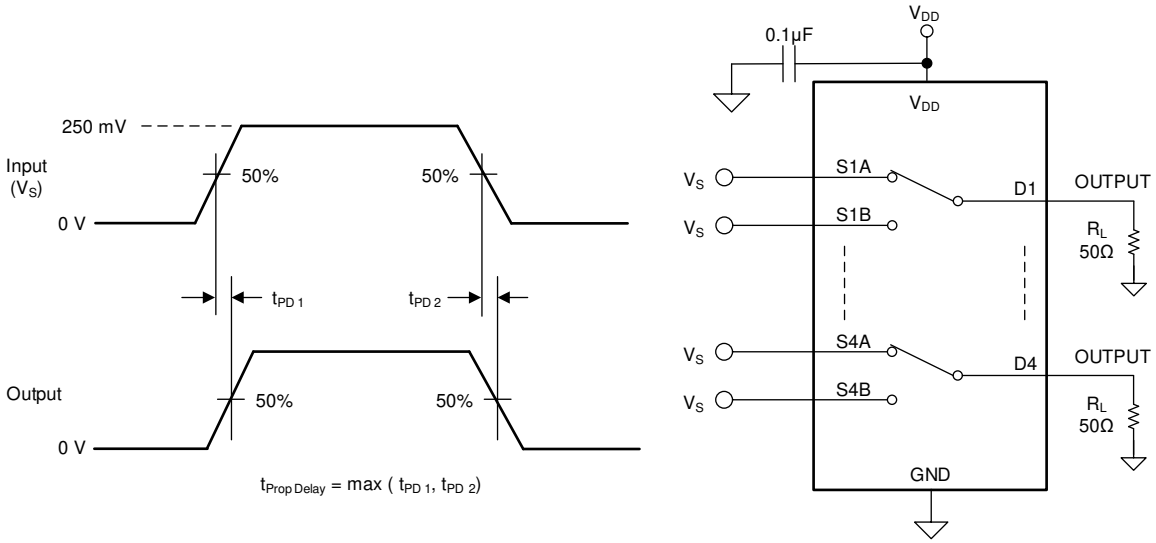


**Figure 35. Propagation Delay Measurement Setup**

## 7.10 Skew

Skew is defined as the difference between propagation delays of any two outputs of the same device. The skew measurement is taken from the output of one channel rising or falling past 50% to a second channel rising or falling past the 50% threshold when the input signals are switched at the same time. Figure 36 shows the setup used to measure skew, denoted by the symbol $t_{SK}$.

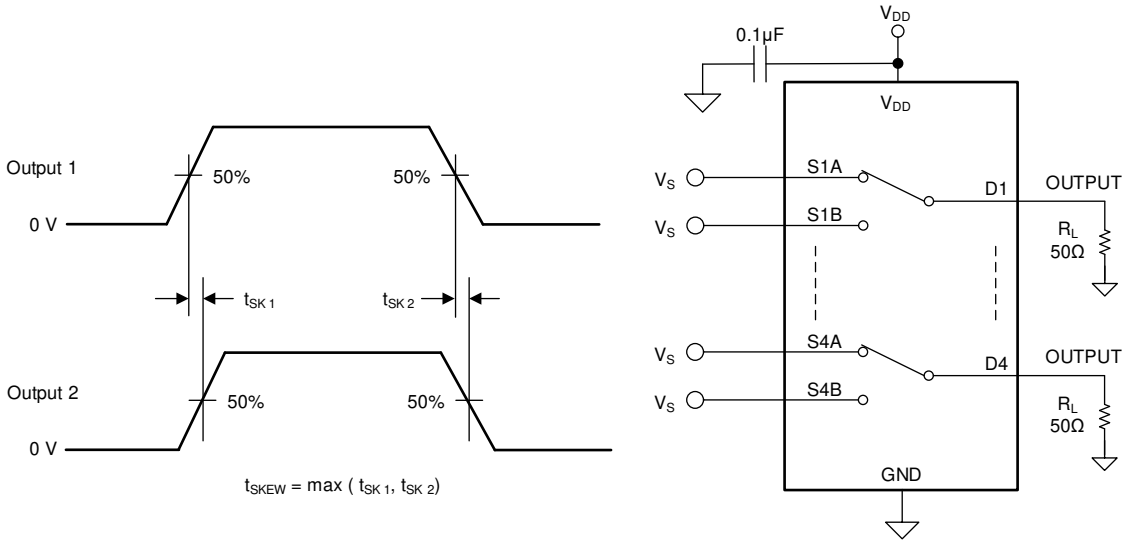


**Figure 36. Skew Measurement Setup**


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## 7.11 Charge Injection

The amount of charge injected into the source or drain of the device during the falling or rising edge of the gate signal is known as charge injection, and is denoted by the symbol $Q_C$. Figure 37 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

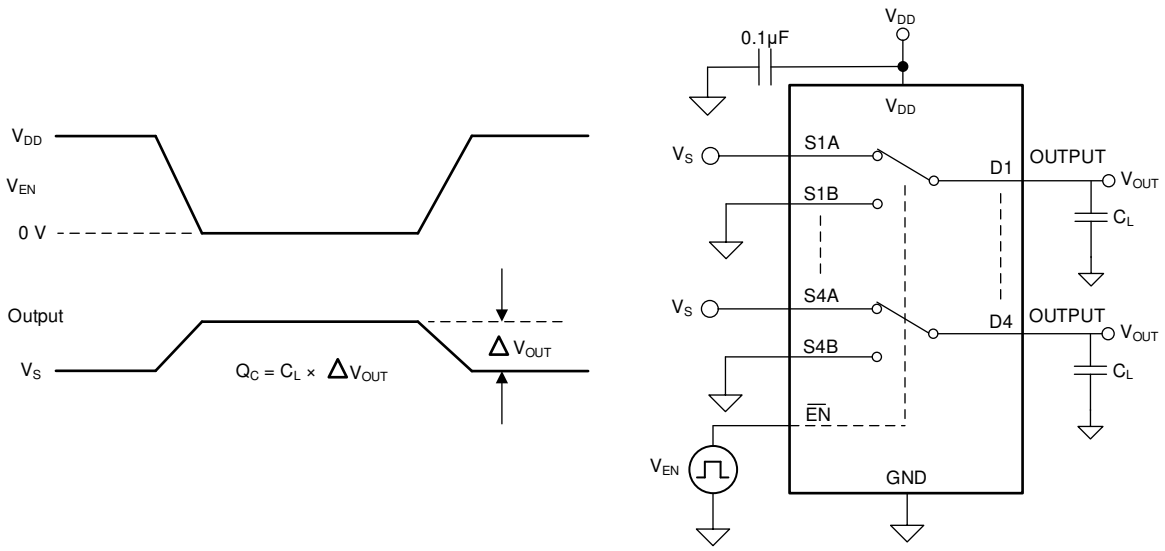


**Figure 37. Charge-Injection Measurement Setup**

## 7.12 Capacitance

The parasitic capacitance of the device is captured at the source (Sx), drain (Dx), and select (SELx) pins. The capacitance is measured in both the on and off state and is denoted by the symbol $C_{ON}$ and $C_{OFF}$. Figure 38 shows the setup used to measure capacitance.

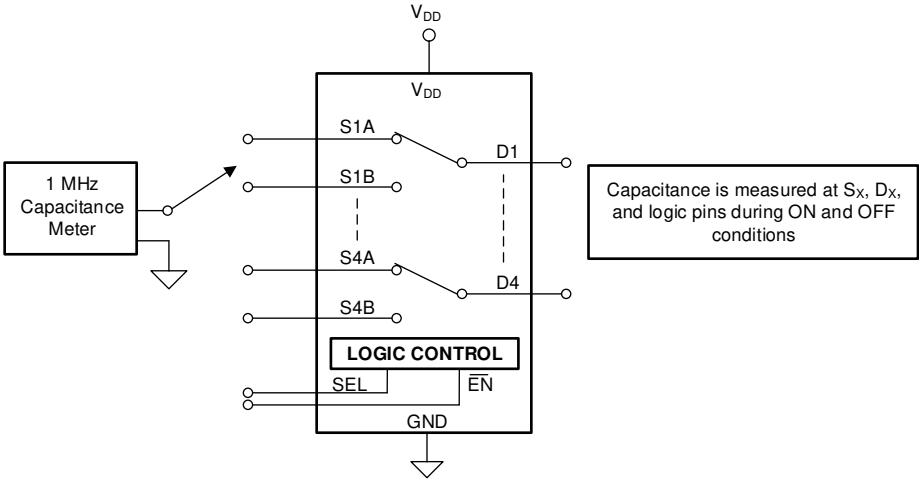


**Figure 38. Capacitance Measurement Setup**

## 7.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, $Z_0$, for the measurement is 50 Ω. Figure 39 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

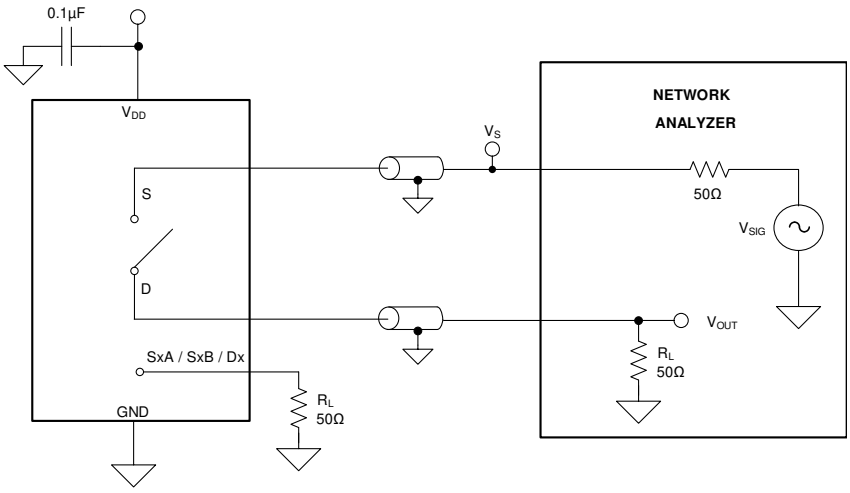


**Figure 39. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{1}$$

## 7.14 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, $Z_0$, for the measurement is 50 Ω. Figure 40 shows the setup used to measure, and the equation used to compute crosstalk.

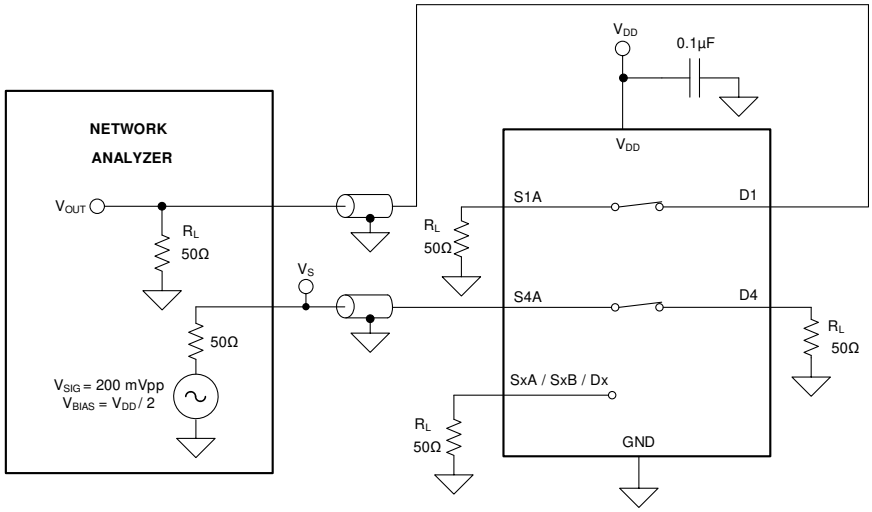


**Figure 40. Channel-to-Channel Crosstalk Measurement Setup**

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{2}$$


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## 7.15 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, $Z_0$, for the measurement is 50 Ω. Figure 41 shows the setup used to measure bandwidth.

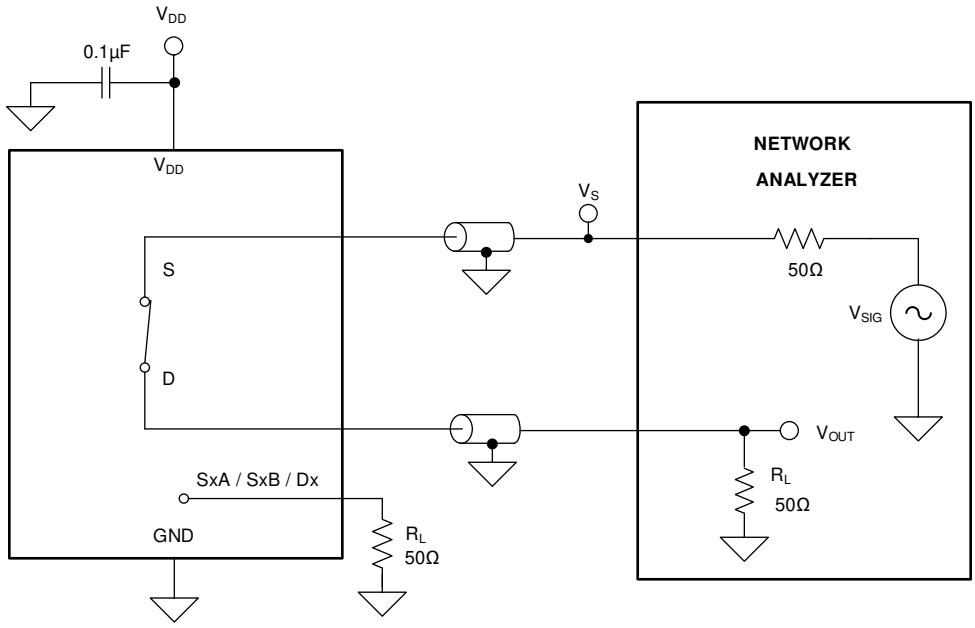



**Figure 41. Bandwidth Measurement Setup**

$$Attenuation = 20 \times Log\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

# 8 Detailed Description

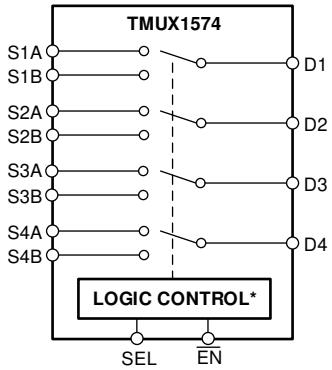
## 8.1 Overview

The TMUX1574 is a high speed 2:1 (SPDT) 4-ch. switch with powered-off protection up to 3.6 V. Wide operating supply of 1.5 V to 5.5 V allows for use in a wide array of applications from servers and communication equipment to industrial applications. The device supports bidirectional analog and digital signals on the source (SxA, SxB) and drain (Dx) pins. The wide bandwidth of this switch allows little or no attenuation of high-speed signals at the outputs to pass with minimum edge and phase distortion as well as propagation delay.

The enable ($\overline{EN}$) pin is an active-low logic pin that controls the connection between the source (SxA, SxB) and drain (Dx) pins of the device. The select pin (SEL) controls the state of all four channels of the TMUX1574 and determines which source pin is connected to the drain. Fail-Safe Logic circuitry allows voltages on the logic control pins to be applied before the supply pin, protecting the device from potential damage. All logic control inputs have 1.8V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

Powered-off protection up to 3.6 V on the signal path of the TMUX1574 provides isolation when the supply voltage is removed ($V_{DD}$ = 0 V). Without this protection feature, the system can back-power the supply rail through an internal ESD diode and cause potential damage to the system.

## 8.2 Functional Block Diagram




*Internal 6MΩ Pull-Down on Logic Pins

## 8.3 Feature Description

### 8.3.1 Bidirectional Operation

The TMUX1574 conducts equally well from source (SxA, SxB) to drain (Dx) or from drain (Dx) to source (SxA, SxB). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

### 8.3.2 Beyond Supply Operation

When the TMUX1574 is powered from 1.5 V to 5.5 V, the valid signal path input/output voltage ranges from GND to $V_{DD}$ x 2, with a maximum input/output voltage of 5.5 V.

Example 1: If the TMUX1574 is powered at 1.5V, the signal range is 0 V to 3 V.

Example 2: If the TMUX1574 is powered at 3V, the signal range is 0 V to 5.5 V.

Example 3: If the TMUX1574 is powered at 5.5V, the signal range is 0 V to 5.5 V.

Other voltage levels not mentioned in the examples support Beyond Supply Operation as long as the supply voltage falls within the recommended operation conditions of 1.5 V to 5.5 V.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## Feature Description (continued)

### 8.3.3 1.8 V Logic Compatible Inputs

The TMUX1574 has 1.8-V logic compatible control inputs. Regardless of the $V_{DD}$ voltage, the control input thresholds remain fixed, allowing a 1.8-V processor GPIO to control the TMUX1574 without the need for an external translator. This saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches.*

### 8.3.4 Powered-off Protection

Powered-off protection up to 3.6 V on the signal path of the TMUX1574 provides isolation when the supply voltage is removed ($V_{DD}$ = 0 V). When the TMUX1574 is powered-off, the I/Os of the device remain in a high-Z state. Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path. The device performance remains within the leakage performance mentioned in the Electrical Specifications. For more information on powered-off protection, refer to *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

### 8.3.5 Fail-Safe Logic

The TMUX1574 has Fail-Safe Logic on the control input pins (SELx) which allows for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1574 to be ramped to 5.5 V while $V_{DD}$ = 0 V. Additionally, the feature enables operation of the TMUX1574 with $V_{DD}$ = 1.5 V while allowing the select pins to interface with a logic level of another device up to 5.5 V.

### 8.3.6 Low Capacitance

The TMUX1574 has very low capacitance in both the ON and OFF states on the source and drain pins. Low capacitance helps to reduce large overshoots and ringing of an amplifier circuit when the switch is connected to the feedback network. Additionally, low capacitance improves system settling time by reducing the switch time constant formed by the On-resistance and On-capacitance. For more information on the benefits of low capacitance refer to *Improve Stability Issues with Low $C_{ON}$ Multiplexers.*

### 8.3.7 Integrated Pull-Down Resistors

The TMUX1574 has internal weak pull-down resistors (6 MΩ) to GND to ensure the logic pins are not left floating. This feature integrates up to four external components and reduces system size and cost.

## 8.4 Device Functional Modes

The enable ($\overline{EN}$) pin is an active-low logic pin that controls the connection between the source (SxA, SxB) and drain (Dx) pins of the device. When the enable pin is pulled high, all switches are turned off. When the enable is pulled low, the select pin controls the signal path selection. The select pin (SEL) controls the state of all four channels of the TMUX1574 and determines which source pin is connected to the drain pins. When the select pin is pulled low, the SxA pin conducts to the corresponding Dx pins. When the select pin is pulled high, the SxB pin conducts to the corresponding Dx pins. The TMUX1574 logic pins have internal weak pull-down resistors (6 MΩ) to GND so that it powers-on in a known state.

The TMUX1574 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or $V_{DD}$ in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (SxA, SxB, or Dx) should be connected to GND.

## 8.5 Truth Tables

**Table 1. TMUX1574 Truth Table**

| INPUTS | | Selected Source Pins Connected To Drain Pins (Dx) |
|---|---|---|
| $\overline{EN}$ | SEL | |
| 0 | 0 | S1A connected to D1<br>S2A connected to D2<br>S3A connected to D3<br>S4A connected to D4 |
| 0 | 1 | S1B connected to D1<br>S2B connected to D2<br>S3B connected to D3<br>S4B connected to D4 |
| 1 | X[(1)] | Hi-Z (OFF) |

(1) X denotes *don't care*.


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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The TMUX15xx family offers high-speed system performance across a wide operating supply (1.5 V to 5.5 V) and operating temperature (-40°C to +125°C). The TMUX1574 supports a number of features that improve system performance such as 1.8 V logic compatibility, supports input voltages beyond supply, Fail-Safe Logic, and Powered-off Protection up to 3.6 V. These features make the TMUX15xx a family of protection multiplexers and switches that can reduce system complexity, board size, and overall system cost.

## 9.2 Typical Application

Common applications that require the features of the TMUX1574 include multiplexing various protocols from a possessor or MCU such as SPI, JTAG, or standard GPIO signals. The TMUX1574 provides superior isolation performance when the device is powered. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications. The example shown in Figure 42 illustrates the use of the TMUX1574 to multiplex an SPI bus to multiple flash memory devices.

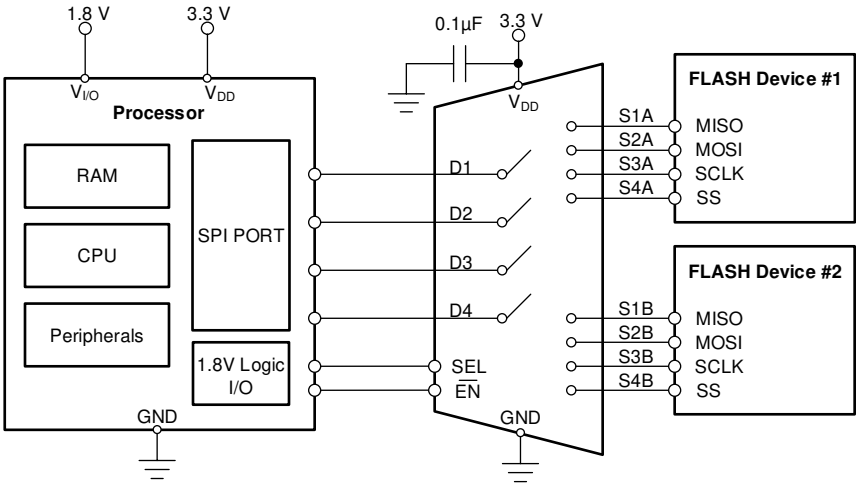


**Figure 42. Multiplexing Flash Memory**

### 9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

**Table 2. Design Parameters**

| PARAMETERS | VALUES |
|---|---|
| Supply ($V_{DD}$) | 3.3 V |
| Input / Output signal range | 0 V to 3.3 V |
| Control logic thresholds | 1.8 V compatible |

### 9.2.2 Detailed Design Procedure

The TMUX1574 can be operated without any external components except for the supply decoupling capacitors. The TMUX1574 has internal weak pull-down resistors (6 MΩ) to GND so that it powers-on with the switches in a known state. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX1574 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. This example can also utilize the Powered-off Protection feature and the inputs can range from 0 V to 3.6 V when $V_{DD}$ = 0 V. The max continuous current can be 25 mA. Due to the voltage range and high speed capability, the TMUX1574 example is suitable for use in SPI, JTAG, and I2S applications. Refer to *Enabling SPI-based flash memory expansion by using multiplexers* for more information on using switches and multiplexers for SPI protocol expansion.

### 9.2.3 Application Curves

Two important specifications when using a switch or multiplexer to pass signals are the device propagation delay and skew.

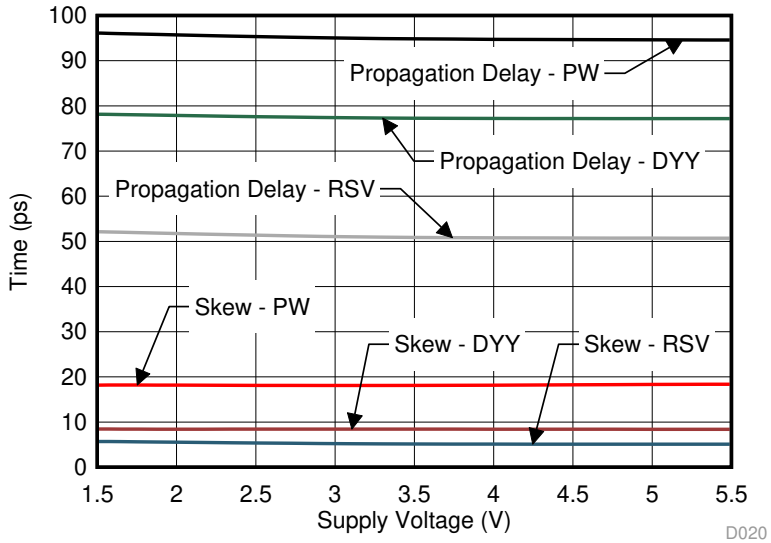


**Figure 43. Propagation Delay and Skew Measurement**

## 10 Power Supply Recommendations

The TMUX1574 operates across a wide supply range of 1.5 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the $V_{DD}$ supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from $V_{DD}$ to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.


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# 11 Layout

## 11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.Figure 44 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

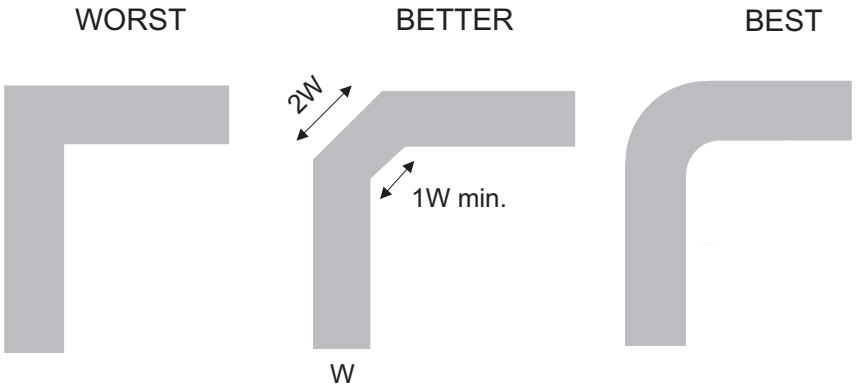


**Figure 44. Trace Example**

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed signals traces because they cause signal reflections.

Route all high-speed signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 45.

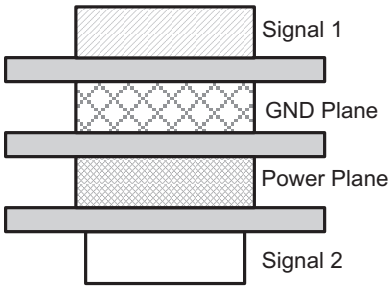


**Figure 45. Example Layout**

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

Figure 46 illustrates an example of a PCB layout with the TMUX1574. Some key considerations are:

### Layout Guidelines (continued)

Decouple the $V_{DD}$ pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the $V_{DD}$ supply.

High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

## 11.2 Layout Example

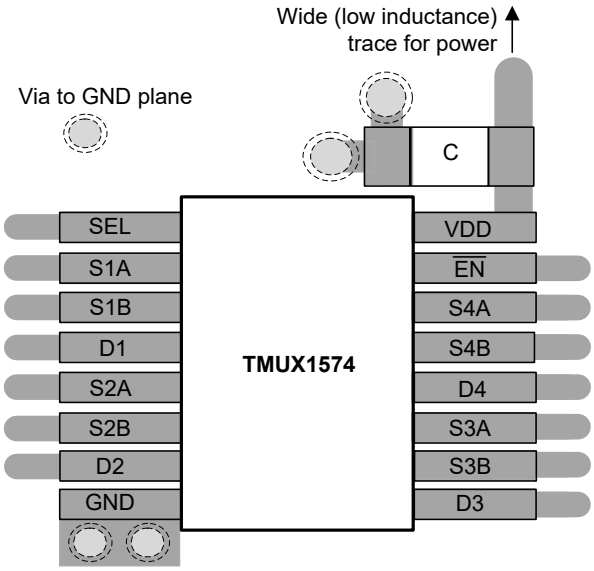


**Figure 46. Example Layout**


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# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *Enabling SPI-based flash memory expansion by using multiplexers*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

Texas Instruments, *High-Speed Interface Layout Guidelines*.

Texas Instruments, *High-Speed Layout Guidelines*.

Texas Instruments, *QFN/SON PCB Attachment*.

Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

E2E is a trademark of Texas Instruments.

## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMUX1574DYYR | Active | Production | SOT-23-THIN (DYY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TMUX1574 |
| TMUX1574DYYR.A | Active | Production | SOT-23-THIN (DYY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TMUX1574 |
| TMUX1574DYYRG4 | Active | Production | SOT-23-THIN (DYY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TMUX1574 |
| TMUX1574DYYRG4.A | Active | Production | SOT-23-THIN (DYY) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | TMUX1574 |
| TMUX1574PWR | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | MUX1574 |
| TMUX1574PWR.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX1574 |
| TMUX1574PWRG4 | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX1574 |
| TMUX1574PWRG4.A | Active | Production | TSSOP (PW) \| 16 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MUX1574 |
| TMUX1574RSVR | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1574 |
| TMUX1574RSVR.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1574 |
| TMUX1574RSVRG4.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1574 |
| TMUX1574T8RSVR | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1574 |
| TMUX1574T8RSVR.A | Active | Production | UQFN (RSV) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1574 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

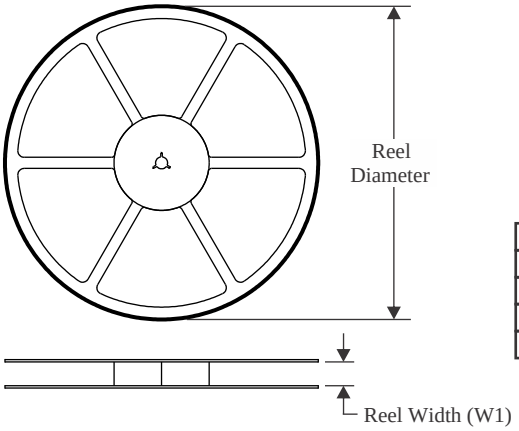
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

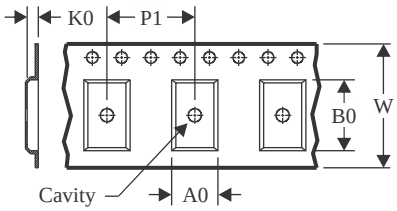
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

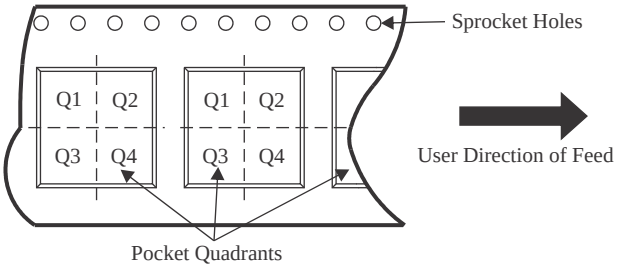



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

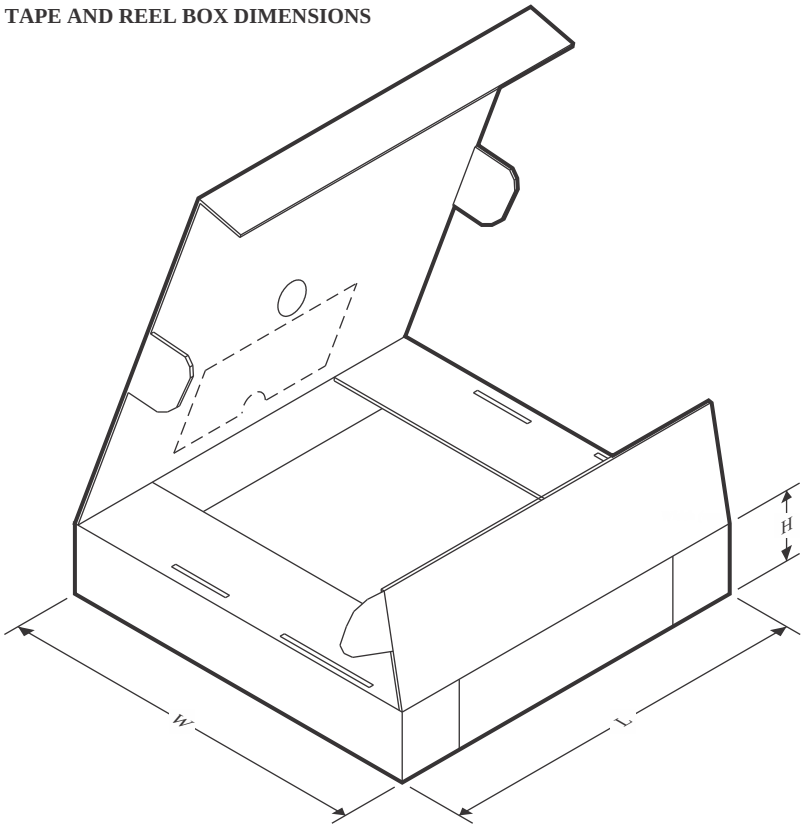
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX1574DYYR | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TMUX1574DYYRG4 | SOT-23-THIN | DYY | 16 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| TMUX1574PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TMUX1574PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.3 | 1.6 | 8.0 | 12.0 | Q1 |
| TMUX1574RSVR | UQFN | RSV | 16 | 3000 | 178.0 | 13.5 | 2.1 | 2.9 | 0.75 | 4.0 | 12.0 | Q1 |
| TMUX1574T8RSVR | UQFN | RSV | 16 | 3000 | 180.0 | 9.5 | 2.1 | 2.9 | 0.75 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMUX1574DYYR | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| TMUX1574DYYRG4 | SOT-23-THIN | DYY | 16 | 3000 | 336.6 | 336.6 | 31.8 |
| TMUX1574PWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| TMUX1574PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| TMUX1574RSVR | UQFN | RSV | 16 | 3000 | 189.0 | 185.0 | 36.0 |
| TMUX1574T8RSVR | UQFN | RSV | 16 | 3000 | 189.0 | 185.0 | 36.0 |

# GENERIC PACKAGE VIEW

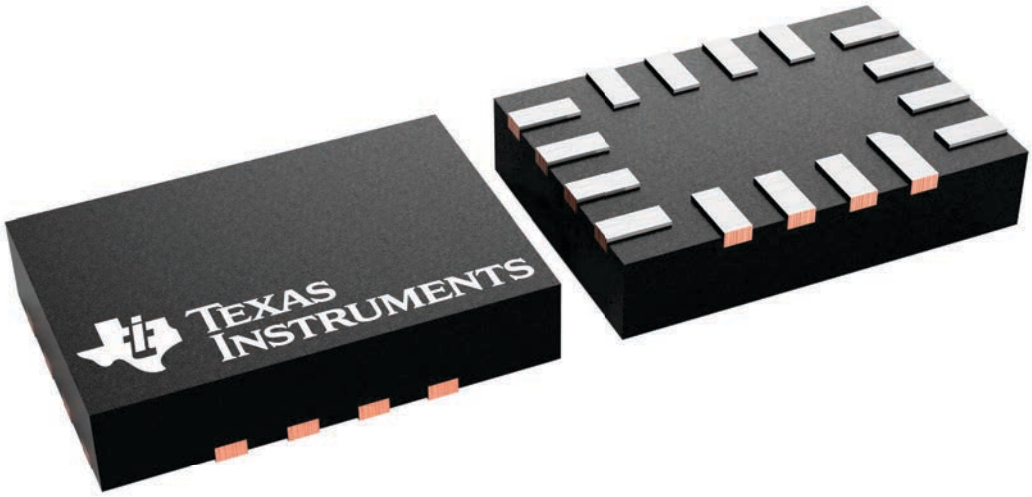
## RSV 16

## UQFN - 0.55 mm max height

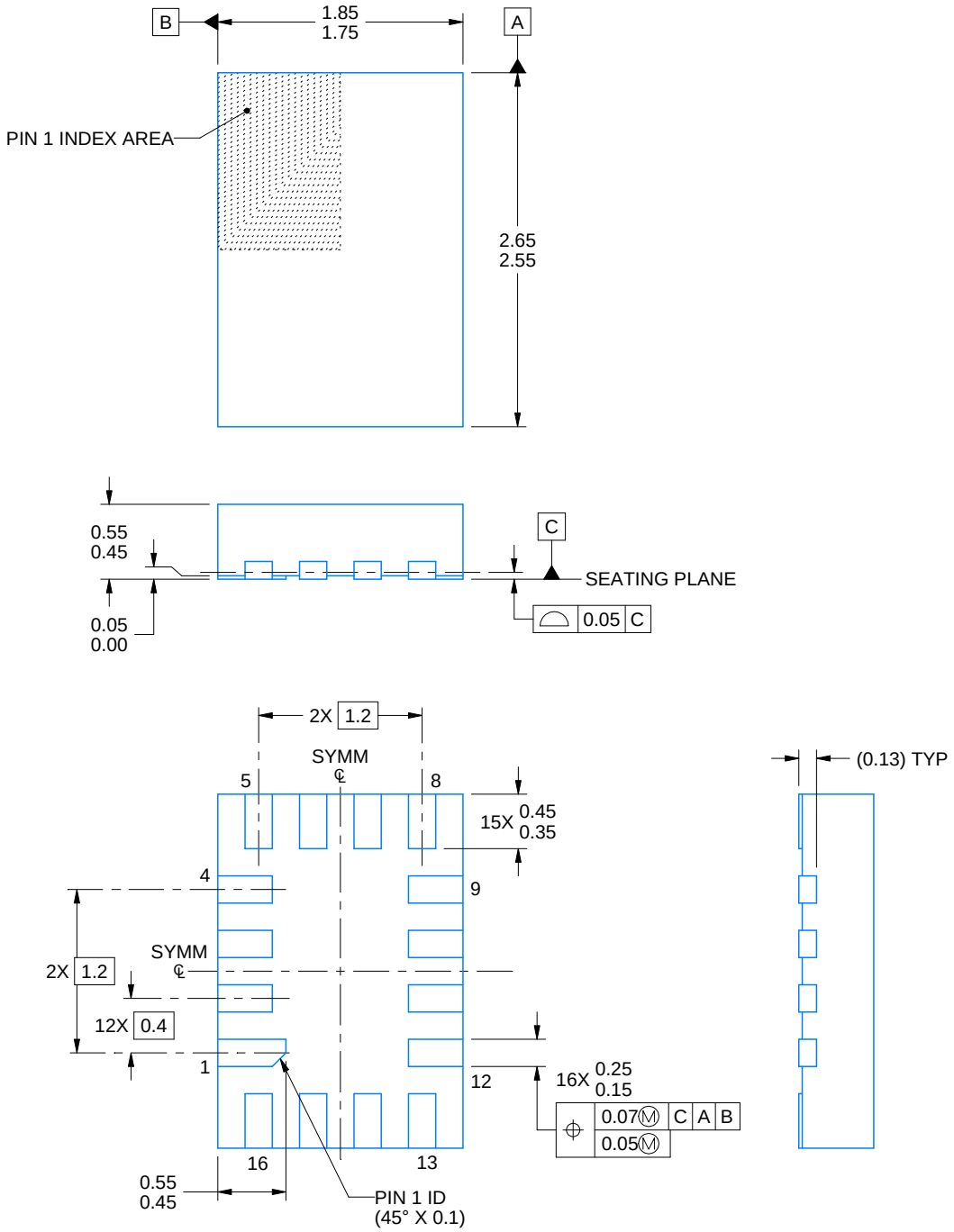
**1.8 x 2.6, 0.4 mm pitch**

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

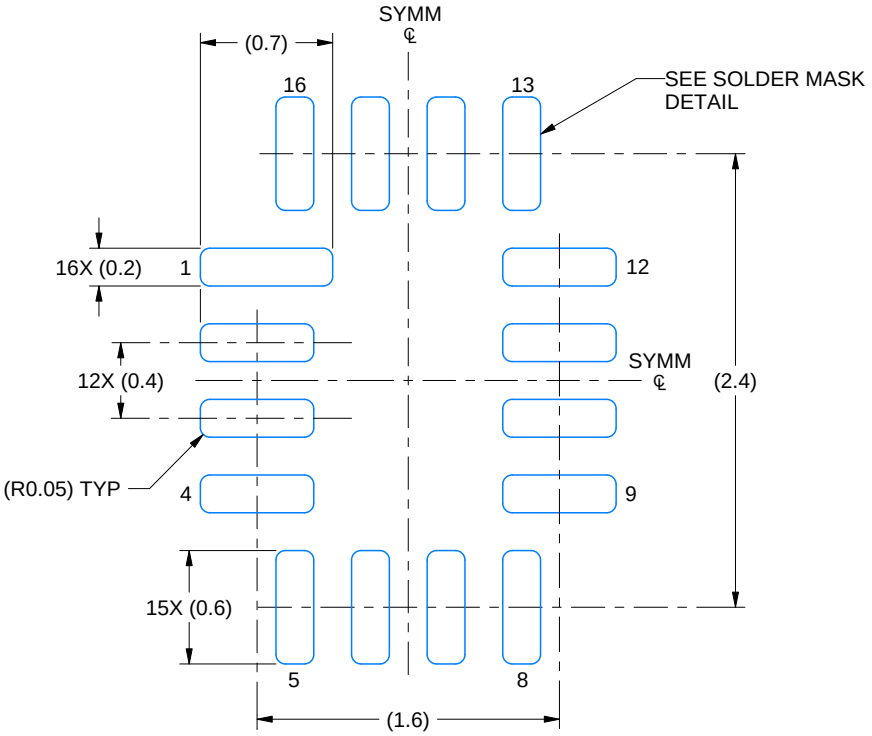



4231225/A

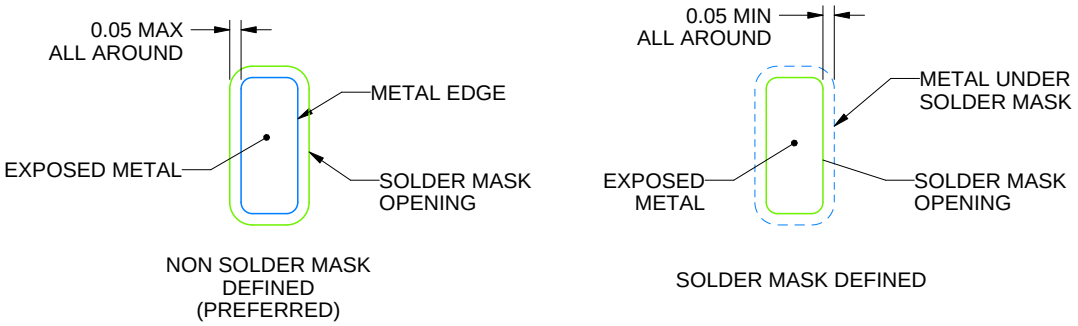



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

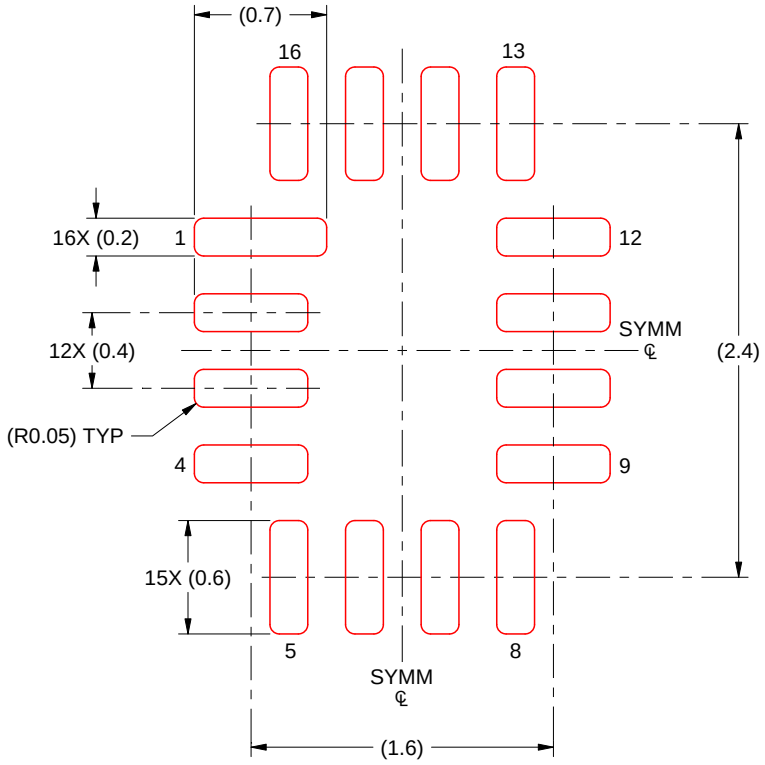



SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

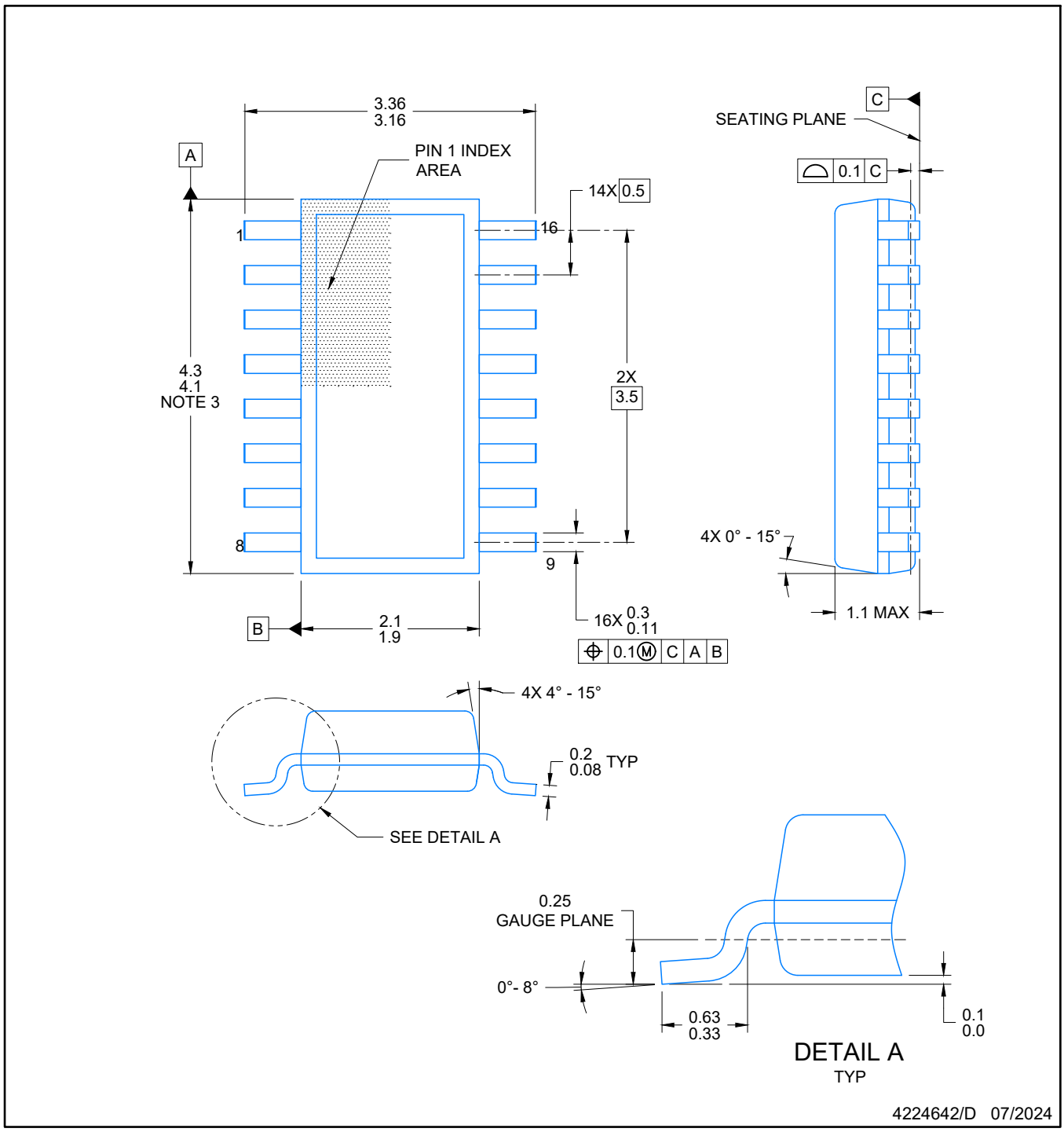



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

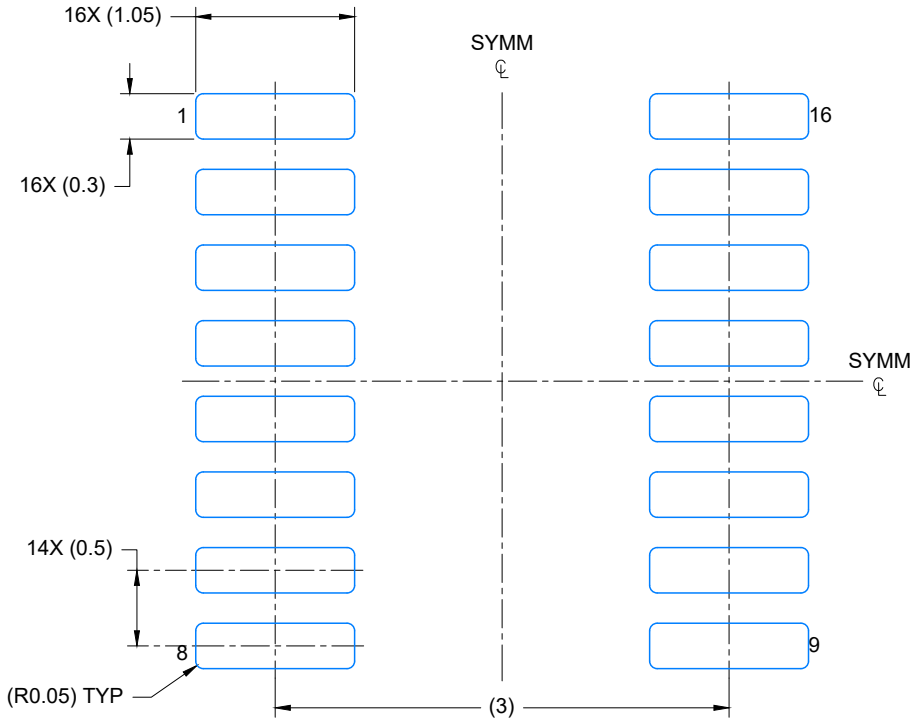
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

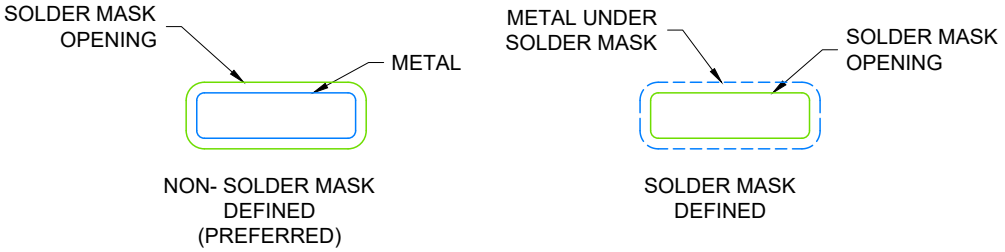



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

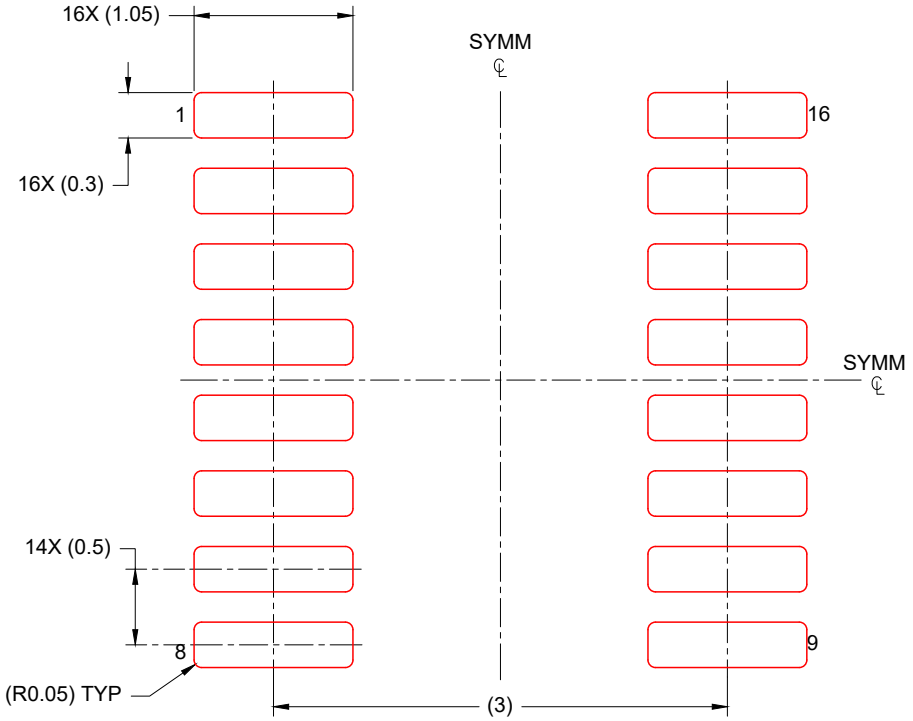



SOLDER MASK DETAILS

4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

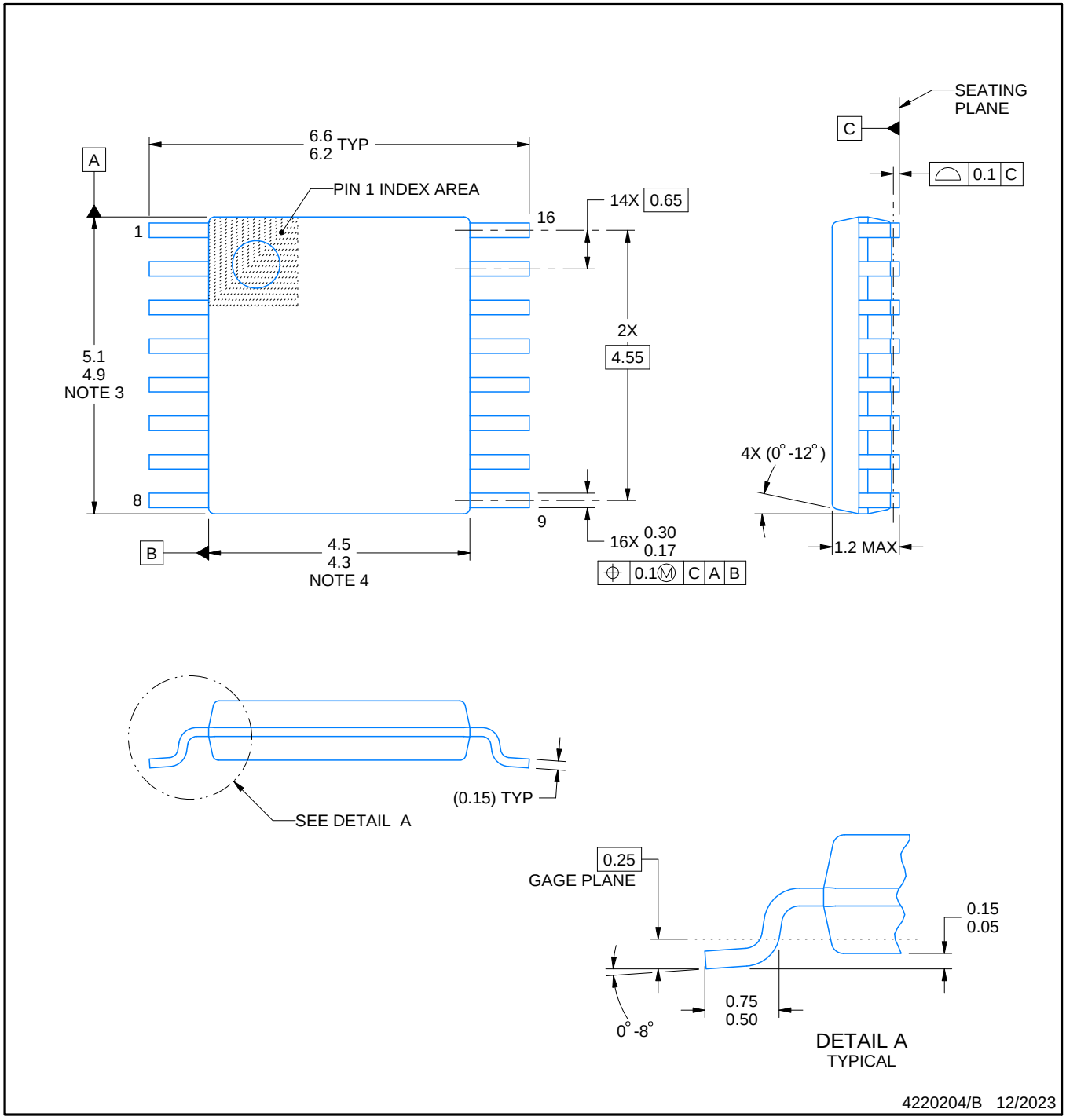



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

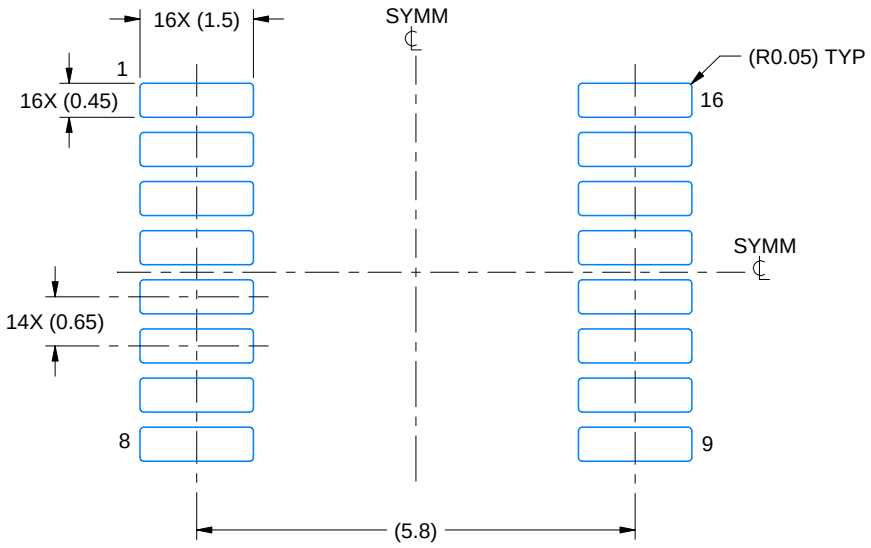
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

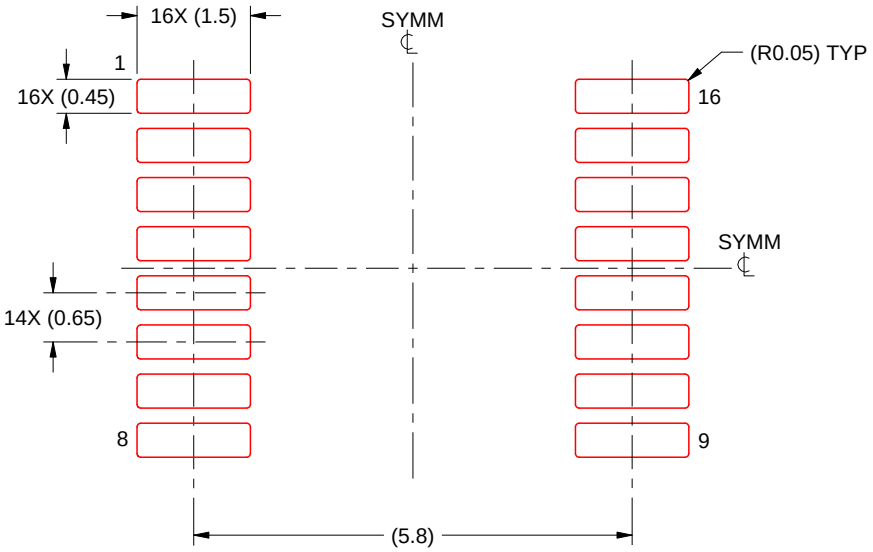
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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