TEXAS INSTRUMENTS
TPA6304-Q1
SLASEP6B – SEPTEMBER 2019 – REVISED DECEMBER 2020

TPA6304-Q1 45-W, 2.1-MHz Analog Input 4-Channel Automotive Class-D Burr-Brown™ Audio Amplifier with Load Dump Protection and I²C Diagnostics

Texas Instruments
Burr-Brown Audio

1 Features

- Highest efficiency Class-D
  - Significantly more efficient than Class-AB
  - Reduce thermal solution with 75% less heat dissipation than Class-AB
- Start/stop operation down to 4.5 V
- AEC-Q100 Qualified for automotive applications:
  - Temperature grade 1: –40°C to 125°C T_A
  - HBM ESD Classification level 2
  - CDM ESD Classification level C2B
- 27 W, 10% THD into 4 Ω at 14.4 V
  - Drives 4 Ω and 2 Ω loads
- Load diagnostics
  - Output open, shorted load
  - Output-to-battery or ground shorts
  - Tweeter connected
- Designed with advanced gate drive to meet CISPR25-L5 EMC specification
  - Class-D at 2.1 MHz, no AM interference
  - Spread Spectrum mode, Phase Offset, Slew Rate Control
- Protection
  - 40 V Load dump
  - Output short protection
  - DC offset and over temperature
  - Fortuitous open ground and power tolerant
- Audio inputs
  - 4 Channel single-ended analog input
  - 10 dB, 16 dB, 22 dB or 28 dB Gain option
- Supports parallel channel drive (PBTL)
- Audio performance into 4 Ω at 14.4 V, 1 kHz
  - THD+N < 0.006%
  - 42 μV_{RMS} Output Noise
  - 80 dB PSRR
  - Efficiency > 80%
- Special features
  - Programmable clip detection
  - Load current limiter
  - Thermal gain foldback
  - Fast and autonomous startup diagnostics
  - AC load impedance measurement with < 10 mA load current

2 Applications

- Automotive head units
- Automotive external amplifier modules

3 Description

The TPA6304-Q1 device is a four-channel analog-input Class-D Burr-Brown™ audio amplifier that implements a 2.1 MHz PWM switching frequency that enables a cost optimized solution in a very small 2.7 cm^2 PCB size, high impedance single ended inputs and full operation down to 4.5 V for start/stop events.

The TPA6304-Q1 Class-D audio amplifier has an optimal design for use in entry level automotive head units that provide analog audio input signals as part of their system design. The Class-D topology dramatically improves efficiency over traditional linear amplifier solutions.

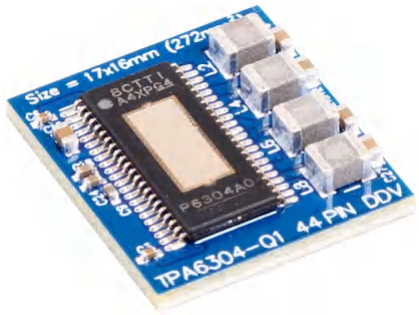
The output switching frequency can be set either above the AM band, which eliminates the AM band interference and reduces output filter size and cost, or below AM band to further optimize efficiency.

The device is offered in a 44 pin HTSSOP package with the exposed thermal pad up.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPA6304-Q1	HTSSOP (44)	14.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Reference Board

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2019) to Revision B (December 2020)	Page
• Changed the device status From: *Advanced information* To: *Production* data	1
• Changed From: Single-Ended Analog input with 3 gain option To: Single-Ended Analog input with 4 gain options in the *Functional Block Diagram*	23

5 Pin Configuration and Functions

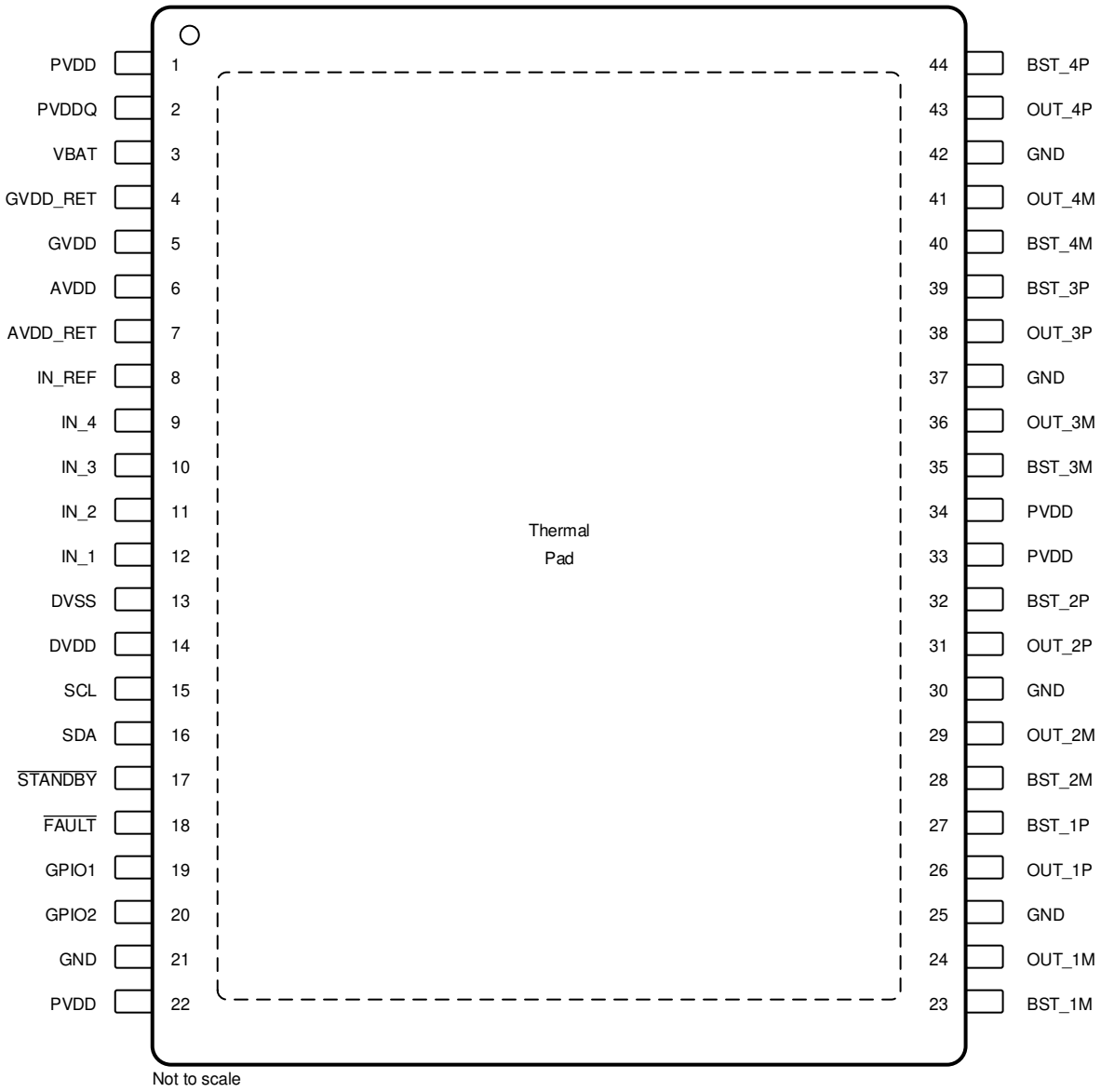


Figure 5-1. DDV Package, 44-Pin HTSSOP, Top View

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AVDD	6	PWR	Voltage regulator bypass, derived from VBAT input pins. Connect 1 µF capacitor from AVDD (pin 6) to AVDD_RET (pin 7).
AVDD_RET	7	GND	AVDD voltage regulator return. Connect to ground.
BST_1M	23	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_1P	27	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2M	28	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2P	32	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_3M	35	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_3P	39	PWR	Bootstrap capacitor connection pins for high-side gate driver

Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BST_4M	40	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_4P	44	PWR	Bootstrap capacitor connection pins for high-side gate driver
DVDD	14	PWR	DVDD supply input. Connect 1 µF capacitor from DVDD to DVSS (pin 13).
DVSS	13	GND	DVDD ground reference. Connect to ground.
$\overline{\text{FAULT}}$	18	DI/O	Reports a fault (active low, open drain), external pullup resistor determines I^2C address during power on reset.
GND	21, 25, 30, 37, 42	GND	Ground
GPIO1	19	DI/O	General purpose IO, function set by register programming.
GPIO2	20	DI/O	General purpose IO, function set by register programming.
GVDD	5	PWR	Gate drive voltage regulator bypass for all output channels, derived from VBAT input pins. Connect 2.2µF capacitor to GVDD_RET (pin 4).
GVDD_RET	4	GND	Gate drive voltage regulator return. Connect to ground.
IN_1	12	AI	Non-inverting input channel. Internally biased to AVDD/2. Connect to AC coupling capacitor.
IN_2	11	AI	Non-inverting input channel. Internally biased to AVDD/2. Connect to AC coupling capacitor.
IN_3	10	AI	Non-inverting input channel. Internally biased to AVDD/2. Connect to AC coupling capacitor.
IN_4	9	AI	Non-inverting input channel. Internally biased to AVDD/2. Connect to AC coupling capacitor.
IN_REF	8	AI	Reference input voltage for IN_1, IN_2, IN_3, IN_4. Internally biased to AVDD/2. Connect to AC coupling capacitor.
OUT_1M	24	NO	Negative output for the channel
OUT_1P	26	PO	Positive output for the channel
OUT_2M	29	NO	Negative output for the channel
OUT_2P	31	PO	Positive output for the channel
OUT_3M	36	NO	Negative output for the channel
OUT_3P	38	PO	Positive output for the channel
OUT_4M	41	NO	Negative output for the channel
OUT_4P	43	PO	Positive output for the channel
PVDD	1, 22, 33, 34	PWR	PVDD voltage input carrying load currents (can be connected to battery).
PVDDQ	2	PWR	PVDD voltage input not loaded with load currents (can be connected to battery).
SCL	15	DI	I^2C clock input
SDA	16	DI/O	I^2C data input and output
$\overline{\text{STANDBY}}$	17	DI	Enables low power standby state (active Low), 100-kΩ internal pulldown resistor.
VBAT	3	PWR	Battery voltage input
Thermal Pad	—	GND	Provides thermal connection for the device. Heatsink must be connected to GND.

(1) AI = analog input, GND = ground, PWR = power, PO = positive output, NO = negative output, DI = digital input, DO = digital output, DI/O = digital input and output, NC = No Connection

6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
PVDD, VBAT	DC supply-voltage range relative to GND		–0.3	30	V
V_{MAX}	Transient supply-voltage range - PVDD, VBAT	t ≤ 400 ms exposure	–1	40	V
V_{RAMP}	Supply-voltage ramp rate - PVDD, VBAT			75	V/ms
V_{IN}	Audio input pins - IN_x, IN_Ref		–0.3	5.5	V
DVDD	DC supply voltage range relative to GND		–0.3	3.5	V
I_{MAX}	Maximum current per pin - PVDD, VBAT, OUTxP, OUT xM, GND	Peak Audio Current, t < 25ms		7.5	A
V_{LOGIC}	Input voltage for logic pins - SCL, SDA, $\overline{FAULT}$, $\overline{STANDBY}$, GPIOx		–0.3	DVDD + 0.5	V
V_{GND}	Maximum voltage between GND pins			±0.3	V
T_J	Maximum operating junction temperature range		–55	175	°C
T_{stg}	Storage temperature range		–55	150	°C

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	All pins	±750	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 22, 23 and 44)	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
PVDD	Output FET Supply Voltage Range	Relative to GND	4.5	14.4	18	V
VBAT	Battery Supply Voltage Range	Relative to GND	4.5	14.4	18	V
DVDD	Digital Logic Supply	Relative to GND	3.0	3.3	3.5	V
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature	An adequate thermal design is required	–40		160	°C
R_L	Nominal speaker load impedance	BTL Mode	2	4		Ω
R_L	Nominal speaker load impedance	PBTL Mode	1.75	2		Ω
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
C_{Bypass}	External capacitance on bypass pins	Pin 1, 3, 6, 14		1		µF
C_{GVDD}	External capacitance on GVDD pin	Pin 5		2.2		µF
C_{OUT}	External capacitance to GND on OUT pins	Limit set by DC-diagnostic timing		1	3.3	µF
L_O	Output filter inductance - I_{SD}	Minimum output filter inductance at I_{SD} current levels. Applies to short to ground or short to power protection.	0.5			µH

6.3 Recommended Operating Conditions (continued)

			MIN	TYP	MAX	UNIT
L_O	Output filter inductance - I_{LIMIT}	Minimum output filter inductance at I_{LIMIT} current levels. Applies to current limiting.	1			µH

6.4 Thermal Information

THERMAL METRIC(1)		TPA6304-Q1(2)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	–	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermalmetrics, see the SPRA953 application report.
(2) JEDEC Standard 4 Layer PCB.

6.5 Electrical Characteristics

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, Gain = 22 dB, BD Mode, AES17 Filter, LC reconstruction filter: 3.3µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2Ω configuration and 1µF, default I^2C settings, see application diagrams in Typical Applications section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All channels playing, no audio input		60	70	mA
I_{VBAT_IDLE}	VBAT idle current	All channels playing, no audio input		115	130	mA
I_{DVDD}	DVDD supply current	All channels playing, -60 dB Signal		4	4.5	mA
I_{PVDD_STBY}	PVDD standby current	$\overline{\text{STANDBY}}$ active, DVDD = 0 V		1.5	10	µA
I_{VBAT_STBY}	VBAT standby current	$\overline{\text{STANDBY}}$ active, DVDD = 0 V		1	2	µA
OUTPUT POWER						
P_{O_BTL}	Output power per channel, BTL	4 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	20	22		W
P_{O_BTL}	Output power per channel, BTL	4 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	25	27		W
P_{O_BTL}	Output power per channel, BTL	4 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C, Inductor DCR = 25mΩ		27		W
P_{O_BTL}	Output power per channel, BTL	2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	32	37		W
P_{O_BTL}	Output power per channel, BTL	2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	40	45		W
$P_{O\_BTL\_SQ}$	Output power per channel with square wave, BTL	4 Ω, PVDD = 14.4 V, 2 V_{RMS} Input Square Wave		45		W
$P_{O\_BTL\_SQ}$	Output power per channel with square wave, BTL	4 Ω, PVDD = 16 V, 2 V_{RMS} Input Square Wave		55		W
P_{O_PBTL}	Output power per channel in parallel mode, PBTL	2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	38	43		W
P_{O_PBTL}	Output power per channel in parallel mode, PBTL	2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	47	53		W

6.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, Gain = 22 dB, BD Mode, AES17 Filter, LC reconstruction filter: 3.3µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2Ω configuration and 1µF, default I^2C settings, see application diagrams in Typical Applications section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EFF_P	Power efficiency	4 channels operating, 25 W output power per channel, R_L = 4 Ω, PVDD = 14.4 V, T_C = 25°C; (includes device and LC filter losses)		88		%
PWM OUTPUT STAGE						
$R_{DS(on)}$	FET drain-to-source resistance	25°C, Including bond wire and package resistance		100		mΩ
$R_{DS(on)}$	FET drain-to-source resistance	25°C, Not including bond wire and package resistance		80		mΩ
AUDIO PERFORMANCE						
V_n	Output noise voltage	Zero input, A-weighting, 10 dB gain		35		µV
V_n	Output noise voltage	Zero input, A-weighting, 16 dB gain		42		µV
V_n	Output noise voltage	Zero input, A-weighting, 22 dB gain		60		µV
V_n	Output noise voltage	Zero input, A-weighting, 28 dB gain		75		µV
THD+N	Total harmonic distortion + noise			0.013		%
G	Gain	Level 1	9	10	10.5	dB
G	Gain	Level 2	15	16	16.5	dB
G	Gain	Level 3	21	22	22.5	dB
G	Gain	Level 4	27	28	28.5	dB
G_{CH}	Channel-to-channel gain variation		–0.5	0	0.5	dB
Crosstalk	Channel crosstalk			–90		dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 V_{RMS}, f = 1 kHz		80		dB
G_{MUTE}	Output attenuation	Assert $\overline{MUTE}$ and compare to amp playing 1W audio into 4 Ω	100	117		dB
V_{CLICK}	Click and Pop	Zero input, ITU-filter, 28dB gain		7		mV
$V_{n\_LINEOUT}$	Line output noise voltage	Zero input, A-weighting, channel set to Line Output, R_L = 600 Ω, Gain = 16 dB		42		µV
THD+N	Line output Total harmonic distortion + noise	V_{OUT} = 2 V_{RMS} , channel set to Line Output		0.01		%
ANALOG INPUT PINS						
R_{IN}	Input impedance	IN_1, IN_2, IN_3, IN_4		80		kΩ
R_{IN}	Input impedance	IN_REF		20		kΩ
V_{IN}	Maximum input voltage swing	V_{IN} AC coupled through capacitor. Pins IN_1, IN_2, IN_3, IN_4		1		V_{RMS}
V_{IN}	Maximum input voltage swing	IN_REF		5		mV
I_{IN}	Maximum input current	IN_1, IN_2, IN_3, IN_4, IN_REF			10	mA
DIGITAL INPUT PINS						
V_{IH}	Input logic level high		70			%DVDD
V_{IL}	Input logic level low				30	%DVDD
I_{IH}	Input logic current	V_I = DVDD		33	50	µA
I_{IL}	Input logic current	V_I = 0	–50	–33		µA

6.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, Gain = 22 dB, BD Mode, AES17 Filter, LC reconstruction filter: 3.3µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2Ω configuration and 1µF, default I^2C settings, see application diagrams in Typical Applications section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OUTPUT PINS						
V_{OH}	Output voltage for logic level high	I = ±2 mA	90			%DVDD
V_{OL}	Output voltage for logic level low	I = ±2 mA			10	%DVDD
BYPASS VOLTAGES						
V_{GVDD}	Gate drive bypass pin voltage			5		V
V_{AVDD}	Analog bypass pin voltage			5		V
OVERVOLTAGE (OV) PROTECTION						
$V_{PVDD\_OV\_SET}$	PVDD overvoltage shutdown set		18.5	20	22	V
$V_{PVDD\_OV\_HYS}$	PVDD overvoltage recovery hysteresis			0.5		V
$V_{VBAT\_OV\_SET}$	VBAT overvoltage shutdown set		18.5	20	22	V
$V_{VBAT\_OV\_HYS}$	VBAT overvoltage recovery hysteresis			0.5		V
UNDERVOLTAGE (UV) PROTECTION						
$VBAT_{UV\_SET}$	VBAT undervoltage shutdown set		3.7		4.5	V
$VBAT_{UV\_HYS}$	VBAT undervoltage recovery hysteresis			0.3		V
$PVDD_{UV\_SET}$	PVDD undervoltage shutdown set		3.7		4.5	V
$PVDD_{UV\_HYS}$	PVDD undervoltage recovery hysteresis			0.3		V
POWER-ON RESET (POR)						
V_{POR_SET}	DVDD power on reset set	Increasing DVDD		1.9		V
V_{POR_HYS}	DVDD power on reset recovery hysteresis			0.5		V
V_{POR_OFF}	DVDD power off threshold	Decreasing DVDD	1.5		2.4	V
OVERTEMPERATURE (OT) PROTECTION						
OTW(i)	Per channel over-temperature warning			160		°C
OTSD(i)	Per channel over-temperature shutdown			175		°C
OTW	Global junction over-temperature warning	Default value (see Misc Control Register 1)		130		°C
OTSD	Global junction over-temperature shutdown			160		°C
OT_{HYS}	Over-temperature recovery hysterisis			15		°C
LOAD OVERCURRENT PROTECTION						
I_{LIMIT}	Load Overcurrent limit	OC level 1, load current (default)	3.0	3.4		A
I_{LIMIT}	Load Overcurrent limit	OC level 2, load current	3.5	4		A

6.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, Gain = 22 dB, BD Mode, AES17 Filter, LC reconstruction filter: 3.3µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2Ω configuration and 1µF, default I^2C settings, see application diagrams in Typical Applications section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LIMIT}	Load Overcurrent limit	OC level 3, load current	5.0	5.8		A
I_{LIMIT}	Load Overcurrent limit	OC level 4, load current	6.0	6.5		A
I_{SD}	Overcurrent shutdown	OC level 1, any short to supply, ground, or other channels (default)		4.7	6	A
I_{SD}	Overcurrent shutdown	OC level 2, any short to supply, ground, or other channels		5.5	7	A
I_{SD}	Overcurrent shutdown	OC level 3, any short to supply, ground, or other channels		8.0	10	A
I_{SD}	Overcurrent shutdown	OC level 4, any short to supply, ground, or other channels		9.0	11	A
DC DETECT						
DC_{FAULT}	Output DC fault protection		1	1.75	2.5	V
SYNC						
f_{sync}	Supported SYNC frequency, master mode	Misc Control 2 Register, PWM_FREQUENCY: 00, f_{sw} = 2.1MHz		8.4		MHz
f_{sync}	Supported SYNC frequency, master mode	Misc Control 2 Register, PWM_FREQUENCY: 01, f_{sw} = 2.3MHz		9.2		MHz
Δf_{sync}	SYNC frequency deviation from nominal, master mode		–10		10	%
f_{sync}	Supported SYNC frequency, slave mode	f_{sw} = 2.1MHz		8.4		MHz
f_{sync}	Supported SYNC frequency, slave mode	f_{sw} = 2.3 MHz		9.2		MHz
Δf_{sync}	Supported SYNC frequency deviation, slave mode		–10		10	%
D_{sync}	Supported SYNC duty cycle, slave mode		44	50	56	%
LOAD DIAGNOSTICS						
S2P	Maximum resistance to detect a short from OUT pin(s) to PVDD			8000		Ω
S2G	Maximum resistance to detect a short from OUT pin(s) to ground			300		Ω
SL	Shorted load detection tolerance	One channel, other channels in Hi-Z		±12.5%		
OL	Minimum impedance detected as open load	Other channels in Hi-Z		110		Ω
T_{DC_DIAG}	DC diagnostic time	4 channels, no faults		174		ms
LO	Maximum detectable impedance for line output mode			12		kΩ
T_{LINE_DIAG}	Line output diagnostic time			150		ms

6.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{out} = 1 kHz, F_{sw} = 2.1 MHz, Gain = 22 dB, BD Mode, AES17 Filter, LC reconstruction filter: 3.3µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2Ω configuration and 1µF, default I^2C settings, see application diagrams in Typical Applications section.

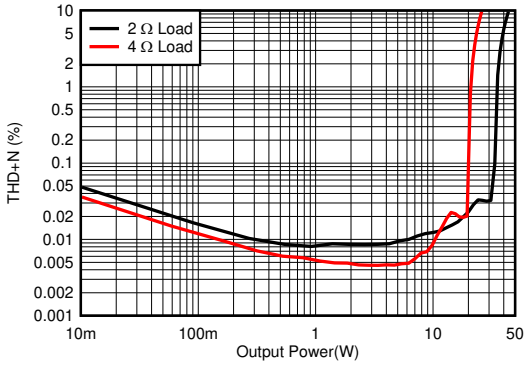
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC_{IMP}	AC impedance accuracy	f = 18.5 kHz, R_L = 4 Ω, Impedance at output pins		±0.75		Ω
T_{AC_DIAG}	AC diagnostic time	4 channels, f = 18.5 kHz		217		ms
F_{AC}	AC diagnostic test frequency	Default frequency		18.5		kHz
I2C CONTROL PORT						
t_{BUS}	Bus free time between start and stop conditions		1.3			µs
t_{H1}	Hold Time, SCL to SDA		0			ns
t_{H2}	Hold Time, start condition to SCL		0.6			µs
t_{START}	I^2C Startup Time After DVDD Power On Reset			10		ms
t_{RISE} (1)	Rise Time, SCL and SDA				300	ns
t_{FALL} (1)	Fall Time, SCL and SDA				300	ns
t_{SU1}	Setup, SDA to SCL		100			ns
t_{SU2}	Setup, SCL to Start Condition		0.6			µs
t_{SU3}	Setup, SCL to Stop Condition		0.6			µs
$t_{W(H)}$	Required Pulse Duration SCL High		0.6			µs
$t_{W(L)}$	Required Pulse Duration SCL Low		1.3			µs

(1) Specified by design.

6.6 Typical Characteristics

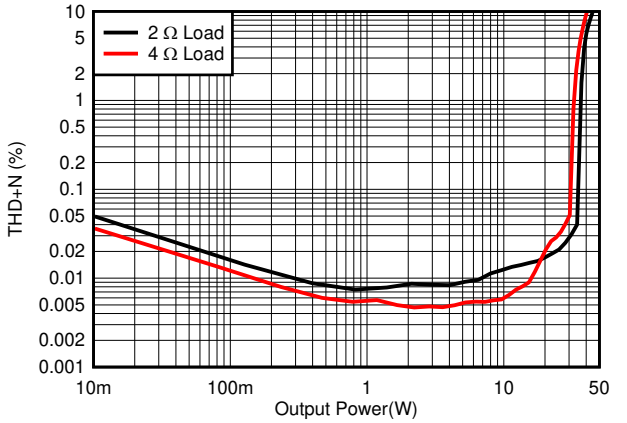
6.6.1 Bridge-Tied Load (BTL), BD

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 2.1 MHz**, Gain = 22 dB, **BD Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 3.3 µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



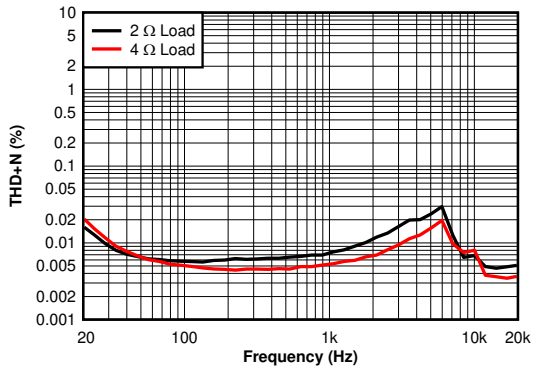
PVDD = 14.4V BTL

Figure 6-1. THD+N vs Power - 2 Ω, 4 Ω - 14.4 V



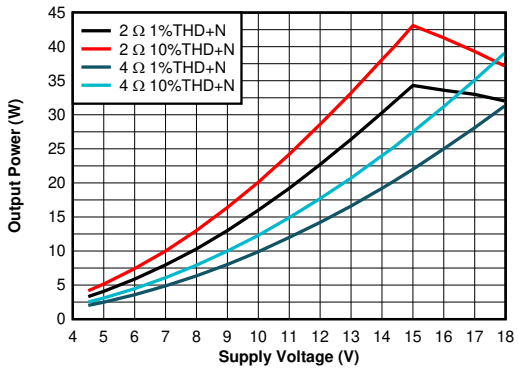
PVDD = 18V BTL

Figure 6-2. THD+N vs Power - 2 Ω, 4 Ω - 18 V



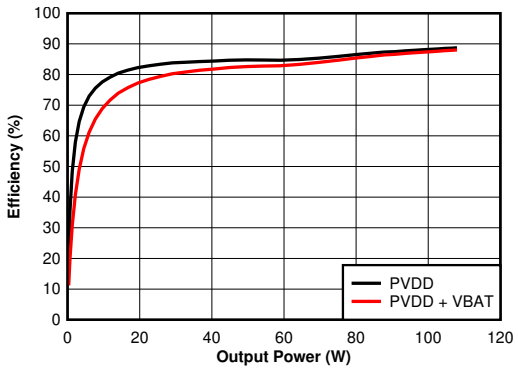
P_O = 1 W BTL

Figure 6-3. THD+N vs Frequency - 2 Ω, 4 Ω



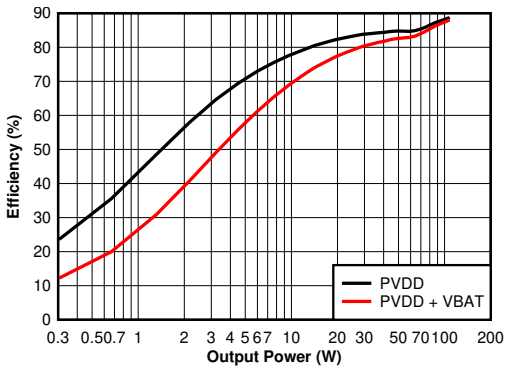
T_C = 75 °C BTL

Figure 6-4. Output Power vs Supply Voltage - 2 Ω 1%, 2 Ω 10%, 4 Ω 1%, 4 Ω 10%



4 Ω T_C = 75 °C BTL

Figure 6-5. Efficiency vs Output Power - 4 Ω

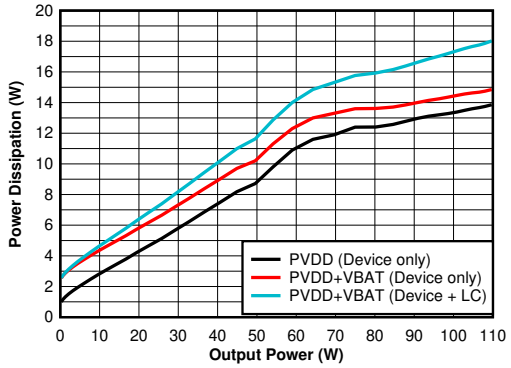


4 Ω T_C = 75 °C BTL

Figure 6-6. Efficiency vs Output Power - 4 Ω (Zoomed)

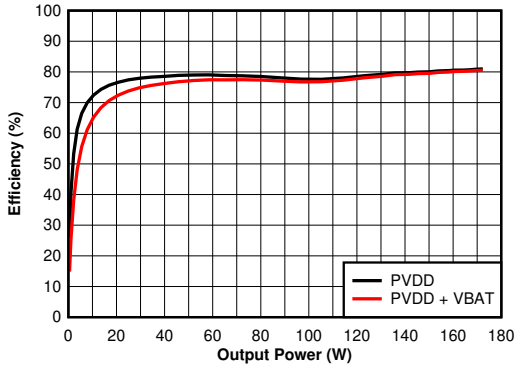
6.6.1 Bridge-Tied Load (BTL), BD (continued)

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 2.1 MHz**, Gain = 22 dB, **BD Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 3.3 µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



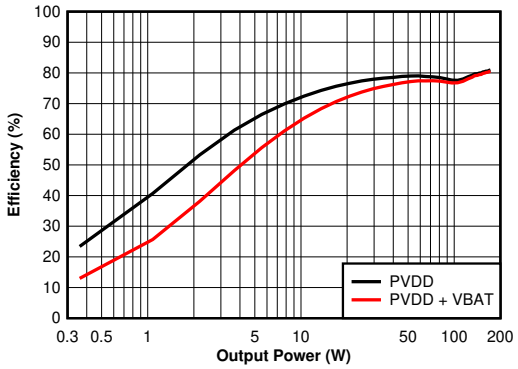
4 Ω T_C = 75 °C BTL

Figure 6-7. Power Dissipation vs Output Power - 4 Ω



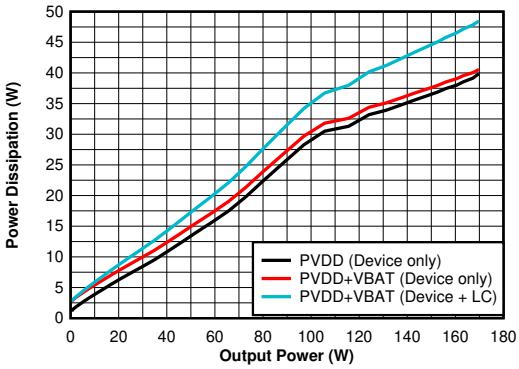
2 Ω T_C = 75 °C BTL

Figure 6-8. Efficiency vs Output Power - 2 Ω



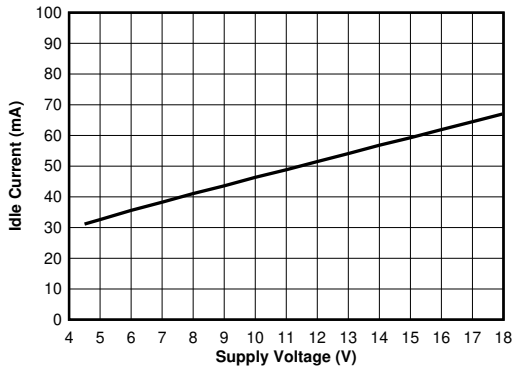
2 Ω T_C = 75 °C BTL

Figure 6-9. Efficiency vs Output Power - 2 Ω (Zoomed)



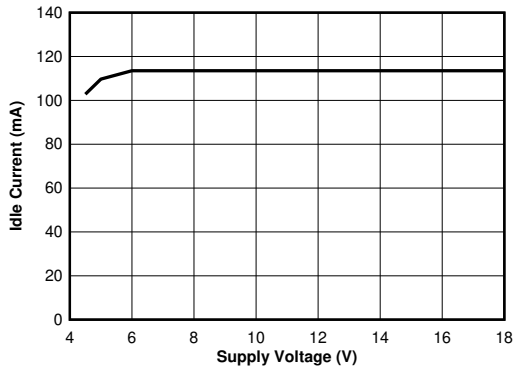
2 Ω T_C = 75 °C BTL

Figure 6-10. Power Dissipation vs Output Power - 2 Ω



BTL

Figure 6-11. PVDD Idle vs Supply Voltage

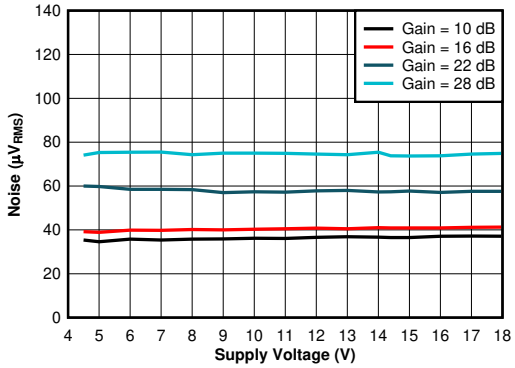


BTL

Figure 6-12. VBAT Idle Current vs Supply Voltage

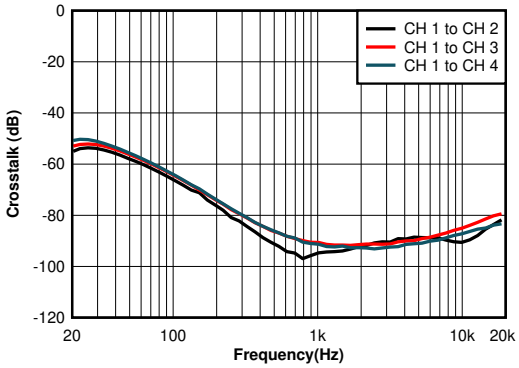
6.6.1 Bridge-Tied Load (BTL), BD (continued)

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 2.1 MHz**, Gain = 22 dB, **BD Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 3.3 µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



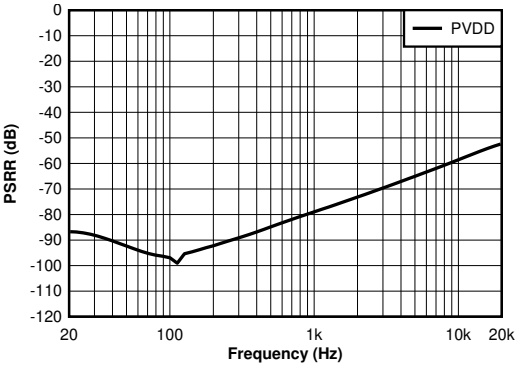
A-Weighted BTL

Figure 6-13. Noise vs Supply Voltage



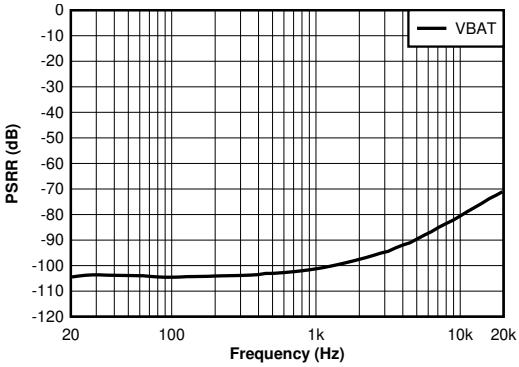
BTL

Figure 6-14. Crosstalk vs Frequency



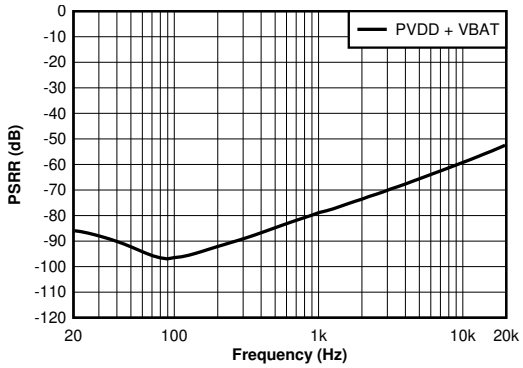
P_O = 1 W PVDD = 14.4 V + 1 V_{RMS} BTL

Figure 6-15. PSRR vs Frequency - PVDD Only



P_O = 1 W VBAT = 14.4 V + 1 V_{RMS} BTL

Figure 6-16. PSRR vs Frequency - VBAT Only

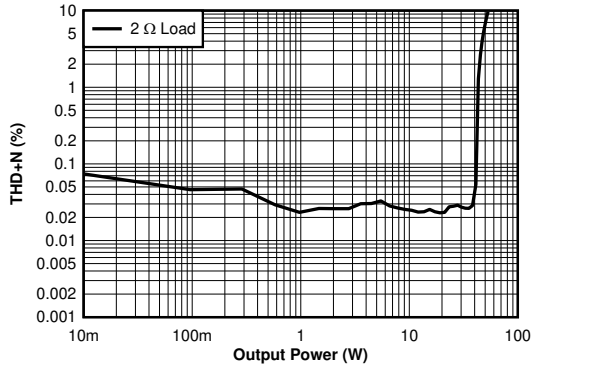


P_O = 1 W PVDD = VBAT = 14.4 V + 1 V_{RMS} BTL

Figure 6-17. PSRR vs Frequency - PVDD+VBAT

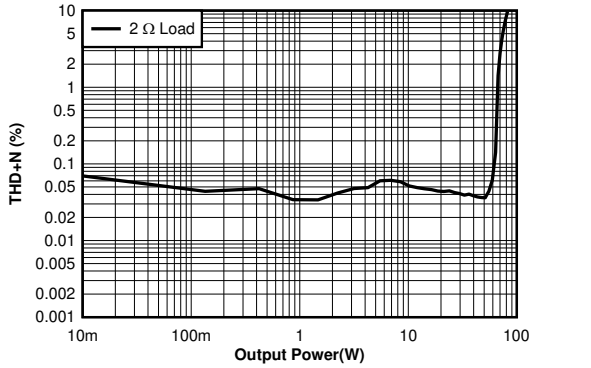
6.6.2 Parallel Bridge-Tied Load (PBTL)

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 2 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 2.1 MHz**, Gain = 22 dB, **BD Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 3.3 µH - ASWPA6055S3R3MT in 2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Section 8.2.2



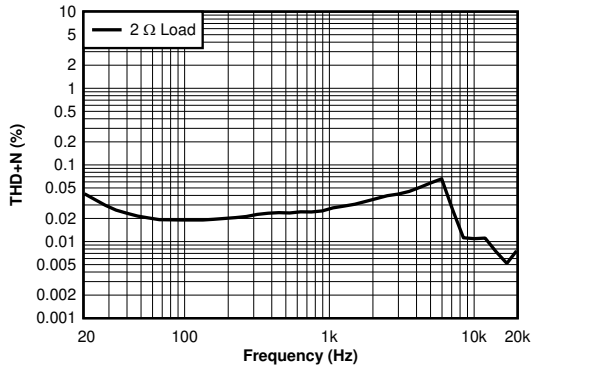
PVDD = 14.4 V PBTL

Figure 6-18. THD+N vs Power - PBTL, 2 Ω, 14.4 V



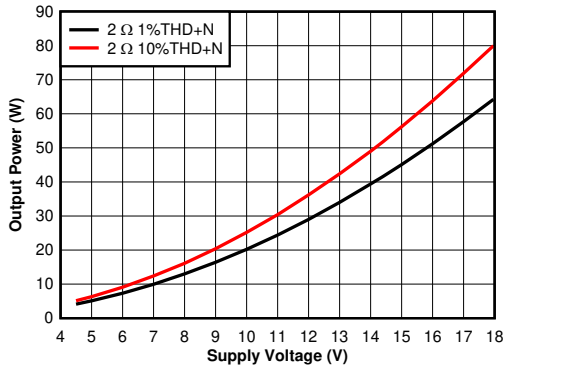
PVDD = 18 V PBTL

Figure 6-19. THD+N vs Power - PBTL, 2 Ω, 18 V



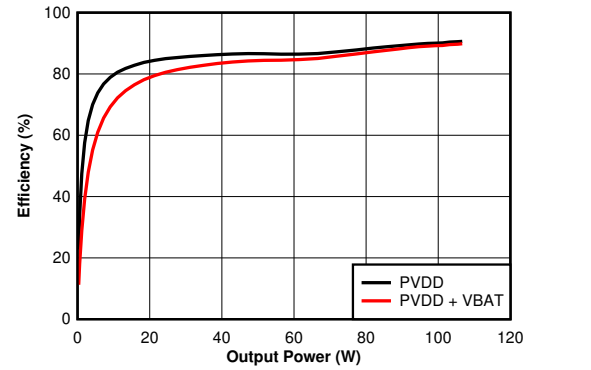
P_O = 1 W PBTL

Figure 6-20. THD+N vs Frequency - PBTL, 2 Ω



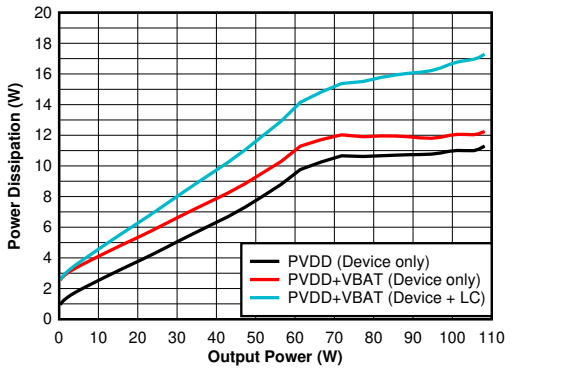
2 Ω T_C = 75 °C PBTL

Figure 6-21. Ouput Power vs Supply Voltage - PBTL, 2 Ω



2 Ω T_C = 75 °C PBTL

Figure 6-22. Efficiency vs Output Power - PBTL, 2 Ω

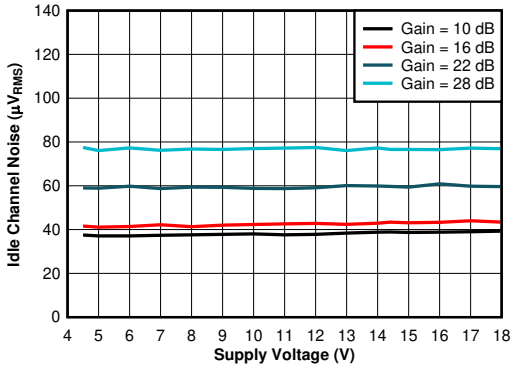


2 Ω T_C = 75 °C PBTL

Figure 6-23. Power Dissipation vs Output Power - PBTL, 2 Ω

6.6.2 Parallel Bridge-Tied Load (PBTL) (continued)

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 2 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 2.1 MHz**, Gain = 22 dB, **BD Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 3.3 µH - ASWPA6055S3R3MT in 2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Section 8.2.2

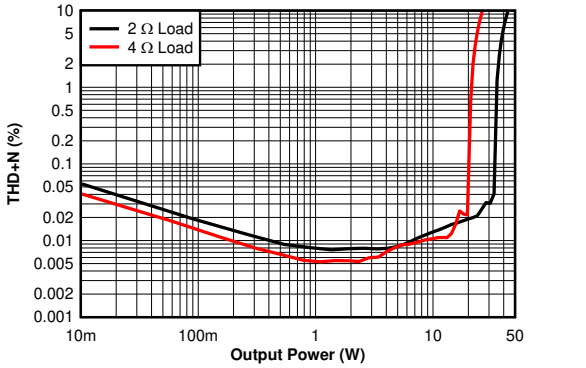


A-Weighted PBTL

Figure 6-24. Noise vs Supply Voltage - PBTL, 2 Ω

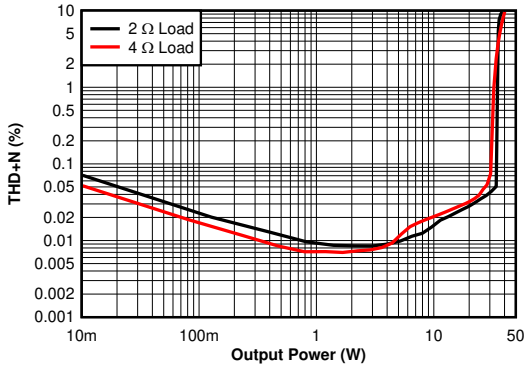
6.6.3 Bridge-Tied Load (BTL), 1SPW

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 2.1 MHz**, Gain = 22 dB, **1SPW Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 3.3 µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



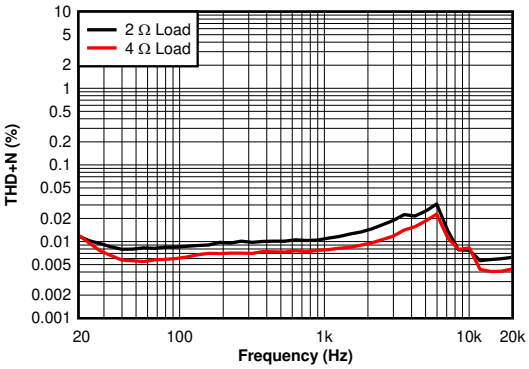
PVDD = 14.4 V BTL

Figure 6-25. THD+N vs Power - BTL, 2 Ω, 4 Ω, 14.4 V, 1SPW



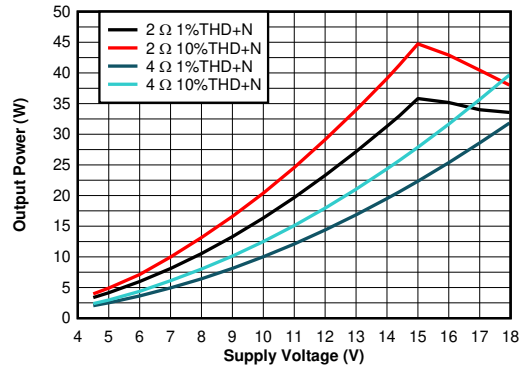
PVDD = 18 V BTL

Figure 6-26. THD+N vs Power - BTL, 2 Ω, 4 Ω, 18 V, 1SPW



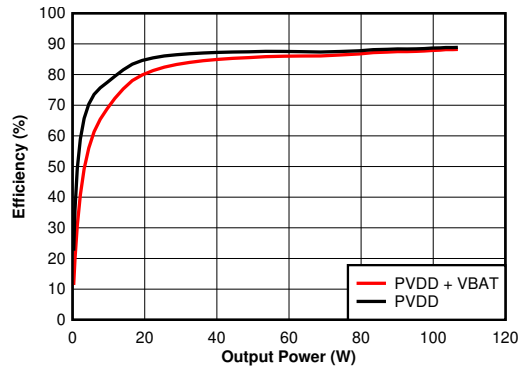
P_O = 1 W BTL

Figure 6-27. THD+N vs Frequency - BTL, 2 Ω, 4 Ω, 14.4 V, 1SPW



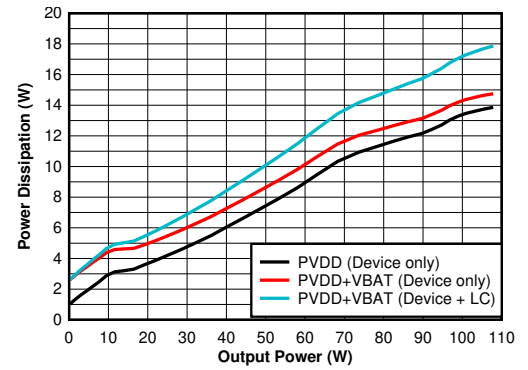
T_C = 75 °C BTL

Figure 6-28. Ouput Power vs Supply Voltage - BTL, 2 Ω, 4 Ω, 1SPW



4 Ω T_C = 75 °C BTL

Figure 6-29. Efficiency vs Output Power - BTL, 4 Ω, 14.4 V, 1SPW

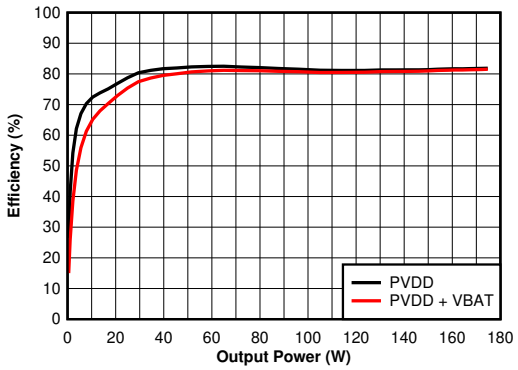


4 Ω T_C = 75 °C BTL

Figure 6-30. Power Dissipation vs Output Power - BTL, 4 Ω, 14.4 V, 1SPW

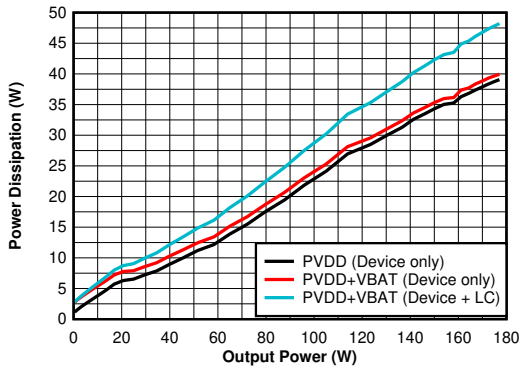
6.6.3 Bridge-Tied Load (BTL), 1SPW (continued)

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 2.1 MHz**, Gain = 22 dB, **1SPW Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 3.3 µH - ASWPA4035S3R3MT in 4Ω, ASWPA6055S3R3MT in 2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



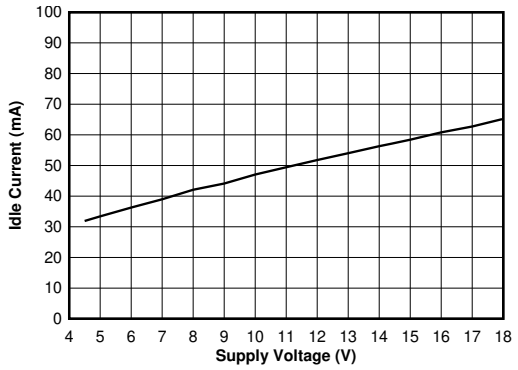
2 Ω T_C = 75 °C BTL

Figure 6-31. Efficiency vs Output Power - BTL, 2 Ω, 14.4 V, 1SPW



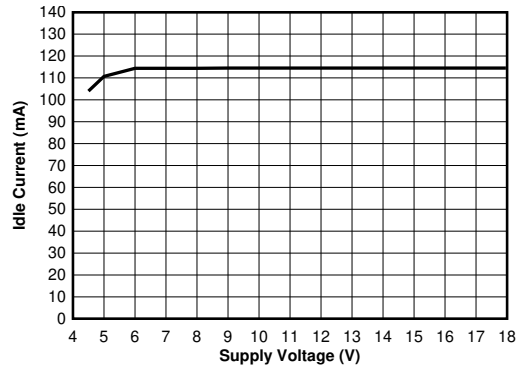
2 Ω T_C = 75 °C BTL

Figure 6-32. Power Dissipation vs Output Power - BTL, 2 Ω, 14.4 V, 1SPW



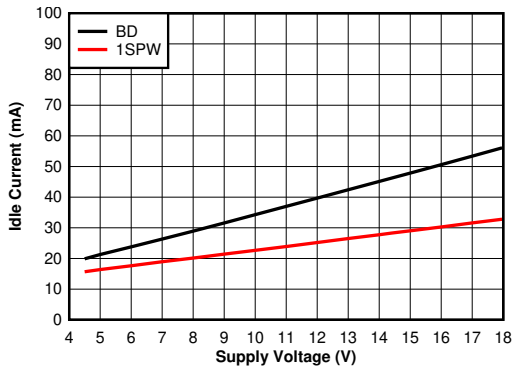
BTL

Figure 6-33. PVDD Idle Current vs Supply Voltage - BTL, 1SPW



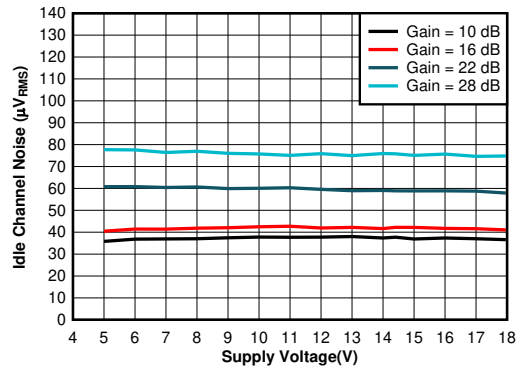
BTL

Figure 6-34. VBAT Idle Current vs Supply Voltage - BTL, 1SPW



F_{SW} = 384 kHz BTL

Figure 6-35. PVDD Idle Current vs Supply Voltage - BTL, 1SPW, 384 kHz

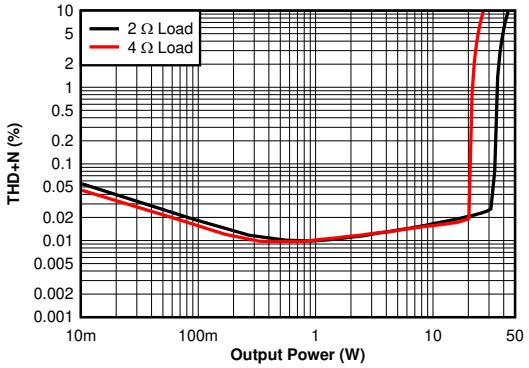


A-Weighted BTL

Figure 6-36. Noise vs Supply Voltage - BTL, 1SPW

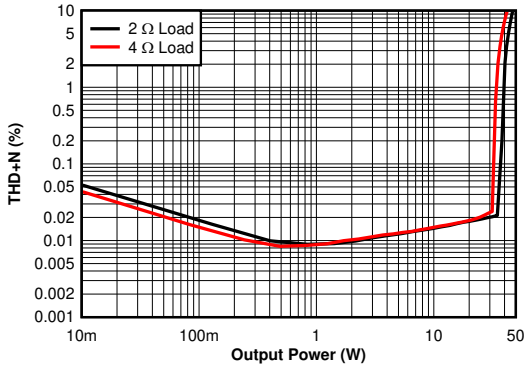
6.6.4 Bridge-Tied Load (BTL), 384 kHz, BD

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 384 kHz**, Gain = 22 dB, **BD Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 10 µH Sagami 7G14C-100M in 4 Ω/2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



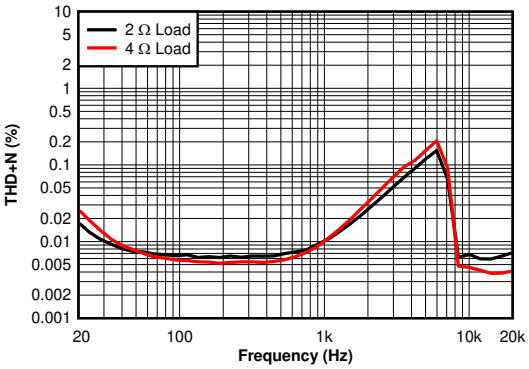
PVDD = 14.4V BTL

Figure 6-37. THD+N vs Power - 2 Ω, 4 Ω - 14.4 V



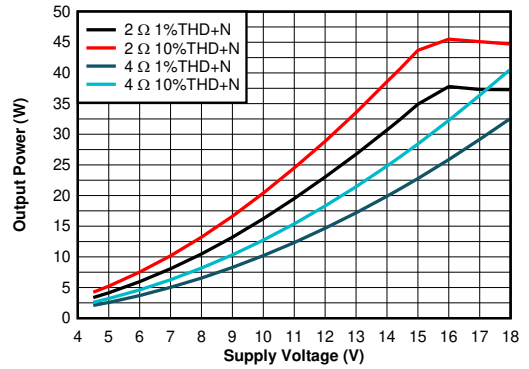
PVDD = 18V BTL

Figure 6-38. THD+N vs Power - 2 Ω, 4 Ω - 18 V



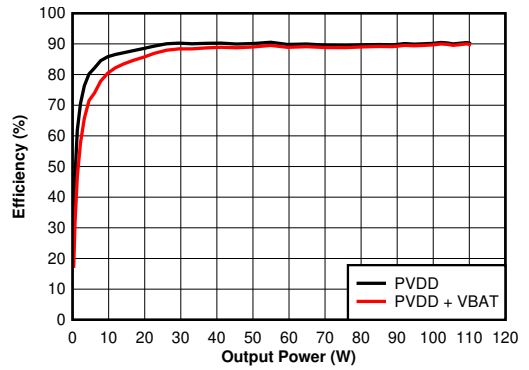
P_O = 1 W BTL

Figure 6-39. THD+N vs Frequency - 2 Ω, 4 Ω



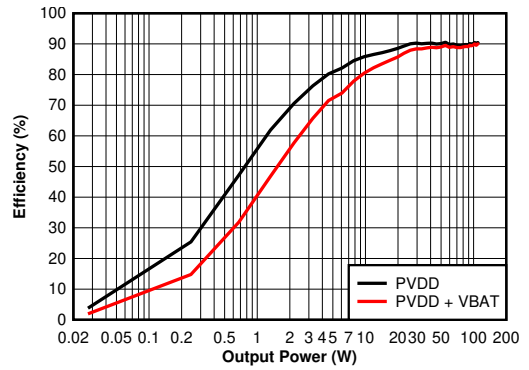
T_C = 75 °C BTL

Figure 6-40. Output Power vs Supply Voltage - 2 Ω 1%, 2 Ω 10%, 4 Ω 1%, 4 Ω 10%



4 Ω T_C = 75 °C BTL

Figure 6-41. Efficiency vs Output Power - 4 Ω

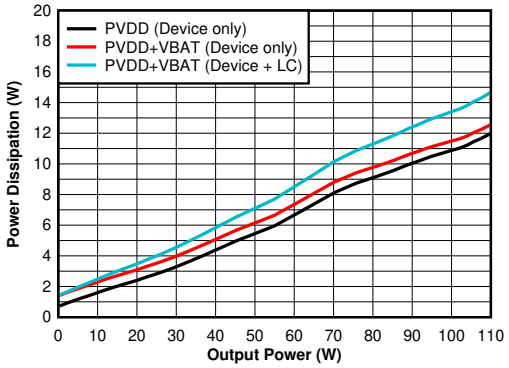


4 Ω T_C = 75 °C BTL

Figure 6-42. Efficiency vs Output Power - 4 Ω (Zoomed)

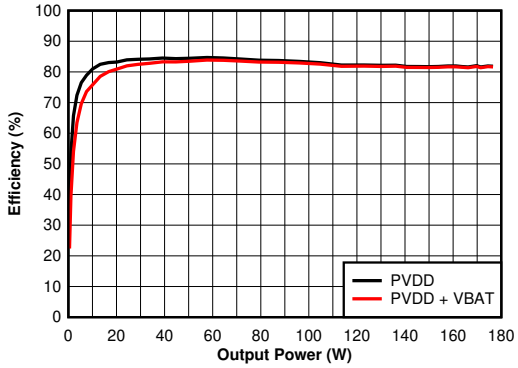
6.6.4 Bridge-Tied Load (BTL), 384 kHz, BD (continued)

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 384 kHz**, Gain = 22 dB, **BD Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 10 µH Sagami 7G14C-100M in 4 Ω/2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



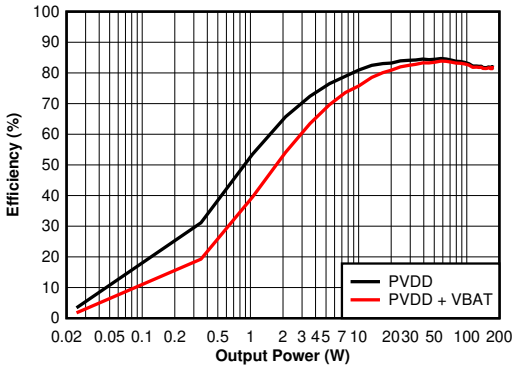
4 Ω T_C = 75 °C BTL

Figure 6-43. Power Dissipation vs Output Power - 4 Ω



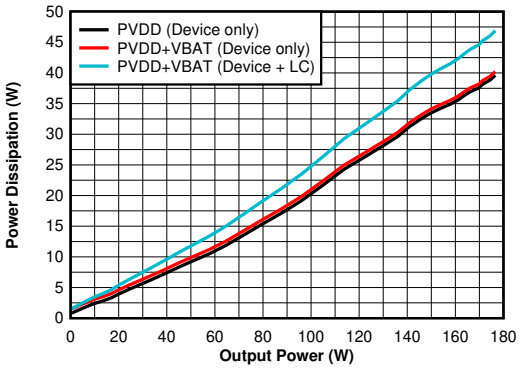
2 Ω T_C = 75 °C BTL

Figure 6-44. Efficiency vs Output Power - 2 Ω



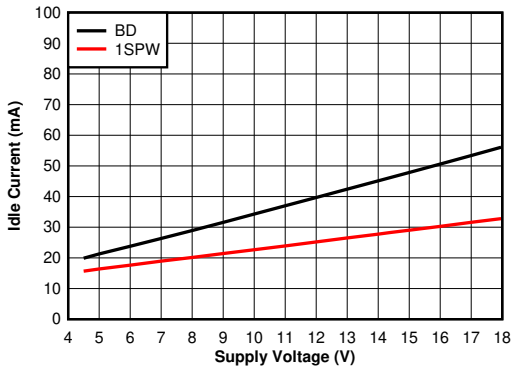
2 Ω T_C = 75 °C BTL

Figure 6-45. Efficiency vs Output Power - 2 Ω (Zoomed)



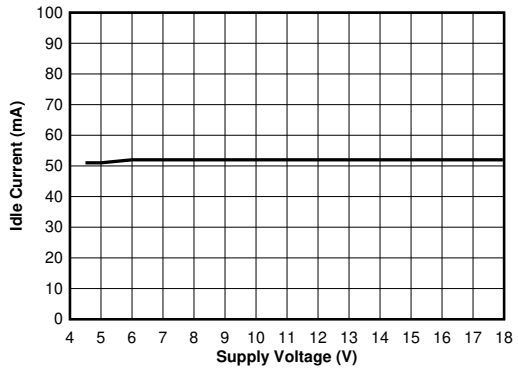
2 Ω T_C = 75 °C BTL

Figure 6-46. Power Dissipation vs Output Power - 2 Ω



BTL

Figure 6-47. PVDD Idle vs Supply Voltage

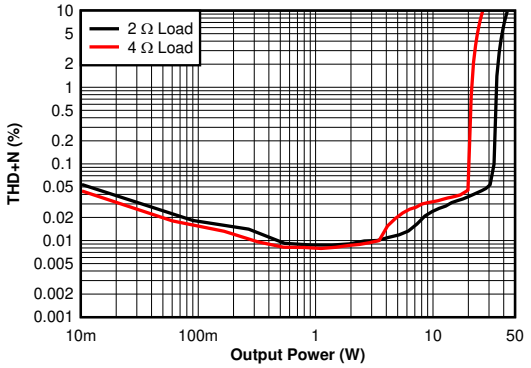


BTL

Figure 6-48. VBAT Idle Current vs Supply Voltage

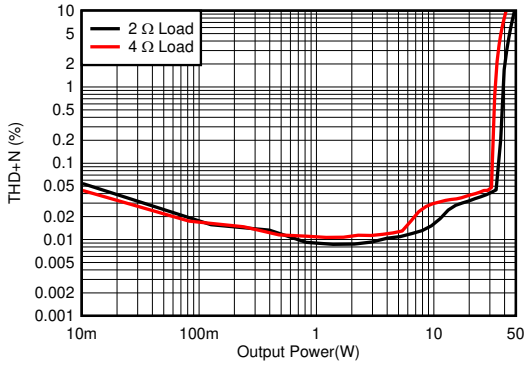
6.6.5 Bridge-Tied Load (BTL), 384 kHz, 1SPW

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 384 kHz**, Gain = 22 dB, **1SPW Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 10 µH Sagami 7G14C-100M in 4 Ω/2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



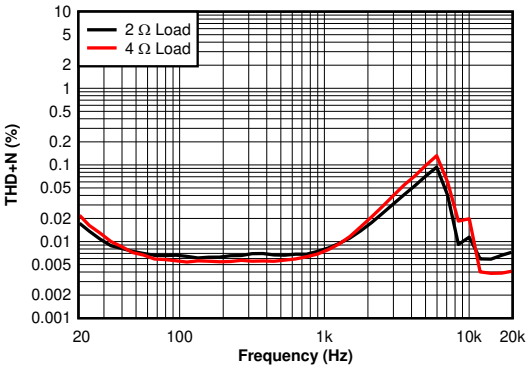
PVDD = 14.4V BTL

Figure 6-49. THD+N vs Power - 2 Ω, 4 Ω - 14.4 V



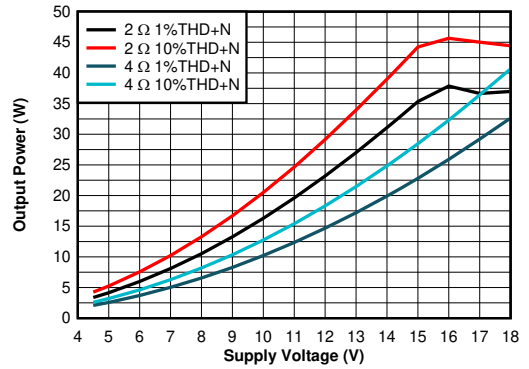
PVDD = 18V BTL

Figure 6-50. THD+N vs Power - 2 Ω, 4 Ω - 18 V



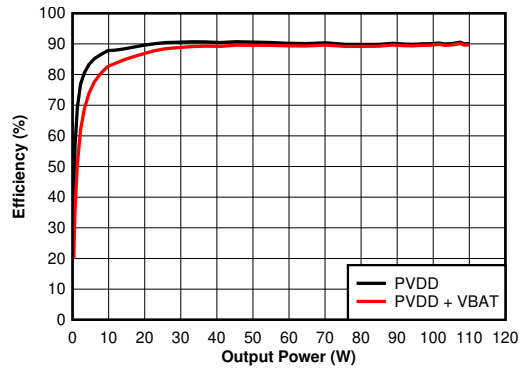
P_O = 1 W BTL

Figure 6-51. THD+N vs Frequency - 2 Ω, 4 Ω



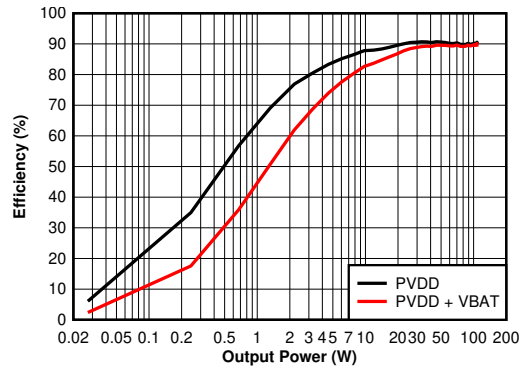
T_C = 75 °C BTL

Figure 6-52. Output Power vs Supply Voltage - 2 Ω 1%, 2 Ω 10%, 4 Ω 1%, 4 Ω 10%



4 Ω T_C = 75 °C BTL

Figure 6-53. Efficiency vs Output Power - 4 Ω

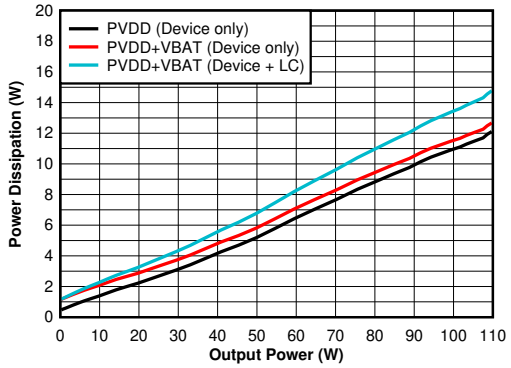


4 Ω T_C = 75 °C BTL

Figure 6-54. Efficiency vs Output Power - 4 Ω (Zoomed)

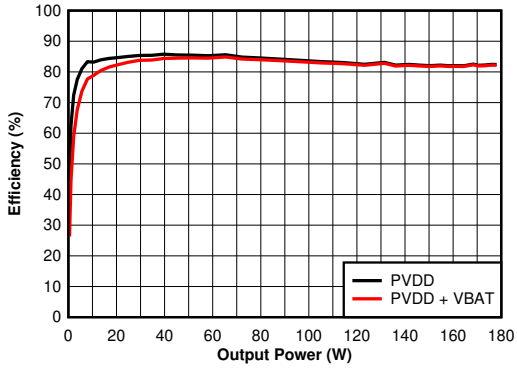
6.6.5 Bridge-Tied Load (BTL), 384 kHz, 1SPW (continued)

T_C = 25°C, PVDD = VBAT = 14.4 V, DVDD = 3.3 V, R_L = 4 Ω, P_{out} = 1 W/ch, f_{OUT} = 1 kHz, **F_{SW} = 384 kHz**, Gain = 22 dB, **1SPW Mode**, AES17 Filter, default I^2C settings, LC reconstruction filter: 10 µH Sagami 7G14C-100M in 4 Ω/2 Ω configuration and 1 µF (unless otherwise noted). See application diagram in Figure 8-2



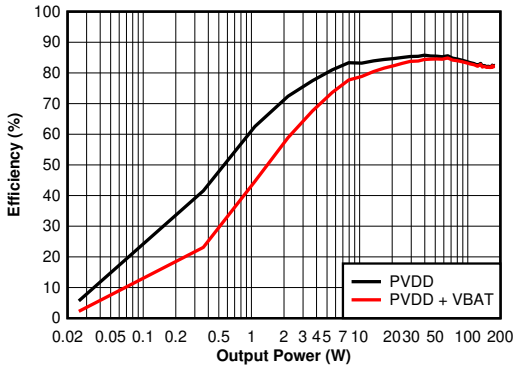
4 Ω T_C = 75 °C BTL

Figure 6-55. Power Dissipation vs Output Power - 4 Ω



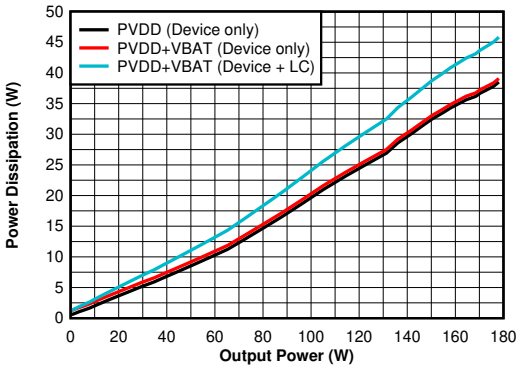
2 Ω T_C = 75 °C BTL

Figure 6-56. Efficiency vs Output Power - 2 Ω



2 Ω T_C = 75 °C BTL

Figure 6-57. Efficiency vs Output Power - 2 Ω (Zoomed)



2 Ω T_C = 75 °C BTL

Figure 6-58. Power Dissipation vs Output Power - 2 Ω

Parameter measurement information

The parameters for the TPA6304-Q1 device were measured using the circuit in Figure 8-2.

7 Detailed Description

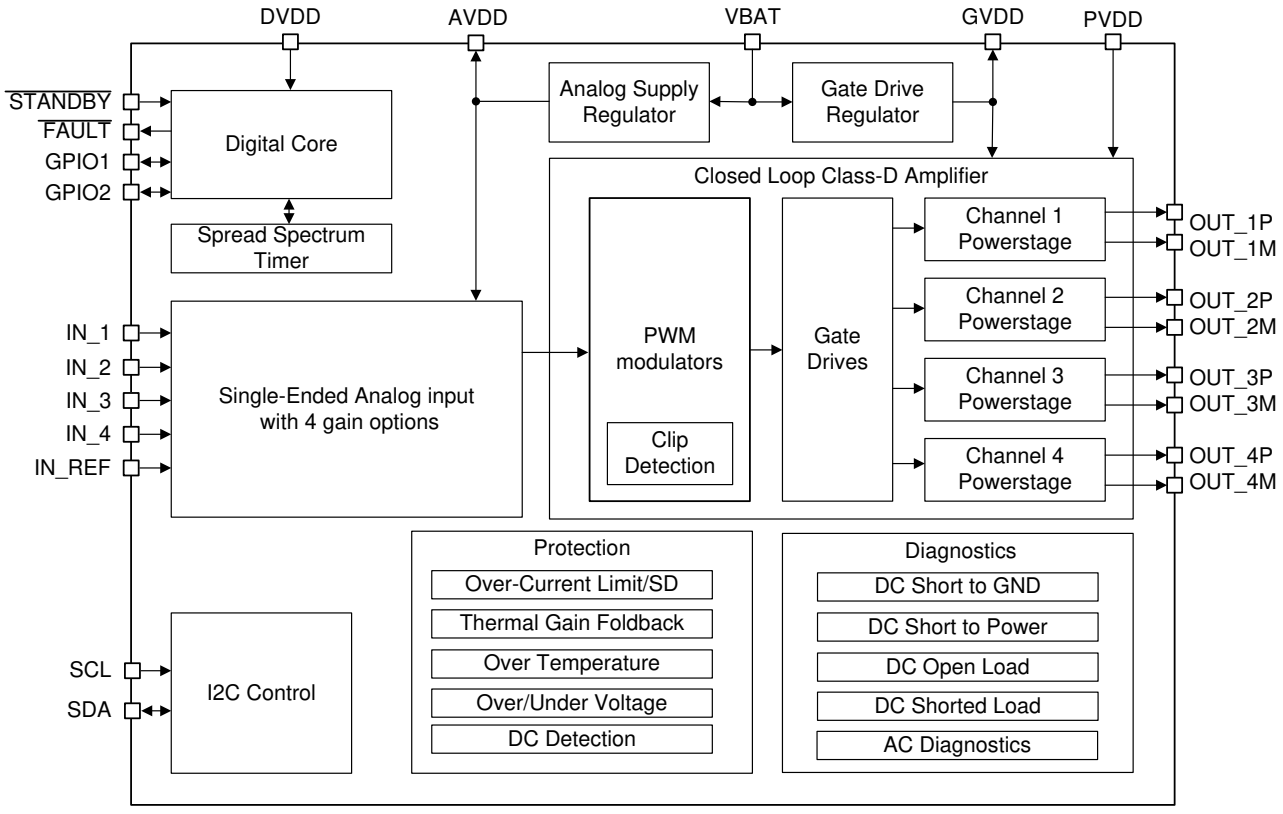
7.1 Overview

The TPA6304-Q1 device is a four-channel analog input Class-D audio amplifier, specifically designed for use in the automotive industry. The device is designed for vehicle battery operation. The ultra-efficient Class-D technology allows for reduced power consumption, PCB area, heat, and peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional Class-AB solutions.

The core design blocks are:

- Single-ended analog inputs
- Clock management
- Pulse width modulator (PWM) with output stage feedback
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Single-Ended Analog Inputs

The TPA6304-Q1 features single-ended analog audio inputs in combination with a reference ground input. Single-ended outputs available in the system are connected via AC coupling capacitors to the TPA6304-Q1 input pins. The TPA6304-Q1 IN_REF pin is connected via AC coupling capacitor and a separate line back to the ground reference point of the source of the single-ended audio signals.

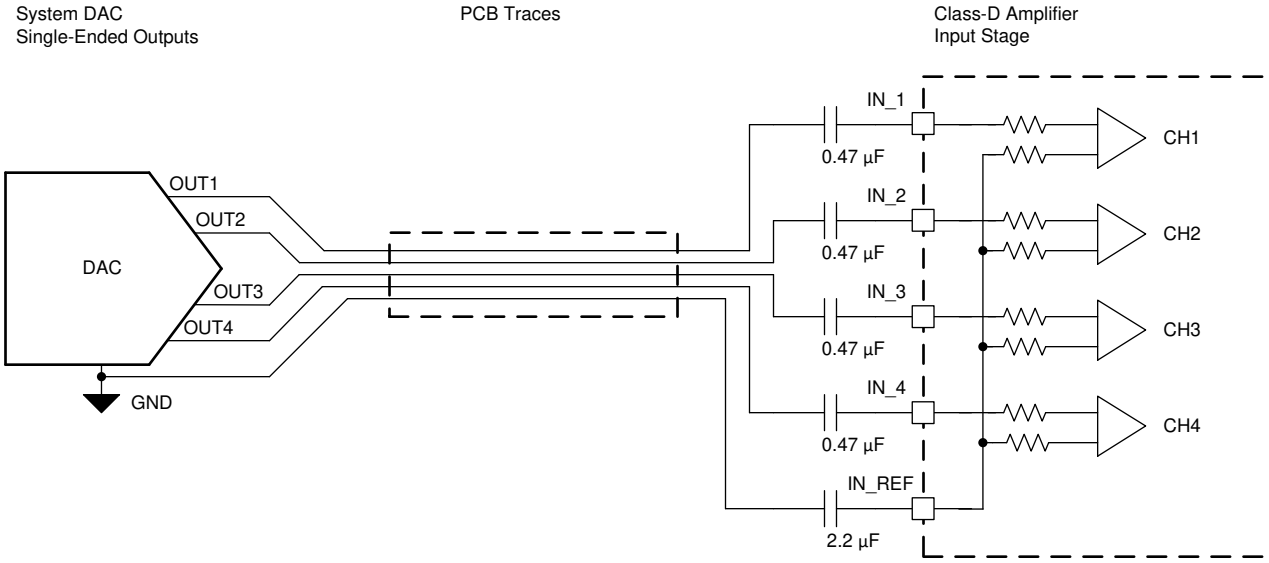


Figure 7-1. Single-Ended Analog Input Connections

7.3.2 Gain Control

The gain of the TPA6304-Q1 is configurable in the Miscellaneous Control Register 2 through I^2C. There are four gain settings of 10 dB, 16 dB, 22 dB, and 28 dB. 28 dB is the default setting. It is recommended to select the lowest possible gain for the expected PVDD operation and input voltage range to optimize dynamic range performance.

The combination of input voltage range and supply voltage sets the requirement for the chosen gain setting. In a typical application with maximum input signal amplitude of 0.5 V_{rms} and 14.4 V supply voltage the default gain of 28 dB allows for full output power of the device.

The input impedance for the IN_1, IN_2, IN_3 and IN_4 pins is typically 80 kΩ and independent of the gain setting. The input impedance for the IN_REF input is typically 20 kΩ.

The inputs need to be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. Time constants for all inputs, IN_1, IN_2, IN_3, IN_4 and IN_REF need to match. The input AC-coupling capacitor together with the input impedance forms a high-pass filter.

If a flat frequency response is required down to 20 Hz the recommended cut-off frequency is a fifth of that, 4 Hz. This can be achieved with a 0.47 µF ac-coupling capacitor.

It is recommenced to use AC-coupling capacitors with low leakage current, like ceramic-, film- or quality electrolytic-capacitors.

The TPA6304-Q1 has an output DC detection built in to protect the attached speaker in case an input AC-coupling capacitor fails or has too high leakage current.

7.3.3 Class-D Operation and Spread Spectrum Control

7.3.3.1 High Frequency Pulse Width Modulator (PWM)

The PWM converts the input audio data into a switched signal of varying duty cycle. The PWM modulator is an advanced design with high bandwidth, low noise, low distortion, and excellent stability.

The TPA6304-Q1, by default, generates its own internal clock signals. This mode of operation is called clock primary mode. The output switching rate is selectable via I²C, Miscellaneous Control Register 2. If desired, an external frequency source can be used to drive the switching output. This signal can be sent to the device using a GPIO Pin. The source frequency is 4x the selected switching frequency. By default, the four channels switches out of phase with a phase offset of 90 degrees between each channel. With 90 degree phase shift and 2.1 MHz switching frequency, the combined ripple current of all output channels are combined such that the effective ripple current has its fundamental at 8.4 MHz This enables the use of smaller and lower cost external filtering components due to lower power supply ripple.

For best EMI results the high frequency clock signals support spread spectrum control.

7.3.3.2 Clock Synchronization

The TPA6304-Q1 supports clock synchronization. During clock synchronization, one device is clock primary (Device A) sending out a synchronization clock and one device is clock secondary (Device B), receiving the synchronization clock. For Device A, set one of the GPIO Pins 'Sync Out'. By default Device A is in clock primary mode. The Sync Pin Control Register allows to set up Device B as clock secondary. Finally one GPIO Pin of Device B is set to 'Sync In' and the corresponding GPIO pins need to be connected on the PCB board.

Device B is frequency locked to one fourth of the received synchronization clock frequency. Device B creates an Invalid Clock Fault Event if the clock signal fed to the GPIO configured as clock sync input is out of nominal range.

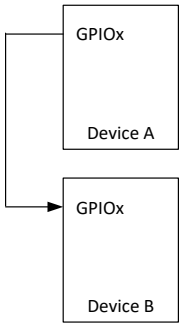


Figure 7-2. Clock Synchronization Diagram

7.3.3.3 Spread Spectrum Control

The TPA6304-Q1 offers spread spectrum control. Controlling the spectrum of the clock signal translates into an optimized behavior of higher frequency signal components which are visible during EMI testing. By default spread spectrum control is turned on and can be turned off in Spread Spectrum Control Register 2.

The four parameters SSC1, SSC2, SSC3 and SSC4 determine the spread spectrum behavior. The following predefined profiles determine allowed and supported combinations of SSCx settings and in addition define settings for the PWM Phase Control Register 1 and PWM Phase Control Register 2.

There are two Spread Spectrum profiles recommend in the TPA6304-Q1:

- Default Profile - optimized for best audio performance and efficiency with EMI performance that can meet most systems specifications.
- Low EMI - optimized for the lowest EMI for systems with stringent EMI system specficiations.

Table 7-1. Spread Spectrum Profiles

	SSC1[7:0]	SSC2[3:0]	SSC3[5:4]	SSC4[5:4]	PWM Phase Control 1	PWM Phase Control 2
Default	0x22	0x0	0x0	0x0	0x40	0x62
Low EMI	0x22	0x0	0x2	0x2	0x40	0x62

7.3.4 Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive the high-current, full-bridge, power-FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

The gate driver power supply voltage, GVDD, is internally generated and a decoupling capacitor must be connected at pin 5.

7.3.5 Power FETs

The BTL output for each channel comprises four N-channel 80 mΩ FETs for high efficiency and maximum power transfer to the load. These FETs are designed to handle large voltage transients during load dump.

7.3.6 Load Diagnostics

The device incorporates both DC- and AC- load diagnostics which are used to determine the status of the load. The DC-diagnostics are turned on by default. The AC-load diagnostics is turned off by default.

7.3.6.1 DC Load Diagnostics

The DC load diagnostics are used to verify the load is connected properly.

In order to support fast system level start up requirements to play audio:

- The diagnostics are available as soon as the device power supplies are within the recommended operating range.
- The diagnostics do not rely on external audio input signals or clock and sync frequencies to be available.

DC Diagnostics pass and allow a channel to enter MUTE or PLAY mode if the following tests pass on the output pins:

- No short to ground
- No short to power
- No shorted load
- No open load

On completion of the diagnostic routine where no fault is reported, the respective CH(i) LDG STATE REPORT bit of Channel State Report CH1, CH2 Register or Channel State Report CH3, CH4 Register is set high.

Any of the following conditions start the DC Load Diagnostics:

- Automatic DC load diagnostics at device initialization. Automatically on all four channels at device initialization: After DVDD power on reset (POR) and when STANDBY Pin transitions from low to high.
- Automatic DC load diagnostics during Hi-Z to MUTE or PLAY transition. When any channel is directed to leave the Hi-Z state and enter the MUTE or PLAY state.
- Manual start of DC load diagnostics. DC diagnostics can be enabled manually to run on any or all channels at any time.

7.3.6.1.1 Automatic DC Load Diagnostics at Device Initialization

The TPA6304-Q1 supports automatic and autonomous DC load diagnostics at device start up. With power stable, the device starts the internal power-on-reset. After completion of power-on-reset, the $\overline{\text{FAULT}}$ pin will be pulled high. The next low to high transition on $\overline{\text{STANDBY}}$ pin starts an automatic DC load diagnostics on all four channels.

No I^2C configuration nor any audio signals are necessary for the TPA6304-Q1 to perform short-to-power (S2P), short-to-ground (S2G), open load (OL), and shorted load (SL) based on default configuration. Systems can benefit from this autonomous operation as it is possible to run the load diagnostics while bringing up the digital part of the audio chain.

For each channel that yields a successful diagnostics test the CH(i) LDG STATE REPORT bit is set. For these channels, once the system is ready to set the channel status to PLAY mode, no further delay is introduced.

If the default values of automatic DC load diagnostics are not desired, the $\overline{\text{STANDBY}}$ pin can be held low until the device is fully configured via I^2C.

7.3.6.1.2 Automatic DC Load Diagnostics During Hi-Z to MUTE or PLAY Transition

By default, the LDG BYPASS bit in DC Load Diagnostics Control Register 1 is not set and the device starts the DC load diagnostics when $\overline{\text{STANDBY}}$ is high and a channel is leaving HiZ state before entering MUTE or PLAY state. If the automatic DC load diagnostics at device initialization already tested that channel with no faults reported then DC load diagnostics is bypassed.

If DC load diagnostics identifies a fault, the CH(i) LDG STATE REPORT bit in Channel State Report CH1, CH2 Register or Channel State Report CH3, CH4 Register stays low indicating 'DC Load Diagnostic did not complete without faults'. Details of the fault is reported in DC Load Diagnostic Report CH1, CH2 Register and DC Load Diagnostic Report CH3, CH4 Register. The channel is retested after approximately 750 ms until either the fault has been eliminated or the diagnostics function is turned off by I^2C control.

If DC load diagnostics completed successfully CH(i) LDG STATE REPORT bit is set high.

7.3.6.1.3 Manual Start of DC Load Diagnostics

Automatic DC load diagnostics may not be a desired function at power up. Setting the LDG ABORT bit in DC Load Diagnostics Control Register 1 disables automatic DC load diagnostics when pulling the $\overline{\text{STANDBY}}$ high. This register must be written before the $\overline{\text{STANDBY}}$ pin is pulled high.

Before a channel can enter PLAY mode, DC load diagnostics need to be started manually.

To run manual DC load diagnostics:

1. Set audio channel into Hi-Z mode by setting CH(i) STATE CONTROL of Channel State Control Register to '01'.
2. Write any desired control parameters for DC load diagnostics in DC Load Diagnostics Control Register 1, DC Load Diagnostics Control Register 2, DC Load Diagnostics Control Register 3, DC Load Diagnostics Control Register 4 and DC Load Diagnostics Control Register 5.
3. Set audio channel into Diag mode to start DC Diagnostics. For that, set CH(i) STATE CONTROL of Channel State Control Register to '11'.
4. Monitor (read) CH(i) STATE REPORT bits in Channel State Report CH1, CH2 Register and Channel State Report CH3, CH4 Register continuously until they change to '001'.
5. The DC load diagnostics results are stored in DC Load Diagnostic Report CH1, CH2 Register and DC Load Diagnostic Report CH3, CH4 Register.
6. For each channel that yields a successful diagnostics test the CH(i) LDG STATE REPORT bit is set in Channel State Report CH1, CH2 Register and Channel State Report CH3, CH4 Register. Once the system is ready to set the channel status to PLAY mode, no further delay is introduced.

7.3.6.1.4 Short-to-Ground

The short-to-ground (S2G) tests triggers a fault condition if there is a conductive path from output pin OUT_(i)M or OUT_(i)P of the tested channel (i) to GND with an impedance below that specified in the Specifications section.

7.3.6.1.5 Short-to-Power

The short-to-power (S2P) tests triggers a fault condition if there is a conductive path from output pin OUT_(i)M or OUT_(i)P of the tested channel (i) to a power rail with an impedance below that specified in the Specifications section. The diagnostic also detects a short to vehicle battery when the supply is boosted.

7.3.6.1.6 Shorted Load and Open Load

The shorted load (SL) test triggers a fault condition if the conductive path between the OUT_(i)M pin and OUT_(i)P pin of the tested channel (i) has an impedance below the threshold set in DC Load Diagnostics Control Register 4 and DC Load Diagnostics Control Register 5. The SL test has a configurable threshold depending on the expected load to be connected. Because the speakers and cable impedance connected to each channel might be different, each channel can be assigned a unique threshold value.

The open load (OL) test triggers a fault condition if the conductive path between the OUT_(i)M pin and OUT_(i)P pin of the tested channel (i) has an impedance higher than that specified in the Specifications section.

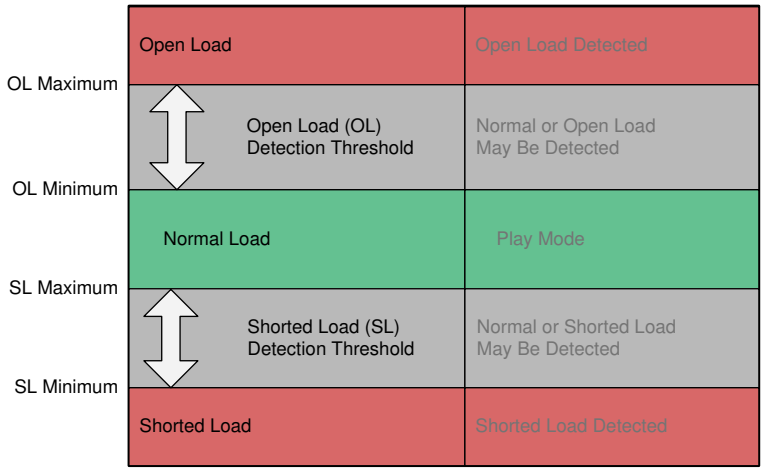


Figure 7-3. DC Load Diagnostic Reporting Thresholds

7.3.6.1.7 Line Output Diagnostics

The device also includes an optional test to detect a line output load (LO). DC Load Diagnostics Control Register 2 configures the channels that are enabled for LO testing. A line output load is a high-impedance load that is above the open load (OL) threshold such that the DC-load diagnostics report an OL condition. If the line output detection bit is set high, when an OL condition is detected during the DC Diagnostic test, the system also checks if a line output load is present. This test may not be pop free, so if an external amplifier is connected it should be muted.

7.3.6.2 AC Load Diagnostics

The AC load diagnostic is used to determine the proper connection of a capacitive coupled speaker or tweeter when used with a passive crossover. The AC load diagnostic is controlled through I^2C. The TPA6304-Q1 provides a required signal source to determine the AC impedance and reports the tweeter detection result back to I^2C registers. The I^2C selected test frequency should create current flow through the desired speaker for proper detection.

Note

If a fault occurs during AC diagnostics, the AC diagnostics is stopped. AC Diagnostics is not allowed to be performed again until the DC Diagnostics are performed. This is to ensure the fault is not potentially a hazard during AC diagnostics.

7.3.6.2.1 Operating Principal

The AC Load Diagnostic circuit of TPA6304-Q1 provides an internally generated stimulus to the load, captures the response of the load, provides real and imaginary parts of the captured complex load impedance and offers a magnitude estimator and tweeter detection comparator.

7.3.6.2.2 Stimulus

The frequency of the stimulus is set in AC Load Diagnostic Frequency Control Register. The device drives a low level, 10 mA output current through the load which does not create any significant sound pressure levels from the speaker.

7.3.6.2.3 Load Impedance

The load impedance as seen by the device is simply the ratio of voltage across the output pins and current flowing through the load.

Typically the load has a frequency dependent magnitude and causes current and voltage to have a phase shift. The TPA6304-Q1 internally captures the load impedance as a complex value consisting of a real and imaginary part. Expressing a load impedance in magnitude and phase or in real and imaginary part is mathematically

equivalent. Both forms can be transformed into each other without loss of information. After AC load diagnostics has finished the real and imaginary parts of the complex impedance are available for readout in I^2C registers starting with the AC Load Diagnostic Report Real Part CH1 Register.

7.3.6.2.4 Tweeter Detection

In most cases, it is sufficient to use the TPA6304-Q1 built-in magnitude estimator and tweeter detection report to perform the desired tweeter detection test. If a tweeter is properly connected in the system the magnitude of the load impedance is close to the nominal impedance of the speaker , for example 4 Ω. Once AC load diagnostics is finished, the magnitude of the load impedance is calculated and compared against a threshold set in the Tweeter Detection Threshold Register. If the measured impedance is lower than the set threshold, the tweeter is detected and marked accordingly in the Tweeter Detection Register.

7.3.6.2.5 Operation

To perform AC load diagnostics on TPA6304-Q1:

1. Use the Channel State Control Register to set the desired set of channels into Hi-Z mode.
2. Start the AC diagnostics by marking the channels in AC Load Diagnostic Control Register 1.
3. Poll the channel state from Channel State Report CH1, CH2 Register or Channel State Report CH3, CH4 Register. Once CH(i) STATE REPORT returns to 'Hi-Z' the AC load diagnostics results are ready for read out.

7.3.7 Power Supply

The device has three power supply inputs:

- DVDD – This pin is a 3.3 V supply pin that provides power to the digital circuitry.
- VBAT – This pin is a higher voltage supply that can be connected to the vehicle battery or the regulated voltage rail in a boosted system within the recommended limits. For best performance, this rail should be 10 V or higher. See the Recommended Operating Conditions table for the maximum supply voltage. This supply rail is used for higher voltage analog circuits but not the output FETs.
- PVDD – This pin is a high-voltage supply that can either be connected to the vehicle battery or to another voltage rail in a boosted system. The PVDD pin supplies the power to the output FETs and can be within the recommended operating limits, even if that is below the VBAT supply, to allow for dynamic voltage systems.

An on-chip regulator is included generating the GVDD voltage necessary for the gate drive circuitry. The GVDD supply pin is provided only for bypass capacitors to filter the supply and should not be used to power other circuits.

The device can withstand fortuitous open ground and power conditions within the Absolute Maximum Ratings for the device. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs.

7.3.7.1 Power-Supply Sequence

The device can accept any sequence of VBAT, PVDD and DVDD supply.

In a typical system, the VBAT and PVDD supplies are both connected to the vehicle battery and power up at the same time.

7.3.7.1.1 Power-Up Sequence

At power-up, the $\overline{\text{STANDBY}}$ pin is recommended to be kept low till all three power supply rails (VBAT, PVDD, DVDD) are within the Recommended Operating Conditions.

7.3.7.1.2 Power-Down Sequence

To power-down the device, first set the $\overline{\text{STANDBY}}$ pin low for at least 10ms before removing PVDD, VBAT or DVDD. After 10ms, the power supplies can be removed.

7.3.8 Device Initialization and Power-On-Reset (POR)

When the system first powers up, or when the DVDD voltage momentarily drops below the POR threshold, the devices initializes.

- During device initialization all I²C registers are be set to default values.
- The FAULT Pin is activated and taken low.
- The I²C device address is determined from the pull-up resistor on the $\overline{\text{FAULT}}$ pin. See I²C Address Selection for details.
- Once the device finished initialization, the open drain $\overline{\text{FAULT}}$ pin is released.

Figure 7-4 shows the time from DVDD voltage crossing the POR threshold to release of the $\overline{\text{FAULT}}$ pin is approximately 10 ms.

After the initialization, bit 4 of the Power Fault Memory Register indicates that the device went through a POR cycle. Reading this I²C register clears the fault signaling bit.

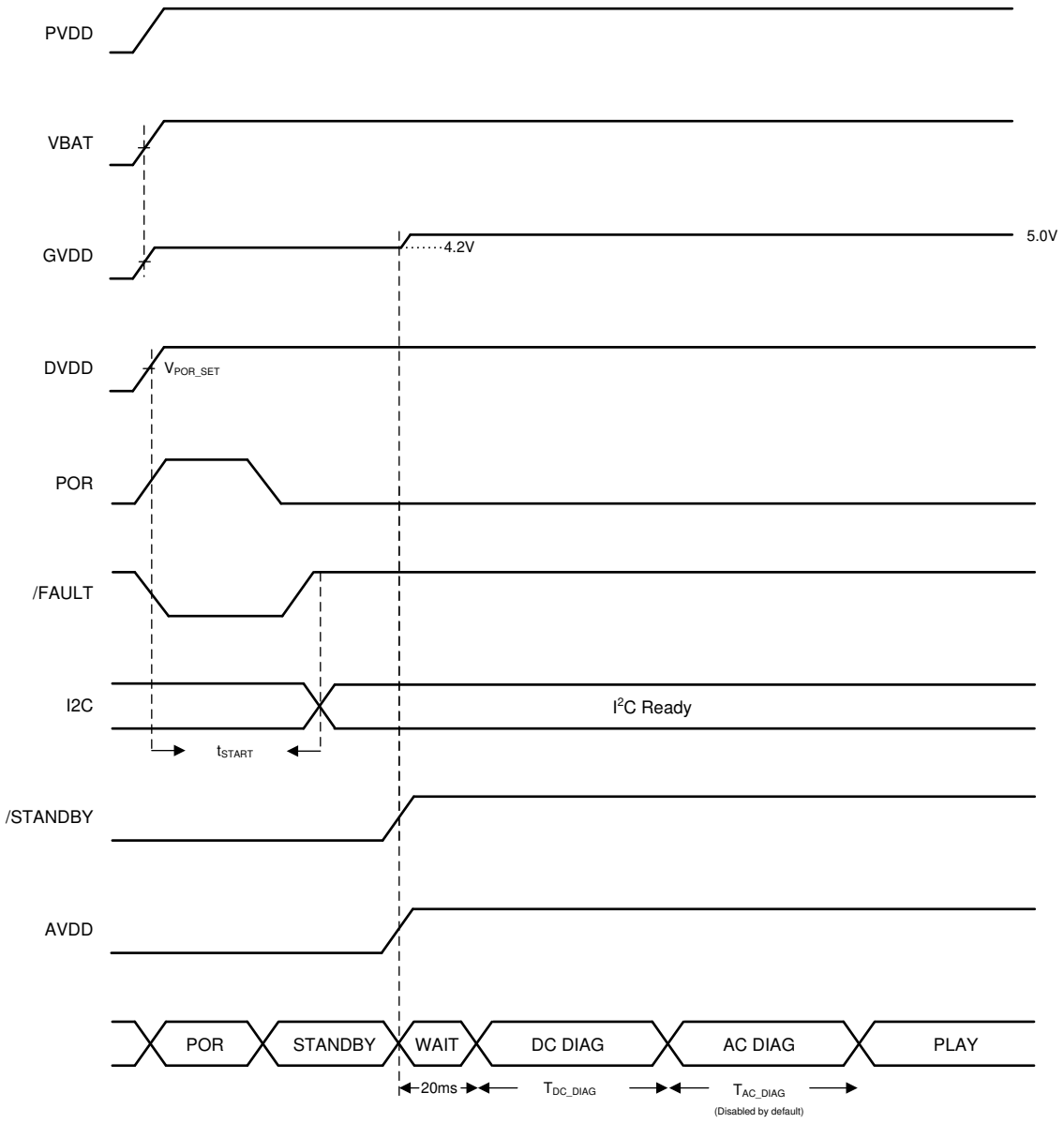


Figure 7-4. Typical Initialization Sequence and Timing

7.3.9 Protection and Monitoring

7.3.9.1 Over Current Protection

If the output load current reaches over current shutdown threshold, I_{SD}, such as during an output short to GND or power supply, then an Over Current Shut Down (OCSD) Event occurs which limits the peak current and

shuts down the affected channel. There are four programmable OC levels that determine I_{SD}. These can be set in Miscellaneous Control Register 1. The time to shutdown the channel varies depending on the severity of the short condition. The channel is placed into the PROTECTIVE SHUTDOWN State, the output stage is high impedance.

Based on the default configuration a fault signal is generated which by default generates an active low signal at the FAULT Pin.

7.3.9.2 DC Detect

The device monitors the DC offset continuously during normal operation at the output of the amplifier. If a channel's DC offset exceeds the DC_{FAULT} threshold, that channel triggers a DC Fault Event and is placed in the PROTECTIVE SHUTDOWN State. This puts the output stage in high impedance.

By default, when a DC Fault Event occurs, a fault signal generates an active low signal on the FAULT Pin.

7.3.9.3 Load Current Limit

Under normal operation, during high level music playback, it is possible that dynamic load currents can rise beyond the maximum load current, I_{LIM}, of the device. In these cases, the device dynamically limits the current into the load.

Each channel is independently monitored and limited. For each of the four over current (OC) levels that can be set in Miscellaneous Control Register 1, there is a corresponding I_{LIM} as shown in Specifications.

If the load current limit is active for at least 50% of a 200 ms window, the device generates a Load Current Warning Event for the affected channel.

In case the load current warning event is active continuously for 800 ms the device generates a Load Current Fault Event and the channel is placed in the PROTECTIVE SHUTDOWN State. This puts the output stage is high impedance.

If OC level 4 is configured in Miscellaneous Control Register 1, the device will also generate a Load Current Fault Event in case the load current limiter is active consecutively for more than 10 ms.

By default, a fault signal generates an active low signal on the FAULT Pin for when an OC event occurs.

7.3.9.4 Clip Detect

Each channel of the device monitors the output signal for situations at which the output voltage saturates and in response can create a Clip Warning Event. Configuring the Clip Detect Signal Configuration Register can enable clip detect, set the threshold at which clipping is detected to either 1%, 2%, 5% or 10%, and allows for mapping channel groups to signals. Setting up GPIO Configuration Register or FAULT Pin Configuration Register to output either Clip Detect Signal Group 1 or Clip Detect Signal Group 2 routes the signal through either Fault, GPIO1 or GPIO2 of the TPA6304-Q1.

7.3.9.5 Temperature Protection and Monitoring

The device monitors temperature with five temperature sensors. Every output channel has one temperature sensor in close proximity to monitor the temperature of it's respective channel. An additional sensor is located in a global position on the die, so it better represents the actual die junction temperature. Based on these sensors warning and fault signals can be generated. A Thermal Gain Foldback scheme is available that autonomously regulates audio gain and consequently limit die temperature.

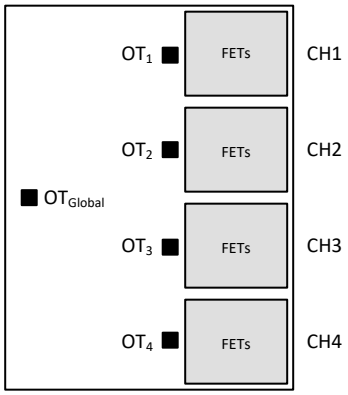


Figure 7-5. Temperature Sensor Locations Within the Device

7.3.9.5.1 Over Temperature Shutdown (OTSD)

The temperature threshold for global OTSD and the threshold for over temperature shutdown generated by the output channels, OTSD(i), are set to fixed values. Refer to Specifications for nominal temperature and recovery hysteresis values.

If the global junction temperature rises above the OTSD threshold, all channels are placed into a protective shutdown state. If the junction temperature of a channel rises above the OTSD threshold the affected channel is put into a protective shutdown state. and an Over Temperature Shut Down (OTSD) Event is created. If over temperature auto recovery is enabled, the effected channels recover the state they were in before OTSD occurred once temperatures have cooled down below respective thresholds. The tolerance of the warning levels and OTSD temperatures track each other.

By default, a fault signal generates an active low signal on the FAULT Pin for when an OTSD even occurs.

7.3.9.5.2 Over Temperature Warning (OTW)

The temperature threshold for global OTW has four levels and can be configured in Miscellaneous Control Register 1. The OTW generated by the output channels, OTW(i), are set to a fixed value. Refer to Specifications for nominal temperature and recovery hysteresis values.

During operation when the device heats up and crosses the threshold a global Over Temperature Warning Event is generated. Similarly, if the temperature at a channel raises above the threshold an Over Temperature Warning Event for that channel is generated. While the device continues to operate, the OTW information enables higher level software to make decisions to optimize thermal system performance.

Based on the default configuration a Warning Signal is generated. As described in the Warning Signal section the signal can either be polled via I^2C register or a hardware signal can be generated by use of a GPIO Pin or FAULT Pin.

7.3.9.5.3 Thermal Gain Foldback (TGFB)

The TGFB circuitry is designed to protect the TPA6304-Q1 from reaching excessive die temperatures. By default, the TGFB is enabled and the device automatically reduces the gain and thereby output power when either the global Over Temperature Warning Event (OTW) or any channel Over Temperature Warning Event, OTW(i) is active. Simultaneously on all channels, the gain is stepped down in 0.5 dB steps with a max attenuation of 12 dB. The gain increases as the temperature is reduced by the same gain step. The attack and release time of the TGFB can be programmed.

The Thermal Gain Foldback Control Register controls whether TGFB is enabled, the rate of gain reduction (attack) and the rate of gain increase or recovery (release). Pop free gain changes are controlled by enabling a zero crossing detector. The zero crossing has a wait time before the gain can change. By default, TGFB and zero crossing detector are enabled with a wait time of 20 µs. Zero Crossing behavior can be adjusted in the Thermal Gain Foldback Control Register. When Thermal Gain Foldback is engaged, that is when the gain is lower than 0 dB a Thermal Gain Foldback Warning Event is created.

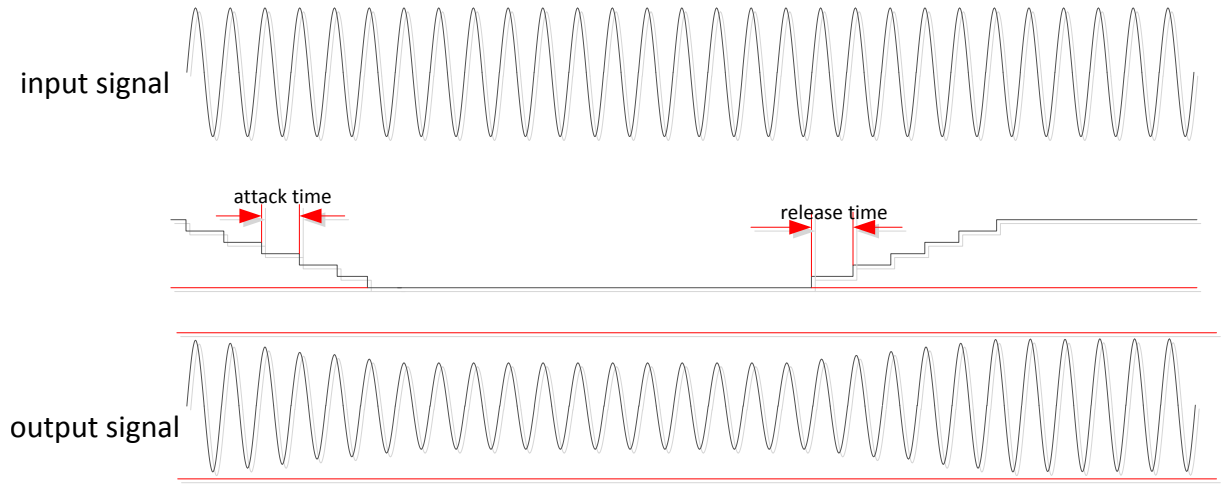


Figure 7-6. Thermal Foldback Attack and Release

7.3.9.6 Power Failures

The power supplies VBAT and PVDD are monitored for under-voltage and over-voltage events as described in section Power Fault Events. This automatically engages shutdown and protects the device. VBAT and PVDD safe operating voltage ranges can be found in the Recommended Operating Conditions table.

The device will shutdown if DVDD supply falls below V_{POR_OFF}. The DVDD POR fault event is described in section Power Fault Events.

7.3.9.7 Load Dump Protection

When supply voltages at the VBAT and PVDD pins rise, over voltage shutdown as described in section Power Fault Events engages and protects the device. The device can withstand 40 V load dump voltage spikes.

7.3.10 Hardware Control Pins

In addition to a $\overline{\text{STANDBY}}$ control pin and a $\overline{\text{FAULT}}$ status pin the device features the two general purpose IO pins GPIO1 and GPIO2. Each GPIO Pin can be configured as $\overline{\text{WARNING}}$ status pin, $\overline{\text{MUTE}}$ control pin, Sync Out or Sync In pin. For a complete list of pin configuration options please see Fault Pin Configuration Options and GPIO Pin Options.

7.3.10.1 $\overline{\text{FAULT}}$ Pin

By default, the $\overline{\text{FAULT}}$ pin is configured to output the Fault Signal as active low signal under any of the following conditions:

- Immediately following a power on reset (POR) until the device is ready to communicate via I^2C
- DC fault
- Over current shutdown
- Load current fault
- Over temperature shutdown

Configuration of the Fault Signal in Fault Signal Configuration Register 1 and Fault Signal Configuration Register 2 allows the fine tuning of the device response to fault events.

After power up, once I^2C communication is established the $\overline{\text{FAULT}}$ pin can be reconfigured to have different behavior. This does not affect the reporting register content of faults or the protection of the device.

Table 7-2. Fault Pin Configuration Options

Name	Description	Setup Code
Fault	**$\overline{\text{FAULT}}$ pin outputs Fault Signal, active low** (default)	**0000**
Warning	$\overline{\text{FAULT}}$ pin outputs Warning Signal, active low	0001

Table 7-2. Fault Pin Configuration Options (continued)

Name	Description	Setup Code
Clip Detect Group 1	$\overline{\text{FAULT}}$ pin outputs Clip Detect Signal Group 1, active high	0010
Clip Detect Group 2	$\overline{\text{FAULT}}$ pin outputs Clip Detect Signal Group 2, active high	0011

7.3.10.2 $\overline{\text{STANDBY}}$ Pin

The $\overline{\text{STANDBY}}$ pin is active low. The device is in a low current mode on the PVDD and VBAT pins while the output pins are placed into a Hi-Z state. All internal analog biases disabled. In $\overline{\text{STANDBY}}$ and while DVDD is present, the I^2C bus is active and the internal registers are active.

Internally this pin is connected to DVSS with a 100 kΩ pull-down resistor.

By default, the pin is configured in three level standby mode (TLSBY).

It is possible to communicate via I^2C while $\overline{\text{STANDBY}}$ pin is low and the $\overline{\text{STANDBY}}$ pin functionality can be set to two level mode by updating the TLSBY value of Micellaneous Control Register 4 during power up sequence.

Table 7-3. Two Level Mode

Input voltage at $\overline{\text{STANDBY}}$ pin	Device mode
GND	Standby
DVDD	Play

Table 7-4. Three Level Mode

Input voltage at $\overline{\text{STANDBY}}$ pin	Voltage Threshold	Device mode
GND	<0.5V	Standby
DVDD/2	DVDD/2 +/- 0.5V	Mute
DVDD	DVDD - 0.5V	Play

7.3.10.3 GPIO Pins

By default the two GPIO pins of the TPA6304-Q1 are in Hi-Z mode. During the initialization period of the system, when the device gets configured via GPIO Configuration Register, the function of the GPIO can be configured.

Table 7-5. GPIO Pin Options

Functionality	Mode	Description	Setup Code
Hi-Z	**Off**	**Pin continuously is in Hi-Z mode** (default)	**0000**
$\overline{\text{WARNING}}$	Open Drain Output	Warning Signal drives active low output	0001
$\overline{\text{FAULT}}$	Open Drain Output	Fault Signal drives active low output	0010
Clip Detect Group 1	Output Buffer	Clip Detect Signal Group 1 drives output	0011
Clip Detect Group 2	Output Buffer	Clip Detect Signal Group 2 drives output	0100
Sync Output	Output Buffer	Modulator frequency drives output	0101
H	Output Buffer	Pin continuously drives logic high output	0110
L	Output Buffer	Pin continuously drives logic low output	0111
Sync Input	Input	Input signal drives modulator	1000
$\overline{\text{MUTE}}$	Input	Active low input mutes the device	1001

7.3.10.4 $\overline{\text{WARNING}}$

The device does not have a dedicated $\overline{\text{WARNING}}$ status pin. Either GPIO1 or GPIO2 can be configured as $\overline{\text{WARNING}}$ pin via GPIO Configuration Register. Once configured, the GPIO outputs the warning signal as active low signal.

The Warning Signal section holds details on configuration options and default settings of the warning signal.

7.3.10.5 $\overline{MUTE}$

The device does not have a dedicated $\overline{MUTE}$ control pin. Either GPIO1 or GPIO2 can be configured as $\overline{MUTE}$ pin via GPIO Configuration Register. Once configured the GPIO is active low input and is used for hardware control of the mute and un-mute function for all channels. When the input signal is set low, all channels stop switching and are set to Hi-Z mode. All internal analog circuitry is biased and enabled, and the input ac-coupling capacitors are charged.

The hardware $\overline{MUTE}$ function is ORed with the I^2C $\overline{MUTE}$ function. If either function is set, the $\overline{MUTE}$ function is asserted.

7.4 Device Functional Modes

7.4.1 Internal Reporting Signals

To support software driver development, the TPA6304-Q1 allows the flexible configuration of internal fault, warning, and clip detect signals. These signals, where applicable, can be configured based on current device status registers or events stored in memory registers. Finally, these signals can be configured and routed to the Fault, GPIO1, or GPIO2 pins for signaling purposes. For details on configuration and routing, see the Fault, Warning and Clip Detect Signal Creation and Configuration section.

7.4.1.1 Fault Signal

Automotive systems have a high demand on gathering device information in case of unexpected conditions. The Fault Signal Configuration Register 1 and Fault Signal Configuration Register 2 of the TPA6304-Q1 allow for a flexible configuration of information necessary for higher level system software to effectively control the system.

The Fault Signal can be configured to be active in response to the following Fault Events:

- Over current shutdown, typically caused by shorts to power or short to ground (latched)
- Shutdown due to DC detection (latched)
- Load current failures, typically caused by shorted load (latched)
- Power failures (latched or non-latched)
- Over-temperature failures (latched or non-latched)
- Clock sync failures, if the device is in clock slave mode (latched or non-latched)
- Channel 1, 2, 3 or 4 in protective shutdown state
- Incomplete diagnostics
- Warning Signal being active

The Fault Signal, by default, gets routed to a GPIO Pin to create a HW signal. Its state can be polled by I^2C read at any time from OTSD CS Fault Status Register.

7.4.1.2 Warning Signal

The Warning Signal can be configured to be active in response to following Warning Events:

- Over-temperature warning (latched or non-latched)
- Thermal Gain Foldback being activated (latched or non-latched)
- Load current warning (latched)
- Power failures (latched or non-latched)
- Over temperature failures (latched or non-latched)
- Clip Detect (latched or non-latched)
- Incomplete diagnostics
- Clock sync failures, if the device is in clock secondary mode (latched or non-latched)

By default, the Warning Signal is active in response to latched over temperature warning events.

The Warning Signal can be routed to a GPIO Pin to create a HW signal or its state can be polled by I^2C read at any time from OTSD CS Fault Status Register.

7.4.1.3 Clip Detect Signal

The clip detect signal can be routed out of the TPA6304-Q1 to support hardware control loops that limit THD in the event of excessively large audio signals. Two independent clip detect signals can be generated. The clip detect signal is based on clip detect warning events.

Section Clip Detect describes the circumstances under which the device creates clip detect warning signals. Each output channel independently creates a clip detect warning signal.

Clip Detect Signal Group 1 can be configured in the Clip Detect Signal Configuration Register to be active when either CH1 or CH2 create a clip detect warning, CH3 or CH4 create a clip detect warning, or any of the four channels creates a clip detect warning.

Clip Detect Signal Group 2 can be configured in the same way as Clip Detect Signal Group 1.

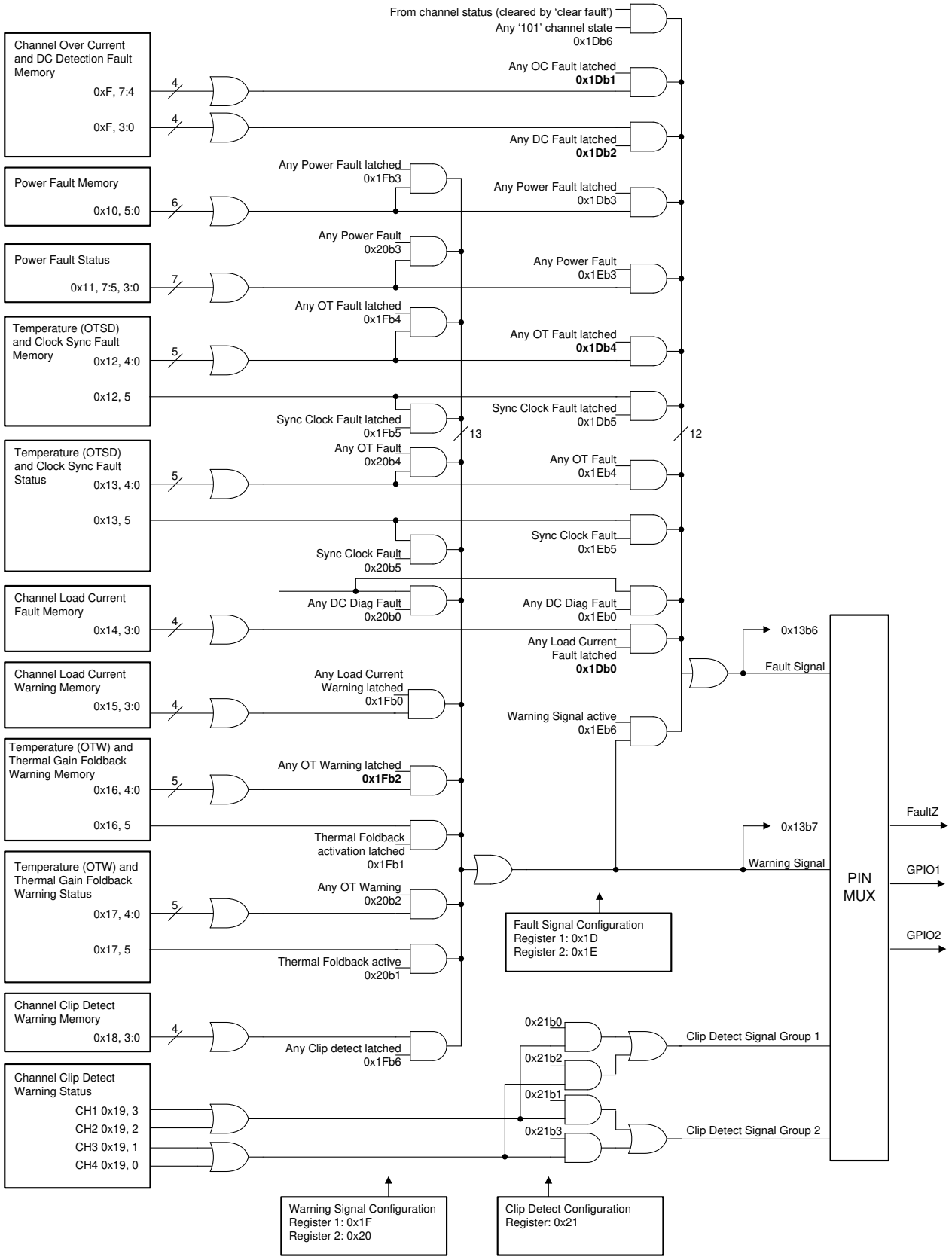


Figure 7-7. Fault, Warning and Clip Detect Signal Creation and Configuration

7.4.2 Device States and Flags

7.4.2.1 Audio Channel States

Every audio channel has its set of states that carefully control the set up and shut down procedure of an audio path from source to load. These states are listed in Audio Channel States, Channel states get reported in Channel State Report CH1, CH2 Register and Channel State Report CH3, CH4 Register.

Table 7-6. Audio Channel States

STATE NAME	OUTPUT FETS	OSCILLATOR	I²C
DIAG	Hi-Z	Stopped	Active
Hi-Z	Hi-Z	Active	Active
MUTE	Hi-Z	Active	Active
PLAY	Switching with audio	Active	Active
PSD	Hi-Z	Active	Active
PSD_AR	Hi-Z	Active	Active

7.4.2.1.1 PROTECTIVE SHUTDOWN with AUTO RECOVERY State

If one or more channels of the device are in PLAY state the device may need to take protective actions and shutdown one or more audio channels. The output FETs of the affected channels are turned off and the output pins are high impedance. Once the cause for the protective shutdown is no longer present, the device resumes back to PLAY. The reported state for affected channels is PROTECTIVE SHUTDOWN with AUTO RECOVERY

Possible reason for individual channels to enter this state is:

- Channel over temperature shutdown (OTSD(i))

Possible reasons for all channels to enter this state are:

- Power failures
- Invalid Clock
- Global over temperature shutdown (OTSD)

The following registers hold all information necessary to identify the reason for the device being in this state:

- Temperature (OTSD) and Clock Sync Fault Status Register
- Power Fault Status Register

7.4.2.1.2 PROTECTIVE SHUTDOWN State

If one or more channels of the device are in PLAY state the device may need to take protective actions and shutdown one or more audio channels. The output FETs of the affected channels is turned off and the output pins are high impedance. The reported state for affected channels is PROTECTIVE SHUTDOWN

Possible reasons for individual channels to enter this state are:

- Over Current Shutdown
- Load Current Fault
- DC fault
- Channel over temperature shutdown (OTSD(i))

Possible reason for all channels to enter this state is:

- Global over temperature shutdown (OTSD)

The following registers hold all information necessary to identify the reason for the device being in this state:

- Temperature (OTSD) and Clock Sync Fault Status Register
- Channel Over Current and DC Detection Fault Memory Register
- Channel Load Current Fault Memory Register

7.4.2.1.2.1 Clear Fault

Note

If one or more channels are in PROTECTIVE SHUTDOWN State, the channel faults only recover after setting the CLEAR FAULT bit in the Miscellaneous Control Register 3.

This clears the faults and set channels into Hi-Z mode.

7.4.2.2 Status and Memory Registers

7.4.2.2.1 Status Registers

The device reports device states and environmental information by means of status and reporting registers. The following set of registers, at any time, hold the full set of device status:

- Channel State Report CH1, CH2 Register
- Channel State Report CH3, CH4 Register
- Power Fault Status Register
- Temperature (OTSD) and Clock Sync Fault Status Register
- Temperature (OTW) and Thermal Gain Foldback Warning Status Register
- Thermal Gain Foldback Status Register

Interrupt driven signaling to the controlling host device is supported by creation of events. Events can be configured to create Warning Signal and Fault Signal.

Alternatively software can routinely read this set of registers to gather device status (polling mode).

7.4.2.2.2 Memory Registers

The device provides a set of memory registers which latch events. This allows software drivers to properly analyze fault situations.

The following set of memory registers is available:

- Channel Over Current and DC Detection Fault Memory Register
- Power Fault Memory Register
- Temperature (OTSD) and Clock Sync Fault Memory Register
- Channel Load Current Fault Memory Register
- Channel Load Current Warning Memory Register
- Temperature (OTW) and Thermal Gain Foldback Warning Memory Register
- Channel Clip Detect Warning Memory Register

The memory registers, for example, support the following scenarios:

- The output pin of the device gets shorted to ground, the device reacts immediately and goes into PROTECTIVE SHUTDOWN State. The software device driver may want to identify why the device is in protective shutdown mode and reads the registers described in the PROTECTIVE SHUTDOWN State section.
- The digital power rail just came up or dropped below POR levels. The device resets all settings and indicates that in the Power Fault Memory Register with the DVDD POR STORED bit set.
- The device heated up and temporarily reducing audio gain. Software can check whether this situation has happened since the last read of Temperature (OTW) and Thermal Gain Foldback Warning Memory Register.

Note

Memory registers only provide information to the controlling host. Reading the memory register clears the content. The status of the device does not change by reading the memory registers.

7.4.3 Fault Events

7.4.3.1 Overview

The device creates fault events as outlined in Details On Generated Fault Events.

Table 7-7. Details On Generated Fault Events

Fault Event	Typical Reason	Channel Status Reporting [1]	Required User Response	Current status (non-latched) reported in	Event latched and reported in [2]
VBAT Over Voltage Fault	VBAT above limit	'100' PROTECTIVE SHUTDOWN with AUTO RECOVERY State	Apply VBAT within spec	Power Fault Status Register	Power Fault Memory Register
VBAT Under Voltage Fault	VBAT below limit		Apply VBAT within spec		
PVDD Over Voltage Fault	PVDD above limit		Apply PVDD within spec		
PVDD Under Voltage Fault	PVDD below limit		Apply PVDD within spec		
GVDD Fault	GVDD regulator fault				
DVDD POR	DVDD voltage dropped below POR limit or initial device startup	'001' Hi-Z State	Write initial device configuration via I^2C	N/A	
Over Temperature SD - Channel	Channel temperature above limit	'101' PROTECTIVE SHUTDOWN State	Clear Fault	Temperature (OTSD) and Clock Sync Fault Status Register	Temperature (OTSD) and Clock Sync Fault Memory Register
Over Temperature SD - Global	Die temperature above limit				
Over Current Shut Down (OCSD) Event	Short to ground or short to power	'101' PROTECTIVE SHUTDOWN State	Clear Fault	N/A	Channel Over Current and DC Detection Fault Memory Register
DC Fault Event	DC voltage at device input				
Load Current Fault Event	Shorted load				Channel Load Current Fault Memory Register
Invalid Clock Fault Event	Missing clock signal while device set up as clock slave	'100' PROTECTIVE SHUTDOWN with AUTO RECOVERY State	Apply sync clock signal within nominal range	Temperature (OTSD) and Clock Sync Fault Status Register	Temperature (OTSD) and Clock Sync Fault Memory Register
If 'OTSD auto recovery' is enabled in Miscellaneous Control Register 3:					
Over Temperature SD- Channel	Channel temperature above limit	'100' PROTECTIVE SHUTDOWN with AUTO RECOVERY State	Cool down device	Temperature (OTSD) and Clock Sync Fault Status Register	Temperature (OTSD) and Clock Sync Fault Memory Register
Over Temperature SD - Global	Die temperature above limit				

7.4.3.2 Power Fault Events

Current status of power fault events is reported in Power Fault Status Register and latched events are reported in Power Fault Memory Register

[1] See Channel State Report CH1, CH2 Register and Channel State Report CH3, CH4 Register for details.
[2] Reading the memory register clears its content. This does not clear fault conditions.

7.4.3.2.1 DVDD POR

When DVDD falls below V_{POR_OFF} the device shuts down. All channels are brought into Hi-Z State and I^2C communication terminates. When DVDD comes back up above V_{POR_SET} or when the device gets first powered up and DVDD rises above V_{POR_SET} the device initiates a Power-On-Reset routine. During this routine all registers and device states are set to default values. It is intended behavior that Power Fault Memory Register reports "DVDD power on reset event stored" after power up.

As DVDD POR is a transient event it is not reported in the Power Fault Status register.

7.4.3.2.2 VBAT Over Voltage Fault

When the VBAT supply rail rises above nominal range a VBAT Over Voltage Fault event is created and the device enters into PROTECTIVE SHUTDOWN with AUTO RECOVERY State. Once VBAT falls back down into nominal range, the fault event is cleared.

7.4.3.2.3 VBAT Under Voltage Fault

When the VBAT supply rail falls below nominal range a VBAT Over Voltage Fault event is created and the device enters into PROTECTIVE SHUTDOWN with AUTO RECOVERY State. Once VBAT rises back up into nominal range, the fault event is cleared.

7.4.3.2.4 PVDD Over Voltage Fault

When the PVDD supply rail rises above nominal range a PVDD Over Voltage Fault event is created and the device enters into PROTECTIVE SHUTDOWN with AUTO RECOVERY State. Once PVDD falls back down into nominal range, the fault event is cleared.

7.4.3.2.5 PVDD Under Voltage Fault

When the VBAT supply rail falls below nominal range a PVDD Under Voltage Fault event is created and the device enters into PROTECTIVE SHUTDOWN with AUTO RECOVERY State. Once PVDD rises back up into nominal range, the fault event is cleared.

7.4.3.2.6 GVDD Fault

This fault indicates a fault condition of the internal gate drive circuitry.

7.4.3.3 Over Temperature Shut Down (OTSD) Event

Section Over Temperature Shutdown describes the circumstances under which the device creates an OTSD event.

Current status of over termperature is reported in Temperature (OTSD) and Clock Sync Fault Status Register and latched events are reported in Temperature (OTSD) and Clock Sync Fault Memory Register

By default, if temperatures rise above the OTSD threshold the device is in PROTECTIVE SHUTDOWN State. Setting the 'OTSD auto recovery' bit in Miscellaneous Control Register 3 configures the device to be in PROTECTIVE SHUTDOWN with AUTO RECOVERY State while temperatures are above OTSD thresholds.

7.4.3.4 Over Current Shut Down (OCSD) Event

Section Over current protection describes the circumstances under which the device creates an OCSD event.

As Over Current Shut Down (OCSD) Event is a transient event it is not reported in a status register. The latched OCSD events are reported in Channel Over Current and DC Detection Fault Memory Register. Affected channels are in PROTECTIVE SHUTDOWN State.

Over Current Shut Down (OCSD) Event also triggers when Load Current Fault Event triggers.

7.4.3.5 DC Fault Event

The DC Detect section describes the circumstances under which the device creates a DC fault event.

As DC Fault Event is a transient event it does not report in a status register. The latched DC fault events are reported in Channel Over Current and DC Detection Fault Memory Register. Affected channels are in PROTECTIVE SHUTDOWN State.

7.4.3.6 Load Current Fault Event

The Load Current Limit section describes the circumstances under which the device creates a load current fault event. This is a transient event that only lasts for a limited time. The device latches the event in Channel Load Current Fault Memory Register.

7.4.3.7 Invalid Clock Fault Event

The Clock Synchronization section describes how two devices operate with synchronized clocks. The device in clock slave mode receives a sync clock. If this sync clock is out of nominal frequency range or suddenly stops, an Invalid Clock Fault Event is created and the device gracefully tranistions to the PROTECTIVE SHUTDOWN with AUTO RECOVERY State. Once sync clock comes back into nominal frequency range the fault events are cleared and the device auto recovers.

Current status is reported in Temperature (OTSD) and Clock Sync Fault Status Register and the latched event is reported in Temperature (OTSD) and Clock Sync Fault Memory Register.

7.4.4 Warning Events

7.4.4.1 Overview

The device creates warning events as outlined in Table 7-8.

Table 7-8. Details On Generated Warning Events

Warning Event	Typical Reason	Current status (non-latched) reported in	Event latched and reported in
Over Temperature - Channel	Channel temperature above warning threshold	Temperature (OTW) and Thermal Gain Foldback Warning Status Register	Temperature (OTW) and Thermal Gain Foldback Warning Memory Register
Over Temperature - Global	Die temperature above warning threshold		
Thermal Gain Foldback active	Die temperature above threshold and TGFB enabled		
Load Current - Channel	Peak current into load reaches maximum	N/A	Channel Load Current Warning Memory Register
Clip Warning Event	Output voltage saturation	Channel Clip Detect Warning Status Register	Channel Clip Detect Warning Memory Register

7.4.4.2 Over Temperature Warning Event

Section Over Temperature Shutdown describes the circumstances under which the device creates an Over Temperature Warning event.

Thermal Gain Foldback, when enabled, responds to over temperature warning events.

Current status is reported in Temperature (OTW) and Thermal Gain Foldback Warning Status Register and latched events are reported in Temperature (OTW) and Thermal Gain Foldback Warning Memory Register.

7.4.4.3 Thermal Gain Foldback Warning Event

When Thermal Gain Foldback is enabled and if it has reduced the gain below 0 dB due to high temperature, the device creates a thermal gain foldback warning event. Once the temperature decreases and the gain foldback circuitry releases the gain back up to 0 dB, this warning is cleared. Current status is reported in Temperature (OTW) and Thermal Gain Foldback Warning Status Register and latched events are reported in Temperature (OTW) and Thermal Gain Foldback Warning Memory Register.

7.4.4.4 Load Current Warning Event

Section Load current limit describes the circumstances under which the device creates a load current warning event. The device latches the event in Channel Load Current Warning Memory Register. As this is a transient event it is not reported in a status register.

7.4.4.5 Clip Warning Event

Section Clip Detect describes the circumstances under which the device creates a clip warning event.

Current clip warning status is reported in Channel Clip Detect Warning Status Register and latched events are reported in Channel Clip Detect Warning Memory Register.

7.5 Programming

7.5.1 I²C Serial Communication Bus

The device communicates with the system processor via the I²C serial communication bus as an I²C slave-only device. The processor can poll the device via I²C to determine the operating status, configure settings, or run diagnostics. For a complete list and description of all I²C controls, see the *Register Maps* section.

7.5.1.1 I²C Address Selection

The device supports two I²C addresses, so up to two devices can be used together in a system with no additional bus switching hardware. The pull up resistor connected to the device $\overline{\text{FAULT}}$ pin and DVDD determines the I²C address during power up. If two devices are present in a system their $\overline{\text{FAULT}}$ pin outputs must not be shared in order for the I²C address detection circuitry to operate correctly. The slave addresses of the device are listed in I²C Addresses.

Table 7-9. I²C Addresses

DESCRIPTION	$\overline{\text{FAULT}}$ pin pull up resistor value	I²C Write	I²C Read
Device 0	Floating	0x58	0x59
Device 1	47k	0x5A	0x5B

7.5.2 I²C Bus Protocol

The device has a bidirectional serial control interface that is compatible with the Inter IC (I²C) bus protocol and supports 100 and 400-kbps data transfer rates for random and sequential write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I²C bus uses two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The device holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

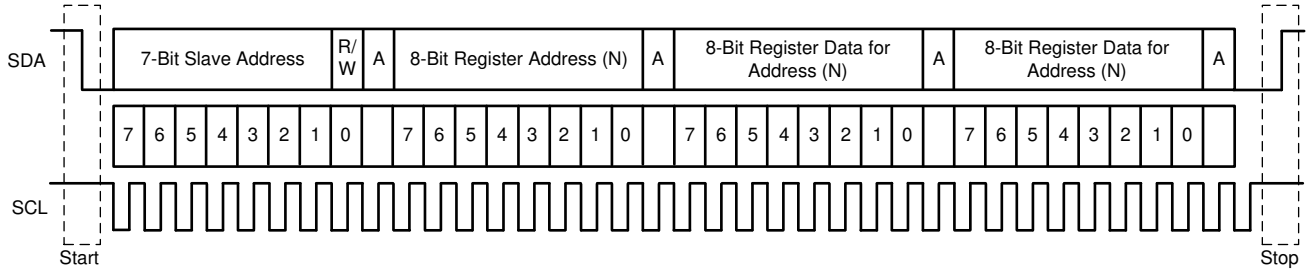


Figure 7-8. Typical I²C Sequence

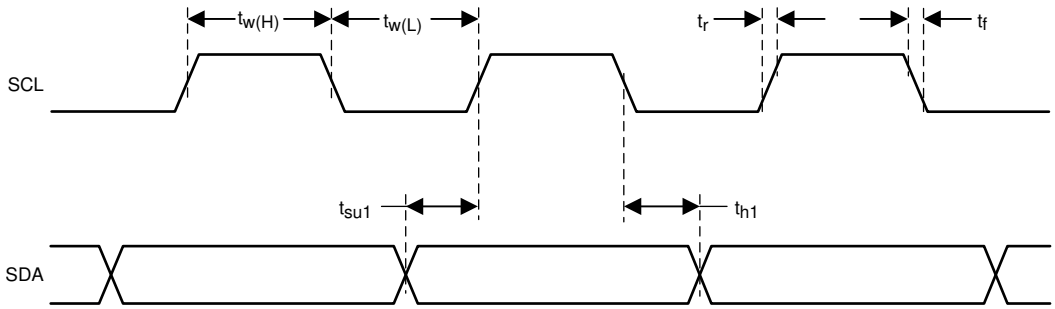


Figure 7-9. SCL and SDA Timing

Use the I²C ADDRx pins to program the device slave address. Read and write data can be transmitted using single-byte or multiple-byte data transfers.

7.5.2.1 Random Write

As shown in Random Write Transfer, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit is a 0. After receiving the correct I²C device address and the read/write bit, the device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data

byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

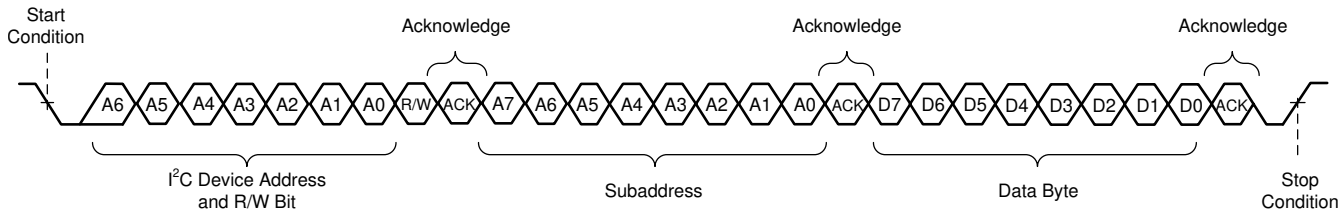


Figure 7-10. Random Write Transfer

7.5.2.2 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in . After receiving each data byte, the device responds with an acknowledge bit and the I2C subaddress is automatically incremented by one.

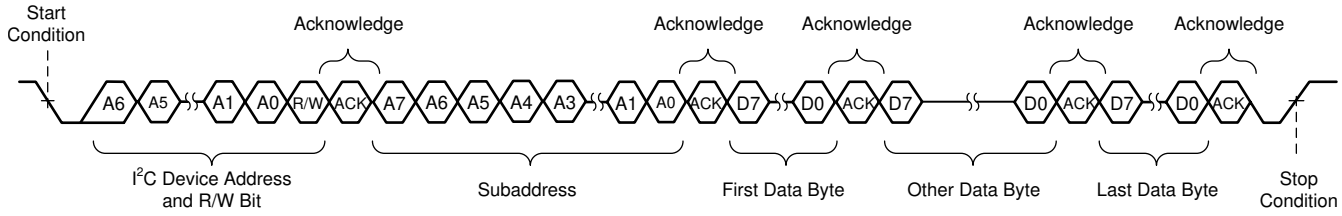


Figure 7-11. Sequential Write Transfer

7.5.2.3 Random Read

As shown in , a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit is a 0. After receiving the address and the read/write bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the address and the read/write bit again. This time the read/write bit is a 1, indicating a read transfer. After receiving the address and the read/write bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

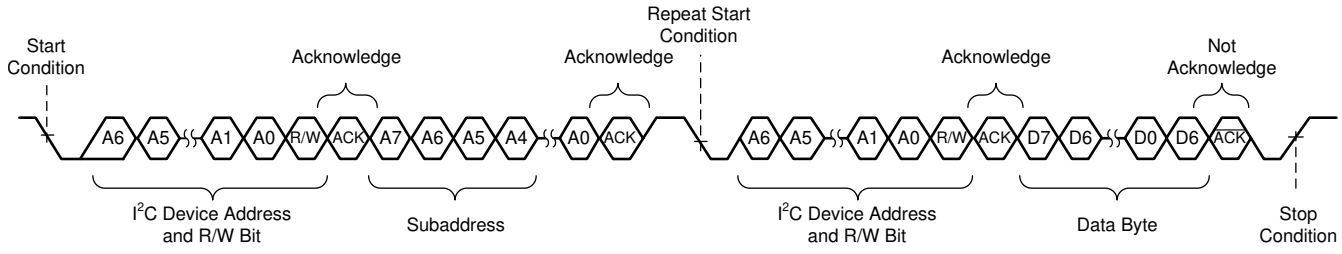


Figure 7-12. Random Read Transfer

7.5.2.4 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in . Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I2C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the transfer.

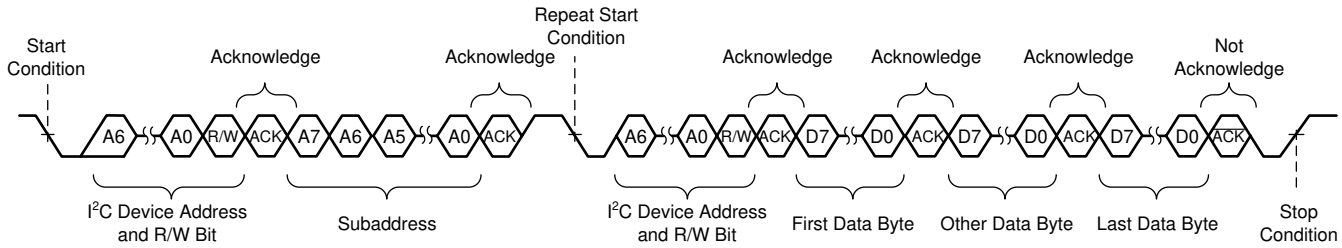


Figure 7-13. Sequential Read Transfer

7.6 Register Maps

7.6.1 Registers

Table 7-10 lists all registers, their functionality and default values. All register offset addresses not listed in Table 7-10 should be considered as reserved locations and the register contents should not be modified.

Table 7-10. Register Map

Offset	Acronym	Register Name	Section
0x1	Mode Control	Mode Control Register	Section 7.6.1.1
0x2	Misc Control 1	Miscellaneous Control Register 1	Section 7.6.1.2
0x3	Misc Control 2	Miscellaneous Control Register 2	Section 7.6.1.3
0x4	Channel State Control	Channel State Control Register	Section 7.6.1.4
0x5	DC LDG Ctrl 1	DC Load Diagnostics Control Register 1	Section 7.6.1.5
0x6	DC LDG Ctrl 2	DC Load Diagnostic Control Register 2	Section 7.6.1.6
0x7	DC LDG Ctrl 3	DC Load Diagnostic Control Register 3	Section 7.6.1.7
0x8	DC LDG Ctrl 4	DC Load Diagnostic Control Register 4	Section 7.6.1.8
0x9	DC LDG Ctrl 5	DC Load Diagnostic Control Register 5	Section 7.6.1.9
0xA	DC LDG Rprt CH12	DC Load Diagnostic Report CH1, CH2 Register	Section 7.6.1.10
0xB	DC LDG Rprt CH34	DC Load Diagnostic Report CH3, CH4 Register	Section 7.6.1.11
0xC	DC LDG Rprt LO	DC Load Diagnostic Report Lineout Loads Register	Section 7.6.1.12
0xD	Channel State Rprt CH12	Channel State Report CH1, CH2 Register	Section 7.6.1.13
0xE	Channel State Rprt CH34	Channel State Report CH3, CH4 Register	Section 7.6.1.14
0xF	Ch OC DC Fault Mem	Channel Over Current and DC Detection Fault Memory Register	Section 7.6.1.15
0x10	Power_Fault_Mem	Power Fault Memory Register	Section 7.6.1.16
0x11	Power Fault Status	Power Fault Status Register	Section 7.6.1.17
0x12	OTSD CS Fault Mem	Temperature (OTSD) and Clock Sync Fault Memory Register	Section 7.6.1.18
0x13	OTSD CS Fault Status	Temperature (OTSD) and Clock Sync Fault Status Register	Section 7.6.1.19
0x14	Ch Current Fault Mem	Channel Load Current Fault Memory Register	Section 7.6.1.20
0x15	Ch Current Warn Mem	Channel Load Current Warning Memory Register	Section 7.6.1.21
0x16	OTW TGFB Warn Mem	Temperature (OTW) and Thermal Gain Foldback Warning Memory Register	Section 7.6.1.22
0x17	OTW TGFB Warn Status	Temperature (OTW) and Thermal Gain Foldback Warning Status Register	Section 7.6.1.23
0x18	Ch ClipDet Warn Mem	Channel Clip Detect Warning Memory Register	Section 7.6.1.24
0x19	Ch ClipDet Warn Status	Channel Clip Detect Warning Status Register	Section 7.6.1.25
0x1C	TGFB Status	Thermal Gain Foldback Status Register	Section 7.6.1.26
0x1D	Fault Sig Conf 1	Fault Signal Configuration Register 1	Section 7.6.1.27
0x1E	Fault Sig Conf 2	Fault Signal Configuration Register 2	Section 7.6.1.28
0x1F	Warn Sig Conf 1	Warning Signal Configuration Register 1	Section 7.6.1.29
0x20	Warn Sig Conf 2	Warning Signal Configuration Register 2	Section 7.6.1.30
0x21	Clip Det Sig Conf	Clip Detect Signal Configuration Register	Section 7.6.1.31
0x22	Fault Pin Conf	Fault Pin Configuration Register	Section 7.6.1.32
0x23	GPIO Conf	GPIO Pin Configuration Register	Section 7.6.1.33
0x24	AC LDG Ctrl 1	AC Load Diagnostic Control Register 1	Section 7.6.1.34
0x25	AC LDG Ctrl 2	AC Load Diagnostic Control Register 2	Section 7.6.1.35
0x26	TWEETER DET THRESH	Tweeter Detection Threshold	Section 7.6.1.36

Table 7-10. Register Map (continued)

Offset	Acronym	Register Name	Section
0x27	AC LDG Rprt CH1 R	AC Load Diagnostic Report R CH1	Section 7.6.1.37
0x28	AC LDG Rprt CH1 I	AC Load Diagnostic Report I CH1	Section 7.6.1.38
0x29	AC LDG Rprt CH2 R	AC Load Diagnostic Report R CH2	Section 7.6.1.39
0x2A	AC LDG Rprt CH2 I	AC Load Diagnostic Report I CH2	Section 7.6.1.40
0x2B	AC LDG Rprt CH3 R	AC Load Diagnostic Report R CH3	Section 7.6.1.41
0x2C	AC LDG Rprt CH3 I	AC Load Diagnostic Report I CH3	Section 7.6.1.42
0x2D	AC LDG Rprt CH4 R	AC Load Diagnostic Report R CH4	Section 7.6.1.43
0x2E	AC LDG Rprt CH4 I	AC Load Diagnostic Report I CH	Section 7.6.1.44
0x2F	TWEETER DET	Tweeter Detection	Section 7.6.1.45
0x30	Misc Control 3	Miscellaneous Control Register 3	Section 7.6.1.46
0x32	REVID	Revision ID	Section 7.6.1.47
0x33	TGFB Ctrl	Thermal Gain Foldback Control Register	Section 7.6.1.48
0x34	AC LDG FREQ Ctrl	AC Load Diagnostic Frequency Control Register	Section 7.6.1.49
0x35	SYNC Ctrl	Sync Pin Control Register	Section 7.6.1.50
0x36	Misc Control 4	Miscellaneous Control Register 4	Section 7.6.1.51
0x37	SS Control 1	Spread Spectrum Control Register 1	Section 7.6.1.52
0x38	SS Control 2	Spread Spectrum Control Register 2	Section 7.6.1.53
0x39	PWM Phase Ctrl 1	PWM Phase Control Register 1	Section 7.6.1.54
0x3A	PWM Phase Ctrl 2	PWM Phase Control Register 2	Section 7.6.1.55

7.6.1.1 Mode Control Register (Offset = 0x1) [reset = 0x00]

Return to the Table 7-10.

Figure 7-14. Mode Control Register

7	6	5	4	3	2	1	0
RESET	PWM MODE	PBTL_34	PBTL_12	CH1 LO MODE	CH2 LO MODE	CH3 LO MODE	CH4 LO MODE
W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-11. Mode Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	W	0b	**0: Normal Operation** 1: Soft reset, will auto clear
6	PWM MODE	R/W	0b	**0: BD Mode** 1: 1SPW Mode
5	PBTL_34	R/W	0b	**0: BTL mode** 1: PBTL mode of Channel 3 and Channel 4
4	PBTL_12	R/W	0b	**0: BTL mode** 1: PBTL mode of Channel 1 and Channel 2
3	CH1 LO MODE	R/W	0b	**0: Channel 1 is in normal / speaker mode** 1: Channel 1 is in line output mode
2	CH2 LO MODE	R/W	0b	**0: Channel 2 is in normal / speaker mode** 1: Channel 1 is in line output mode
1	CH3 LO MODE	R/W	0b	**0: Channel 3 is in normal / speaker mode** 1: Channel 1 is in line output mode
0	CH4 LO MODE	R/W	0b	**0: Channel 4 is in normal / speaker mode** 1: Channel 1 is in line output mode

7.6.1.2 Misc Control 1 Register (Offset = 0x2) [reset = 0x10]

Return to the Table 7-10.

Figure 7-15. Misc Control 1 Register

7	6	5	4	3	2	1	0
RESERVED	PI Control	OTW CONTROL		OC CONTROL		RESERVED	
R/W-0b	R/W-0b	R/W-1b		R/W-0b		R/W-0b	

Table 7-12. Misc Control 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	PI Control	R/W	0b	**0: Disable Pulse Injection Mode** 1: Enable Pulse Injection Mode
5-4	OTW CONTROL	R/W	1b	00: Global over temperature warning set to 140 °C **01: Global over temperature warning set to 130 °C** 10: Global over temperature warning set to 120 °C 11:Global over temperature warning set to 110 °C
3-2	OC CONTROL	R/W	0b	See electrical characteristics table for details **00: OC Level 1** 01: OC Level 2 10: OC Level 3 11: OC Level 4
1-0	RESERVED	R/W	0b	

7.6.1.3 Misc Control 2 Register (Offset = 0x3) [reset = 0xFF]

Return to the Table 7-10.

Figure 7-16. Misc Control 2 Register

7	6	5	4	3	2	1	0
CH1 GAIN		CH2 GAIN		CH3 GAIN		CH4 GAIN	
R/W-11b		R/W-11b		R/W-11b		R/W-11b	

Table 7-13. Misc Control 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH1 GAIN	R/W	11b	00: 10dB 01: 16dB 10: 22dB **11: 28dB**
5-4	CH2 GAIN	R/W	11b	00: 10dB 01: 16dB 10: 22dB **11: 28dB**
3-2	CH3 GAIN	R/W	11b	00: 10dB 01: 16dB 10: 22dB **11: 28dB**
1-0	CH4 GAIN	R/W	11b	00: 10dB 01: 16dB 10: 22dB **11: 28dB**

7.6.1.4 Channel State Control Register (Offset = 0x4) [reset = 0x55]

Return to the Table 7-10.

Figure 7-17. Channel State Control Register

7	6	5	4	3	2	1	0
CH1 STATE CONTROL		CH2 STATE CONTROL		CH3 STATE CONTROL		CH4 STATE CONTROL	
R/W-1b		R/W-1b		R/W-1b		R/W-1b	

Table 7-14. Channel State Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH1 STATE CONTROL	R/W	1b	00: Set channel state to PLAY **01: Set channel state to HI-Z** 10: Set channel state to MUTE 11: Set channel to start DC load diagnostic
5-4	CH2 STATE CONTROL	R/W	1b	00: Set channel state to PLAY **01: Set channel state to HI-Z** 10: Set channel state to MUTE 11: Set channel to start DC load diagnostic
3-2	CH3 STATE CONTROL	R/W	1b	00: Set channel state to PLAY **01: Set channel state to HI-Z** 10: Set channel state to MUTE 11: Set channel to start DC load diagnostic
1-0	CH4 STATE CONTROL	R/W	1b	00: Set channel state to PLAY **01: Set channel state to HI-Z** 10: Set channel state to MUTE 11: Set channel to start DC load diagnostic

7.6.1.5 DC LDG Ctrl 1 Register (Offset = 0x5) [reset = 0x00]

Return to the Table 7-10.

Figure 7-18. DC LDG Ctrl 1 Register

7	6	5	4	3	2	1	0
LDG ABORT	LDG BUFFER WAIT TIME		RESERVED		LDG WAIT BYPASS	LDG SLOL DISABLE	LDG BYPASS
R/W-0b	R/W-0b		R/W-0b		R/W-0b	R/W-0b	R/W-0b

Table 7-15. DC LDG Ctrl 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDG ABORT	R/W	0b	**0: Normal operation** 1: Abort DC load diagnostic
6-5	LDG BUFFER WAIT TIME	R/W	0b	**00: Buffer wait time 1ms** 01: Buffer wait time 2ms 10: Buffer wait time 5ms 11: Buffer wait time 10ms
4-3	RESERVED	R/W	0b	
2	LDG WAIT BYPASS	R/W	0b	**0: Enable the waiting loop at the end of shorted / open load detection** 1: Bypass the waiting loop at the end of shorted / open load detection
1	LDG SLOL DISABLE	R/W	0b	**0: Shorted load and open load detection are enabled** 1: Shorted load, open load and line out out detection are disabled
0	LDG BYPASS	R/W	0b	**0: Automatic DC diagnostic when leaving Hi-Z mode and after channel fault** 1: DC diagnostic will not run automatically

7.6.1.6 DC LDG Ctrl 2 Register (Offset = 0x6) [reset = 0x00]

Return to the Table 7-10.

Figure 7-19. DC LDG Ctrl 2 Register

7	6	5	4	3	2	1	0
RESERVED	LDG S2PS2G AVG TIME	LDG SLOL AVG TIME		LDG LO ENABLE CH1	LDG LO ENABLE CH2	LDG LO ENABLE CH3	LDG LO ENABLE CH4
R/W-0b	R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-16. DC LDG Ctrl 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	LDG S2PS2G AVG TIME	R/W	0b	Averaging time for Short-to-Power and Short-to-Ground measurement **0: 0.2 ms** 1: 0.7 ms
5-4	LDG SLOL AVG TIME	R/W	0b	Averaging time for shorted load and open load measurements: **00: Same averaging time as selected for Short-to-Power and Short-to-Ground in bit 6 of this register** 01: 10.7 ms 10: 21.3 ms 11: 42.7 ms
3	LDG LO ENABLE CH1	R/W	0b	**0: Disable DC Load Diagnostics to check for line-out load on CH1** 1: Enable DC Load Diagnostics to check for line-out load on CH1
2	LDG LO ENABLE CH2	R/W	0b	**0: Disable DC Load Diagnostics to check for line-out load on CH2** 1: Enable DC Load Diagnostics to check for line-out load on CH2
1	LDG LO ENABLE CH3	R/W	0b	**0: Disable DC Load Diagnostics to check for line-out load on CH3** 1: Enable DC Load Diagnostics to check for line-out load on CH3
0	LDG LO ENABLE CH4	R/W	0b	**0: Disable DC Load Diagnostics to check for line-out load on CH4** 1: Enable DC Load Diagnostics to check for line-out load on CH4

7.6.1.7 DC LDG Ctrl 3 Register (Offset = 0x7) [reset = 0x00]

Return to the Table 7-10.

Figure 7-20. DC LDG Ctrl 3 Register

7	6	5	4	3	2	1	0
LDG RAMP 2		LDG SETTLING 2		LDG RAMP 1		LDG SETTLING 1	
R/W-0b		R/W-0b		R/W-0b		R/W-0b	

Table 7-17. DC LDG Ctrl 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LDG RAMP 2	R/W	0b	Ramp time, shorted load and open load diagnostics **00: 15 ms** 01: 30 ms 10: 10 ms 11: 20 ms
5-4	LDG SETTLING 2	R/W	0b	Settling time, shorted load and open load diagnostics **00: 10 ms** 01: 5 ms 10: 20 ms 11: 15 ms
3-2	LDG RAMP 1	R/W	0b	Ramp time, short-to-power and short-to-ground diagnostics **00: 5 ms** 01: 2.5 ms 10: 10 ms 11: 15 ms
1-0	LDG SETTLING 1	R/W	0b	Settling time, short-to-power and short-to-ground diagnostics **00: 10ms** 01: 5 ms 10: 20 ms 11: 30 ms

7.6.1.8 DC LDG Ctrl 4 Register (Offset = 0x8) [reset = 0x11]

Return to the Table 7-10.

Figure 7-21. DC LDG Ctrl 4 Register

7	6	5	4	3	2	1	0
CH1 DC LDG SL				CH2 DC LDG SL			
R/W-1b				R/W-1b			

Table 7-18. DC LDG Ctrl 4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH1 DC LDG SL	R/W	1b	Channel 1 DC load diagnostic shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω
3-0	CH2 DC LDG SL	R/W	1b	Channel 2 DC load diagnostic shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

7.6.1.9 DC LDG Ctrl 5 Register (Offset = 0x9) [reset = 0x11]

Return to the Table 7-10.

Figure 7-22. DC LDG Ctrl 5 Register

7	6	5	4	3	2	1	0
CH3 DC LDG SL				CH4 DC LDG SL			
R/W-1b				R/W-1b			

Table 7-19. DC LDG Ctrl 5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CH3 DC LDG SL	R/W	1b	Channel 3 DC load diagnostic shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω
3-0	CH4 DC LDG SL	R/W	1b	Channel 4 DC load diagnostic shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

7.6.1.10 DC LDG Rprt CH12 Register (Offset = 0xA) [reset = 0x00]

Return to the Table 7-10.

Figure 7-23. DC LDG Rprt CH12 Register

7	6	5	4	3	2	1	0
CH1 S2G	CH1 S2P	CH1 OL	CH1 SL	CH2 S2G	CH2 S2P	CH2 OL	CH2 SL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-20. DC LDG Rprt CH12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 S2G	R	0b	**0: No short-to-GND detected on channel 1** 1: Short-to-GND detected on channel 1
6	CH1 S2P	R	0b	**0: No short-to-power detected on channel 1** 1: Short-to-power detected on channel 1
5	CH1 OL	R	0b	**0: No open load detected on channel 1** 1: Open load detected on channel 1
4	CH1 SL	R	0b	**0: No shorted load detected on channel 1** 1: Shorted load detected on channel 1
3	CH2 S2G	R	0b	**0: No short-to-GND detected on channel 2** 1: Short-to-GND detected on channel 2
2	CH2 S2P	R	0b	**0: No short-to-power detected on channel 2** 1: Short-to-power detected on channel 2
1	CH2 OL	R	0b	**0: No open load detected on channel 2** 1: Open load detected on channel 2
0	CH2 SL	R	0b	**0: No shorted load detected on channel 2** 1: Shorted load detected on channel 2

7.6.1.11 DC LDG Rprt CH34 Register (Offset = 0xB) [reset = 0x00]

Return to the Table 7-10.

Figure 7-24. DC LDG Rprt CH34 Register

7	6	5	4	3	2	1	0
CH3 S2G	CH3 S2P	CH3 OL	CH3 SL	CH4 S2G	CH4 S2P	CH4 OL	CH4 SL
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-21. DC LDG Rprt CH34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH3 S2G	R	0b	**0: No short-to-GND detected on channel 3** 1: Short-to-GND detected on channel 3
6	CH3 S2P	R	0b	**0: No short-to-power detected on channel 3** 1: Short-to-power detected on channel 3
5	CH3 OL	R	0b	**0: No open load detected on channel 3** 1: Open load detected on channel 3
4	CH3 SL	R	0b	**0: No shorted load detected on channel 3** 1: Shorted load detected on channel 3
3	CH4 S2G	R	0b	**0: No short-to-GND detected on channel 4** 1: Short-to-GND detected on channel 4
2	CH4 S2P	R	0b	**0: No short-to-power detected on channel 4** 1: Short-to-power detected on channel 4
1	CH4 OL	R	0b	**0: No open load detected on channel 4** 1: Open load detected on channel 4
0	CH4 SL	R	0b	**0: No shorted load detected on channel 4** 1: Shorted load detected on channel 4

7.6.1.12 DC LDG Rprt LO Register (Offset = 0xC) [reset = 0x00]

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Figure 7-25. DC LDG Rprt LO Register

7	6	5	4	3	2	1	0
RESERVED				CH1 LO LDG	CH2 LO LDG	CH3 LO LDG	CH4 LO LDG
R-0b				R-0b	R-0b	R-0b	R-0b

Table 7-22. DC LDG Rprt LO Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	
3	CH1 LO LDG	R	0b	**0: No line output detected on channel 1** 1: Line output detected on channel 1
2	CH2 LO LDG	R	0b	**0: No line output detected on channel 2** 1: Line output detected on channel 2
1	CH3 LO LDG	R	0b	**0: No line output detected on channel 3** 1: Line output detected on channel 3
0	CH4 LO LDG	R	0b	**0: No line output detected on channel 4** 1: Line output detected on channel 4

7.6.1.13 Channel State Rprt CH12 Register (Offset = 0xD) [reset = 0x24]

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Figure 7-26. Channel State Rprt CH12 Register

7	6	5	4	3	2	1	0
CH1 STATE REPORT			CH2 STATE REPORT			CH1 LDG STATE REPORT	CH2 LDG STATE REPORT
R-1b			R-1b			R-0b	R-0b

Table 7-23. Channel State Rprt CH12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	CH1 STATE REPORT	R	1b	Channel 1 is in state: 101: PSD (protective shutdown) 100: PSD_AR (protective shutdown, will auto recover) 011: DIAG 010: MUTE **001: HI-Z** 000: PLAY
4-2	CH2 STATE REPORT	R	1b	Channel 2 is in state: 101: PSD (protective shutdown) 100: PSD_AR (protective shutdown, will auto recover) 011: DIAG 010: MUTE **001: HI-Z** 000: PLAY
1	CH1 LDG STATE REPORT	R	0b	**0: DC Load Diagnostic did not complete without faults on channel 1** 1: DC Load Diagnostic completed without faults on channel 1
0	CH2 LDG STATE REPORT	R	0b	**0: DC Load Diagnostic did not complete without faults on channel 2** 1: DC Load Diagnostic completed without faults on channel 2

7.6.1.14 Channel State Rprt CH34 Register (Offset = 0xE) [reset = 0x24]

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Figure 7-27. Channel State Rprt CH34 Register

7	6	5	4	3	2	1	0
CH3 STATE REPORT			CH4 STATE REPORT			CH3 LDG STATE REPORT	CH4 LDG STATE REPORT
R-1b			R-1b			R-0b	R-0b

Table 7-24. Channel State Rprt CH34 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	CH3 STATE REPORT	R	1b	Channel 3 is in state: 101: PSD (protective shutdown) 100: PSD_AR (protective shutdown, will auto recover) 011: DIAG 010: MUTE **001: HI-Z** 000: PLAY
4-2	CH4 STATE REPORT	R	1b	Channel 4 is in state: 101: PSD (protective shutdown) 100: PSD_AR (protective shutdown, will auto recover) 011: DIAG 010: MUTE **001: HI-Z** 000: PLAY
1	CH3 LDG STATE REPORT	R	0b	**0: DC Load Diagnostic did not complete without faults on channel 3** 1: DC Load Diagnostic completed without faults on channel 3
0	CH4 LDG STATE REPORT	R	0b	**0: DC Load Diagnostic did not complete without faults on channel 4** 1: DC Load Diagnostic completed without faults on channel 4

7.6.1.15 Ch OC DC Fault Mem Register (Offset = 0xF) [reset = 0x00]

Register clears to 0x0 upon reading.
For channel restart, DC and/or OC fault needs to be cleared by writing to register 0x30.

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Figure 7-28. Ch OC DC Fault Mem Register

7	6	5	4	3	2	1	0
CH1 OC FAULT STORED	CH2 OC FAULT STORED	CH3 OC FAULT STORED	CH4 OC FAULT STORED	CH1 DC FAULT STORED	CH2 DC FAULT STORED	CH3 DC FAULT STORED	CH4 DC FAULT STORED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-25. Ch OC DC Fault Mem Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 OC FAULT STORED	R	0b	**0: No channel 1 over current fault event stored** 1: Channel 1 over current fault event stored
6	CH2 OC FAULT STORED	R	0b	**0: No channel 2 over current fault event stored** 1: Channel 2 over current fault event stored
5	CH3 OC FAULT STORED	R	0b	**0: No channel 3 over current fault event stored** 1: Channel 3 over current fault event stored
4	CH4 OC FAULT STORED	R	0b	**0: No channel 4 over current fault event stored** 1: Channel 4 over current fault event stored
3	CH1 DC FAULT STORED	R	0b	**0: No channel 1 DC fault event stored** 1: Channel 1 DC fault event stored
2	CH2 DC FAULT STORED	R	0b	**0: No channel 2 DC fault event stored** 1: Channel 2 DC fault event stored
1	CH3 DC FAULT STORED	R	0b	**0: No channel 3 DC fault event stored** 1: Channel 3 DC fault event stored
0	CH4 DC FAULT STORED	R	0b	**0: No channel 4 DC fault event stored** 1: Channel 4 DC fault event stored

7.6.1.16 Power_Fault_Mem Register (Offset = 0x10) [reset = 0x00]

Register clears to 0x0 upon reading.

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Figure 7-29. Power_Fault_Mem Register

7	6	5	4	3	2	1	0
RESERVED		GVDD FAULT STORED	DVDD POR STORED	PVDD OV STORED	VBAT OV STORED	PVDD UV STORED	VBAT UV STORED
R-0b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-26. Power_Fault_Mem Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	
5	GVDD FAULT STORED	R	0b	**0: No GVDD regulator fault event stored** 1: GVDD regulator fault event stored
4	DVDD POR STORED	R	0b	0: No DVDD power on reset event stored **1: DVDD power on reset event stored**
3	PVDD OV STORED	R	0b	**0: No PVDD over voltage event stored** 1: PVDD over voltage event stored
2	VBAT OV STORED	R	0b	**0: No VBAT over voltage event stored** 1: VBAT over voltage event stored
1	PVDD UV STORED	R	0b	**0: No PVDD under voltage event stored** 1: PVDD under voltage event detected and stored
0	VBAT UV STORED	R	0b	**0: No VBAT under voltage event stored** 1: VBAT under voltage event stored

7.6.1.17 Power Fault Status Register (Offset = 0x11) [reset = 0x00]

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Figure 7-30. Power Fault Status Register

7	6	5	4	3	2	1	0
GLOBAL WARNING	GLOBAL FAULT	GVDD FAULT	RESERVED	PVDD OV	VBAT OV	PVDD UV	VBAT UV
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-27. Power Fault Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL WARNING	R	0b	**0: No warning** 1: If any warning active in device, regardless of warning signal configuration
6	GLOBAL FAULT	R	0b	**0: No fault** 1: If any fault active in device, regardless of fault signal configuration
5	GVDD FAULT	R	0b	**0: No GVDD regulator fault detected** 1: GVDD regulator fault detected
4	RESERVED	R	0b	
3	PVDD OV	R	0b	**0: PVDD supply voltage is not above OV threshold** 1: PVDD supply voltage is above OV threshold
2	VBAT OV	R	0b	**0: VBAT supply voltage is not above OV threshold** 1: VBAT supply voltage is above OV threshold
1	PVDD UV	R	0b	**0: PVDD supply voltage is not below UV threshold** 1:PVDD supply voltage is below UV threshold
0	VBAT UV	R	0b	**0: VBAT supply voltage is not below UV threshold** 1: VBAT supply voltage is below UV threshold

7.6.1.18 OTSD CS Fault Mem Register (Offset = 0x12) [reset = 0x00]

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Figure 7-31. OTSD CS Fault Mem Register

7	6	5	4	3	2	1	0
RESERVED		INVALID CLOCK STORED	OTSD STORED	CH1 OTSD STORED	CH2 OTSD STORED	CH3 OTSD STORED	CH4 OTSD STORED
R-0b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-28. OTSD CS Fault Mem Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	
5	INVALID CLOCK STORED	R	0b	Only applies if device is configured in clock slave mode: **0: No clock synchronization fault event stored** 1:Clock synchronization fault event stored
4	OTSD STORED	R	0b	**0: No global over temperature shutdown event stored** 1:Global over temperature shutdown event stored
3	CH1 OTSD STORED	R	0b	**0: No channel 1 over temperature shutdown event stored** 1: Channel 1 over temperature shutdown event stored
2	CH2 OTSD STORED	R	0b	**0: No channel 2 over temperature shutdown event stored** 1: Channel 2 over temperature shutdown event stored
1	CH3 OTSD STORED	R	0b	**0: No channel 3 over temperature shutdown event stored** 1: Channel 3 over temperature shutdown event stored
0	CH4 OTSD STORED	R	0b	**0: No channel 4 over temperature shutdown event stored** 1: Channel 4 over temperature shutdown event stored

7.6.1.19 OTSD CS Fault Status Register (Offset = 0x13) [reset = 0x00]

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Figure 7-32. OTSD CS Fault Status Register

7	6	5	4	3	2	1	0
WARNING SIGNAL	FAULT SIGNAL	INVALID CLOCK	OTSD	CH1 OTSD	CH2 OTSD	CH3 OTSD	CH4 OTSD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-29. OTSD CS Fault Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	WARNING SIGNAL	R	0b	**0: If internal warning signal is not active** 1: If internal warning signal is active (configured by warning signal configuration registers)
6	FAULT SIGNAL	R	0b	**0: If internal fault signal is not active** 1: If internal fault signal is active (configured by fault signal configuration registers)
5	INVALID CLOCK	R	0b	Only applies if device is configured in clock slave mode: **0: No Synchronization clock error detected** 1: Synchronization clock error detected
4	OTSD	R	0b	**0: Global die temperature is not above OTSD threshold** 1: Global die temperature is above OTSD threshold
3	CH1 OTSD	R	0b	**0: Channel 1 temperature is not above OTSD threshold** 1: Channel 1 temperature is above OTSD threshold
2	CH2 OTSD	R	0b	**0: Channel 2 temperature is not above OTSD threshold** 1: Channel 2 temperature is above OTSD threshold
1	CH3 OTSD	R	0b	**0: Channel 3 temperature is not above OTSD threshold** 1: Channel 3 temperature is above OTSD threshold
0	CH4 OTSD	R	0b	**0: Channel 4 temperature is not above OTSD threshold** 1: Channel 4 temperature is above OTSD threshold

7.6.1.20 Ch Current Fault Mem Register (Offset = 0x14) [reset = 0x00]

Register clears to 0x0 upon reading.
To restart the channel, the load current faults need to be cleared by writing to Register 0x30.

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Figure 7-33. Ch Current Fault Mem Register

7	6	5	4	3	2	1	0
RESERVED				CH1 I-LIMIT FAULT STORED	CH2 I-LIMIT FAULT STORED	CH3 I-LIMIT FAULT STORED	CH4 I-LIMIT FAULT STORED
R-0b				R-0b	R-0b	R-0b	R-0b

Table 7-30. Ch Current Fault Mem Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	
3	CH1 I-LIMIT FAULT STORED	R	0b	**0: No channel 1 load current fault event stored** 1: Channel 1 load current fault event stored
2	CH2 I-LIMIT FAULT STORED	R	0b	**0: No channel 2 load current fault event stored** 1: Channel 2 load current fault event stored
1	CH3 I-LIMIT FAULT STORED	R	0b	**0: No Channel 3 load current fault event stored** 1: Channel 3 load current fault event stored
0	CH4 I-LIMIT FAULT STORED	R	0b	**0: No channel 4 load current fault event stored** 1: Channel 4 load current fault event stored

7.6.1.21 Ch Current Warn Mem Register (Offset = 0x15) [reset = 0x00]

Register clears to 0x0 upon reading.

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Figure 7-34. Ch Current Warn Mem Register

7	6	5	4	3	2	1	0
RESERVED				CH1 I-LIMIT WARN STORED	CH2 I-LIMIT WARN STORED	CH3 I-LIMIT WARN STORED	CH4 I-LIMIT WARN STORED
R-0b				R-0b	R-0b	R-0b	R-0b

Table 7-31. Ch Current Warn Mem Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	
3	CH1 I-LIMIT WARN STORED	R	0b	**0: No channel 1 load current warning event stored** 1: Channel 1 load current warning event stored
2	CH2 I-LIMIT WARN STORED	R	0b	**0: No channel 2 load current warning event stored** 1: Channel 2 load current warning event stored
1	CH3 I-LIMIT WARN STORED	R	0b	**0: No channel 3 load current warning event stored** 1: Channel 3 load current warning event stored
0	CH4 I-LIMIT WARN STORED	R	0b	**0: No channel 4 load current warning event stored** 1: Channel 4 load current warning event stored

7.6.1.22 OTW TGFB Warn Mem Register (Offset = 0x16) [reset = 0x00]

Register clears to 0x0 upon reading.

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Figure 7-35. OTW TGFB Warn Mem Register

7	6	5	4	3	2	1	0
RESERVED		TGFBW STORED	OTW STORED	CH1 OTW STORED	CH2 OTW STORED	CH3 OTW STORED	CH4 OTW STORED
R-0b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-32. OTW TGFB Warn Mem Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	
5	TGFBW STORED	R	0b	**0: No thermal gain fold back activation event stored** 1: Thermal gain fold back activation event stored
4	OTW STORED	R	0b	**0: No global over temperature warning event stored** 1:Global over temperature warning event stored
3	CH1 OTW STORED	R	0b	**0: No channel 1 over temperature warning event stored** 1: Channel 1 over temperature warning event stored
2	CH2 OTW STORED	R	0b	**0: No channel 2 over temperature warning event stored** 1: Channel 2 over temperature warning event stored
1	CH3 OTW STORED	R	0b	**0: No channel 3 over temperature warning event stored** 1: Channel 3 over temperature warning event stored
0	CH4 OTW STORED	R	0b	**0: No channel 4 over temperature warning event stored** 1: Channel 4 over temperature warning event stored

7.6.1.23 OTW TGFB Warn Status Register (Offset = 0x17) [reset = 0x00]

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Figure 7-36. OTW TGFB Warn Status Register

7	6	5	4	3	2	1	0
RESERVED		TGFBW	OTW	CH1 OTW	CH2 OTW	CH3 OTW	CH4 OTW
R-0b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 7-33. OTW TGFB Warn Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0b	
5	TGFBW	R	0b	**0: Thermal gain fold back is not activated** 1: Thermal gain fold back is activated
4	OTW	R	0b	**0: Global die temperature is not above OTW threshold** 1: Global die temperature is above OTW threshold
3	CH1 OTW	R	0b	**0: Channel 1 temperature is not above OTW threshold** 1: Channel 1 temperature is above OTW threshold
2	CH2 OTW	R	0b	**0: Channel 2 temperature is not above OTW threshold** 1: Channel 2 temperature is above OTW threshold
1	CH3 OTW	R	0b	**0: Channel 3 temperature is not above OTW threshold** 1: Channel 3 temperature is above OTW threshold
0	CH4 OTW	R	0b	**0: Channel 4 temperature is not above OTW threshold** 1: Channel 4 temperature is above OTW threshold

7.6.1.24 Ch ClipDet Warn Mem Register (Offset = 0x18) [reset = 0x00]

Register clears to 0x0 upon reading.

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Figure 7-37. Ch ClipDet Warn Mem Register

7	6	5	4	3	2	1	0
RESERVED				CH1 CLIP STORED	CH2 CLIP STORED	CH3 CLIP STORED	CH4 CLIP STORED
R-0b				R-0b	R-0b	R-0b	R-0b

Table 7-34. Ch ClipDet Warn Mem Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	
3	CH1 CLIP STORED	R	0b	**0: No channel 1 clipping event stored** 1: Channel 1 clipping event stored
2	CH2 CLIP STORED	R	0b	**0: No channel 2 clipping event stored** 1: Channel 2 clipping event stored
1	CH3 CLIP STORED	R	0b	**0: No channel 3 clipping event stored** 1: Channel 3 clipping event stored
0	CH4 CLIP STORED	R	0b	**0: No channel 4 clipping event stored** 1: Channel 4 clipping event stored

7.6.1.25 Ch ClipDet Warn Status Register (Offset = 0x19) [reset = 0x00]

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Figure 7-38. Ch ClipDet Warn Status Register

7	6	5	4	3	2	1	0
RESERVED				CH1 CLIP	CH2 CLIP	CH3 CLIP	CH4 CLIP
R-0b				R-0b	R-0b	R-0b	R-0b

Table 7-35. Ch ClipDet Warn Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	
3	CH1 CLIP	R	0b	**0: Channel 1 clipping is not present or not above clip detect threshold** 1: Channel 1 clipping is above clip detect threshold
2	CH2 CLIP	R	0b	**0: Channel 2 clipping is not present or not above clip detect threshold** 1: Channel 2 clipping is above clip detect threshold
1	CH3 CLIP	R	0b	**0: Channel 3 clipping is not present or not above clip detect threshold** 1: Channel 3 clipping is above clip detect threshold
0	CH4 CLIP	R	0b	**0: Channel 4 clipping is not present or not above clip detect threshold** 1: Channel 4 clipping is above clip detect threshold

7.6.1.26 TGFB Status Register (Offset = 0x1C) [reset = 0x00]

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Figure 7-39. TGFB Status Register

7	6	5	4	3	2	1	0
RESERVED			TGFB GAIN				
R-0b			R-0b				

Table 7-36. TGFB Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	
4-0	TGFB GAIN	R	0b	Gain set by thermal gain foldback control in response to die temperature is: **00000: 0 dB** 00001: -0.5 dB 00010: -1 dB .... 10111: - 11.5 dB 11000: - 12 dB

7.6.1.27 Fault Sig Conf 1 Register (Offset = 0x1D) [reset = 0x17]

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Figure 7-40. Fault Sig Conf 1 Register

7	6	5	4	3	2	1	0
RESERVED	FAULT ON PROTECTIVE SHUTDOWN	FAULT ON INVALID CLOCK STORED	FAULT ON OTSD STORED	FAULT ON POWER FAULT STORED	FAULT ON DC STORED	FAULT ON OC STORED	FAULT ON ILIMIT STORED
R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-1b	R/W-1b

Table 7-37. Fault Sig Conf 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	FAULT ON PROTECTIVE SHUTDOWN	R/W	0b	**0: Fault signal is not activated by any CH[1..4] STATE REPORT = '101'** 1: If any CH[1..4] STATE REPORT = '101', fault signal is active
5	FAULT ON INVALID CLOCK STORED	R/W	0b	**0: Fault signal is not activated by INVALID CLOCK STORED bit** 1: If INVALID CLOCK STORED bit is set, fault signal is active
4	FAULT ON OTSD STORED	R/W	1b	0: Fault signal is not activated by any CH[1..4] OTSD STORED bit or OTSD STORED bit **1: If any CH[1..4] OTSD STORED bit or OTSD STORED bit is set, fault signal is active**
3	FAULT ON POWER FAULT STORED	R/W	0b	**0: Fault Signal is not activated by any stored bit in "Power Fault Memory Register"** 1: If VBAT UV STORED bit, VBAT OV STORED bit, PVDD UV STORED bit, PVDD OV STORED bit, DVDD POR STORED bit, or GVDD FAULT STORED bit is set, fault signal is active.
2	FAULT ON DC STORED	R/W	1b	0: Fault signal is not activated by any CH[1..4] DC FAULT STORED bit **1: If any CH[1..4] DC FAULT STORED bit is set, fault signal is active**
1	FAULT ON OC STORED	R/W	1b	0: Fault signal is not activated by any CH[1..4] OC FAULT STORED bit **1: If any CH[1..4] OC FAULT STORED bit is set, fault signal is active**
0	FAULT ON ILIMIT STORED	R/W	1b	0: Fault signal is not activated by any CH[1..4] I-LIMIT FAULT STORED bit **1: If any CH[1..4] I-LIMIT FAULT STORED bit is set, fault signal is active**

7.6.1.28 Fault Sig Conf 2 Register (Offset = 0x1E) [reset = 0x00]

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Figure 7-41. Fault Sig Conf 2 Register

7	6	5	4	3	2	1	0
RESERVED	FAULT ON WARN	FAULT ON INVALID CLOCK	FAULT ON OTSD	FAULT ON POWER FAULT	RESERVED	RESERVED	FAULT ON INCOMPLETE LDG
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-38. Fault Sig Conf 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	FAULT ON WARN	R/W	0b	**0: Fault signal is not activated when warning singal is active.** 1: Fault signal is active when warning signal is active
5	FAULT ON INVALID CLOCK	R/W	0b	**0: Fault signal is not activated by INVALID CLOCK bit** 1: If INVALID CLOCK bit is set, fault signal is active
4	FAULT ON OTSD	R/W	0b	**0: Fault signal is not activated by any CH[1..4] OTSD bit or OTSD** 1: If any CH[1..4] OTSD bit or OTSD bit is set, fault signal is active
3	FAULT ON POWER FAULT	R/W	0b	**0: Fault Signal is not activated by any stored bit in "Power Fault Status Register"** 1: If VBAT UV bit, VBAT OV bit, PVDD UV bit, PVDD OV bit, or GVDD FAULT bit is set, fault signal is active.
2	RESERVED	R/W	0b	
1	RESERVED	R/W	0b	
0	FAULT ON INCOMPLETE LDG	R/W	0b	**0: Fault signal is not activated by any CH[1..4] LDG STATE REPORT bit** 1: If any CH[1..4] LDG STATE REPORT bit is not set, fault signal Is active

7.6.1.29 Warn Sig Conf 1 Register (Offset = 0x1F) [reset = 0x04]

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Figure 7-42. Warn Sig Conf 1 Register

7	6	5	4	3	2	1	0
RESERVED	WARN ON CLIP DET STORED	WARN ON INVALID CLOCK STORED	WARN ON OTSD STORED	WARN ON POWER FAULT STORED	WARN ON OTW STORED	WARN ON TGFB STORED	WARN ON ILIMIT STORED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b

Table 7-39. Warn Sig Conf 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	WARN ON CLIP DET STORED	R/W	0b	**0: Warning signal is not activated by any CH[1..4] CLIP STORED bit** 1: If any CH[1..4] CLIP STORED bit is set, warning signal is active
5	WARN ON INVALID CLOCK STORED	R/W	0b	**0: Warning signal is not activated by INVALID CLOCK STORED bit** 1: If INVALID CLOCK STORED bit is set, warning signal is active
4	WARN ON OTSD STORED	R/W	0b	**0: Warning signal is not activated by any CH[1..4] OTSD STORED bit or OTSD STORED** 1: If any CH[1..4] OTSD STORED bit or OTSD STORED bit is set, warning signal is active
3	WARN ON POWER FAULT STORED	R/W	0b	**0: Warning Signal is not activated by any stored bit in "Power Fault Memory Register"** 1: If VBAT UV STORED bit, VBAT OV STORED bit, PVDD UV STORED bit, PVDD OV STORED bit, DVDD POR STORED bit, or GVDD FAULT STORED bit is set, warning signal is active.
2	WARN ON OTW STORED	R/W	1b	0: Warning signal is not activated by any CH[1..4] OTW STORED bit or OTW STORED bit **1: If any CH[1..4] OTW STORED bit or OTW STORED bit is set, warning signal is active**
1	WARN ON TGFB STORED	R/W	0b	**0: Warning signal is not activated by TGFBW STORED** 1: Warning signal is active if TGFBW STORED is active
0	WARN ON ILIMIT STORED	R/W	0b	**0: Warning signal is not activated by any CH[1..4] I-LIMIT WARN STORED bit** 1: If any CH[1..4] I-LIMIT WARN STORED bit is set, warning signal is active

7.6.1.30 Warn Sig Conf 2 Register (Offset = 0x20) [reset = 0x00]

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Figure 7-43. Warn Sig Conf 2 Register

7	6	5	4	3	2	1	0
RESERVED		WARN ON INVALID CLOCK	WARN ON OTSD	WARN ON POWER FAULT	WARN ON OTW	WARN ON TGFB	WARN ON INCOMPLETE LDG
R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-40. Warn Sig Conf 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0b	
5	WARN ON INVALID CLOCK	R/W	0b	**0: Warning signal is not activated by INVALID CLOCK bit** 1: If INVALID CLOCK bit is set, warning signal is active
4	WARN ON OTSD	R/W	0b	**0: Warning signal is not activated by any CH[1..4] OTSD bit or OTSD** 1: If any CH[1..4] OTSD bit or OTSD bit is set, warning signal is active
3	WARN ON POWER FAULT	R/W	0b	**0: Warning Signal is not activated by any stored bit in "Power Fault Status Register"** 1: If VBAT UV bit, VBAT OV bit, PVDD UV bit, PVDD OV bit, or GVDD FAULT bit is set, warning signal is active.
2	WARN ON OTW	R/W	0b	**0: Warning signal is not activated by any CH[1..4] OTW bit or OTW bit** 1: If any CH[1..4] OTW STORED bit or OTW STORED bit is set, warning signal is active
1	WARN ON TGFB	R/W	0b	**0: Warning signal is not activated by TGFBW** 1: Warning signal is active if TGFBW is active
0	WARN ON INCOMPLETE LDG	R/W	0b	**0: Warning signal is not activated by any CH[1..4] LDG STATE REPORT bit** 1: If any CH[1..4] LDG STATE REPORT bit is not set, warning signal is active

7.6.1.31 Clip Det Sig Conf Register (Offset = 0x21) [reset = 0x00]

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Figure 7-44. Clip Det Sig Conf Register

7	6	5	4	3	2	1	0
RESERVED	CLIP DET EN	CLIP DET LVL		CLIP DET CH34 GRP2	CLIP DET CH34 GRP1	CLIP DET CH12 GRP2	CLIP DET CH12 GRP1
R/W-0b	R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-41. Clip Det Sig Conf Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	CLIP DET EN	R/W	0b	**0: Clip detect is disabled** 1: Clip detect is enabled
5-4	CLIP DET LVL	R/W	0b	**00: 2% THD** 01: 5% THD 10: 10% THD 11: 1% THD
3	CLIP DET CH34 GRP2	R/W	0b	**0: Clip Detect Signal Group 2 is not activated by CH3 CLIP or CH4 CLIP** 1: Clip Detect Signal Group 2 is active when CH3 CLIP or CH4 CLIP is active
2	CLIP DET CH34 GRP1	R/W	0b	**0: Clip Detect Signal Group 1 is not activated by CH3 CLIP or CH4 CLIP** 1: Clip Detect Signal Group 1 is active when CH3 CLIP or CH4 CLIP is active
1	CLIP DET CH12 GRP2	R/W	0b	**0: Clip Detect Signal Group 2 is not activated by CH1 CLIP or CH2 CLIP** 1: Clip Detect Signal Group 2 is active when CH1 CLIP or CH2 CLIP is active
0	CLIP DET CH12 GRP1	R/W	0b	**0: Clip Detect Signal Group 1 is not activated by CH1 CLIP or CH2 CLIP** 1: Clip Detect Signal Group 1 is active when CH1 CLIP or CH2 CLIP is active

7.6.1.32 Fault Pin Conf Register (Offset = 0x22) [reset = 0x00]

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Figure 7-45. Fault Pin Conf Register

7	6	5	4	3	2	1	0
RESERVED				FAULT PIN CONF			
R/W-0b				R/W-0b			

Table 7-42. Fault Pin Conf Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0b	
3-0	FAULT PIN CONF	R/W	0b	Fault Pin is set to: **0000: FaultZ** **Open Drain Output. Active low when fault signal is active.** 0001: WarningZ - Open Drain Output. Active low when warning signal is active. 0010: Clip Detect 1 - Buffer Output. Active high when clip detect group 1 signal is active. 0011: Clip Detect 2 - Buffer Output. Active high when clip detect group 2 signal is active.

7.6.1.33 GPIO Conf Register (Offset = 0x23) [reset = 0x00]

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Figure 7-46. GPIO Conf Register

7	6	5	4	3	2	1	0
GPIO2 PIN CONF				GPIO1 PIN CONF			
R/W-0b				R/W-0b			

Table 7-43. GPIO Conf Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO2 PIN CONF	R/W	0b	GPIO 2 pin set to: **0000: Hi-Z** 0001: WarningZ Pin - Open Drain Output. Active low when warning signal is active. 0010: FaultZ Pin - Open Drain Output. Active low when fault signal is active. 0011: Clip Detect 1 - Buffer Output. Active high when clip detect group 1 signal is active. 0100: Clip Detect 2 - Buffer Output. Active high when clip detect group 2 signal is active. 0101: Sync out - Buffer Output. Sends output stage switching frequency 0110: DVDD (high) 0111: GND (low) 1000: Sync in - Input. Accepts switching frequency of clock master device 1001: MuteZ - Input. Low level input will mute the device
3-0	GPIO1 PIN CONF	R/W	0b	GPIO 1 pin set to: **0000: Hi-Z** 0001: WarningZ - Open Drain Output. Active low when warning signal is active. 0010: FaultZ - Open Drain Output. Active low when fault signal is active. 0011: Clip Detect 1 - Buffer Output. Active high when clip detect group 1 signal is active. 0100: Clip Detect 2 - Buffer Output. Active high when clip detect group 2 signal is active. 0101: Sync out - Buffer Output. Sends output stage switching frequency 0110: DVDD (high) 0111: GND (low) 1000: Sync in - Input. Accepts switching frequency of clock master device 1001: MuteZ - Input. Low level input will mute the device

7.6.1.34 AC LDG Ctrl 1 Register (Offset = 0x24) [reset = 0x00]

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Figure 7-47. AC LDG Ctrl 1 Register

7	6	5	4	3	2	1	0
RESERVED			AC DIAG GAIN	CH1 AC DIAG START	CH2 AC DIAG START	CH3 AC DIAG START	CH4 AC DIAG START
R/W-0b			R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-44. AC LDG Ctrl 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0b	
4	AC DIAG GAIN	R/W	0b	**0: Gain 1 (0-100 Ω)** 1: Gain 8 (0-12.5 Ω)
3	CH1 AC DIAG START	R/W	0b	**0: Normal operation** 1: Start AC diagnostic on channel 1 once channel is in Hi-Z mode
2	CH2 AC DIAG START	R/W	0b	**0: Normal operation** 1: Start AC diagnostic on channel 2 once channel is in Hi-Z mode
1	CH3 AC DIAG START	R/W	0b	**0: Normal operation** 1: Start AC diagnostic on channel 3 once channel is in Hi-Z mode
0	CH4 AC DIAG START	R/W	0b	**0: Normal operation** 1: Start AC diagnostic on channel 4 once channel is in Hi-Z mode

7.6.1.35 AC LDG Ctrl 2 Register (Offset = 0x25) [reset = 0x8]

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Figure 7-48. AC LDG Ctrl 2 Register

7	6	5	4	3	2	1	0
RESERVED				TW DET AVG	RESERVED	TW DET CALC TYPE	TW DET JUDGE
R/W-0b				R/W-1b	R/W-0b	R/W-0b	R/W-0b

Table 7-45. AC LDG Ctrl 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0b	
3	TW DET AVG	R/W	1b	0: Fast mode **1: Normal mode**
2	RESERVED	R/W	0b	
1	TW DET CALC TYPE	R/W	0b	**0: AC pass/fail judgement type 2** Calculate magnitude of impedance as Re(Z)+0.5*Im(Z) 1: AC pass/fail judgement type 1 Calculate magnitude of impedance as Re(Z)
0	TW DET JUDGE	R/W	0b	**0: Enable Tweeter detection judegement** Calculate magnitude of impedance Check whether calculated result is lower than tweeter detection threshold value If yes, set tweeter detection bit 1: Disable Tweeter detection calculation

7.6.1.36 TWEETER DET THRESH Register (Offset = 0x26) [reset = 0x00]

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Figure 7-49. TWEETER DET THRESH Register

7	6	5	4	3	2	1	0
TW DET THRESHOLD							
R/W-0b							

Table 7-46. TWEETER DET THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TW DET THRESHOLD	R/W	0b	Set the reference value for AC load diag pass/fail judgement. 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.37 AC LDG Rprt CH1 R Register (Offset = 0x27) [reset = 0x00]

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Figure 7-50. AC LDG Rprt CH1 R Register

7	6	5	4	3	2	1	0
CH1 AC IMP R							
R-0b							

Table 7-47. AC LDG Rprt CH1 R Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1 AC IMP R	R	0b	Register value corresponds to the real part of complex impedance seen at CH1 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.38 AC LDG Rprt CH1 I Register (Offset = 0x28) [reset = 0x00]

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Figure 7-51. AC LDG Rprt CH1 I Register

7	6	5	4	3	2	1	0
CH1 AC IMP I							
R-0b							

Table 7-48. AC LDG Rprt CH1 I Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH1 AC IMP I	R	0b	Register value corresponds to the complement of the imaginary part of complex impedance seen at CH1 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.39 AC LDG Rprt CH2 R Register (Offset = 0x29) [reset = 0x00]

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Figure 7-52. AC LDG Rprt CH2 R Register

7	6	5	4	3	2	1	0
CH2 AC IMP R							
R-0b							

Table 7-49. AC LDG Rprt CH2 R Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2 AC IMP R	R	0b	Register value corresponds to the real part of complex impedance seen at CH2 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.40 AC LDG Rprt CH2 I Register (Offset = 0x2A) [reset = 0x00]

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Figure 7-53. AC LDG Rprt CH2 I Register

7	6	5	4	3	2	1	0
CH2 AC IMP I							
R-0b							

Table 7-50. AC LDG Rprt CH2 I Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH2 AC IMP I	R	0b	Register value corresponds to the complement of the imaginary part of complex impedance seen at CH2 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.41 AC LDG Rprt CH3 R Register (Offset = 0x2B) [reset = 0x00]

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Figure 7-54. AC LDG Rprt CH3 R Register

7	6	5	4	3	2	1	0
CH3 AC IMP R							
R-0b							

Table 7-51. AC LDG Rprt CH3 R Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3 AC IMP R	R	0b	Register value corresponds to the real part of complex impedance seen at CH3 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.42 AC LDG Rprt CH3 I Register (Offset = 0x2C) [reset = 0x00]

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Figure 7-55. AC LDG Rprt CH3 I Register

7	6	5	4	3	2	1	0
CH3 AC IMP I							
R-0b							

Table 7-52. AC LDG Rprt CH3 I Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH3 AC IMP I	R	0b	Register value corresponds to the complement of the imaginary part of complex impedance seen at CH3 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.43 AC LDG Rprt CH4 R Register (Offset = 0x2D) [reset = 0x00]

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Figure 7-56. AC LDG Rprt CH4 R Register

7	6	5	4	3	2	1	0
CH4 AC IMP R							
R-0b							

Table 7-53. AC LDG Rprt CH4 R Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4 AC IMP R	R	0b	Register value corresponds to the real part of complex impedance seen at CH4 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.44 AC LDG Rprt CH4 I Register (Offset = 0x2E) [reset = 0x00]

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Figure 7-57. AC LDG Rprt CH4 I Register

7	6	5	4	3	2	1	0
CH4 AC IMP I							
R-0b							

Table 7-54. AC LDG Rprt CH4 I Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CH4 AC IMP I	R	0b	Register value corresponds to the complement of the imaginary part of complex impedance seen at CH4 output 0.8 Ω/code if AC DIAG GAIN = 0 0.1 Ω/code if AC DIAG GAIN = 1 See Section 7.6.1.34

7.6.1.45 TWEETER DET Register (Offset = 0x2F) [reset = 0x00]

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Figure 7-58. TWEETER DET Register

7	6	5	4	3	2	1	0
RESERVED				CH1 TW DET	CH2 TW DET	CH3 TW DET	CH4 TWDET
R-0b				R-0b	R-0b	R-0b	R-0b

Table 7-55. TWEETER DET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	
3	CH1 TW DET	R	0b	**0: No tweeter detected on channel 1.** 1: Tweeter detected on channel 1.
2	CH2 TW DET	R	0b	**0: No tweeter detected on channel 2.** 1: Tweeter detected on channel 2.
1	CH3 TW DET	R	0b	**0: No tweeter detected on channel 3.** 1: Tweeter detected on channel 3.
0	CH4 TW DET	R	0b	**0: No tweeter detected on channel 4.** 1: Tweeter detected on channel 4.

7.6.1.46 Misc Control 3 Register (Offset = 0x30) [reset = 0x00]

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Figure 7-59. Misc Control 3 Register

7	6	5	4	3	2	1	0
CLEAR FAULT	RESERVED	PRECHG TIME		OTSD AUTO RECOVERY	RESERVED	PULL UP	RESERVED
W-0b	R/W-0b	R/W-0b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-56. Misc Control 3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLEAR FAULT	W	0b	**0: Normal operation** 1: Clear fault
6	RESERVED	R/W	0b	
5-4	PRECHG TIME	R/W	0b	Precharge wait time sets the time for AC coupling input caps to settle during startup **0: 20 ms** 1: 15 ms 2: 40 ms 3: 50 ms
3	OTSD AUTO RECOVERY	R/W	0b	**0: Device will not auto recover from over temperature shutdown** 1: Device will auto recover from over temperature shutdown
2	RESERVED	R/W	0b	
1	PULL UP	R/W	0b	Control internal pull-up for GPIO1 and GPIO2 if configured to Open Drain Output **0: Enable internal pull-up** 1: Disable internal pull-up
0	RESERVED	R/W	0b	

7.6.1.47 REVID Register (Offset = 0x32) [reset = 0x00]

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Figure 7-60. REVID Register

7	6	5	4	3	2	1	0
REV ID							
R-0b							

Table 7-57. REVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REV ID	R	0x21	Revision ID

7.6.1.48 TGFB Ctrl Register (Offset = 0x33) [reset = 0x00]

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Figure 7-61. TGFB Ctrl Register

7	6	5	4	3	2	1	0
ZC WAIT TIME		BYPASS	ZC BYPASS	ATTACK		RELEASE	
R/W-0b		R/W-0b	R/W-0b	R/W-0b		R/W-0b	

Table 7-58. TGFB Ctrl Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ZC WAIT TIME	R/W	0b	System waits this period for zero crossing, then changes gain regardless. **00: 20 µs** 01: 80 µs 10: 320 µs 11: 1280 µs
5	BYPASS	R/W	0b	**0: Enable Thermal Gain Foldback** 1: Disable Thermal Gain Foldback
4	ZC BYPASS	R/W	0b	**0: Enable zero crossing detection** 1: Disable zero crossing detection. Gain changes as soon as thermal condition is met without waiting for zero detection.
3-2	ATTACK	R/W	0b	**00: 1 dB / 100ms** 01: 1 dB / 200ms 10: 1 dB / 400ms 11: 1 dB / 800ms
1-0	RELEASE	R/W	0b	**00: 1 dB / 200ms** 01: 1 dB / 400ms 10: 1 dB / 800ms 11: 1 dB / 1600ms

7.6.1.49 AC LDG FREQ Ctrl Register (Offset = 0x34) [reset = 0xC8]

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Figure 7-62. AC LDG FREQ Ctrl Register

7	6	5	4	3	2	1	0
STIMULUS FREQUENCY (93.75 Hz/bit)							
R/W-11001000b							

Table 7-59. AC LDG FREQ Ctrl Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	STIMULUS FREQUENCY (93.75 Hz/bit)	R/W	11001000b	0000 0000: Default. 18.75kHz 0000 0001: 93.75 Hz 0000 0010: 187.5 Hz …. **1100 1000: 18.75 kHz** …. 1111 1111: 23.90625 kHz

7.6.1.50 SYNC Ctrl Register (Offset = 0x35) [reset = 0x1]

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Figure 7-63. SYNC Ctrl Register

7	6	5	4	3	2	1	0
RESERVED				SYNC ERROR WD		SYNC ERROR DET BYPASS	MASTER SLAVE
R/W-0b				R/W-0b		R/W-0b	R/W-1b

Table 7-60. SYNC Ctrl Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0b	
3-2	SYNC ERROR WD	R/W	0b	SYNC Clock Error watchdog timer. For PWM frequency of 2.1MHz or 2.3MHz, timer set to **00: 2.5µs** 01: 5µs 10: 7.5µs 11: 10µs For PWM frequency of 384kHz, 460kHz or 576kHz, timer set to **00: 5µs** 01: 10µs 10: 15µs 11: 20µs
1	SYNC ERROR DET BYPASS	R/W	0b	**0: SYNC Clock Error detection** 1: Clock Error Detection bypassed
0	MASTER SLAVE	R/W	1b	0: Slave Mode - GPIO 1 or 2 need to be configured as SYNC IN and external clock required **1: Master Mode - Device generates clock internally**

7.6.1.51 Misc Control 4 Register (Offset = 0x36) [reset = 0x00]

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Figure 7-64. Misc Control 4 Register

7	6	5	4	3	2	1	0
RESERVED	TLSBY	SSC4		SPREAD SPECTRUM SYNC CLOCK	PWM FREQUENCY		
R/W-0b	R/W-0b	R/W-0b		R/W-0b	R/W-0b		

Table 7-61. Misc Control 4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6	TLSBY	R/W	0b	Three level mode for standby pin 0: Two level mode **1: Three level mode with MUTE at mid-voltage level**
5-4	SSC4	R/W	0b	Spread Spectrum Control 4
3	SPREAD SPECTRUM SYNC CLOCK	R/W	0b	Select whether sync clock input will be spread spectrum modulated before setting PWM frequency. Applies if device is set to clock slave mode. **0: Spread spectrum mode applied to clock sync input signal** 1: Spread spectrum mode not applied to clock sync input signal
2-0	PWM FREQUENCY	R/W	0b	PWM switching frequency setting: **000: 2.1 MHz** 001: 2.3 MHz 010: 576 kHz 011: 384 kHz 100: 460 kHz

7.6.1.52 SS Control 1 Register (Offset = 0x37) [reset = 0x22]

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Figure 7-65. SS Control 1 Register

7	6	5	4	3	2	1	0
SSC1							
R/W-100010b							

Table 7-62. SS Control 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SSC1	R/W	100010b	Spread Spectrum Control 1

7.6.1.53 SS Control 2 Register (Offset = 0x38) [reset = 0x80]

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Figure 7-66. SS Control 2 Register

7	6	5	4	3	2	1	0
SS ENABLE	RESERVED	SSC3		SSC2			
R/W-1b	R/W-0b	R/W-0b		R/W-0b			

Table 7-63. SS Control 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SS ENABLE	R/W	1b	0: Disable spread spectrum mode **1: Enable spread spectrum mode**
6	RESERVED	R/W	0b	
5-4	SSC3	R/W	0b	Spread Spectrum Control 3
3-0	SSC2	R/W	0b	Spread Spectrum Control 2

7.6.1.54 PWM Phase Ctrl 1 Register (Offset = 0x39) [reset = 0x40]

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Figure 7-67. PWM Phase Ctrl 1 Register

7	6	5	4	3	2	1	0
RESERVED	PHASE CH2			RESERVED			PHASE SEL
R/W-0b	R/W-100b			R/W-0b			R/W-0b

Table 7-64. PWM Phase Ctrl 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6-4	PHASE CH2	R/W	100b	Phase offset of Channel 2 vs Channel 1 in manual mode 000: 0 degree 001: 45 degree 010: 90 degree 011: 135 degree **100: 180 degree** 101: 225 degree 110: 270 degree 111: 315 degree
3-1	RESERVED	R/W	0b	
0	PHASE SEL	R/W	0b	Adjustment mode for PWM phase of channel 2, 3 and 4 relative to channel 1 **0: Manual mode** 1: Automatic mode

7.6.1.55 PWM Phase Ctrl 2 Register (Offset = 0x3A) [reset = 0x62]

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Figure 7-68. PWM Phase Ctrl 2 Register

7	6	5	4	3	2	1	0
RESERVED	PHASE CH4			RESERVED	PHASE CH3		
R/W-0b	R/W-110b			R/W-0b	R/W-10b		

Table 7-65. PWM Phase Ctrl 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0b	
6-4	PHASE CH4	R/W	110b	Phase offset of Channel 4 vs Channel 1 in manual mode 000: 0 degree 001: 45 degree 010: 90 degree 011: 135 degree 100: 180 degree 101: 225 degree **110: 270 degree** 111: 315 degree
3	RESERVED	R/W	0b	
2-0	PHASE CH3	R/W	10b	Phase offset of Channel 3 vs Channel 1 in manual mode 000: 0 degree 001: 45 degree **010: 90 degree** 011: 135 degree 100: 180 degree 101: 225 degree 110: 270 degree 111: 315 degree

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPA6304-Q1 is a four-channel analog input Class-D audio-amplifier design for use in automotive head units and external amplifier modules. The TPA6304-Q1 incorporates the necessary functionality to perform in demanding OEM applications.

8.1.1 AM Radio Avoidance

AM-radio frequency interference is avoided by setting the switching frequency of the device above the AM band. The switching frequency options available for AM avoidance are 2.1 MHz and 2.3 MHz.

8.1.2 Parallel BTL Operation (PBTL)

The device has the capability of placing two channels into a parallel configuration that allows for twice the current drive capability for low impedance loads. BTL and PBTL modes can be me mixed. Channels 1 and 2 can be placed in PBTL, channels 3 and 4 can be placed into PBTL, or both pairs can be placed in PBTL. Follow the Typical application schematic for proper input and output connections for PBTL configuration useing both pairs. The speaker output connections must be made on the speaker side of the LC filter. The device can drive more current with paralleling BTL channels on the load side of the LC output filter. The input connections on channel 2 and channel 4 should be connected to ground.

The Mode Control Register has to be set for PBTL operations. Bit 4 sets channels 1 and 2 to PBTL and Bit 5 sets channels 3 and 4 to PBTL. These bits must only be changed while the $\overline{\text{STANDBY}}$ pin is asserted low.

Load diagnostics is supported for PBTL channels.

8.1.3 Reconstruction Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. The amplifier outputs require a reconstruction filter that comprises a series inductor and a capacitor to ground on each half-bridge output, generally called an LC filter. The LC filter attenuates the PWM frequency and reduces electromagnetic emissions, allowing the reconstructed audio signal to pass to the speakers. Design of the reconstruction filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N requirements, the selection of the inductors used in the output filter should be carefully considered. Refer to the Class-D LC Filter Design, *SLAA701A*, application report for a detailed description of proper component description and design of the LC filter based upon the specified load and frequency response.

The recommended low-pass cutoff frequency of the LC filter is dependent on the selected switching frequency. The low-pass cutoff frequency can be as high as 100 kHz for a PWM frequency of 2.1 MHz.

Certain specifications must be understood for a proper inductor. See the application note TAS6424-Q1 Inductor Selection Guide, *SLOA242*, for information on selection the proper inductor. The inductance value is given at zero current, but the inductors do have current through them as the TPA6304-Q1 drives current into the load. Use the inductance versus current curve for the inductor to made sure the inductance does not drop below 2 µH (for f_{sw} = 2.1 MHz) at the maximum current for the system design during normal operation. The DCR of the inductor directly affects the output power of the system design. The lower the DCR, the more power is provided to the speakers. The typical inductor DCR for a 4 Ω system is 40 to 50 mΩ and for a 2 Ω system is 15 to 25 mΩ.

8.1.4 Bootstrap Capacitors

The bootstrap capacitors provide the gate-drive voltage of the upper N-channel FET. These capacitors must be sized appropriately for the system specification. For typical applications use 1 µF.

8.1.5 Line Driver Applications

In many automotive audio applications, the same head unit must drive either a speaker (with several Ω of impedance) or an external amplifier input (with several kilo Ω of impedance). The design is capable of supporting both applications and has special line driver gain and diagnostics. Coupled with the high switching frequency the device is well suited for this type of application. The line driver mode uses the same signal path as the normal speaker output mode with similar audio performance. Set the desired channel in line driver mode via the Mode Control Register and the desired gain via the Misc Control 2 Register. The external connected amplifier needs to have a differential impedance between 600 Ω and 4.7 kΩ for the DC line diagnostic to detect the connected external amplifier. Figure 8-1 shows the recommended external amplifier input configuration, balanced capacitor coupled.

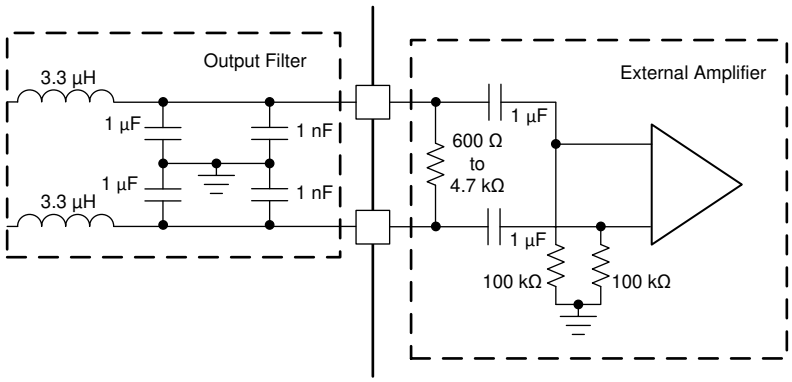

Figure 8-1. Line Driver External Amplifier Input Configuration

8.2 Typical Applications

8.2.1 BTL Application

Figure 8-2 shows the schematic of a typical 4-channel solution for a head-unit application.

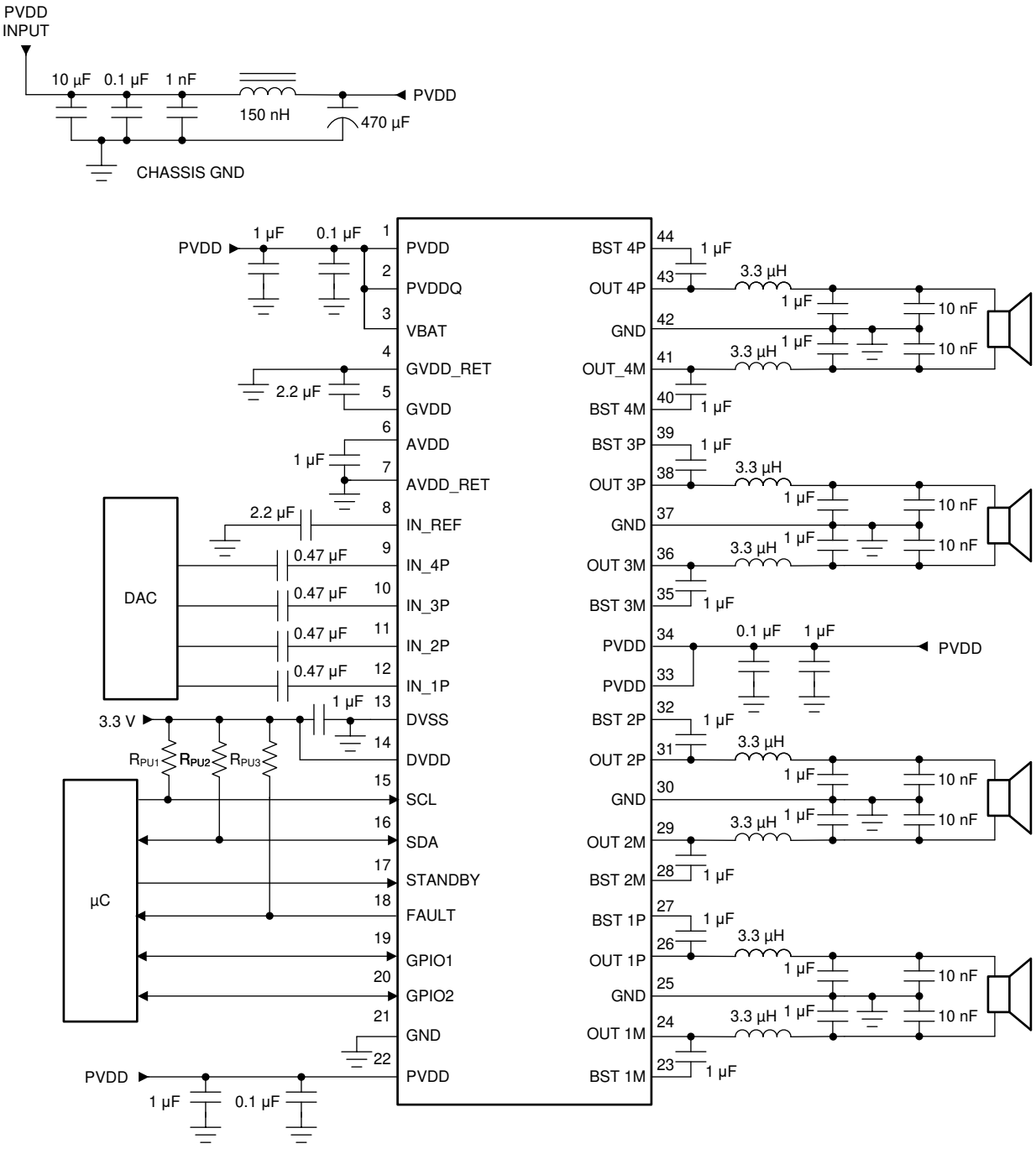

Figure 8-2. Typical 4-Channel BTL Application Schematic

8.2.1.1 Design Requirements

This head-unit example is focused on the smallest solution size for 4 times 25 W output power into 4 Ω with a battery supply of 14.4 V.

The switching frequency is set above the AM-band at 2.1 MHz.

The selection of a 2.1 MHz switching frequency enables the use of a small output inductor value of 3.3 µH which leads to a very small footprint.

8.2.1.2 Detailed Hardware Design Procedure

Use the following procedure for the hardware design:

- Determine the output power that is required into the load. The output power requirement determines the required power supply voltage and current. The output reconstruction filter components that are required are also driven by the output power.
- With the requirements, adjust the typical application schematic in Figure 8-2.

8.2.2 PBTL Application

Figure 8-3 shows a schematic of a typical 2-channel solution for a head unit or external amplifier application where high power into 2 Ω is required.

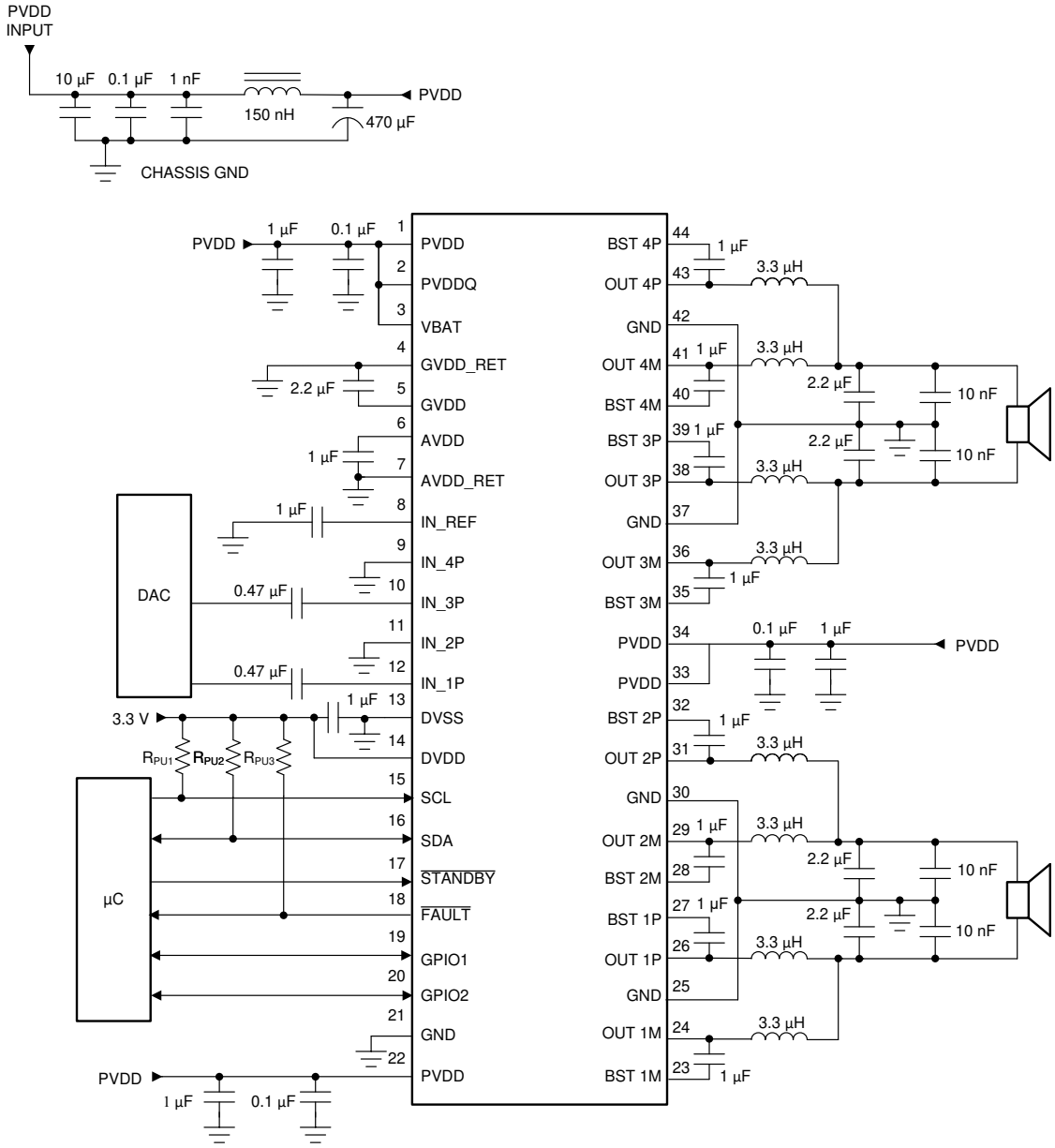

Figure 8-3. 2-Channel PBTL Application Schematic

8.2.2.1 Detailed Hardware Design Procedure

Use the following procedure for the hardware design:

- Determine the output power that is required into the load. The output power requirement determines the required power supply voltage and current. The output reconstruction filter components that are required are also driven by the output power.
- With the requirements, adjust the typical application schematic in Figure 8-3.

9 Power Supply Recommendations

The TPA6304-Q1 requires a minimum of two power supply rails, PVDD and DVDD, when PVDD and VBAT are connected to the same supply. In the case VBAT is different from PVDD, then three power supplies will be required. The PVDD supply is the high-current supply that provides power to the output stage. The VBAT supply is a lower current rail that provides power to the lower voltage circuitry. The DVDD supply is the 3.3 V logic supply and must be maintained in the tolerance as shown in the *Recommended Operating Conditions* table.

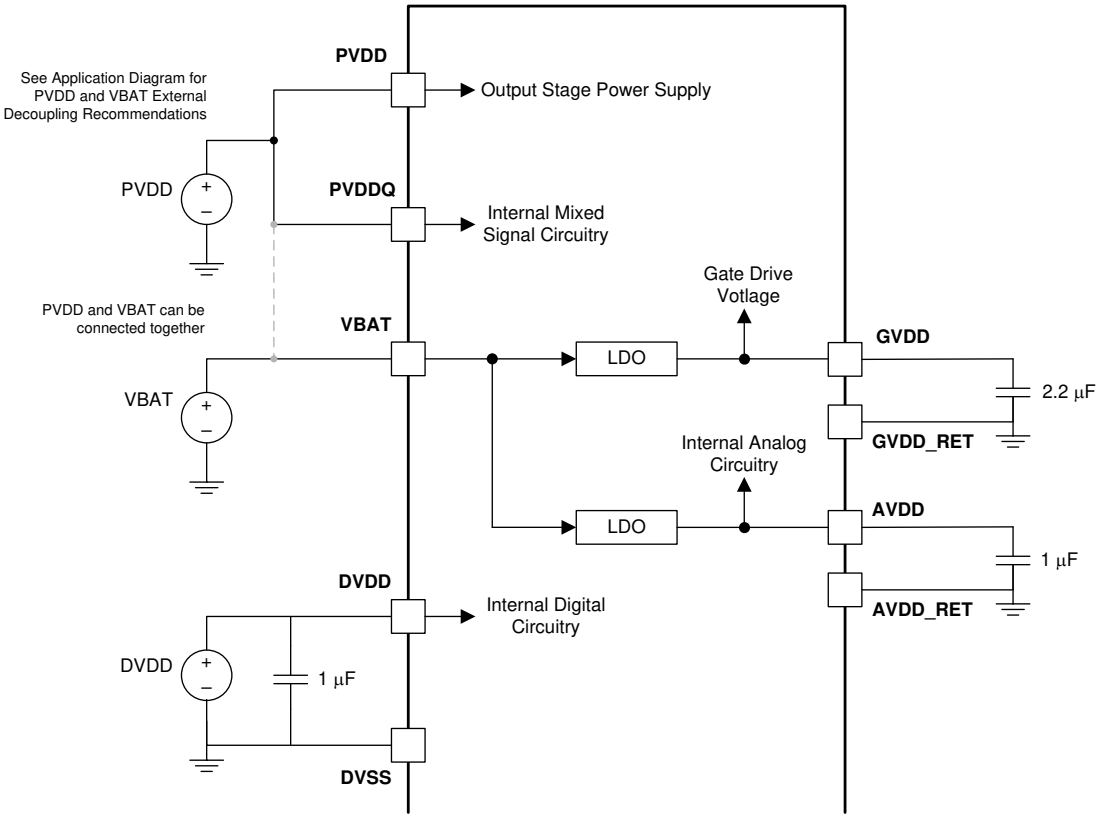

Figure 9-1. Power Supply Block

10 Layout

10.1 Layout Guidelines

The pinout of the TPA6304-Q1 was selected to provide flow through layout with all high-power connections on the right side, and all low-power signals and supply decoupling on left side.

Section 10.2 shows the area for the components in the application example (see the *Figure 8-2* section). This layout example is taken from the EVM PCB.

The TPA6304-Q1 EVM uses a four-layer PCB. The copper thickness was selected as 70 µm to optimize power loss.

The small value of the output filter provides a small size and, in this case, the low height of the inductor enables double sided mounting.

10.1.1 Electrical Connection of Thermal Pad and Heat Sink

For the DDV package, the heat sink connected to the thermal pad of the device should be connected to GND. The thermal pad must not be connected to any other electrical node.

10.1.2 General Considerations

The EVM layout is optimized for low noise and EMC performance.

The TPA6304-Q1 has an exposed thermal pad that is up, away from the PCB. The layout must consider an external heat sink.

Refer to Layout Top Example for the following guidelines:

- A ground plane, A, on the same side as the device pins helps reduce EMI by providing a very-low loop impedance for the high-frequency switching current.
- The decoupling capacitors on PVDD, B, are very close to the device with the ground return close to the ground pins.
- The ground connections for the capacitors in the LC filter, C, have a direct path back to the device and also the ground return for each channel is the shared. This direct path allows for improved common mode EMI rejection.
- The traces from the output pins to the inductors, D, should have the shortest trace possible to allow for the smallest loop of large switching currents.
- Heat-sink mounting screws, E, should be close to the device to keep the loop short from the package to ground.
- Many vias, F, stitching together the ground planes can create a shield to isolate the amplifier and power supply.

10.2 Layout Example

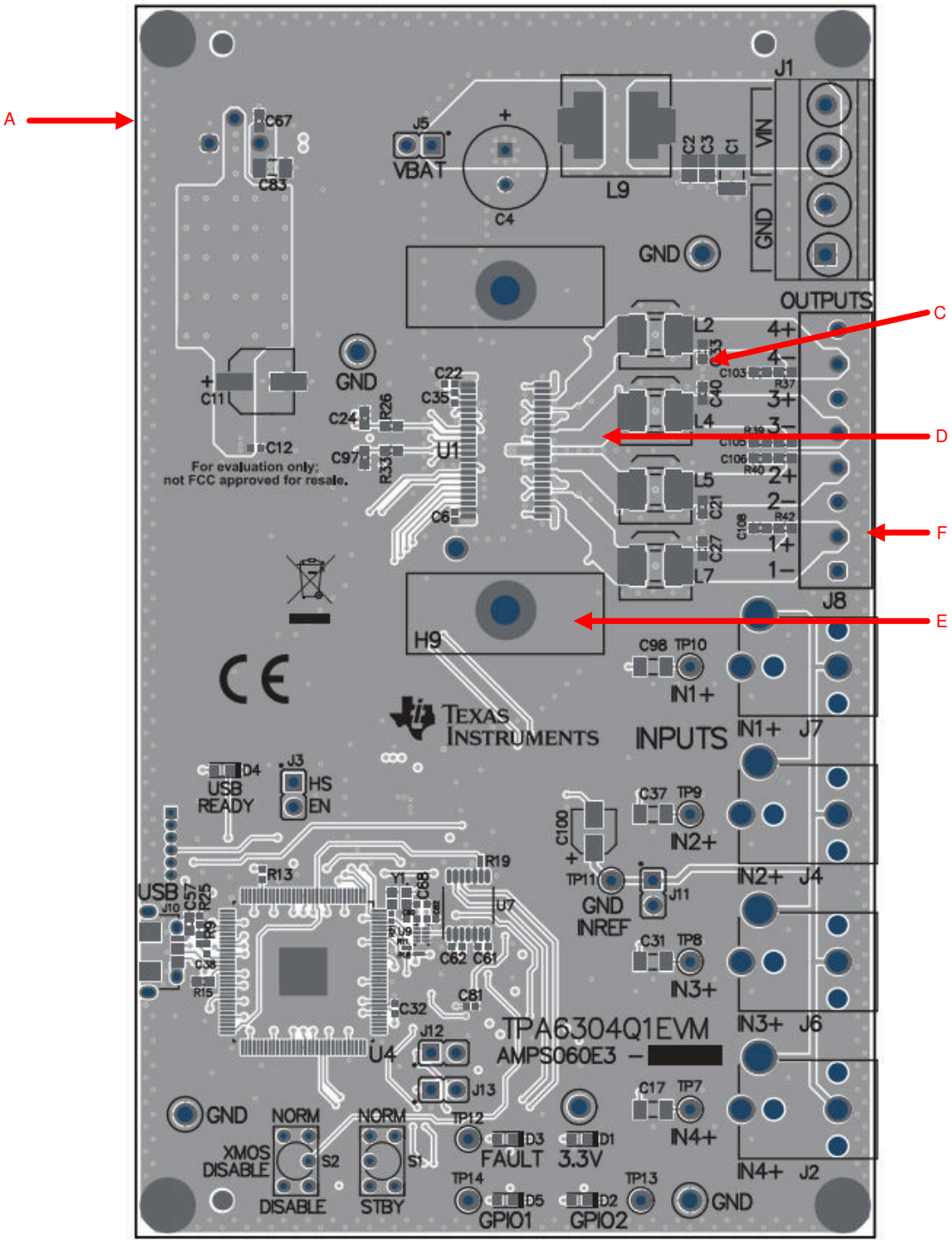

Figure 10-1. Layout Top Example

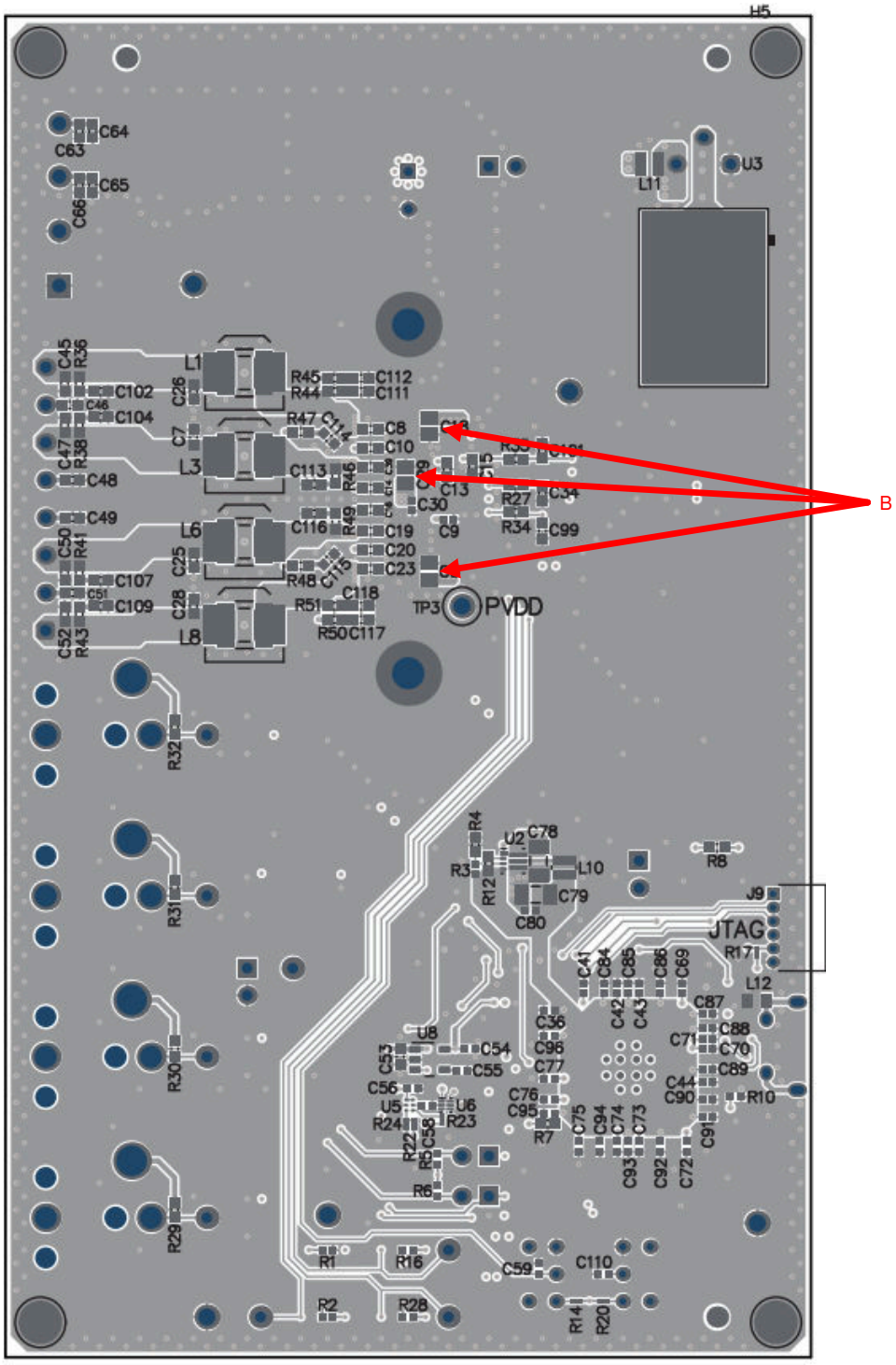

Figure 10-2. Layout Bottom Example

10.3 Thermal Considerations

The thermally enhanced PowerPAD package has an exposed pad up for connection to a heat sink. The output power of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system, such as the ambient operating temperature. The heat sink absorbs heat from the TPA6304-Q1 and transfers it to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. Heat sinks can be smaller than that of classic linear amplifier design

because of the excellent efficiency of class-D amplifiers. This device is intended for use with a heat sink, therefore, $R_{\theta JC}$ is used as the thermal resistance from junction to the exposed metal package. This resistance dominates the thermal management, so other thermal transfers is not considered. The thermal resistance of $R_{\theta JA}$ (junction to ambient) is required to determine the full thermal solution. The thermal resistance is comprised of the following components:

- $R_{\theta JC}$ of the TPA6304-Q1
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

The thermal resistance of the thermal interface material can be determined from the manufacturer's value for the area thermal resistance (expressed in °Cmm^2/W) and the area of the exposed metal package. For example, a typical, white, thermal grease with a 0.0254 mm (0.001 inch) thick layer is approximately 4.52°C mm^2/W. The TPA6304-Q1 in the DDV44 package has an exposed area of 28.7 mm^2. By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the thermal grease. The thermal resistance of the thermal grease is 0.157°C/W

Table 10-1 lists the modeling parameters for one device on a heat sink. The junction temperature is assumed to be 115°C while delivering an average power of 10 watts per channel into a 4 Ω load. The thermal-grease example previously described is used for the thermal interface material. Use Equation 1 to design the thermal system.

$$R_{\theta JA} = R_{\theta JC} + \text{thermal interface resistance} + \text{heat sink resistance} \quad (1)$$

Table 10-1. Thermal Modeling

Description	Value
Ambient Temperature	25°C
Average Power to load	20W (4 x 5W)
Power dissipation	6W (See Figure 6-7)
Junction Temperature	115°C
ΔT inside package	3.6°C (0.6°C/W × 6W)
ΔT through thermal interface material	0.942°C (0.157°C/W × 6W)
Required heat sink thermal resistance	14.24°C/W ([115°C – 25°C – 3.6°C – 0.942°C] / 6W)
System thermal resistance to ambient $R_{\theta JA}$	14.99°C/W

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

PurePath™ Console 3 Graphical Development Suite

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6304QDDVRQ1	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA6304
TPA6304QDDVRQ1.A	Active	Production	HTSSOP (DDV) | 44	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPA6304

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

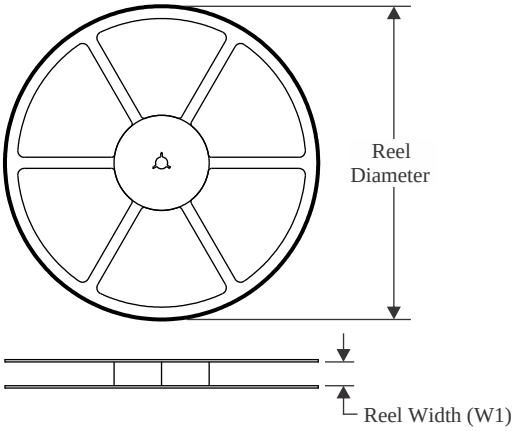
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

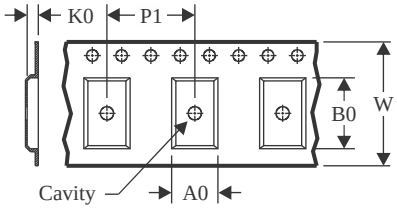
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

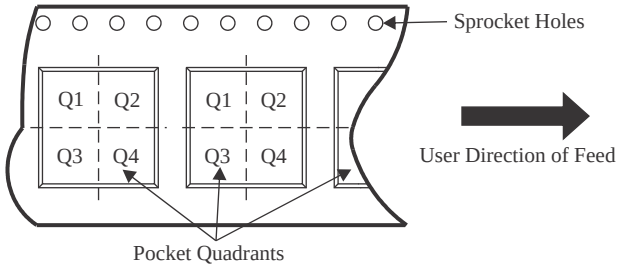


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

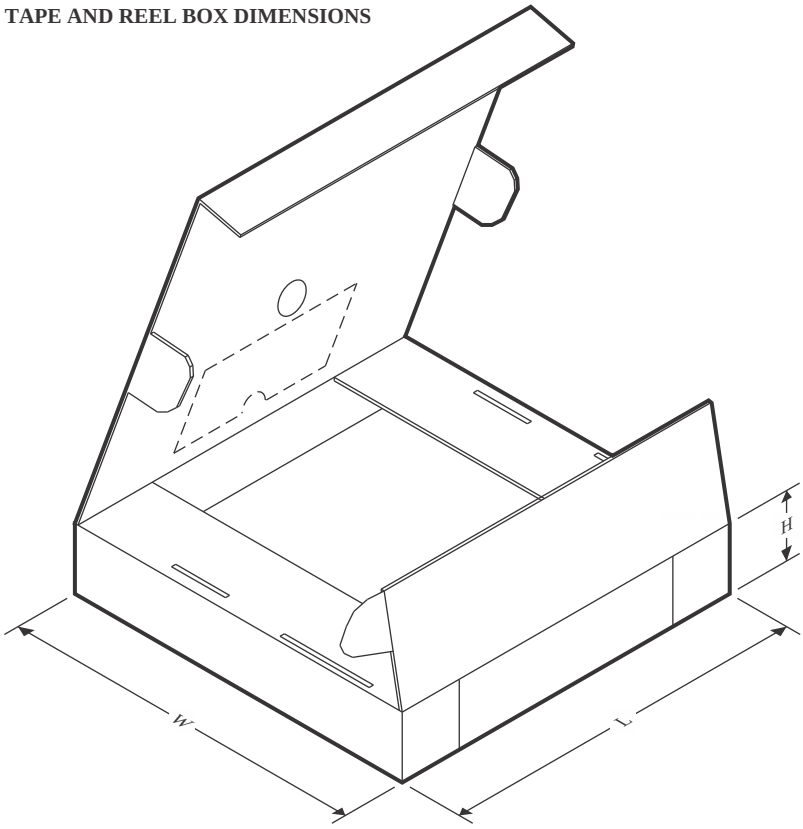
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6304QDDVRQ1	HTSSOP	DDV	44	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

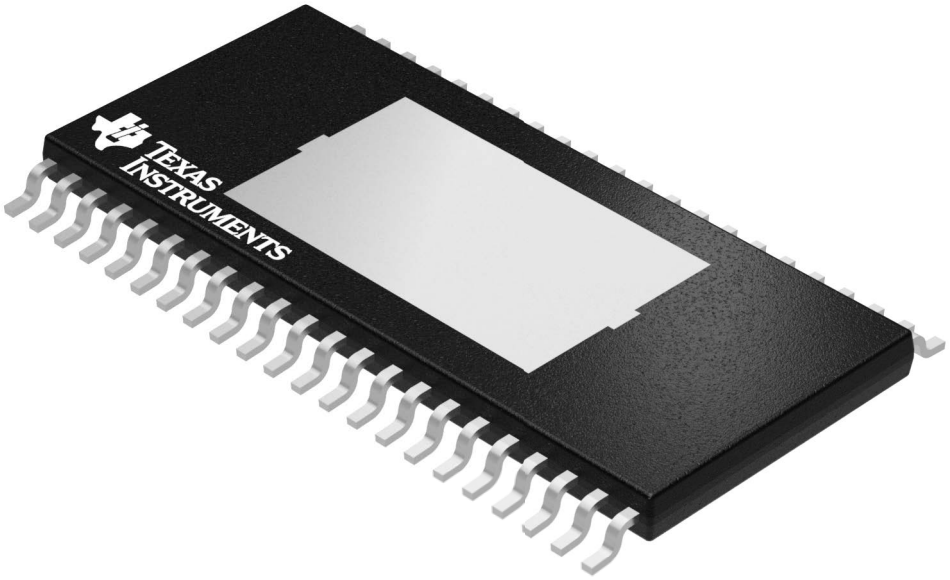


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6304QDDVRQ1	HTSSOP	DDV	44	2000	356.0	356.0	45.0

DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

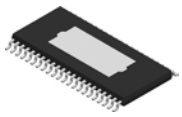
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

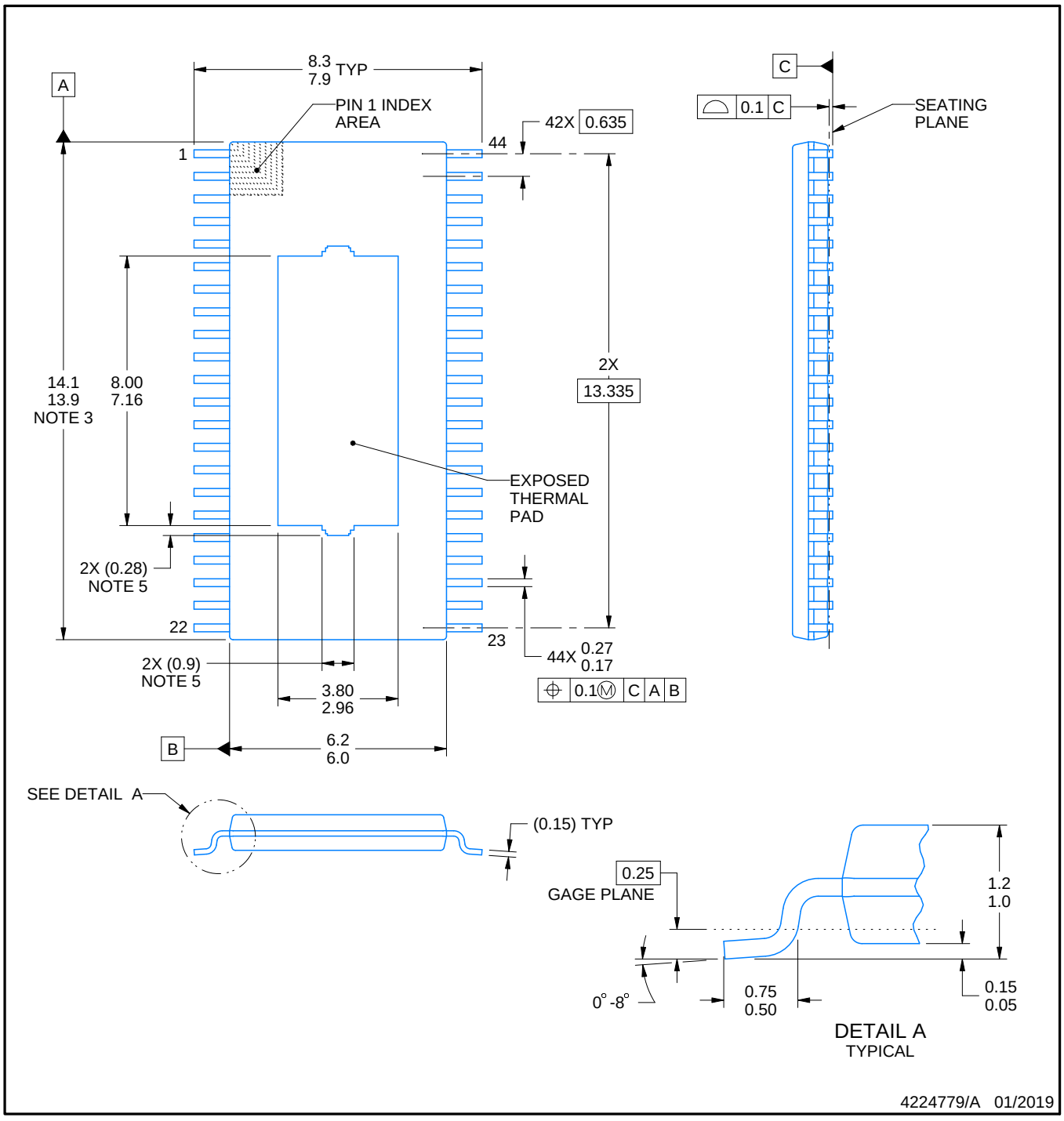
PACKAGE OUTLINE

DDV0044E



PowerPAD™ TSSOP - 1.2 mm max height

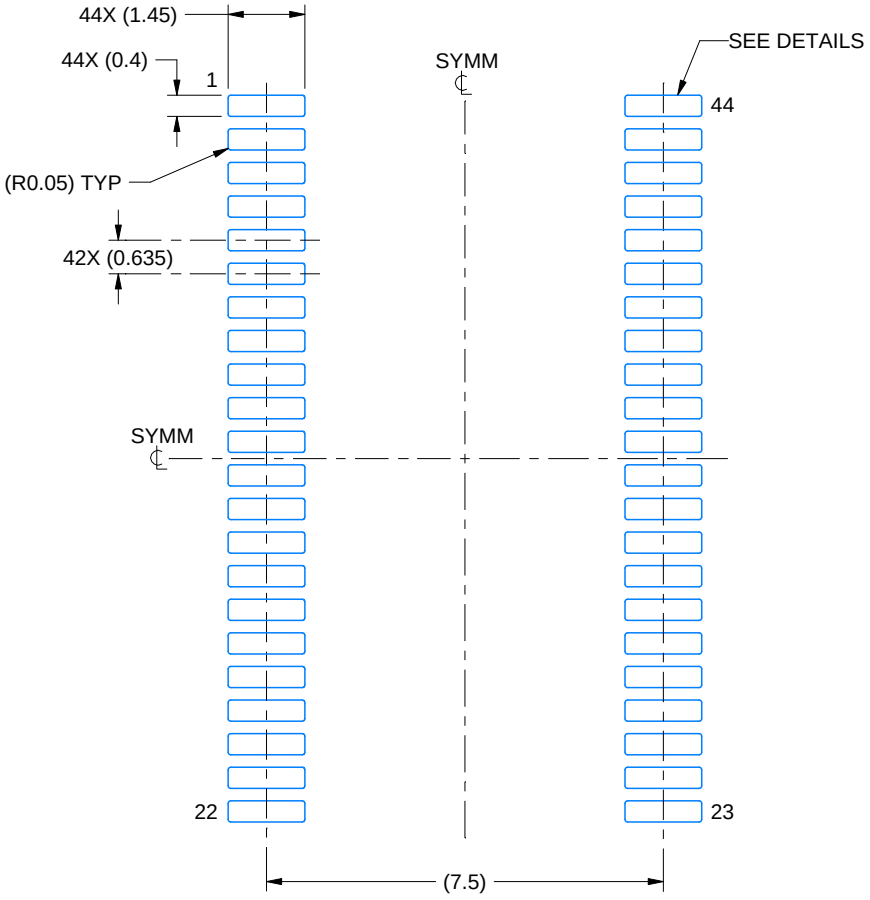
PLASTIC SMALL OUTLINE



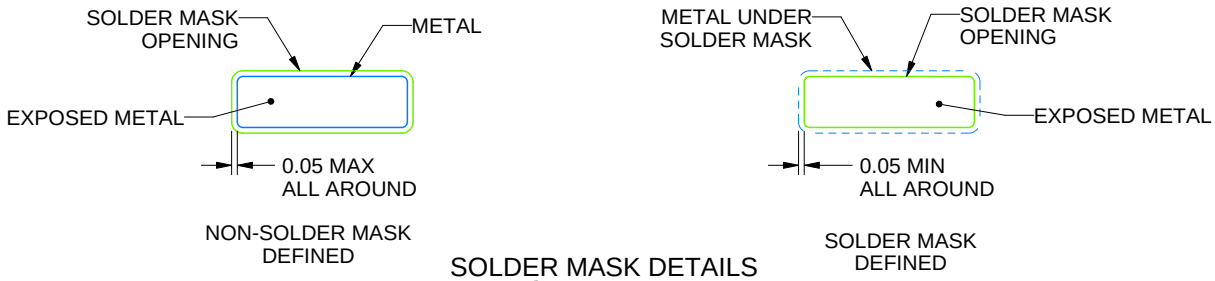
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



SOLDER MASK DETAILS

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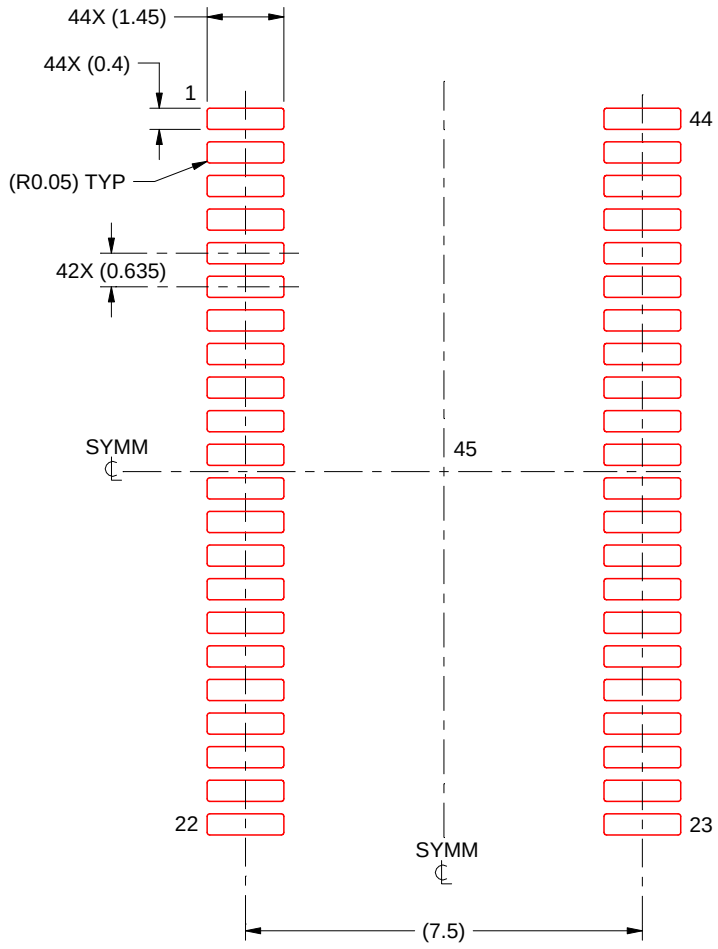
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 7X

4224779/A 01/2019

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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