TPDxE05U06 1, 4, 6 Channel ESD Protection Device for Super-Speed (Up to 6 Gbps) Interface

1 Features

- IEC 61000-4-2 level 4 ESD protection
  - ±12kV contact discharge
  - ±15kV air gap discharge
- IEC 61000-4-4 EFT protection
  - 80A (5/50ns)
- IEC 61000-4-5 surge protection
  - 2.5A (8/20µs)
- IO capacitance 0.42pF to 0.5pF (typical)
- DC breakdown voltage 6.5V (minimum)
- Ultra low leakage current 10nA (maximum)
- Low ESD clamping voltage
- Industrial temperature range: –40°C to +125°C
- Easy straight-through routing packages
- Industry standard SOD-523 package (1.60mm × 0.80mm × 0.65mm)

2 Applications

- HDMI 1.4*b*
- HDMI 2.0
- USB 3.0
- MHL
- LVDS interfaces
- DisplayPort
- PCI-express®
- eSata interfaces
- V-by-One® HS

3 Description

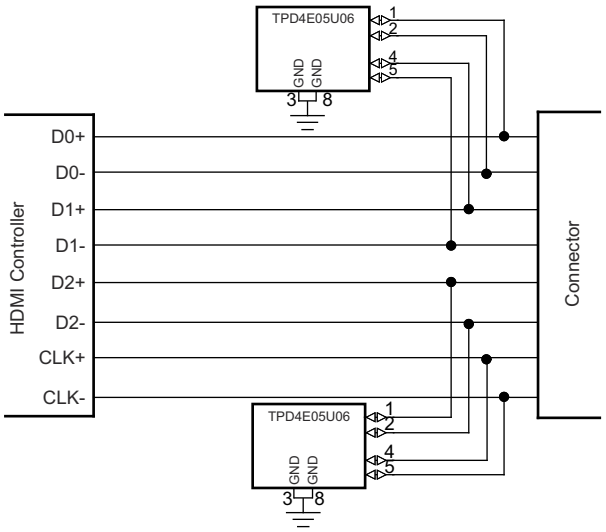
The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06 ultra-low loading capacitance makes the device and excellent choice for protecting any high-speed signal pins.

Typical applications for TPDxE05U06 includes high speed signal lines in HDMI 1.4*b*, HDMI 2.0, USB 3.0, MHL, LVDS, DisplayPort, PCI-Express®, eSata, and V-by-One® HS.

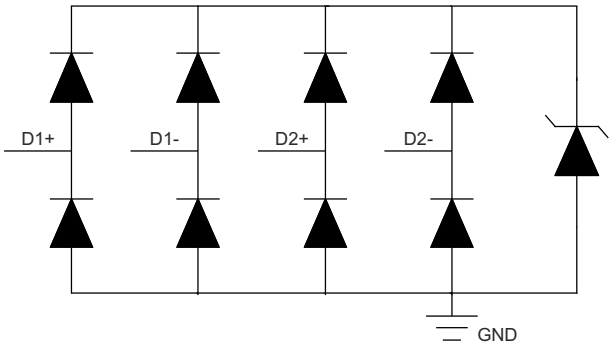
Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
TPD1E05U06	1 channel	DPY (X1SON, 2)
		DYA (SOD-523, 2)
TPD4E05U06	4 channels	DQA (USON, 10)
TPD6E05U06	6 channels	RVZ (USON, 14)

(1) For more information, see Section 10.



Simplified Schematic



TPD4E05U06 Functional Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

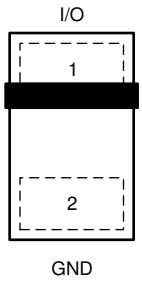


Figure 4-1. DPY Package 2-Pin X1SON (Top View)

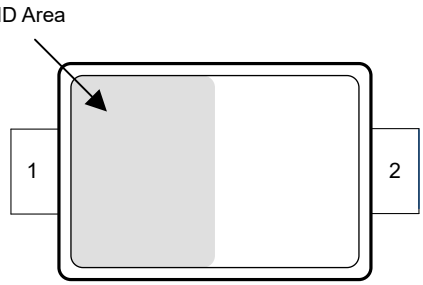


Figure 4-2. DYA Package 2-Pin SOD-523 (Top View)

Table 4-1. Pin Functions TPD1E05U06 DPY and DYA

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
GND	2	Ground	Ground; Connect to ground
I/O	1	I/O	ESD protected channel(2)

(1) I = input, O = output
(2) Place as close to the connector as possible.

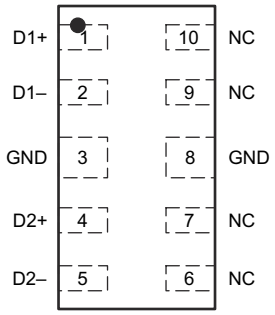


Figure 4-3. DQA Package 10-Pin USON (Top View)

Table 4-2. Pin Functions TPD4E05U06 DQA

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
D1+	1	I/O	ESD protected channel(2)
D1–	2	I/O	ESD protected channel(2)
D2+	4	I/O	ESD protected channel(2)
D2–	5	I/O	ESD protected channel(2)
GND	3	Ground	Ground; Connect to ground
GND	8		
NC	6	—	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	7		
NC	9		
NC	10		

(1) I = input, O = output
(2) Place as close to the connector as possible.

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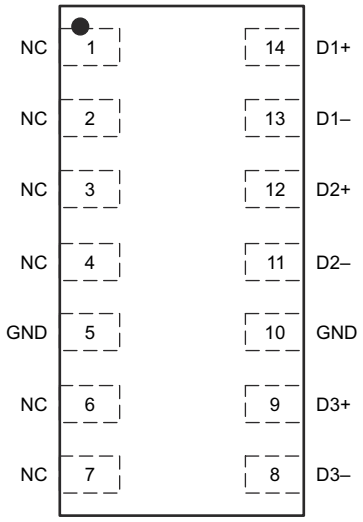


Figure 4-4. RVZ Package 14-Pin USON (Top View)

Table 4-3. Pin Functions TPD6E05U06 RVZ

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
D1+	14	I/O	ESD protected channel(2)
D1–	13	I/O	ESD protected channel(2)
D2+	12	I/O	ESD protected channel(2)
D2–	11	I/O	ESD protected channel(2)
D3+	9	I/O	ESD protected channel(2)
D3–	8	I/O	ESD protected channel(2)
GND	5	Ground	Ground; Connect to ground
GND	10		
NC	1	—	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	2		
NC	3		
NC	4		
NC	6		
NC	7		

(1) I = input, O = output
(2) Place as close to the connector as possible.

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5 Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Electrical Fast Transient (2) (3)	IEC 61000-4-4 (5/50ns)		80	A
Peak Pulse (2) (3)	IEC 61000-4-5 Current (8/20us)		2.5	A
	IEC 61000-4-5 Power (8/20us)		40	W
T_A	Ambient Operating Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	155	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25℃

5.1 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge – DPY, DQA, and RVZ	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	V
$V_{(ESD)}$	Electrostatic discharge – DYA	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±4000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1500 V may actually have higher performance.

5.2 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±12000	V
		IEC 61000-4-2 air-gap discharge	±15000	

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	0		5.5	V
T_A	Operating free-air temperature	-40		125	°C

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5.3 Thermal Information

THERMAL METRIC (1)		TPD1E05U06		TPD4E05U06	TPD6E05U06	UNIT
		DPY (X1SON)	DYA (SOD523)	DQA (USON)	RVZ (USON)	
		2 PINS	2 PINS	10 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	697.3	772.1	327	197.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	471	444.6	189.5	119.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	575.9	540.4	257.7	92.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	175.7	159.9	60.9	22	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	575.1	533.9	257	91.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITION		MIN	TYP	MAX	UNIT
INPUT - OUTPUT RESISTANCE								
V_{RWM}	Reverse stand-off voltage		I_{IO} < 10 µA				5.5	V
V_{BR}	Break-down voltage		I_{IO} = 1 mA		6.5		8.5	V
V_{Clamp}	Clamp voltage		I_{PP} = 1 A, TLP, from I/O to GND (1)			10		V
			I_{PP} = 5 A, TLP, from I/O to GND (1)			14		
			I_{PP} = 1 A, TLP, from GND to I/O (1)			3		
			I_{PP} = 5 A, TLP, from GND to I/O (1)			7		
I_{LEAK}	Leakage current		V_{IO} = 2.5 V			0.01	10	nA
R_{DYN}	Dynamic resistance	DPY package	I/O to GND (2)			0.8		Ω
			GND to I/O (2)			0.8		
		DYA package	I/O to GND (2)			0.8		
			GND to I/O (2)			0.7		
		DQA package	I/O to GND (2)			0.8		
			GND to I/O (2)			0.8		
		RVZ package	I/O to GND (2)			0.8		
			GND to I/O (2)			0.8		
CAPACITANCE								
C_L	Line capacitance (3)		V_{IO} = 2.5 V; f = 1 MHz , I/O to GND	TPD1E05U06 DPY package		0.42		pF
				TPD1E05U06 DYA package		0.42		
				TPD4E05U06 DQA package		0.5		
				TPD6E05U06 RVZ package		0.47		
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of input capacitance		GND Pin = 0 V, f = 1 MHz, VBIAS = 2.5 V, Channel x pin to GND – channel y pin to GND			0.05	0.07	pF

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5.4 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
C_{CROSS}	Channel to channel input capacitance	GND Pin = 0 V, f = 1 MHz, VBIAS = 2.5 V, between channel pins		0.01	0.06	pF

(1) Transition line pulse with 100 ns width, 200 ps rise time.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A.
(3) Capacitance data is taken at 25°C.

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5.5 Typical Characteristics

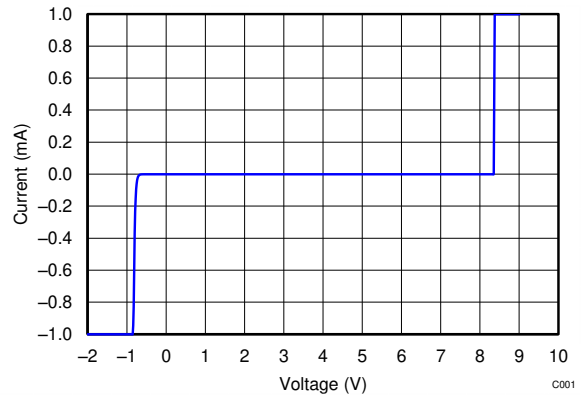


Figure 5-1. DC Voltage Sweep I-V Curve

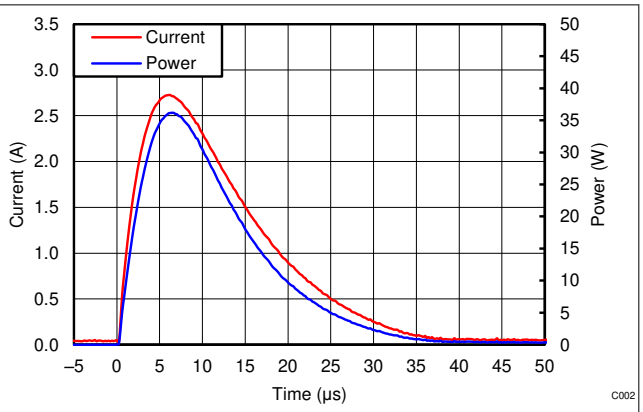


Figure 5-2. Surge Curve (tp = 8/20 µs), Pin IO to GND

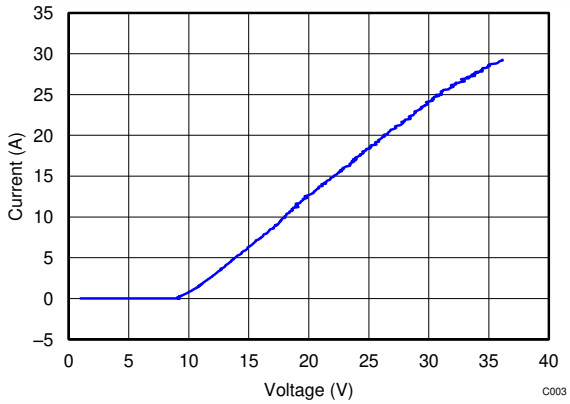


Figure 5-3. Positive TLP Plot IO to GND

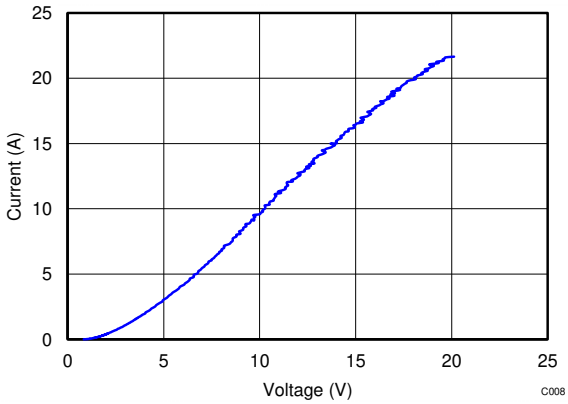


Figure 5-4. Negative TLP Plot IO to GND

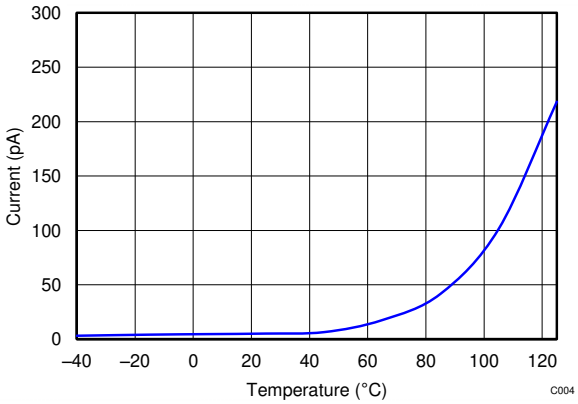


Figure 5-5. Leakage vs Temperature

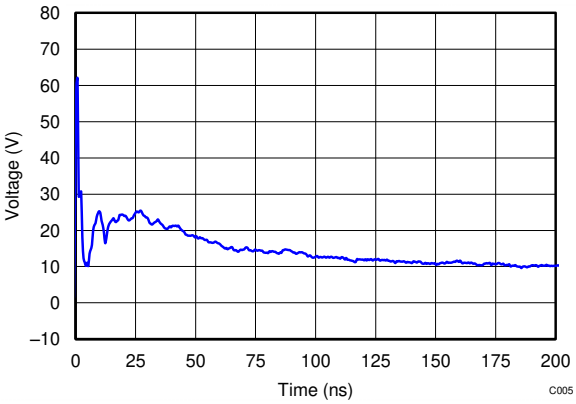


Figure 5-6. 8-kV IEC Waveform

5.5 Typical Characteristics (continued)

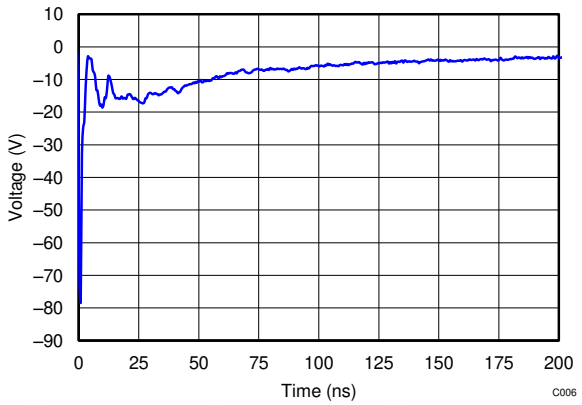


Figure 5-7. –8-kV IEC Waveform

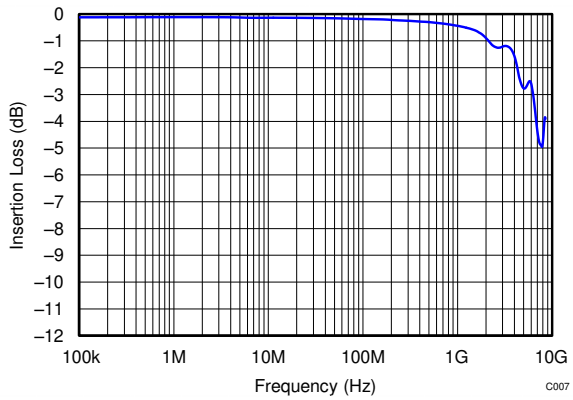


Figure 5-8. TPD1E05U06 Insertion Loss

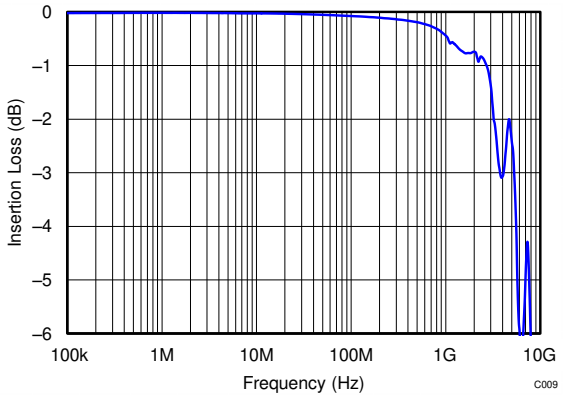


Figure 5-9. TPD4E05U06 Insertion Loss

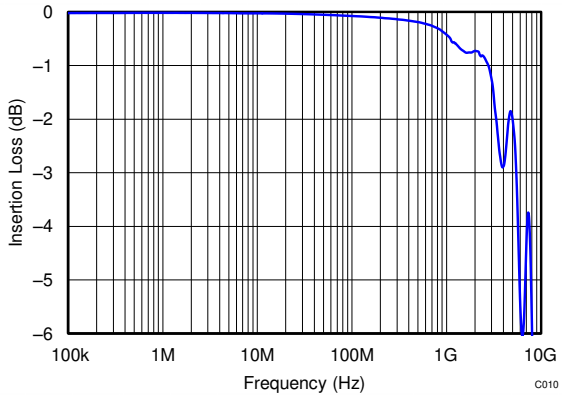


Figure 5-10. TPD6E05U06 Insertion Loss

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6 Detailed Description

6.1 Overview

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06 ultra-low loading capacitance makes the device an excellent choice for protecting any high-speed signal pins.

6.2 Functional Block Diagram

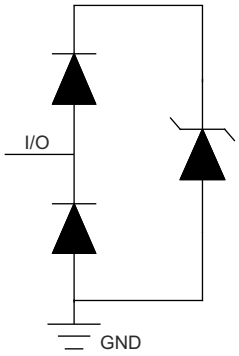


Figure 6-1. TPD1E05U06 Block Diagram

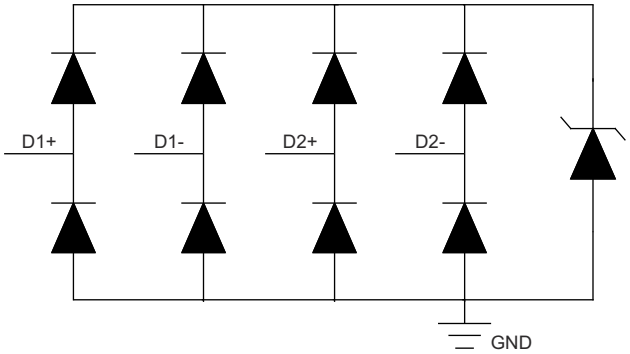


Figure 6-2. TPD4E05U06 Block Diagram

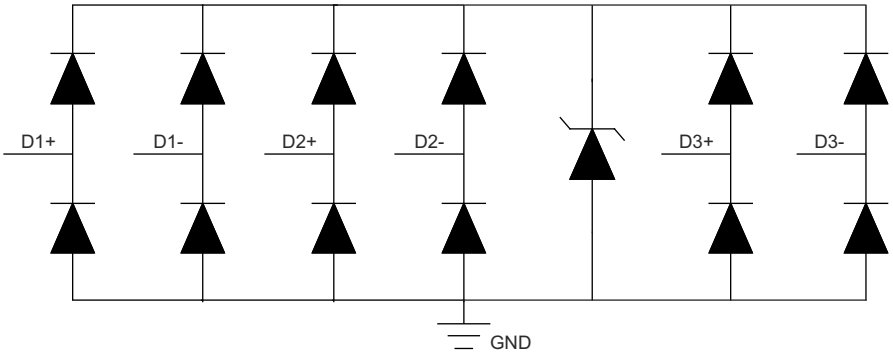


Figure 6-3. TPD6E05U06 Block Diagram

6.3 Feature Description

The TPDxE05U06 is a family of unidirectional Transient Voltage Suppressor (TVS) Electrostatic Discharge (ESD) protection diodes with ultra-low capacitance. Each device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The TPDxE05U06s ultra-low loading capacitance makes it and excellent choice for protecting any high-speed signal pins.

6.3.1 ±15-kV IEC61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air. An ESD-surge clamp diverts the current to ground.

6.3.2 IEC61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground. This has been validated on the TPD4E05U06 only.

6.3.3 IEC61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 40 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

6.3.4 I/O Capacitance

The capacitance between each I/O pin to ground is 0.42 pF (TPD1E05U06), 0.5 pF (TPD4E05U06) or 0.47 pF (TPD6E05U06). These devices support data rates up to 6 Gbps.

6.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5V, which protects sensitive equipment from surges above the reverse standoff voltage of 5.5V.

6.3.6 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of 2.5 V.

6.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 10 V (I_{PP} = 1 A).

6.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

6.3.9 Easy Flow-Through Routing

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

6.4 Device Functional Modes

The TPDxE05U06 is a passive integrated circuit that triggers when voltages are above VBR or below the lower diodes V_f (–0.6 V). During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPDxE05U06 (usually within 10s of nano-seconds) the device reverts to passive.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPDxE05U06 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

7.2 Typical Applications

7.2.1 HDMI 2.0 Application

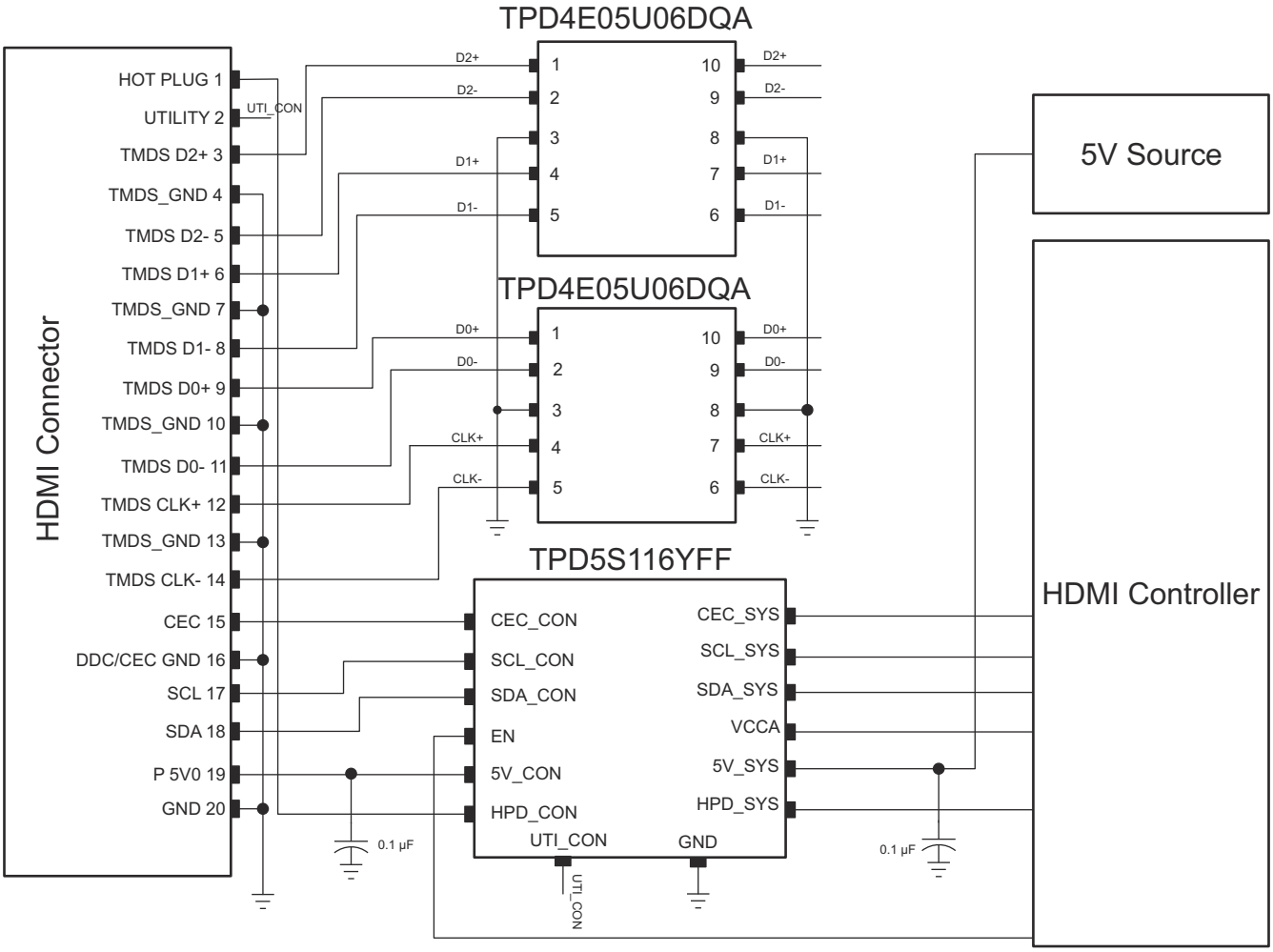


Figure 7-1. HDMI 2.0 Schematic

7.2.1.1 Design Requirements

For this design example, the two TPD4E05U06 devices, and a TPD5S116 are being used in an HDMI 2.0 application. This provides a complete port protection scheme.

Given the HDMI 2.0 application, the parameters listed in Table 7-1 are known.

Table 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1, 2, 4, or 5	0 V to 5 V
Operating frequency	3 GHz

7.2.1.2 Detailed Design Procedure

7.2.1.2.1 Signal Range on Pin 1, 2, 4, or 5

The TPD4E05U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels is going to protect which signal lines. Any I/O supports a signal range of 0 to 5.5 V.

7.2.1.3 Application Curves

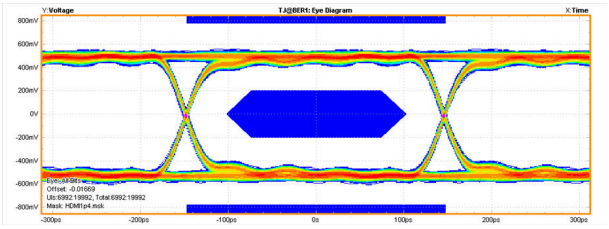


Figure 7-2. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram Unpopulated EVM

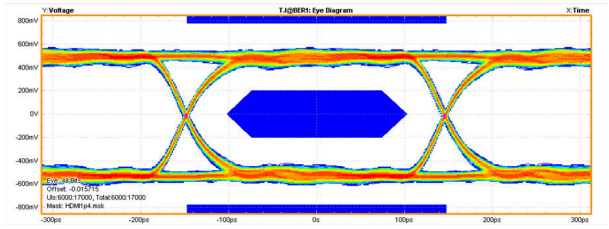


Figure 7-3. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD1E05U06

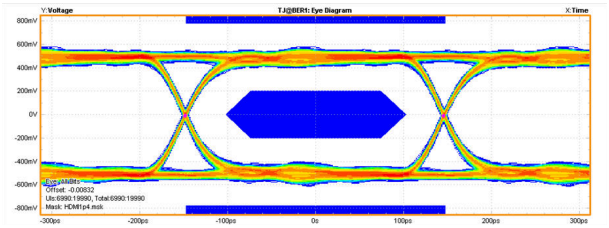


Figure 7-4. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD4E05U06

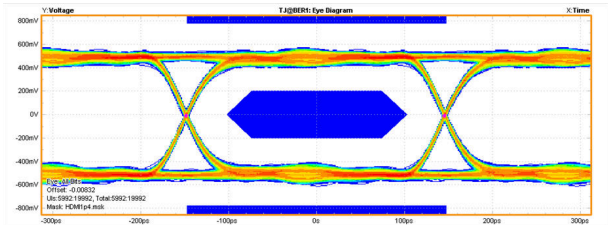


Figure 7-5. 3.4-Gbps HDMI 1.4 TP1 Eye Diagram TPD6E05U06

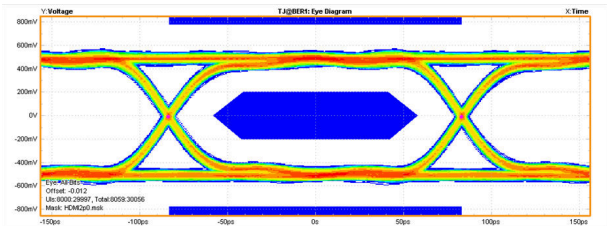


Figure 7-6. 6-Gbps HDMI 2.0 (TP1) Eye Diagram Unpopulated EVM

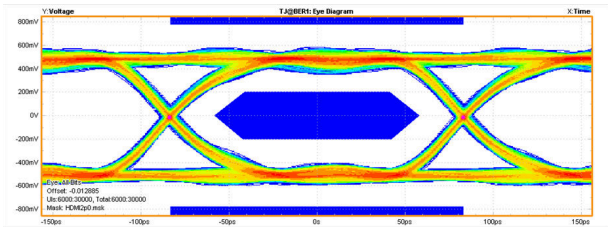


Figure 7-7. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD1E05U06

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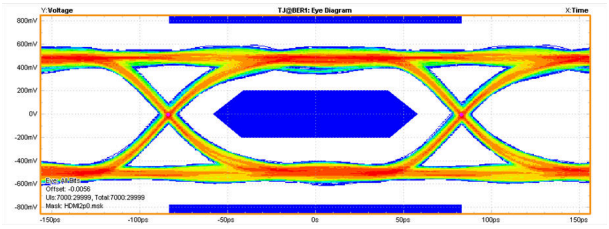


Figure 7-8. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD4E05U06

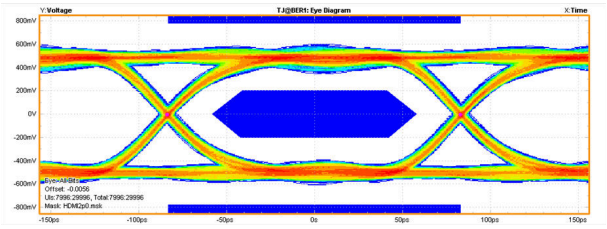


Figure 7-9. 6-Gbps HDMI 2.0 (TP1) Eye Diagram TPD6E05U06

7.2.2 HDMI 2.0 Application

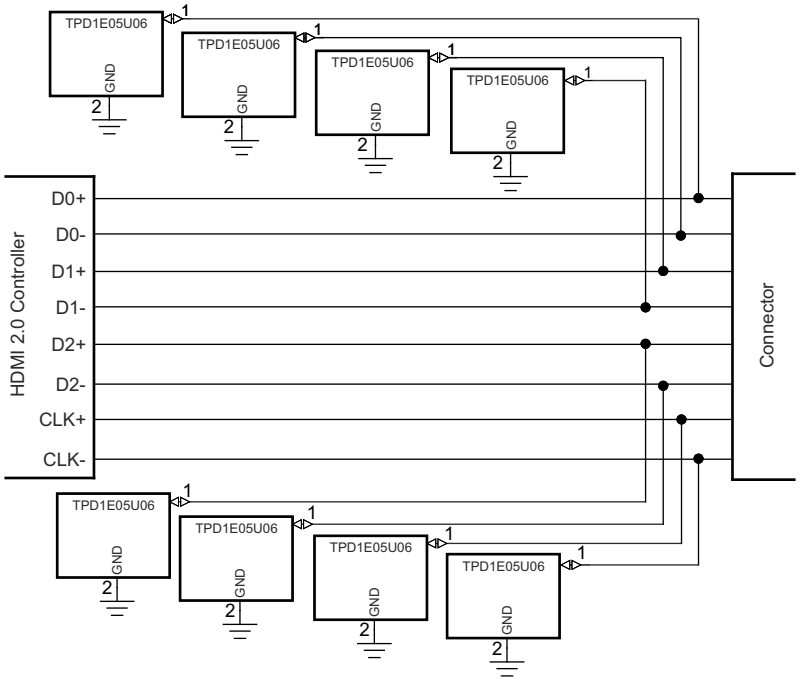


Figure 7-10. HDMI 2.0 Schematic

7.2.2.1 Design Requirements

For this design example, the TPD1E05U06 and the TPD5S116 are used to protect the data pairs and control lines of the HDMI 2.0 connection. This provides full HDMI 2.0 port protection.

Given the HDMI 2.0 application, the following parameters in Table 7-2 are known.

Table 7-2. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on data lines	0 V to 5 V
Operating frequency	3 GHz

7.2.2.2 Detailed Design Procedure

7.2.2.2.1 Signal Range

The TPD1E05U06 has 1 protection channel for signal lines, supporting a signal range of 0 V to 5.5 V.

7.2.2.2.2 Operating Frequency

The TPD1E05U06 has 0.42 pF of capacitance, which supports HDMI 2.0 data rates.

7.2.2.3 Application Curves

Refer to the *Section 7.2.1.3* section.

7.3 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care must be taken to make sure that the maximum voltage specifications for each line are not violated.

7.4 Layout

7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

7.4.2 Layout Example

7.4.2.1 TPD4E05U06 Layout Example

This application is typical of an HDMI 1.4 layout.

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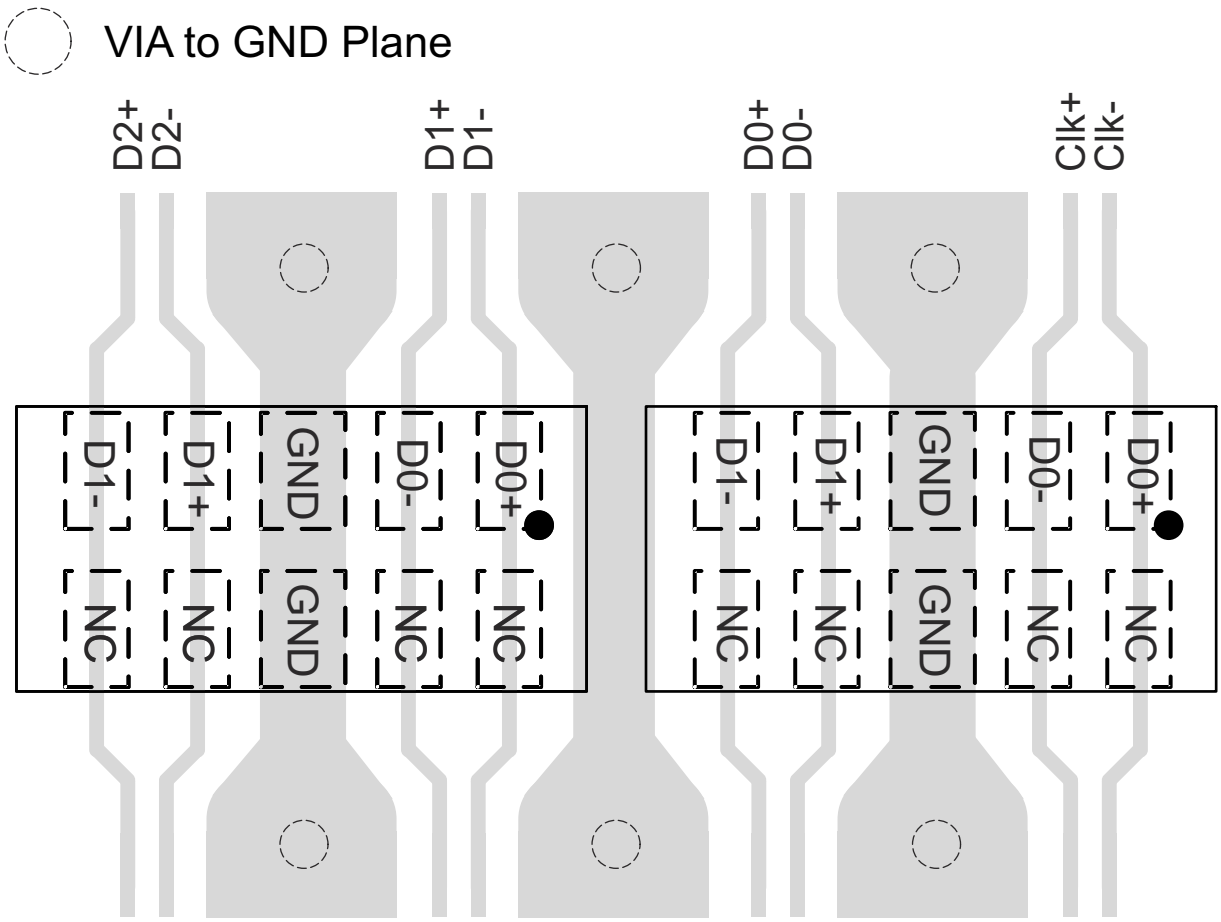


Figure 7-11. TPD4E05U06 Layout

7.4.2.2 TPD1E05U06 Layout Example

This application is typical of an HDMI 2.0 layout.

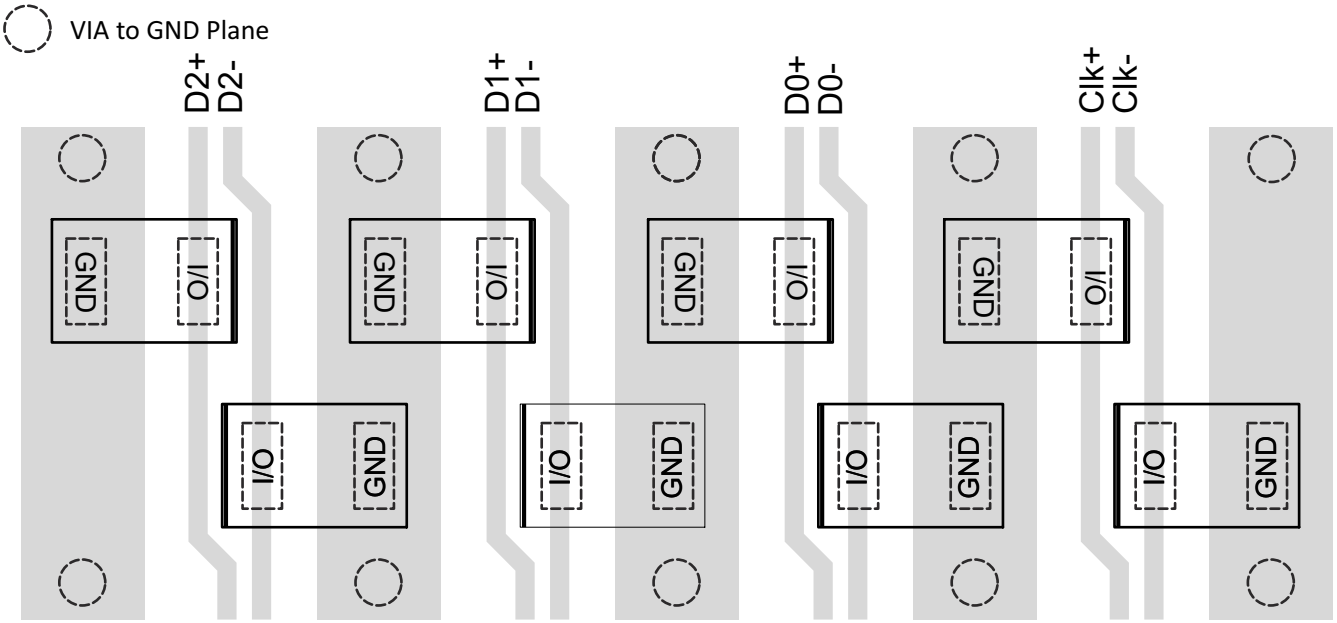


Figure 7-12. TPD1E05U06 Layout

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet
- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *TPD6E05U06RVZ EVM* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *ESD PROTECTION DIODES EVM* user's guide
- Texas Instruments, *TPD1E05U06DPY EVM* user's guide
- Texas Instruments, *TPD4E05U06DQA EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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PCI-express® and PCI-Express® are registered trademarks of PCI-SIG .
V-by-One® is a registered trademark of Thine Electronics, Inc.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (February 2022) to Revision O (August 2024)	Page
• Updated the *Device Information* table	1

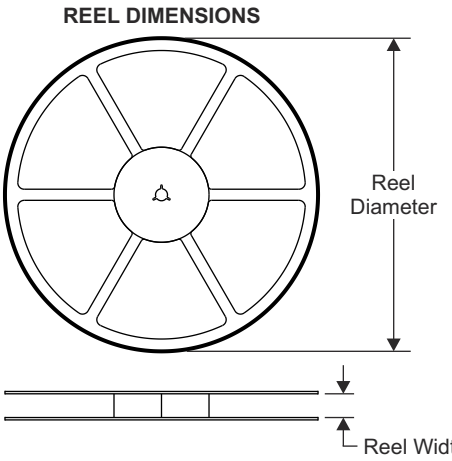
Changes from Revision M (January 2017) to Revision N (February 2022)	Page
• Updated the SOD-523 package information from the body size dimensions (0.8 mm × 1.2 mm) to the lead-to-lead dimensions (1.60 mm × 0.80 mm × 0.65 mm)	1

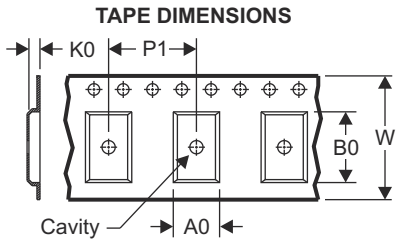
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10 Mechanical, Packaging, and Orderable Information

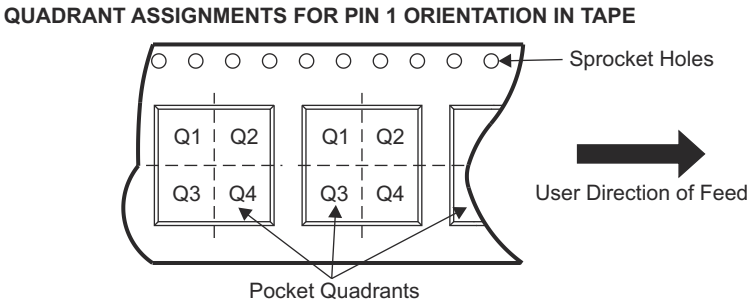
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information





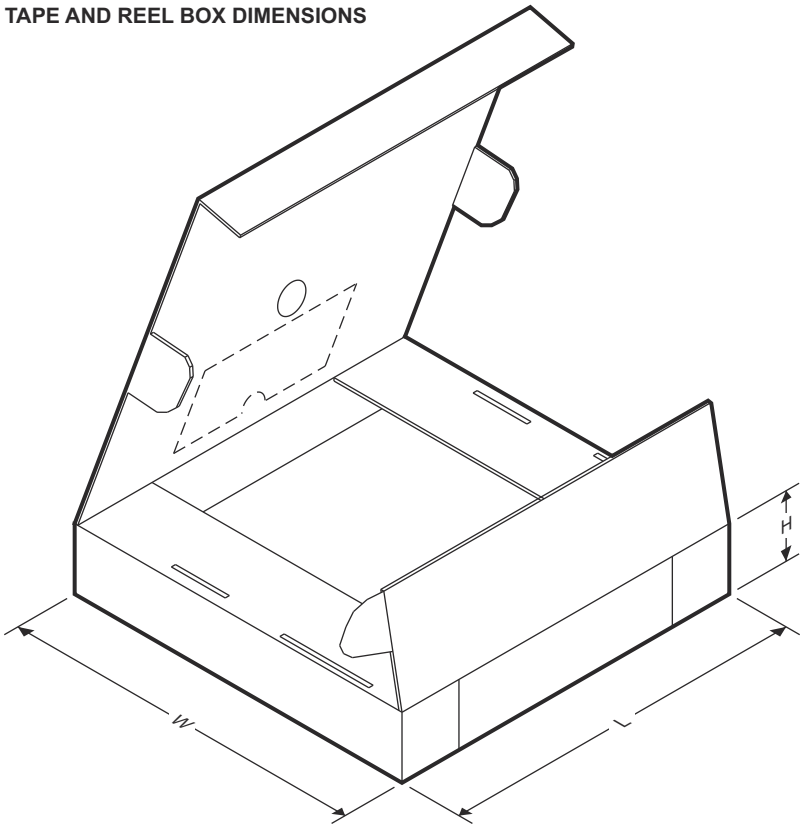
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E05U06DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
TPD1E05U06DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E05U06DYAR	SOT-5X3	DYA	2	3000	178.0	9.5	0.5	1.94	0.73	2.0	8.0	Q1
TPD4E05U06DQAR	USON	DQA	10	3000	180.0	8.4	1.2	2.7	0.63	4.0	8.0	Q1
TPD6E05U06RVZR	USON	RVZ	14	3000	180.0	13.2	1.65	3.8	0.7	4.0	12.0	Q1
TPD6E05U06RVZR	USON	RVZ	14	3000	178.0	13.5	1.6	3.75	0.7	4.0	12.0	Q1

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TAPE AND REEL BOX DIMENSIONS



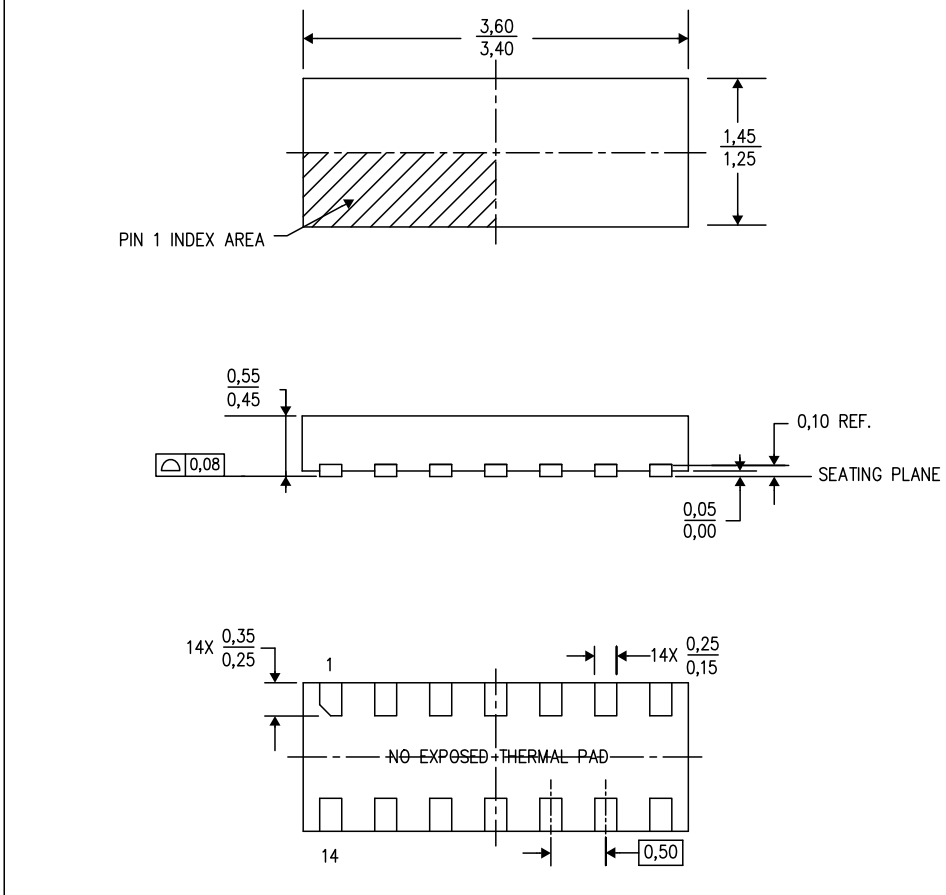
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E05U06DPYR	X1SON	DPY	2	10,000	210.000	185.000	35.000
TPD1E05U06DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E05U06DYAR	SOT-5X3	DYA	2	3000	210.0	200.0	42.0
TPD4E05U06DQAR	USON	DQA	10	3000	210.0	185.0	35.0
TPD6E05U06RVZR	USON	RVZ	14	3000	189.0	185.0	36.0
TPD6E05U06RVZR	USON	RVZ	14	3000	184.0	184.0	19.0

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10.2 Mechanical Data

MECHANICAL DATA

RVZ (R–PUSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



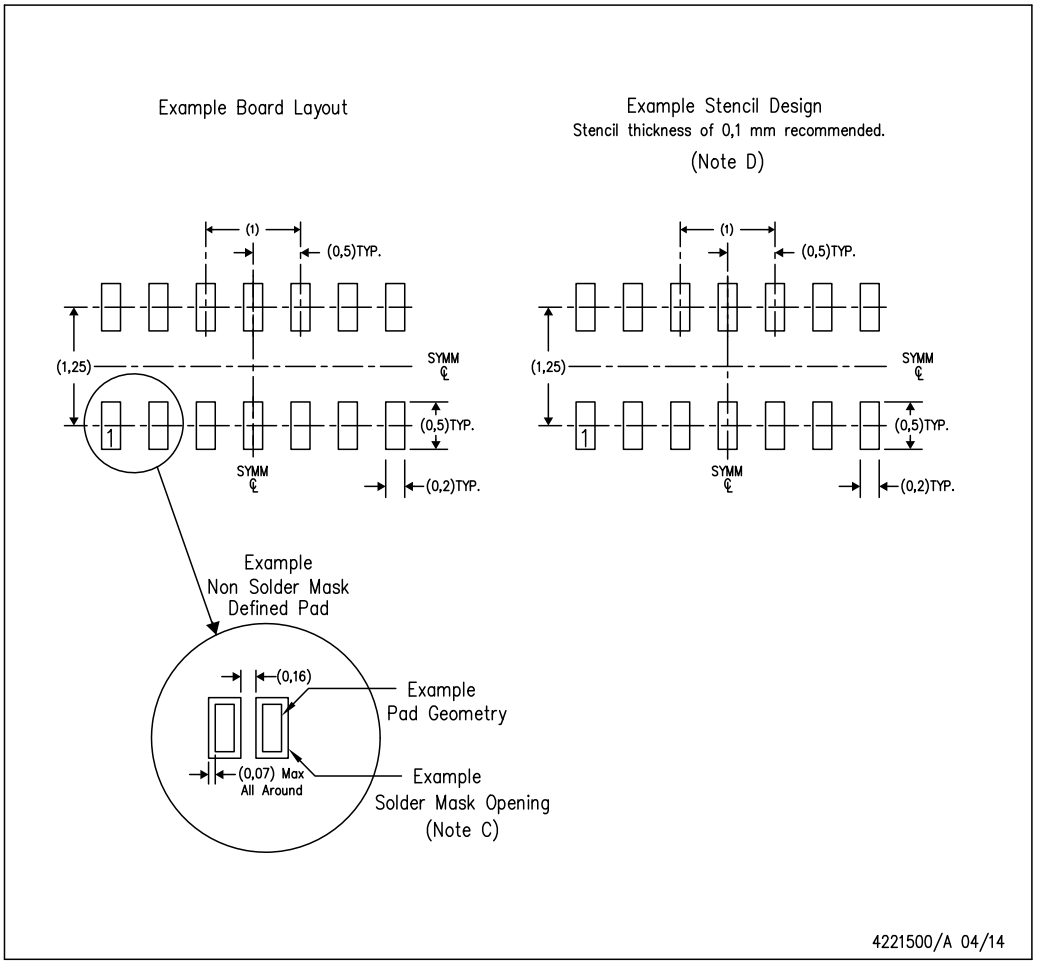
4218112/B 04/14

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

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LAND PATTERN DATA

RVZ (R–PUSON–N14) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

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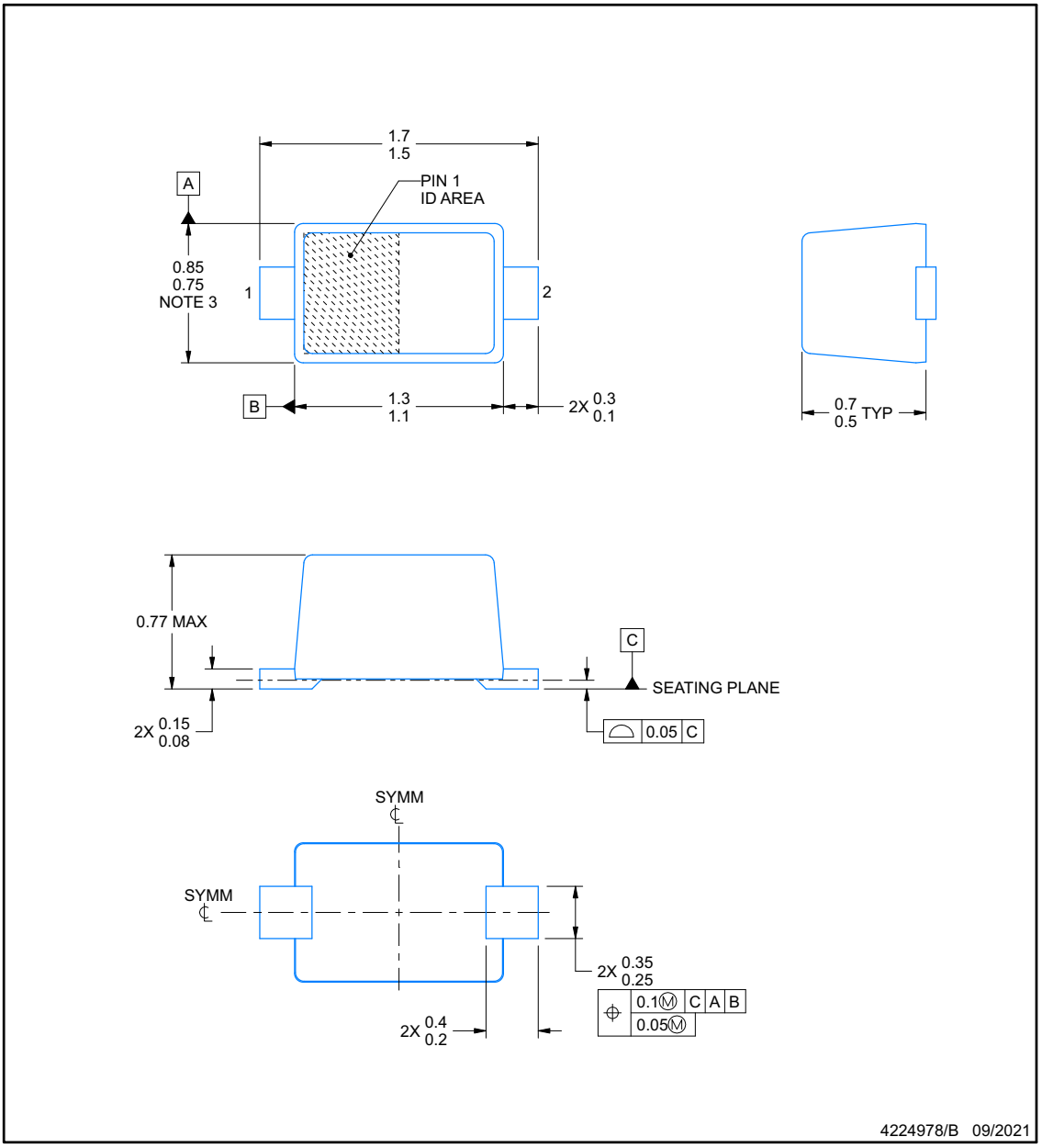


PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height

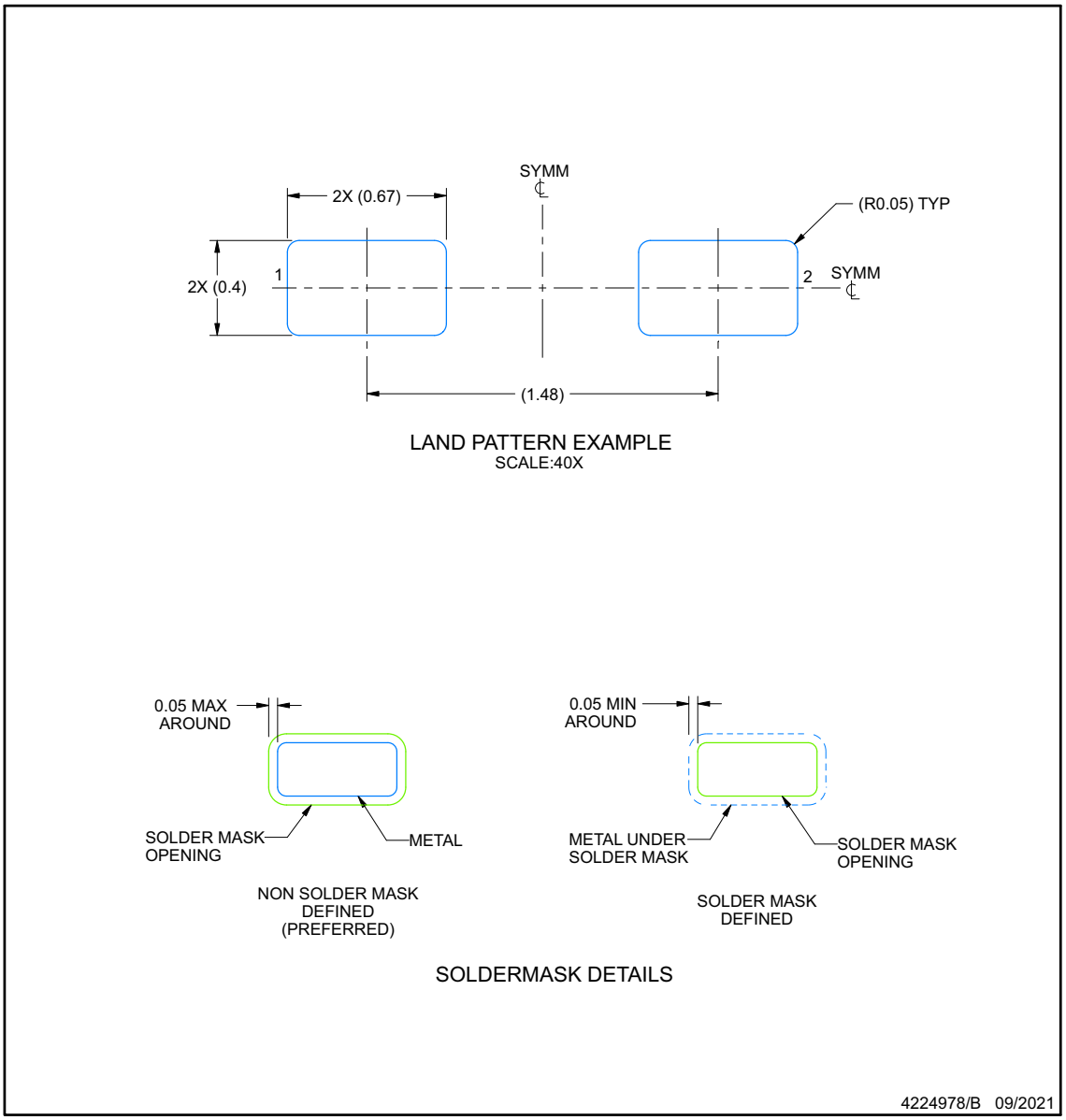
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EXAMPLE BOARD LAYOUT

DYA0002A

SOT (SOD-523) - 0.77 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

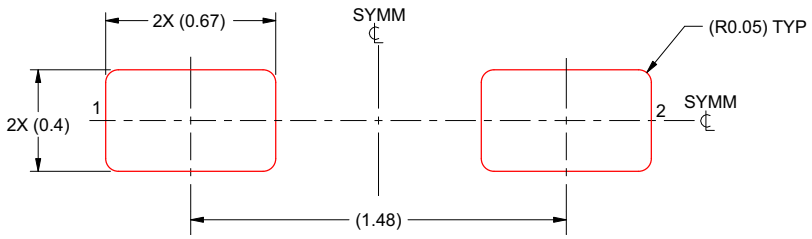
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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EXAMPLE STENCIL DESIGN

DYA0002A — **SOT (SOD-523) - 0.77 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4224978/B 09/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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GENERIC PACKAGE VIEW

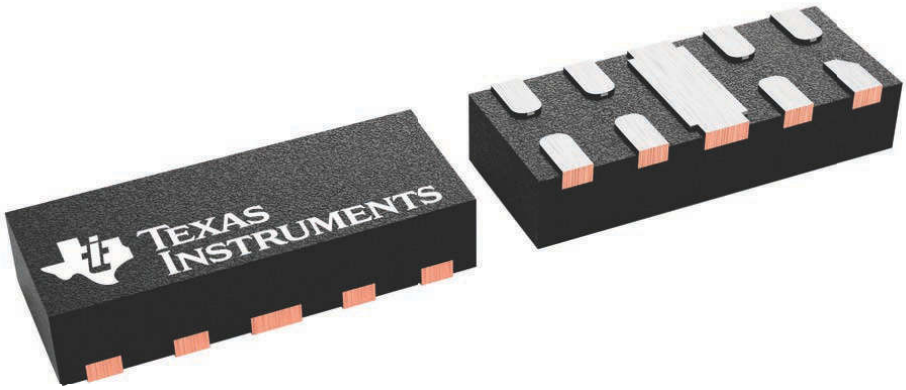
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230320/A

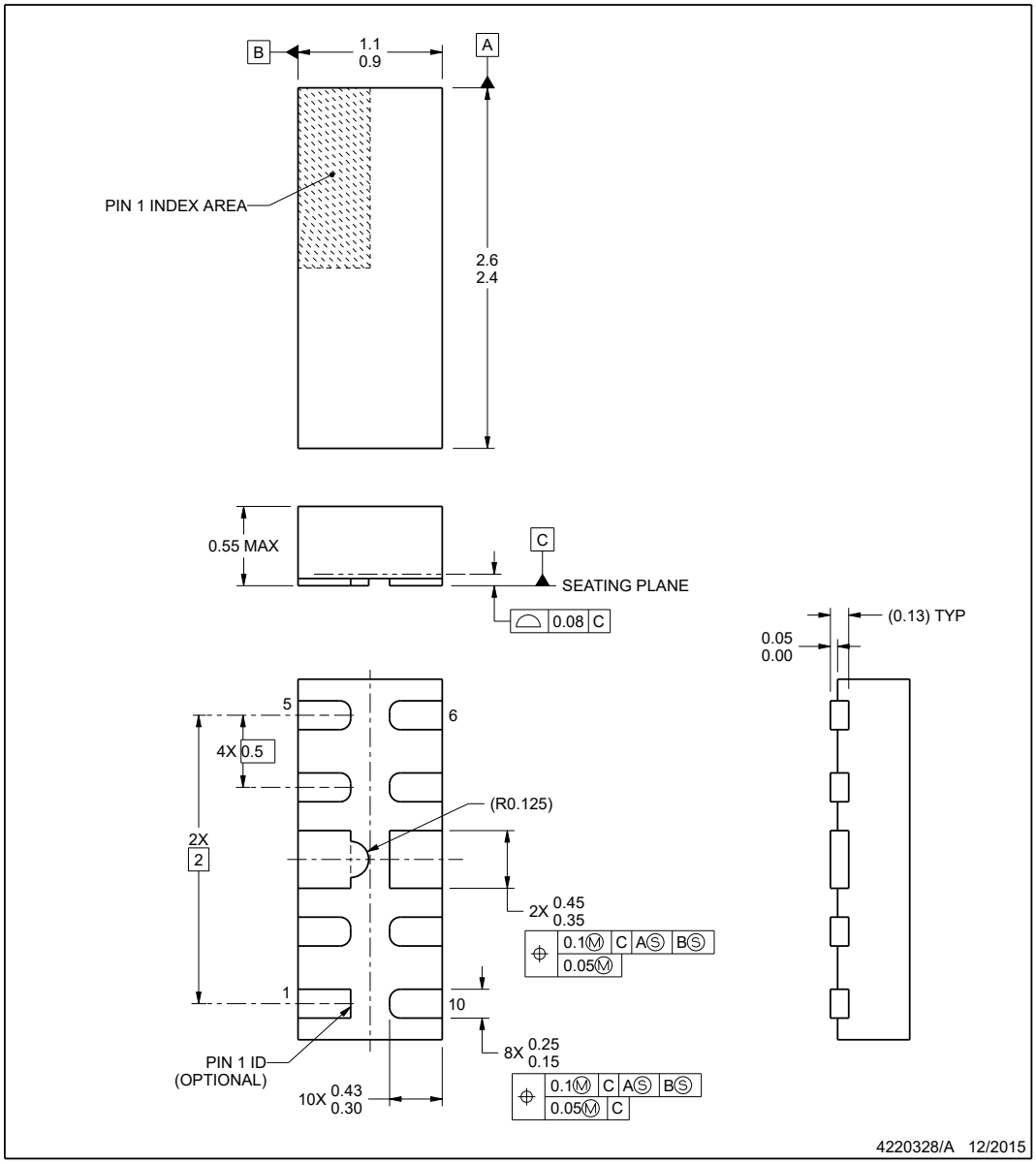
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PACKAGE OUTLINE

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

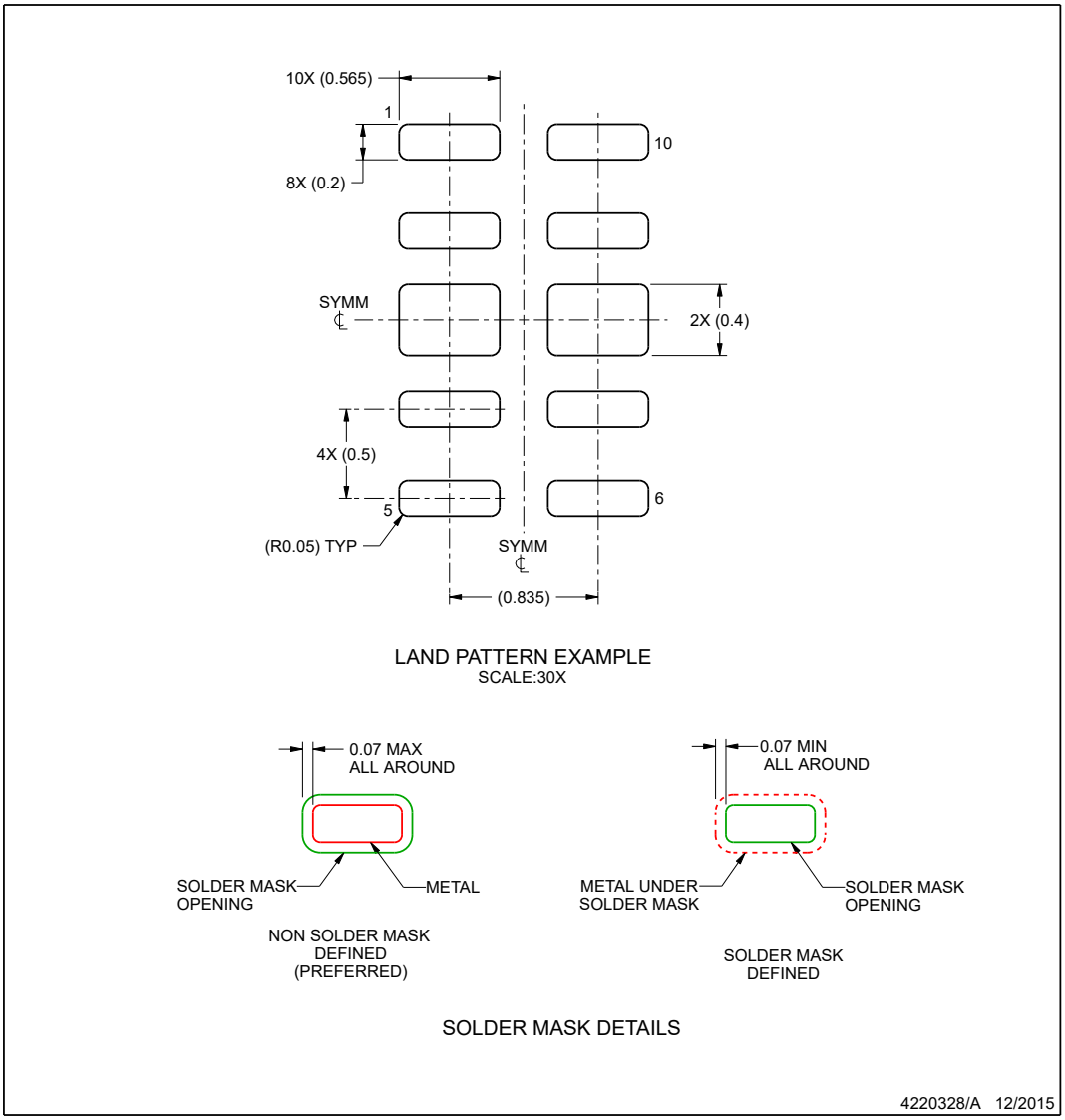
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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EXAMPLE BOARD LAYOUT

DQA0010A — **USON - 0.55 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

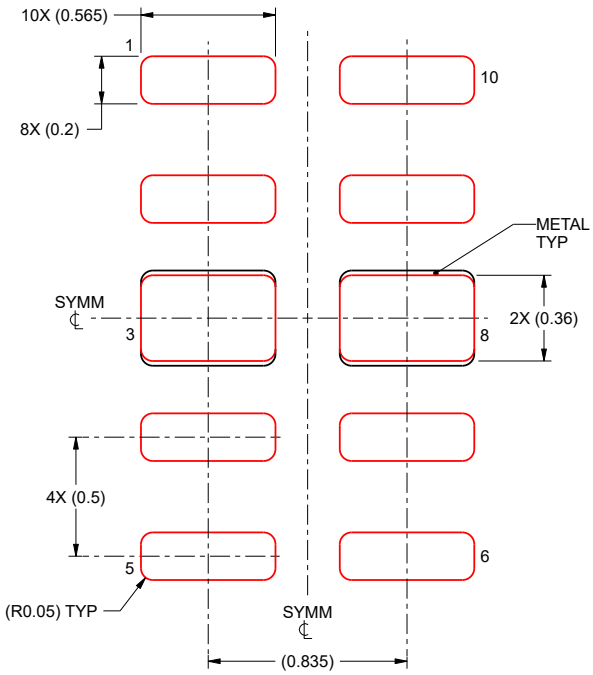
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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EXAMPLE STENCIL DESIGN

DQA0010A **USON - 0.55 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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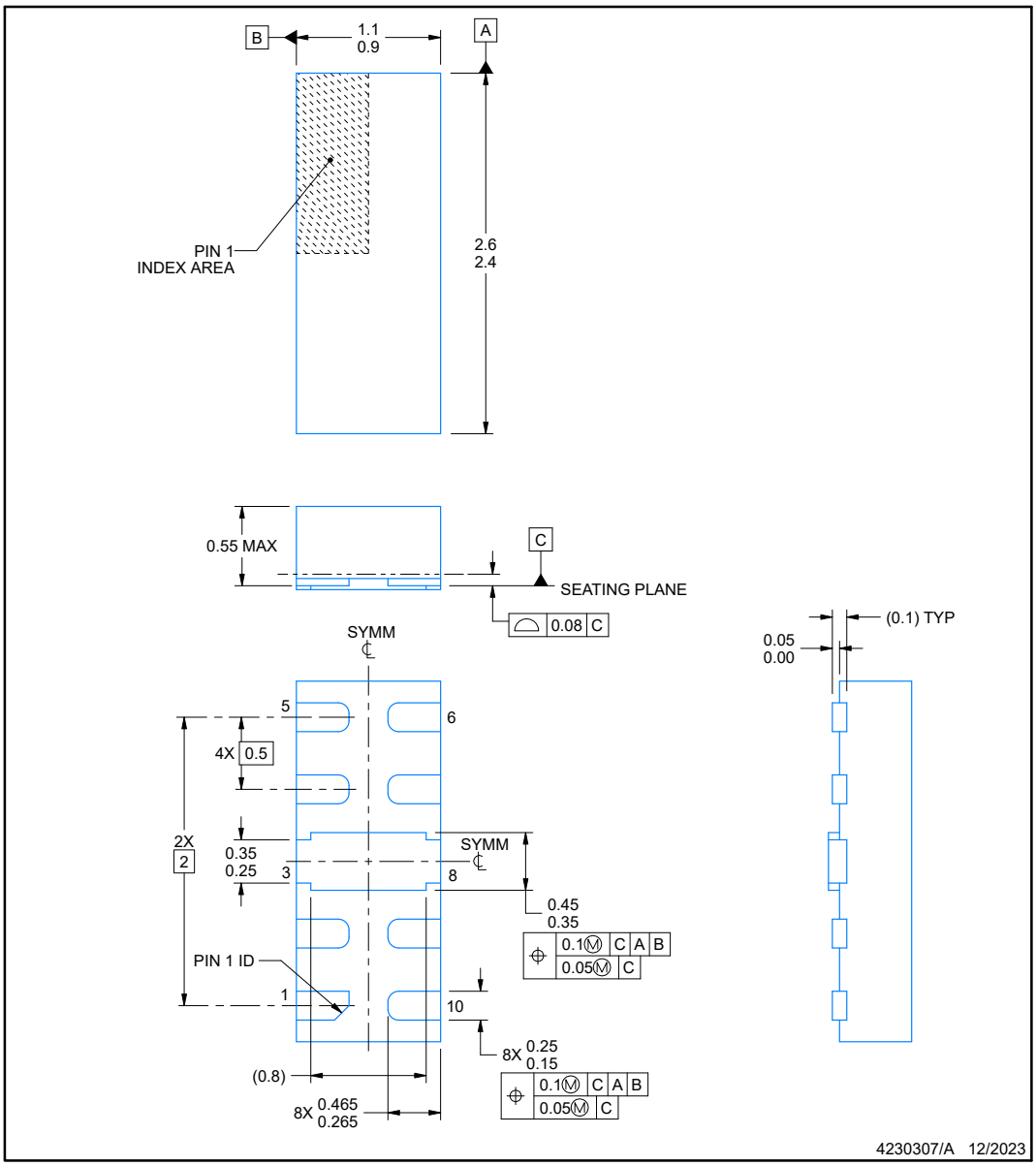
PACKAGE OUTLINE

DQA0010B



USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

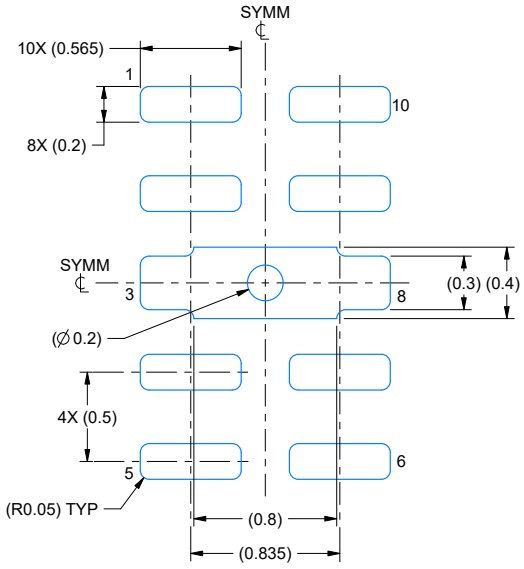
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EXAMPLE BOARD LAYOUT

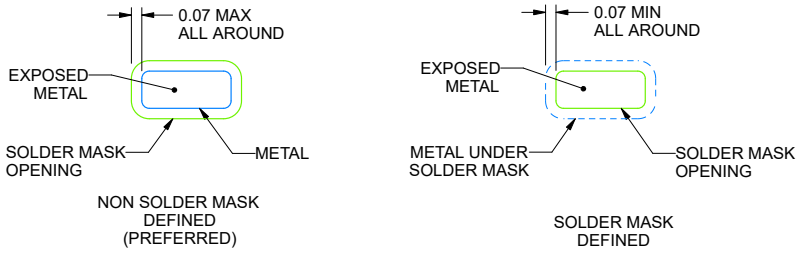
DQA0010B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

4230307/A 12/2023

NOTES: (continued)

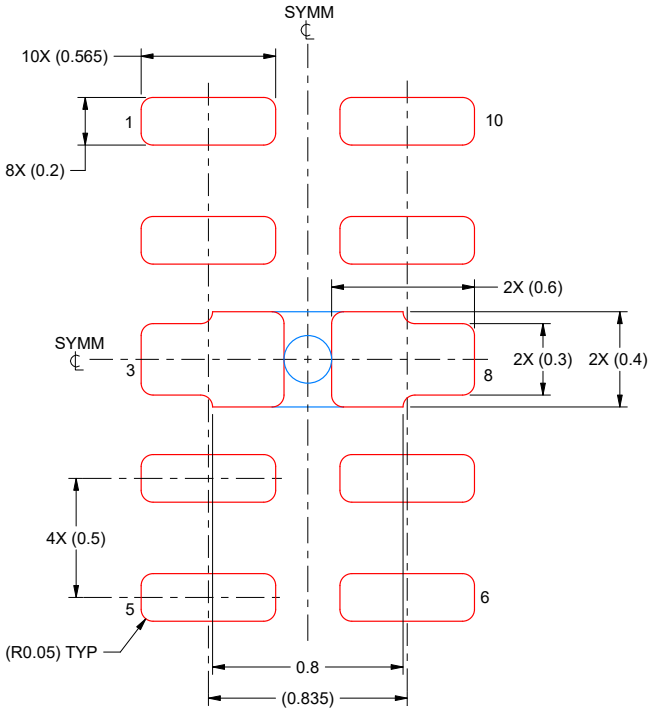
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

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EXAMPLE STENCIL DESIGN

DQA0010B — **USON - 0.55 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4230307/A 12/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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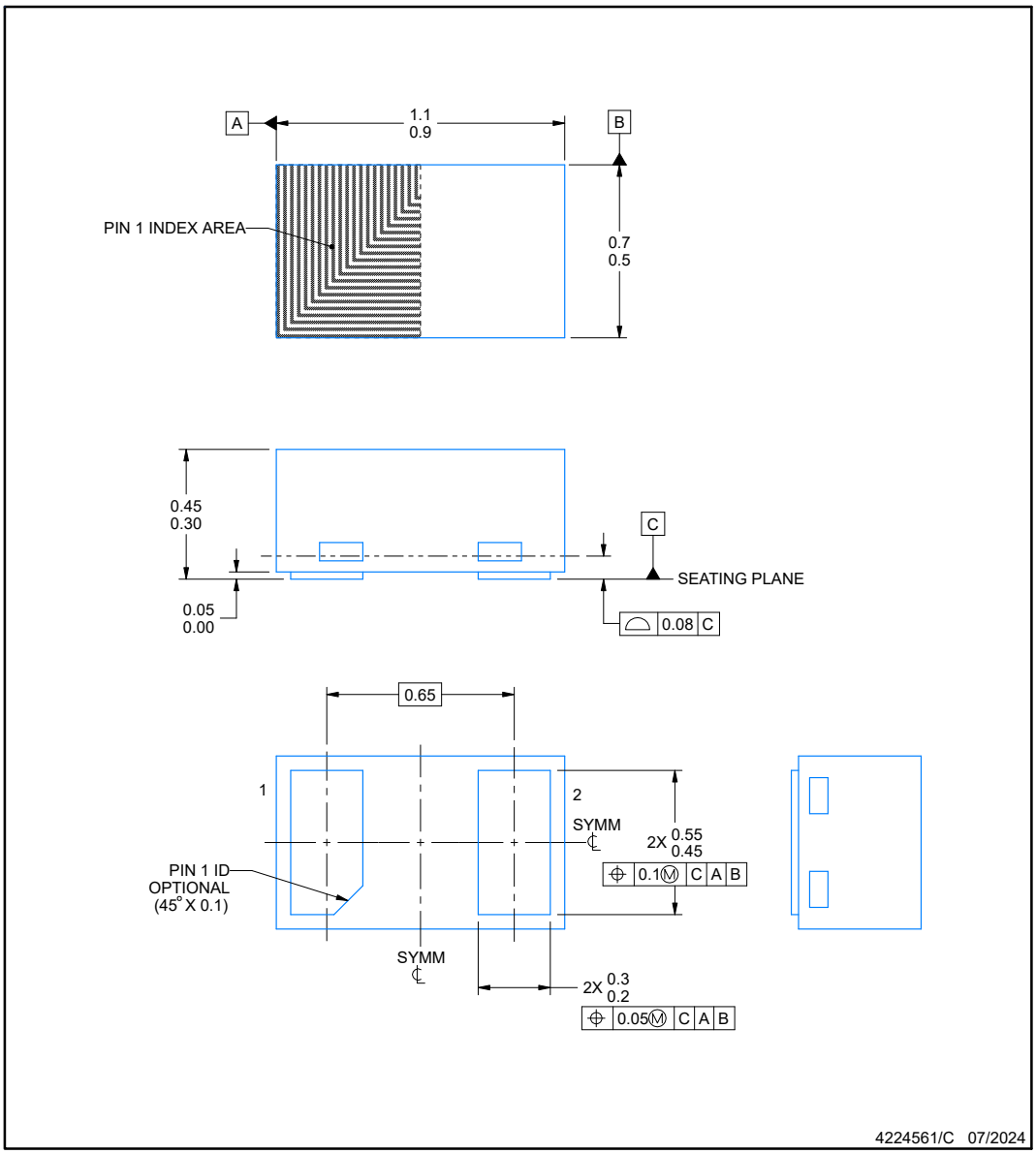
PACKAGE OUTLINE

DPY0002A



X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

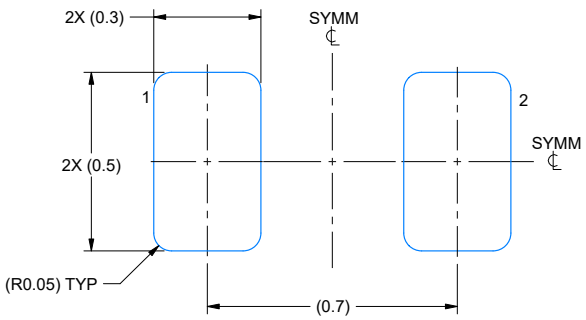
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

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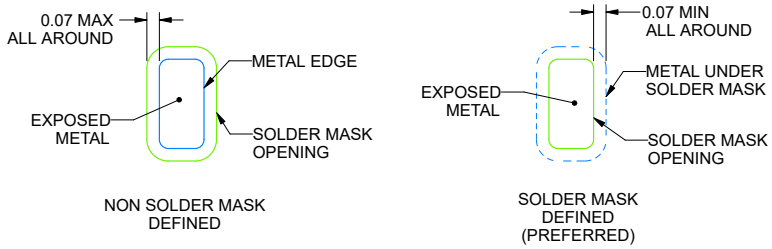
EXAMPLE BOARD LAYOUT

DPY0002A — **X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

4224561/C 07/2024

NOTES: (continued)

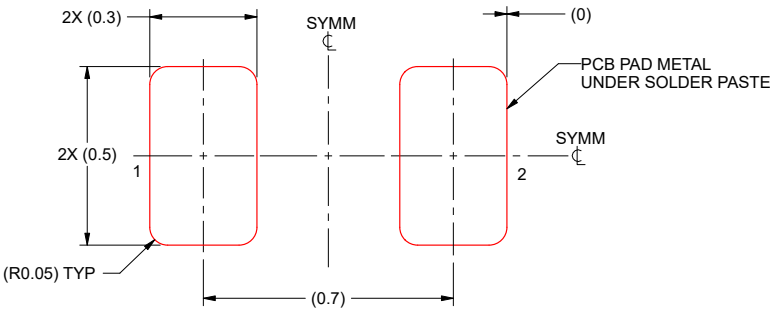
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

DPY0002A — **X1SON - 0.45 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/C 07/2024

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD1E05U06DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(BK, C1, C6) C2
TPD1E05U06DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(BK, C1, C6) C2
TPD1E05U06DPYTG4	Active	Production	X1SON (DPY) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1 C2
TPD1E05U06DPYTG4.B	Active	Production	X1SON (DPY) | 2	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C1 C2
TPD1E05U06DYAR	Active	Production	SOT-5X3 (DYA) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	1KS
TPD1E05U06DYAR.B	Active	Production	SOT-5X3 (DYA) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	1KS
TPD4E05U06DQAR	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BLG, BRG, DQA) BRY
TPD4E05U06DQAR.B	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BLG, BRG, DQA) BRY
TPD4E05U06DQARG4	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQA
TPD4E05U06DQARG4.B	Active	Production	USON (DQA) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DQA
TPD6E05U06RVZR	Active	Production	USON (RVZ) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BV, BVY)
TPD6E05U06RVZR.B	Active	Production	USON (RVZ) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(BV, BVY)
TPD6E05U06RVZRG4	Active	Production	USON (RVZ) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BV
TPD6E05U06RVZRG4.B	Active	Production	USON (RVZ) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPD1E05U06, TPD4E05U06 :

- Automotive : TPD1E05U06-Q1, TPD4E05U06-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

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