TPD2E1B06 Dual-Channel High-Speed ESD Protection Device

1 Features

- Provides System Level ESD Protection for Low Voltage IO Interface
- IEC 61000-4-2 Level 4 ESD Rating
- Low IO Capacitance: 0.85 pF (Typical)
- DC Breakdown Voltage: 7 V (Minimum)
- Ultra-Low Leakage Current: 10 nA (Maximum)
- Low ESD Clamping Voltage
- Temperature Range: –40°C to 125°C
- Small Easy-to-Route DRL package

2 Applications

- Gaming Machines
- eBooks
- Portable Media Players
- Digital Cameras

3 Description

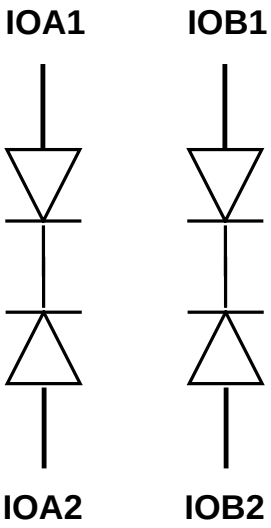
The TPD2E1B06 device is a dual-channel, ultra-low capacitance ESD protection device. It offers ±10-KV IEC contact ESD protection. Its 1-pF line capacitance makes it suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I2C. The TPD2E1B06 device has two common layout methods, and both are highlighted in *Layout*.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD2E1B06	SOT (6)	1.60 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2013) to Revision D **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision B (September 2013) to Revision C **Page**

- Added air gap ESD specification to the ABSOLUTE MAXIMUM RATINGS table. ... 3

Changes from Revision A (August 2013) to Revision B **Page**

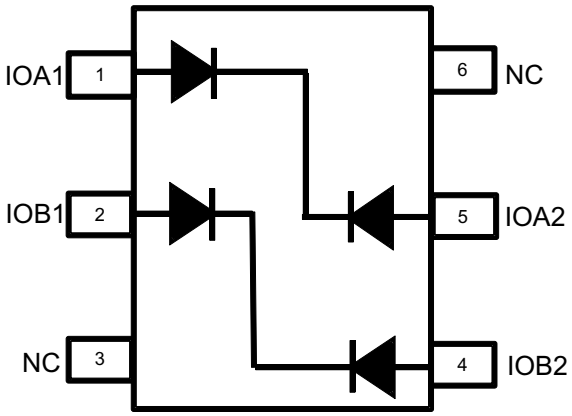
- Added TYPICAL CHARACTERISTICS section. ... 5

Changes from Original (July 2013) to Revision A **Page**

- Revised document from PREVIEW to PRODUCTION DATA. ... 1

5 Pin Configuration and Functions

DRL Package
6-Pin SOT
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	USAGE
NAME	NO.			
IOA1	1	I/O	ESD protected channel	See *Application Information*.
IOA2	5	I/O		
IOB1	2	I/O		
IOB2	4	I/O		
NC	3, 6	NC	No connect	Can be left floating, grounded, or connected to VCC

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Operating temperature	–40	125	°C
I_{PP}	Peak pulse current (tp = 8/20 µs)(2)		2.5	A
P_{PP}	Peak pulse power (tp = 8/20 µs)(2)		35	W
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Using Routing Option 1 or 2 as shown in Figure 13 or Figure 14.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge(1)	±10000	V
		IEC 61000-4-2 air-gap discharge(1)	±15000	

(1) Using Routing Option 1 or 2 as shown in Figure 13 or Figure 14.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Pin IOA1 to IOA2; Pin IOB1 to IOB2	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPD2E1B06 DRL (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	349.7	ºC/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	120.5	ºC/W
$R\theta_{\theta JB}$	Junction-to-board thermal resistance	171.4	ºC/W
ψ_{JT}	Junction-to-top characterization parameter	10.8	ºC/W
ψ_{JB}	Junction-to-board characterization parameter	169.4	ºC/W

(1) For more information about traditional and new thermal metrics, the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range. (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse standoff voltage				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, I/O to GND(1)(2)		11		V
		I_{PP} = 5 A, TLP, I/O to GND(1)(2)		15		
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, GND to I/O (1)(2)		11		V
		I_{PP} = 5 A, TLP, GND to I/O (1)(2)		15		
R_{DYN}	Dynamic resistance			0.9		Ω
C_{L1}	Pin 2 and 5 capacitance	Pin 1 and 4 = GND, f = 1 MHz, V_{BIAS} = 2.5 V(2)(3)		0.85		pF
C_{L2}	Pin 1 and 4 capacitance	Pin 2 and 5 = GND, f = 1 MHz, V_{BIAS} = 2.5 V(2)(4)		1.05		pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	7		9.5	V
I_{LEAK}	Leakage current	V_{BIAS} = +2.5 V		1	10	nA

(1) Transmission line pulse with rise time 10 ns and pulse width 100 ns.
(2) T_A = 25°C
(3) Using Routing Option 1, Figure 13.
(4) Using Routing Option 2, Figure 14.

6.6 Typical Characteristics

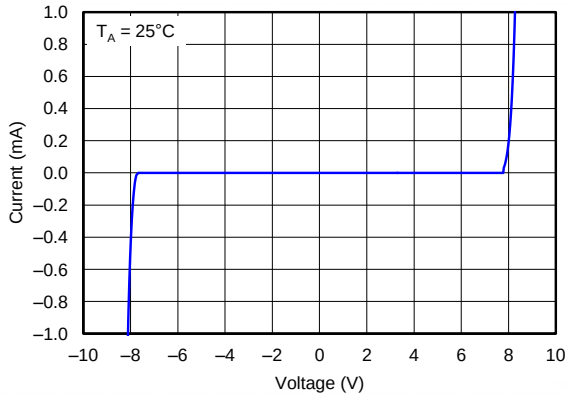


Figure 1. I_V Curve

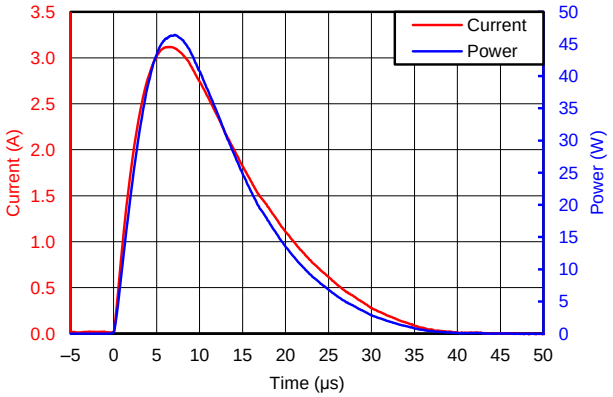


Figure 2. Maximum Surge Rating

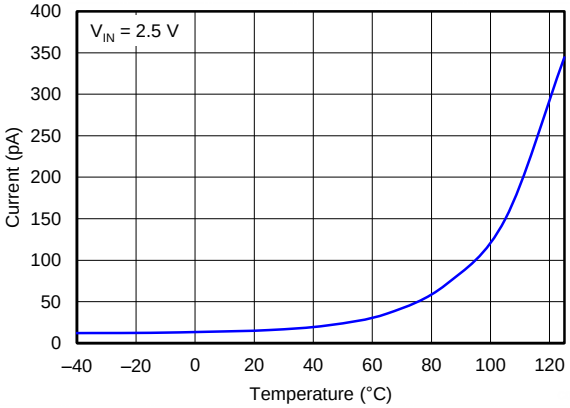


Figure 3. I_{LEAK} vs Temperature

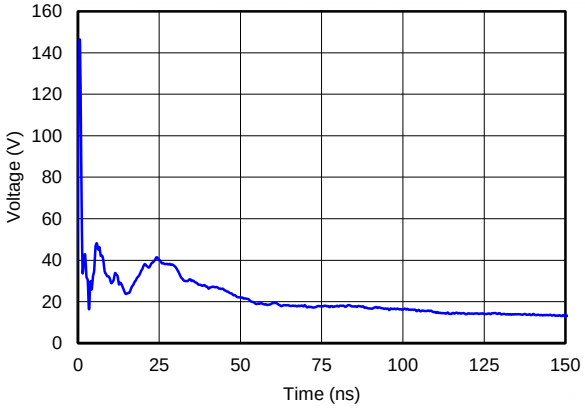


Figure 4. +8-kV Contact ESD Clamping

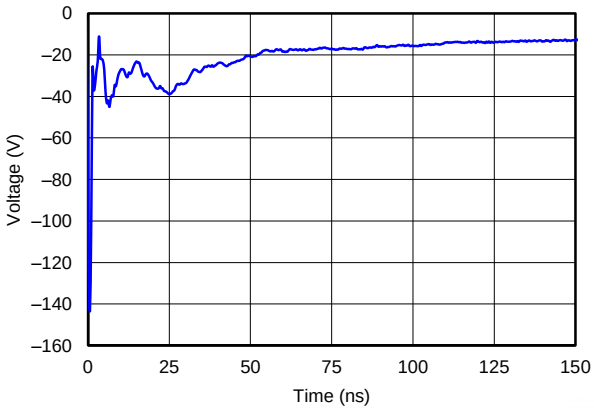


Figure 5. –8-kV Contact ESD Clamping

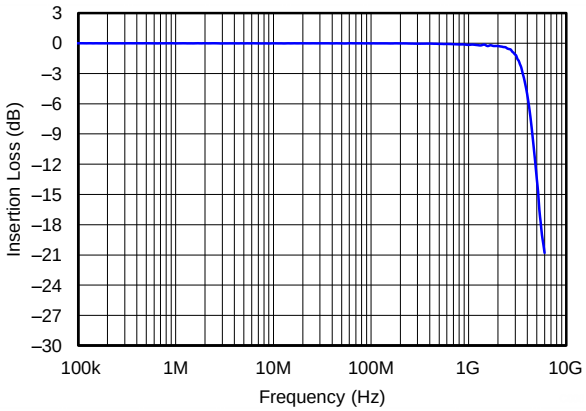


Figure 6. Insertion Loss

Typical Characteristics (continued)

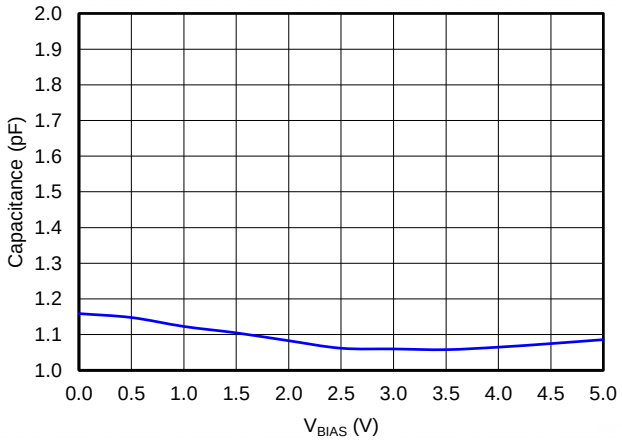


Figure 7. Capacitance vs V_{BIAS}

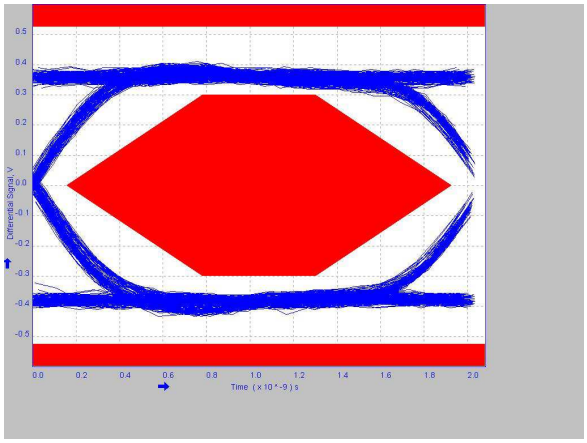


Figure 8. Eye Diagram Without TPD2E1B06DRL on EVM

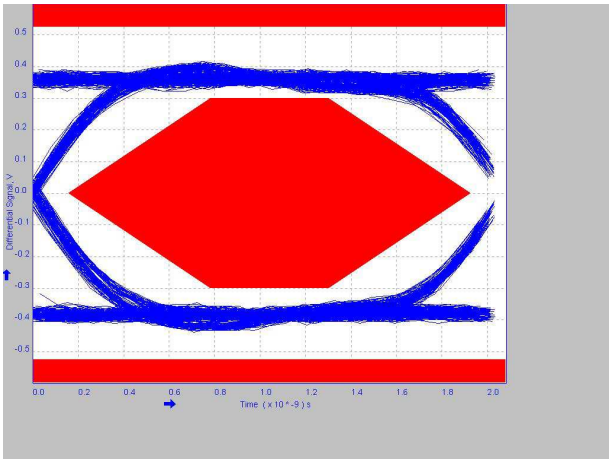


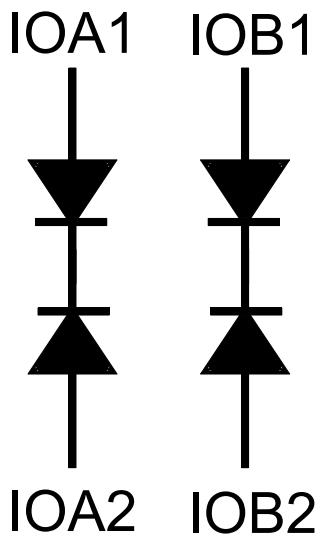
Figure 9. Eye Diagram With TPD2E1B06DRL on EVM

7 Detailed Description

7.1 Overview

The TPD2E1B06 is a bidirectional, low-capacitance, two-channel ESD clamping device. It has more than IEC 61000-4-2 Level 4 ESD Rating. The low IO capacitance makes the device a good fit for a wide range of data speeds. Common applications include USB 2.0, LVDS, and I2C.

7.2 Functional Block Diagram



7.3 Feature Description

The TPD2E1B06 device provides robust system level IEC protection. This device protects circuit from ESD strikes up to ±10-kV contact and ±15-kV air-gap specified in the IEC 61000-4-2 level 4. It also handles up to 2.5-A surge current (IEC61000-4-5 8/20 µs). The I/O capacitance of 0.85 pF supports high data rates. The device has a small dynamic resistance of 0.9 Ω, making clamping voltage low when the device is actively protecting other circuits. With low capacitance and dynamic resistance, the TPD2E1B06 is a good fit for interfaces like USB 2.0, LVDS, and I2C. The breakdown is bidirectional so that this protection device is especially good for bidirectional signals like audio lines. Low leakage allows the diode to conserve power when working below the V_{RWM}. The temperature range of –40°C to 125°C makes this ESD device work at extensive temperatures in most environments.

7.4 Device Functional Modes

The TPD2E1B06 is a passive clamp that has low leakage during normal operation when the voltage across each channel is below V_{RWM} and activates when the it goes above V_{BR}. During IEC ESD events, transient voltages will be clamped. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low-leakage passive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface connector, the system becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. There are 2 channels of back-to-back diodes in TPD2E1B06. The device is typically used to provide a path to ground for dissipating ESD events between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

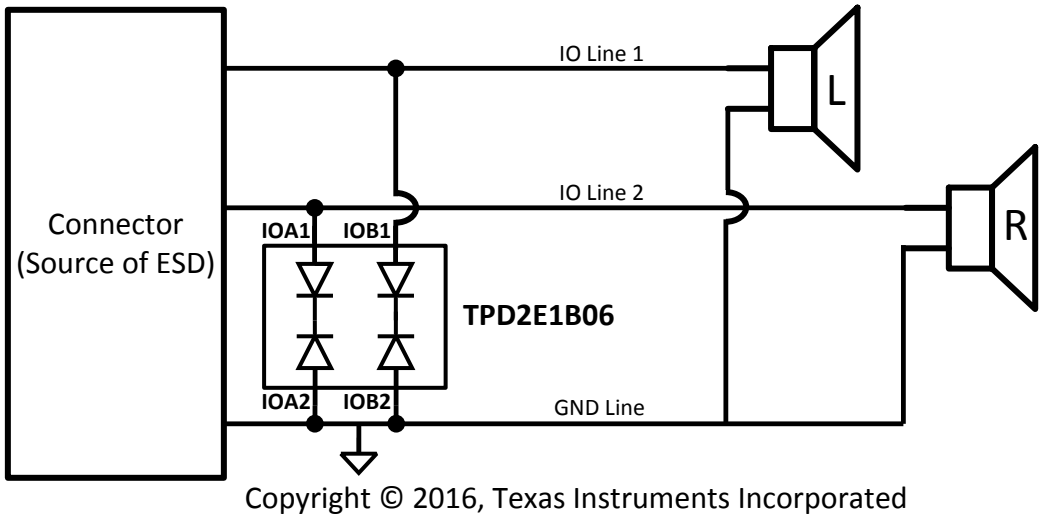


Figure 10. Typical Application Schematic

8.2.1 Design Requirements

In this design example, a TPD2E1B06 is used to protect audio channels. Table 1 lists the system parameters.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Audio Amplifier Class	AB
Audio signal voltage range	–3 V to 3 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD Protection	±8-kV Contact/ ±15-kV Air-Gap

8.2.2 Detailed Design Procedure

For some parameters, the designer must ensure the following before designing:

- Voltage range on the protected line must not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM})
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode

- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode

For this application, the audio signal voltage range is –3 V to 3 V. The V_{RWM} for the TVS is –5.5 V to 5.5 V; therefore, the bidirectional TVS will not break down during normal operation.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz; ensure that the TVS I/O capacitance will not distort this signal by filtering it. With TPD2E1B06 typical capacitance of 0.85 pF, which leads to a typical 3-dB bandwidth of more than 3 GHz, this diode has way sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires above standard Level 4 IEC 61000-4-2 system-level ESD protection (±8-kV Contact and ±15-kV Air-Gap). TPD2E1B06 can survive at least ±10-kV Contact and ±15-kV Air-Gap. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide the full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, a system designer must use proper board layout of their TVS ESD protection diodes. See *Layout* for instructions on properly laying out the TPD2E1B06.

8.2.3 Application Curves

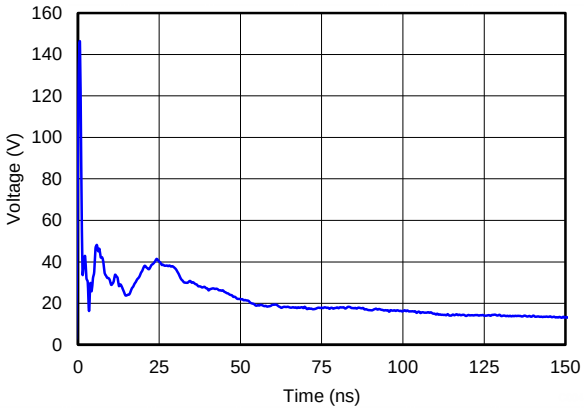


Figure 11. +8-kV Contact ESD Clamping

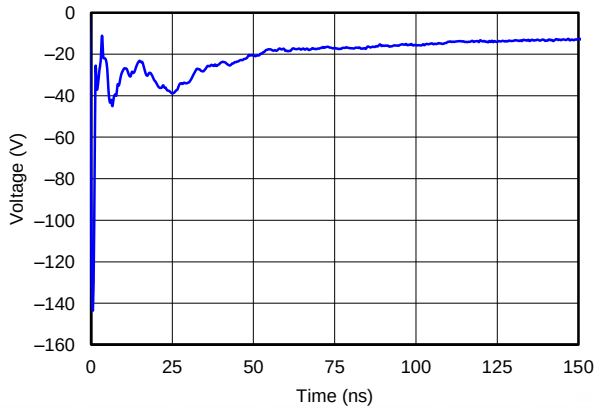


Figure 12. –8-kV Contact ESD Clamping

9 Power Supply Recommendations

This TPD2E1B06 is a passive TVS diode-based ESD protection device so it does not have any power requirements. Take care not to violate the maximum voltage specifications for each pin.

10 Layout

10.1 Layout Guidelines

• The optimum placement of the TPD2E1B06 is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The printed-circuit board (PCB) designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces, which are between the TVS and the connector.

• Route the protected traces as straight as possible.

• Avoid sharp corners on the protected traces. Electric fields tend to build up on corners, increasing EMI coupling.

• Use thick and short traces for the ground pins

10.2 Layout Examples

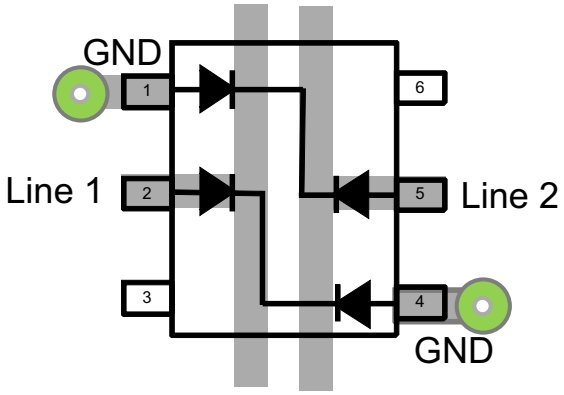


Figure 13. Routing Option 1

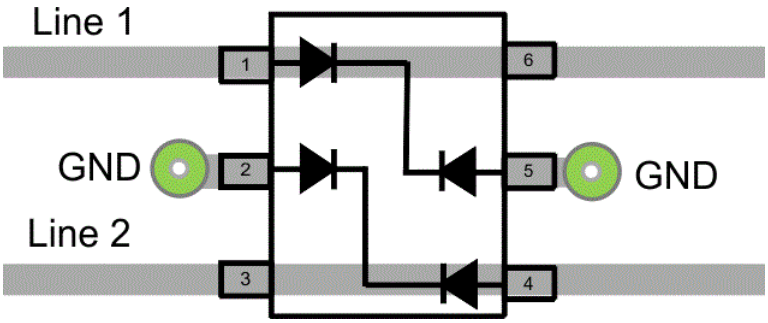


Figure 14. Routing Option 2

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E1B06DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(DUH, DUL) DUG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

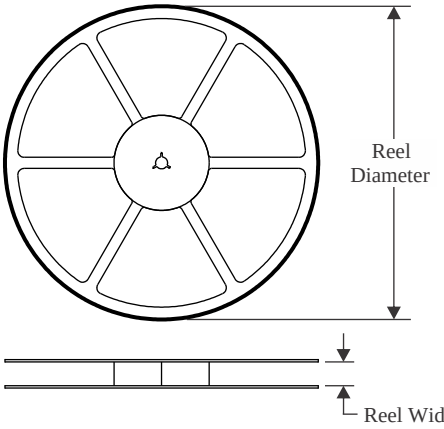
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

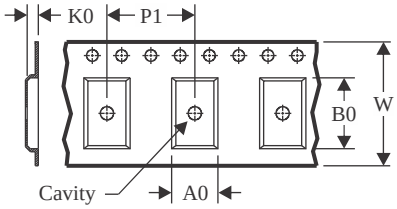
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

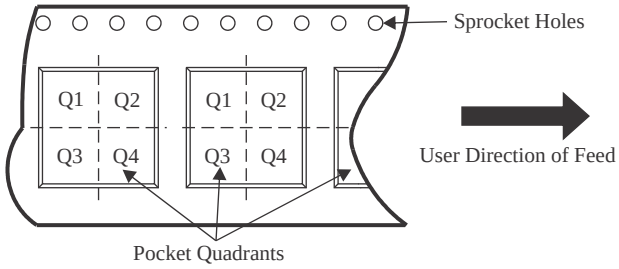


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

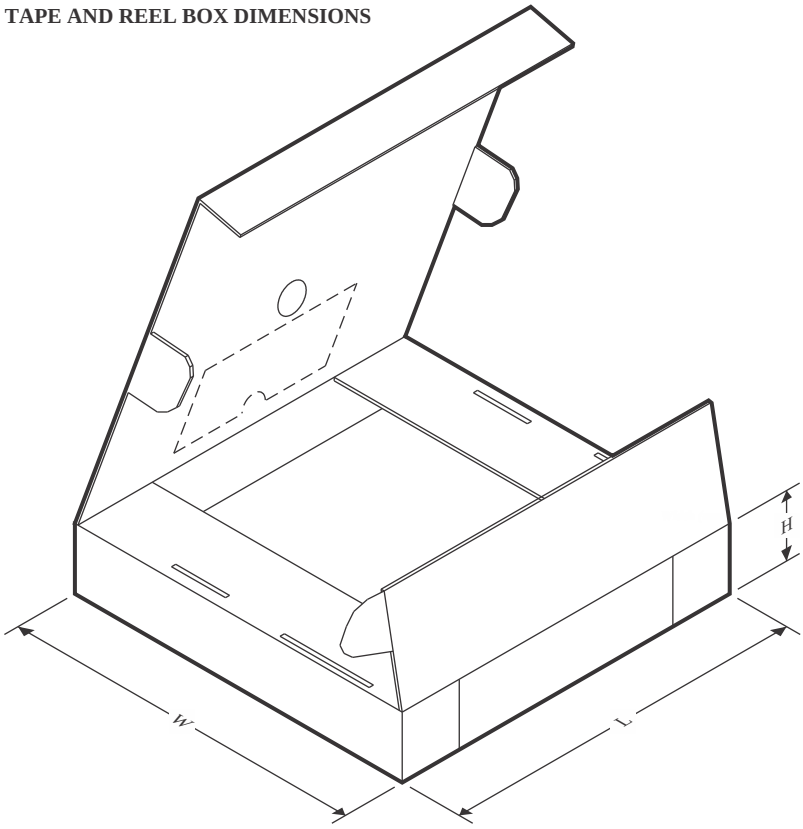
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

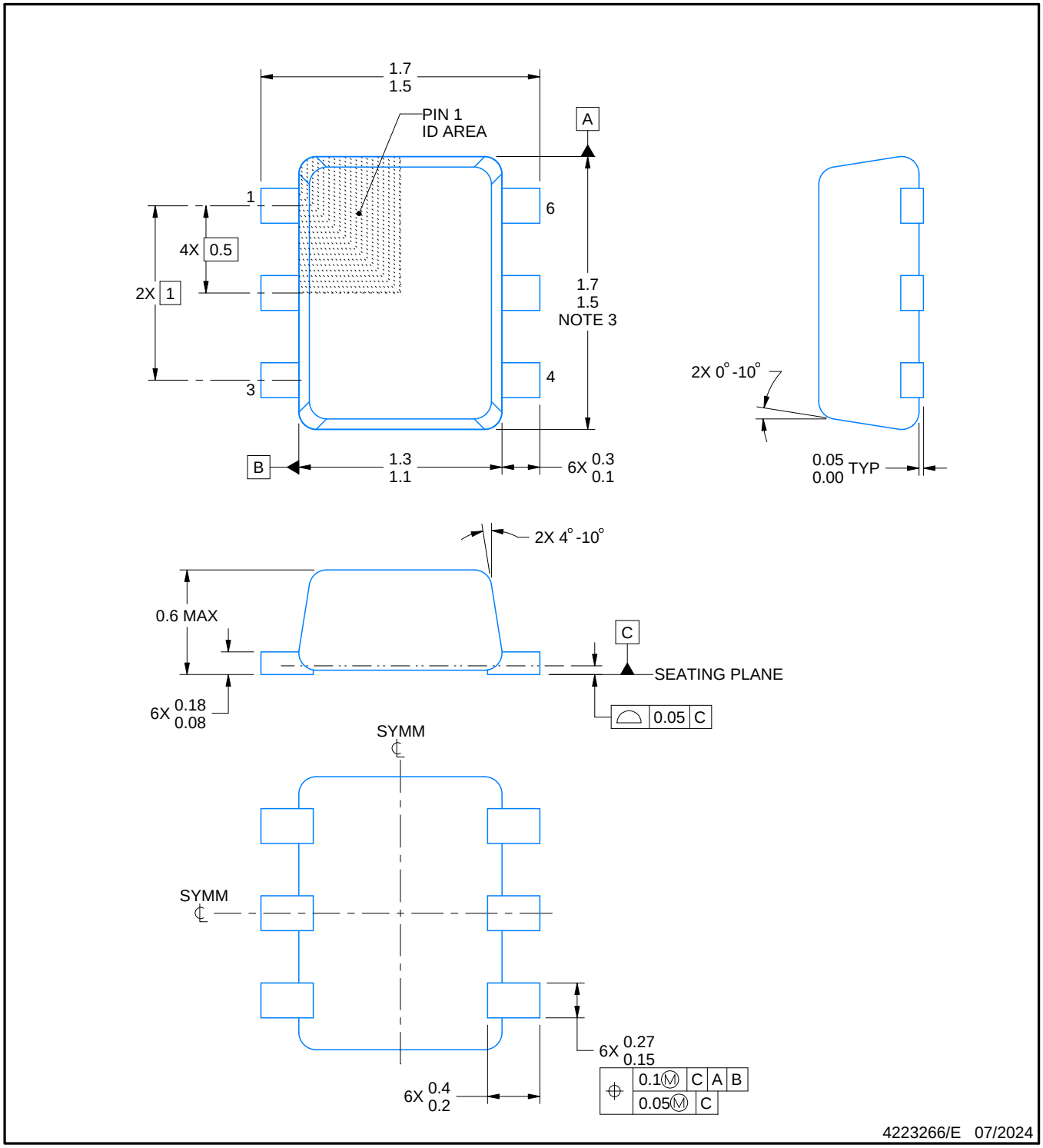
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	183.0	183.0	20.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

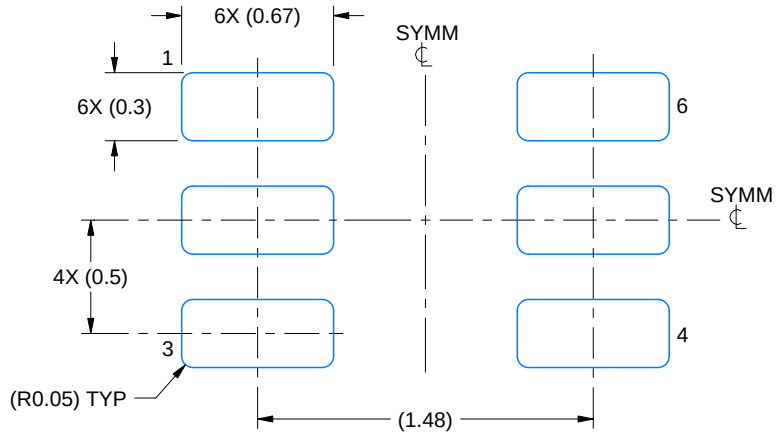
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

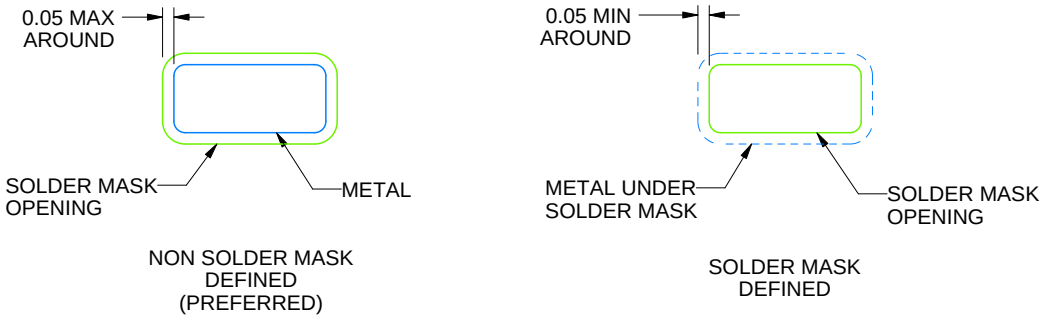
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X

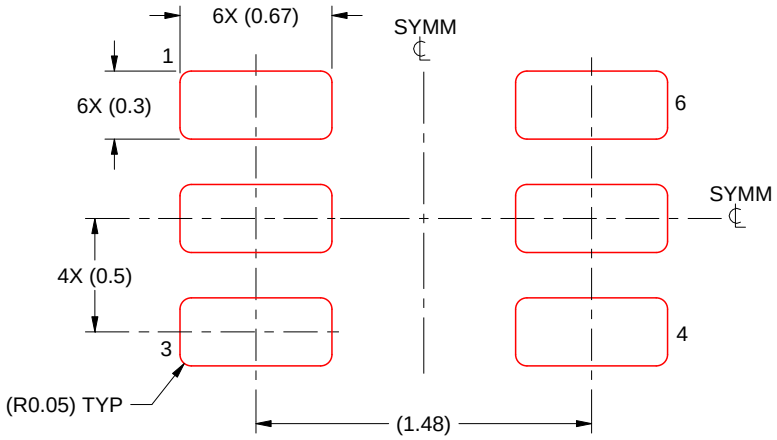


SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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