



TPD4E02B04 4-Channel ESD Protection Diode for USB Type-C and HDMI 2.0

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
 - ± 12 -kV Contact Discharge
 - ± 15 -kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
 - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
 - 2 A (8/20 μ s)
- IO Capacitance:
 - 0.25 pF (Typical)
 - 0.33 pF (Maximum)
- DC Breakdown Voltage: 5.5 V (Minimum)
- Ultra Low Leakage Current: 10 nA (Maximum)
- Low ESD Clamping Voltage: 8.8 V at 5-A TLP
- Supports High Speed Interfaces up to 10 Gbps
- Industrial Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Easy Flow-Through Routing Package

2 Applications

- End Equipment
 - Laptops and Desktops
 - Set-Top Boxes
 - TV and Monitors
 - Mobile and Tablets
 - DVR and NVR

• Interfaces

- USB Type-C
- USB 3.1 Gen 2
- HDMI 2.0/1.4
- USB 3.0
- DisplayPort 1.3
- PCI Express 3.0

3 Description

The TPD4E02B04 is a bidirectional TVS ESD protection diode array for USB Type-C and HDMI 2.0 circuit protection. The TPD4E02B04 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

This device features a 0.25-pF IO capacitance per channel making it ideal for protecting high-speed interfaces up to 10 Gbps such as USB 3.1 Gen2. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

The TPD4E02B04 is offered in the industry standard USON-10 (DQA) package. The package features flow-through routing and 0.5-mm pin pitch easing implementation and reducing design time.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E02B04	USON (10)	2.50 mm x 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

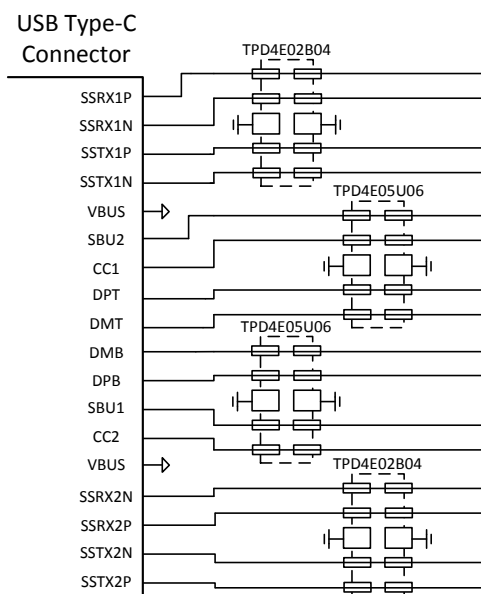


Table of Contents

1 Features	1	7.4 Device Functional Modes.....	11
2 Applications	1	8 Application and Implementation	12
3 Description	1	8.1 Application Information.....	12
4 Revision History	2	8.2 Typical Application	12
5 Pin Configuration and Functions	3	9 Power Supply Recommendations	15
6 Specifications	4	10 Layout	15
6.1 Absolute Maximum Ratings	4	10.1 Layout Guidelines	15
6.2 ESD Ratings.....	4	10.2 Layout Examples.....	15
6.3 ESD Ratings—IEC Specification	4	11 Device and Documentation Support	17
6.4 Recommended Operating Conditions	4	11.1 Documentation Support	17
6.5 Thermal Information	4	11.2 Receiving Notification of Documentation Updates	17
6.6 Electrical Characteristics.....	5	11.3 Community Resources.....	17
6.7 Typical Characteristics	6	11.4 Trademarks	17
7 Detailed Description	10	11.5 Electrostatic Discharge Caution.....	17
7.1 Overview	10	11.6 Glossary	17
7.2 Functional Block Diagram	10	12 Mechanical, Packaging, and Orderable Information	17
7.3 Feature Description.....	10		

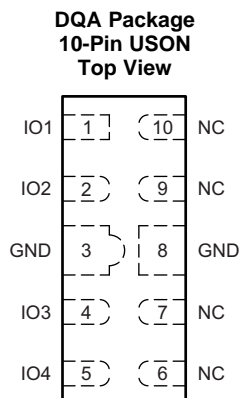
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2016) to Revision B	Page
• Updated Capacitance spec in the <i>Features</i> , <i>Description</i> , , <i>IO Capacitance</i> and <i>Operating Frequency</i> sections	1
• Made changes to <i>Operating Frequency</i>	1
• Updated <i>Figure 15</i> , <i>Figure 16</i> , <i>Figure 22</i> and <i>Figure 23</i>	1

Changes from Original (November 2015) to Revision A	Page
• Changed device status from <i>Product Preview</i> to <i>Production Data</i>	1

5 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground
GND	8		
IO1	1	I/O	ESD protected channel
IO2	2		
IO3	4		
IO4	5		
NC	6	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	7		
NC	9		
NC	10		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 μ s)		17	W
	IEC 61000-4-5 Current (t_p - 8/20 μ s)		2	A
T_A	Operating free-air temperature	-40	125	°C
T_{stg}	Storage temperature	-65	155	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	
		± 2500	
		± 1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	V
		IEC 61000-4-2 air-gap discharge	
		± 12000	
		± 15000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	-3.6	3.6	V
T_A	Operating free-air temperature	-40	125	°C

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD4E02B04	UNIT
		DQA (USON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	348.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	214.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	270.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	81.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	270.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

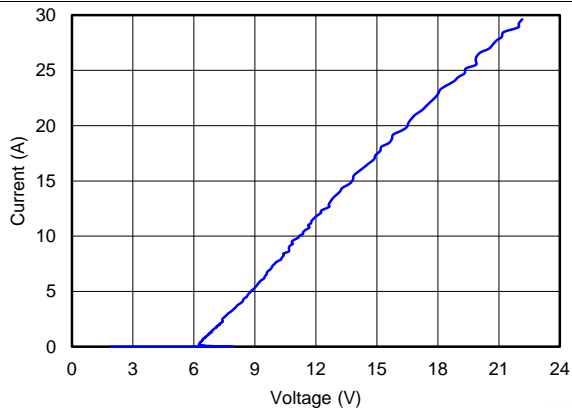
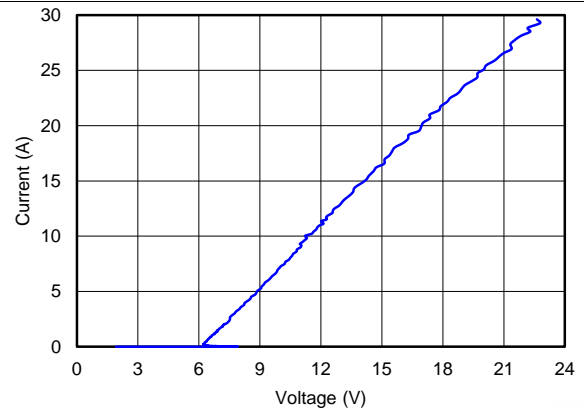
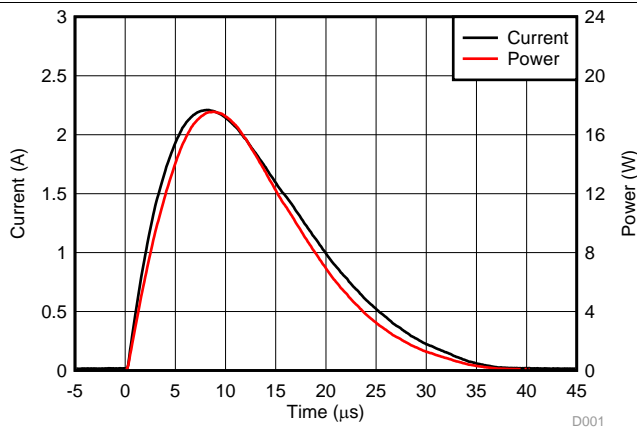
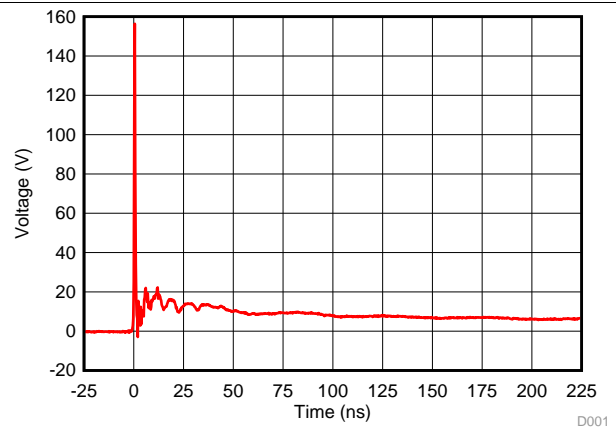
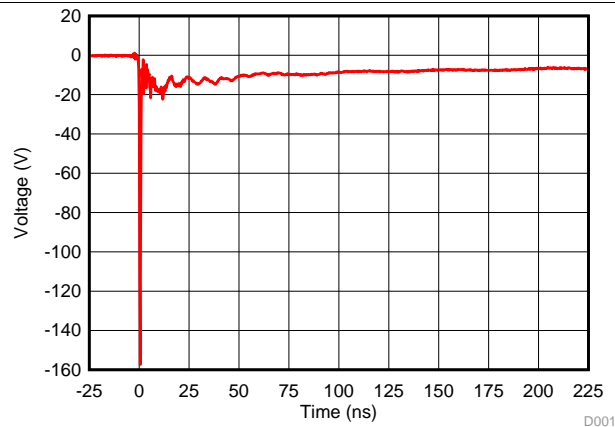
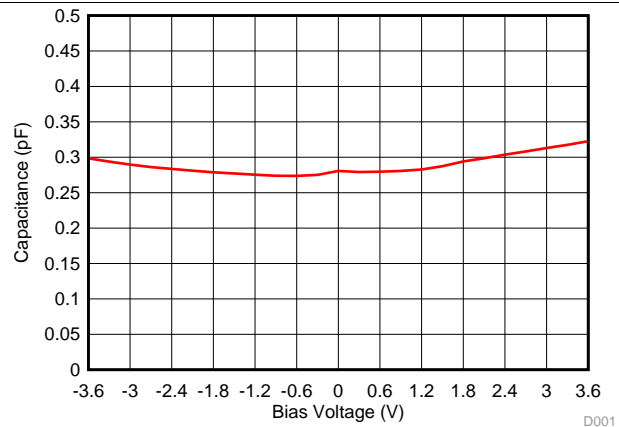
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	I _{IO} < 10 nA	–3.6		3.6	V
V _{BRF}	Breakdown voltage, any IO pin to GND ⁽¹⁾	I _{IO} = 1 mA, T _A = 25°C	5.5	6.4	7.5	V
V _{BRR}	Breakdown voltage, GND to any IO pin ⁽¹⁾	I _{IO} = 1 mA, T _A = 25°C	–5.5	–6.4	–7.5	V
V _{HOLD}	Holding voltage ⁽²⁾	I _{IO} = 1 mA		5.8		V
V _{CLAMP}	Clamping voltage	I _{PP} = 1 A, TLP, from IO to GND		6.6		V
		I _{PP} = 5 A, TLP, from IO to GND		8.8		
		I _{PP} = 1 A, TLP, from GND to IO		6.6		
		I _{PP} = 5 A, TLP, from GND to IO		8.8		
I _{LEAK}	Leakage current, any IO to GND	V _{IO} = ±2.5 V			10	nA
R _{DYN}	Dynamic resistance	IO to GND		0.47		Ω
		GND to IO		0.47		
C _L	Line capacitance	V _{IO} = 0 V, f = 1 MHz, IO to GND, T _A = 25°C		0.25	0.33	pF
ΔC _L	Variation of line capacitance	Delta of capacitance between any two IO pins, V _{IO} = 0 V, f = 1 MHz, T _A = 25°C, GND = 0 V		0.01	0.07	pF
C _{CROSS}	Channel to channel capacitance	Capacitance from one IO to another, V _{IO} = 0 V, f = 1 MHz, GND = 0 V		0.13		pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when 1 mA is applied in the positive-going direction, before the device latches into the snapback state.

(2) V_{HOLD} is defined as the voltage when 1 mA is applied in the negative-going direction, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics


Figure 1. Positive TLP Curve

Figure 2. Negative TLP Curve

Figure 3. Surge Curve ($t_p = 8/20 \mu s$), any IO pin to GND

Figure 4. 8-kV IEC Waveform

Figure 5. -8-kV IEC Waveform

Figure 6. Capacitance vs Bias Voltage

Typical Characteristics (continued)

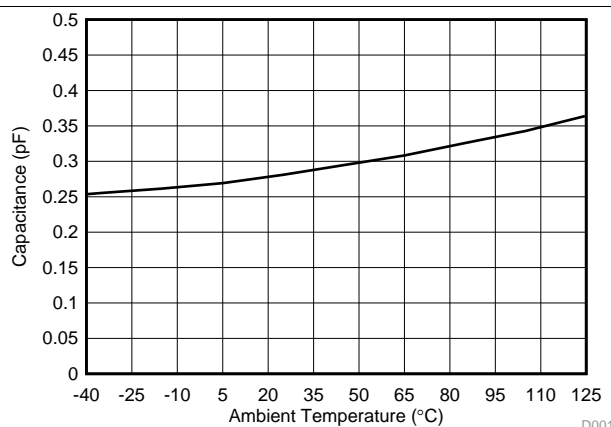


Figure 7. Capacitance vs Ambient Temperature

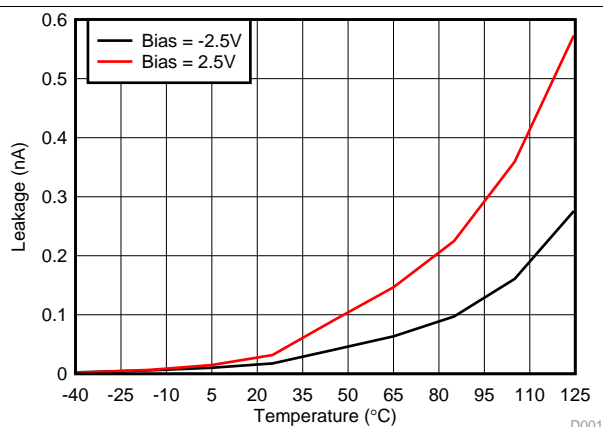


Figure 8. Leakage Current vs Temperature

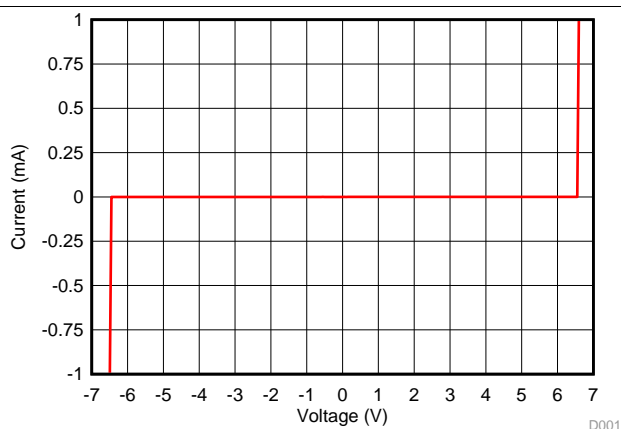


Figure 9. DC Voltage Sweep I-V Curve

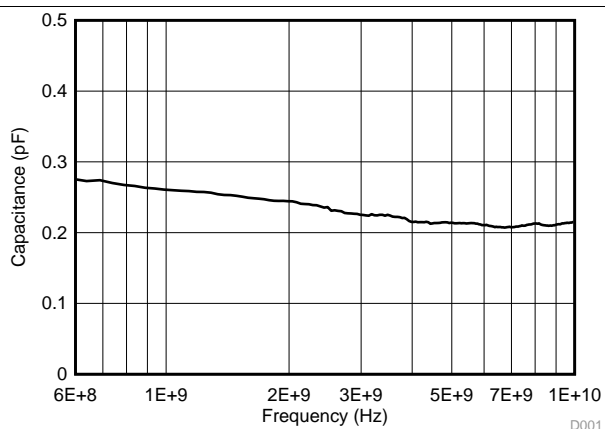


Figure 10. Capacitance vs Frequency

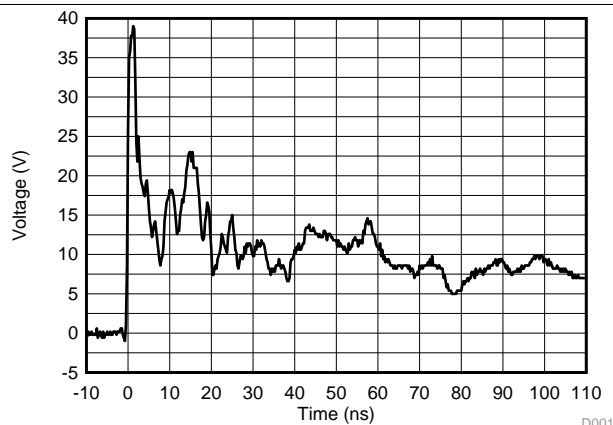


Figure 11. 8-kV IEC Waveform through 2-m HDMI Cable

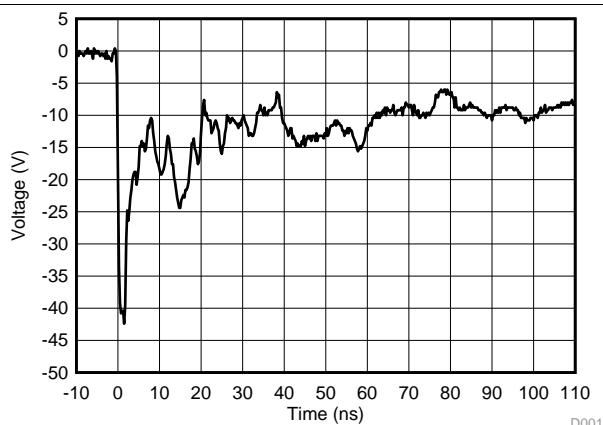


Figure 12. -8-kV IEC Waveform through 2-m HDMI Cable

Typical Characteristics (continued)

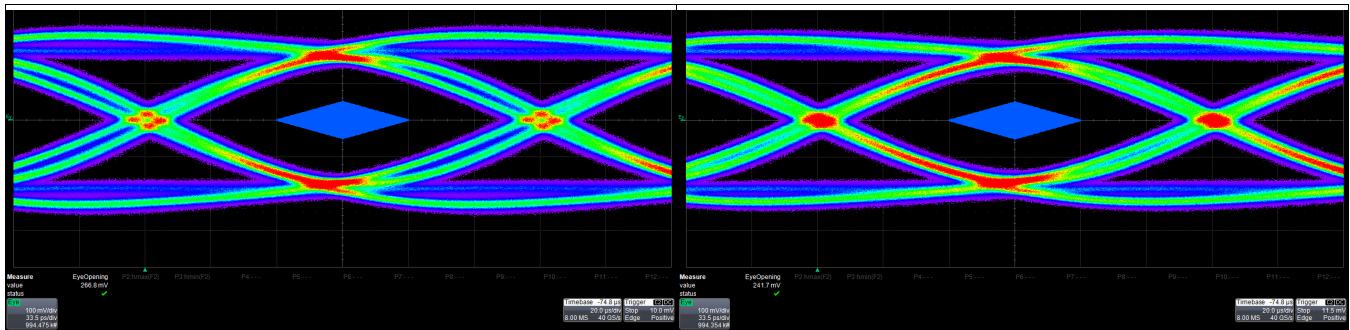


Figure 13. USB3.0 Eye Diagram (Bare Board)

Figure 14. USB3.0 Eye Diagram (With TPD4E02B04)

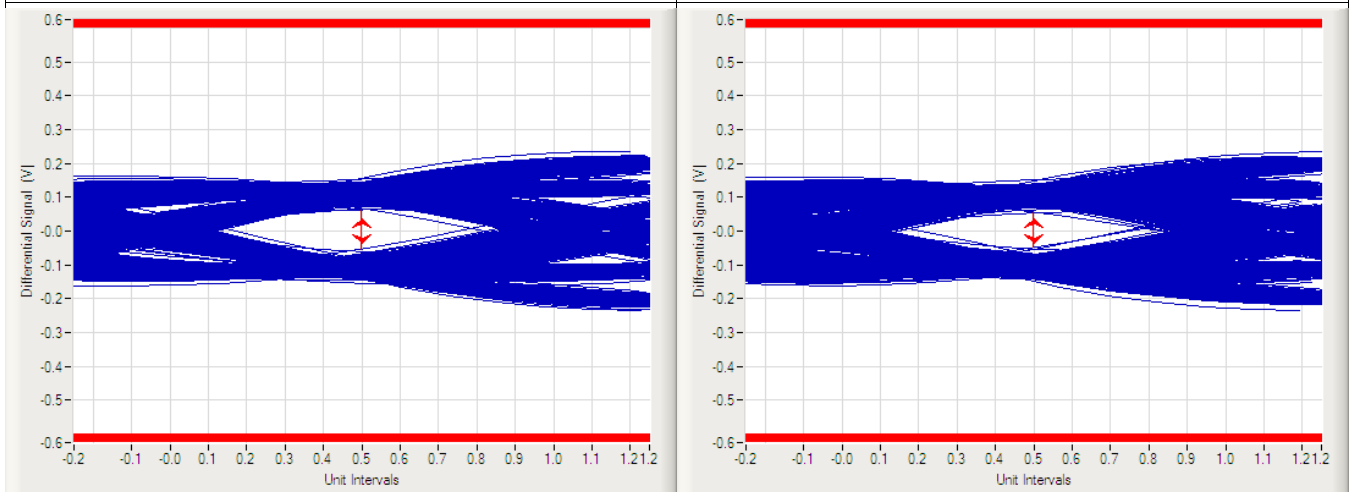


Figure 15. USB3.1 Gen 2 Eye Diagram (Bare Board)

Figure 16. USB3.1 Gen 2 Eye Diagram (With TPD4E02B04)

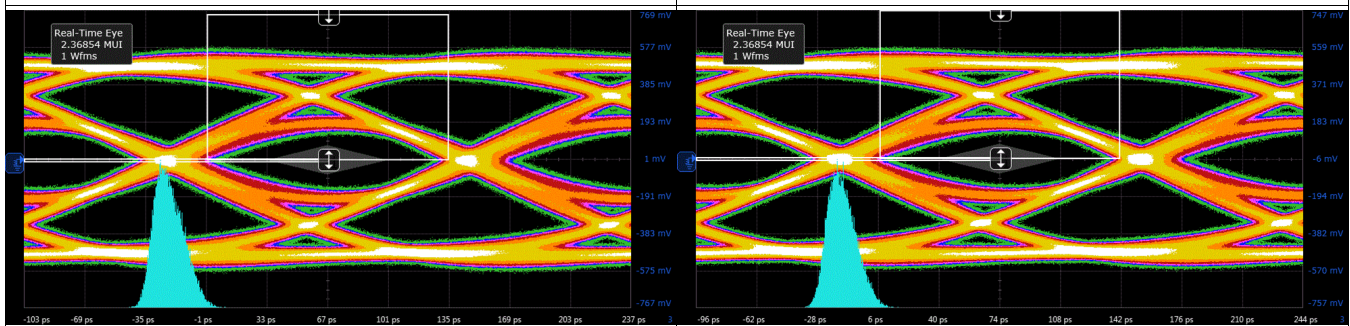


Figure 17. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

Figure 18. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD4E02B04)

Typical Characteristics (continued)

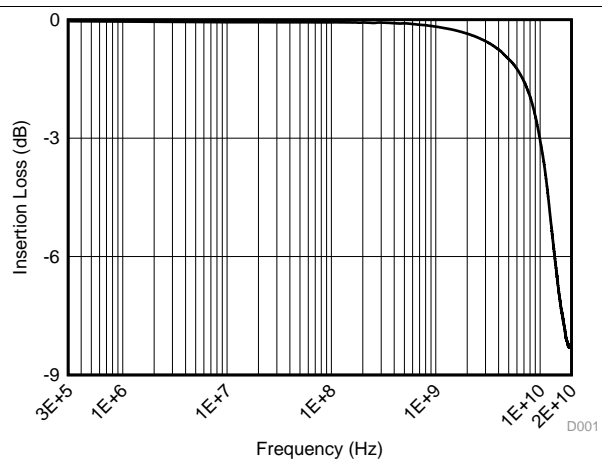


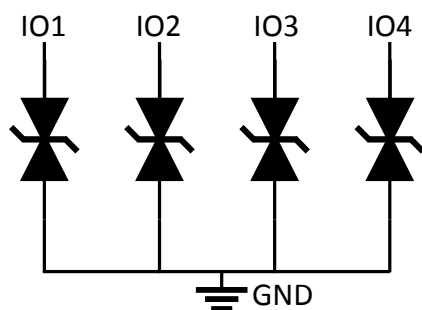
Figure 19. Differential Insertion Loss

7 Detailed Description

7.1 Overview

The TPD4E02B04 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ± 12 -kV contact and ± 15 -kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50- Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2 A and 17 W (8/20 μ s waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.25 pF (typical) and 0.33 pF (maximum). This device supports data rates up to 10 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ± 5.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ± 3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ± 2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.8 V ($I_{PP} = 5$ A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 10 Gbps, because of the extremely low IO capacitance.

Feature Description (continued)

7.3.9 Industrial Temperature Range

This device features an industrial operating range of -40°C to $+125^{\circ}\text{C}$.

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The package offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD4E02B04 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR} . During ESD events, voltages as high as $\pm 15\text{ kV}$ (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD4E02B04 (usually within 10s of nanoseconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E02B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a safe level for the protected IC.

8.2 Typical Application

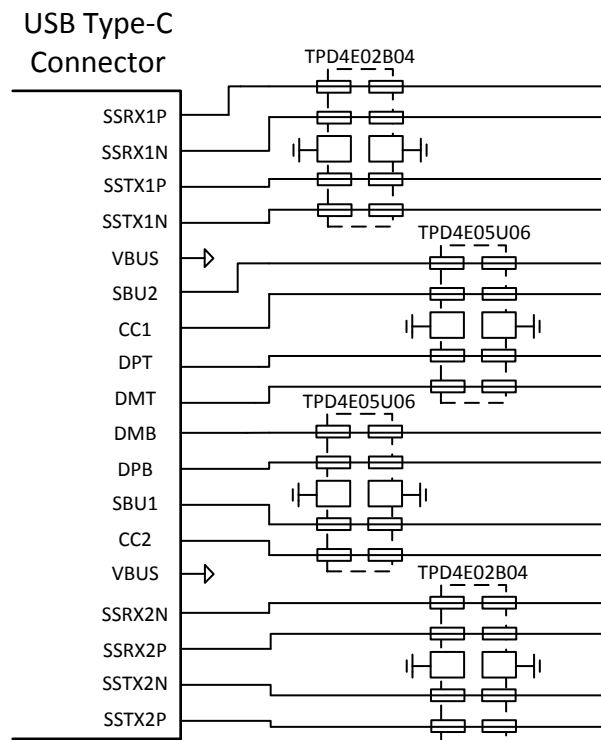


Figure 20. USB 3.1 Gen 2 Type-C ESD Schematic

Typical Application (continued)

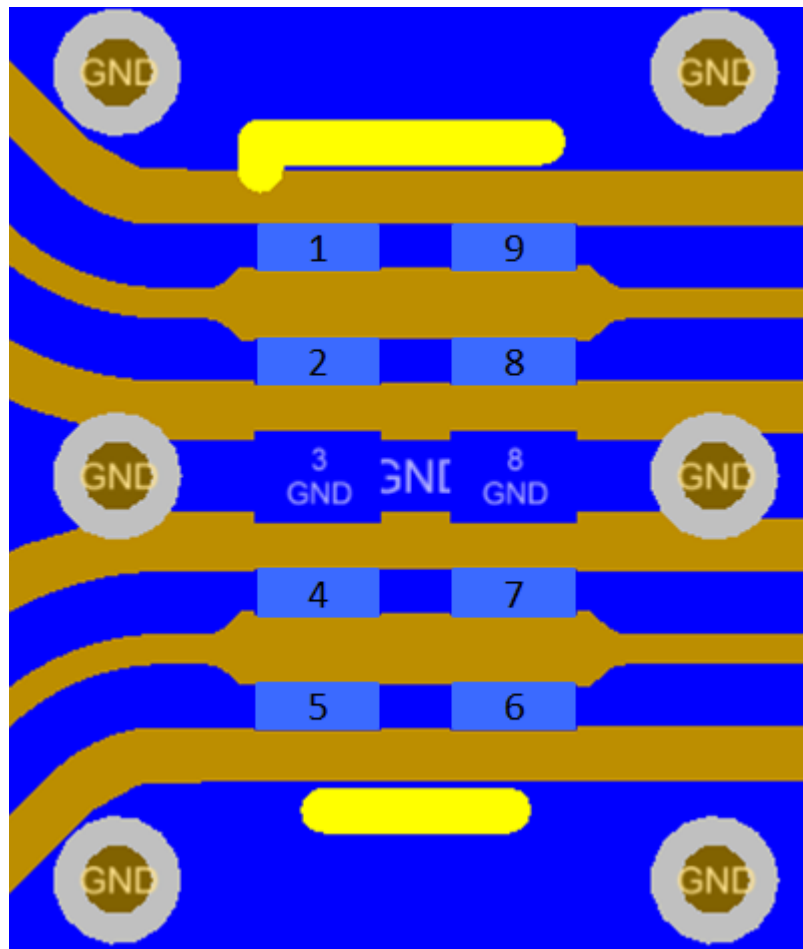


Figure 21. USB 3.1 Gen 2 SuperSpeed Layout

8.2.1 Design Requirements

For this design example two TPD4E02B04 devices and two TPD4E05U06 devices are being used in a USB 3.1 Gen 2 Type-C application. This provides a complete ESD protection scheme.

Given the USB 3.1 Gen 2 Type-C application, the parameters listed in [Table 1](#) are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal Range on SuperSpeed+ Lines	0 V to 3.6 V
Operating Frequency on SuperSpeed+ Lines	5 GHz
Signal Range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating Frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD4E02B04 supports signal ranges between -3.6 V and 3.6 V , which supports the SuperSpeed+ pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V , which supports the CC, SBU, and DP/DM lines.

8.2.2.2 Operating Frequency

The TPD4E02B04 has a 0.25 pF (typical) capacitance, which supports the USB3.1 Gen 2 data rates of 10 Gbps . The TPD4E05U06 has a 0.5 pF (typical) capacitance, which easily supports the CC, SBU, and DP/DM data rates.

8.2.3 Application Curves

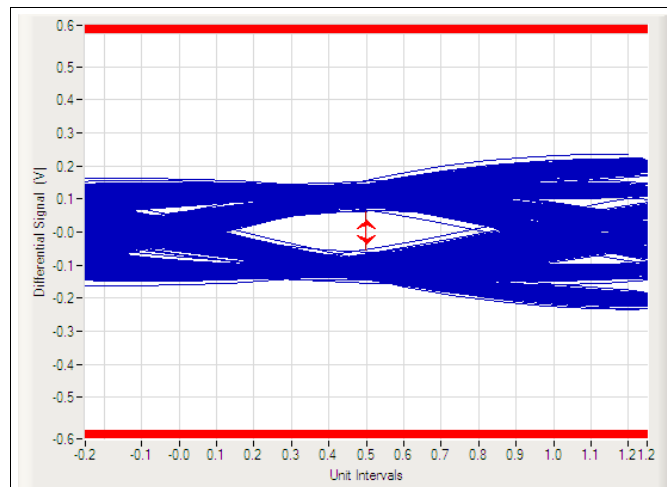


Figure 22. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

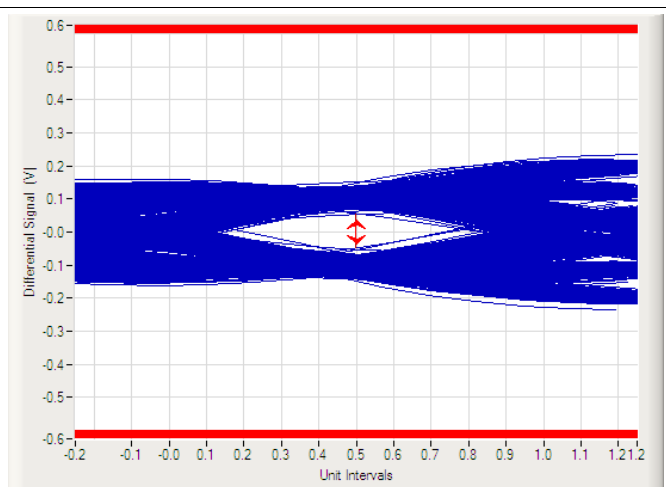


Figure 23. USB 3.1 Gen 2 10-Gbps Eye Diagram (With TPD4E02B04)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
 - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

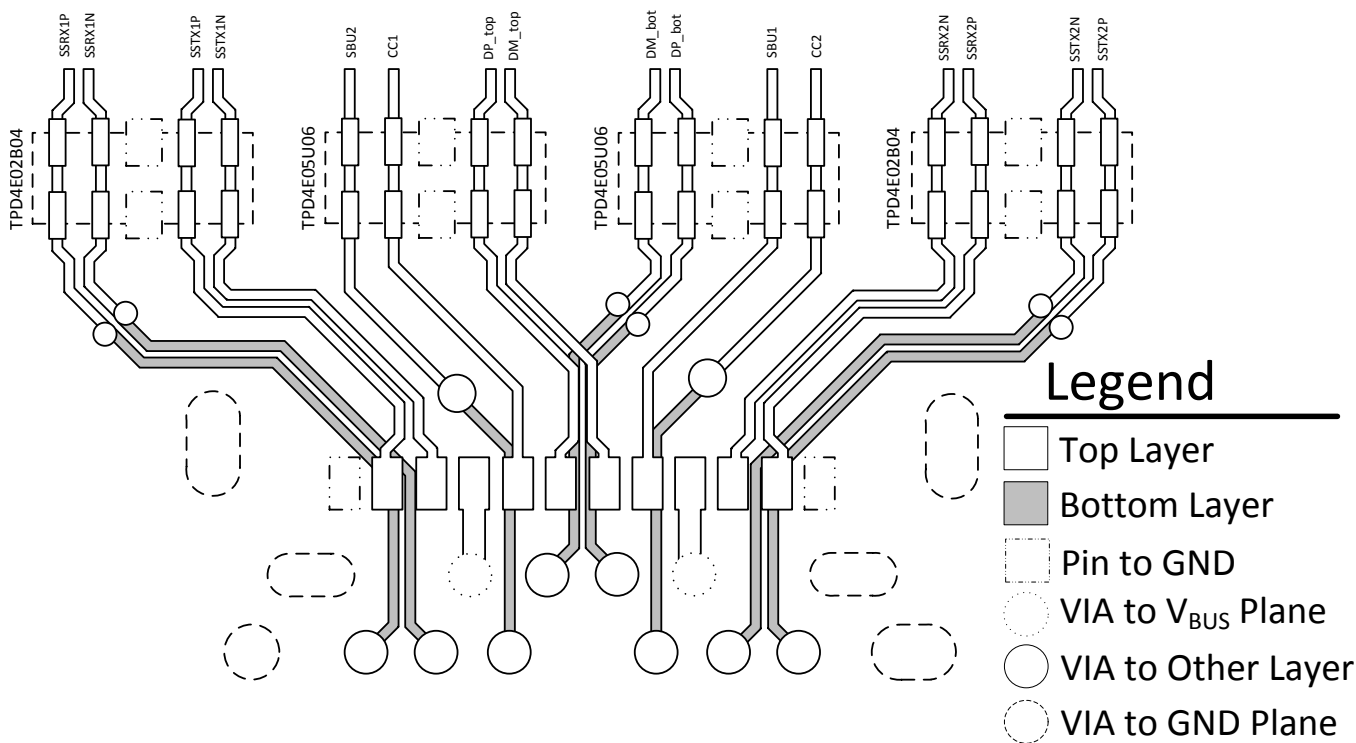


Figure 24. USB Type-C Mid-Mount, Hybrid Connector with One-Sided ESD Layout

Layout Examples (continued)

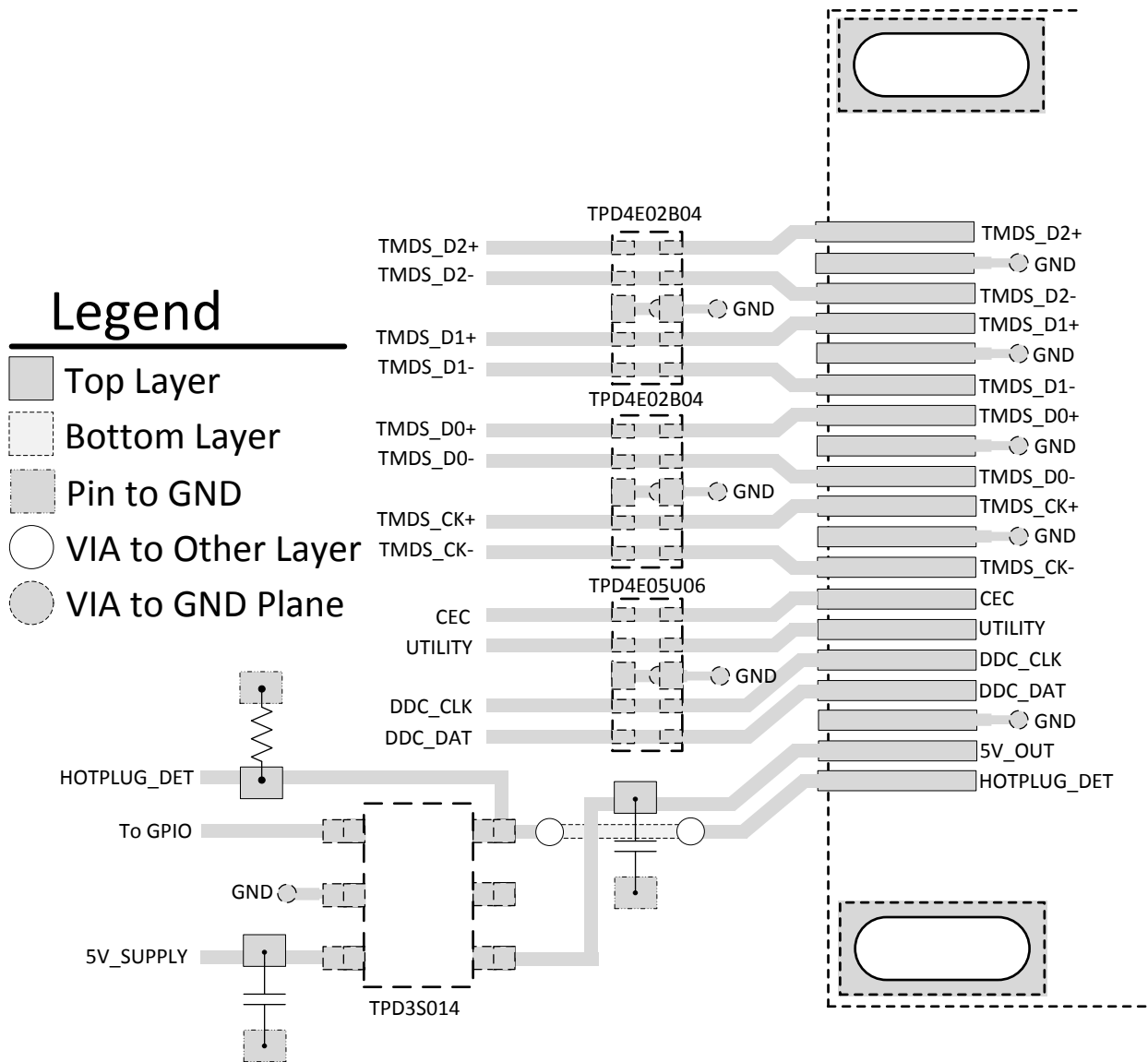


Figure 25. HDMI2.0 Type-A Transmitter Port Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Reading and Understanding an ESD Protection Datasheet*, [SLLA305](#)
- *ESD Layout Guide*, [SLVA680](#)
- *Picking ESD Diodes for Ultra High-Speed Data Lines*, [SLVA785](#)
- *TPD4E02B04EVM Users Guide*, [SLVUAH6](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E02B04DQAR	Active	Production	USON (DQA) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SG 1SY
TPD4E02B04DQAR.B	Active	Production	USON (DQA) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SG 1SY
TPD4E02B04DQARG4.B	Active	Production	USON (DQA) 10	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1SY

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPD4E02B04 :

- Automotive : [TPD4E02B04-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E02B04DQAR	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E02B04DQAR	USON	DQA	10	3000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

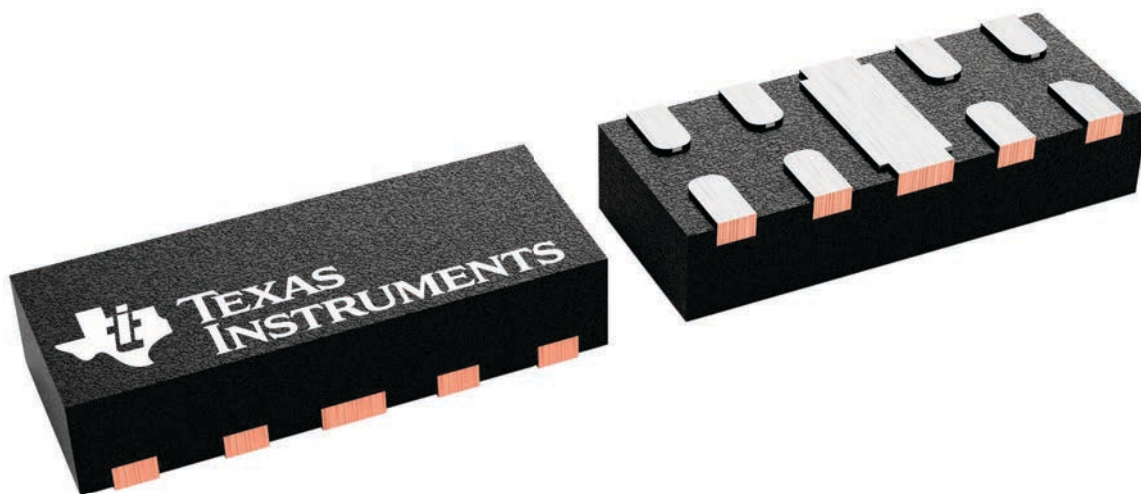
DQA 10

USON - 0.55 mm max height

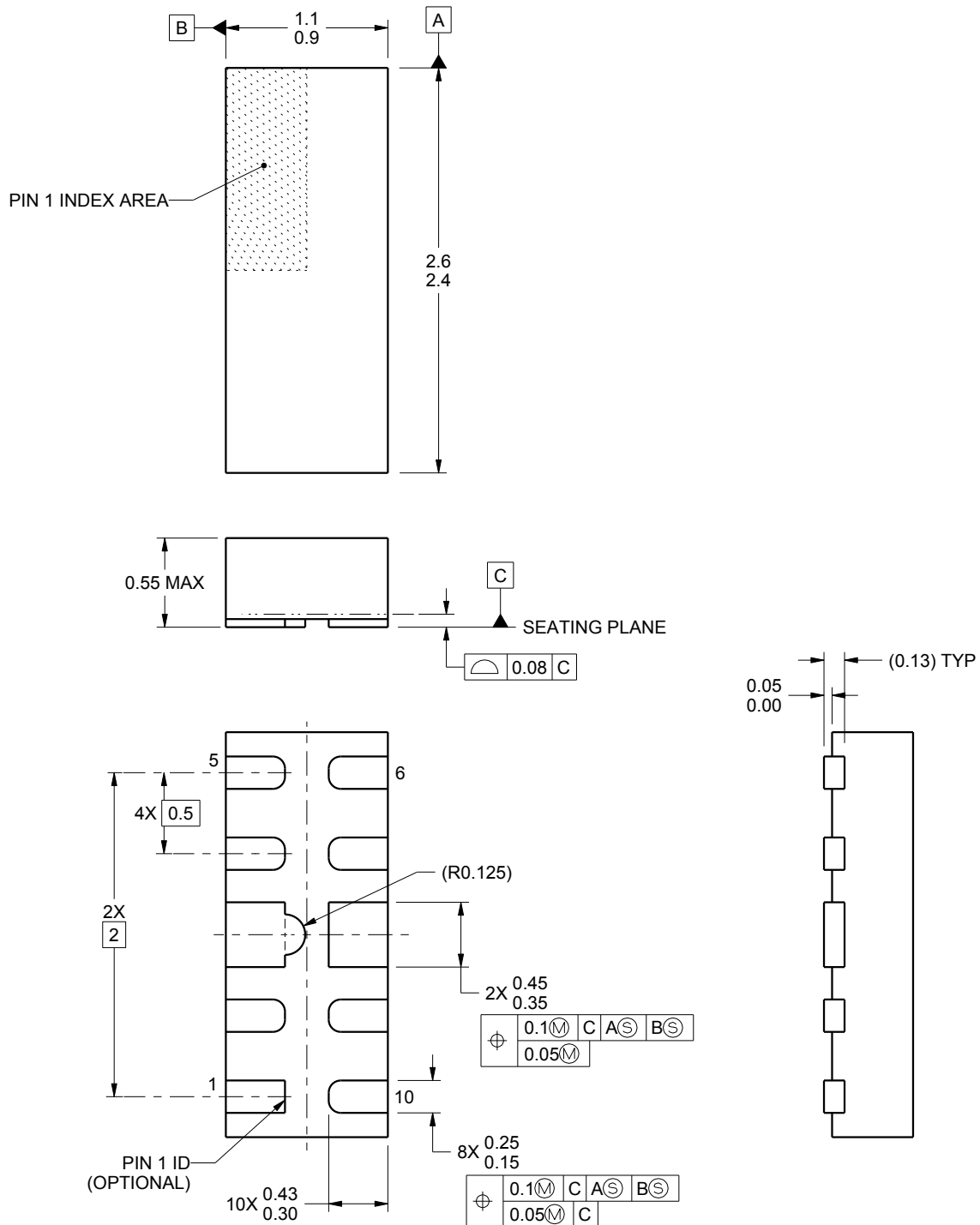
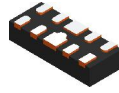
1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4230320/A



4220328/A 12/2015

NOTES:

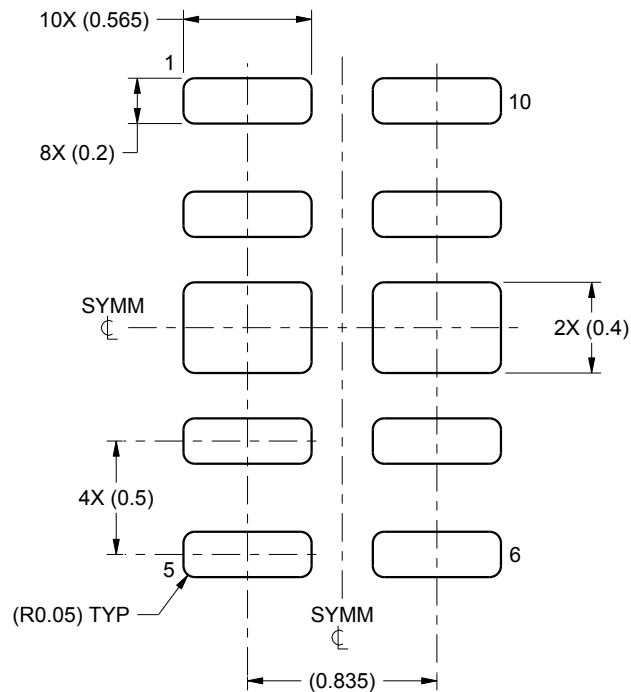
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

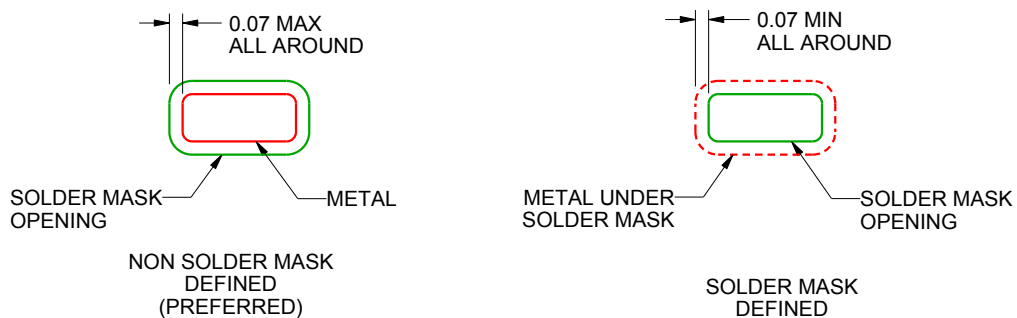
DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

4220328/A 12/2015

NOTES: (continued)

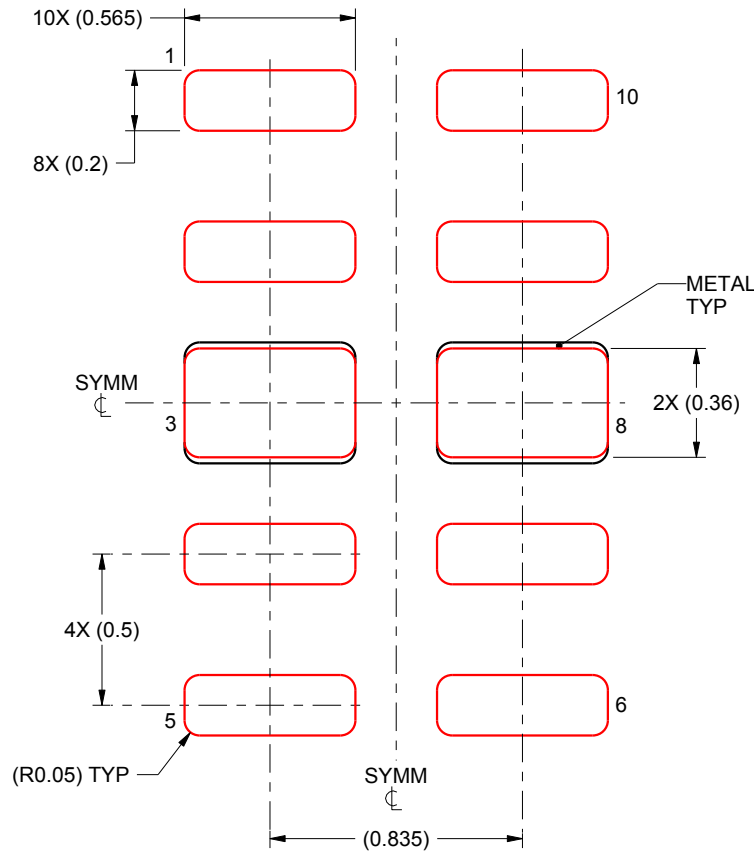
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220328/A 12/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2025, Texas Instruments Incorporated

Last updated 10/2025