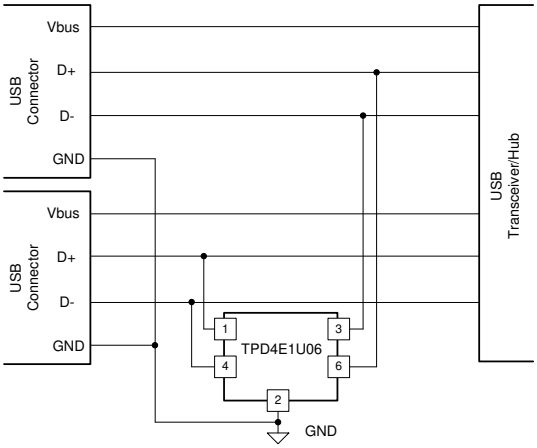
TPD4E1U06 Quad-Channel, High-Speed ESD Protection Device

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±15kV Contact Discharge
  - ±15kV Air-Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80A (5/50ns)
- IEC 61000-4-5 Surge Protection
  - 3A (8/20µs)
- IO Capacitance 0.8pF (Typical)
- DC Breakdown Voltage 6.5V (Minimum)
- Ultra Low Leakage Current 10nA (Maximum)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to +125°C
- Small, Easy-to-Route DCK, and DBV Package

2 Applications

- USB 2.0
- Ethernet
- HDMI Control Lines
- MIPI Bus
- LVDS
- SATA



Simplified Schematic

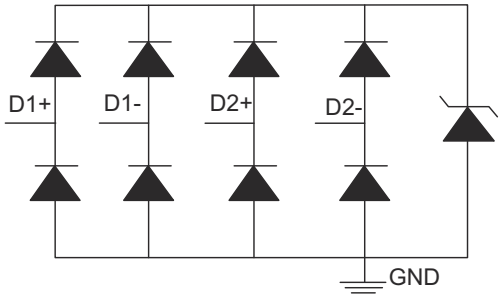
3 Description

The TPD4E1U06 is a quad-channel unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diode with ultra low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. The 0.8pF line capacitance makes it an excellent choice for a wide range of applications. Typical application areas include HDMI, USB2.0, MHL, and DisplayPort.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPD4E1U06DCK	SC70	2.00mm × 1.25mm
TPD4E1U06DBV	SOT-23	2.90mm × 1.60mm

(1) For all available packages, see Section 10.



Circuit Schematic Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

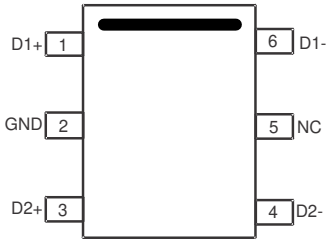


Figure 4-1. DCK Package6-Pin SC70Top View

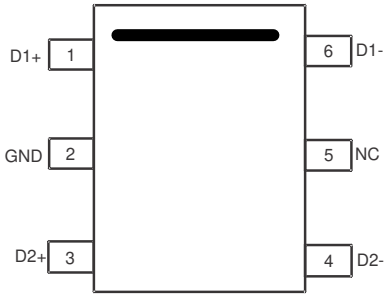


Figure 4-2. DBV Package6-Pin SOT-23Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D1+	1	I/O	ESD protected channel. Connect to data line as close to the connector as possible
D1–	6	I/O	
D2–	4	I/O	
D2+	3	I/O	
GND	2	GND	Ground. Connect to ground
NC	5	I/O	No connect. Can be left floating, grounded, or connected to VCC

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	IEC 61000-4-4 EFT protection (5/50ns)		80	A
I_{PP}	IEC 61000-4-5 surge protection (8/20µs) peak pulse current		3	A
P_{PP}	IEC 61000-4-5 surge protection (8/20µs) peak pulse power		45	W
	Operating temperature	–40	125	°C
T_{stg}	Storage temperature	–65	115	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact ESD	±15000	V
		IEC 61000-4-2 air-gap ESD	±15000	

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	0	5.5	V
T_A	Operating free-air temperature	–40	125	°C

5.5 Thermal Information

THERMAL METRIC(1)		TPD4E1U06		UNIT
		DBV (SOT-23)	DCK (SC-70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.3	274.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	166.1	113.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.4	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	57.3	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.9	75.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.6 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} = 10µA				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1A, tp = 8/20µs, from I/O to GND(1)			11		V
		I_{PP} = 3A, tp = 8/20µs, from I/O to GND(1)			15		V
R_{DYN}	Dynamic resistance	Pin x to GND pin(2)			1.0		Ω
		GND to pin x			0.6		
C_L	Line capacitance	f = 1MHz, V_{BIAS} = 2.5V, 25°C			0.8	1	pF
C_{CROSS}	Channel to channel input capacitance	Pin 2 = 0V, f = 1MHz, V_{BIAS} = 2.5V, between channel pins	DCK package		0.006	0.015	pF
			DBV package		0.01	0.025	
$\Delta C_{IO\text{-}TO\text{-}GND}$	Variation of channel input capacitance	Pin 2 = 0V, f = 1MHz, V_{BIAS} = 2.5V, channel_x pin to ground – channel_y pin to ground			0.025	0.07	pF
V_{BR}	Break-down voltage, IO to GND	I_{IO} = 1mA		6.5		8.5	V
I_{LEAK}	Leakage current	V_{IO} = 2.5V			1	10	nA

(1) Non-repetitive current pulse 8/20µs exponentially decaying waveform according to IEC61000-4-5.
(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10A and I = 20A.

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5.7 Typical Characteristics

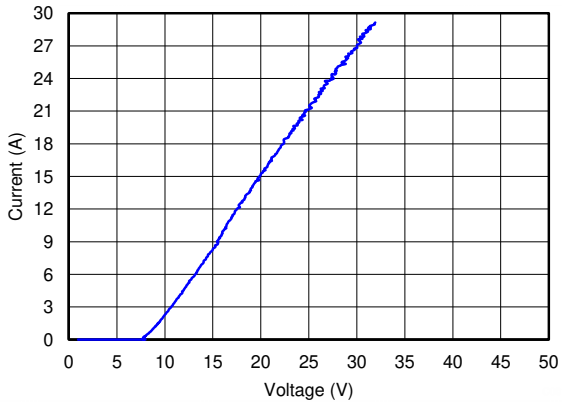


Figure 5-1. TLP, Data to GND

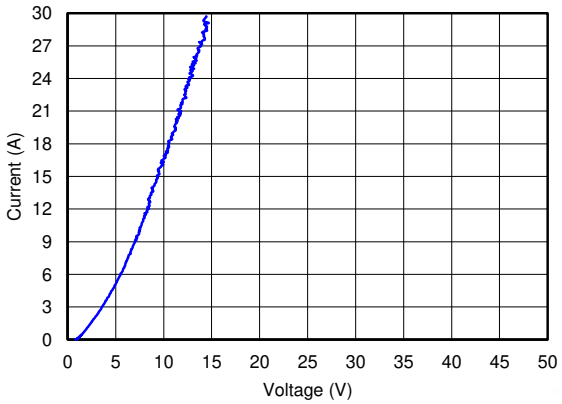


Figure 5-2. TLP, GND to Data

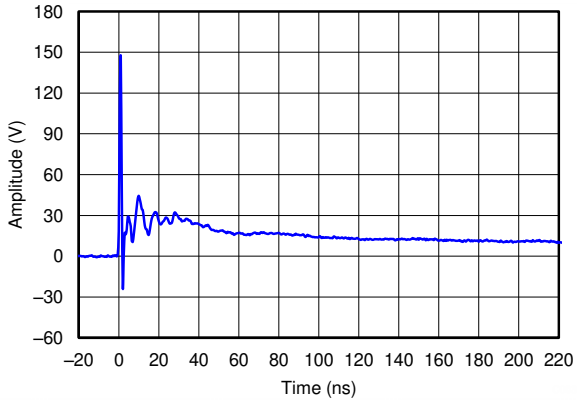


Figure 5-3. IEC 61000-4-2 Clamping Voltage, 8kV Contact

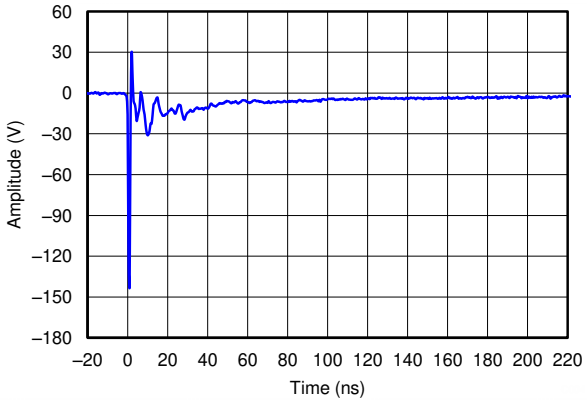


Figure 5-4. IEC 61000-4-2 Clamping Voltage, –8kV Contact

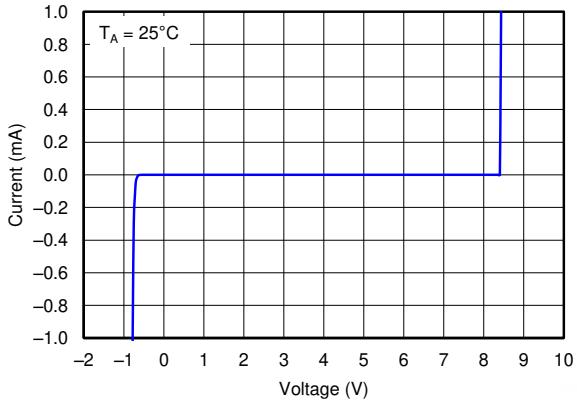


Figure 5-5. Diode Curve

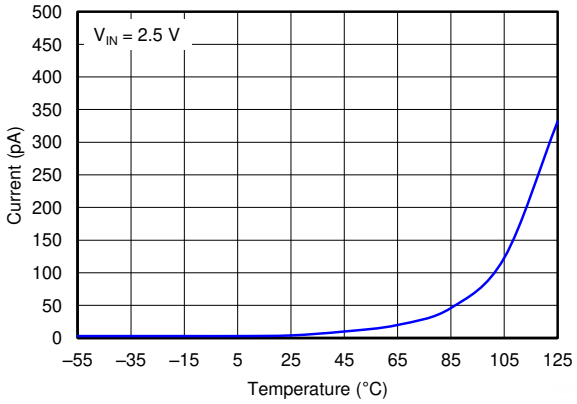


Figure 5-6. I_{LEAK} vs Temperature

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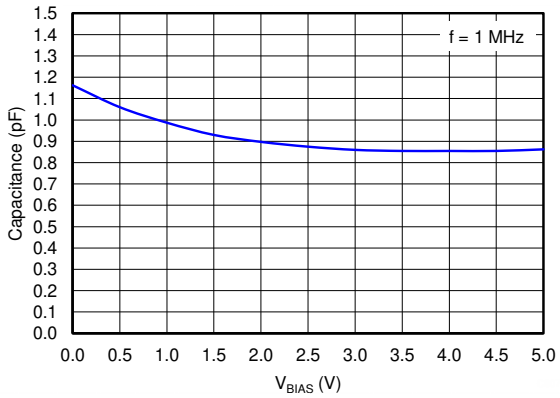


Figure 5-7. Capacitance Across V_{BIAS}

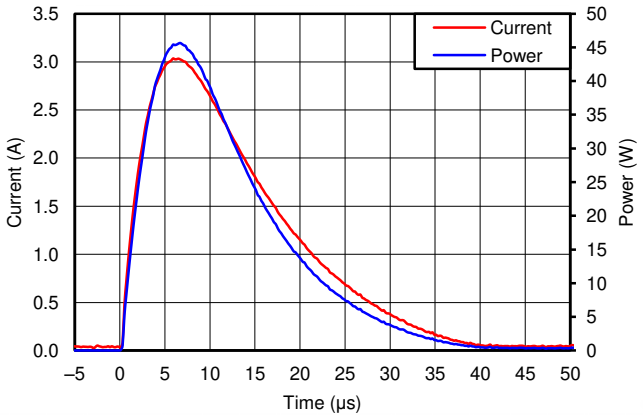


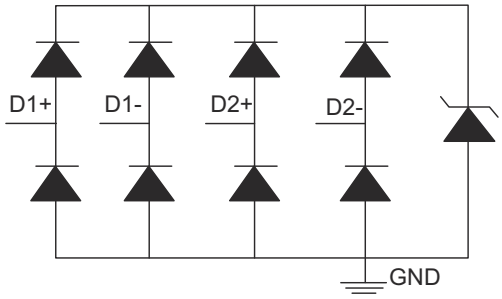
Figure 5-8. Surge Curve (tp = 8/20µs), Pin IO to GND

6 Detailed Description

6.1 Overview

The TPD4E1U06 is a quad channel unidirectional TVS ESD protection diode with ultra low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 international standard. Typical application areas include HDMI, USB2.0, MHL, and DisplayPort. The 0.8pF line capacitance makes it an excellent choice for a wide range of applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 IEC 61000-4-2 Level 4 ESD Protection

The I/O pins can withstand ESD events up to ±15kV contact and air. An ESD/surge clamp diverts the current to ground.

6.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 3A and 45W (8/20µs waveform). An ESD-surge clamp diverts this current to ground.

6.3.3 IEC 61000-4-4 EFT Protection

The IO pins can withstand an electrical fast transient burst of up to 80A (5/50ns waveform, 4kV with 50Ω impedance). An ESD-surge clamp diverts the current to ground.

6.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.8pF.

6.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5V. This confirms that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5V.

6.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10nA (Maximum) with a bias of 2.5V.

6.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 11V (I_{PP} = 1A).

6.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

6.3.9 Small, Easy-to-Route Packages

The layout of this device makes it simple to add protection to the design. Industry standard packages allow for easy additions to the board and easy layout.

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6.4 Device Functional Modes

The TPD4E1U06 is a passive integrated circuit that triggers when voltages are above V_{BR} or below the forward diode drop. During ESD events, voltages as high as ±15kV can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD4E1U06 (usually within 10s of nano-seconds) the device reverts to passive.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPD4E1U06 is a TVS diode array which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

7.2 Typical Application

For this design example, one TPD4E1U06 device is being used in a dual USB 2.0 application. This provides a complete port protection scheme.

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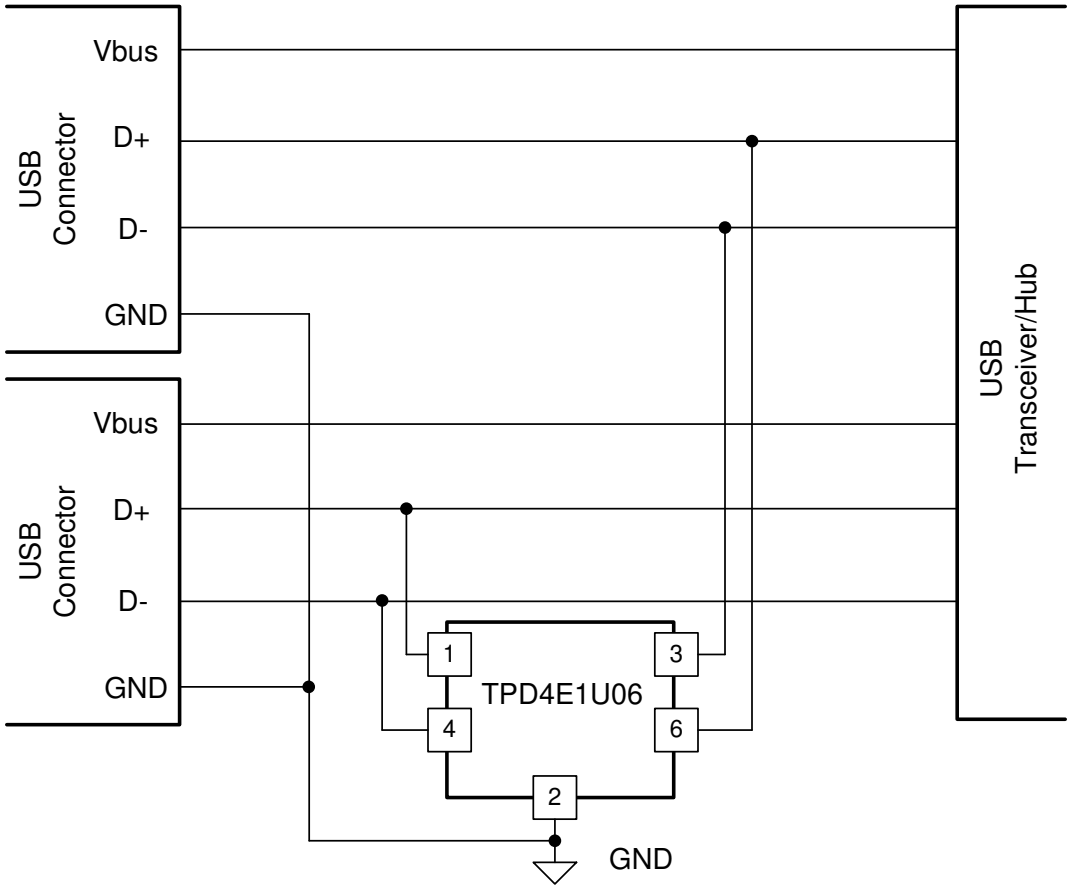


Figure 7-1. Dual USB 2.0 Application

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7.2.1 Design Requirements

Given the USB 2.0 application, the parameters in Table 7-1 are known.

Table 7-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on pins 1, 3, 4, or 6	0V to 5V
Operating frequency	240MHz

7.2.2 Detailed Design Procedure

7.2.2.1 Signal Range on Pins 1, 3, 4, or 6

The TPD4E1U06 has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 4 I/O channels protect which signal lines. Any I/O supports a signal range of 0 to 5.5V.

7.2.2.2 Operating Frequency

The TPD4E1U06 has a capacitance of 0.8pF (typical), supporting USB 2.0 data rates.

7.2.3 Application Curve

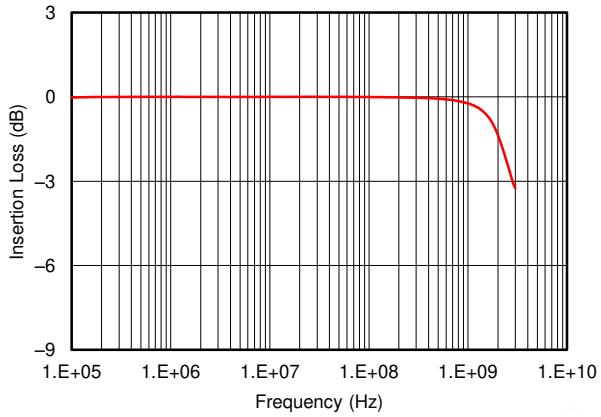


Figure 7-2. Insertion Loss Graph

7.3 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Do not violate the recommended I/O specification (0V to 5.5V) to confirm the device functions properly.

7.4 Layout

7.4.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

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7.4.2 Layout Example

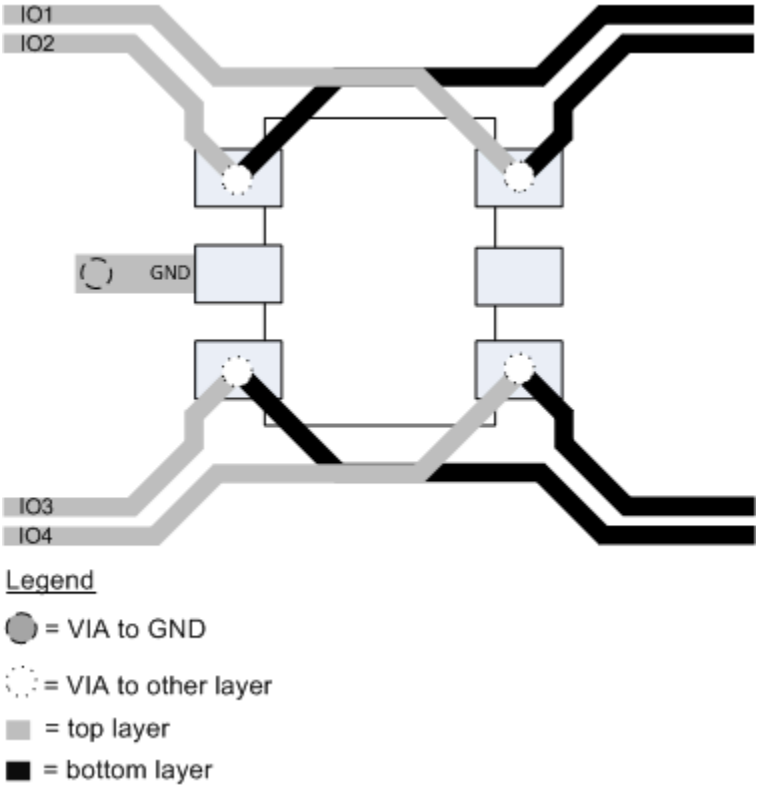


Figure 7-3. PCB Layout Recommendation

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Reading and Understanding an ESD Protection Datasheet*
- Texas Instruments, *ESD Layout Guide*
- Texas Instruments, *TTPD4E1U06DCK EVM User's Guide*
- Texas Instruments, *TPD4E1U06DBV EVM User's Guide*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

8.3 Community Resources

8.4 Trademarks

All trademarks are the property of their respective owners.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2017) to Revision E (October 2026)	Page
• Added TPD4E1U06-G4 to the datasheet	1

Changes from Revision C (October 2014) to Revision D (April 2017)	Page
• Updated DCK and DBV Pinout image	3
• Added 61000-4-5 spec to *Absolute Maximum Ratings* table	4
• Added *Section 6.3.2* section	8
• Added *Section 6.3.3* section	8

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E1U06DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(NG4, NG4P)
TPD4E1U06DBVR.B	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(NG4, NG4P)
TPD4E1U06DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(BP6, BP8, BPI) (BPP, BPP, BPS)
TPD4E1U06DCKR.B	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(BP6, BP8, BPI) (BPP, BPP, BPS)
TPD4E1U06DCKRG4	Active	Production	SC70 (DCK) | 3	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	BPP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

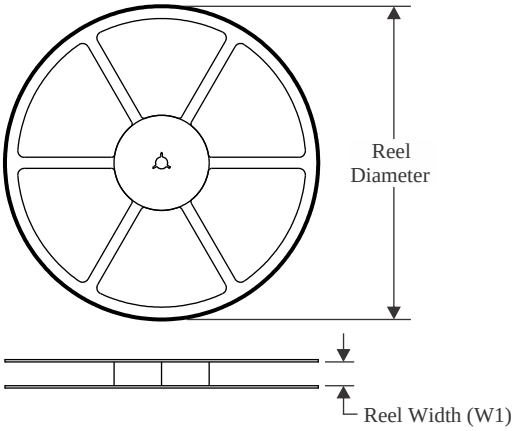
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

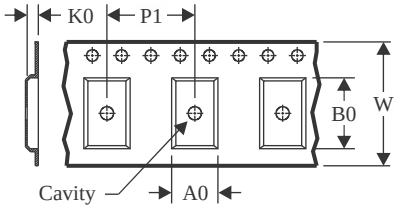
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

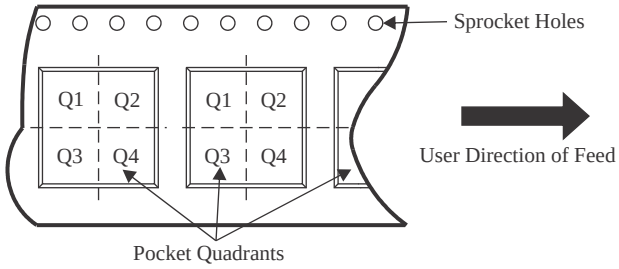


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

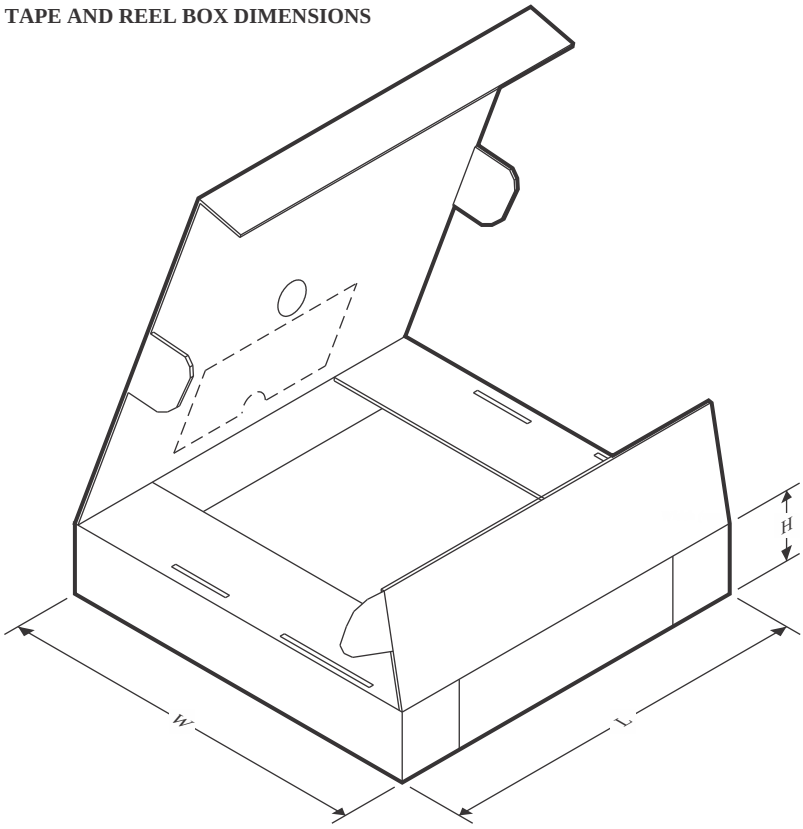
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E1U06DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPD4E1U06DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

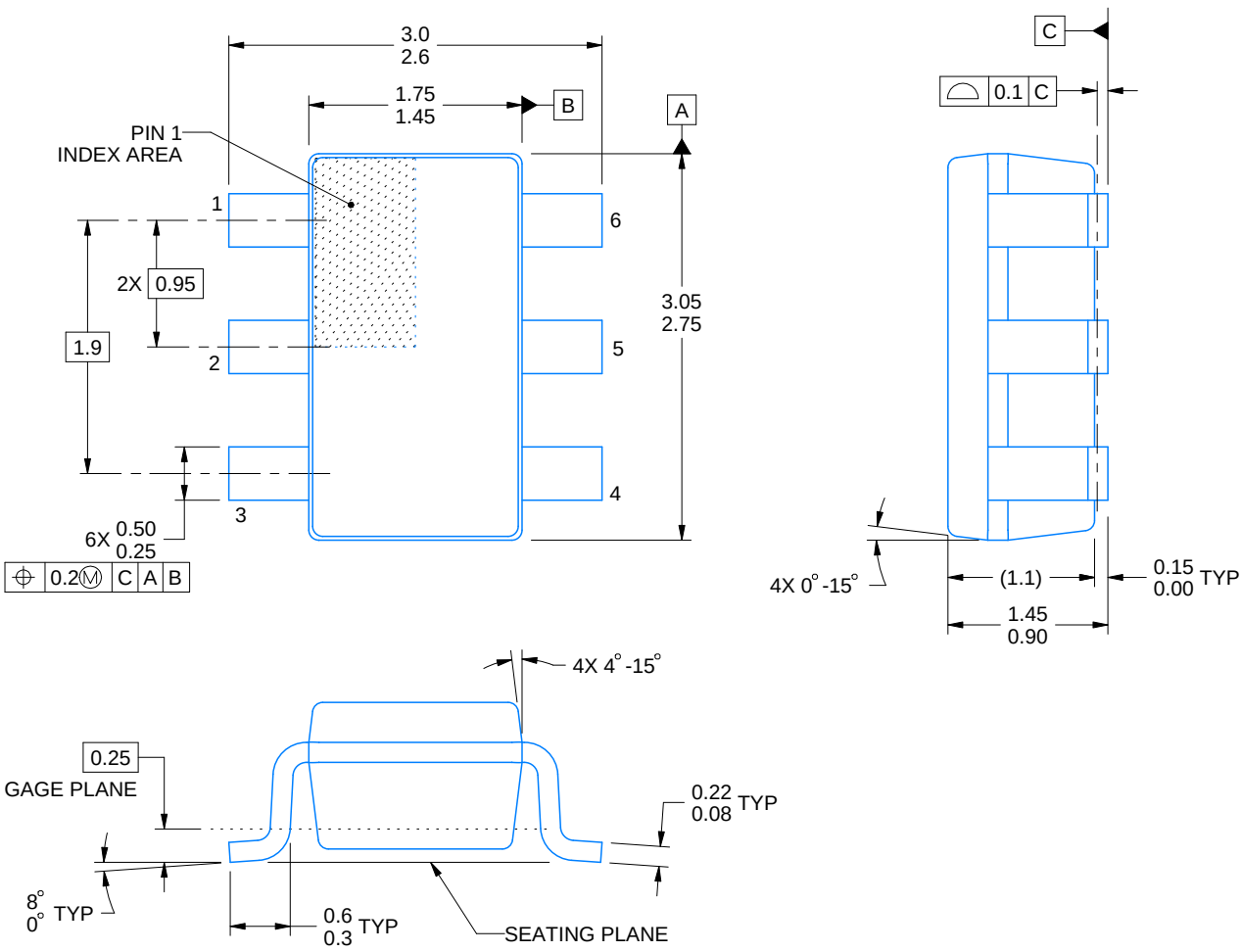
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E1U06DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPD4E1U06DCKR	SC70	DCK	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

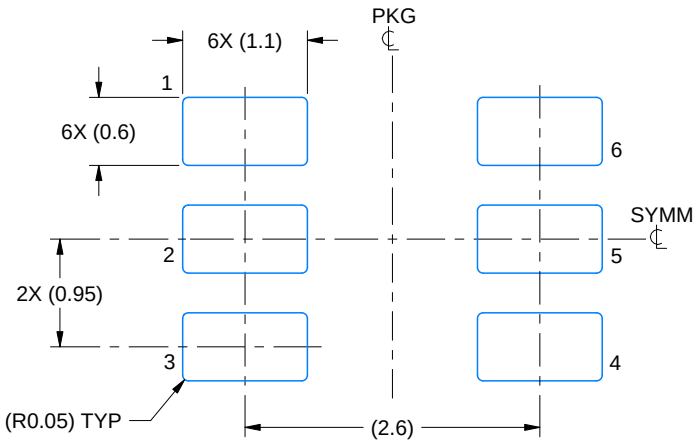
SMALL OUTLINE TRANSISTOR



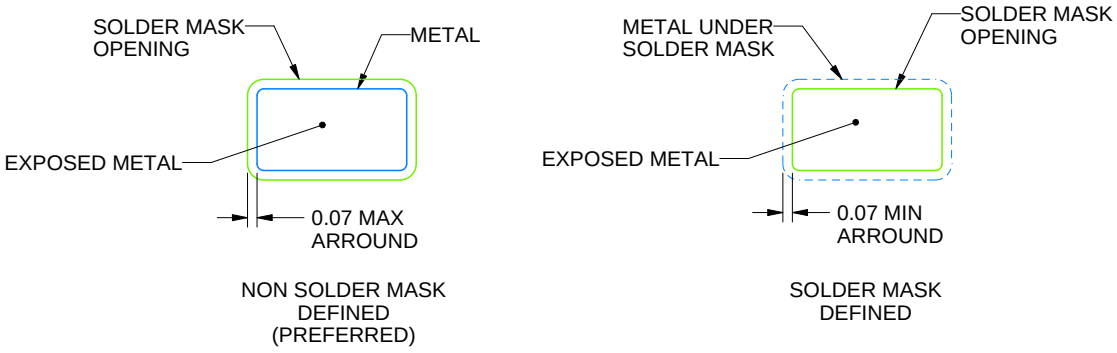
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

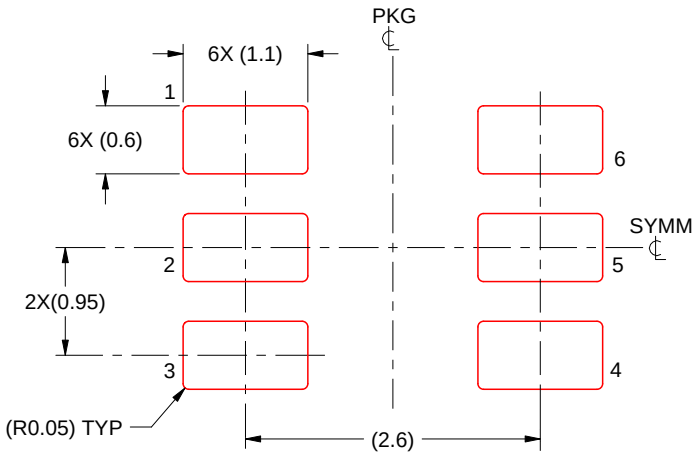


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

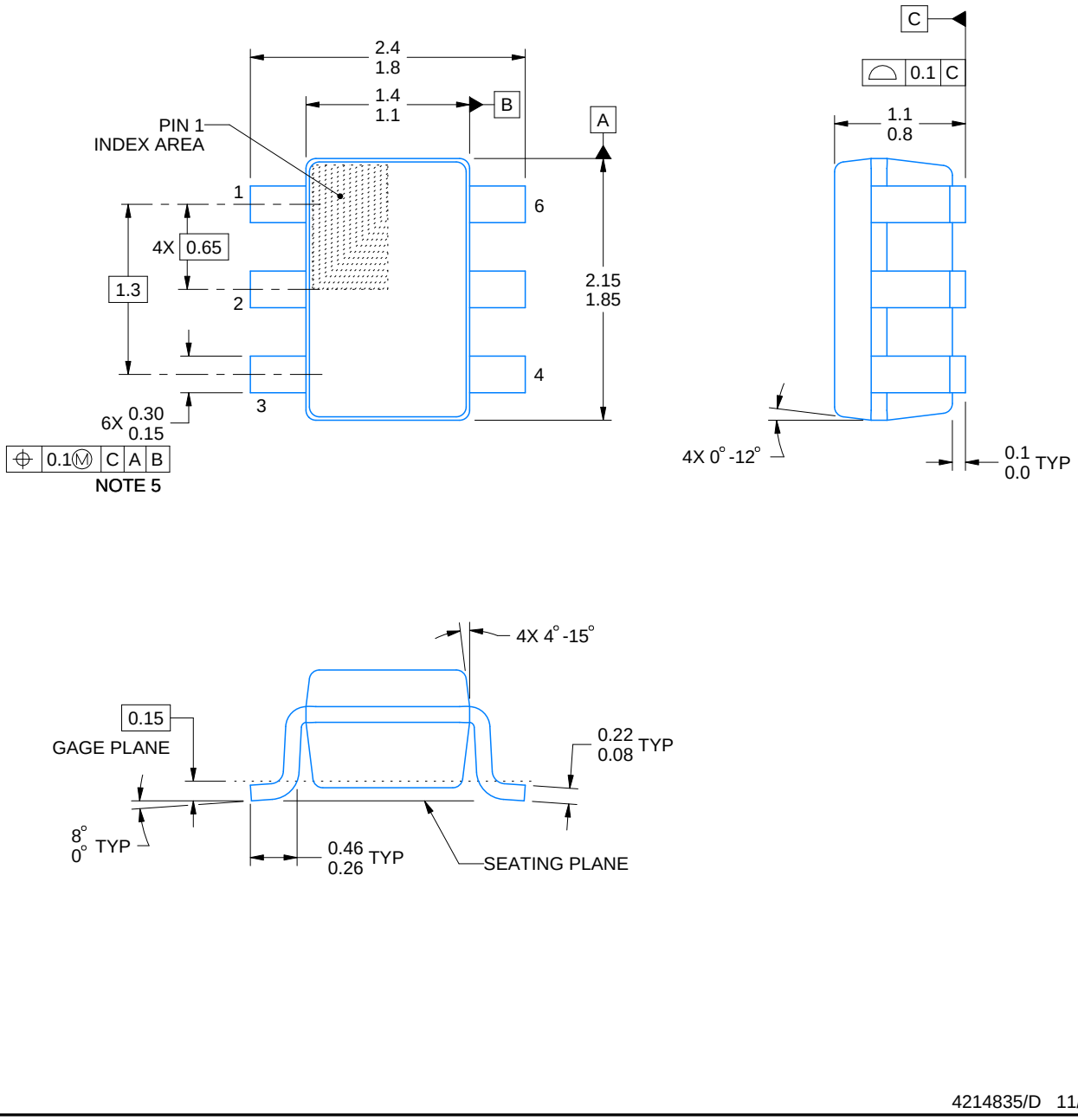
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

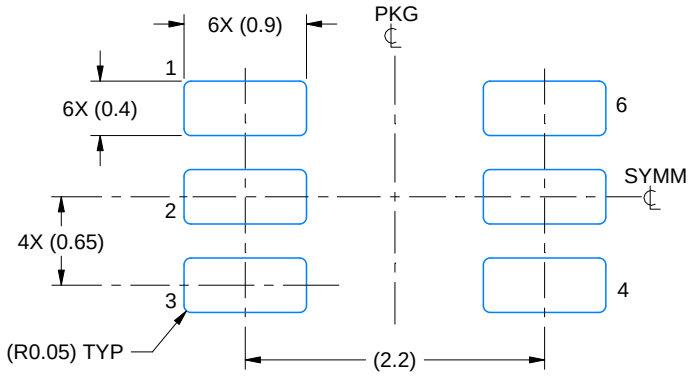
SMALL OUTLINE TRANSISTOR



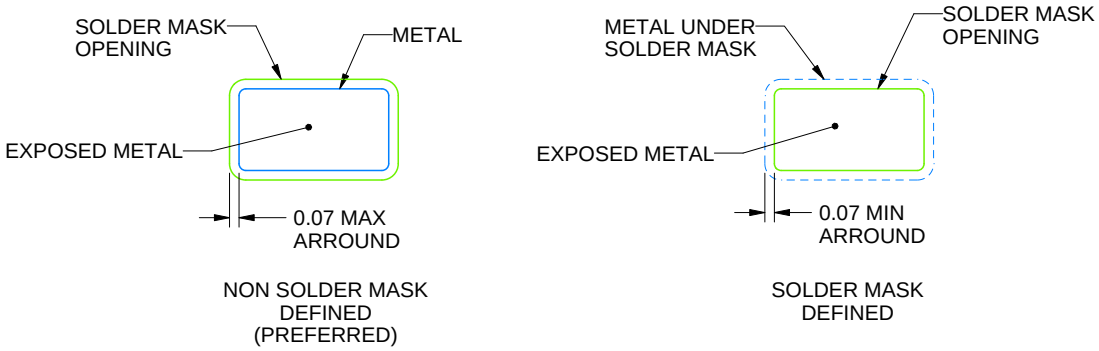
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

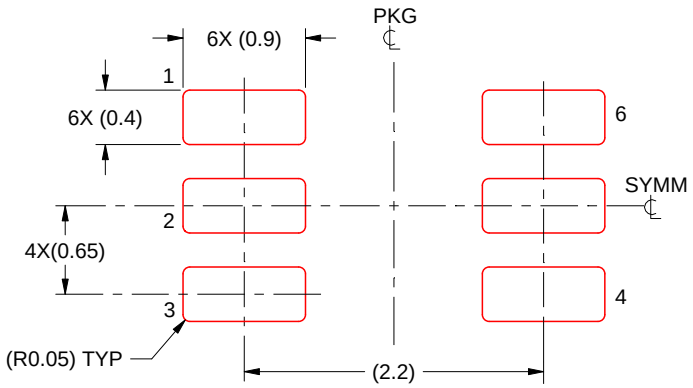


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

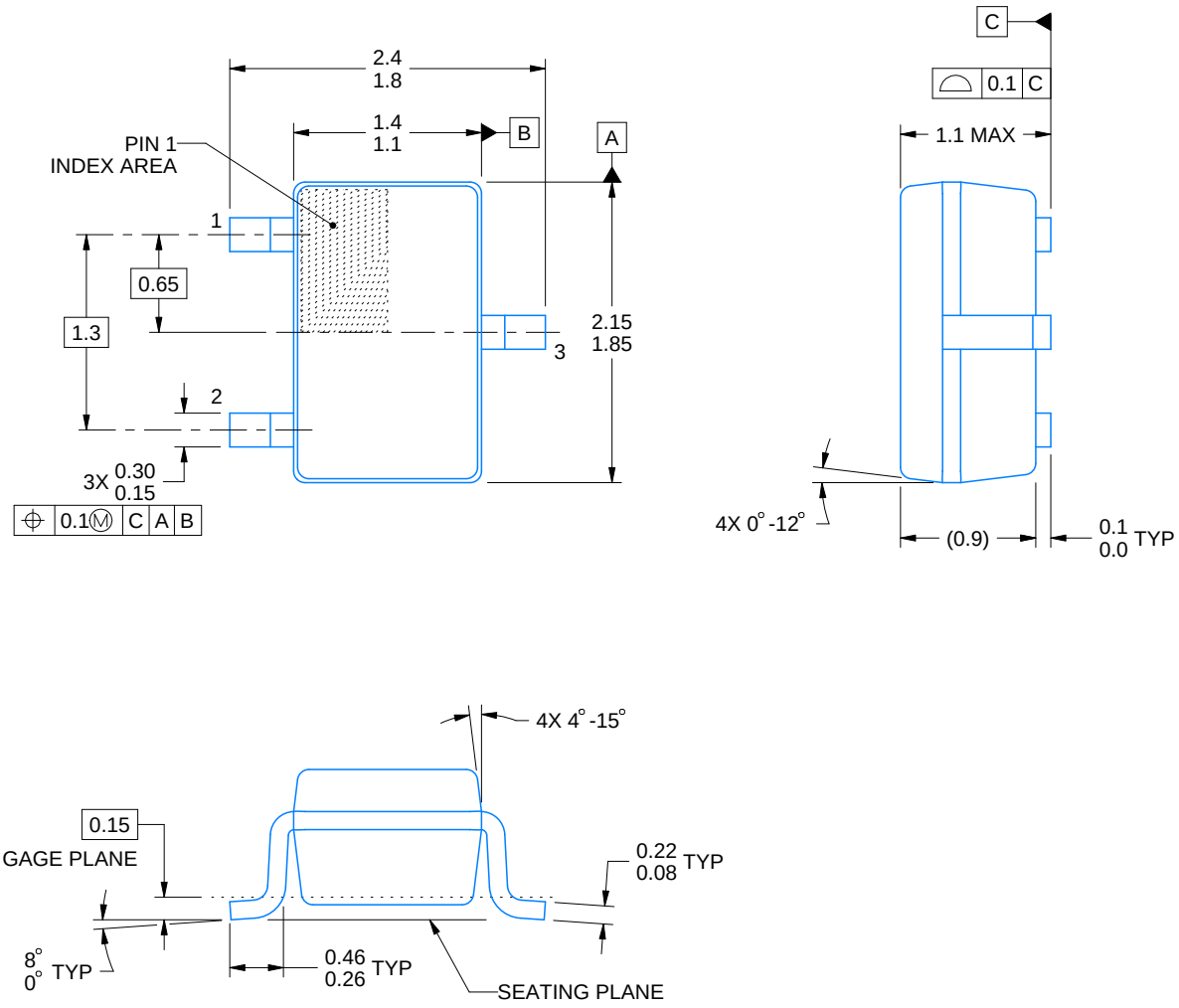
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0003A

SOT-SC70 - 1.1 max height

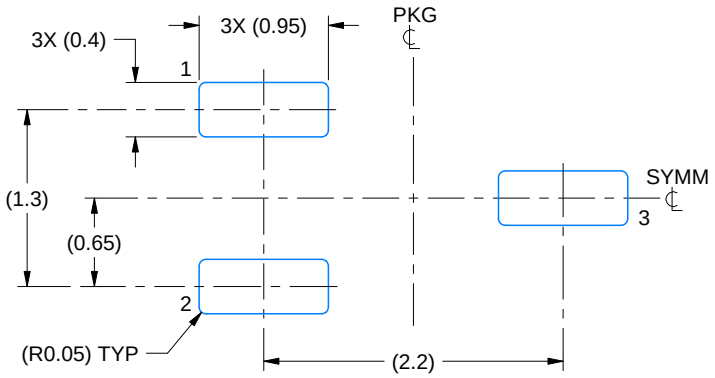
SMALL OUTLINE TRANSISTOR SC70



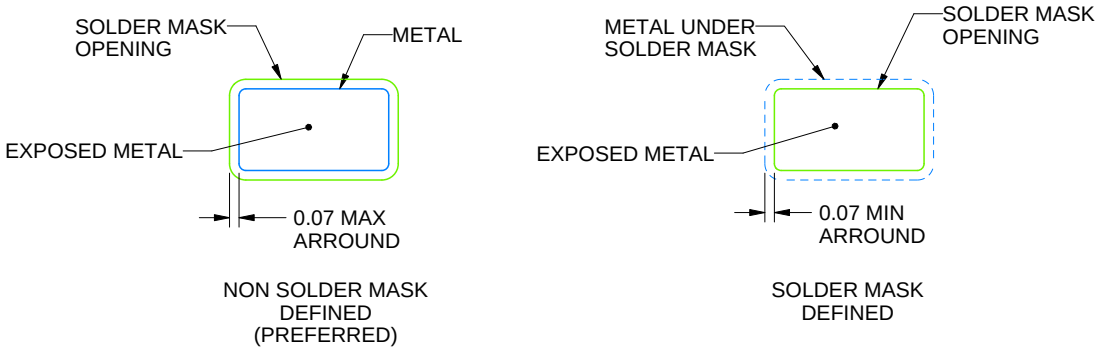
4220745/F 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

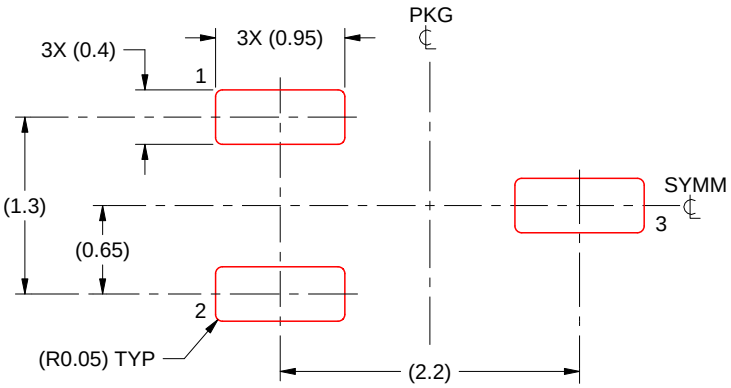


SOLDER MASK DETAILS

4220745/F 11/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/F 11/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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