TPS12S24F-Q1 80V, Low I_Q Automotive Dual High-Side Switch Controller With Low-Power Mode, Load Wakeup, I2T, SPI, and Diagnostics

1 Features

- AEC-Q100 automotive qualified for grade 1 temperature
- Input range: 3.5V to 70V (80V absolute maximum)
- Dual-channel SPI controlled smart high-side switch controller
- Low I_Q = 40µA in low-power mode
- Dual gate drive: GATEx: 0.5A source and 2A sink
- Integrated bypass switch capable to support 780mA continuous load current
- User programmable EEPROM with Limphome mode
- SPI configurable mode to drive capacitive loads
- Fast transition (7.5µs) from low-power mode to active mode using adjustable load wakeup threshold with $\overline{\text{FLT/WAKE}}$ indication
- Accurate analog current monitor output (VIMONx): ±2% at 30mV V_{SNS}
- Robust integrated protection:
  - Programmable Bi-I2T wire harness protection
  - Adjustable Bi-SCP (short-circuit) protection
  - NTC based external FET overtemperature protection
  - External FET adjustable VDS overvoltage protection
  - Controller overtemperature warning
  - Protection against reverse battery events down to –40V
  - Automatic shut off on loss of battery and ground
  - Adjustable undervoltage lockout and overvoltage protection
- Configure the digital sense output with integrated ADC to measure:
  - Bi-directional load current sense
  - Input and output supply voltage
  - External FET temperature
  - Controller temperature
  - External FET Drain to source voltage
- Provides fault diagnostics through SPI and indication using the $\overline{\text{FLT/WAKE}}$ pin
  - Detection of open load and short-to-battery or FET short

2 Applications

- Power distribution box
- Body control module
- DC/DC converter
- Battery management system

3 Description

TPS12S24F-Q1 is a family of low I_Q smart dual high side drivers with protection and diagnostics. With a wide operating voltage range from 3.5V to 70V and a 80V absolute maximum rating the device is an excellent choice for 12V, 24V, and 48V automotive system designs.

It has two integrated gate drives with 0.5A source and 2A sink (GATEx). In low-power mode, the integrated low-power path is kept ON and the main FETs are turned OFF with I_Q of 35µA (typical). The device automatically switches to the active mode with main FETs (GATEx) ON when load current exceeds configurable load wakeup threshold and asserts $\overline{\text{FLT/WAKE}}$ low as wakeup indication to the MCU. Further, the device also includes various capacitive charging modes which can configured over SPI.

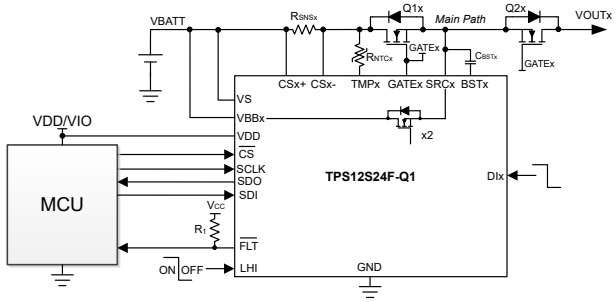
Diagnostics features include a digital bi-directional current with adjustable Bi-I2T based overcurrent and Bi-short circuit protection using an external R_{SNS} resistor, output voltage, input voltage, FET temperature sense, controller temperature and FET VDS sense that can be read over the SPI to diagnosis external FET and load failures.

The TPS12S24F-Q1 is available in a 30-pin VQFN package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS12S24F-Q1	RHB (VQFN, 30)	5.00mm × 5.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS12S24F-Q1 Application Circuit Driving PAAT Loads, B2B FETs

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4 Pin Configuration and Functions

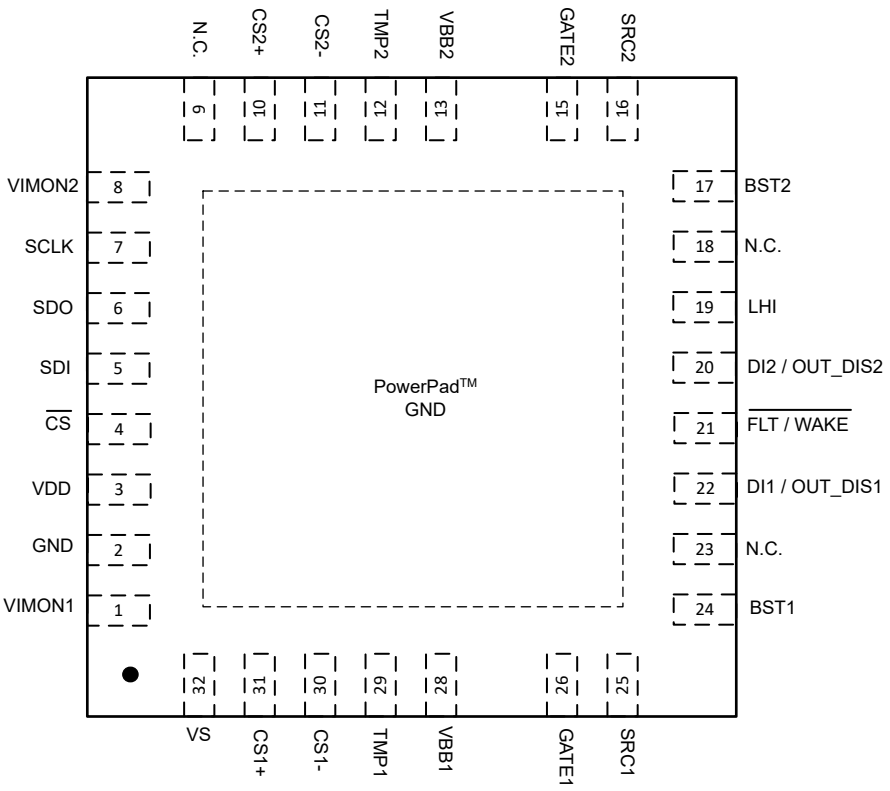


Figure 4-1. RHB Package, 30-Pin VQFN (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
VIMON1	1	O	Analog current monitoring output voltage for channel 1. Leave it floating or connect capacitor if unused.
GND	2	G	Connect GND to system ground.
VDD	3	P	Logic input supply. Connect 1µF capacitor to GND.
$\overline{CS}$	4	I	SPI chip select (active low). Internally pulled up to VDD.
SDI	5	I	SPI data input to the device.
SDO	6	O	SPI data output from the device. Internally pulled up to VDD.
SCLK	7	I	SPI clock input to the device.
VIMON2	8	O	Analog current monitoring output voltage for channel 2. Leave it floating or connect capacitor if unused.
N.C.	9	—	No connect. Leave floating or connect to input supply.

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Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CS2+	10	I	Main path current sense positive input for channel 2. Connect to input supply if unused.
CS2–	11	I	Main path current sense negative input for channel 2. Connect to input supply if unused.
TMP2	12	I	Temperature Input for channel 2. Analog connection to external NTC thermistor. Leave it floating if unused.
VBB2	13	I	Drain of integrated bypass FET for channel 2. Connect to input supply if unused.
GATE2	15	O	High current gate driver pull-up and pull-down for channel 2. 0.5A peak source and 2A sink capacity. This pin pulls GATE2 up to BST2 and down to SRC2. For the fastest tun-on and turn-off, tie this pin directly to the gate of the external high side MOSFET in main path. Leave it floating if unused.
SRC2	16	O	Source connection of the external FET for channel 2.
BST2	17	O	High side bootstrapped supply for channel 2. An external capacitor with a minimum value of 0.1µF must connect between this pin and SRC2. Voltage swing on this pin is 12V to (VS + 12V).
N.C.	18	—	No connect. Leave floating or connect to input supply.
LHI	19	I	Externally enables the LIMPHOME mode. Leave it floating or connect to ground if unused.
DI2 / OUT_DIS2	20	I	Controls GATE2 of channel 2 Configurable through EEPROM through DI_OUT_DIS_FN bit. If programmed as **DI**: Sets the output behavior in the LIMP HOME mode, if configured through the CHx_LH_IN bits If programmed as **OUT_DIS**: Pulls GATE2 to SRC2 if asserted high Leave it floating or connect to ground if unused.
$\overline{\text{FLT}}$ /$\overline{\text{WAKE}}$	21	O	Open drain fault or WAKE output. This pin asserted low by device when device enters into active mode (when LPM_ENTRY bit is low or when a load wakeup event has occurred).
DI1 / OUT_DIS1	22	I	Controls GATE1 of channel 1 Configurable through EEPROM through DI_OUT_DIS_FN bit. If programmed as **DI**: Sets the output behavior in the LIMP HOME mode, if configured through the CHx_LH_IN bits If programmed as **OUT_DIS**: Pulls GATE1 to SRC1 if asserted high. Leave it floating or connect to ground if unused.
N.C.	23	—	No connect. Leave floating or connect to input supply.
BST1	24	O	High side bootstrapped supply for channel 1. An external capacitor with a minimum value of 0.1µF must connect between this pin and SRC1. Voltage swing on this pin is 12V to (VS + 12V).
SRC1	25	O	Source connection of the external FET for channel 1.
GATE1	26	O	High current gate driver pull-up and pull-down for channel 1. 0.5A peak source and 2A sink capacity. This pin pulls GATE1 up to BST1 and down to SRC1. For the fastest tun-on and turn-off, tie this pin directly to the gate of the external high side MOSFET in main path

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Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VBB1	28	I	Drain of integrated bypass FET for channel 1. Connect to input supply if unused.
TMP1	29	I	Temperature input for channel 1. Analog connection to external NTC thermistor. Leave it floating if unused.
CS1–	30	I	Main path current sense negative input for channel 1. Connect to input supply if unused.
CS1+	31	I	Main path current sense positive input for channel 1. Connect to input supply if unused.
VS	32	P	Supply Pin of the controller.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input pins	CSx+, CSx–, TMPx, SRCx, LHI, DIx / OUT_DISx to GND	–40	80	V
Input pins	VBBx, VS to GND	–0.3	80	V
Input pins	Maximum Voltage slew rate on drain side input pins (VBBx, VS, CSx+, CSx–, TMPx)		60	V/µs
Input pins	Maximum Voltage slew rate on SRCx		200	V/µs
Input pins	VBBx, VS, CSx+, CSx–, TMPx to SRCx	–2	80	V
Input pins	GATEx, BSTx to SRCx	–0.3	19	V
Input pins	CSx+ to CSx–	–0.3	0.3	V
Input pins	CSx+ to CSx– for 100µs	–0.6	0.6	V
Input pins	CS1+ to CS2+, CS1– to CS2–	–0.3	0.3	V
Input pins	CSx– to TMPx	–0.3	0.3	V
Input pins	VDD, $\overline{CS}$, SCLK, SDI to GND	–0.3	5.5	V
Output pins	$\overline{FLT}$ / $\overline{WAKE}$ to GND	–0.3	80	V
Output pins	SDO, VIMONx to GND	–0.3	5.5	V
Output pins	GATEx, BSTx to GND	–40	100	V
Sink current	$I_{(CSx+)}$ to $I_{(CSx–)}$, 1msec		100	mA
Operating junction temperature, T_j(2)		–40	150	°C
Storage temperature, T_{stg}		–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins ()	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input pins	CSx+, CSx–, TMPx, SRCx, LHI, DIx / OUT_DISx to GND	–40		70	V
Input pins	VBBx VS to GND	0		70	V
Input pins	VDD	3		5.5	V
Input pins	$\overline{CS}$, SCLK, SDI to GND	0		5.5	V
Output pins	SDO, VIMONx to GND	0		5.5	V
Output pins	$\overline{FLT}$ / $\overline{WAKE}$ to GND	0		70	V
Tj	Operating Junction temperature(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

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(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC(1)		TPS12S24F-Q1 RHB 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx\ –\ SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VS) and DIGITAL SUPPLY VOLTAGE (VDD)						
VBB, VS	Operating input voltage		3.5		70	V
$V_{(VS_PORR)}$	Input supply POR threshold, rising			3		V
$V_{(VS_PORF)}$	Input supply POR threshold, falling			2.5		V
$V_{(VDD_PORR)}$	VDD supply POR threshold, rising			2		V
$V_{(VDD_PORF)}$	VDD supply POR threshold, falling			1.45		V
$I_{(GND)}$	Total system quiescent current for both channels	$V_{(VDD)}$ = 5.5V, Active mode		3.5		mA
		$V_{(VDD)}$ = 3V, Active mode		3.5		mA
$I_{(VDD)}$	VDD supply current	$V_{(VDD)}$ = 5.5V, Active mode		1		mA
		$V_{(VDD)}$ = 3V, Active mode		50		µA
$I_{(GND)}$	Total system quiescent current for both channels	$V_{(VDD)}$ = 0V, Low power mode		35		µA
$I_{(GND)}$	Sleep mode ground current	Sleep mode $V_{(SRCx)}$ = 0V, $V_{(VDD)}$ = 0V		2		µA
UNDERVOLTAGE LOCKOUT (UVLO) AND OVERVOLTAGE (OV) PROTECTION						
$V_{CHx(UVLOF)}$	VBB UVLO (CS1+ pin) falling threshold voltage range	UVLO_SET_CHx bits to set VBB UVLO falling threshold	4.5		32	V
$V_{CHx(OVR)}$	VBB OVLO (CS1+ pin) rising threshold voltage range	OVLO_SET_CHx bits to set VBB OVLO rising threshold	16		72	V
CHARGE PUMP (BSTx–SRCx)						
$I_{CHx(BST_AM)}$	Charge Pump Supply current in active mode	$V_{(BSTx\ –\ SRCx)}$ = 10V, Active mode		600		µA
$V_{CHx(BST_UVLOR)}$	$V_{(BSTx\ –\ SRCx)}$ UVLO voltage threshold, rising	Active mode		9		V
$V_{CHx(BST_UVLOF)}$	$V_{(BSTx\ –\ SRCx)}$ UVLO voltage threshold, falling	Active mode		8		V
$VCP_{CHx(LOW_AM)}$	Charge pump turn on voltage in active mode	Active mode		12.5		V
$VCP_{CHx(HIGH_AM)}$	Charge pump turn off voltage in active mode	Active mode		13.5		V
$VCP_{CHx(AM_VS_3V)}$	Charge pump voltage at $V_{(VS)}$ = 3V	Low power and active mode		8		V
$V_{CHx(GATE_GOOD)}$	GATEx Drive Good rising threshold			6		V
GATE DRIVER OUTPUTS (GATEx, Gx)						

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5.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx – SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CHx(GATE_PU)}$	Peak source current			0.5		A
$I_{CHx(GATE_PD)}$	Peak sink current			2		A
$I_{CHx(GATE_PU_INRUSH)}$	Gate charge (sourcing) current during cap charging	CAP_CHRG_CHx = 0x1		100		µA
CURRENT SENSE AND CURRENT MONITOR (CSx+, CSx–, VIMONx)						
$V_{CHx(VSNS_Range)}$	Voltage range across external current sense resistor R_{SNSx}		0		200	mV
$V_{CHx(ISNS_GAINx)}$	Current sense gain setting	ISNS_GAIN_CHx = 0x0		15		V/V
		ISNS_GAIN_CHx = 0x1		30		V/V
		ISNS_GAIN_CHx = 0x2		50		V/V
		ISNS_GAIN_CHx = 0x3		65		V/V
		ISNS_GAIN_CHx = 0x4		85		V/V
		ISNS_GAIN_CHx = 0x5		100		V/V
		ISNS_GAIN_CHx = 0x6		120		V/V
		ISNS_GAIN_CHx = 0x7		135		V/V
$V_{CHx(ISNS_Acc)}$	Target VIMONx accuracy in Production samples	±6mV ≤ V_{SNSx} < ±15mV	–5		5	%
		±15mV ≤ V_{SNSx} ≤ ±200mV	–2		2	%
$V_{CHx(ISNS_ADC_Acc)}$	Target Digital current sense accuracy in Production samples	±6mV ≤ V_{SNSx} < ±15mV	–7		7	%
		±15mV ≤ V_{SNSx} ≤ ±200mV	–2.5		2.5	%
VDS MONITORING AND PROTECTION (CSx-, SRCx)						
$V_{CHx(VDS_SNS)}$	VDS sense monitoring range over ADC		±50		±1850	mV
$V_{CHx(IVDS_GAINx)}$	VDS sense and protection gain setting	VDS_GAIN_CHx = 0x1		30		V/V
		VDS_GAIN_CHx = 0x2		8		V/V
		VDS_GAIN_CHx = 0x3		1.5		V/V
$V_{CHx(VDS_OVP)}$	VDS protection threshold range in 50mV steps	VDS_SET_CHx bits to set VDS protection threshold	±300		±1400	mV
INPUT VOLTAGE (CSx+) AND OUTPUT VOLTAGE (SRCx) SENSE MONITORING						
$V_{CH1(VBB_SNS)}$ $V_{CHx(VOUT_SNS)}$	Digital input (CS1+) and output voltage (SRCx) sense range		6		60	V
I2T BASED OVERCURRENT AND SHORT CIRCUIT PROTECTION						
$V_{CHx(VNOM)}$	I2T start VNOM threshold range	NOM_CUR_CHx bits to set VNOM threshold	3		75	mV
$V_{CHx(SCP)}$	SCP threshold range	FWD_SCP_SET_CHx and REV_SCP_SET_CHx bits	±10		±158	mV
$V_{CHx(SCP)_Acc}$	Target SCP threshold accuracy in Production samples	±20mV ≤ $V_{CHx(SCP)}$ ≤ ±158mV	–5		+5	%
ADC CHARACTERISTICS (ISNS, TSNS, VDS, VBB, VOUT, TCONT)						
	ADC Signals	ISNS1, ISNS2, TSNS1, TSNS2, VBB, VDS1, VDS2, VOUT1, VOUT2, TCONT				
V_{ADC_REF}	ADC reference voltage			2.8		V
I_{ADC}	ADC current consumption			0.5		mA
LOAD WAKEUP PATH CHARACTERISTICS (VBBx, SRCx)						
$V_{CHx(LPM_SCP)}$	Short-circuit threshold in LPM (VBBx to SRCx voltage)			2.5		V

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5.5 Electrical Characteristics (continued)

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx – SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CHx(LWUx)}$	Load wakeup current threshold 1			100		mA
	Load wakeup current threshold 2			200		mA
	Load wakeup current threshold 3			400		mA
	Load wakeup current threshold 4			780		mA
TEMPERATURE MONITOR (CSx–, TMPx)						
$V_{CHx(TSD)}$	NTC Threshold setting	TSNS_TSD_SET_CHx bits to set TSD protection threshold	45		160	℃
INPUT CONTROLS (LHI, DIx), & FAULT FLAG ($\overline{FLT}$)						
V_{LHI_H}, V_{DIx/OUT_DISx_H}	LHI, DIx/OUT_DISx pin rising threshold voltage			1.5		V
V_{LHI_L}, V_{DIx/OUT_DISx_L}	LHI, DIx/OUT_DISx pin falling threshold voltage			1.15		V
$R_{(\overline{FLT} / \overline{WAKE})}$	$\overline{FLT}$ / $\overline{WAKE}$ Pull-down resistance			100		Ω
$V_{CHx(STB_OL_TH)}$	Off state Open-load (OL) detection voltage			0.8		V
$I_{CHx(OL_OFF)}$	Off state open-load (OL) detection internal pull-up current setting 1			33		µA
	Off state open-load (OL) detection internal pull-up current setting 2			54		µA
	Off state open-load (OL) detection internal pull-up current setting 3			130		µA
	Off state open-load (OL) detection internal pull-up current setting 4			254		µA
$I_{CHx(SHRT_VBB)}$	Off state SRCx pulldown current			4		mA
$T_{CHx(TSDR_BYP_FET)}$	Bypass FET thermal shutdown, rising			165		℃
$T_{CHx(TSDF_BYP_FET)}$	Bypass FET thermal shutdown, falling			140		℃
$T_{(CONT_TSD_WRN)}$	Controller overtemperature warning threshold			135		℃
DIGITAL INPUT PIN CHARACTERISTICS ($\overline{CS}$, SCLK, SDI)						
$V_{IH, DIG}$	DIG pin Input voltage high-level	3.0V ≤ VDD ≤ 5.5V	0.7x V_{VDD}			V
$V_{IL, DIG}$	DIG pin Input voltage low-level	3.0V ≤ VDD ≤ 5.5V			0.3x V_{VDD}	V
R_{DIGx}	Internal pulldown resistor			1.0		MΩ
$I_{IH, DIG}$	Input current high-level	V_{DIG} = 5V		5		µA
DIGITAL OUTPUT PIN CHARACTERISTICS (SDO)						
V_{OH_SDO}	Output Logic High Voltage drop	SDO Pin current = 2mA		0.2		V

5.6 Switching Characteristics

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx – SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GATEx(DIx_H)}$	DIx turn on propagation delay	DIx ↑ to GATEx ↑, $C_{L(GATEx)}$ = 47nF		4		µs
$t_{GATEx(DIx_L)}$	DIx turn off propagation delay	DIx ↓ to GATEx ↓, $C_{L(GATEx)}$ = 47nF		4		µs
$t_{GATEx(DIx_H)}$	OUT_DISx turn off propagation Delay	OUT_DISx ↑ to GATEx ↓, $C_{L(GATEx)}$ = 47nF		2		µs

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5.6 Switching Characteristics (continued)

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx – SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GATEx(DIx_L)}$	OUT_DISx turn on propagation Delay	OUT_DISx ↓ to GATEx ↑, $C_{L(GATEx)}$ = 47nF		4		µs
t_{DIx_MASK}	DIx / OUT_DISx masking time setting	CONFIG_DI_MASK = 0x1		8.5		µs
		CONFIG_DI_MASK = 0x2		12		µs
		CONFIG_DI_MASK = 0x3		23		µs
$t_{(LHI_H)}$	LHI going high to Limphome mode propagation Delay	LHI ↑ to GATEx ↓, C_L = 47nF CHx_LH_IN = 0x2 CONFIG_LHI_MASK = 0x0		4		µs
$t_{(LHI_L)}$	LHI going low to active mode propagation delay	LIMP_STAT bit ↓ to GATEx ↑, C_L = 47nF CHx_LH_IN = 0x2 CONFIG_LHI_MASK = 0x0		4		µs
t_{LHI_MASK}	LHI masking time setting	CONFIG_LHI_MASK = 0x1		10		µs
		CONFIG_LHI_MASK = 0x2		12		µs
		CONFIG_LHI_MASK = 0x3		23		µs
$t_{Gx_ON(LPMx)}$	Active mode to LPM mode transition delay	LPM_ENTRY = '0' to '1' to $V_{(Gx)}$ > $V_{(Gx_GOOD)}$ AUTO_LPM_ENTRY = 0x0 (disabled)		10		µs
$t_{GATEx_OFF(LPMx)}$	Active mode to LPM mode transition delay	LPM_ENTRY = '0' to '1' $V_{(Gx)}$ > $V_{(Gx_GOOD)}$ to $V_{(GATEx)}$ < $V_{(GATEx_GOOD)}$, $C_{L(GATEx)}$ = 47nF AUTO_LPM_ENTRY = 0x0 (disabled)		200		µs
$t_{GATEx(WAKE_LPMx)}$	LPM Mode to Active mode transition delay with LPM bit	LPM = '0' to '1' to $V_{(GATEx)}$ > $V_{(GATEx_GOOD)}$, $C_{L(GATEx)}$ = 47nF AUTO_LPM_ENTRY = 0x0 (disabled)		50		µs
$t_{Gx(WAKE_LPMx)}$	LPM Mode to Active mode transition delay with LPM bit	$V_{(GATEx)}$ > $V_{(GATEx_GOOD)}$ to $V_{(Gx)}$ < $V_{(Gx_GOOD)}$ AUTO_LPM_ENTRY = 0x0 (disabled)		30		µs
$t_{GATEx(WAKE_LWUx)}$	GATEx turn ON propagation delay 1 during Load wakeup	$I_{CHx(LOAD)}$ ↑ $I_{CHx(LWUx)}$ to GATEx ↑, $C_{L(GATEx)}$ = 47nF LPM_EXIT_CURR_CHx = 0x0 **LOAD_WAKE_DEGLITCH = 0x0** AUTO_LPM_ENTRY = 0x0 (disabled)		7.5		µs
$t_{GATEx(WAKE_LWUx_MASK)}$	Load wakeup masking time	**LOAD_WAKE_DEGLITCH = 0x1** AUTO_LPM_ENTRY = 0x0 (disabled)		50		µs
$t_{Gx(WAKE_LWUx)}$	Gx turn OFF propagation delay during Load wakeup	ILOADx ↑ $I_{(LWU)}$, GATE ↑ (above $V_{(G_GOOD)}$) to $V_{(Gx)}$ < $V_{(Gx_GOOD)}$, $C_{L(G)}$ = 1nF LPM_EXIT_CURR_CHx = 0x0 LOAD_WAKE_DEGLITCH = 0x0 AUTO_LPM_ENTRY = 0x0 (disabled)		30		µs
$t_{GATEx(UVLOx_OFF)}$	UVLO turn off propagation delay	$V_{(CSx+)}$ < $V_{CHx(UVLOF)}$ to GATEx ↓, $C_{L(GATEx)}$ = 47nF UVLO_MASK_CHx = 0x0		5		µs
$t_{CHx(UVLO_MASK)}$	UVLO masking time setting	UVLO_MASK_CHx = 0x1		6		µs
		UVLO_MASK_CHx = 0x2		45		µs
		UVLO_MASK_CHx = 0x3		175		µs
$t_{GATEx(OVx_OFF)}$	OV Turn OFF Propagation Delay	$V_{(CSx+)}$ > $V_{CHx(OVR)}$ to GATEx ↓, $C_{L(GATEx)}$ = 47nF OVLO_MASK_CHx = 0x0		5		µs

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5.6 Switching Characteristics (continued)

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx\ –\ SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CHx(OV_MASK)}$	OV masking time setting	OVLO_MASK_CHx = 0x1		6		µs
		OVLO_MASK_CHx = 0x2		45		µs
		OVLO_MASK_CHx = 0x3		175		µs
$t_{CHx(VDS_DELAY)}$	VDS protection propagation delay	VDS_MASK_CHx = 0x0 VDS_GAIN_CHx = 0x1		15		µs
$t_{CHx(VDS_MASK)}$	VDS protection mask time setting	VDS_MASK_CHx = 0x1		5		µs
		VDS_MASK_CHx = 0x2		45		µs
		VDS_MASK_CHx = 0x3		245		µs
$t_{CHx(TSNS_DELAY)}$	External FET overtemperature (TSD) protection propagation delay	TSNS_TSD_MASK_CHx = 0x0		1		µs
$t_{CHx(TSNS_MASK)}$	TSD protection mask time setting	TSNS_TSD_MASK_CHx = 0x1		7.5		µs
		TSNS_TSD_MASK_CHx = 0x2		50		µs
		TSNS_TSD_MASK_CHx = 0x3		500		µs
$t_{GATEx(VS_OFF)}$	GATEx turn off propogation delay with VS falling < $V_{(VS_PORF)}$	$V_{(VS)}$ ↓ < $V_{(VS_PORF)}$ to GATEx ↓, $C_{L(GATEx)}$ = 47nF		50		µs
t_{OC}	I2T protection delay accuracy for Production samples		–15		15	%
t_{SC}	Short circuit protection propagation delay	$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCPx)}$ to GATEx ↓, C_L = 47nF $V_{(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x0 REV_SCP_MASK_CHx = 0x0		1.1		µs

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5.6 Switching Characteristics (continued)

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx\ –\ SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SC_MASK}	Short circuit protection masking time setting	$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCP)}$ to GATEx ↓, C_L = 47nF $V_{CHx(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x1 REV_SCP_MASK_CHx = 0x1		4		µs
		$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCP)}$ to GATEx ↓, C_L = 47nF $V_{CHx(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x2 REV_SCP_MASK_CHx = 0x2		9		µs
		$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCP)}$ to GATEx ↓, C_L = 47nF $V_{CHx(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x3 REV_SCP_MASK_CHx = 0x3		24		µs
		$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCP)}$ to GATEx ↓, C_L = 47nF $V_{CHx(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x4 REV_SCP_MASK_CHx = 0x4		44		µs
		$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCP)}$ to GATEx ↓, C_L = 47nF $V_{CHx(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x5 REV_SCP_MASK_CHx = 0x5		89		µs
		$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCP)}$ to GATEx ↓, C_L = 47nF $V_{CHx(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x6 REV_SCP_MASK_CHx = 0x6		134		µs
		$V_{(CSx+–CSx-)}$ ↑ $V_{CHx(SCP)}$ to GATEx ↓, C_L = 47nF $V_{CHx(SCP)}$ = 20mV FWD_SCP_MASK_CHx = 0x7 REV_SCP_MASK_CHx = 0x7		179		µs
t_{LPM_SC}	Short circuit protection propagation delay in LPM (short in LPM)	$V_{(VBBx–SRCx)}$ ↑ $V_{(Hx(LPM_SCP)}$ to GATEx ↑, $C_{L(GATEx)}$ = 47nF		10		µs
$t_{GATEx_OFF(RPP)}$	GATEx turn off delay during reverse polarity event when $V_{(BSTx)}$ > $V_{(BSTx_UVLOF)}$	$V_{(CSx+)}$ = 12 to –14V to GATEx ↓, $C_{L(GATEx)}$ = 47nF, C_{BST} = 470nF		10		µs
t_{AUTO_RETRY}	Auto retry time setting	AUTO_RETRY_DURATION_CHx = 00		1		ms
		AUTO_RETRY_DURATION_CHx = 01		10		ms
		AUTO_RETRY_DURATION_CHx = 10		100		µs
t_{AUTO_RETRY}	Auto retry time setting	AUTO_RETRY_DURATION_CHx = 11		100		ms
f_{CHx_PWM}	PWM frequency setting	PWM_EN = 1, PWM_FREQ_CHx = 000		1		Hz
		PWM_EN = 1, PWM_FREQ_CHx = 111		1770		Hz
$t_{WATCHDOG}$	Watchdog timeout configuration	WD_EN = 1, WD_TO = 00		520		µs
		WD_EN = 1, WD_TO = 01		400		ms
		WD_EN = 1, WD_TO = 10		800		ms
		WD_EN = 1, WD_TO = 11		1200		ms
$t_{GATEx(\overline{FLTx}_ASSERT)}$	$\overline{FLT}$ assertion delay			1		µs

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5.6 Switching Characteristics (continued)

T_J = –40°C to +150°C. $V_{(VBBx)}$ = $V_{(VS)}$ = 6 to 70V, $V_{(BSTx – SRCx)}$ = 12V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(ISNS_POL_DELAY)}$	Delay for current direction indication on ISNS_POLARITY bit	$V_{(SNSx)}$ ↑ or ↓ to ISNS_POLARITY_CHx ↑ or ↓ $V_{(SNSx)}$ = 30 to –30mV		10		µs

5.7 SPI Timing Requirements

Over operating junction temperature T_J = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{READY}	Initialization time for digital				65	µs
f_{SPI}	SPI clock (SCLK) frequency	C_{SDO} = 30pF, IO protection resistor kΩ			10	MHz
t_{high}	High time: SCLK logic high-time duration		45			ns
t_{low}	Low time: SCLK logic low-time duration		45			ns
t_{sucs}	$\overline{CS}$ setup time: time delay between falling edge of $\overline{CS}$ and rising edge of SCLK		45			ns
t_{su_SDI}	SDI setup time: setup time of SDI before the falling edge of SCLK		15			ns
t_{h_SDI}	SDI hold time: hold time of SDI before the falling edge of SCLK		30			ns
t_{d_SDO}	Delay time: time delay from rising edge of SCLK to data valid at SDO				30	ns
t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of $\overline{CS}$		45			ns
t_{dis_cs}	$\overline{CS}$ disable time, $\overline{CS}$ high to SDO high impedance			10		ns
t_{hics}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high		500			ns

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6 Parameter Measurement Information

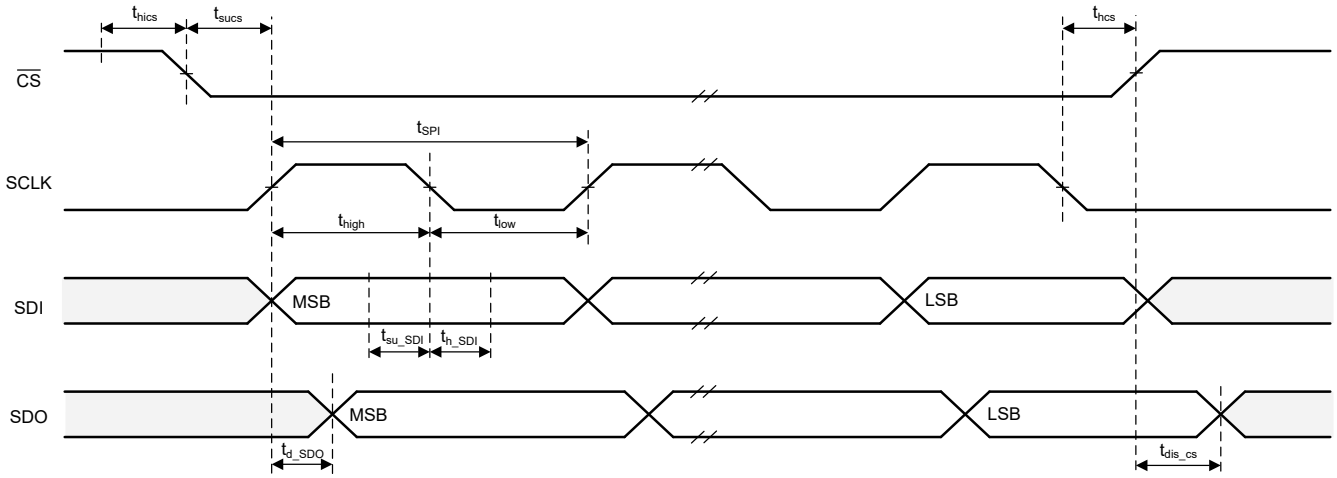


Figure 6-1. SPI Timing Characteristics Definitions

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7 Detailed Description

7.1 Overview

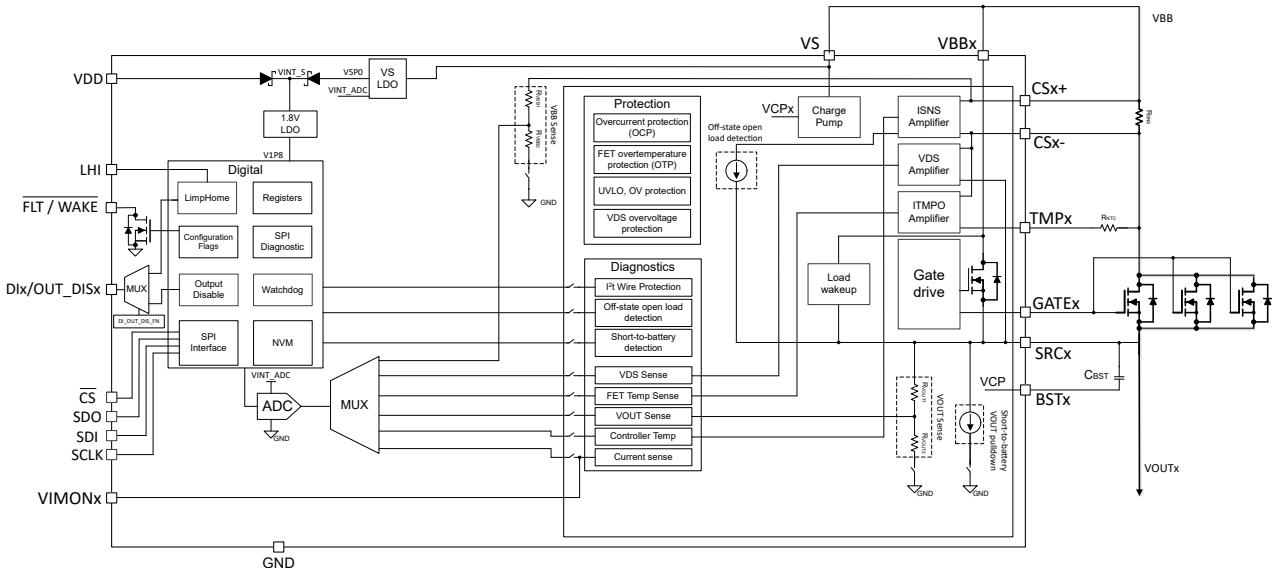
TPS12S24F-Q1 is a family of low I_Q smart dual high side drivers with protection and diagnostics. With a `wide operating voltage range from 3.5V to 70V and a 80V absolute maximum rating the device is an excellent choice for 12V, 24V, and 48V automotive system designs.

It has two integrated gate drives with 0.5A source and 2A sink (GATEx). In low-power mode, the integrated low-power path is kept ON which can allow load current up to 780mA and the main FETs are turned OFF with I_Q of 35µA (typical). The device automatically switches to the active mode with main FETs (GATEx) ON when load current exceeds configurable load wakeup threshold and asserts $\overline{\text{FLT / WAKE}}$ low as wakeup indication to the MCU. Further, the device also includes various capacitive charging modes which can configured over SPI.

Protection and Diagnostics features include a digital bi-directional current with adjustable I2T based overcurrent and short circuit protection using an external R_{SNS} resistor, output voltage, input voltage, FET temperature sense, controller temperature and FET VDS sense that can be read over the SPI to diagnosis external FET and load failures. Auto-retry and latch-off fault behavior is configurable.

The TPS12S24F-Q1 is available in a 30-pin VQFN package.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Supply Input

The device works with two power supply inputs – a chip supply input (VS) and a low voltage digital supply input (VDD) typically generated with a DC-DC converter or LDO external to the device. The low voltage digital supply input (5V or 3.3V) is used for SPI supply matching the I/O supply of the MCU.

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7.3.2 Charge Pump and Gate Driver Output (VS, GATEx, BSTx, SRCx)

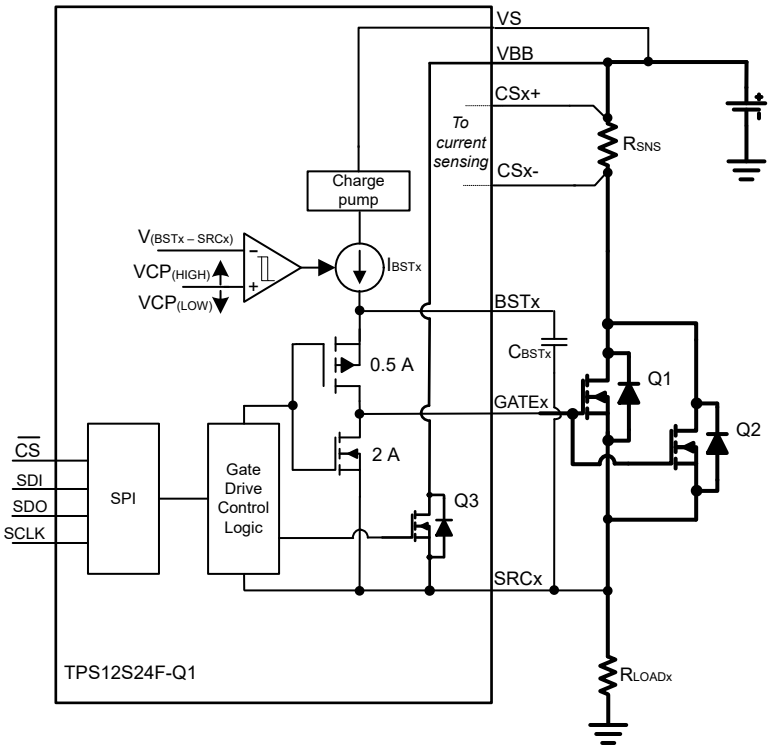


Figure 7-1. Gate Driver

Figure 7-1 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 0.5A/2A peak source/sink gate driver (GATEx) for main FETs Q1, Q2. The bypass FET (Q3) is integrated in TPS12Sx4F-Q1. The strong gate drivers for main path enable paralleling of FETs in high power system designs establishing minimum transition time in saturation region. A 12V, 600µA charge pump is derived from VS terminal and charges the external bootstrap capacitor, C_{BSTx} that is placed across the gate driver (BSTx and SRCx).

VS is the supply pin to the controller. With VS applied and VDD above $V_{(VDD_PORR)}$, the charge pump turns ON whenever $\overline{CS}$ is pulled low and charges the C_{BSTx} capacitor. After the voltage across C_{BSTx} crosses $V_{(BST_UVLOR)}$, the GATE driver block is activated. The device has a 1V (typical) UVLO hysteresis to establish chattering less performance during initial GATEx turn ON. Select C_{BSTx} based on the external FET Q_G and allowed dip during FET turn ON. In active mode, the charge pump remains enabled until the BSTx to SRCx voltage reaches $VCP_{CHx(HIGH_AM)}$, typically, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BSTx to SRCx voltage discharges to $VCP_{CHx(LOW_AM)}$ typically at which point the charge pump is enabled.

The voltage between BSTx and SRCx continue to charge and discharge between $VCP_{CHx(HIGH_AM)}$ and $VCP_{CHx(LOW_AM)}$ in active mode as shown in the Figure 7-2.

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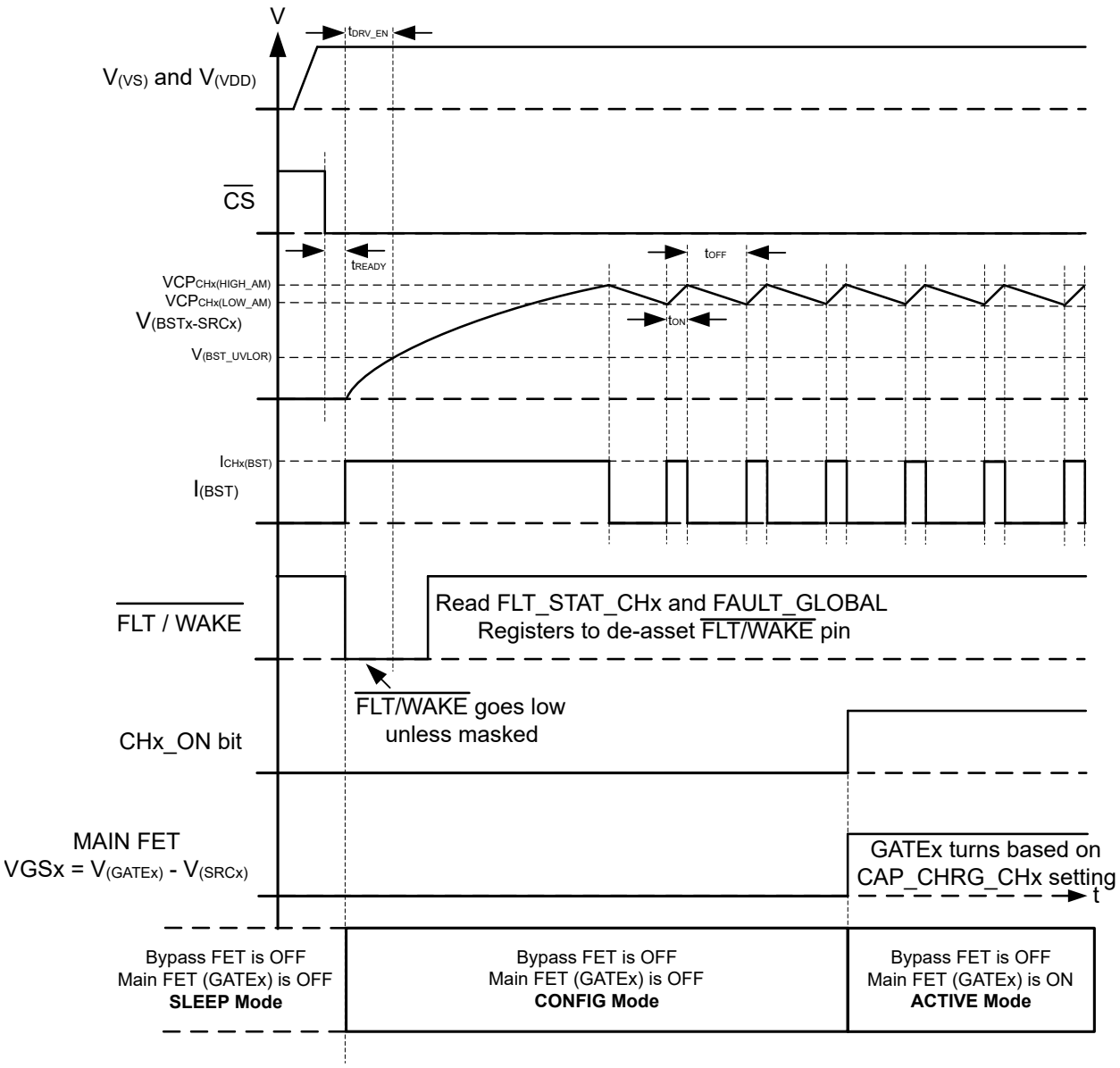


Figure 7-2. Charge Pump Operation

Use the following equation to calculate the initial gate driver enable delay:

$$t_{DRV_ENx} = \frac{C_{BSTx} \times V_{CHx(BST_UVLOR)}}{I_{CHx(BST)}} \quad (1)$$

Where

- C_{BSTx} is the charge pump capacitance connected across BSTx and SRCx pins
- $V_{CHx(BST_UVLOR)}$ = 9V (typical)
- $I_{CHx(BST)}$ is the chare pump current (600µA typical)

In switching applications, if the charge pump supply demand is higher than $I_{CHx(BST)}$, then supply BSTx can be externally supplied using a low leakage diode (D1x) and VAUX supply as Figure 7-3 shows.

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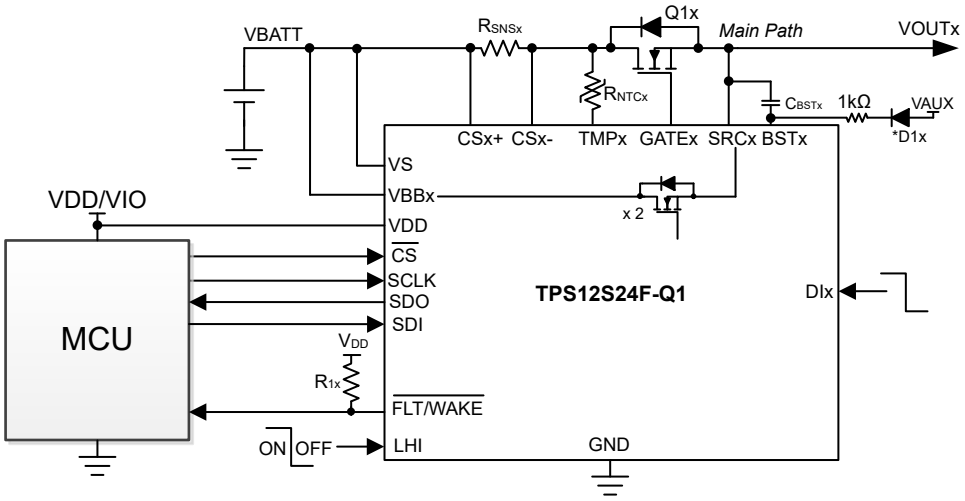


Figure 7-3. TPS12SxxF-Q1 Application Circuit With External Supply to BSTx

Note

V_{AUX} can be supplied by external supply ranging from 8.1V to 15V. Input supply VBB or VS can also connect to BSTx through the D1 diode to reduce T_{DRV_EN}.

7.3.3 Driving Capacitive, Resistive and Inductive Loads

All off-board loads have different type. Each load profile interacts differently with the Smart High Side Switch or Controller and require different considerations to specify robust protection. Whether the load is resistive, capacitive, inductive, or does not fall neatly into one of those categories such as LEDs changes how driving the load must be approached and designed. The user must understand what load profile is expected, and then understand how that impacts the design of the output stage.

Table 7-1. Load Driving Using TPS12SxxF-Q1

TYPE OF LOAD	LOAD DRIVING METHOD	REGISTER SETTING
Capacitive Load, CAP_CHRG_CHx = 0x0, 0x1 or 0x3	Using Short-circuit protection (SCP) based auto-retry method	CAP_CHRG_CHx = 0x0 INRUSH_DURATION_CHx = 0x0 to 0x7 *(used only for VOUT_ERR_CHx indication)* FWD_SCP_SET_CHx = 0x0 to 0xF AUTO_RETRY_DURATION_CHx = 0x0 to 0x3 LATCH_CHx = 0x0 FOLDBACK_LOCK_DIS_CHx = 0x1
	Using main path gate slew control	CAP_CHRG_CHx = 0x1 INRUSH_DURATION_CHx = 0x0 to 0x7 *(used only for VOUT_ERR_CHx indication)*
	Using main path PWM mode	CAP_CHRG_CHx = 0x3, PWM_DTY_CHx = 0x00 to 0xFF and PWM_FREQ_CHx = 0x0 to 0xF INRUSH_DURATION_CHx = 0x0 to 0x7
Resistive or Inductive Load	Using main path PWM method	CAP_CHRG_CHx = 0x0 PWM_EN_CHx = 0x1, PWM_DTY_CHx = 0x00 to 0xFF to and PWM_FREQ_CHx = 0x0 to 0xF

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7.3.3.1 Capacitive Load Driving

Certain end equipment like automotive power distribution unit and zonal controller power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur and potentially damaging the power FETs. Table 7-1highlights different capacitor charging methods supported by TPS12SxxF-Q1 family.

7.3.3.1.1 Using SCP Based Auto-Retry Method (GATEx):

TPS12SxxF-Q1 has integrated short-circuit protection (SCP) threshold setting using FWD_SCP_SET_CHx bits along with auto-retry time setting using AUTO_RETRY_DURATION_CHx bits which is used for controlling GATEx during capacitive load driving. Figure 7-7 shows application circuit for driving capacitive load using SCP based auto-retry method. See also Table 7-1 for all configurable parameters during this mode.

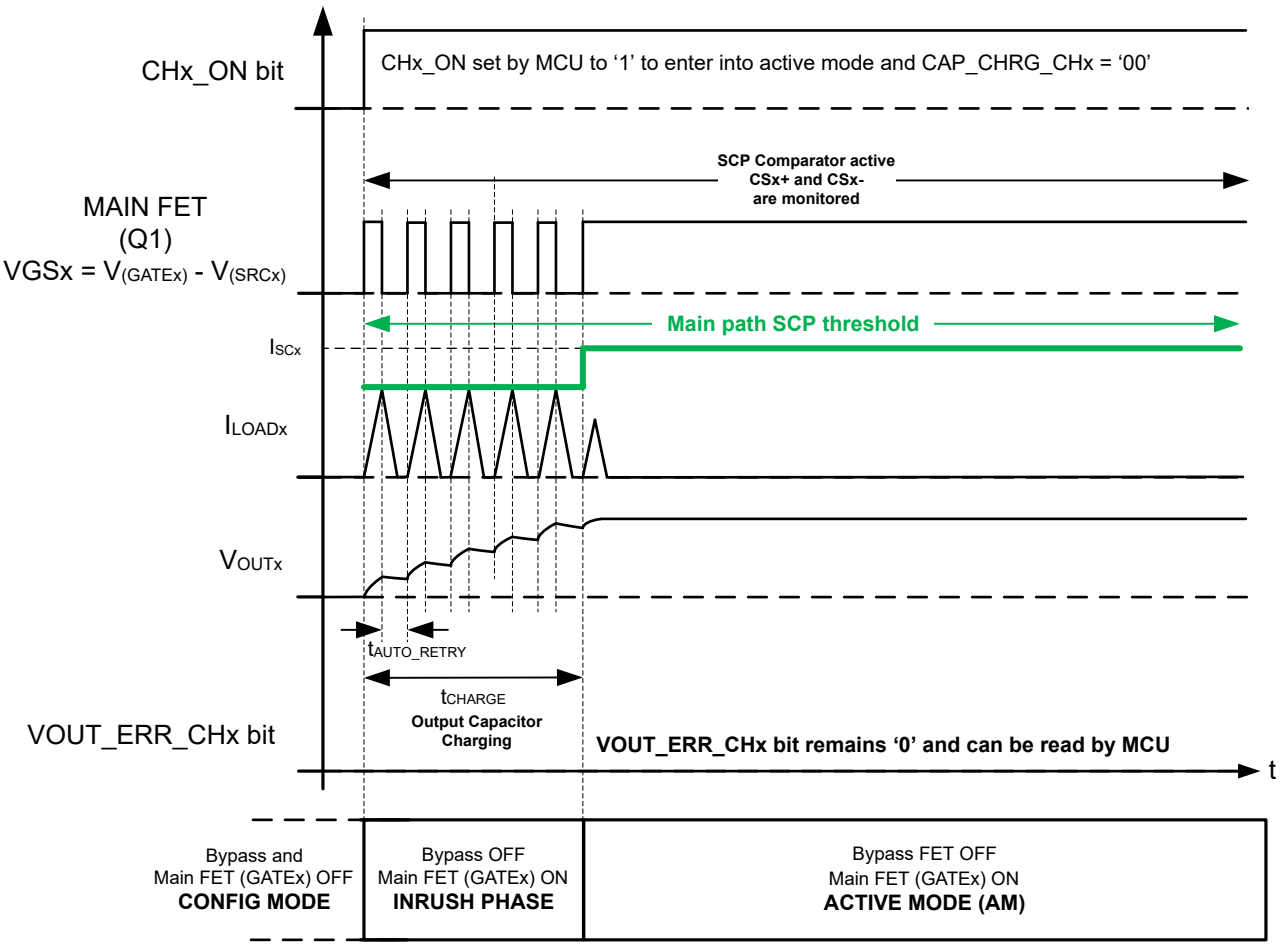


Figure 7-4. Timing Diagram For Bulk Capacitor Charging Using SCP Based Auto-Retry Method

VOUT_ERR_CHx bit is an indication bit for GATEx being ON/OFF after set INRUSH_DURATION_CHx. The device does not take any action based on this bit. If the bulk capacitor takes more than 100ms (maximum inrush duration setting) to precharge to desired output voltage then device continues to charge bulk capacitor even after 100ms inrush duration. The VOUT_ERR_bit is set '1' after set inrush duration which can be ignored by microcontroller.

7.3.3.1.2 Using Main Path Gate Slew Rate Control Method (GATEx, SRCx):

In the applications where low-power bypass path is not used, the cap charging can be done using main FET GATE drive control.

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For limiting inrush current during turn ON of the main FET with capacitive loads, use R_{GATEx} and C_{GATEx} as shown in Figure 7-5. The R_{GATEx} and C_{GATEx} components slow down the voltage ramp rate at the gate of main FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

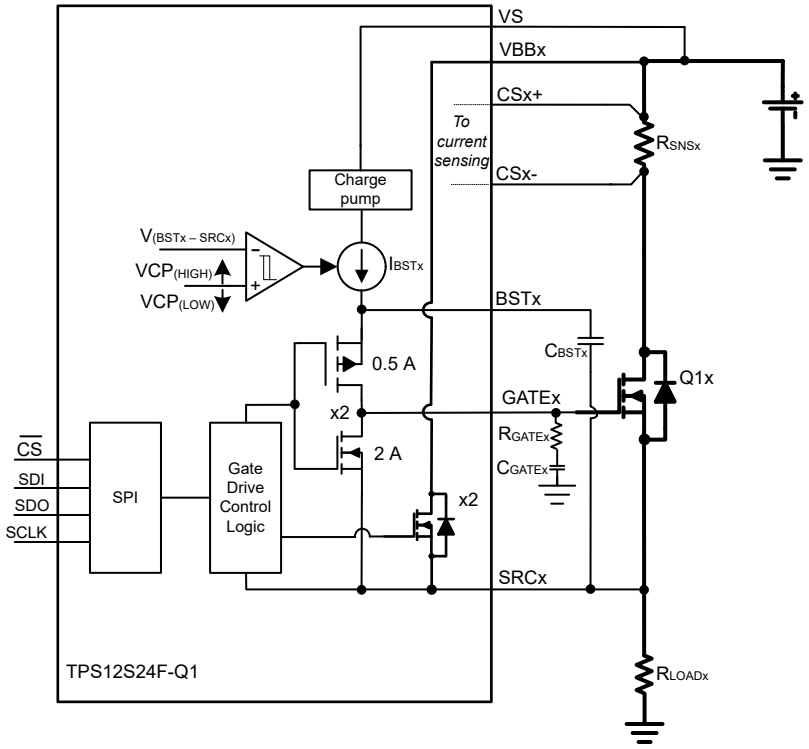


Figure 7-5. Gate Slew Rate Control in Main Path

In Config mode, when CHx_ON bit is set to '1 ' with CAP_CHRG_CHx bit set as “10”, the device turns ON main FET (GATEx) by pulling GATEx high with $I_{CHx(GATE_PU_INRUSH)}$ of source current and the bypass FET is kept OFF. GATEx drive current is increased to $I_{CHx(GATE_PU)}$ after VGS has reached $V_{CHx(GATE_GOOD)}$ threshold. VOUT_ERR_CHx bit is set to '1' by device after inrush duration set by INRUSH_DURATION_CHx bits if VGS sensed across GATEx and SRCx pins is less than $V_{CHx(GATE_GOOD)}$ threshold and can be read by MCU over SPI.

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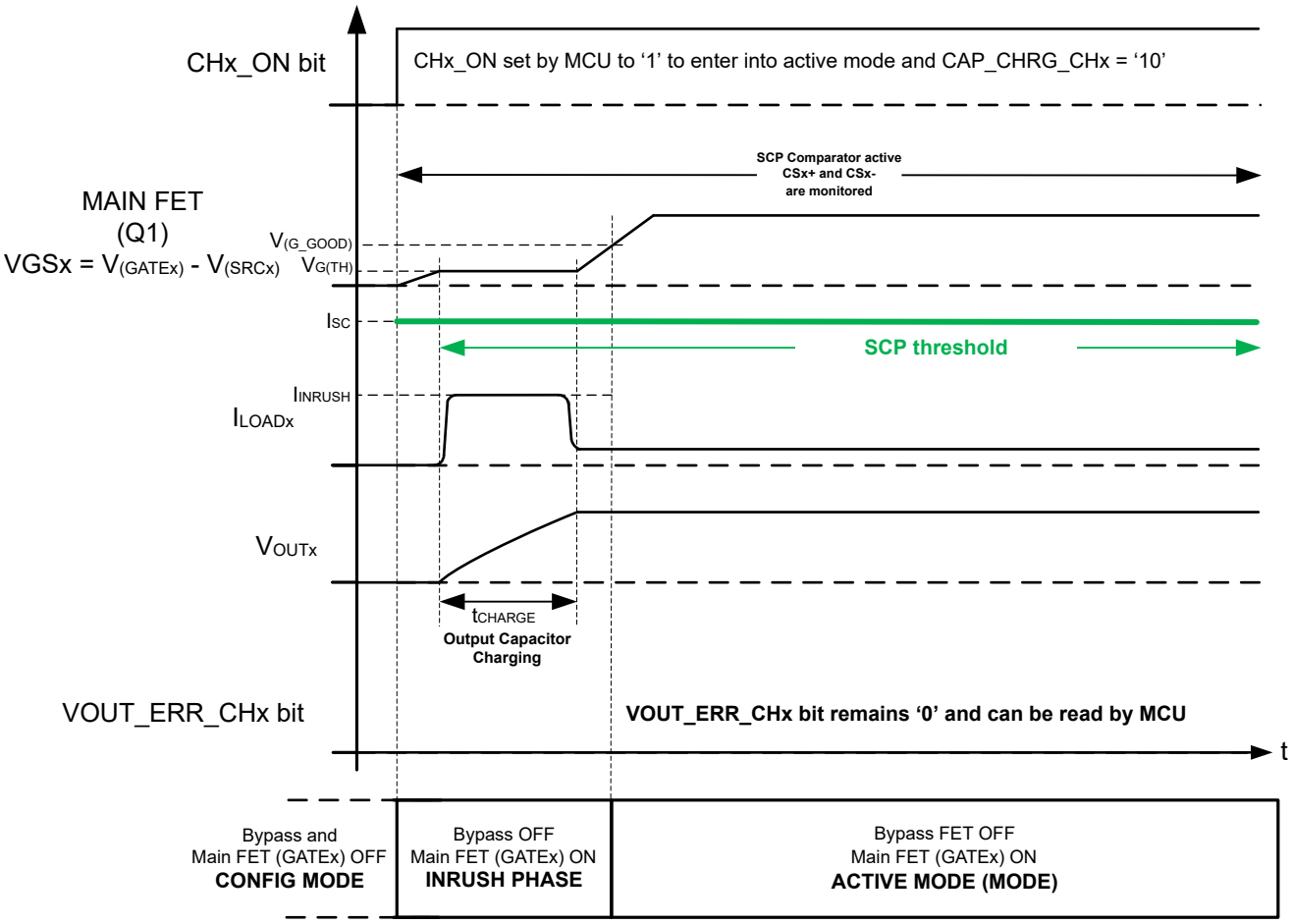


Figure 7-6. Timing Diagram for Bulk Capacitor Charging Using Main Path Gate Slew Rate Control

VOUT_ERR_CHx bit is an indication bit for GATEx being ON/OFF after set INRUSH_DURATION_CHx. The device does not take any action based on this bit. If the bulk capacitor takes more than 100ms (max inrush duration setting) to pre-charge to desired output voltage then device continues to charge bulk capacitor even after 100ms inrush duration. The VOUT_ERR_bit will be set '1' after set inrush duration which can be ignored by microcontroller.

7.3.3.1.2.1 Setting the INRUSH Current

Use Equation 2 to calculate the I_{INRUSH}:

$$I_{INRUSHx} = C_{LOADx} \times \frac{V_{BATT}}{t_{CHARGEx}} \quad (2)$$

Where

- C_{LOADx} is the load capacitance
- V_{BATT} is the input voltage
- $t_{chargex}$ is the charge time

Use Equation 3 to calculate the required C_{GATEx} value.

$$C_{GATEx} = \frac{C_{LOADx} \times I_{CHx(GATE_PU_INRUSH)}}{I_{INRUSHx}} \quad (3)$$

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Where

- $I_{CHx(GATE_PU_INRUSH)}$ is 100µA (typical)
- C_{LOADx} is the load capacitance
- VBATT is the input voltage
- $t_{CHARGEx}$ is the charge time

Use a series resistor R_{GATEx} in conjunction with C_{GATEx} to limit the discharge current from C_{GATEx} during turn off. The recommended value for R_{GATEx} is from 220Ω to 470Ω.

7.3.3.1.2.2 Sizing CBSTx Capacitor

C_{GATEx} results in an additional loading on C_{BSTx} to charge during turn-ON. Use Equation 4 to calculate the required C_{BSTx} value:

$$C_{BSTx} = 10 \times \left[\frac{Q_{gx(total)}}{\Delta V_{BST}} + C_{GATEx}\right] \quad (4)$$

Where

- $Q_{gx(total)}$ is the total gate charge of the FET
- ΔV_{BST} (1V typical) is the hysteresis across BSTx to SRCx pins

7.3.3.1.3 Using PWM Control Method (GATEx)

TPS12SxxF-Q1 has integrated PWM generator used for controlling GATEx during capacitive load driving. Figure 7-7 shows application circuit for driving capacitive load using PWM control method.

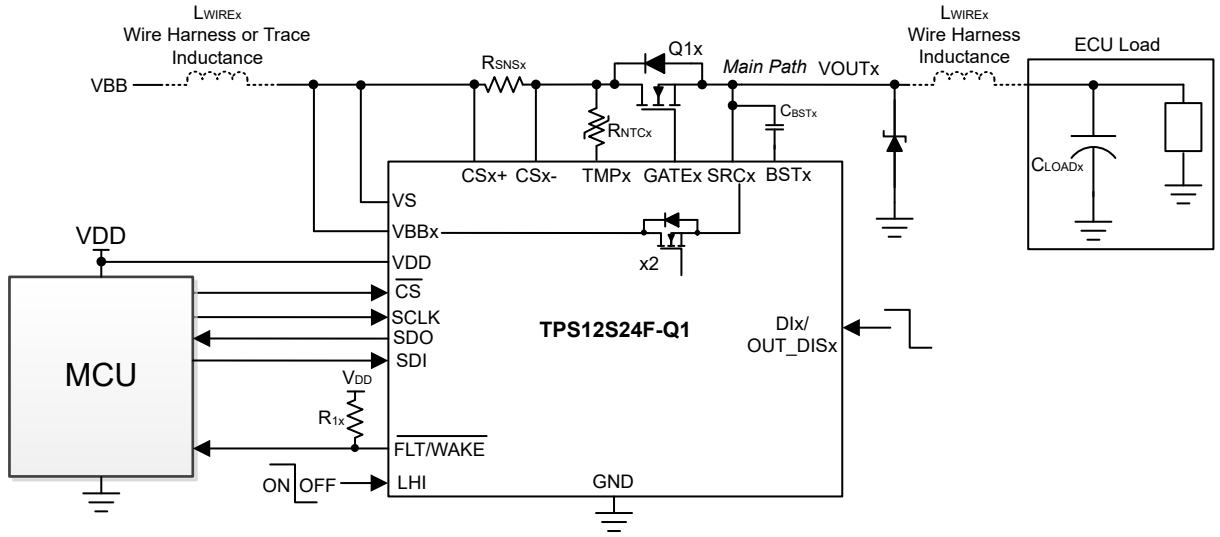


Figure 7-7. TPS12SxxF-Q1 Application Circuit for Capacitive Load Driving Using PWM or SCP Based Auto-Retry Method

L_{WIREx} is the wire harness inductance from device output to capacitive load.

Select the PWM duty cycle and frequency over SPI based on C_{LOADx}, L_{WIREx} and t_{CHARGE} specifications. The capacitor charging or inrush duration can be set by INRUSH_DURATION_CHx bits. Refer to Table 7-1 for all configurable parameters during this mode.

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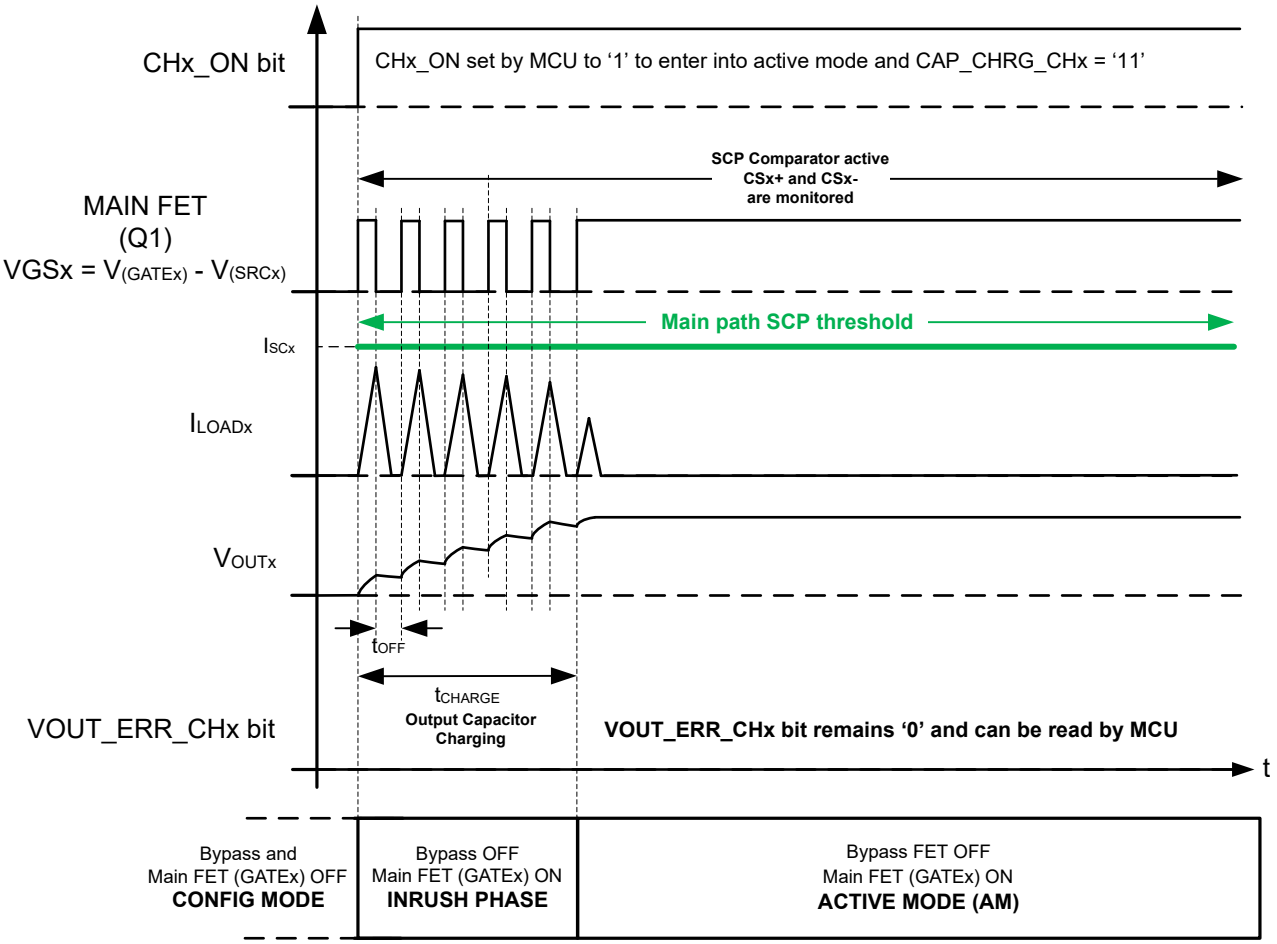


Figure 7-8. Timing Diagram for Bulk Capacitor Charging Using PWM Method

PWM is only enabled for set INRUSH_DURATION_CHx only.

VOUT_ERR_CHx bit is an indication bit for GATEx being ON/OFF after set INRUSH_DURATION_CHx. The device does not take any action based on this bit.

There is a fixed delay of maximum 60us across temperature after the GATEx goes low before the GATEx turns on again. This intentional delay confirms safe turn OFF of the external FET and limits the duty cycle for higher frequencies. As higher frequency is selected, maximum achievable duty cycle comes down.

For Example: if frequency is 3kHz (333us) then maximum achievable duty cycle is approximately 82% [(333us-60us)/333us] across temperature.

7.3.3.2 Resistive or Inductive Load Driving

Resistive loads are the simplest loads to drive as resistive loads follow Ohm's Law:

$$V = I \times R \quad (5)$$

It is simple because the designer knows the voltage (typically 13.5V or 52V for a car battery) and the resistance of the load (by measuring it with an ohmmeter). With these two parameters, the user can calculate the maximum current that flows through the circuit. In typical applications the current through the load must vary to provide

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the intended output. The most basic way to vary the current through the load is through pulse width modulating (PWM).

An inductive load is any load that stores magnetic energy when connected to a supply voltage. The inductive load impedance consists of both a resistance and inductance in series. When resistance and inductance are switched off, inductive loads can generate a transient negative voltage of hundreds of volts due to the stored magnetic energy in the inductance. This transient voltage can cause severe damage to the drive circuit. To prevent any potential damage, during switch-off the stored magnetic energy must be dissipated by clamping the voltage across the inductive load. An external TVS or standard diode connects from output to ground (or TVS diode across drain to source) that protects the circuit by clamping the voltage over the switch to a set voltage and recirculating the current through the clamp. This causes the stored energy to be safely dissipated. With this large clamp voltage the demagnetization time is decreased leading to a safe and quick turn-off time for inductive loads.

Figure 7-9 shows application circuit for driving resistive or Inductive loads. Refer to Table 7-1 for all configurable parameters during this mode.

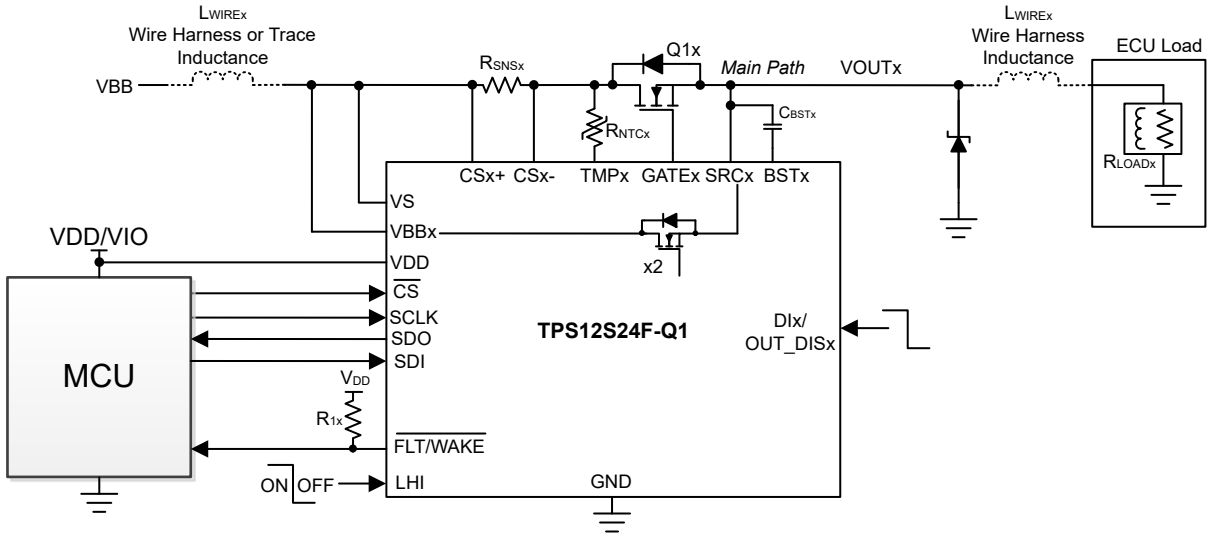


Figure 7-9. TPS12SxxF-Q1 Application Circuit for Driving Inductive or Resistive Loads

There is a fixed delay of maximum 60us across temperature after the GATEx goes low before the GATEx turns on again. This intentional delay confirms safe turn OFF of the external FET and limits the duty cycle for higher frequencies. As higher frequency is selected, maximum achievable duty cycle comes down.

For Example: if frequency is 3kHz (333us) then maximum achievable duty cycle is approximately 82% [(333us-60us)/333us] across temperature.

7.3.4 Protection Mechanisms

The SPI controller family is designed to operate in the automotive environment. Failures detection is provided to implement protections for the external MOSFETs and eventually for the load. The protection mechanisms allow the device to be robust against many system-level events such as load dump, reverse battery, output short-to-ground, overload and more.

7.3.4.1 I2T Based Overcurrent and Short-Circuit Protection

The device includes a programmable fuse protection for each channel, that is based on a defined time-current curve and is commonly referred to as I2T protection in melting fuse datasheets. The intent is to match the switch turnoff behavior of a melting fuse. The NOM_CUR_CHx bits and I2T_TRIP_CHx bits set the time-current curve

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and immediate shutdown protection (I_{SC}) to create the full I2T protection for the device. The I2T protection of the device consists of three regions:

The I2T protection of the device consists of three regions:

1. Nominal current
2. I2T based Fuse shutdown
3. Immediate shutdown protection (SCP)

The operational region for the fuse-based shutdown is shown in the Figure 7-10. Exemplary values for the current values that bound the operational region is included.

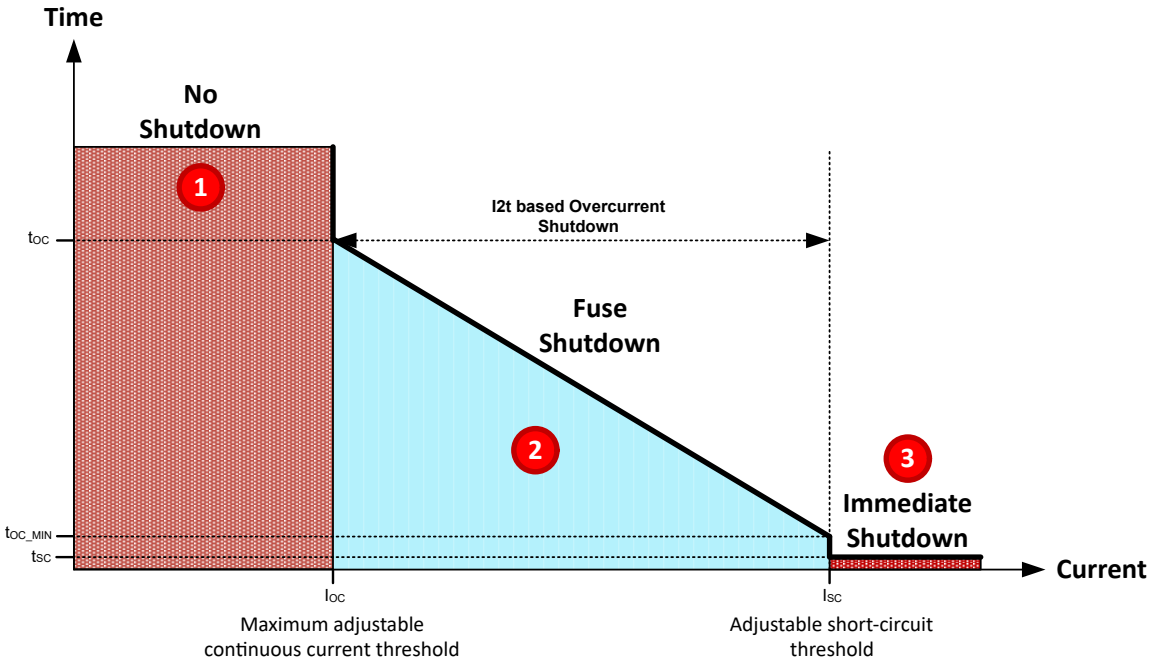


Figure 7-10. Configurable Current vs Time Characteristics Curve For TPS12SxxF-Q1

The nominal current region (1) defines the region where the device can supply current indefinitely without turning off. This is roughly equivalent to the fuse current rating of a melting fuse. This region is set by the NOM_CUR_CHx bits and if the output current is less than the NOM_CUR_CHx setting then the device can supply current indefinitely as previously stated and it does not start the I2T accumulation. If the output current is greater than or equal to the NOM_CUR_CHx setting then the device enters the I2T accumulation loop and starts to accumulate until the I2T_TRIP_CHx threshold is met. If the output current falls back below the NOM_CUR_CHx before the I2T_TRIP_CHx value is reached then the device starts the I2T de-accumulation.

Above the nominal current region, is the fuse shutdown region (2) which is set by the I2T_TRIP_CHx bits. This region defines the curvature of time-current curve and the region where the I2T accumulation of the device is active and where I2T_MOD_CHx is set to 1. Based on the output current level and the NOM_CUR_CHx setting the device trips at different time intervals based on the I2T_TRIP_CHx value that is set. Depending on the DCR_CHx bit in the I2T_CONFIG_CHx register, the time-current curve of the device is defined by the equations in the following sections.

7.3.4.1.1 I2T Accumulation and De-Accumulation for DCR_CHx = '0' Setting

$$\text{I2T_TRIP_DIG} = \left(\text{ILOAD_DIG}^2\right) \times t \times 50\mu s \quad (6)$$

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For DCR_CHx = 0, the device also offers a configurable decrement factor through the ACC_DCR0_CHx bits in the I2T_CONFIG_CHx register which can vary the decrement time for DCR_CHx = 0. ILOAD_DIG is the digital value of scaled current from current sense amplifier.

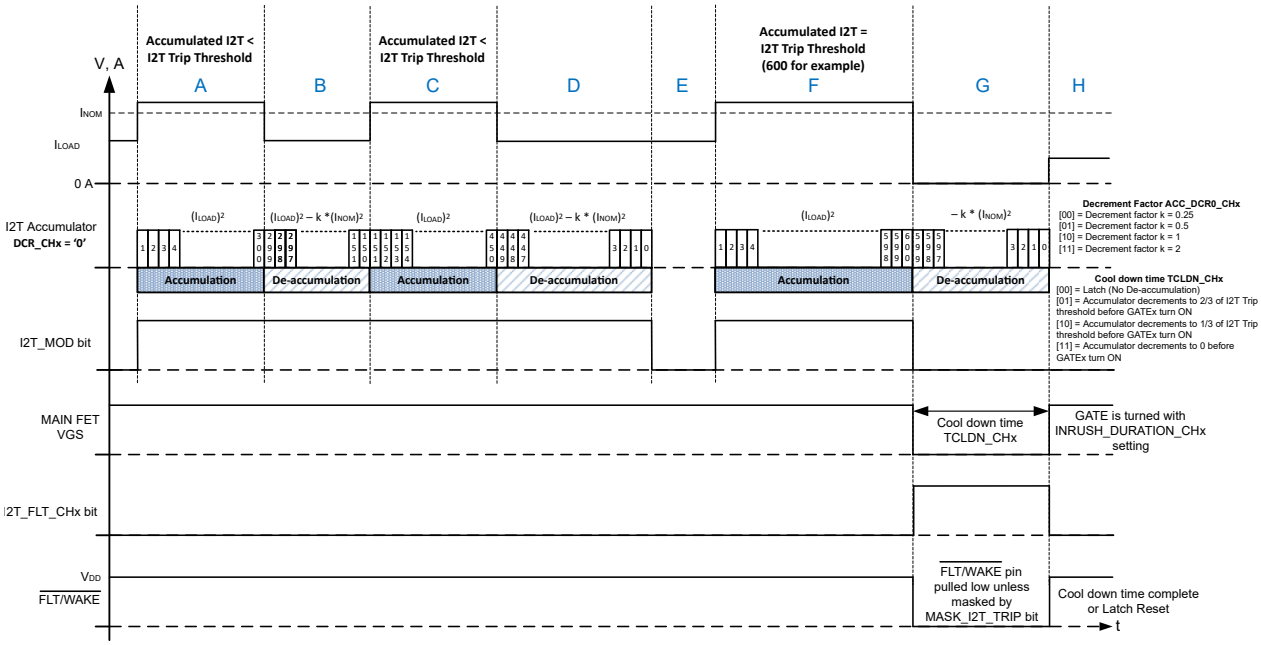


Figure 7-11. I2T Accumulation and De-Accumulation With DCR_CHx = '0' Setting

7.3.4.1.2 I2T Accumulation and De-accumulation for DCR_CHx = '1' Setting

$$\text{I2T_TRIP_DIG} = \left(\text{ILOAD_DIG}^2 - \text{INOM_DIG}^2\right) \times \text{t} \quad \times 50\mu\text{s} \tag{7}$$

Depending on the DCR_CHx setting, the I2T_TRIP_CHx bits in the I2T_CONFIG_CHx has different I2T_TRIP_DIG thresholds. For more information on the I2T trip thresholds, see the I2T_CONFIG_CHx register.

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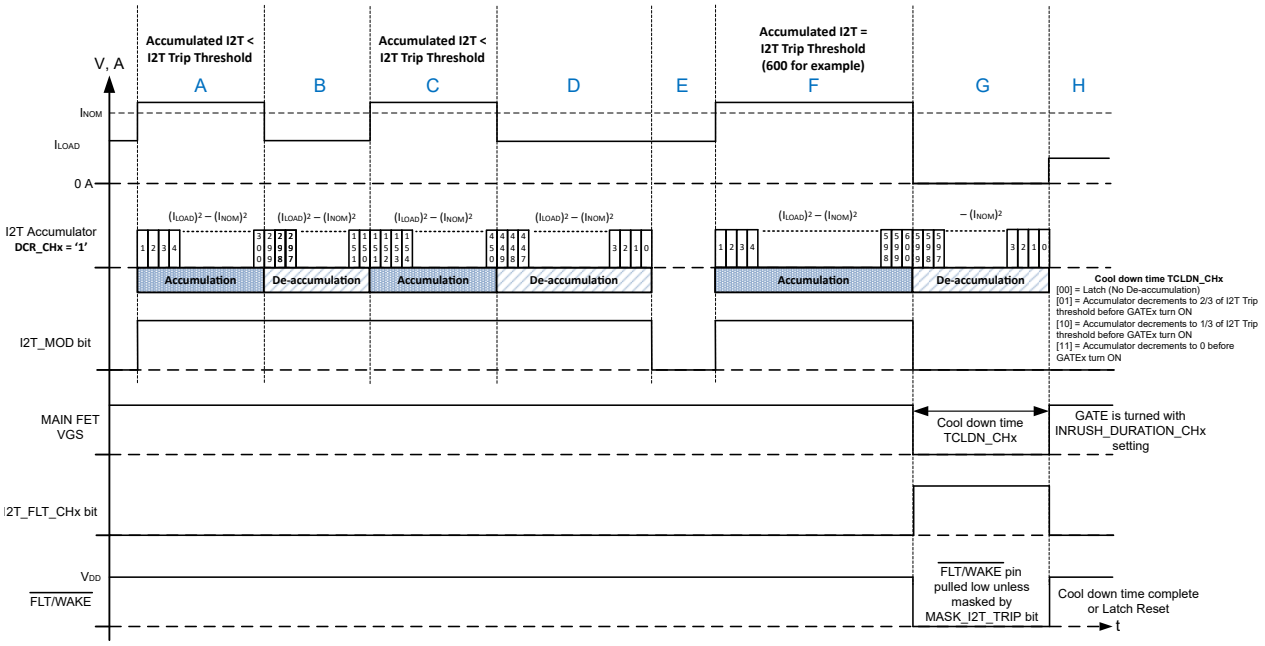


Figure 7-12. I2T Accumulation and De-Accumulation With DCR_CHx = '1' Setting

If the accumulation does not exceed the I2T_TRIP_CHx value and the current falls below NOM_CUR_CHx then equation 1 or equation 2 depending on the DCR_CHx setting is used to decrement the accumulated energy based on the ISNSx value until it reaches zero. While the device continues to decrement down to zero, the I2T_MOD_CHx bit remains one until accumulated energy returns back to zero and then the I2T_MOD_CHx bit is set back to zero. If any conversions are disabled due to a channel entering the I2T loop then the conversions are re-enabled when I2T_MOD_CHx = 0.

If a shutdown occurs either due to the I2T_TRIP_CHx value then, the device remains off for a period set by the TCLDN_CHx. If the TCLDN_CHx = 00 then the device remains in latch off and does not retry.

The immediate shutdown overcurrent protection (SCP) region (3) is set by the FWD_SCP_SET_CHx and REV_SCP_SET_CHx bits. If the output current exceeds the I_{SC} level then the device turns off immediately. The retry or latched off behavior for the SCP is set by the LATCH_CHx bit and described in the auto-retry and latch-off operation section.

The device also features I2T accumulation in reverse direction as Figure 7-13 shows. The accumulation is not reset at the crossover point (zero load current) whenever load current flows from one direction to another and remains above INOM current threshold.

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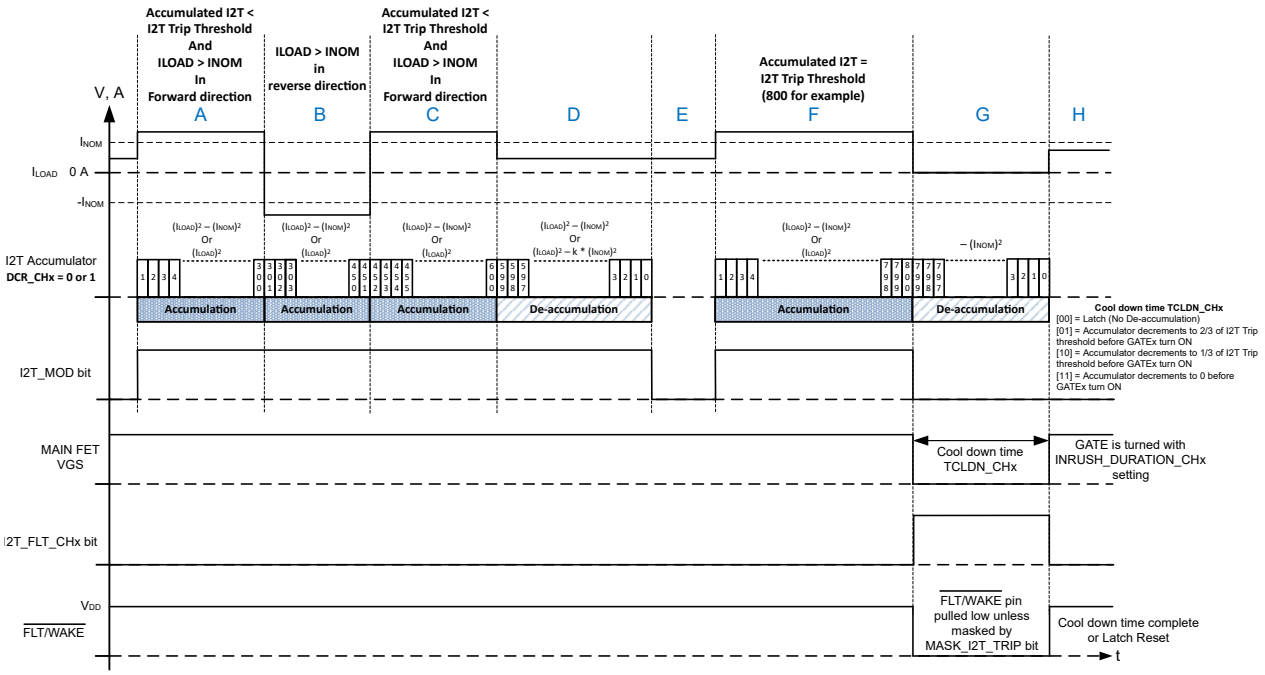


Figure 7-13. I2T Accumulation and De-Accumulation During Forward and Reverse Load Current Flow

7.3.4.2 NTC-Based External FET Over-Temperature Protection

TPS12SxxF-Q1 features an external FET temperature monitoring amplifier and overtemperature protection. This temperature monitoring function is implemented with a differential amplifier with input pin as TMPx and internal output signal as TSNSx. The output of temperature amplifier acts as one of the inputs for integrated ADC. The device also features integrated comparator on TSNSx output internally to detect external main FET overtemperature fault. When voltage on internal TSNSx signal exceeds TSNS_TSD_SET_CHx threshold for more than TSNS_TSD_MASK_CHx masking time then main FET (GATEx) turns OFF, device goes into auto-retry or latch-off based on setting in LATCH_CHx bit and $\overline{\text{FLT/WAKE}}$ asserts low unless masked.

The overtemperature threshold can be set through the SPI in the range from 45°C to 160°C in steps of 5°C using TSNS_TSD_SET_CHx bits.

R_{NTCx} is the thermistor (in this case an NTC thermistor) resistance which varies with the temperature and R_{TMPx} is a normal resistor used to linearize the thermistor behavior with respect to temperature, positioned as per Figure 7-14.

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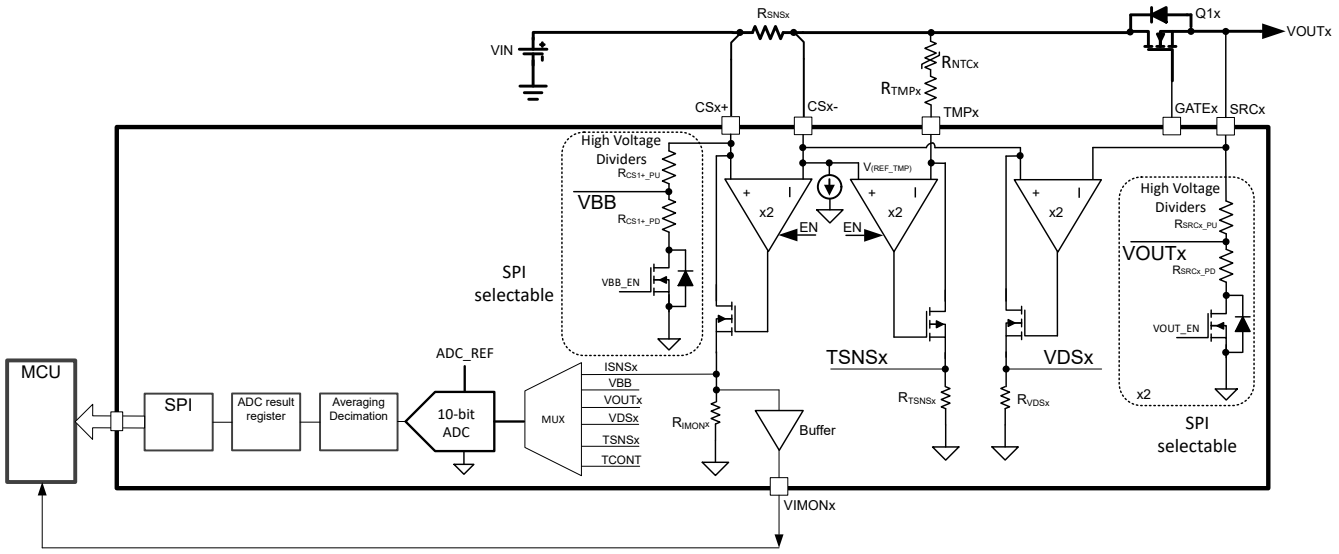


Figure 7-14. NTC Based Temperature Sensing and Protection

7.3.4.3 Device Junction Overtemperature Warning

The device temperature is internally monitored and sensed temperature is stored in ADC_RESULT_TCONT. If the sensed controller temperature exceeds $T_{(CONT_TSD_WRN)}$ threshold then CHAN_OCP_I2T_TSD_OV and THERMAL_WRN_CHx is set '1' which can be read by MCU over SPI.

7.3.4.4 Input Undervoltage and Overvoltage Protection

TPS12SxxF-Q1 features integrated undervoltage (UVLO) and overvoltage (OVLO) protection for both channels. The device uses CS1+ pin for sensing input voltage and compares with set UVLO or OV threshold. If the sensed CS1+ voltage is lower than $V_{CHx(UVLOF)}$ set using UVLO_SET_CHx or higher than VCHx(OVR) set using OVLO_SET_CHx for more than $t_{CHx(UVLO_MASK)}$ set using UVLO_MASK_CHx or $t_{CHx(OV_MASK)}$ delay set using OV_MASK_CHx then main path gate drive (GATEx) is turned OFF.

VBB undervoltage is indicated by GLOBAL_ERR_WRN and VBB_UVLO bit in FAULT_GLOBAL register. VBB overvoltage is indicated by CHAN_OCP_I2T_TSD_O V bit in FAULT_GLOBAL register.

$\overline{\text{FLT/WAKE}}$ is also asserted low if configured in FAULT_MASK register using MASK_VBB_UVLO or MASK_VBB_OVLO bit. Main FET (GATEx) is turned ON again whenever CS1+ voltage goes above $V_{CHx(UVLOR)}$ or below $V_{CHx(OVF)}$. $V_{CHx(UVLO_Hys)}$ or $V_{CHx(OV_Hys)}$ is programmable using UVLO_HYS_CHx or OVLO_HYS_CHx bits.

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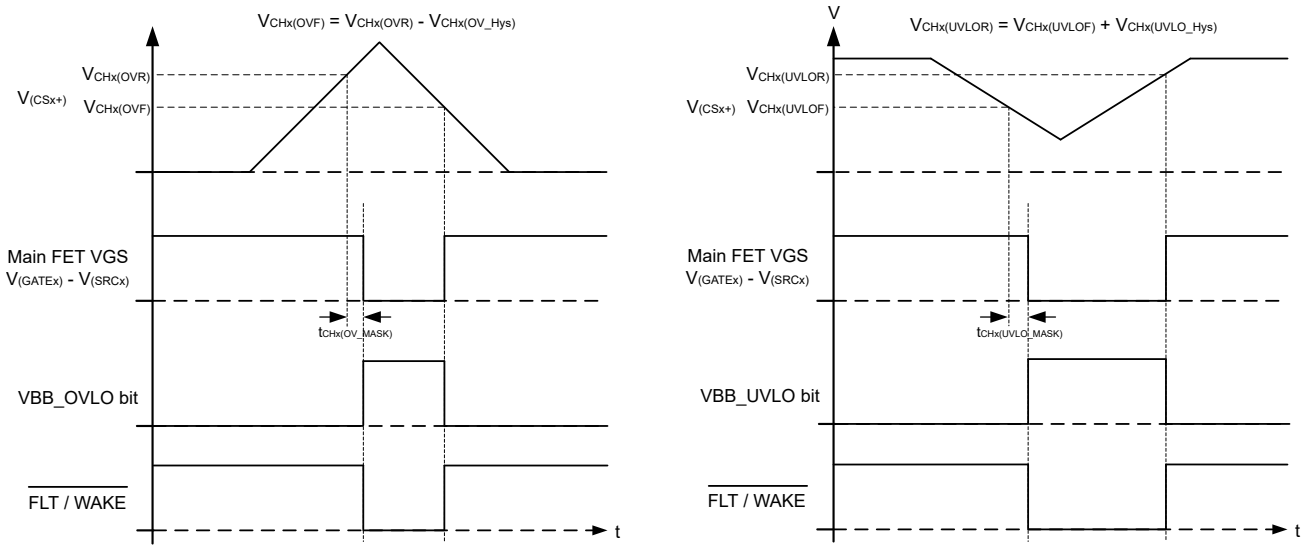


Figure 7-15. Timing Diagram For Input Supply Overvoltage and Undervoltage Protection

7.3.4.5 External FET Drain to Source Voltage (VDS) Overvoltage Protection

The drain to source voltage of activated channels is continuously monitored to prevent linear mode conduction of the external FETs. The voltage for CSx- to SRCx is always monitored internally.

VDS overvoltage protection in available in forward as well as reverse direction and can be enabled using VDS_PROT_EN_CHx along with threshold setting using VDS_OVP_SET_CHx bits. A configurable filter time set using VDS__OVP_MASK_CHx is provided for each channel independently to set masking or deglitch time to avoid false trip due to noisy signal measurement.

7.3.4.6 Bi-VDS Based Short-Circuit Protection

The drain to source voltage of activated channels is continuously monitored which can also be used for VDS based short circuit protection (SCP). The VDS based SCP protection is available in both the direction and can be enabled using VDS_PROT_EN_CHx bit along with threshold setting using combination of VDS_OVP_SET_CHx and VDS_GAIN_CHx bits. A configurable filter time set using VDS_OVP_MASK_CHx is provided for each channel independently to set masking or deglitch time to avoid false trip due to noisy signal measurement. Figure 7-16 shows application circuit with VDS based SCP protection without current sense resistor (R_{SNSx}) leading to system-level size and cost reduction.

With GATEx tunred on by CHx_ON bit, first VGS of external FET is sensed by monitoring the voltage across GATEx to SRCx pins. Once GATEx to SRCx voltage raises above $V_{CHx(GATE_GOOD)}$ (7.5V typical) threshold which specifies that the external FET is enhanced, then the VDS based protection is activated.

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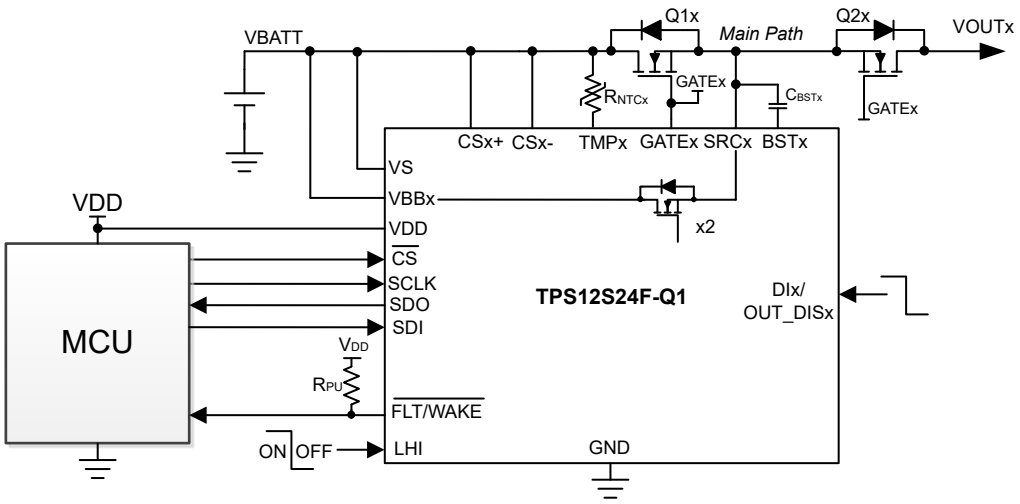


Figure 7-16. TPS12SxxF-Q1 VDS Based SCP Protection Application Circuit

Table 7-2 shows threshold setting for VDS based SCP protection based on combination of VDS_OVP_SET_CHx and VDS_GAIN_CHx[1:0] bits.

Table 7-2. Threshold Settings For VDS Based SCP Protection

VDS_OVP_SET_CHx[4:0]	VDS OVP THRESHOLD (mV)		
VDS_GAIN_CHx[1:0] =	'11'	'10'	'01'
0	300	56	15
1	340	64	17
2	380	72	19
3	425	80	21
4	465	87.5	24
5	510	95	26
6	550	105	28
7	590	110	30
8	635	120	32
9	675	126.5	34
10	715	135	36
11	760	142.5	38
12	800	150	40
13	840	158	42
14	880	165	44
15	925	175	46
16	965	182	48
17	1010	190	50
18	1050	197	52
19	1090	205	54
20	1130	212.5	56
21	1175	220	58

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Table 7-2. Threshold Settings For VDS Based SCP Protection (continued)

VDS_OVP_SET_CHx[4:0]	VDS OVP THRESHOLD (mV)		
VDS_GAIN_CHx[1:0] =	'11'	'10'	'01'
22	1215	230	61
23	1260	236	63
24	1300	245	65
25	1340	252	67
26	1385	260	69
27	Reserved	267.5	71
28	Reserved	275	73.5
29	Reserved	283	75
30	Reserved	290	77.5
31	Reserved	300	80

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7.3.4.7 Reverse Polarity Protection

The TPS12SxxF-Q1 devices features integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Reverse polarity faults occur during installation and maintenance of the end equipments. The device is tolerant to reverse polarity voltages down to –40V both on input and on the output. The device turns OFF back to back FETs when input reverse battery events is detected to protect the load. Figure 7-17 shows application circuit with series diode on VS (D_{VS}) and VBBx (D_{VBBx}) pins for input polarity protection.

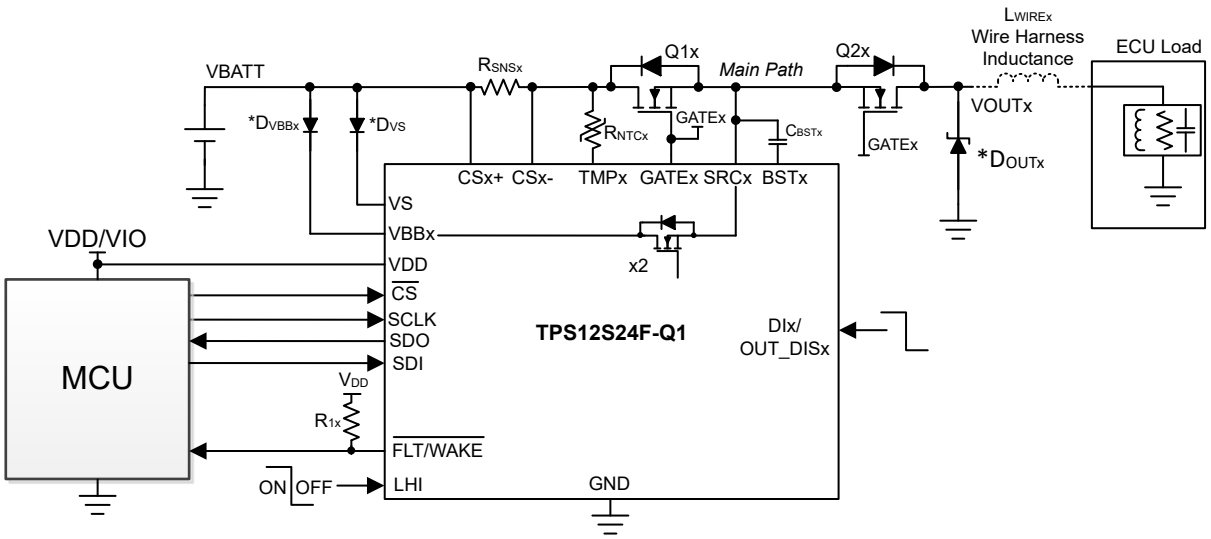


Figure 7-17. TPS12SxxF-Q1 Application Circuit For Input Reverse Polarity Protection

On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems the output side TVS or a diode (D_{OUTx}) limit the output negative voltage level.

7.3.4.8 Loss of Ground

If the device GND pin connection is lost with MCU ground still connected to ECU ground then device detects loss of ground when device GND voltage exceeds 2V threshold with respect to MCU ground, GATEx drive is disabled regardless of the control signal status in config, active, or limphome mode. If the GATEx drives are already disabled when the ground connection is lost, the GATEx drive remains disabled. During loss of

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device ground, the total IQ of the device can conduct through any of the following pins: $\overline{CS}$, SDI, SCLK, LHI, or DIx/OUT_DISx, using whichever path has the lowest impedance (resistance to current flow) as Figure 7-18 shows.

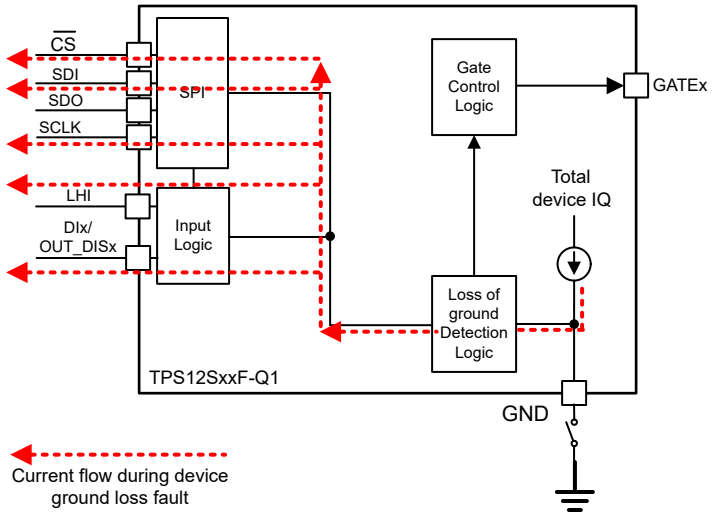


Figure 7-18. Current Flow During Device Loss of Ground Fault

Table 7-3 lists impact of loss of ground fault on gate drive in different states.

Table 7-3. Ground Faults

STATE/MODE	GATE DRIVE STATUS AFTER DEVICE GROUND LOSS FAULT
Low power mode	Bypass FET remains ON and device remains in LPM. Device is capable to detect loadwakeup in loss of device ground fault state also. LPM IQ flows through path shown in below figure.
Config, active, or limphome mode	GATEx remains off or turns off from on. Active mode IQ flows through path shown in below figure

7.3.5 Diagnostic Mechanisms

7.3.5.1 ADC Sense Signals

The TPS12SxxF-Q1 provides an integrated successive approximation 10-bit ADC which can convert different analog signals to digital signals which can be read out through SPI. The ADC can convert the following analog signals:

- Channel input voltage sense available from ADC_RESULT_VBB register
- Channel output voltage sensing available from ADC_RESULT_CHx_V register
- External FET temperature sensing available from ADC_RESULT_CHx_T register
- Controller Junction temperature sensing available from ADC_RESULT_TCONT register
- Channel drain to source voltage sensing available from ADC_RESULT_CHx_VDS register

Figure 7-19 provides a functional block diagram of the integrated ADC along with the analog signal inputs to the ADC. Conversion of any of the analog signals can either be disabled globally through the ADC_CONFIG register.

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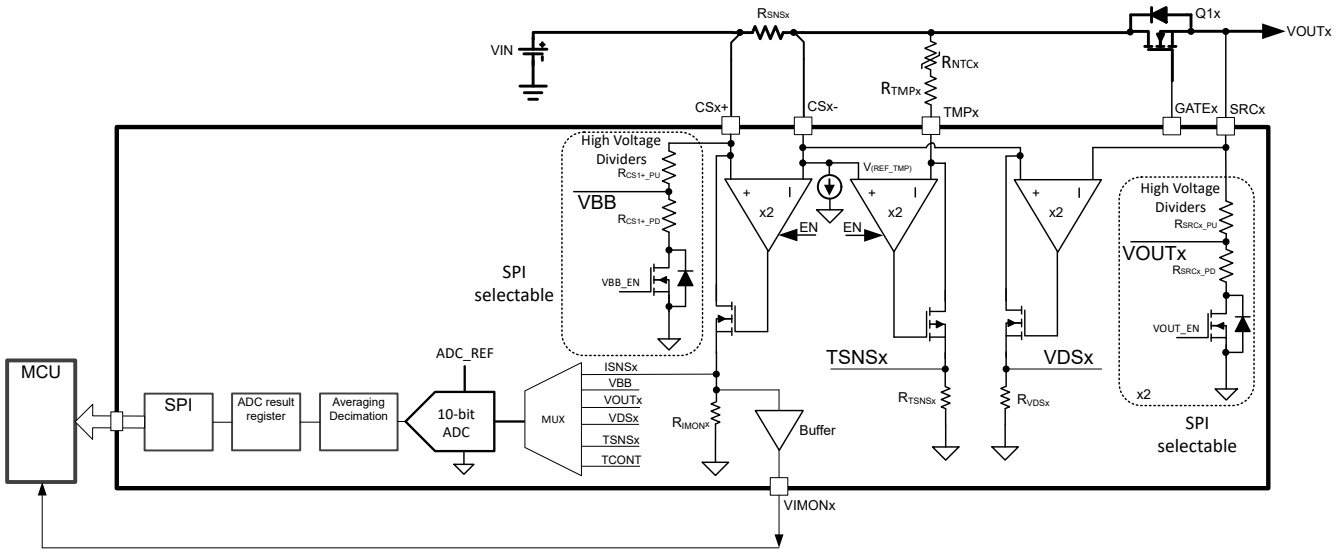


Figure 7-19. TPS12SxxF-Q1 ADC Block Diagram

The device also provides a configurable delay which can also help to further reduce the quiescent current of the device by reducing the sampling rate of the ADC. The configurable delay is set by the ADC_CONFIG_DELAY bits in the ADC_CONFIG register.

If I2T protection is enabled (I2T_EN_CHx = 1) and either channel is not in I2T mode (I2T_MOD_CHx = 0), then the device converts each of the analog signals in a round robin sequence with the configurable delay. Figure 7-20 below shows the ADC scheduling if no channel is in I2T mode (I2T_MOD_CHx = 0) and all analog signal conversions are enabled. If I2T protection is disabled then the round robin sequence below also applies.

If I2T protection is enabled (I2T_EN_CHx = 1) and one or both of the channels are in I2T mode (I2T_MOD_CHx = 1), then the device disables all conversions except for the ISNSx conversions which are used for the internal I2T protection. The device also disables the configurable delay function as well. Figure 7-20 below shows the ADC scheduling if one or both of the channels are in I2T mode (I2T_MOD_CHx = 1).

If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the VBB, TCONT, TSNSx, VDSx measurement, if enabled, is disabled for all the channels and the VSNS_RDY_CHx bit is 0. Once the channels exit the I2T loop (I2T_MOD_CHx = 0), then all these measurements are automatically re-enabled if previously enabled before the I2T event.

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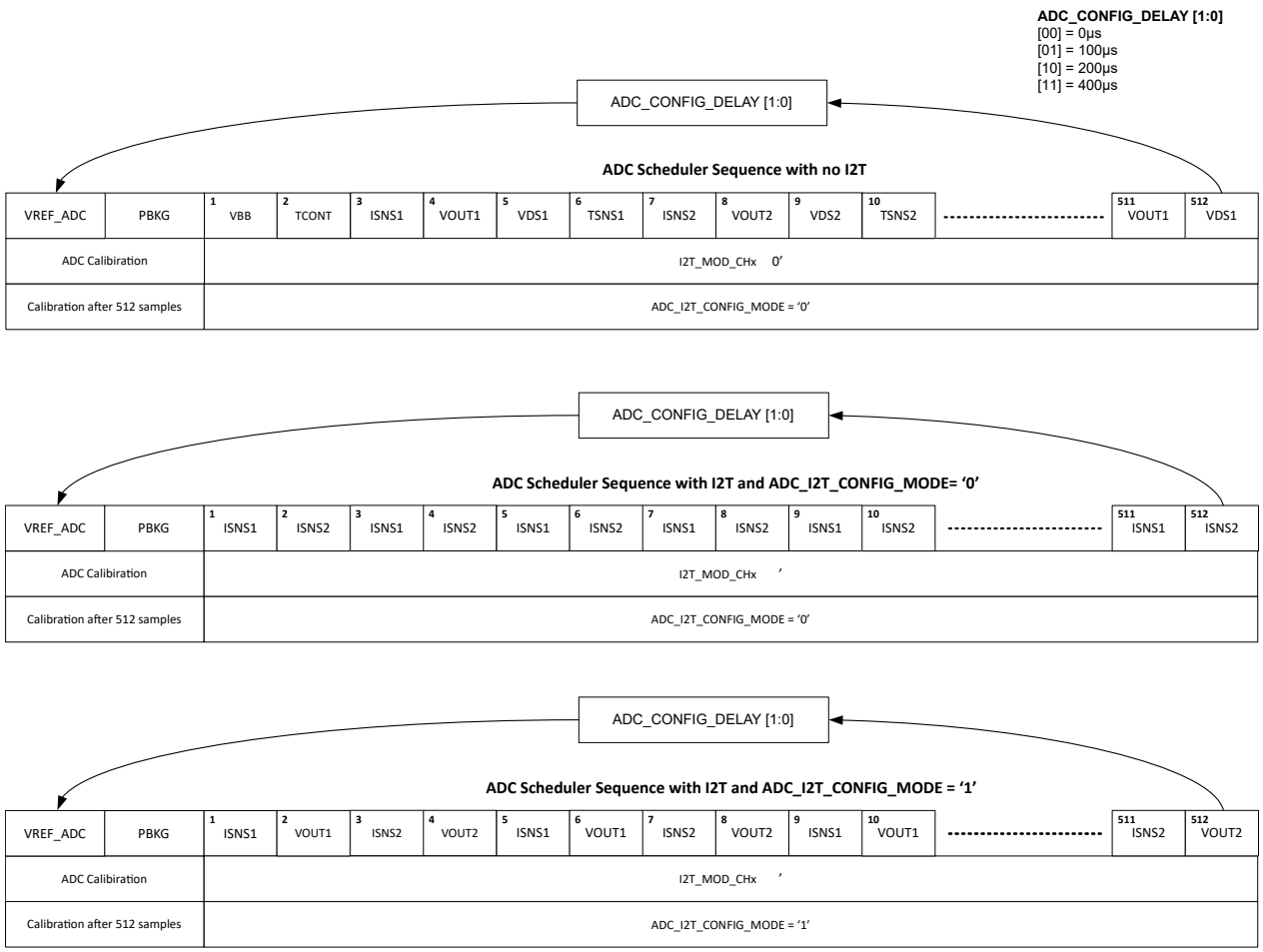


Figure 7-20. TPS12SxxF-Q1 ADC Conversion Sequence

The reference voltage for the ADC is fixed internally and is specified in the electrical characteristics table through the V_{ADC_REF} parameter. The ground reference of the ADC connects internally to the GND of the device.

The conversion equation for each of the analog signals can be found in the respective sections below.

7.3.5.2 Analog and Digital Current Monitor (VIMONx)

The device features integrated current sense amplifier which is used for monitoring the voltage drop across the external shunt resistor as a sensor for the load current in forward and reverse direction. The bi-directional current sense circuit provide a voltage signal that is proportional to the output current of the switch – a voltage signal that is sampled at the input of the integrated ADC is desired and the direction of current information is stored in ISNS_POLARITY_CHx bit in ADC_RESULT_CHx_I register. The voltage-based conversion enables a common-sense voltage for other signals (CSx+/SRCx/TSNSx/TCONT/VDSx) that are converted by the ADC.

Note that the current sense resistor and GAIN setting must be selected by the customer appropriately to get the voltage to ADC input to within the ADC range.

The 10-bit digital current sense output can be read from the ADC_RESULT_CHx_I register. The ISNS_RDY_CHx bit is set if the ADC conversion result is updated in the register from the last time the register is read.

Consider the following factors when selecting the RSNS value:

- Current sense amplifier gain (GAIN)
- Largest and smallest diagnosable load current required for application operation

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- Full-scale voltage of the ADC
- Tolerance of the RSNS resistor used

The differential gain of the current sense amplifier is configurable by the configuration bits ISNS_GAIN_CHx in DIAG_CONFIG_CHx register.

Table 7-4. ISNS Amplifier GAIN Settings

ISNS_GAIN_CHx	CURRENT SENSE AMPLIFIER GAIN (V/V)
0x0	15
0x1	30
0x2	50
0x3	65
0x4	85
0x5	100
0x6	120
0x7	135

Note

The current sense information can be read on VIMONx pin and ADC_RESULT_CHx_I register whether the main FET (GATEx) is ON or OFF as current sense information is independent of main FET (GATEx) status.

The ADC conversion equation for current sense is in Equation 8.

$$\text{ADC_RESULT_CHx_I} = \frac{1023}{V_{\text{ADC_REF}}} \times V_{\text{CHx(ISNS_GAINx)}} \times I_{\text{CHx(LOAD)}} \times R_{\text{SNSx}} \quad (8)$$

7.3.5.3 Input Supply Voltage Measurement

The TPS12SxxF-Q1 device senses CS1+ pin voltage and provides a VBB voltage measurement through the 10-bit ADC. The VBB voltage measurement is disabled by default. The VBB voltage sense function can be enabled through the ADC_VBB_DIS bit in the ADC_CONFIG register.

The conversion equation for the VBB voltage measurement is detailed in Equation 9. The ADC measurement result is available in the ADC_RESULT_VBB register. The VBB_RDY bit is set to one if a new ADC conversion result exists since the register is last read.

$$\text{ADC_RESULT_VBB} = \frac{1023}{V_{\text{(ADC_REF)}}} \times \frac{3}{76} \times \text{VBB} \quad (9)$$

7.3.5.4 Output Voltage Measurement

The TPS12SxxF-Q1 device senses SRCx pin voltage and provides an output voltage measurement per channel through the integrated 10-bit ADC. The output voltage measurement function is disabled by default. To enable the output voltage sense function it must be globally enabled in the ADC_CONFIG register through the ADC_VSNS_DIS bit. If the global bit is enabled then the device enables the output voltage measurement on each channel according to the VSNS_DIS_CHx bit in the respective CHx_CONFIG register.

The conversion equation for the output voltage measurement is detailed in Equation 10. The ADC measurement result is available in the ADC_RESULT_CHx_V register. The VSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register is last read.

$$\text{ADC_RESULT_CHx_V} = \frac{1023}{V_{\text{(ADC_REF)}}} \times \frac{3}{80} \times V_{\text{SRCx}} \quad (10)$$

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7.3.5.5 External FET Temperature Measurement

The TPS12SxxF-Q1 senses external FET temperature via NTC resistor and provides a temperature measurement for each of the power MOSFETs through the 10-bit ADC. The FET temperature sense function is disabled by default. To enable the FET temperature sense function for each channel it must be globally enabled in the ADC_CONFIG register through the ADC_TSNS_DIS bit. The conversion equation for the FET temperature measurement is Equation 11. The ADC measurement result is available in the ADC_RESULT_CHx_T register. The TSNS_RDY_CHx bit is set to one if a new ADC conversion result exists since the register is last read.

$$\text{ADC_RESULT_CHx_T} = \frac{1023}{V_{(\text{ADC_REF})}} \times \frac{\left(V_{(\text{REF_TMP})} \times R_{\text{TSNSx}}\right)}{\left(R_{\text{NTCx}} + R_{\text{TMPx}}\right)} \quad (11)$$

Where

- $V_{(\text{REF_TMP})}$ = 50mV
- Integrated R_{TSNSx} = 45kΩ for standard 10kΩ NTC and 90kΩ for standard 47kΩ NTC
- Recommended R_{TMPx} = 700Ω for standard 10kΩ NTC and 1500Ω for standard 47kΩ NTC

7.3.5.6 External FET Bi-Directional Drain to Source (Bi-VDS) Measurement

The TPS12SxxF-Q1 device senses across CSx- to SRC and provides a drain-to-source voltage (VDS) measurement per channel in forward as well as reverse direction through the integrated 10-bit ADC to prevent linear mode conduction of the external FETs. The VDS voltage measurement function can be enabled using ADC_VDS_DIS bit. If enabled then the device enables the VDS voltage measurement on each channel according to the VDS_SNS_DIS_CHx bit in the respective CHx_CONFIG register.

The conversion equation for the VDS voltage measurement is below. The VDS conversion equation is only valid for VDS voltages from ±15mV to ±1.4V. The ADC measurement result is available in the ADC_RESULT_CHx_VDS register. The VDSSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register is last read.

With GATEx tunred on by CHx_ON bit, first VGS of external FET is sensed by monitoring the voltage across GATEx to SRCx pins. Once GATEx to SRCx voltage raises above V(G_GOOD) (7V typical) threshold which confirms that the external FET is enhanced, then the VDS based monitoring activates.

$$\text{ADC_RESULT_CHx_VDS} = \frac{1023}{V_{(\text{ADC_REF})}} \times V_{\text{CHx}(\text{VDS_GAINx})} \times \text{VDSx} \quad (12)$$

Select VDS_SCP_GAIN_VDSx between 1.5, 8, and 30 using the VDS_SCP_GAIN_CHx bits.

7.3.5.7 Controller Temperature Measurement

The TPS12SxxF-Q1 device provides controller temperature measurement as per equationEquation 13 through the integrated 10-bit ADC.

$$\text{ADC_RESULT_TCONT} = \frac{1023}{V_{(\text{ADC_REF})}} \times \left(2.1 - 0.00643 \times T\right) \quad (13)$$

7.3.5.8 VOUT Short-to-Battery or FET Short and Open-Load Detection

The TPS12SxxF-Q1 device is capable of detecting output short-to-battery or external FET drain to source short and open-load events regardless of whether the channel output is turned on or off, however the two conditions use different methods.

7.3.5.8.1 Measurement With Main FET (GATEx) Enabled

When the main FET (GATEx) is ON, the VOUT short-to-battery external FET drain to source short and open-load conditions can be measured with the current sense feature. In both cases, the load current is measured using the current sense circuit and the ADC (available in the ADC_RESULT_CHx_I registers). The current sense accuracy can be increased at low current levels by increasing the gain from a nominal value of to higher gain

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value setting by the configuration bits ISNS_GAIN_CHx in DIAG_CONFIG_CHx register. This enables the ADC to measure the low load current with higher accuracy.

7.3.5.8.2 Detection With Main FET (GATEx) Disabled

The device can detect an open load or a short-to-battery event when the main FET (GATEx) is OFF. These are referred to below as off state open load (OL) detection and off state short-to-battery (SVBB) detection. When the main FET (GATEx) is OFF, the device can distinguish between an open load event and a short-to-battery event through a defined sequence that are described below.

See a block diagram for the off-state open load and off-state short-to-battery detection in Figure 7-21.

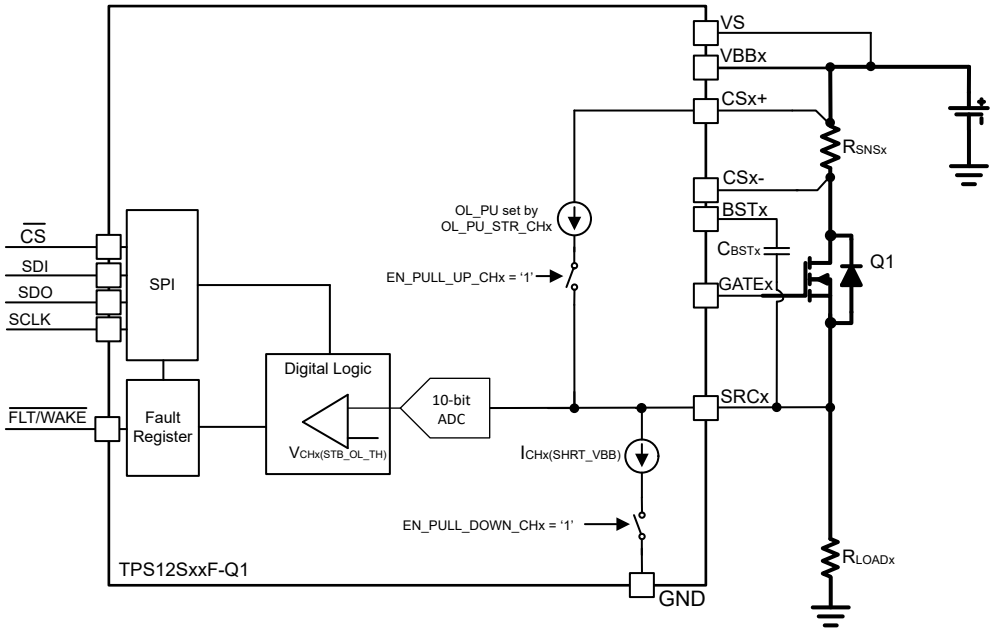


Figure 7-21. TPS12SxxF-Q1 Off-State FET Short and Open Load Detection Block Diagram

7.3.5.8.2.1 Off-State Short-to-Battery Detection

The device also integrates a pull-down current ($I_{CHx(SHRT_VBB)}$) for each channel which can be used to help distinguish between an open load and a short-to-battery fault when the channel is disabled. Initially GATEx is turned off via CHx_ON bit and then pull-down current ($I_{CHx(SHRT_VBB)}$) can be enabled through the EN_PULL_DOWN_CHx bit and VOUTx information is also recorded and stored internally at the same time.

After some time delay based on output wire harness inductance, output capacitor and loading, SVBB_DIAG_EN_CHx bit can be enabled by MCU to record VOUTx once again. If the delta of present VOUTx and past stored VOUTx information is higher than $V_{CHx(STB_OL_TH)}$ then short to battery fault is not present otherwise the fault in indicated in FLT_STAT_CHx register and $\overline{\text{FLT/WAKE}}$ pin asserts low unless masked.

7.3.5.8.2.2 Off-State Open Load Detection

Once short to battery detection is complete without any fault then pulldown current can be disabled and open load detection can be run. The device integrates a pull-up current source ($I_{CHx(OL_PU)}$) for each channel which can be used to pull-up the output to determine if open load fault is present or not. The pull-up current source is enabled EN_PULL_UP_CHx bit and VOUTx information is also recorded and stored internally at the same time.

The strength of the internal pull-up can be programmed through the OL_PU_STR_CHx bits for each channel in the DIAG_CONFIG_CHx registers.

After some time delay based on output wire harness inductance, output capacitor and loading, OL_DIAG_EN_CHx bit can be enabled by MCU to record VOUTx once again. If the delta of present VOUTx

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and past stored VOUTx information is lower than $V_{CHx(STB_OL_TH)}$ then open load fault is not present otherwise the fault in indicated in FLT_STAT_CHx register and $\overline{FLT}$/WAKE pin asserts low unless masked.

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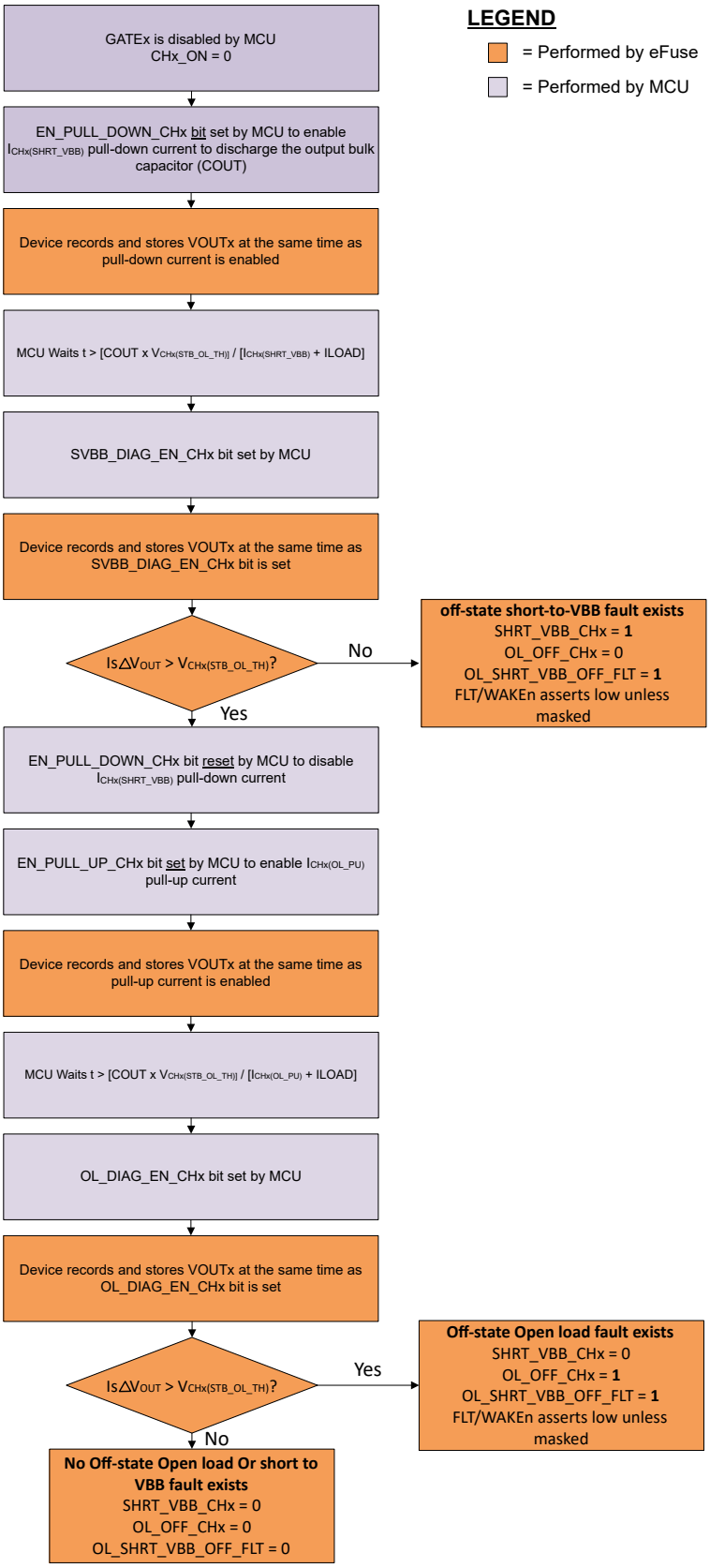


Figure 7-22. Flow Chart For FET Short and Open Load Detection With Gate Drive Disabled

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7.3.5.9 VOUT Short-to-Battery or FET Short Detection for Power at all Times (PAAT) Loads

The device integrates a pull-down current ($I_{CHx(SHRT_VBB)}$) for each channel which can be used to detect VOUT short-to-battery or FET short fault when the channel is disabled. See the below flow chart for detection mechanism

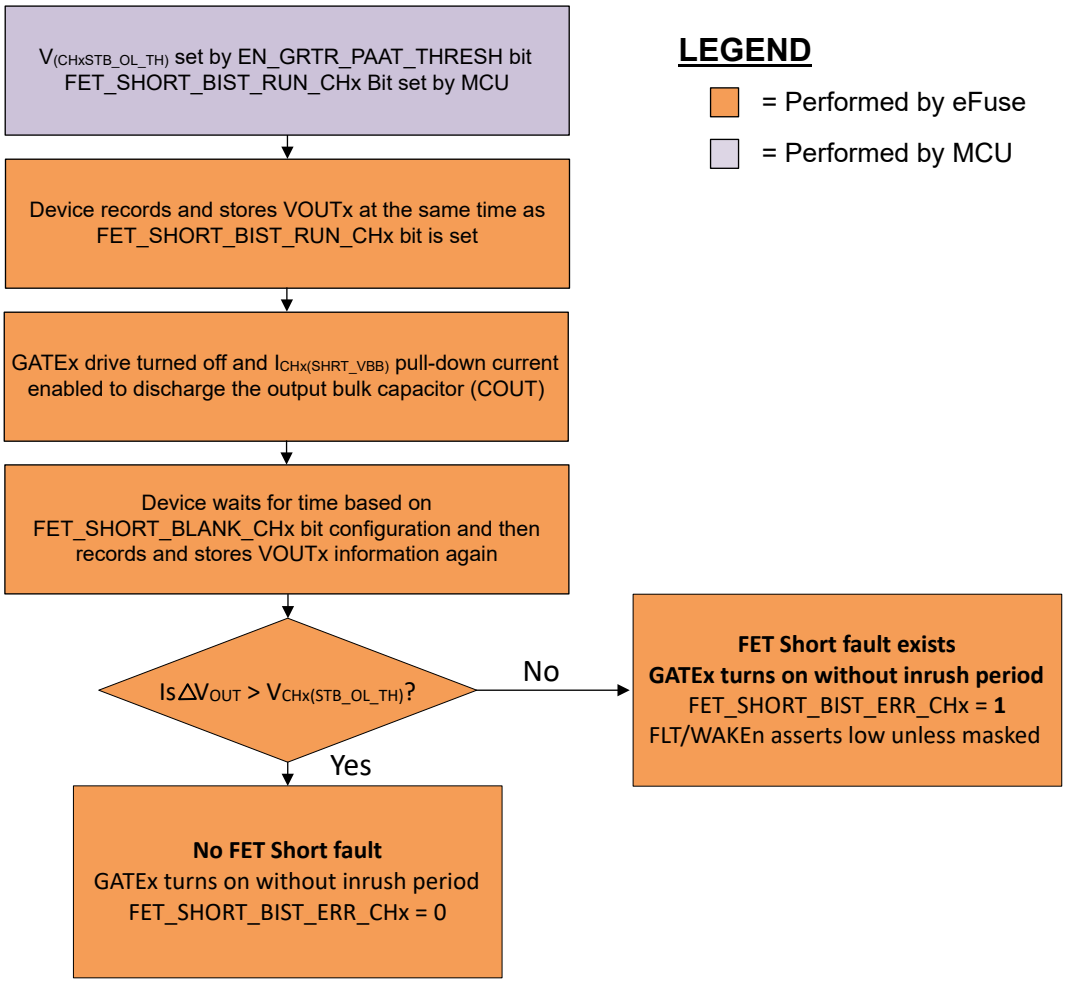


Figure 7-23. Flow Chart For FET Short Diagnosis For PAAT Loads

7.3.6 Fault Indication ($\overline{FLT}$ / $\overline{WAKE}$)

The device provides enhanced fault reporting through a $\overline{FLT/WAKE}$ status pin and fault status bits through SPI. The $\overline{FLT/WAKE}$ status pin allows the device to interrupt the system when a fault has occurred on the device. The $\overline{FLT/WAKE}$ status pin is an open-drain output that asserts low when a fault occurs on the device. For faults which are read clear, the $\overline{FLT/WAKE}$ pin goes high if the fault no longer exists and the specific register to clear the fault is read. Indication on the $\overline{FLT/WAKE}$ pin can be masked for some faults through FAULT_MASK register. See the FAULT_MASK register for more details.

The device also provides fault information through SPI through a global fault register (FAULT_GLOBAL) and channel specific fault registers (FLT_STAT_CHx) to enable the system to quickly diagnose what caused the fault in the device. The device outputs the FAULT_GLOBAL [15:8] bits on the SDO header so these status bits can be continuously read in each SPI transaction. For more details on each of the individual fault status bits see the FAULT_GLOBAL and FLT_STAT_CHx registers in the register map.

When the device is in low-power mode no fault information is available through the $\overline{FLT/WAKE}$ pin. If short-circuit occurs in LPM, the device protects itself then transitions to ACTIVE mode and then signals fault on the $\overline{FLT/WAKE}$ pin and in the fault status registers.

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Table highlights how the device signals different events through the $\overline{\text{FLT/WAKE}}$ pin and the fault status bits.

Table 7-5. Fault Reporting

EVENT / FAULT	DETECTION	PROTECTION (GATE DRIVES TURNED OFF)	BIT FIELD NAME IN FAULT_GLOBAL REGISTER	BIT FIELD NAME IN FLT_STAT_CHx REGISTER	OPTIONAL INDICATION ON $\overline{\text{FLT/WAKE}}$ PIN	BIT FIELD NAME IN FAULT_MASK REGISTER
Input supply (VBB) UVLO	Yes	Yes	VBB_UVLO and GLOBAL_ERR_WRN		Yes unless masked	MASK_VBB_UVLO
Input supply (VBB) UVLO warning ($V_{(CSx+)}$ < 6V)	Yes	No	VBB_UV_WRN and GLOBAL_ERR_WRN		No	-
VDD UVLO	Yes	No	VDD_UVLO	-	Yes unless masked	MASK_VDD_UVLO
SPI Watchdog error	Yes	Transition to Limphome mode	WD_ERR		Yes unless masked	MASK_WD_ERR
SPI CRC/frame error	Yes	No	SPI_ERR		Yes unless masked	MASK_SPI_ERR
NVM CRC ERROR	Yes	Yes	NVM_CRC_ERR in BIST_RESULT register		Yes unless masked	MASK_NVM_CRC_ERR
POR	Yes	Yes	POR		Yes	
Off state Open load fault	Yes	No	OL_SHRT_VBB_OFF_FLT and CHx_FLT	OL_OFF_CHx	Yes unless masked	MASK_OL_OFF
VOUT short to VBB fault	Yes	No	OL_SHRT_VBB_OFF_FLT and CHx_FLT	SHRT_VBB_CHx	Yes unless masked	MASK_SHRT_VBB
External FET Over-Temperature (TSD) Shutdown	Yes	Yes	CHAN_OCP_I2T_TSD_OV and CHx_FLT	THERMAL_SD_CHx	Yes unless masked	MASK_TSD
Bypass FET Over-Temperature Shutdown	Yes	Bypass FET turned OFF Main FET turns ON	CHx_FLT	THERMAL_SD_BYP_CHx	Yes	-
Chip (controller) overtemperature warning	Yes	No		THERMAL_WRN_CHx	Yes unless masked	TSD_CONT_FLT_EN bit in DEV_CONFIG_2 register
Overvoltage on VBB	Yes	Yes	CHAN_OCP_I2T_TSD_OV		Yes unless masked	MASK_VBB_OVLO
VOUT shorted to ground (SCP)	Yes	Yes	CHAN_OCP_I2T_TSD_OV and CHx_FLT	OCP_CHx	Yes unless masked	MASK_OCP

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Table 7-5. Fault Reporting (continued)

EVENT / FAULT	DETECTION	PROTECTION (GATE DRIVES TURNED OFF)	BIT FIELD NAME IN FAULT_GLOBAL REGISTER	BIT FIELD NAME IN FLT_STAT_CHx REGISTER	OPTIONAL INDICATION ON $\overline{\text{FLT/WAKE}}$ PIN	BIT FIELD NAME IN FAULT_MASK REGISTER
I2T Protection	Yes	Yes	CHAN_OCP_I2T_TSD_OV and CHx_FLT	I2T_FLT_CHx	Yes unless masked	MASK_I2T_TRIP
Reverse battery (Reverse Polarity)	Yes	Yes			Yes unless masked	MASK_REV_POL_FLT
Charge pump undervoltage	Yes	Yes	CHx_FLT	CPUMP_UVLO_CHx	Yes unless masked	MASK_CPUMP_UVLO
Loss of device GND	Yes	Yes	No		No	-
Main FET (GATEx) ON/OFF after inrush duration	Yes	No	-	VOUT_ERR_CHx	No	-
Load wakeup	Yes	No	CHx_FLT	LPM_WAKE_CHx	Yes (Always available)	
VOUT short to ground in LPM	Yes	Bypass FET turned OFF Main FET turns ON	CHx_FLT	LPM_HS_CHx	Yes unless masked	MASK_LPM_HS
VDS overvoltage fault	Yes	Yes	CHx_FLT	VDS_FLT_CHx	Yes unless masked	MASK_VDS_FAULT
Main FET (GATEx) ON/OFF status	Yes	No	SW_STATE_M_CH1 in SW_STATE register		No	
Limphome indication	Yes	Transition to Limphome mode	LIMPHOME_STAT		Yes unless masked	LIMPHOME_STAT_FLT_EN bit in DEV_CONFIG_3 register
OUT_DISx Indication	Yes	Yes	SW_STATE_M_CH1 in SW_STATE register		Yes	
Load current change from forward to reverse direction indication	Yes	No	ISNS_POLARITY_CHx bit in ADC_RESULT_CHx_I		Yes unless masked	ISNS_POLARITY_FLT_EN bit in DEV_CONFIG_2 register

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7.3.6.1 FAULT_GLOBAL [15:8] Bits

The TPS12SxxF-Q1 device outputs the FAULT_GLOBAL [15:8] bits on the SDO header so these status bits can be continuously read during each SPI transaction. The FAULT_GLOBAL [15:8] bits are configurable as read clear or real-time status bits based on the FLT_LTCH_DIS bit setting in the DEV_CONFIG register. The FLT_LTCH_DIS bit however does not apply to the LPM_STATUS bit.

If FLT_LTCH_DIS = 0, then the fault bits are latched and clear only when the associated register in the bit description is read and the fault no longer exists. Table below highlights which registers need to be read to clear

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each of the different fault bits if the fault no longer exists. This is also detailed in each of the bit descriptions in the register map.

Table 7-6. FAULT_GLOBAL[15:8] Bits

BIT	BIT NAME	REGISTER WHICH NEEDS TO BE READ TO CLEAR THE FAULT BIT IF THE FAULT NO LONGER EXISTS
15	Reserved	N/A
14	VS_POR	FAULT_GLOBAL
13	CH2_FLT	FLT_STAT_CH2
12	CH1_FLT	FLT_STAT_CH1
11	LPM_STATUS	-
10	CHAN_OCP_I2T_TSD_OV	FLT_STAT_CHx
9	I2T_MOD	FLT_STAT_CHx
8	GLOBAL_ERR_WRN	FAULT_GLOBAL

If FLT_LTCH_DIS = 1, then the fault bits are not latched and clear when the fault no longer exists.

7.3.7 Output Disable (OUT_DISx) Function

The TPS12SxxF-Q1 device provide a function to quickly disable output channel x in t**OFF_OUT_DIS** if the OUT_DISx pin goes high. The output disable (OUT_DIS) function is used to turn off an output quickly due to an emergency situation where the output must be quickly turned OFF.

This OUT_DIS function is multiplexed with the Direct Input (DI) function on a per channel basis. If DI_OUT_DIS_FN_CHx is set to '1' in the DIAG_CONFIG_CHx register, the DIx/OUT_DISx pin is configured as a OUT_DIS for that channel. Program the masking time using CONFIG_DI_MASK[1:0] bits in case there are any ground bounce issues in the device.

Table 7-7 shows the GATEx state based on the different pin and register configurations for the OUT_DIS function (**OUT_DIS Logic Table when DI_OUT_DIS_FN_CHx = '1'**).

Table 7-7. GATEx States

DI_OUT_DIS_FN_CHx	OUT_DISx	LHI	GATEx - SRCx Voltage
1	Low	Low	Follow CHx_ON
	Low	High	Follow CHx_LH_IN
	High	Low	Low
	High	High	Low

If the OUT_DISx pin is high with the output channel off and the OUT_DISx pin is then asserted low, the output channel follows either the CHx_ON bit if in ACTIVE mode or follow the CHx_LH_IN bits in the LIMPHOME mode. In this scenario, the channel goes through the inrush period based on CAP_CHRG_CHx bits if the CHx_ON bit or the CHx_LH_IN bits are configured for the channel to be enabled.

7.3.8 Brief Supply Interruptions Behavior

The device has integrated supply interruption detection to pass LV124 standard E10 pulse for 12V and LV148 standard E9 pulse for 48V system designs.

7.3.8.1 EVENT1

Whenever input supply voltage goes below $V_{(CSx+_POR)}$ threshold, GATEx drive in turned off. If the supply exceeds again $V_{(CSx+_POR)}$ threshold within t_{CSx_MASK} time programmable using E10_CONFIG_CHx bits then

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GATEx turns on within t_{GATEx_DIxH} duration to minimize voltage droop on output preventing undervoltage of downstream loads. The device does not follow capacitor charging configuration in CAP_CHRG_CHx bits.

7.3.8.2 EVENT2

Whenever input supply voltage goes below $V_{(CSx+_POR)}$ threshold, GATEx drive in turned off. If the supply exceeds again $V_{(CSx+_POR)}$ threshold after t_{CSx_MASK} time programmable using E10_CONFIG_CHx bits then GATEx turns on by following capacitor charging configuration in CAP_CHRG_CHx bits.

Note

It is mandatory to have an RC or a diode plus capacitor filter on the VS pin so that VS voltage remains above $V_{(VS_PORF)}$ threshold during supply interruption period. This filter confirms BSTx to SRCx voltage or chargepump active during supply interruption period.

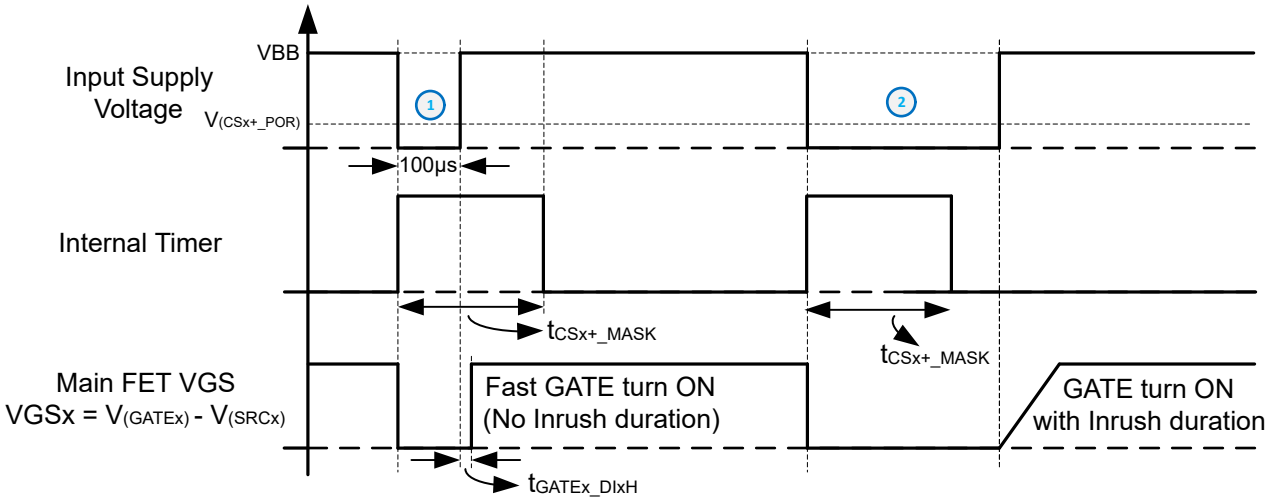


Figure 7-24. TPS12SxxF-Q1 Configuration During Brief Supply Interruption

7.3.9 SPI Mode Operation

The TPS12SxxF-Q1 communicates with the host controller through a high-speed SPI. The interface has three logic inputs: clock (SCLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is tri-stated when the $\overline{CS}$ pin is high. The maximum SPI clock rate is 10MHz, but is limited in practice by the series protection resistor. The device supports simple daisy chain SPI. This mode can be used with or without CRC. The communication between the TPS12SxxF-Q1 and the controller or MCU is through a SPI bus in a primary-secondary configuration. The external MCU is always an SPI primary device that sends command requests on the SDI pin of the TPS12SxxF-Q1 and receives device responses on the SDO pin of the device. The TPS12SxxF-Q1 device is always an SPI secondary device that receives command requests over the SDI line and sends responses (such as status and measured values) to the external MCU over the SDO line. The TPS12SxxF-Q1 device can connect to the primary MCU in the following formats:

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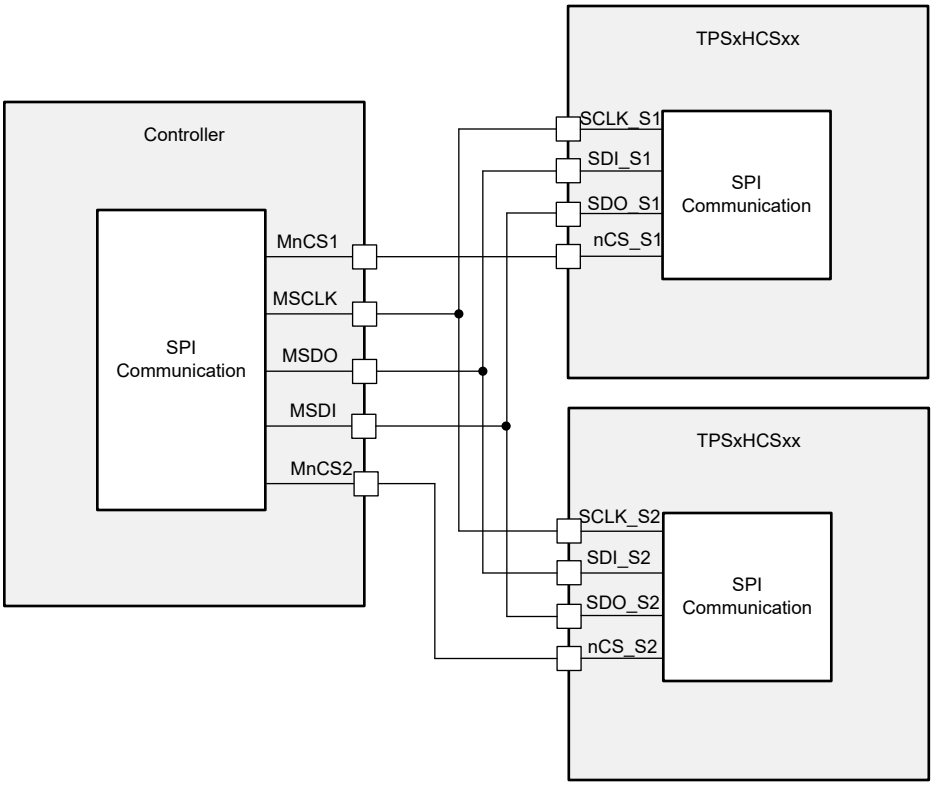


Figure 7-25. Independent Secondary Configuration (Separate nCS Signal)

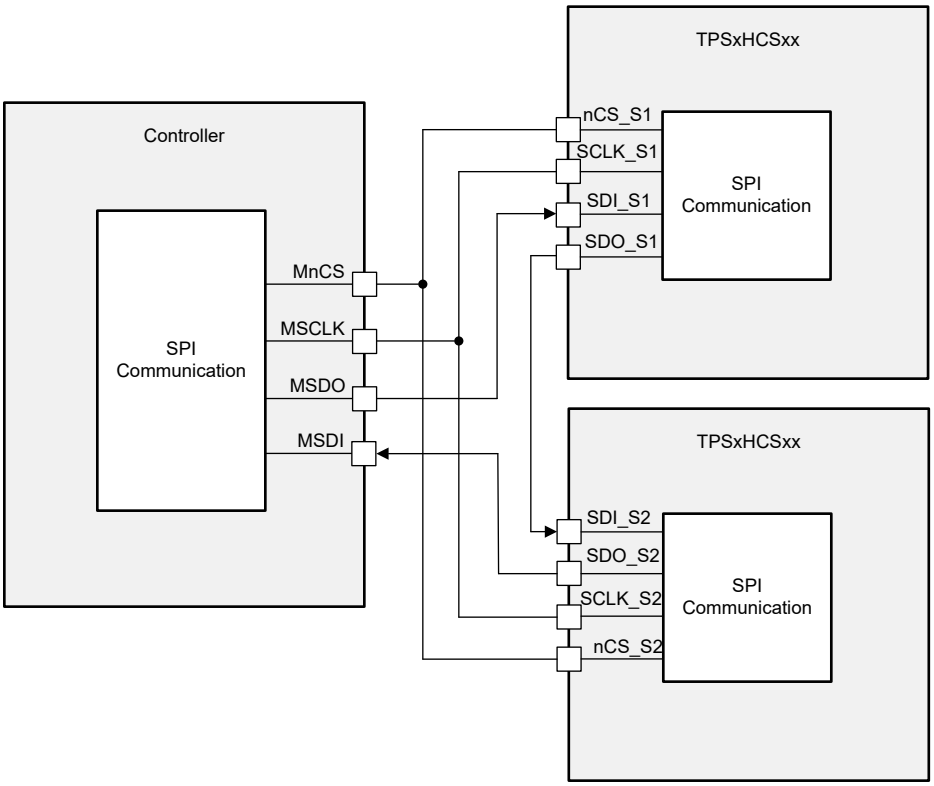


Figure 7-26. Daisy Chain Configuration

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7.3.9.1 SPI

The following sections describe the behavior of the SPI pin.

7.3.9.2 Chip Select ($\overline{CS}$)

The system microcontroller selects the TPS12SxxF-Q1 to receive communication using the CS pin. With the $\overline{CS}$ pin in a logic LOW state, command/configuration words can be sent to the TPS12SxxF-Q1 through the serial input (SDI) pin, and the device information can be retrieved by the microcontroller through the serial output (SDO) pin. The falling edge of the $\overline{CS}$ enables the SDO output and latches the content of the FAULT_GLOBAL register that is sending out on SDO. The microcontroller can issue a READ command to retrieve information stored in the registers. The rising edge on the $\overline{CS}$ pin initiates the following actions: 1. Addressed registers are updated if there is no SPI communication error and if it is an SPI write command. 2. Read clear register is cleared if a READ command to this register is issued during $\overline{CS}$ = LOW. To avoid any corrupted data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. A clean $\overline{CS}$ signal is needed to confirm no incomplete SPI words are sent to the device. This pin is internally pulled up to the VDD rail.

7.3.9.3 System Clock (SCLK)

The system clock (SCLK) pin clocks the internal shift register of the TPS12SxxF-Q1. The SDI data is latched into the input shift register on the falling edge of the SCLK signal. The SDO pin shifts the device stored information out on the rising edge of SCLK. The SDO data is available for the microcontroller to read on the falling edge of SCLK. False clocking of the shift register must be avoided to confirm validity of data and it is essential the SCLK pin be in a logic LOW state whenever CS pin makes any transition. Therefore, it is recommended that the SCLK pin gets pulled to a logic LOW state as long as the device is not accessed and the $\overline{CS}$ pin is at a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SDI pins are ignored and the SDO pin remains as a high-impedance output.

7.3.9.4 Serial Data In (SDI) and Serial Data Out (SDO)

The SDI pin is used for serial instruction data input. SDI information is latched into the input shift register on the falling edge of the SCLK when $\overline{CS}$ is low. The SDO pin is the output from the internal shift register. This pin is internally pulled up to the VDD rail. SDO pin is high-impedance when the CS pin is high. Each successive rising SCLK edge makes the next data bit available for the microcontroller to read on the falling edge of SCLK. SDO goes back to high-impedance when $\overline{CS}$ is high.

7.3.9.5 CRC Error Detection and Checking of Clocks

Setting the CRC_EN bit high enables CRC error detection and CRC is calculated based on 28 bits (including upper nibble of CRC byte on SDI). A CRC-4-ITU-Normal Check Sequence (FCS) is then sent along with each serial transaction. The 4-bit CRC is based on the normal generator polynomial X4+X+1 with CRC starting value = 1111. When CRC is enabled, the TPS12SxxF-Q1 expects a check byte appended to the SDI program/configure data that it receives. To program a complete word, exact bits of information (shown in following table) must be enter into the device. When CRC is disabled, the IC enables register write only if exactly bits have been clocked in. When CRC is enabled, the IC enables register write only if exactly bits have been clocked in with no CRC errors. In case the word length exceeds or does not meet the required length or there is CRC errors, the SPI_ERR bit in the FAULT_GLOBAL register is asserted to logic “1”,and the data received is considered invalid. Note the SPI_ERR bit is not flagged if SCLK is not present. The SPI_ERR is sent back to the SPI Main device on SDO during next chip access. Note that clear on read applies only when there is no SPI error when the register is read.

7.3.9.6 SPI Frame Format

The device uses a 24-bit frame width (when CRC is not used) with the format in Figure 7-27. Please note that the 16-bit wide "Data Out" in the SDO output is always for the previous SPI command frame (Read or Write).

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CRCEN = 0	SDI	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		R(0)	RA6	RA5	RA4	RA3	RA2	RA1	RA0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Read	Register address							Don’t care								Don’t care							
	SDO	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		F15	F14	F13	F12	F11	F10	F9	F8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Register FAULT_GLOBAL (0 x 03) [15:8]								Data out								Data out							

CRCEN = 0	SDI	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		W(1)	RA6	RA5	RA4	RA3	RA2	RA1	RA0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Write	Register address							Data in								Data in							
	SDO	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		F15	F14	F13	F12	F11	F10	F9	F8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Register FAULT_GLOBAL (0 x 03) [15:8]								Data out								Data out							

Figure 7-27. 24-Bit, CRC Disabled (CRC_EN=0)

CRCEN = 1	SDI	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		R(0)	RA6	RA5	RA4	RA3	RA2	RA1	RA0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	x	CRC3	CRC2	CRC1	CRC0
		Read	Register address							Don’t care								Don’t care								CRC BYTE							
	SDO	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		F15	F14	F13	F12	F11	F10	F9	F8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	1	1	1	1	CRC3	CRC2	CRC1	CRC0
		Register FAULT_GLOBAL (0 x 03) [15:8]								Data out								Data out								CRC BYTE							

CRCEN = 1	SDI	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		W(1)	RA6	RA5	RA4	RA3	RA2	RA1	RA0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x	CRC3	CRC2	CRC1	CRC0
		Write	Register address							Data in								Data in								CRC BYTE							
	SDO	Bit31	Bit30	Bit29	Bit28	Bit27	Bit26	Bit25	Bit24	Bit23	Bit22	Bit21	Bit20	Bit19	Bit18	Bit17	Bit16	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		F15	F14	F13	F12	F11	F10	F9	F8	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	1	1	1	1	CRC3	CRC2	CRC1	CRC0
		Register FAULT_GLOBAL (0 x 03) [15:8]								Data out								Data out								CRC BYTE							

Figure 7-28. 32-Bit, CRC Enabled (CRC_EN=1)

7.3.9.7 SPI Watchdog Function

The TPS12SxxF-Q1 device offers an optional SPI watchdog function to monitor for valid SPI transactions from the host controller and loss of the VDD supply. If a valid SPI transaction does not occur in the configurable timeout period, WD_TO, then the $\overline{\text{FLT/WAKE}}$ pin goes low and the WD_ERR bit in the FAULT_GLOBAL register is set to '1'. A valid SPI transaction consists of a SPI transaction with no SPI errors or CRC errors (if enabled). If the VDD supply to the device drops below the VDD_UVLO threshold then SPI on the device is not operational. If the VDD supply remains below the VDD_UVLO for longer than the watchdog time period, then the device issues a watchdog error where the WD_ERR bit is set to 1 and the $\overline{\text{FLT/WAKE}}$ pin goes low unless masked.

The watchdog function is enabled through WD_EN bit in the DEV_CONFIG register. Table below showcases the different configurable watchdog timeout windows, WD_TO.

Table 7-8. Watchdog Timer Settings

WD_TO[1:0] SETTING	WATCHDOG TIMEOUT PERIOD
0x0	400µs
0x1	400ms
0x2	800ms

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Table 7-8. Watchdog Timer Settings (continued)

WD_TO[1:0] SETTING	WATCHDOG TIMEOUT PERIOD
0x3	1200ms

7.4 Device Functional Modes

7.4.1 State Diagram

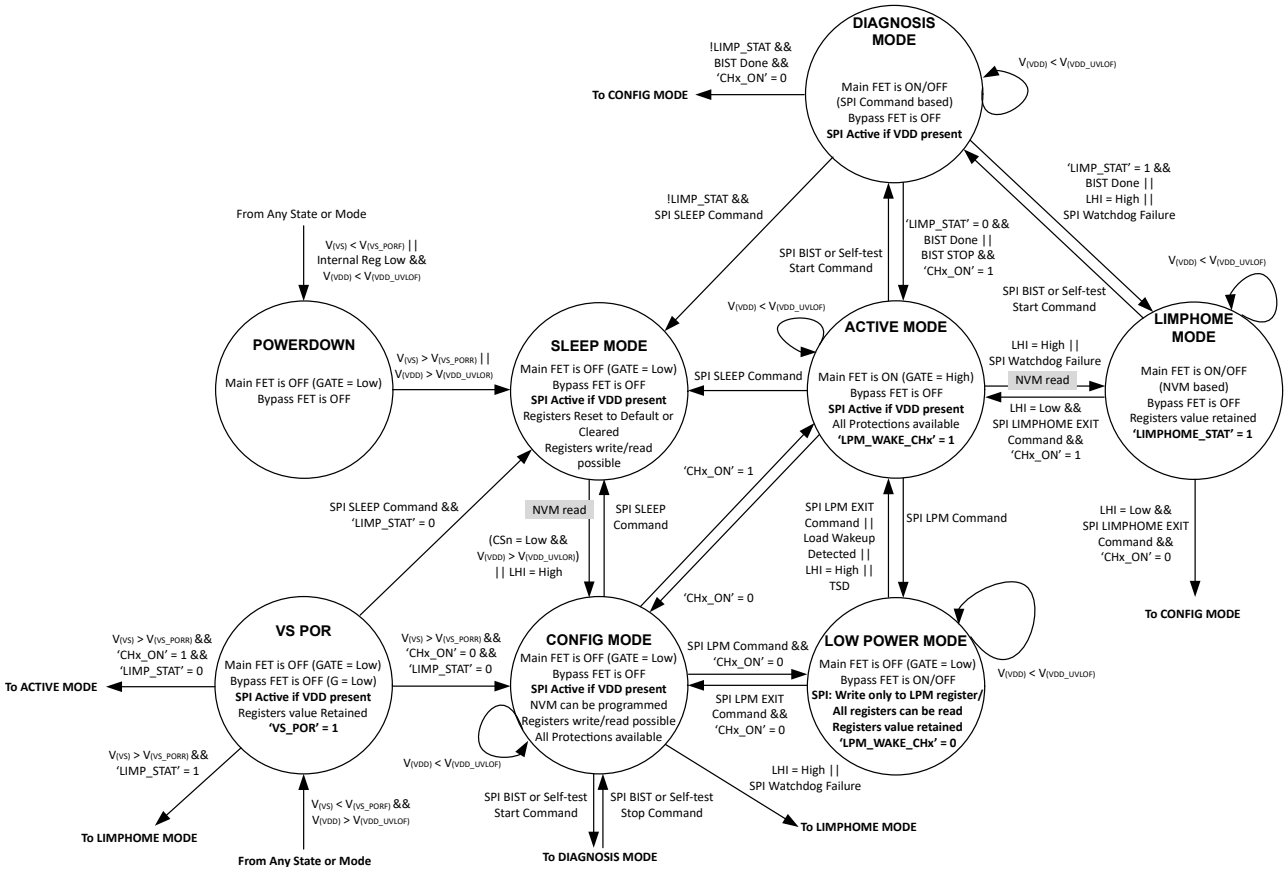


Figure 7-29. State Diagram

7.4.2 Power Down

If applied VS voltage is below $V_{(VS_PORF)}$ and VDD is below $V_{(VDD_PORF)}$ then the device is in disabled state. In this mode, the charge pump and all the protection features are disabled. Both the gate drive outputs (GATEx and Bypass FET) are turned OFF.

7.4.3 Sleep Mode

The TPS12SxxF-Q1 device offers a SLEEP mode where the device is placed into an ultra-low current consumption state. When the device is in SLEEP mode, both gate drives (GATEx and bypass FET) are OFF, registers are cleared and all digital circuits are powered off. The device transitions to this mode if VS < $V_{V(VS_PORR)}$ and VDD < $V_{(VDD_PORR)}$. The device can manually be put into SLEEP mode by writing '1' to the SLEEP bit in the SLEEP register. The device can be woken from the SLEEP mode through the $\overline{CS}$ pin going low. There are two methods to wake the device up from SLEEP through the $\overline{CS}$ pin: 1. Pulse the $\overline{CS}$ pin low for t < t_{READY}. Hold the $\overline{CS}$ pin low for at least t_{READY} and continue to hold $\overline{CS}$ pin low through the first SPI transaction Both methods above results in the device waking up without a SPI_ERR fault. Use a sample SPI transaction to satisfy method number 1 if the sample SPI transaction is completed in t < t_{READY}. Figure below shows examples

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of the two proper wakeup scenarios which results in no SPI_ERR fault and one improper wakeup scenario which results in a SPI_ERR fault. Upon wake up from SLEEP mode, the values in the registers are set to their reset values detailed in the register map below. Additionally, the $\overline{\text{FLT/WAKE}}$ pin is asserted low and the POR, VDD_UVLO, and VBB_UVLO fault bits are asserted and is cleared when the FAULT_GLOBAL register is read if none of these faults currently exist when read.

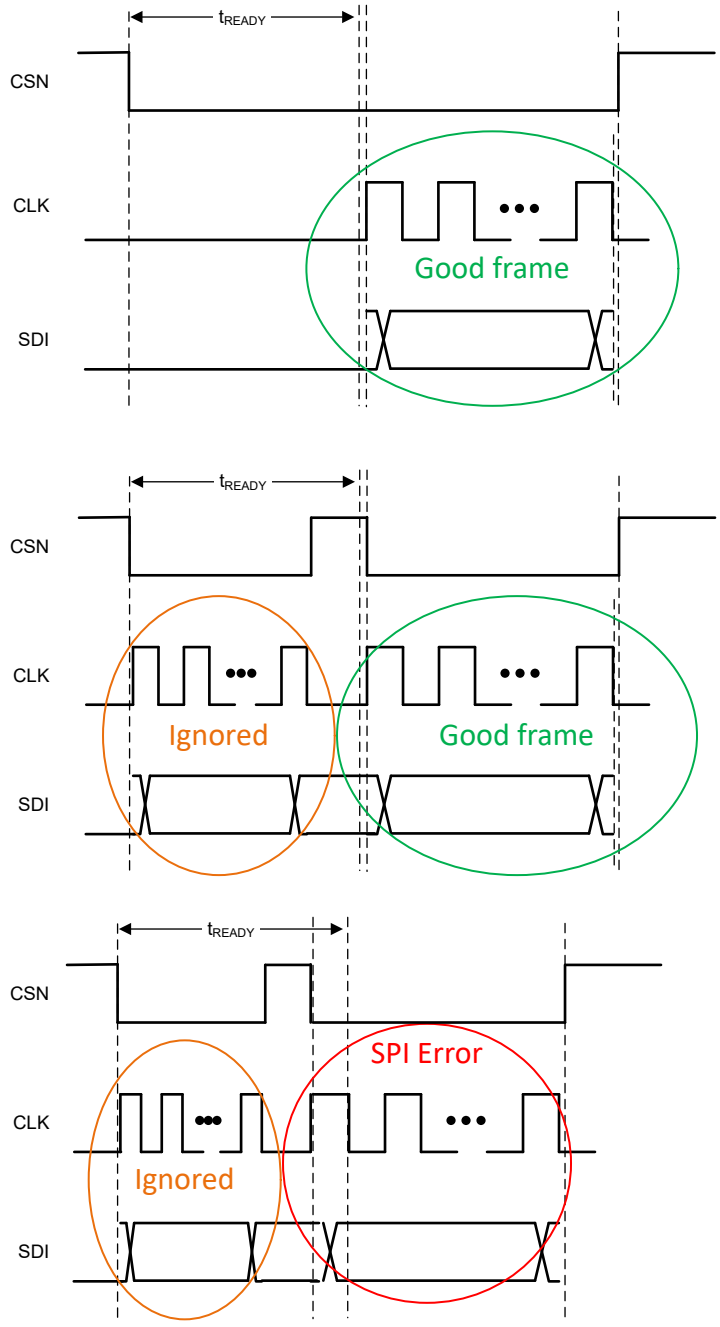


Figure 7-30. Startup Communication Timing

7.4.4 Config or Active Mode (AM)

The CONFIG/ACTIVE mode is where the device stays during normal operation when the gate drives are OFF (CONFIG) or ON (ACTIVE). The difference between the two is that all of the registers can be configured in the CONFIG mode (with the GATEx OFF and Bypass FET OFF). The configuration registers (especially ones

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needed to successfully enable the channel) are expected to be written to before the gate drive can be turned ON, when transitioning from the SLEEP mode (and all the registers are automatically loaded from NVM data). However, the configuration registers are retained while in the LPM and so the device does not need to be reconfigured while transitioning from the LPM to the ACTIVE mode.

SPI communication and diagnostics checks are fully supported in this.

The device can be transitioned into the CONFIG from the SLEEP mode by the $\overline{CS}$ pin going low (a sample SPI command serves this purpose). The device completes the transition through all initializations and functional safety checks. The device transitions to and from the LIMPHOME mode depending on the internal SPI watchdog monitor and the status of the LHI input pin. The device can transition into and out of the LPM by LPM_ENTRY bit in LPM register.

7.4.5 Low Power Mode (LPM)

The device transitions from ACTIVE to low power mode (LPM) whenever LPM_ENTRY bit is set to '1'. In LPM, charge pump is enabled with main FET (GATEx) OFF and bypass FET ON and $\overline{FLT/WAKE}$ pin asserted high in this mode.

The device features two types of loadwakeup mechanism described in subsequent sections

7.4.5.1 Automatic Low Power Mode (LPM) to Active Mode (AUTO_LPM_ENTRY = '0')

When the device is in low-power mode (LPM), LPM_STATUS bit is set '1'. The device transitions from LPM to active mode automatically whenever load current ($I_{CHx(LOAD)}$) exceeds load wakeup trigger threshold ($I_{CHx(LWUx)}$) setting configured in LPM_EXIT_CURR_CHx. After load current exceeds load wakeup threshold, device automatically turns ON the main FET (GATEx) first and bypass FET is turned OFF after main FET (GATEx) has fully turned ON and $\overline{FLT/WAKE}$ pin asserts low indicating the exit from the LPM. LPM_WAKE_CHx bit is also set to '1' in register map and LPM_STATUS bit is also reset to '0'.

Load wakeup deglitch time can be selected in LOAD_WAKE_DEGLITCH setting. AUTO LPM feature has to be disabled by resetting AUTO_LPM_ENTRY bit to '0'.

The device features short circuit current protection in LPM. If the voltage between VBBx to SRCx exceeds $V_{CHx(LPM_SCP)}$ threshold then bypass FET is turned OFF in nanoseconds and main FET (GATEx) is turned ON within t_{LPM_SC} time along with $\overline{FLT/WAKE}$ pin asserted low. LPM_HS_CHx bit is set to '1' to indicate short-circuit in low-power mode which can be read by MCU over SPI.

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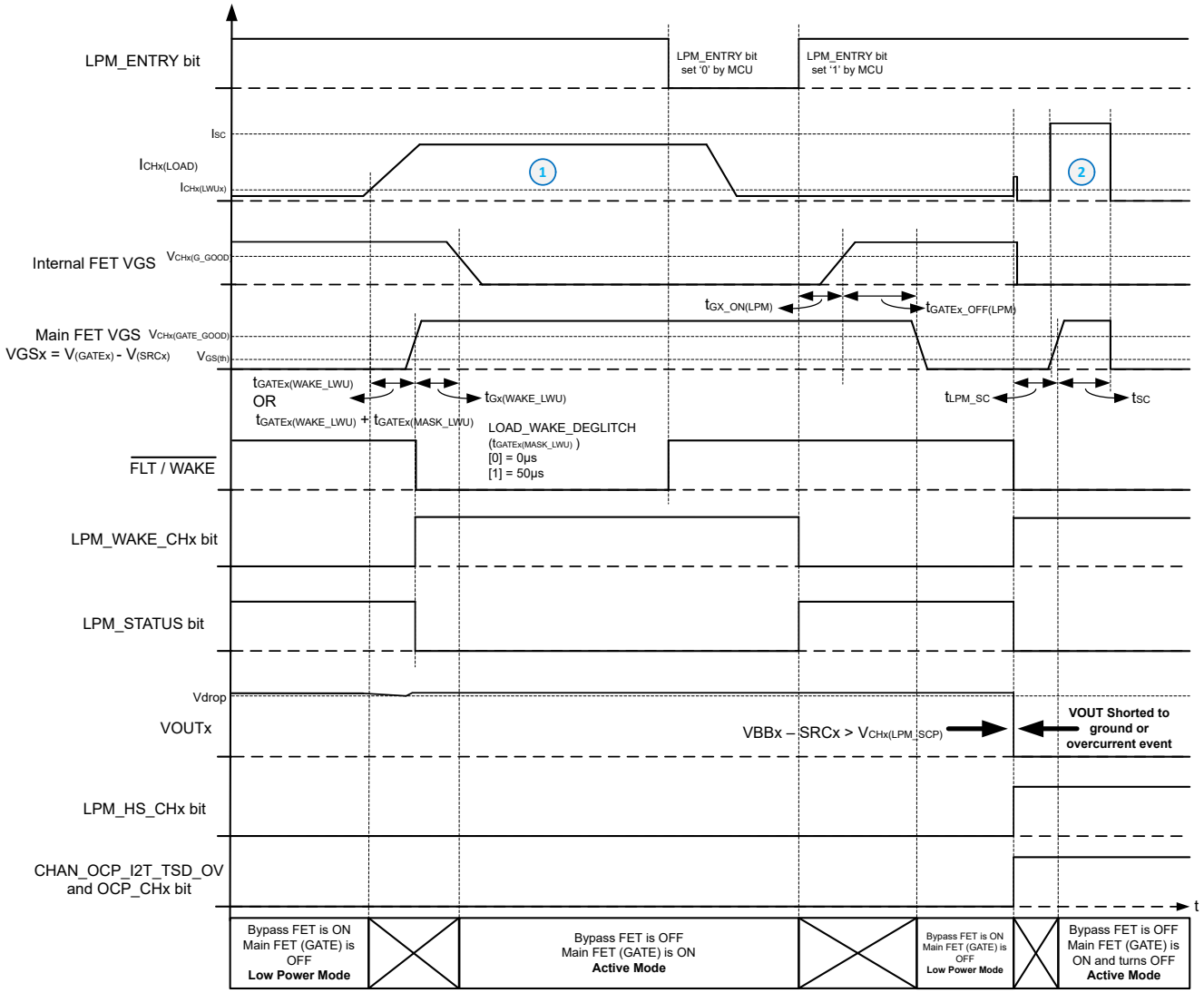


Figure 7-31. Timing Diagram for Loadwakeup and VOUT Shorted to Ground Fault in LPM

7.4.5.2 Automatic Low Power Mode (LPM) to Active Mode to LPM (AUTO LPM) for ECU polling (AUTO_LPM_ENTRY = '1')

The TPS12SxxF-Q1 has integrated AUTO LPM feature which can be enabled by AUTO_LPM_ENTRY bit in DEV_CONFIG register. AUTO LPM functionality provides flexibility for the device to automatically transition from active to a low IQ LPM while keeping power available to output at all times.

If AUTO_LPM_ENTRY bit is set to '1' and loadwakeup is detected by device ($I_{CHx(LOAD)}$ > $I_{CHx(LWUx)}$) then device starts internal timer ($t_{LPM_WAKE_DEGLITCH}$) based on LPM_WAKE_DEGLITCH timer setting in LPM register. After the 500us (current sense amplifier startup and settling time), device sense V_{SNSx} ($I_{CHx(LOAD)}$ × RSNSx) voltage through CSx+ and CSx- pin and starts comparing VSNSx with fixed $V_{CHx(AUTO_LPM_THS)}$ (1mV typical) threshold.

7.4.5.2.1 EVENT1

If sensed VSNSx goes **below** $V_{CHx(AUTO_LPM_THS)}$ within LPM_WAKE_DEGLITCH timer and VSNSx stays below $V_{CHx(AUTO_LPM_THS)}$ threshold for AUTO_LPM_FILTER setting then device automatically transitions to LPM by turning on the bypass FET and then turning off the main path (GATEx drive). $\overline{\text{FLT / WAKE}}$ is not asserted and remains high.

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Note

It is recommended to set LPM_WAKE_DEGLITCH time more than loadwakeup current pulse time plus AUTO_LPM_FILTER setting, otherwise device stays in active mode and does not transition to LPM automatically.

7.4.5.2.2 EVENT2

If sensed VSNSx stays **above** $V_{CHx(AUTO_LPM_THS)}$ within LPM_WAKE_DEGLITCH timer setting then device remains in active mode with the main path on (GATEx drive). $\overline{FLT/WAKE}$ is asserted low to indication WAKE to the MCU. MCU can reset LPM_ENTRY bit to '0' to de-assert the $\overline{FLT/WAKE}$ pin to high.

7.4.5.2.3 EVENT3

LPM_WAKE_DEGLITCH and AUTO_LPM_FILTER setting is only enabled when load wake-up is detected. These settings are disabled when $\overline{FLT/WAKE}$ is asserted low once.

The device features short-circuit current protection in LPM. If the voltage between VBBx to SRCx exceeds $V_{CHx(LPM_SCP)}$ threshold then bypass FET is turned OFF in nanoseconds and main FET (GATEx) is turned ON within t_{LPM_SC} time along with $\overline{FLT/WAKE}$ pin asserted low as shown in above image as **EVENT 2**. LPM_HS_CHx bit is set to '1' to indicate short circuit in low-power mode which can be read by MCU over SPI.

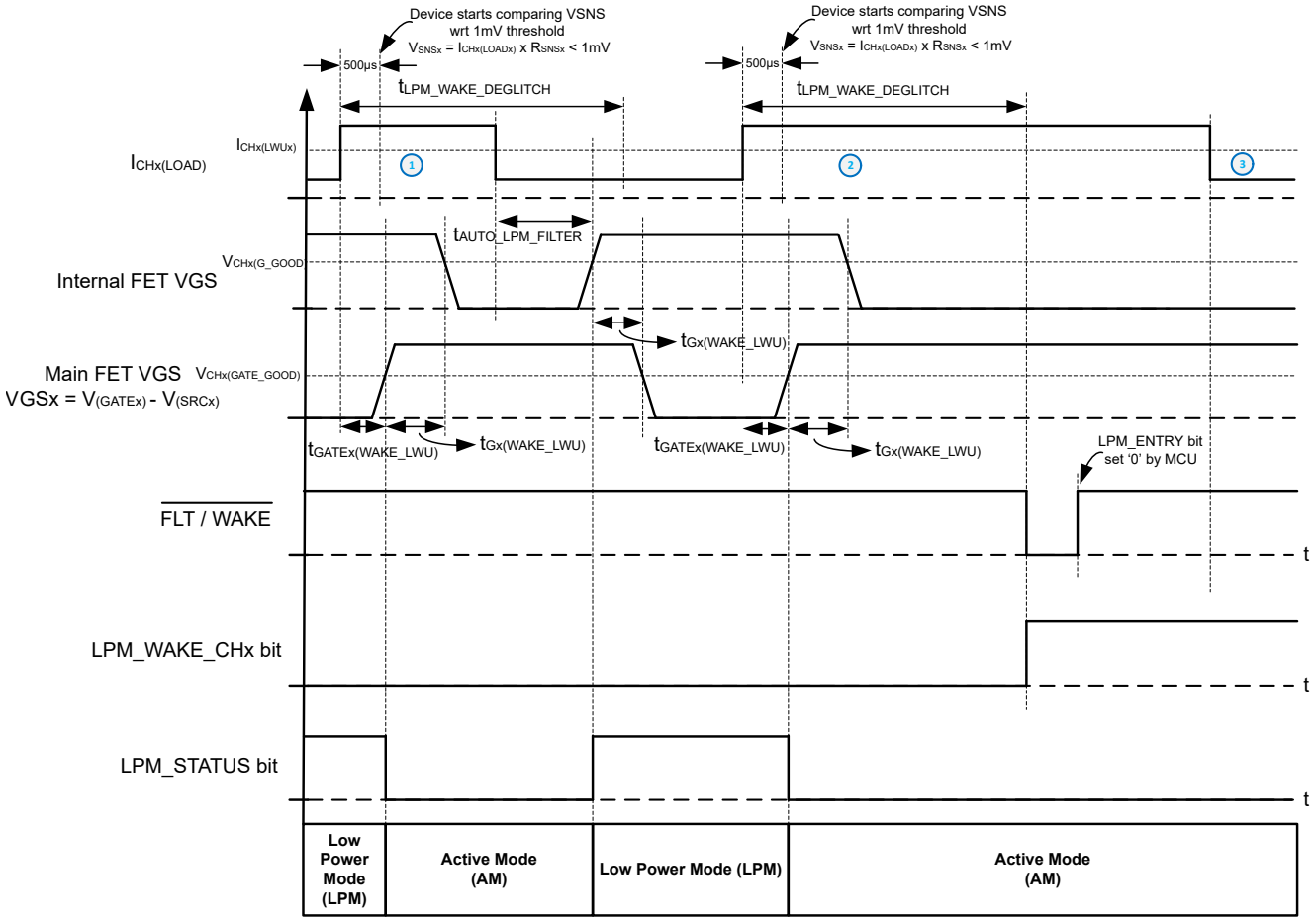


Figure 7-32. Timing Diagram For Loadwakeup With Automatic LPM Entry For ECU Polling

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7.4.6 Limphome Mode

The device offers a LIMPHOME mode to set the outputs to a desired safe state (high, low, keep state, or according DIx) in case of a SPI communication failure, system-level failure (for example, car crash), or MCU failure (software or hardware). Place the device can into the LIMPHOME mode through the following ways:

- LHI is pulled high
- Watchdog timeout error

The state of the output in LIMPHOME are determined by the CHx_LH_IN bits. Depending on the DI_OUT_DIS_FN_CHx bit setting the CHx_LH_IN settings can vary. See the below tables for more details on this. See the Output Disable (OUT_DIS) Function section for more details on the DI_OUT_DIS_FN_CHx bit and OUT_DIS function.

Table 7-9. Limp Home Channel Control Options - DI_OUT_DIS_FN_CHx = '0'

DEV_CONFIG	10:9	CHx_LH_IN	R/W	2b00	These bits determine how the channel × output must respond in LIMPHOME mode.	0b00 = DI pin controls the output when in LIMPHOME mode 0b01 = Keeps the same output state from CHx_ON bit when entering LIMPHOME mode 0b10 = Output is OFF in LIMPHOME mode 0b11 = Output is ON in LIMPHOME mode

Table 7-10. Limp Home Channel Control Options - DI_OUT_DIS_FN_CHx = '1'

DEV_CONFIG	10:9	CHx_LH_IN	R/W	2b00	These bits determine how the channel × output must respond in LIMPHOME mode.	0b00 = Output is OFF in LIMPHOME mode 0b01 = Keeps the same output state from CHx_ON bit when entering LIMPHOME mode 0b10 = Output is OFF in LIMPHOME mode 0b11 = Output is ON in LIMPHOME mode

The register values are retained in the LIMPHOME mode. When the device enters LIMPHOME mode, the LIMPHOME_STAT bit in the FAULT_GLOBAL register is set high. In LIMPHOME mode, registers can be read but no write transactions can occur other than to clear the LIMPHOME_STAT bit in the FAULT_GLOBAL register to exit LIMPHOME mode.

To clear the LIMPHOME_STAT bit, the LHI pin has to be pulled low and a '1' has to be written to the LIMPHOME_STAT bit to clear the bit and to allow for the device to exit the LIMPHOME mode. Once the device exits LIMPHOME mode to ACTIVE mode, the device has full read and write access.

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7.5 TPS12S24F-Q1 Pre-Production Silicon Limitations

Table 7-11. Summary of Pre-Production Silicon Limitations

PARAMETER	TEST CONDITION/ EXPLANATION	OBSERVATION IN PRE-PRODUCTION SILICON	EXPECTED BEHAVIOR. TO BE FIXED IN PRODUCTION SILICON
Current sense Accuracy	VSNSx = 6mV, GAINx setting = 50V/V	VIMONx pin voltage = 243.5mV ISNS register value: ADC_RESULT_CHx_I = 87 **ISNS accuracy is 12%**	VIMONx pin voltage = 275mV ISNS register value: ADC_RESULT_CHx_I = 101 **ISNS digital sense accuracy must be (7%).** **I2T accuracy directly impact by ISNS accuracy.**
SCP in LPM	Output Short to ground in LPM. Bypass FET turn off instantly and main FET turn on	LPM bypass FET Thermal shutdown bit goes **'1'** LPM_HS_CHx bit remains **'0'**	LPM bypass FET Thermal shutdown remains **'0'** LPM_HS_CHx bit must go to **'1'** **Functionality is working but wrong indication**
WAKE Indication	•	Gate going high within 7.5us after loadwakeup detection but $\overline{\text{FLT/WAKE}}$ pin goes low after **50usec**	$\overline{\text{FLT/WAKE}}$ pin goes low after **5usec**. **No major impact at system level**
GLOBAL_ERR_FLT register read	Observed only after LPM Exit Working normally in active mode	VBB_UV_WRN = **'1'** GLOBAL_ERR = **'1'**	VBB_UV_WRN = **'0'** GLOBAL_ERR = **'0'** **No major impact at the system level**.
SDO pin state	CSn pulled low to high	SDO retains LSB of last data value. Cannot support parallel SPI.	SDO must be tri-state when CSn is pulled low to high.
GND Loss Detection	Device GND floating or high slew rate transient (10V/us) lifting GND pin >2V threshold	Gate turns off. Digital gets stuck (SPI Write does not work) because internal oscillator is susceptible to high slew rate on GND which can occur due to poor grounding or hot-swapping	The GATEx must turn off. GATEx must turn on automatically when GND is restored and SPI Write/ Read works normally.
Charge pump UVLO	CPUVLO falling threshold	8V. Device can detect CPUVLO during FET turn off if C_{BSTx} is not sized properly.	Should be 6.5V. Use CBST > 10x [Ciss (external FET) + CGATEx]
FET Short BIST	Run FET short BIST on CH1 and CH2	FET Short BIST indication works only for CH2.	FET Short BIST indication works for CH1 and CH2.
Open load detection	Run OL detection on CH1 and CH2	OL detection indication works only for CH2.	OL detection indication works for CH1 and CH2.

7.5.1 SDO Pin Tristate Workaround (Only for Parallel SPI Configuration, not for Daisy-Chain)

Figure 7-33 shows SN74LVC1G125 based circuit needed on SDO pin of each slave device when multiple TPS12S24F-Q1 devices are used in parallel SPI configuration.

- $\overline{\text{CS}}$ goes low, Buffer turn on to connect master MCU with respective slave device SDO pin
- $\overline{\text{CS}}$ goes high, Buffer turns off disconnecting SDO pin of slave device from master MCU and SDO pins of other slave devices

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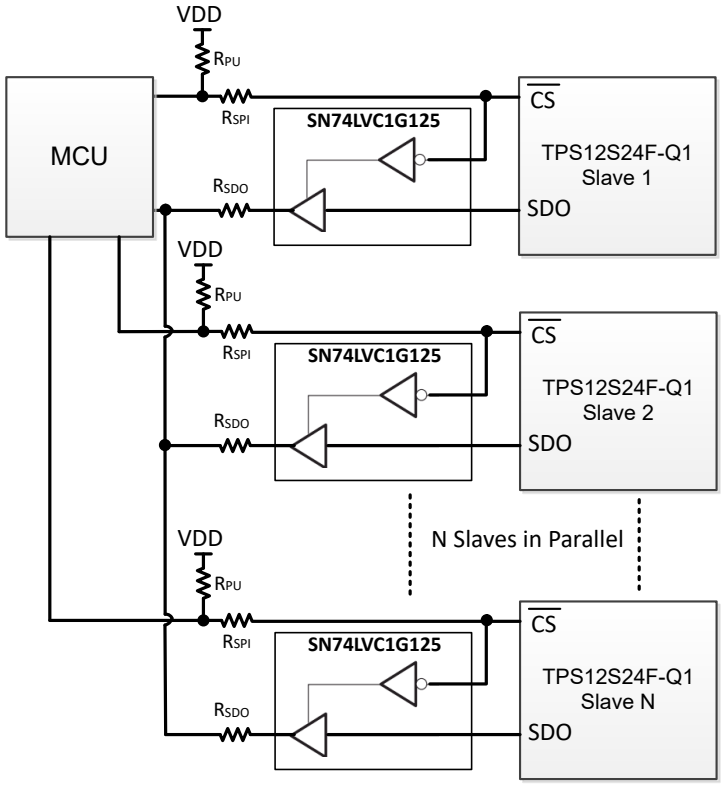


Figure 7-33. SDO Tristate Discrete Circuit Implementation

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8 Register Maps

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8.1 TPS12S24F-Q1 Registers

Table 8-1 lists the memory-mapped registers for the TPS12S24F-Q1 registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. TPS12S24F-Q1 Registers

Offset	Acronym	Register Name	Section
0h	DEV_ID	Read the device ID from NVM	Section 8.1.1
1h	SLEEP	Sets to go into SLEEP sate from ACTIVE or STANDBY state	Section 8.1.2
2h	LPM	Sets to go in or out of Low power mode (LPM STATE)	Section 8.1.3
3h	FAULT_GLOBAL	Faults for any channel and global faults	Section 8.1.4
4h	FAULT_MASK	Mask the reporting of the faults on the fault pin	Section 8.1.5
5h	BIST_RESULT	BIST Diagniostic result	Section 8.1.6
6h	SW_STATE	Turn on/off GATEx	Section 8.1.7
7h	DEVICE_TEST	Device Status, Limphome, and locking set by SPI	Section 8.1.8
8h	DEV_CONFIG	Device Configureable settings register	Section 8.1.9
9h	ADC_CONFIG	ADC configuration - disable ADC conversions or ADC entirely	Section 8.1.10
Ah	ADC_RESULT_VBB	ADC conversion result VBB	Section 8.1.11
Bh	ADC_RESULT_BIST	ADC conversion result BIST	Section 8.1.12
Ch	FLT_STAT_CH1	Status of the channels and channel faults	Section 8.1.13
Dh	PWM_CH1	Set all PWM configurations for channel 1	Section 8.1.14
Eh	ILIM_CONFIG_CH1	Set all current limit configuration for channel 1	Section 8.1.15
Fh	DIAG_CONFIG_CH1	Configuration register for channel 1	Section 8.1.16
10h	ADC_RESULT_CH1_I	ADC conversion result load current sense CH1	Section 8.1.17
11h	ADC_RESULT_CH1_T	ADC conversion result TJ sense CH1	Section 8.1.18
12h	ADC_RESULT_CH1_V	ADC conversion result VOUT sense CH1	Section 8.1.19
13h	ADC_RESULT_CH1_VDS	ADC conversion result VDS sense CH1	Section 8.1.20
14h	I2T_CONFIG_CH1	Set all I2T configuration bits	Section 8.1.21
15h	FLT_STAT_CH2	Status of the channels and channel faults	Section 8.1.22
16h	PWM_CH2	Set all PWM configurations for channel 2	Section 8.1.23
17h	ILIM_CONFIG_CH2	Set all current limit configuration for channel 2	Section 8.1.24
18h	DIAG_CONFIG_CH2	Configuration register for channel 2	Section 8.1.25
19h	ADC_RESULT_CH2_I	ADC conversion result load current sense CH2	Section 8.1.26
1Ah	ADC_RESULT_CH2_T	ADC conversion result TJ sense CH2	Section 8.1.27
1Bh	ADC_RESULT_CH2_V	ADC conversion result VOUT sense CH2	Section 8.1.28
1Ch	ADC_RESULT_CH2_VDS	ADC conversion result VDS sense CH2	Section 8.1.29
1Dh	I2T_CONFIG_CH2	Set all I2T configuration bits	Section 8.1.30
1Eh	I2T_TRIP_CH1	I2T_TRIP configuration bit, 8 bit per channel	Section 8.1.31
1Fh	I2T_ACC_RD_CH1	I2T_ACCUM % related yto I2T_TRIP	Section 8.1.32
20h	I2T_ACC_RD_CH2	I2T_ACCUM % related yto I2T_TRIP	Section 8.1.33
33h	I2T_TRIP_CH2	I2T_TRIP configuration bit, 8 bit per channel	Section 8.1.34
34h	ADC_RESULT_TCONT	TCONT read out	Section 8.1.35
35h	SCP_CONFIG_CH1	SCP configuration for the Device	Section 8.1.36
36h	SCP_CONFIG_CH2	SCP configuration for the Device	Section 8.1.37
37h	UV_CONFIG_CH1	Under Voltage for the Device CH1	Section 8.1.38
38h	UV_CONFIG_CH2	Under Voltage for the Device CH2	Section 8.1.39
39h	OV_CONFIG_CH1	Over Voltage for the Device CH1	Section 8.1.40

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Table 8-1. TPS12S24F-Q1 Registers (continued)

Offset	Acronym	Register Name	Section
3Ah	OV_CONFIG_CH2	Over Voltage for the Device CH2	Section 8.1.41
3Bh	VDS_CONFIG	VDS sense for the Device	Section 8.1.42
3Ch	TEMP_CONFIG	Temp Settings	Section 8.1.43
3Dh	DEV_CONFIG_2	Device Configureable settings register	Section 8.1.44
3Eh	DEV_CONFIG_3	Device Configureable settings register	Section 8.1.45
3Fh	EEPROM_PROGRAM_CONTROL_STATUS	Customer EEPROM program control/status reg	Section 8.1.46

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. TPS12S24F-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

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8.1.1 DEV_ID Register (Offset = 0h) [Reset = 0000h]

DEV_ID is shown in Table 8-3.

Return to the Summary Table.

Table 8-3. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEV_ID	R	0h	Read the unique device ID A123h = TPS12S24F_Pre-production Silicon

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8.1.2 SLEEP Register (Offset = 1h) [Reset = FFFEh]

SLEEP is shown in Table 8-4.

Return to the Summary Table.

Table 8-4. SLEEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	7FFFh	Reserved
0	SLEEP	R/W	0h	Setting this bit to 1 puts the device into SLEEP mode where everything shuts off

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8.1.3 LPM Register (Offset = 2h) [Reset = 3F0Eh]

LPM is shown in Table 8-5.

Return to the Summary Table.

Table 8-5. LPM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	LPM_WAKE_DEGLITCH	R/W	0h	Sets the Deglitch time for AUTO LPM exit from loadwakeup to FLT/ WAKEn signal assertion 0h = 1ms 1h = 10ms 2h = 20ms 3h = 100ms
13-8	RESERVED	R	3Fh	Reserved
7-6	LPM_EXIT_CURR_CH2	R/W	0h	Set the threshold for exit from LPM due to load current increase - CH2. 0h = 100mA 1h = 200mA 2h = 400mA 3h = 780mA
5-4	LPM_EXIT_CURR_CH1	R/W	0h	Set the threshold for exit from LPM due to load current increase - CH1. 0h = 100mA 1h = 200mA 2h = 400mA 3h = 780mA
3-1	RESERVED	R	7h	Reserved
0	LPM_ENTRY	R/W	0h	Setting this bit to 1 puts the device into LPM 0h = No change 1h = Device enters to LPM from ACTIVE / CONFIG mode

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8.1.4 FAULT_GLOBAL Register (Offset = 3h) [Reset = 8147h]

FAULT_GLOBAL is shown in Table 8-6.

Return to the Summary Table.

Table 8-6. FAULT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1h	Reserved
14	VS_POR	R	0h	The bit is set if VS supply is below the POR threshold at any time. The fault bit is cleared if the FAULT_GLOBAL register is read and the POR condition is removed 0h = No VS POR fault 1h = VS POR fault
13	CH2_FLT	R	0h	The bit is set if there is a fault (on or off-state fault) in channel 2. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CH2 register is read and the fault condition no longer exists. 0h = no on or off-state fault in CH2 1h = On or off-state fault in CH2
12	CH1_FLT	R	0h	The bit is set if there is a fault (on or off-state fault) in channel 1. If FLT_LTCH_DIS bit is set, then the fault bit is latched and is cleared only when the FLT_STAT_CH1 register is read and the fault condition no longer exists. 0h = no on or off-state fault in CH1 1h = On or off-state fault in CH1
11	LPM_STATUS	R	0h	The bit is set if the device is in Low Power Mode (LPM) state and is cleared only when the device is in the ACTIVE state. 0h = Device is not in the LPM mode 1h = Device has entered the LPM mode
10	CHAN_OCP_I2T_TSD_OV	R	0h	The bit is set if there is an overcurrent protection or I2T protection or external FET thermal shutdown or over voltage protection fault in any one of the channels. If FLT_LTCH_DIS bit is 0, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition no longer exists. 0h = no overcurrent protection, I2T protection, external FET thermal shutdown or over voltage protection fault in any of the channels 1h = Overcurrent protection or I2T protection or external FET thermal shutdown or over voltage protection fault in one of the channels
9	I2T_MOD	R	0h	This bit is Set 1 if any of the channel enters the I2T mode
8	GLOBAL_ERR_WRN	R	1h	The bit is set if there is a global fault reported in the FAULT_GLOBAL register : SPI error, watchdog error, VBB_UVLO, VBB_UV_WRN, VDD_UVLO, POR fault or LIMPHOME_STAT bit is set. If FLT_LTCH_DIS bit is 0, then the fault bit is latched and is cleared only when the FAULT_GLOBAL register is read and the fault condition no longer exists. 0h = no global fault 1h = One of the following errors have occurred: SPI error, watchdog error, VBB_UVLO, VBB_UV_WRN, VDD_UVLO, POR fault or LIMPHOME_STAT bit is set.
7	LIMPHOME_STAT	W1C	0h	This bit is set high if the device is currently in the LIMPHOME mode.
6	POR	RC	1h	The bit is indicative of whether a power on reset has occurred. 0h = There is no power-on reset anytime after the last register read. The register bit is cleared on read, so if read again and the bit is 0, means that no power-on reset has occurred since the read. 1h = A power-on reset has occurred since the last register read.
5	LPM_STATUS_LATCH	RC	0h	The bit is set if the device is in Low Power Mode (LPM). This bit is cleared only when the FAULT_GLOBAL register is read and the device is in the ACTIVE state. 0h = Device is not in the LPM state 1h = Device has entered the LPM state

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Table 8-6. FAULT_GLOBAL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPI_ERR	RC	0h	The bit is set if there is an SPI communication error either from format, clock or CRC errors.The fault bit is latched and cleared only after FAULT_GLOBAL read and the error is removed. 0h = No SPI communication error fault 1h = SPI communication error either from format, clock or CRC has occurred
3	WD_ERR	RC	0h	The bit is set if the watchdog timer is enabled and there has not been an acceptable SPI command in the watchdog timeout window. The fault bit is latched and cleared only after FAULT_GLOBAL read and the error is removed. 0h = No SPI interface watchdog error 1h = SPI watchdog timeout error has occurred
2	VDD_UVLO	RC	1h	The bit is set if VDD supply is below the UVLO threshold at any time. The fault bit is cleared if the FAULT_GLOBAL register is read and the UVLO condition is removed 0h = No VDD UVLO fault 1h = VDD UVLO fault
1	VBB_UV_WRN	RC	1h	The bit is set if VBB supply is below the UV warning (UV_WRN) threshold at any time. The fault bit is cleared if the FAULT_GLOBAL register is read and the UV condition is removed 0h = No VBB UV_WRN fault 1h = VBB UV_WRN fault
0	VBB_UVLO	RC	1h	The bit is set if VBB supply is below the UV threshold at any time. The fault bit is cleared if the FAULT_GLOBAL register is read and the UV condition is removed 0h = No VBB UVLO fault 1h = VBB UVLO fault

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8.1.5 FAULT_MASK Register (Offset = 4h) [Reset = 0000h]

FAULT_MASK is shown in Table 8-7.

Return to the Summary Table.

Table 8-7. FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MASK_REV_POL_FLT	R/W	0h	The bit is set to mask the Input Reverse Polarity fault signaling on the FLT pin output. 0h = Input Reverse Polarity Fault is signaled on the FLT pin 1h = Input Reverse Polarity fault is not signaled (masked from) on the FLT pin
14	MASK_VBB_OVLO	R/W	0h	The bit is set to mask the supply voltage VBB OVLO fault signaling on the FLT pin output. 0h = VBB OVLO fault is signaled on the FLT pin 1h = VBB OV fault is not signaled (masked from) on the FLT pin
13	MASK_CPUVLO	R/W	0h	The bit is set to mask the signaling CPUMP UVLO fault on the FLT pin 0h = CPUVLO Fault is signaled on the FLT pin 1h = CPUVLO fault is not signaled (masked from) on the FLT pin
12	MASK_VDS_FAULT	R/W	0h	The bit is set to mask the signaling VDS protection fault on the FLT pin 0h = VDS Fault is signaled on the FLT pin 1h = VDS fault is not signaled (masked from) on the FLT pin
11	MASK_LPM_HS	R/W	0h	The bit is set to mask the signaling LPM Hard Short protection fault on the FLT pin 0h = LPM Hard Short Fault is signaled on the FLT pin 1h = LPM Hard Short fault is not signaled (masked from) on the FLT pin
10	MASK_NVM_CRC_ERR	R/W	0h	The bit is set to mask the signaling NVM_CRC_ERR fault on the FLT pin 0h = NVM_CRC_ERR Fault is signaled on the FLT 1h = NVM_CRC_ERR fault is not signaled (masked from) on the FLT pin
9	MASK_I2T_TRIP	R/W	0h	The bit is set to mask the signaling I2T protection fault on the FLT pin 0h = I2T Fault is signaled on the FLT pin on I2T Trip 1h = I2T Trip Protection fault is not signaled (masked from) on the FLT pin
8	MASK_VDD_UVLO	R/W	0h	The bit is set to mask the supply voltage VDD UVLO fault signaling on the FLT pin output. 0h = VDD UVLO fault is signaled on the FLT pin 1h = VDD UVLO fault is not signaled (masked from) on the FLT pin
7	MASK_OCP	R/W	0h	The bit is set to mask the signaling short circuit protection fault (CB_CHx / SCP_CHx) fault on the FLT pin 1h = SCP Fault is signaled on the FLT pin
6	MASK_FET_SHRT	R/W	0h	The bit is set to mask the signaling Fet short fault on the FLT pin 0h = FET Short fault is signaled on the FLT pin 1h = FET Short fault is not signaled (masked from) on the FLT pin
5	MASK_SHRT_VBB	R/W	0h	The bit is set to mask the signaling off-state Short to VBB fault on the FLT pin 0h = Short to VBB Fault is signaled on the FLT pin 1h = Short to VBB fault is not signaled (masked from) on the FLT pin
4	MASK_OL_OFF	R/W	0h	The bit is set to mask the signaling off-state open load fault on the FLT pin 0h = Off-state wire-break fault is signaled on the FLT pin 1h = Off-state wire-break fault is not signaled (masked from) on the FLT pin
3	MASK_TSD	R/W	0h	The bit is set to mask the signaling TSD (external FET overtemperature protection) fault on the FLT pin 1h = TSD Fault is signaled on the FLT pin

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Table 8-7. FAULT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	MASK_SPI_ERR	R/W	0h	The bit is set to mask the SPI error (SPI_ERR) signaling on the FLT pin 0h = SPI error is signaled on FLT pin 1h = FLT pin not impacted by SPI error
1	MASK_WD_ERR	R/W	0h	The bit is set to mask the SPI watchdog error (WD_ERR) signaling on the FLT pin 0h = SPI watchdog error is signaled on FLT pin 1h = FLT pin not impacted by SPI watchdog error
0	MASK_VBB_UVLO	R/W	0h	The bit is set to mask the supply voltage VBB UVLO fault signaling on the FLT pin output. 0h = VBB UVLO fault is signaled on the FLT pin 1h = VBB UVLO fault is not signaled (masked from) on the FLT pin

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8.1.6 BIST_RESULT Register (Offset = 5h) [Reset = 0000h]

BIST_RESULT is shown in Table 8-8.

Return to the Summary Table.

Table 8-8. BIST_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIST_FORCED_EXIT	RC	0h	The bit is set to 1 in case the any BIST exited due to abnormal forced condition, it gets cleared once BIST_RESULT register is read and no more abnormal exit happens 0h = BIST didn't exit forcibly 1h = One or more BIST exited forcibly
14	UV_BIST_ERR_CH2	RC	0h	The bit is set to 1 in case the UV BIST check detects an error for CH2 0h = BIST for UV Passed for CH2 1h = BIST for UV Failed for CH2
13	OV_BIST_ERR_CH2	RC	0h	The bit is set to 1 in case the OV BIST check detects an error for CH2 0h = BIST for OV Passed for CH2 1h = BIST for OV Failed for CH2
12	VDS_BIST_ERR_CH2	RC	0h	The bit is set to 1 in case the VDS BIST check detects an error for CH1 0h = BIST for VDS CH1 Passed 1h = BIST for VDS CH1 Failed
11	TSNS_BIST_ERR_CH2	RC	0h	The bit is set to 1 in case the TSNS BIST check detects an error for CH1 0h = BIST for TSNS CH1 Passed 1h = BIST for TSNS CH1 Failed
10	SCP_BIST_ERR_CH2	RC	0h	The bit is set to 1 in case the SCP BIST check detects an error for CH1 0h = BIST for SCP CH1 Passed 1h = BIST for SCP CH1 Failed
9	UV_BIST_ERR_CH1	RC	0h	The bit is set to 1 in case the UV BIST check detects an error 0h = BIST for UV Passed 1h = BIST for UV Failed
8	OV_BIST_ERR_CH1	RC	0h	The bit is set to 1 in case the OV BIST check detects an error 0h = BIST for OV Passed 1h = BIST for OV Failed
7	VDS_BIST_ERR_CH1	RC	0h	The bit is set to 1 in case the VDS BIST check detects an error for CH1 0h = BIST for VDS CH1 Passed 1h = BIST for VDS CH1 Failed
6	TSNS_BIST_ERR_CH1	RC	0h	The bit is set to 1 in case the TSNS BIST check detects an error for CH1 0h = BIST for TSNS CH1 Passed 1h = BIST for TSNS CH1 Failed
5	SCP_BIST_ERR_CH1	RC	0h	The bit is set to 1 in case the SCP BIST check detects an error for CH1 0h = BIST for SCP CH1 Passed 1h = BIST for SCP CH1 Failed
4	NVM_CRC_ERR	R	0h	The bit is set to 1 in case the NVM CRC check detects an error. 0h = CRC check for NVM Passed 1h = CRC check for NVM Failed
3	FET_SHORT_BIST_ERR_CH2	RC	0h	This bit indicates whether or not the BIST for the FET shorted CH2 passed 0h = BIST for FET short CH2 Passed 1h = BIST for FET short CH2 Failed
2	FET_SHORT_BIST_ERR_CH1	RC	0h	This bit indicates whether or not the BIST for the FET shorted CH1 passed 0h = BIST for FET short CH1 Passed 1h = BIST for FET short CH1 Failed

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Table 8-8. BIST_RESULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADC_BIST_ERR	RC	0h	This bit indicates whether or not the BIST for the ADC passed 0h = BIST for ADC Passed 1h = BIST for ADC Failed
0	BG_BIST_ERR	RC	0h	This bit indicates whether or not the BIST for the Bandgap passed 0h = BIST for BG Passed 1h = BIST for BG Failed

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8.1.7 SW_STATE Register (Offset = 6h) [Reset = C0CCh]

SW_STATE is shown in Table 8-9.

Return to the Summary Table.

Table 8-9. SW_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	3h	Reserved
13	SWEN_S_CH2	R	0h	This Bit indicates the status of the internal SWEN signal of the CH2 bypass FET 0h = CH2 Bypass FET SWEN is Low 1h = CH2 SBypass FET SWEN is High
12	SWEN_S_CH1	R	0h	This Bit indicates the status of the internal SWEN signal of the CH1 bypass FET 0h = CH1 Bypass FET SWEN is Low 1h = CH1 Bypass FET SWEN is High
11	SW_STATE_S_CH2	R	0h	This Bit indicates the status of the VGS of the CH2 bypass FET 0h = CH2 Bypass FET VGS Comp is Low 1h = CH2 Bypass FET VGS Comp is High
10	SW_STATE_S_CH1	R	0h	This Bit indicates the status of the VGS of the CH1 bypass FET 0h = CH1 Bypass FET VGS Comp is Low 1h = CH1 Bypass FET VGS Comp is High
9	SW_STATE_M_CH2	R	0h	This Bit indicates the status of the VGS of the CH2 Main FET 0h = CH2 Main FET VGS Comp is Low 1h = CH2 Main FET VGS Comp is High
8	SW_STATE_M_CH1	R	0h	This Bit indicates the status of the VGS of the CH1 Main FET 0h = CH1 Main FET VGS Comp is Low 1h = CH1 Main FET VGS Comp is High
7-6	RESERVED	R	3h	Reserved
5	SWEN_M_CH2	R	0h	This Bit indicates the status of the internal SWEN of the CH2 Main FET 0h = CH2 Main FET SWEN is Low 1h = CH2 Main FET SWEN is High
4	SWEN_M_CH1	R	0h	This Bit indicates the status of the internal SWEN of the CH1 Main FET 0h = CH1 Main FET SWEN is Low 1h = CH1 Main FET SWEN is High
3-2	RESERVED	R	3h	Reserved
1	CH2_ON	R/W	0h	Set this bit to 1 to turn on the FET and CH2 output ON 0h = CH2 Output set to OFF 1h = CH2 Output set to ON
0	CH1_ON	R/W	0h	Set this bit to 1 to turn on the FET and CH1 output ON 0h = CH1 Output set to OFF 1h = CH1 Output set to ON

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8.1.8 DEVICE_TEST Register (Offset = 7h) [Reset = 0010h]

DEVICE_TEST is shown in Table 8-10.

Return to the Summary Table.

Table 8-10. DEVICE_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIST_CTRL_CHECK	R/W	0h	Set this bit to 1 to turn off the FET during the BIST. 0h = Fet remains ON during the BIST 1h = Fet remains OFF during the BIST
14	VDS_BIST_DIRECTION	R/W	0h	Depending upon direction selected, particular comparator is selected for BIST. 0h = Reverse direction 1h = Forward direction
13	BIST_CH_SEL	R/W	0h	Set this bit to select for which channel we want to enable the BIST for (ISNS, VDS, UV, OV, TSNS). BIST_CH_SEL will be latched until all the BISTs for that channel are done. 0h = Channel 1 selected 1h = Channel 2 selected
12	I2T_BIST_RUN_CH2	R/W	0h	Run the BIST diagnostics for the I2T protection channel 2 good signal and assert the fault with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for I2T Running
11	SCP_BIST_RUN_CH2	R/W	0h	Run the BIST diagnostics for the SCP protection channel 2 good signal and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for SCP Running
10	OV_BIST_RUN	R/W	0h	Run the BIST diagnostics for the OV protection based on BIST_CH_SEL bits for good signal and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for OV Running for selected channel
9	UV_BIST_RUN	R/W	0h	Run the BIST diagnostics for the UV protection based on BIST_CH_SEL bits for good signal and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for UV Running for selected channel
8	VDS_BIST_RUN	R/W	0h	Run the BIST diagnostics for the VDS protection (external FET (main)) based on BIST_CH_SEL bits for good signal and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for VDS Running for selected channel
7	TSNS_BIST_RUN	R/W	0h	Run the BIST diagnostics for the Temp protection (external FET (main)) based on BIST_CH_SEL bits for good signal and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for TSNS Running for selected channel
6	I2T_BIST_RUN_CH1	R/W	0h	Run the BIST diagnostics for the I2T protection channel 1 good signal and assert the fault with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for I2T Running
5	SCP_BIST_RUN_CH1	R/W	0h	Run the BIST diagnostics for the SCP protection channel 1 good signal and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for SCP Running

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Table 8-10. DEVICE_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ISNS_BIST_RUN	R/W	1h	Run the BIST diagnostics for the ISNS based on BIST_CH_SEL bits for good signal and update the BIST_RESULT register with the result. Not available when in I2T loop or under overcurrent or thermal fault conditions. Reset bit back to 0 after BIST has been run successfully. 0h = BIST not Running 1h = BIST for ISNS Running for selected channel
3	FET_SHORT_BIST_RUN_CH2	R/W	0h	Run the BIST diagnostics for the CH2 FET short failure and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST for CH2 FET short failure not Running 1h = BIST for CH2 FET short failure Running
2	FET_SHORT_BIST_RUN_CH1	R/W	0h	Run the BIST diagnostics for the CH1 FET short failure and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST for CH1 FET short failure not Running 1h = BIST for CH1 FET short failure Running
1	ADC_BIST_RUN	R/W	0h	Run the BIST diaagnostics for the ADC good signal and update the BIST_RESULT register with the result. Not available while in I2T loop or under overcurrent or thermal fault conditions. Reset bit back to 0 after BIST has been run. 0h = BIST not Running 1h = BIST for ADC Running
0	BG_BIST_RUN	R/W	0h	Run the BIST diagnostics for the Band Gap good signal and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST not Running 1h = BIST for BG Running

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8.1.9 DEV_CONFIG Register (Offset = 8h) [Reset = 7800h]

DEV_CONFIG is shown in Table 8-11.

Return to the Summary Table.

Table 8-11. DEV_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CRC_EN	R/W	0h	Set this bit to 1 to enable CRC check of SPI command frame. 0h = No CRC check of SPI command frame 1h = CRC check of SPI command frame enabled
14-11	RESERVED	R	Fh	Reserved
10-9	CH2_LH_IN	R/W	0h	Decides what to do with the output for LIMPHOME mode for channel 2. 0h = DI control output when in Limphome mode 1h = keep output as it enter Limphome mode 2h = output will be off during Limphome mode 3h = output will be on during Limphome mode
8-7	CH1_LH_IN	R/W	0h	Decides what to do with the output for LIMPHOME mode for channel 1. 0h = DI control output when in Limphome mode 1h = keep output as it enter Limphome mode 2h = output will be off during Limphome mode 3h = output will be on during Limphome mode
6	LIMPHOME_CONFIG	R/W	0h	Set this bit to enable the reloading of NVM values into the register upon entering into LIMPHOME mode configuration. NVM is read by default when device transitions from SLEEP to LIMPHOME mode irrespective of this bit setting. 0h = Register values in LIMPHOME mode is retained 1h = Register values are reloaded from NVM during Limphome mode transition
5	AUTO_LPM_ENTRY	R/W	0h	Set this bit to 1 to enable automatic entry to low power mode when the current is below AUTO LPM threshold. 0h = No automatic entry to low power mode when the load current is below AUTO LPM threshold 1h = The device automatically enters low power mode when the load current below AUTO LPM threshold
4	AUTO_LPM_FILTER	R/W	0h	This bit sets the Auto LPM filter time when the Auto LPM condition is achieved 0h = Auto LPM Filter time is 1ms 1h = Auto LPM Filter time is 100us
3	WD_EN	R/W	0h	The bit is set to enable the watchdog function. The watchdog is triggered if there is not a valid SPI command in the watchdog timeout window. 0h = Watchdog is disabled 1h = Watchdog function is enabled
2-1	WD_TO	R/W	0h	Sets the timeout period for the SPI watchdog monitor. The watchdog timeout is triggered if there is not a valid SPI command in the watchdog timeout window. 0h = Watchdog timeout 520us 1h = Watchdog timeout is 400ms 2h = Watchdog timeout is 800ms 3h = Watchdog timeout is 1200ms
0	FLT_LTCH_DIS	R/W	0h	Set this bit to 1 to not latch the fault bits in the register and cleared on read. 0h = Fault bits in FLT_STAT_CHx register latched and cleared only on read 1h = Fault bits in FLT_STAT_CHx register not latched, cleared when the fault disappears

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8.1.10 ADC_CONFIG Register (Offset = 9h) [Reset = FD3Ah]

ADC_CONFIG is shown in Table 8-12.

Return to the Summary Table.

Table 8-12. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	3Fh	Reserved
9	ADC_I2T_CONFIG_MODE	R/W	0h	Set this bit to 1 to enable Both VOUT and ISNS conversion per channel else only ISNS will be converted in the I2T mode. 0h = Only ISNS will be sampled per channel in I2T Mode 1h = ISNS and VOUT both sampled per channel in I2T Mode for the power calculation requirement
8	ADC_TCONT_SNS_DIS	R/W	1h	Set this bit to 1 to disable Controller TEMP sense functionality, exclude TCONT_SNS conversion in the ADC conversion sequence. 0h = TSNS ADC functionality enabled, include TSNS ADC conversion in the sequence 1h = TSNS ADC functionality is disabled
7-6	ADC_CONFIG_DELAY	R/W	0h	Set the sampling rate for current sense as well current sense conversion. Use these settings to reduce the rate of current sense measurement as well as the current consumption. The total time for all conversions (whether enabled or not) is increase to to 2x and 4x for 0x2 and 0x3 setting respectively. 0h = 0us 1h = 100us 2h = 200us 3h = 400us
5	ADC_VDS_DIS	R/W	1h	Set this bit to 1 to disable VDS sense functionality, exclude VDS conversion in the ADC conversion sequence. 0h = VDS ADC functionality is enabled, include VDS ADC conversion in the sequence 1h = VDS SNS ADC functionality is disabled
4	ADC_VSNS_DIS	R/W	1h	Set this bit to 1 to disable VOUT sense functionality, exclude VOUT conversion in the ADC conversion sequence. 0h = VOUTSNS ADC functionality enabled, include VOUT_SNS ADC conversion in the sequence 1h = VOUTSNS ADC functionality is disabled
3	ADC_TSNS_DIS	R/W	1h	Set this bit to 1 to disable external FET temperature sense functionality, exclude TSNS conversion in the ADC conversion sequence. 0h = TSNS ADC functionality enabled, include TSNS ADC conversion in the sequence 1h = TSNS ADC functionality is disabled
2	ADC_ISNS_DIS	R/W	0h	Set this bit to 1 to disable ISNS functionality, exclude ISNS conversion in the ADC conversion sequence. Enabled by default. 0h = ISNS ADC functionality enabled, include ISNS ADC conversion in the sequence 1h = ISNS ADC functionality is disabled
1	ADC_VBB_DIS	R/W	1h	Set this bit to 1 to disable VBB_SNS functionality, exclude supply voltage VBB_SNS conversion in the ADC conversion sequence. 0h = VBB_SNS ADC functionality is enabled, Include supply voltage VBB_SNS ADC conversion in the sequence 1h = VBB_SNS ADC functionality is disabled
0	ADC_DIS	R/W	0h	Setting this bit to 1, disables all ADC function (enabled by default) 0h = ADC function enabled 1h = All ADC function disabled

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8.1.11 ADC_RESULT_VBB Register (Offset = Ah) [Reset = F800h]

ADC_RESULT_VBB is shown in Table 8-13.

Return to the Summary Table.

Table 8-13. ADC_RESULT_VBB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VBB_RDY	RC	0h	Making sure the ADC conversion is new from the last time this was read 0h = VBB ADC Value not updated 1h = New VBB ADC Value Ready
9-0	ADC_RESULT_VBB	R	0h	ADC result (10-bits) from the conversion of the VBB voltage

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8.1.12 ADC_RESULT_BIST Register (Offset = Bh) [Reset = E000h]

ADC_RESULT_BIST is shown in Table 8-14.

Return to the Summary Table.

Table 8-14. ADC_RESULT_BIST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	ISNS_BIST_CH_INFO	RC	0h	This bit will indicate the channel information for which Isns bist is initiated. 0h = ISNS BIST Enabled for CH1 1h = ISNS BIST Enabled for CH2
11	ADC_ISNS_BIST	RC	0h	This bit will indicate whether ISNS or ADC Bist result is updated. 0h = ISNS BIST Value updated 1h = ADC Bist Value updated
10	BIST_RESULT_RDY	RC	0h	Making sure the ADC conversion is new from the last time this was read 0h = BIST ADC Value not updated 1h = New BIST ADC Value Ready
9-0	ADC_RESULT_BIST	RC	0h	ADC result (10-bits) from the conversion of the BIST voltage

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8.1.13 FLT_STAT_CH1 Register (Offset = Ch) [Reset = 0010h]

FLT_STAT_CH1 is shown in Table 8-15.

Return to the Summary Table.

Table 8-15. FLT_STAT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VDS_FLT_CH1	RC	0h	The bit is set if VDS protection has triggered at any time in CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and fault condition does not exist anymore 0h = No VDS protection fault in CH1 1h = VDS protection fault in CH1
14	THERMAL_SD_BYP_CH1	RC	0h	The bit is set if the thermal shutdown has occurred at any time in Bypass FET CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and channel temperature has fallen below the thermal shutdown reset threshold. 0h = No Bypass FET thermal shutdown fault in CH1 1h = Bypass FET Thermal shutdown has occurred in CH1
13	OCP_CH1	RC	0h	The bit is set if SCP has triggered at any time in CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and fault condition does not exist anymore 0h = No short-circuit protection fault (SCP) fault in CH1 1h = short-circuit protection fault (SCP) has occurred in CH1
12	I2T_MOD_CH1	R	0h	If the device is in the I2T loop and accumulating this bit will be 1, when the device is out of the loop it will be 0, read only 0h = I2T is off/not working 1h = I2T is currently running
11	LATCH_STAT_CH1	R	0h	The bit is high if the channel has been latched off after a fault that shut down the channel. Clears when the channel is toggled back on 0h = CH1 is not latched off 1h = CH1 is currently latched off
10	FLT_CH1	R	0h	The bit is set if any fault occurs in CH1. It's live fault indication. It also includes all the faults which affect gate control for CH1. This bit remains asserted for auto retry duration as well. 0h = No fault in CH1 1h = One or more fault has occurred in CH1
9	LPM_HS_CH1	RC	0h	LPM HS has happpened during LPM. The fault is latched and cleared when the FLT_STAT_CH1 register is read and LPM HS has gone. 0h = CH1 is not faced with LPM HS 1h = CH1 is is faced with LPM HS
8	VOUT_ERR_CH1	RC	0h	The bit is set if the output of the channel is not high when the channel is enabled after the INRUSH_DURATION_CHx period and Gate high is not achieved. Cleared when FLT_STAT_CH1 register is read and fault condition does not exist anymore. 0h = Output voltage is correct when enabled CH1 1h = Output voltage is incorrect when channel is supposed to be enabled or disabled in CH1
7	I2T_FLT_CH1	RC	0h	The bit is set if there is a fault from I2T setting (overcurrent). Only can go high if I2T_EN is high and an associated fault occurs on that channel. Cleared when FLT_STAT_CH1 register is read and fault condition does not exist anymore 0h = no I2T fault or I2T is not enabled 1h = I2T fault has occurred on CH1
6	LPM_WAKE_CH1	RC	0h	This bit is set if this loadwakeup happens on CH1. Cleared when FLT_STAT_CH1 register is read and fault condition does not exist anymore 0h = No Loadwakeup on CH1 1h = Loadwakeup triggered on CH1

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Table 8-15. FLT_STAT_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	TSD_CH1	RC	0h	The bit is set if the external FET thermal shutdown has occurred at any time in CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and channel temperature has fallen below the thermal shutdown reset threshold. 0h = No TSD fault in CH1 1h = TSD has occurred in CH1
4	RESERVED	R	1h	Reserved
3	SHRT_VBB_CH1	RC	0h	The bit is set if output short to VBB has occurred at any time in CH1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and fault condition does not exist anymore. 0h = No Short to VBB fault in CH1 or short to VBB in OFF state not enabled 1h = Output Short to VBB fault present
2	OL_OFF_CH1	RC	0h	The bit is set if the open load off state threshold been triggered. Only valid if OL_OFF_EN_CH1 is active. 0h = No off state open load fault in CH1 or OL detection in OFF state not enabled 1h = Off State Open Load fault present
1	CPUMP_UVLO_CH1	RC	0h	This bit is set if the chargepump UVLO is triggered. The fault is latched and cleared when the FLT_STAT_CH1 register is read and CP UVLO fault has gone. 0h = No CPUVLO on CH1 1h = CPUVLO fault ocurred on CH1
0	THERMAL_WRN_CH1	RC	0h	The bit is set if Controller temperature is above the overtemperature warning threshold The bit is cleared when over-temperature earning condition does not exist anymore. 0h = Controller temperature below over-temperature warning threshold 1h = Controller temperature above over-temperature warning threshold

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8.1.14 PWM_CH1 Register (Offset = Dh) [Reset = F000h]

PWM_CH1 is shown in Table 8-16.

Return to the Summary Table.

Table 8-16. PWM_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-9	PWM_FREQ_CH1	R/W	0h	Set the PWM frequency 0h = 0.8Hz 1h = 3.4Hz 2h = 13.8Hz 3h = 111Hz 4h = 221Hz 5h = 425Hz 6h = 885Hz 7h = 1770Hz
8-1	PWM_DTY_CH1	R/W	0h	8 bit to set duty cycle for PWM operation of CH1. Each bit ~0.39% duty cycle, linearly up to 100% dutycycle. 0x0 = GATEx always ON 0x1 = Reserved 0x2 = 2 x 0.39% 0x3 = 3 x 0.39% 0x4 = 5 x 0.39% 0x5 = 6 x 0.39% and so on
0	PWM_EN_CH1	R/W	0h	Enable PWM for CH1 0h = Output follows SW_STATE behavior (ON/OFF) 1h = Output is PWM according to duty cycle and frequency set if SW_STATE CH1 is ON

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8.1.15 ILIM_CONFIG_CH1 Register (Offset = Eh) [Reset = 001Fh]

ILIM_CONFIG_CH1 is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. ILIM_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LATCH_CH1	R/W	0h	If fault occurs that channel shuts down, this bit sets if the channel auto retries or latches off 0h = GATEx turns on after set retry duration 1h = latch off until SW_STATE register is written to again or LHI or DIx/OUT_DISx is toggled.
14	DI_OUT_DIS_FN_CH1	R/W	0h	Set this bit to 1 to use the DI1/OUT_DIS1 pin as Output_Disable 0h = The Limphome mode is determined by a DI1/OUT_DIS1 pin (DI pin function) 1h = Outputs are disabled when DI1/OUT_DIS1 pin is set HI (OUT_DIS function)
13-12	CAP_CHRG_CH1	R/W	0h	Puts the part into the capacitive load driving mode. 0h = Using SCP based auto-retry method 1h = Using main path gate slew control 2h = Using bypass path gate slew rate control (only applicable to TPS12Sx3F-Q1) 3h = Using main path PWM mode
11	I2T_EN_CH1	R/W	0h	Enables the I2T functionality for channel 1. . 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH1	R/W	0h	Sets the delay period during GATEx turn ON. 0h = 0 1h = 2 2h = 4 3h = 6 4h = 10 5h = 20 6h = 50 7h = 100 ms
7-6	AUTO_RETRY_DURATION_CH1	R/W	0h	Setting the autoretry time for the channel when it is set as autoretry part and the fault goes away. Auto retry duration is applicable after SCP, VDS overvoltage or external FET temperature shutdown (TSD) faults. 00 - 1ms 01 - 10ms 10 - 100us 11 - 100ms
5	FOLDBACK_LOCK_DIS_CH1	R/W	0h	Set this bit for infinite auto retry after SCP, VDS overvoltage or external FET temperature shutdown (TSD) faults. 0h = Finite (13) autoretry then latch the channel to the foldback lock state. The Auto retry time becomes 10x after every 7th cycle. The retry counter resets only when CHx_ON bit, LHI or DIx/OUT_DISx pins are toggled. 1h = Infinite Auto retry. The Auto retry time remains same for infinite cycles.
4-0	RESERVED	R	1Fh	Reserved

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8.1.16 DIAG_CONFIG_CH1 Register (Offset = Fh) [Reset = 0200h]

DIAG_CONFIG_CH1 is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. DIAG_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable the VOUT SNS ADC functionality for this channel 0h = VOUT SNS ADC functionality enabled 1h = VOUT SNS ADC functionality is disabled
14	VDSSNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable the ADC VDSSNS functionality for this channel 0h = VDSSNS ADC functionality enabled 1h = VDSSNS ADC functionality is disabled
13	ISNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable ISNS ADC functionality for this channel 0h = ISNS ADC functionality enabled 1h = ISNS ADC functionality is disabled
12-10	ISNS_GAIN_CH1	R/W	0h	Sets the Gain of the ISNS for CH1 0h = 15 1h = 30 2h = 50 3h = 65 4h = 85 5h = 100 6h = 120 7h = 135
9	RESERVED	R	1h	Reserved
8-7	FET_SHORT_BLANK_CH1	R/W	0h	Sets the blanking time FET Short fault before the fault is registered. 0h = 50us 1h = 250us 2h = 500us 3h = 2ms
6-5	OL_PU_STR_CH1	R/W	0h	Sets the pullup current value (at the OUTx pins) by the off-state open load detection circuit. 0h = 33uA 1h = 54uA 2h = 130uA 3h = 254uA
4	EN_PULL_DOWN_CH1	R/W	0h	This bit enables the Pull Down current source for CH1. Bit will automatically be cleared once SVBB algorithm is completed or exited abnormally. 0h = Pull Down current source disabled for CH1 1h = Pull Down current source enabled for CH1
3	EN_PULL_UP_CH1	R/W	0h	This bit enables the Pull Up current source for CH1. Bit will automatically be cleared once OL algorithm is completed or exited abnormally. 0h = Pull Up current source disabled for CH1 1h = Pull Up current source enabled for CH1
2	SVBB_DIAG_EN_CH1	R/W	0h	This bit will enable the algorithm for short to battery in off state for CH1. Forcing this bit to 0 during diagnostics will lead to abnormal exit. Bit will automatically be cleared once algorithm is complete.The status is updated in FLT_STAT_CH1 register 0h = No SVBB running for CH1 1h = SVBB running in OFF state for CH1
1	OL_DIAG_EN_CH1	R/W	0h	This bit will enable the algorithm for open load in off state for CH1. Forcing this bit to 0 during diagnostics will lead to abnormal exit. Bit will automatically be cleared once algorithm is complete.The status is updated in FLT_STAT_CH1 register 0h = No OL running for CH1 1h = OL running in OFF state for CH1

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Table 8-18. DIAG_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable the ADC TSNS functionality for this channel 0h = TSNS ADC functionality enabled 1h = TSNS ADC functionality is disabled

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8.1.17 ADC_RESULT_CH1_I Register (Offset = 10h) [Reset = E800h]

ADC_RESULT_CH1_I is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. ADC_RESULT_CH1_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	3h	Reserved
13	ISNS_POLARITY_CH1	R	1h	The bit is set to 1 if current via sense resistor (CSx+ to CSx-) is in forward direction 0h = ISNS read is done while the current is in reverse direction 1h = ISNS read is done while the current is in forward direction
12	ISNS_CH1_ONOFF_STAT	R	0h	The bit is set to 0 if the ADC conversion of ISNS is done while the channel is OFF 0h = ISNS conversion done while the CH1 FET is OFF 1h = ISNS conversion done while the CH1 FET is ON
11	RESERVED	R	1h	Reserved
10	ISNS_RDY_CH1	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH1_I	R	0h	ADC result (10-bits) from the conversion of the current in CH1

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8.1.18 ADC_RESULT_CH1_T Register (Offset = 11h) [Reset = F800h]

ADC_RESULT_CH1_T is shown in Table 8-20.

Return to the Summary Table.

Table 8-20. ADC_RESULT_CH1_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TSNS_RDY_CH1	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH1_T	R	0h	ADC result (10-bits) from the conversion of the temperature in CH1

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8.1.19 ADC_RESULT_CH1_V Register (Offset = 12h) [Reset = F800h]

ADC_RESULT_CH1_V is shown in Table 8-21.

Return to the Summary Table.

Table 8-21. ADC_RESULT_CH1_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VSNS_RDY_CH1	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH1_V	R	0h	ADC result (10-bits) from the conversion of the output voltage in CH1

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8.1.20 ADC_RESULT_CH1_VDS Register (Offset = 13h) [Reset = F800h]

ADC_RESULT_CH1_VDS is shown in Table 8-22.

Return to the Summary Table.

Table 8-22. ADC_RESULT_CH1_VDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VDSSNS_RDY_CH1	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH1_VDS	R	0h	ADC result (10-bits) from the conversion of the VDS in CH2

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8.1.21 I2T_CONFIG_CH1 Register (Offset = 14h) [Reset = 07E0h]

I2T_CONFIG_CH1 is shown in Table 8-23.

Return to the Summary Table.

Table 8-23. I2T_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH1	R/W	0h	2bits to Set cool down threshold for I2T functionality for Channel1 (threshold to retry after I2T shutdown). 0h = Latch mode (or no retry) 1h = Acuumulator decrements to 2/3 times of I2T TRIP threshold 2h = Acuumulator decrements to 1/3 times of I2T TRIP threshold 3h = Acuumulator decrements to 0
13	DCR_CH1	R/W	0h	Sets the mode of operation 0h = I2T Mode DCR0 1h = I2T Mode DCR1
12-11	ACC_DCR0_CH1	R/W	0h	Decrement of IACC with IADC <NOM_CUR when DCR_CHx = 0.
10-5	RESERVED	R	3Fh	Reserved
4-0	NOM_CUR_CH1	R/W	0h	5 bits to set the nomial current value of Channel 1. 00h = 3mV 01h = 4.5mV 02h = 6mV 03h = 7.5mV 04h = 9mV 05h = 10.5mV 06h = 12mV 07h = 13.5mV 08h = 15mV 09h = 16.5mV 0Ah = 18mV 0Bh = 19.5mV 0Ch = 21mV 0Dh = 22.5mV 0Eh = 24mV 0Fh = 25.5mV 10h = 27mV 11h = 28.5mV 12h = 30mV 13h = 31.5mV 14h = 33mV 15h = 34.5mV 16h = 36mV 17h = 37.5mV 18h = 39mV 19h = 41.5mV 1Ah = 44mV 1Bh = 48mV 1Ch = 62mV 1Dh = 66mV 1Eh = 70mV 1Fh = 75mV

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8.1.22 FLT_STAT_CH2 Register (Offset = 15h) [Reset = 0010h]

FLT_STAT_CH2 is shown in Table 8-24.

Return to the Summary Table.

Table 8-24. FLT_STAT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VDS_FLT_CH2	RC	0h	The bit is set if VDS protection has triggered at any time in CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and fault condition does not exist anymore 0h = No VDS protection fault in CH2 1h = VDS protection fault (SCP / CB due to overcurrent fault has occurred in CH2
14	THERMAL_SD_BYP_CH2	RC	0h	The bit is set if the thermal shutdown has occurred at any time in Bypass FET CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and channel temperature has fallen below the thermal shutdown reset threshold. 0h = No Bypass FET thermal shutdown fault in CH2 1h = Bypass FET Thermal shutdown has occurred in CH2
13	OCP_CH2	RC	0h	The bit is set if SCP protection has triggered at any time in CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and fault condition does not exist anymore 0h = No short-circuit protection fault (SCP) fault in CH2 1h = Short-circuit protection fault (SCP) has occurred in CH2
12	I2T_MOD_CH2	R	0h	If the device is in the I2T loop and accumulating this bit will be 1, when the device is out of the loop it will be 0, read only 0h = I2T is off/not working 1h = I2T is currently running
11	LATCH_STAT_CH2	R	0h	The bit is high if the channel has been latched off after a fault that shut down the channel. Clears when the channel is toggled back on 0h = CH2 is not latched off 1h = CH2 is currently latched off
10	FLT_CH2	R	0h	The bit is set if any fault occurs in CH2. It's live fault indication. It also includes all the faults which affect gate control for CH2. This bit remains asserted for auto retry duration as well. 0h = No fault in CH2 1h = One or more fault has occurred in CH2
9	LPM_HS_CH2	RC	0h	LPM HS has happpened during LPM. The fault is latched and cleared when the FLT_STAT_CH2 register is read and LPM HS has gone. 0h = CH2 is not faced with LPM HS 1h = CH2 is is faced with LPM HS
8	VOUT_ERR_CH2	RC	0h	The bit is set if the output of the channel is not high when the channel is enabled after the INRUSH_DURATION period and Gate high is not achieved. Cleared when FLT_STAT_CH2 register is read and fault condition does not exist anymore. 0h = Output voltage is correct when enabled CH2 1h = Output voltage is incorrect when channel is supposed to be enabled or disabled in CH2
7	I2T_FLT_CH2	RC	0h	The bit is set if there is a fault from I2T setting (overcurrent). Only can go high if I2T_EN is high and an associated fault occurs on that channel. Cleared when FLT_STAT_CH2 register is read and fault condition does not exist anymore 0h = no I2T fault or I2T is not enabled 1h = I2T fault has occurred on CH2
6	LPM_WAKE_CH2	RC	0h	This bit is set if this loadwakeup happens on CH2. Cleared when FLT_STAT_CH2 register is read and fault condition does not exist anymore 0h = No Loadwakeup on CH2 1h = Loadwakeup triggered on CH2

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Table 8-24. FLT_STAT_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	THERMAL_SD_CH2	RC	0h	The bit is set if the external FET thermal shutdown has occurred at any time in CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and channel temperature has fallen below the thermal shutdown reset threshold. 0h = No TSD fault in CH2 1h = TSD has occurred in CH2
4	RESERVED	R	1h	Reserved
3	SHRT_VBB_CH2	RC	0h	The bit is set if short to VBB has occurred at any time in CH2. The fault is latched and cleared when the FLT_STAT_CH2 register is read and fault condition does not exist anymore. 0h = No Short to VBB fault in CH2 or short to VBB in OFF state not enabled 1h = Short to VBB Fault present
2	OL_OFF_CH2	RC	0h	The bit is set if the open load off state threshold been triggered. Only valid if OL_OFF_EN_CH2 is active. 0h = No off state open load fault in CH2 or OL detection in OFF state not enabled 1h = Off State Open Load Fault present
1	CPUMP_UVLO_CH2	RC	0h	This bit is set if the CPUVLO happens. The fault is latched and cleared when the FLT_STAT_CH2 register is read and CP UVLO fault has gone. 0h = No CPUVLO on CH2 1h = CPUVLO fault ocurred on CH2
0	THERMAL_WRN_CH2	RC	0h	The bit is set if Controller temperature is above the overtemperature warning threshold The bit is cleared when over-temperature earning condition does not exist anymore. 0h = Controller temperature below over-temperature warning threshold 1h = Controller temperature above over-temperature warning threshold

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8.1.23 PWM_CH2 Register (Offset = 16h) [Reset = F000h]

PWM_CH2 is shown in Table 8-25.

Return to the Summary Table.

Table 8-25. PWM_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-9	PWM_FREQ_CH2	R/W	0h	Set the PWM frequency for CH2 0h = 0.8Hz 1h = 3.4Hz 2h = 13.8Hz 3h = 111Hz 4h = 221Hz 5h = 425Hz 6h = 885Hz 7h = 1770Hz
8-1	PWM_DTY_CH2	R/W	0h	8 bit to set duty cycle for PWM operation of CH2. Each bit ~0.39% duty cycle, linearly up to 100% dutycycle. 0x0 = GATEx always ON 0x1 = Reserved 0x2 = 2 x 0.39% 0x3 = 3 x 0.39% 0x4 = 5 x 0.39% 0x5 = 6 x 0.39% and so on
0	PWM_EN_CH2	R/W	0h	Enable PWM for CH2 0h = Output follows SW_STATE behavior (ON/OFF) 1h = Output is PWM according to duty cycle and frequency set if SW_STATE CH2 is ON

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8.1.24 ILIM_CONFIG_CH2 Register (Offset = 17h) [Reset = 001Fh]

ILIM_CONFIG_CH2 is shown in Table 8-26.

Return to the Summary Table.

Table 8-26. ILIM_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LATCH_CH2	R/W	0h	If fault occurs that channel shuts down, this bit sets if the channel auto retries or latches off 0h = GATEx turns on after set retry duration 1h = latch off until SW_STATE register is written to again or LHI or DIx/OUT_DISx is toggled.
14	DI_OUT_DIS_FN_CH2	R/W	0h	Set this bit to 1 to use the DI2/OUT_DIS2 pin as Output_Disable 0h = The Limphome mode is determined by a DI2/OUT_DIS2 pin (DI pin function) 1h = Outputs are disabled when DI2/OUT_DIS2 pin is set HI (OUT_DIS function)
13-12	CAP_CHRG_CH2	R/W	0h	Puts the part into the capacitive load driving mode. 0h = Using SCP based auto-retry method 1h = Using main path gate slew control 2h = Using bypass path gate slew rate control (only applicable to TPS12Sx3F-Q1) 3h = Using main path PWM mode
11	I2T_EN_CH2	R/W	0h	Enables the I2T functionality for channel 2. 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH2	R/W	0h	Sets the delay period during with inrush current limit level applies. 0h = 0 1h = 2 2h = 4 3h = 6 4h = 10 5h = 20 6h = 50 7h = 100 ms
7-6	AUTO_RETRY_DURATION_CH2	R/W	0h	Setting the autoretry time for the channel when it is set as autoretry part and the fault goes away. Auto retry duration is applicable after SCP, VDS overvoltage or external FET temperature shutdown (TSD) faults. 00 - 1ms 01 - 10ms 10 - 100us 11 - 100ms
5	FOLDBACK_LOCK_DIS_CH2	R/W	0h	Set this bit for infinite auto retry after SCP, VDS overvoltage or external FET temperature shutdown (TSD) faults. 0h = Finite (13) autoretry then latch the channel to the foldback lock state. The Auto retry time becomes 10x after every 7th cycle. The retry counter resets only when CHx_ON bit, LHI or DIx/OUT_DISx pins are toggled. 1h = Infinite Auto retry. The Auto retry time remains same for infinite cycles.
4-0	RESERVED	R	1Fh	Reserved

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8.1.25 DIAG_CONFIG_CH2 Register (Offset = 18h) [Reset = 0200h]

DIAG_CONFIG_CH2 is shown in Table 8-27.

Return to the Summary Table.

Table 8-27. DIAG_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH2	R/W	0h	Set this bit to 1 to disable the VOUT SNS ADC functionality for this channel 0h = VOUT SNS ADC functionality enabled 1h = VOUT SNS ADC functionality is disabled
14	VDSSNS_DIS_CH2	R/W	0h	Set this bit to 1 to disable the ADC VDSSNS functionality for this channel 0h = VDSSNS ADC functionality enabled 1h = VDSSNS ADC functionality is disabled
13	ISNS_DIS_CH2	R/W	0h	Set this bit to 1 to disable ISNS ADC functionality for this channel 0h = ISNS ADC functionality enabled 1h = ISNS ADC functionality is disabled
12-10	ISNS_GAIN_CH2	R/W	0h	Sets the Gain of the ISNS for CH2 0h = 15 1h = 30 2h = 50 3h = 65 4h = 85 5h = 100 6h = 120 7h = 135
9	RESERVED	R	1h	Reserved
8-7	FET_SHORT_BLANK_CH2	R/W	0h	Sets the blanking time for FET Short fault before the fault is registered. 0h = 50us 1h = 250us 2h = 500us 3h = 2ms
6-5	OL_PU_STR_CH2	R/W	0h	Sets the pullup current value (at the OUTx pins) by the off-state open load detection circuit. 0h = 33uA 1h = 54uA 2h = 130uA 3h = 254uA
4	EN_PULL_DOWN_CH2	R/W	0h	This bit enables the Pull Down current source for CH2. Bit will automatically be cleared once SVBB algorithm is completed or exited abnormally. 0h = Pull Down current source disabled for CH2 1h = Pull Down current source enabled for CH2
3	EN_PULL_UP_CH2	R/W	0h	This bit enables the Pull Up current source for CH2. Bit will automatically be cleared once OL algorithm is completed or exited abnormally. 0h = Pull Up current source disabled for CH2 1h = Pull Up current source enabled for CH2
2	SVBB_DIAG_EN_CH2	R/W	0h	This bit will enable the algorithm for short to battery in off state for CH2. Forcing this bit to 0 during diagnostics will lead to abnormal exit. Bit will automatically be cleared once algorithm is complete.The status is updated in FLT_STAT_CH2 register 0h = No SVBB running for CH2 1h = SVBB running in OFF state for CH2
1	OL_DIAG_EN_CH2	R/W	0h	This bit will enable the algorithm for open load in off state for CH2. Forcing this bit to 0 during diagnostics will lead to abnormal exit. Bit will automatically be cleared once algorithm is complete.The status is updated in FLT_STAT_CH2 register 0h = No OL running for CH2 1h = OL running in OFF state for CH2

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Table 8-27. DIAG_CONFIG_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	TSNS_DIS_CH2	R/W	0h	Set this bit to 1 to disable the ADC TSNS functionality for this channel 0h = TSNS ADC functionality enabled 1h = TSNS ADC functionality is disabled

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8.1.26 ADC_RESULT_CH2_I Register (Offset = 19h) [Reset = E800h]

ADC_RESULT_CH2_I is shown in Table 8-28.

Return to the Summary Table.

Table 8-28. ADC_RESULT_CH2_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	3h	Reserved
13	ISNS_POLARITY_CH2	R	1h	The bit is set to 1 if current via sense resistor (CSx+ to CSx-) is in forward direction 0h = ISNS read is done while the current is in reverse direction 1h = ISNS read is done while the current is in forward direction
12	ISNS_CH2_ONOFF_STAT	R	0h	The bit is set to 0 if the ADC conversion of ISNS is done while the channel is OFF 0h = ISNS conversion done while the CH2 FET is OFF 1h = ISNS conversion done while the CH2 FET is ON
11	RESERVED	R	1h	Reserved
10	ISNS_RDY_CH2	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH2_I	R	0h	ADC result (10-bits) from the conversion of the current in CH2

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8.1.27 ADC_RESULT_CH2_T Register (Offset = 1Ah) [Reset = F800h]

ADC_RESULT_CH2_T is shown in Table 8-29.

Return to the Summary Table.

Table 8-29. ADC_RESULT_CH2_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TSNS_RDY_CH2	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH2_T	R	0h	ADC result (10-bits) from the conversion of the temperature in CH2

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8.1.28 ADC_RESULT_CH2_V Register (Offset = 1Bh) [Reset = F800h]

ADC_RESULT_CH2_V is shown in Table 8-30.

Return to the Summary Table.

Table 8-30. ADC_RESULT_CH2_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VSNS_RDY_CH2	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH2_V	R	0h	ADC result (10-bits) from the conversion of the output voltage in CH2

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8.1.29 ADC_RESULT_CH2_VDS Register (Offset = 1Ch) [Reset = F800h]

ADC_RESULT_CH2_VDS is shown in Table 8-31.

Return to the Summary Table.

Table 8-31. ADC_RESULT_CH2_VDS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VDSSNS_RDY_CH2	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_CH2_VDS	R	0h	ADC result (10-bits) from the conversion of the VDS in CH2

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8.1.30 I2T_CONFIG_CH2 Register (Offset = 1Dh) [Reset = 07E0h]

I2T_CONFIG_CH2 is shown in Table 8-32.

Return to the Summary Table.

Table 8-32. I2T_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH2	R/W	0h	2bits to Set cool down threshold for I2T functionality for CH2 (threshold to retry after I2T shutdown). 0h = Latch mode (or no retry) 1h = Acuumulator decrements to 2/3 times of I2T TRIP threshold 2h = Acuumulator decrements to 1/3 times of I2T TRIP threshold 3h = Acuumulator decrements to 0
13	DCR_CH2	R/W	0h	Sets the mode of operation 0h = I2t Mode DCR0 1h = I2t Mode DCR1
12-11	ACC_DCR0_CH2	R/W	0h	Decrement of IACC with IADC <NOM_CUR when DCR_CHx = 0.
10-5	RESERVED	R	3Fh	Reserved
4-0	NOM_CUR_CH2	R/W	0h	5 bits to set the nomial current value of Channel 2. 00h = 3mV 01h = 4.5mV 02h = 6mV 03h = 7.5mV 04h = 9mV 05h = 10.5mV 06h = 12mV 07h = 13.5mV 08h = 15mV 09h = 16.5mV 0Ah = 18mV 0Bh = 19.5mV 0Ch = 212V 0Dh = 22.5mV 0Eh = 24mV 0Fh = 25.5mV 10h = 27mV 11h = 28.5mV 12h = 30mV 13h = 31.5mV 14h = 33mV 15h = 34.5mV 16h = 36mV 17h = 37.5mV 18h = 39mV 19h = 41.5mV 1Ah = 44mV 1Bh = 48mV 1Ch = 62mV 1Dh = 66mV 1Eh = 70mV 1Fh = 75mV

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8.1.31 I2T_TRIP_CH1 Register (Offset = 1Eh) [Reset = FF80h]

I2T_TRIP_CH1 is shown in Table 8-33.

Return to the Summary Table.

Table 8-33. I2T_TRIP_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	FFh	Reserved
7-0	I2T_TRIP_CH1	R/W	80h	8 bits to set the I2T_TRIP of CH1

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8.1.32 I2T_ACC_RD_CH1 Register (Offset = 1Fh) [Reset = 0000h]

I2T_ACC_RD_CH1 is shown in Table 8-34.

Return to the Summary Table.

Give the relative accum value with respect to the I2T Trip setting. 10 bit

Table 8-34. I2T_ACC_RD_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	I2T_ACC_RD_CH1	R	0h	16 MSBs of I2T Accumulator of CH1

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8.1.33 I2T_ACC_RD_CH2 Register (Offset = 20h) [Reset = 0000h]

I2T_ACC_RD_CH2 is shown in Table 8-35.

Return to the Summary Table.

Give the relative accum value with respect to the I2T Trip setting. 10 bit

Table 8-35. I2T_ACC_RD_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	I2T_ACC_RD_CH2	R	0h	16 MSBs of I2T Accumulator of CH2

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8.1.34 I2T_TRIP_CH2 Register (Offset = 33h) [Reset = FF80h]

I2T_TRIP_CH2 is shown in Table 8-36.

Return to the Summary Table.

Table 8-36. I2T_TRIP_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	FFh	Reserved
7-0	I2T_TRIP_CH2	R/W	80h	8 bits to set the I2T_TRIP of CH2

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8.1.35 ADC_RESULT_TCONT Register (Offset = 34h) [Reset = F800h]

ADC_RESULT_TCONT is shown in Table 8-37.

Return to the Summary Table.

Table 8-37. ADC_RESULT_TCONT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TCONT_SNS_RDY	RC	0h	Making sure the ADC conversion is new from the last time this was read
9-0	ADC_RESULT_TCONT	R	0h	ADC result (10-bits) from the conversion of the temperature in Controller

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8.1.36 SCP_CONFIG_CH1 Register (Offset = 35h) [Reset = 8890h]

SCP_CONFIG_CH1 is shown in Table 8-38.

Return to the Summary Table.

Table 8-38. SCP_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	FWD_SCP_SET_CH1	R/W	8h	Forward SCP Setting for CH1 00h = 10mV 01h = 12mV 02h = 14.35mV 03h = 17.2mV 04h = 20mV 05h = 24.17mV 06h = 28.7mV 07h = 35mV 08h = 43.32mV 09h = 51.68mV 0Ah = 63.3mV 0Bh = 75.81mV 0Ch = 93.37mV 0Dh = 110mV 0Eh = 133.3mV 0Fh = 158.2mV
11-8	REV_SCP_SET_CH1	R/W	8h	Reverse SCP Setting for CH1 00h = 10mV 01h = 12mV 02h = 14.35mV 03h = 17.2mV 04h = 20mV 05h = 24.17mV 06h = 28.7mV 07h = 35mV 08h = 43.32mV 09h = 51.68mV 0Ah = 63.3mV 0Bh = 75.81mV 0Ch = 93.37mV 0Dh = 110mV 0Eh = 133.3mV 0Fh = 158.2mV
7-5	FWD_SCP_MASK_CH1	R/W	4h	Forward SCP masking setting for CH1 0h = 0us 1h = 4us 2h = 9us 3h = 24us 4h = 44us 5h = 89us 6h = 134us 7h = 179us
4-2	REV_SCP_MASK_CH1	R/W	4h	Reverse SCP masking setting for CH1 0h = 0us 1h = 4us 2h = 9us 3h = 24us 4h = 44us 5h = 89us 6h = 134us 7h = 179us
1	FWD_SCP_DIS_CH1	R/W	0h	Disable Forward SCP Protection for CH1 0h = SCP functionality enabled for CH1 1h = SCP functionality is disabled for CH1

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Table 8-38. SCP_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	REV_SCP_DIS_CH1	R/W	0h	Disable Reverse SCP Protection for CH1 0h = SCP functionality enabled for CH1 1h = SCP functionality is disabled for CH1

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8.1.37 SCP_CONFIG_CH2 Register (Offset = 36h) [Reset = 8890h]

SCP_CONFIG_CH2 is shown in Table 8-39.

Return to the Summary Table.

Table 8-39. SCP_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	FWD_SCP_SET_CH2	R/W	8h	Forward SCP Setting for CH2 00h = 10mV 01h = 12mV 02h = 14.35mV 03h = 17.2mV 04h = 20mV 05h = 24.17mV 06h = 28.7mV 07h = 35mV 08h = 43.32mV 09h = 51.68mV 0Ah = 63.3mV 0Bh = 75.81mV 0Ch = 93.37mV 0Dh = 110mV 0Eh = 133.3mV 0Fh = 158.2mV
11-8	REV_SCP_SET_CH2	R/W	8h	Reverse SCP Setting for CH2 00h = 10mV 01h = 12mV 02h = 14.35mV 03h = 17.2mV 04h = 20mV 05h = 24.17mV 06h = 28.7mV 07h = 35mV 08h = 43.32mV 09h = 51.68mV 0Ah = 63.3mV 0Bh = 75.81mV 0Ch = 93.37mV 0Dh = 110mV 0Eh = 133.3mV 0Fh = 158.2mV
7-5	FWD_SCP_MASK_CH2	R/W	4h	Forward SCP masking setting for CH2 0h = 0us 1h = 4us 2h = 9us 3h = 24us 4h = 44us 5h = 89us 6h = 134us 7h = 179us
4-2	REV_SCP_MASK_CH2	R/W	4h	Reverse SCP masking setting for CH2 0h = 0us 1h = 4us 2h = 9us 3h = 24us 4h = 44us 5h = 89us 6h = 134us 7h = 179us
1	FWD_SCP_DIS_CH2	R/W	0h	Disable Forward SCP Protection for CH2 0h = SCP functionality enabled for CH2 1h = SCP functionality is disabled for CH2

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Table 8-39. SCP_CONFIG_CH2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	REV_SCP_DIS_CH2	R/W	0h	Disable Reverse SCP Protection for CH2 0h = SCP functionality enabled for CH2 1h = SCP functionality is disabled for CH2

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8.1.38 UV_CONFIG_CH1 Register (Offset = 37h) [Reset = 8AF0h]

UV_CONFIG_CH1 is shown in Table 8-40.

Return to the Summary Table.

Table 8-40. UV_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UVLO_SET_CH1	R/W	8h	UVLO falling protection Threshold Setting 00h = UVLO Disabled 01h = 4.5V 02h = 5V 03h = 6V 04h = 7V 05h = 8V 06h = 9V 07h = 16V 08h = 18V 09h = 20V 0Ah = 22V 0Bh = 24V 0Ch = 26V 0Dh = 28V 0Eh = 30V 0Fh = 32V
11-10	UVLO_HYST_CH1	R/W	2h	UVLO CH1 Hysteresis Setting 0h = 0.57V 1h = 1V 2h = 2V 3h = 4V
9-8	UVLO_MASK_CH1	R/W	2h	UVLO masking delay for CH1 0h = 0us 1h = 6us 2h = 45us 3h = 175us
7-4	RESERVED	R	Fh	Reserved
3-2	E10_CONFIG_CH1	R/W	0h	E10 Config masking time
1	UVLO_LPM_EN_CH1	R/W	0h	UVLO CH1 Enable during LPM 0h = UVLO functionality disabled in LPM 1h = UVLO functionality enabled in LPM
0	UVLO_EN_CH1	R/W	0h	UVLO CH1 Enable 0h = UVLO functionality disabled 1h = UVLO functionality enabled

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8.1.39 UV_CONFIG_CH2 Register (Offset = 38h) [Reset = 8AF0h]

UV_CONFIG_CH2 is shown in Table 8-41.

Return to the Summary Table.

Table 8-41. UV_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UVLO_SET_CH2	R/W	8h	UVLO falling protection Threshold Setting 00h = UVLO Disabled 01h = 4.5V 02h = 5V 03h = 6V 04h = 7V 05h = 8V 06h = 9V 07h = 16V 08h = 18V 09h = 20V 0Ah = 22V 0Bh = 24V 0Ch = 26V 0Dh = 28V 0Eh = 30V 0Fh = 32V
11-10	UVLO_HYST_CH2	R/W	2h	UVLO CH2 Hysteresis Setting 0h = 0.57V 1h = 1V 2h = 2V 3h = 4V
9-8	UVLO_MASK_CH2	R/W	2h	UVLO masking delay for CH2 0h = 0us 1h = 6us 2h = 45us 3h = 175us
7-4	RESERVED	R	Fh	Reserved
3-2	E10_CONFIG_CH2	R/W	0h	E10 Config masking time
1	UVLO_LPM_EN_CH2	R/W	0h	UVLO CH2 Enable during LPM 0h = UVLO functionality disabled in LPM 1h = UVLO functionality enabled in LPM
0	UVLO_EN_CH2	R/W	0h	UVLO CH2 Enable 0h = UVLO functionality disabled 1h = UVLO functionality enabled

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8.1.40 OV_CONFIG_CH1 Register (Offset = 39h) [Reset = 8AFCh]

OV_CONFIG_CH1 is shown in Table 8-42.

Return to the Summary Table.

Table 8-42. OV_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	OVLO_SET_CH1	R/W	8h	OVLO rising protection Threshold Setting 00h = 8V 01h = 16V 02h = 18V 03h = 36V 04h = 38V 05h = 40V 06h = 42V 07h = 44V 08h = 54V 09h = 56V 0Ah = 58V 0Bh = 60V 0Ch = 66V 0Dh = 68V 0Eh = 70V 0Fh = 72V
11-10	OVLO_HYST_CH1	R/W	2h	OVLO CH1 Hysteresis Setting 0h = 2V 1h = 4V 2h = 6V 3h = 8V
9-8	OVLO_MASK_CH1	R/W	2h	OVLO masking delay for CH2 0h = 0us 1h = 6us 2h = 45us 3h = 175us
7-2	RESERVED	R	3Fh	Reserved
1	OVLO_LPM_EN_CH1	R/W	0h	OVLO CH1 Enable during LPM 0h = OVLO functionality disabled in LPM 1h = OVLO functionality enabled in LPM
0	OVLO_EN_CH1	R/W	0h	OVLO CH1 Enable 0h = OVLO functionality disabled 1h = OVLO functionality enabled

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8.1.41 OV_CONFIG_CH2 Register (Offset = 3Ah) [Reset = 8AFCh]

OV_CONFIG_CH2 is shown in Table 8-43.

Return to the Summary Table.

Table 8-43. OV_CONFIG_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	OVLO_SET_CH2	R/W	8h	OVLO rising protection Threshold Setting 00h = 8V 01h = 16V 02h = 18V 03h = 36V 04h = 38V 05h = 40V 06h = 42V 07h = 44V 08h = 54V 09h = 56V 0Ah = 58V 0Bh = 60V 0Ch = 66V 0Dh = 68V 0Eh = 70V 0Fh = 72V
11-10	OVLO_HYST_CH2	R/W	2h	OVLO CH2 Hysteresis Setting 0h = 2V 1h = 4V 2h = 6V 3h = 8V
9-8	OVLO_MASK_CH2	R/W	2h	OVLO masking delay for CH2 0h = 0us 1h = 6us 2h = 45us 3h = 175us
7-2	RESERVED	R	3Fh	Reserved
1	OVLO_LPM_EN_CH2	R/W	0h	OVLO CH2 Enable during LPM 0h = OVLO functionality disabled in LPM 1h = OVLO functionality enabled in LPM
0	OVLO_EN_CH2	R/W	0h	OVLO CH2 Enable 0h = OVLO functionality disabled 1h = OVLO functionality enabled

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8.1.42 VDS_CONFIG Register (Offset = 3Bh) [Reset = 2142h]

VDS_CONFIG is shown in Table 8-44.

Return to the Summary Table.

Table 8-44. VDS_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VDS_PROT_EN_CH2	R/W	0h	Enable VDS Protection for Channel 2
14	VDS_PROT_EN_CH1	R/W	0h	Enable VDS Protection for Channel 1
13-9	VDS_OVP_SET_CH2	R/W	10h	VDS protection Threshold set for CH2. Refer Table 7-2 for threshold settings.
8-7	VDS_OVP_MASK_CH2	R/W	2h	VDS masking delay setting for CH2 0h = 0us 1h = 5us 2h = 45us 3h = 245us
6-2	VDS_OVP_SET_CH1	R/W	10h	VDS protection Threshold set for CH1. Refer Table 7-2 for threshold settings.
1-0	VDS_OVP_MASK_CH1	R/W	2h	VDS masking delay setting for CH1 0h = 0us 1h = 5us 2h = 45us 3h = 245us

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8.1.43 TEMP_CONFIG Register (Offset = 3Ch) [Reset = 8403h]

TEMP_CONFIG is shown in Table 8-45.

Return to the Summary Table.

Table 8-45. TEMP_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	TSNS_TSD_SET_CH2	R/W	10h	External FET overtemperature (TSD) threshold for CH2 00h = 45°C 1B TO 0XFFh = Reserved 01h = 50°C 02h = 55°C 03h = 60°C 04h = 65°C 05h = 70°C 06h = 75°C 07h = 80°C 08h = 85°C 09h = Reserved 0Ah = 90°C 0Bh = 95°C 0Ch = 100°C 0Dh = Reserved 0Eh = 105°C 0Fh = 110°C 10h = Reserved 11h = 115°C 12h = 120°C 13h = 125°C 14h = 130°C 15h = 135°C 16h = 140°C 17h = 145°C 18h = 150°C 19h = 155°C 1Ah = 160°C
10-6	TSNS_TSD_SET_CH1	R/W	10h	External FET overtemperature (TSD) threshold for CH1 1B TO 0XFFh = Reserved 00h = 45°C 01h = 50°C 02h = 55°C 03h = 60°C 04h = 65°C 05h = 70°C 06h = 75°C 07h = 80°C 08h = 85°C 09h = Reserved 0Ah = 90°C 0Bh = 95°C 0Ch = 100°C 0Dh = Reserved 0Eh = 105°C 0Fh = 110°C 10h = Reserved 11h = 115°C 12h = 120°C 13h = 125°C 14h = 130°C 15h = 135°C 16h = 140°C 17h = 145°C 18h = 150°C 19h = 155°C 1Ah = 160°C

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Table 8-45. TEMP_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	TSNS_TSD_MASK_CH2	R/W	0h	2 bit setting to set the masking time for TSD CH2 0h = 0us 1h = 7.5us Ah = 50us Bh = 500us
3-2	TSNS_TSD_MASK_CH1	R/W	0h	2 bit setting to set the masking time for TSD CH1 0h = 0us 1h = 7.5us Ah = 50us Bh = 500us
1	TSD_EN_CH2	R/W	1h	1 bit to enable/disable the TSD CH2 0h = TSD functionality disabled for CH2 1h = TSD functionality enabled for CH2
0	TSD_EN_CH1	R/W	1h	1 bit to enable/disable the TSD CH1 0h = TSD functionality disabled for CH1 1h = TSD functionality enabled for CH1

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8.1.44 DEV_CONFIG_2 Register (Offset = 3Dh) [Reset = 0000h]

DEV_CONFIG_2 is shown in Table 8-46.

Return to the Summary Table.

Table 8-46. DEV_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTOLPM_COMP_ACTIVE_SD_EN	R/W	0h	This bit will enables the GATEx to turn off when the AUTOLPM comparator detects high in active 0h = AUTOLPM comparator has no effect on gate control in active mode. 1h = GATEx turn off when the AUTOLPM comparator trips in active mode.
14	TSD_CONT_FLT_EN	R/W	0h	This bit will signal flt when the Controller overtemperature warning bit goes high. 0h = Controller overtemperature warning is not signalled on the FLT pin. 1h = Controller overtemperature warning is signalled on the FLT pin.
13	ISNS_POLARITY_FLT_EN	R/W	0h	This bit will be set high when the ISNS_POLARITY bit goes to 1 0h = ISNS_POLARITY_CHx based FLT is not signalled on the FLT pin. 1h = ISNS_POLARITY_CHx based FLT is signalled on the FLT pin
12	RNTC_TYPE_CH2	R/W	0h	This bit sets the RNTC type for the TSNS CH2 0h = 10k NTC at 25C 1h = 47k NTC at 25C
11	RNTC_TYPE_CH1	R/W	0h	This bit sets the RNTC type for the TSNS CH1 0h = 10k NTC at 25C 1h = 47k NTC at 25C
10	LOAD_WAKE_DEGLITCH	R/W	0h	This bit sets the deglitch on the Load Wakeup 0h = Load Wakeup is not deglitched 1h = Load Wakeup is deglitched by 50us
9-8	SAMPLING_FREQ_CH2	R/W	0h	sets the Frequency for the sampling in LPM for CH2 when the EN_SAMPLING_CH2 is set 0h = 10Hz 1h = 20Hz Ah = 40Hz Bh = 80Hz
7-6	SAMPLING_FREQ_CH1	R/W	0h	sets the Frequency for the sampling in LPM for CH1 when the EN_SAMPLING_CH1 is set 0h = 10Hz 1h = 20Hz Ah = 40Hz Bh = 80Hz
5	EN_SAMPLING_CH2	R/W	0h	This bit sets the sampling on the CP during LPM for CH2 0h = CP Sampling functionality in LPM disabled for CH2 1h = CP Sampling functionality in LPM enabled for CH2
4	EN_SAMPLING_CH1	R/W	0h	This bit sets the sampling on the CP during LPM for CH1 0h = CP Sampling functionality during LPM disabled for CH1 1h = CP Sampling functionality during LPM enabled for CH1
3-2	CONFIG_DI_MASK	R/W	0h	This bit sets the masking time on the DIx/OUT_DISx pin 0h = 0us 1h = 8.5us Ah = 12us Bh = 23us
1-0	CONFIG_LHI_MASK	R/W	0h	This bit sets the masking time on the LHI pin 0h = 0us 1h = 10us Ah = 12us Bh = 23us

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8.1.45 DEV_CONFIG_3 Register (Offset = 3Eh) [Reset = FF00h]

DEV_CONFIG_3 is shown in Table 8-47.

Return to the Summary Table.

Table 8-47. DEV_CONFIG_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	FFh	Reserved
7	EN_GRTR_PAAT_THRESH	R/W	0h	This bit will enable high threshold for FET_SHRT_BIST for all channel in ON state for the use cases where supply can have some transients 0h = PAAT Threshold is 0.8V 1h = PAAT Threshold is 7V
6	LIMPHOME_STAT_FLT_EN	R/W	0h	This bit enable LIMPHOME_STAT bit on FLT pin. 0h = LIMPHOME_STAT bit is not signalled on the FLT pin 1h = LIMPHOME_STAT bit is signalled on the FLT pin
5	CNFG_ISNS_DLY_CH2	R/W	0h	This bit to select the delay for ISNS for CH2
4	CNFG_ISNS_DLY_CH1	R/W	0h	This bit to select the delay for ISNS for CH1
3-2	VDS_GAIN_CH2	R/W	0h	This bit sets the gain of the VDS amplifier for CH2 00 = Disable VDS sense and protection 01 = 1.5 V/V 10 = 8 V/V 11 = 30 V/V
1-0	VDS_GAIN_CH1	R/W	0h	This bit sets the gain of the VDS amplifier for CH1 00 = Disable VDS sense and protection 01 = 1.5 V/V 10 = 8 V/V 11 = 30 V/V

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8.1.46 EEPROM_PROGRAM_CONTROL_STATUS Register (Offset = 3Fh) [Reset = FFFCh]

EEPROM_PROGRAM_CONTROL_STATUS is shown in Table 8-48.

Return to the Summary Table.

Table 8-48. EEPROM_PROGRAM_CONTROL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	3FFFh	Reserved
1	RESERVED	R	0h	This bit indicates if eeprom is busy in NVM Read or Re-program sequence. 0h = No eeprom related operation 1h = EEPROM is busy
0	RESERVED	R	0h	This bit indicates if eeprom is undergoing re-program sequence. This bit self clears to 0 after operation completion. 0h = No eeprom related operation 1h = EEPROM is undergoing reprogram sequence

8.2 EEPROM (NVM) Overview

TPS12S24F-Q1 provides user programmable Electrically Erasable Programmable Read-Only Memory (EEPROM) for some configuration registers and some customer defined programmable registers. This enables the user to reprogram the default values for these registers. Table shows which registers can be programmed through the EEPROM programming procedure.

Table 8-49. Register Overview

OFFSET	REGISTER NAME	EEPROM USER PROGRAMMABLE
00h	DEV_ID	N
01h	SLEEP	N
02h	LPM	N
03h	FAULT_GLOBAL	N
04h	FAULT_MASK	Y
05h	BIST_RESULT	N
06h	SW_STATE	N
07h	DEVICE_TEST	N
08h	DEV_CONFIG	Y
09h	ADC_CONFIG	N
0Ah	ADC_RESULT_VBB	N
0Bh	ADC_RESULT_BIST	N
0Ch	FLT_STAT_CH1	N
0Dh	PWM_CH1	Y
0Eh	ILIM_CONFIG_CH1	Y
0Fh	DIAG_CONFIG _CH1	Y
10h	ADC_RESULT_CH1_I	N
11h	ADC_RESULT_CH1_T	N
12h	ADC_RESULT_CH1_V	N
13h	ADC_RESULT_CH1_VDS	N
14h	I2T_CONFIG_CH1	Y
15h	FLT_STAT_CH2	N
16h	PWM_CH2	Y
17h	ILIM_CONFIG_CH2	Y

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Table 8-49. Register Overview (continued)

OFFSET	REGISTER NAME	EEPROM USER PROGRAMMABLE
18h	DIAG_CONFIG _CH2	Y
19h	ADC_RESULT_CH2_I	N
1Ah	ADC_RESULT_CH2_T	N
1Bh	ADC_RESULT_CH2_V	N
1Ch	ADC_RESULT_CH2_VDS	N
1Dh	I2T_CONFIG_CH2	Y
1Eh	I2T_TRIP_CH1	Y
1Fh	I2T_ACC_RD_CH1	N
20h	I2T_ACC_RD_CH2	N
32h	DEVICE_DIAGNOSTIC	N
33h	I2T_TRIP_CH2	Y
34h	ADC_RESULT_TCONT	N
35h	SCP_CONFIG_CH1	Y
36h	SCP_CONFIG_CH2	Y
37h	UV_CONFIG_CH1	Y
38h	UV_CONFIG_CH2	Y
39h	OV_CONFIG_CH1	Y
3Ah	OV_CONFIG_CH2	Y
3Bh	VDS_CONFIG	Y
3Ch	TEMP_CONFIG	Y
3Dh	DEV_CONFIG_2	Y
3Eh	DEV_CONFIG_2	Y
3Fh	EEPROM_PROGRAM_CONTROL_STATUS	Y

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EEPROM programming procedure

The default values for the user programmable registers can be reprogrammed through the below procedure. The following conditions need to be met in order to re-program the EEPROM correctly

- VS voltage ≥ 6V, referenced to device GND
- VDD voltage > VDD_UVLO, referenced to device GND

Figure shows the procedure of how to re-program the default values.

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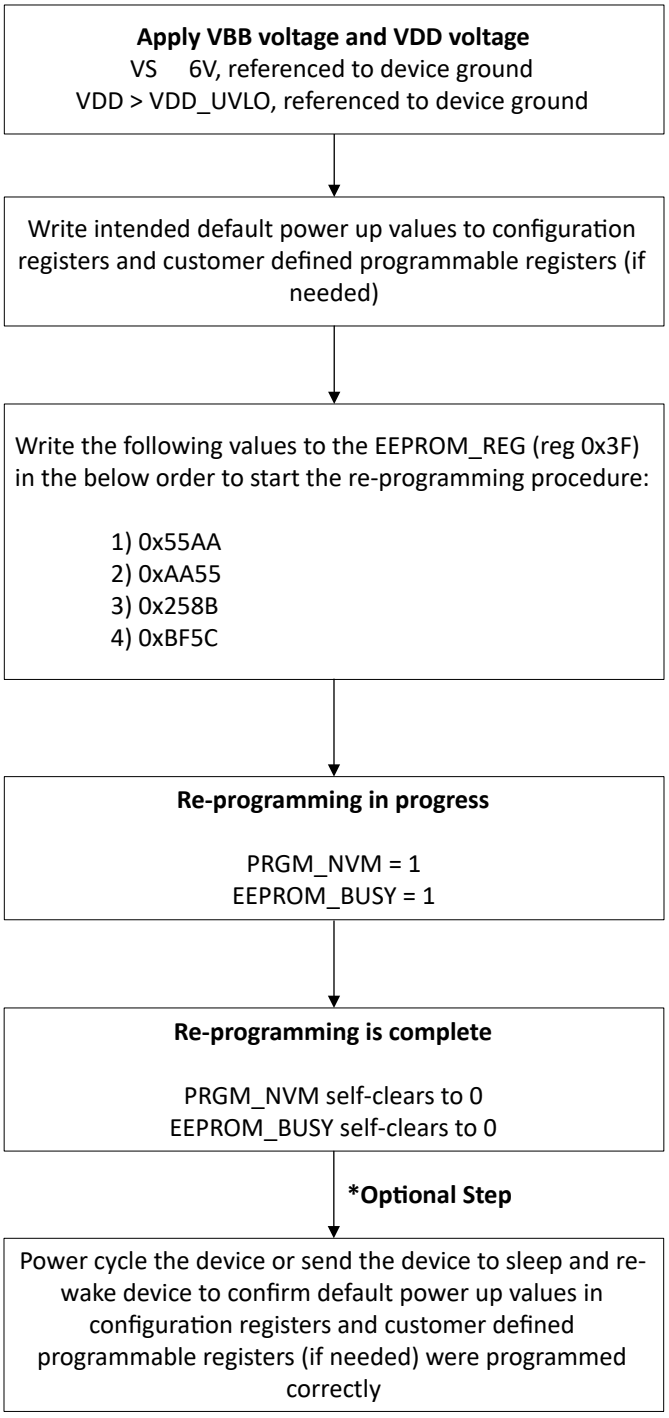


Figure 8-1. EEPROM Re-Programming Procedure

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9 Application and Implementation

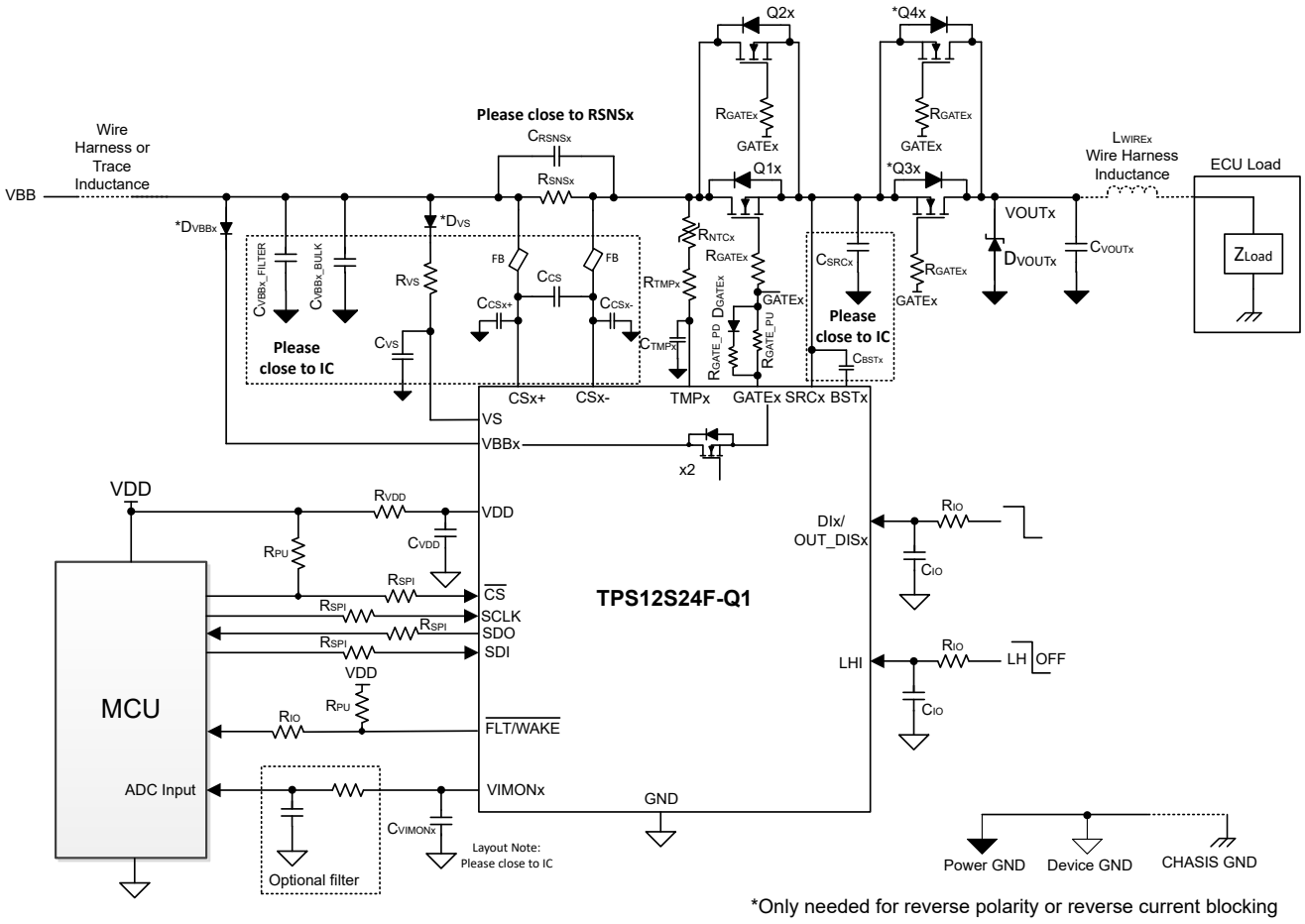
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

9.2.1 Driving Power at All Times (PAAT) Loads With Automatic Load Wakeup and Output Bulk Capacitor Charging



*Only needed for reverse polarity or reverse current blocking

Figure 9-1. Typical Application

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Example Programming Procedure

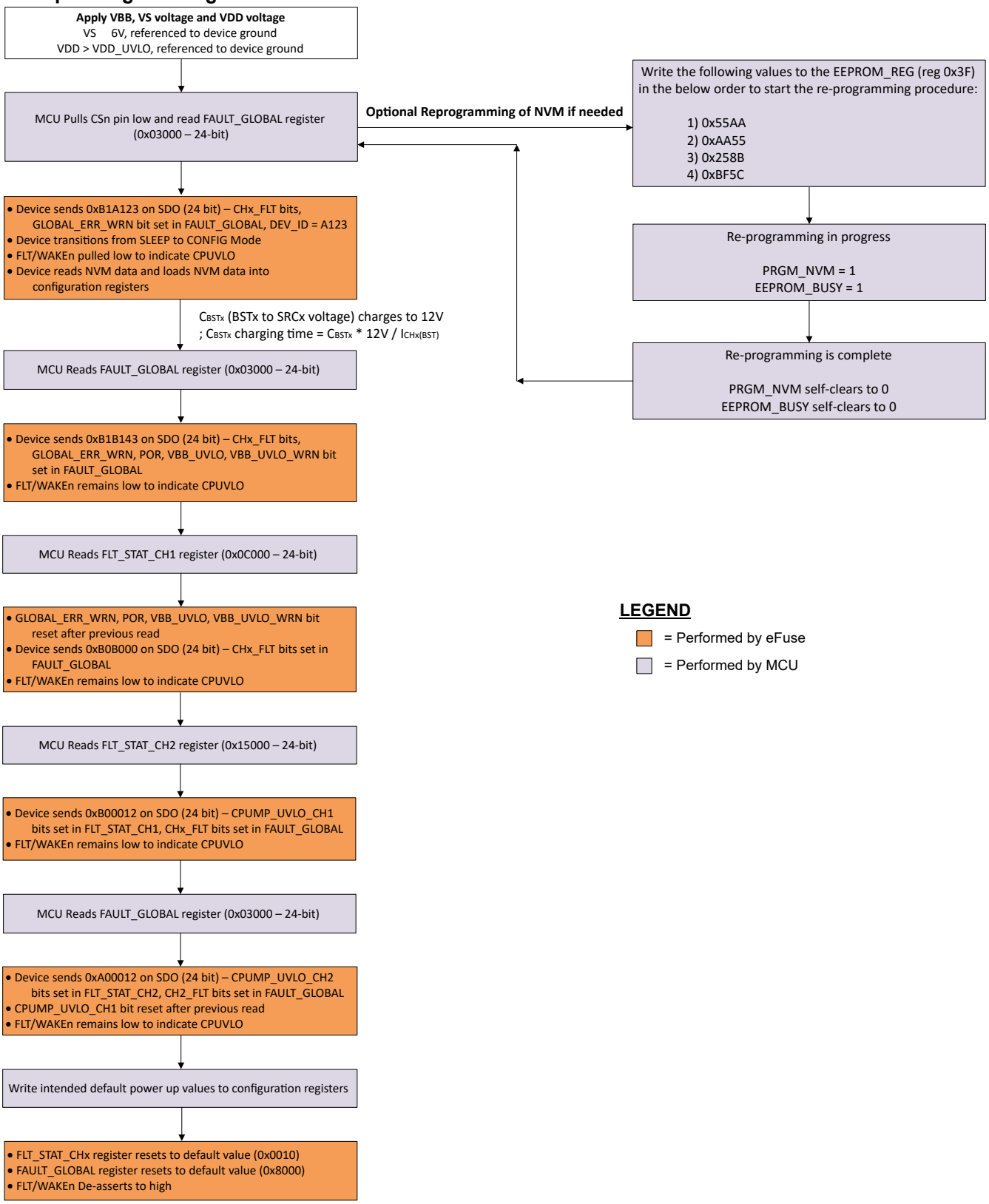


Figure 9-2. TPS12S24F-Q1 Example Programming Procedure

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9.2.1.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Typical input voltage, V_{BATT_MIN} to V_{BATT_MAX}	16V to 60V for 48V system design Or 6V to 35V for 12V system design
Undervoltage lockout set point, $V_{(VBB_UVLOF)}$	16V for 48V system design 6V for 48V system design
Maximum load current, I_{OUT}	50A
I^2t Start threshold, I_{NOM}	60A
Short-circuit protection threshold, I_{SC}	150A
Fault response	Latch
Load wakeup threshold, I_{LWU}	100mA
Output bulk capacitor, C_{BULK}	3mF

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Selection of Main Path MOSFETs

For selecting the main path MOSFETs, important electrical parameters are the maximum continuous drain current ID, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance $R_{DS(ON)}$. The maximum continuous drain current rating (ID) must exceed the maximum continuous load current. The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application.

9.2.1.2.2 Selection of Bootstrap Capacitor, C_{BSTx}

The internal charge pump charges the external bootstrap capacitor (connected between BSTx and SRCx pins) with $I_{CHx(BST)}$. Use Equation 14 to calculate the minimum required value of the bootstrap capacitor for driving multiple FETs in parallel.

$$C_{BSTx} = 10 \times \left[\frac{Q_{gx(total)}}{\Delta V_{BST}} + C_{GATEx}\right] \quad (14)$$

C_{GATEx} is needed only when main FET gate slew rate control method is used for bulk capacitor charging.

Table 9-2. Configuration Register Settings

BIT FIELD NAME	SETTING
CAP_CHRG_CHx	Sets capactior charging method
INRUSH_DURATION_CHx	Sets inrush duration
LPM_EXIT_CURR_CHx	Sets load wakeup current
UV_CONFIG_CHx	Sets VBB UVLO threshold, hysteresis and masking time
I2T_CONFIG_CHx	Sets I2t start threshold, cooldown timer
I2T_TRIP_CHx	Sets I2t trip threshold
SCP_CONFIG_CHx	Sets SCP threshold, masking time
LATCH_CHx	Auto-retry or latch

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9.2.1.3 Application Curves

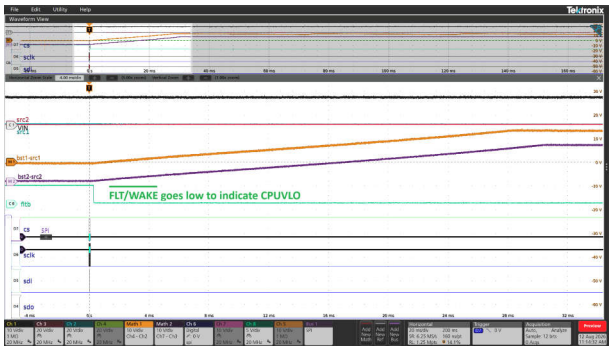


Figure 9-3. $\overline{CS}$ Pulled From High to Low For Device Transition From SLEEP to CONFIG Mode

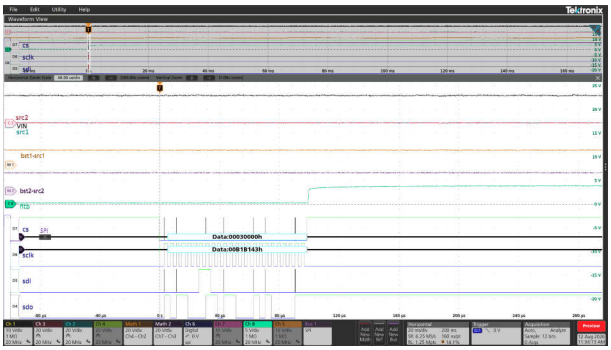


Figure 9-4. Read FLT_STAT_CHx First and Then FAULT_GLOBAL Registers to Clear These Registers and Deassert $\overline{FLT/WAKE}$ Pin

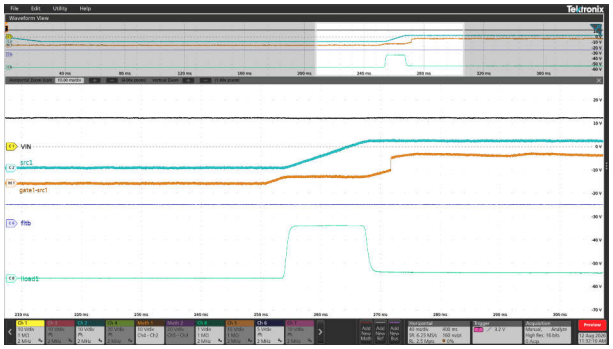


Figure 9-5. CHx_ON Bit Set From '0' to '1' With CAP_CHRG_CHx = 0x1 (Main Path GATE Slew Rate Control) With C_{OUT} = 3.3mF, C_{GATE} = 100nF, C_{BST} = 2µF

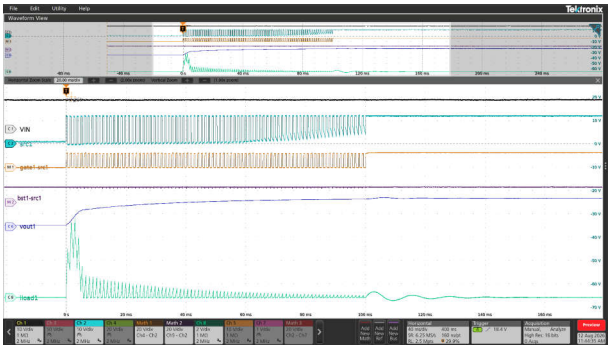


Figure 9-6. CHx_ON Bit Set From '0' to '1' With CAP_CHRG_CHx = 0x3 (PWM Method) With C_{OUT} = 3.3mF, C_{GATE} = 100nF, C_{BST} = 2µF, LIN = 5µH, LOUT = 1mH, PWM Frequency = 885Hz

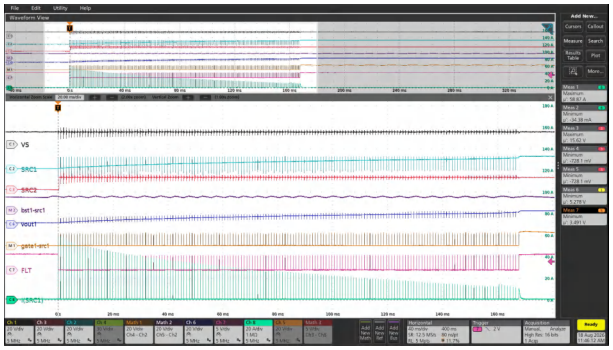


Figure 9-7. CHx_ON Bit Set From '0' to '1' With CAP_CHRG_CHx = 0x0 (SCP Based Auto Retry) With COUT = 3.3mF, CBST = 2µF, LIN = 2µH, LOUT = 1µH, SCP Threshold = 10mV, SCP Delay = 5.2µs, Auto Retry Time = 1ms, FOLDBACK_LATCH_DIS = 0x1 (Infinite Auto Retry Cycle)

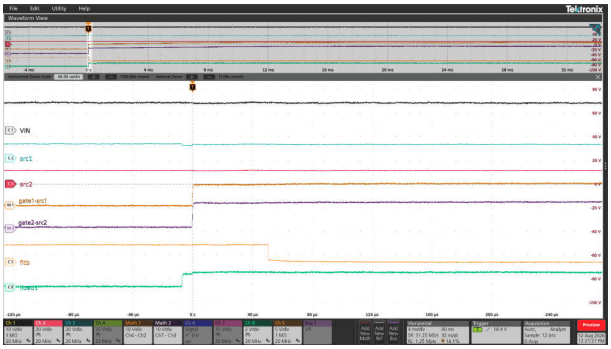


Figure 9-8. LPM to Active Mode Via Increase in Load Current

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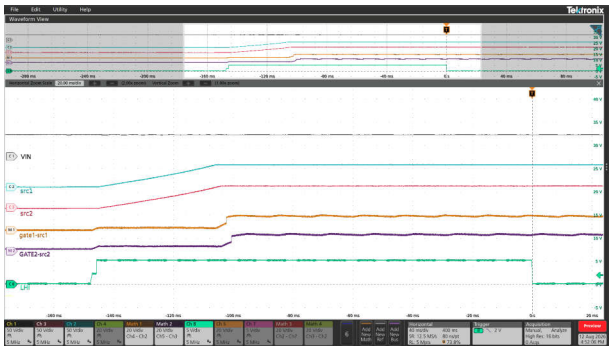


Figure 9-9. CONFIG to LIMPHOME Mode When LHI is Pulled From Low to High With CAP_CHRG_CHx = 0x1 (Main Path GATE Slew Rate Control) With C_{OUT} = 3.3mF, C_{GATE} = 100nF, C_{BST} = 2µF

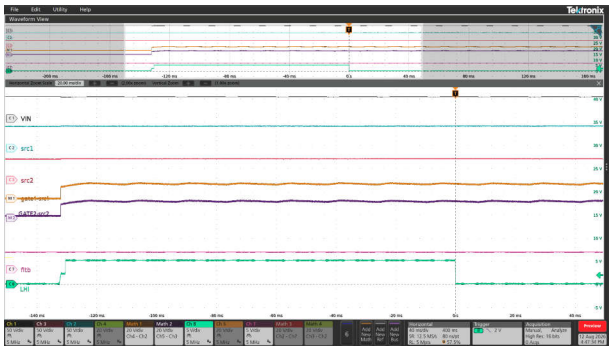


Figure 9-10. LPM to LIMPHOME Mode When LHI is Pulled From Low to High

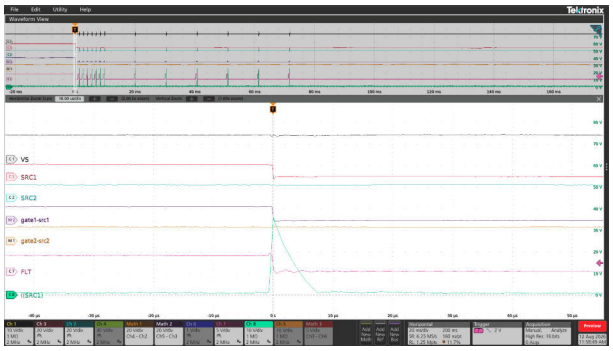


Figure 9-11. Output Short to Ground Fault Behavior on CH1 in ACTIVE Mode With RSNS = 1mΩ, SCP Threshold = 20mV, SCP Delay = 1.1µs, FOLDBACK_LATCH_DIS = 0x0 (Finite Auto Retry Cycle)



Figure 9-12. Zoomed Output Short to Ground Fault Behavior on CH1 in ACTIVE Mode With RSNS = 1mΩ, SCP Threshold = 20mV, SCP Delay = 1.1µs, Auto Retry Duration = 1ms, FOLDBACK_LOCK_DIS = 0x0 (Finite Auto Retry Cycle)



Figure 9-13. Zoomed Output Short to Ground Fault Behavior on CH1 in ACTIVE Mode With RSNS = 1mΩ, SCP Threshold = 20mV, SCP Delay = 1.1µs, Auto Retry Duration = 1ms, FOLDBACK_LOCK_DIS = 0x1 (Infinite Auto Retry Cycle)

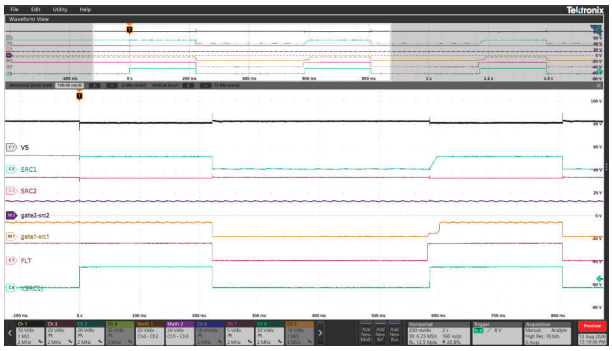


Figure 9-14. I2T Protection Behavior on CH1 in ACTIVE Mode

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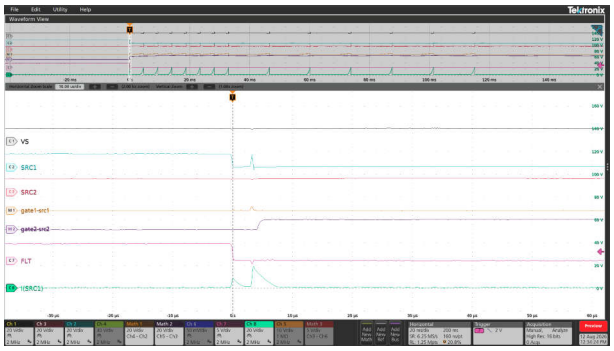


Figure 9-15. Output Short to Ground Fault Behavior on CH1 in LOW POWER Mode (LPM) With RSNS = 1mΩ, SCP Threshold = 20mV, SCP Delay = 1.1µs, FOLDBACK_LATCH_DIS = 0x0 (Finite Auto Retry Cycle)

9.3 System Examples

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9.3.1 TPS12S24F-Q1 System Level Configurations

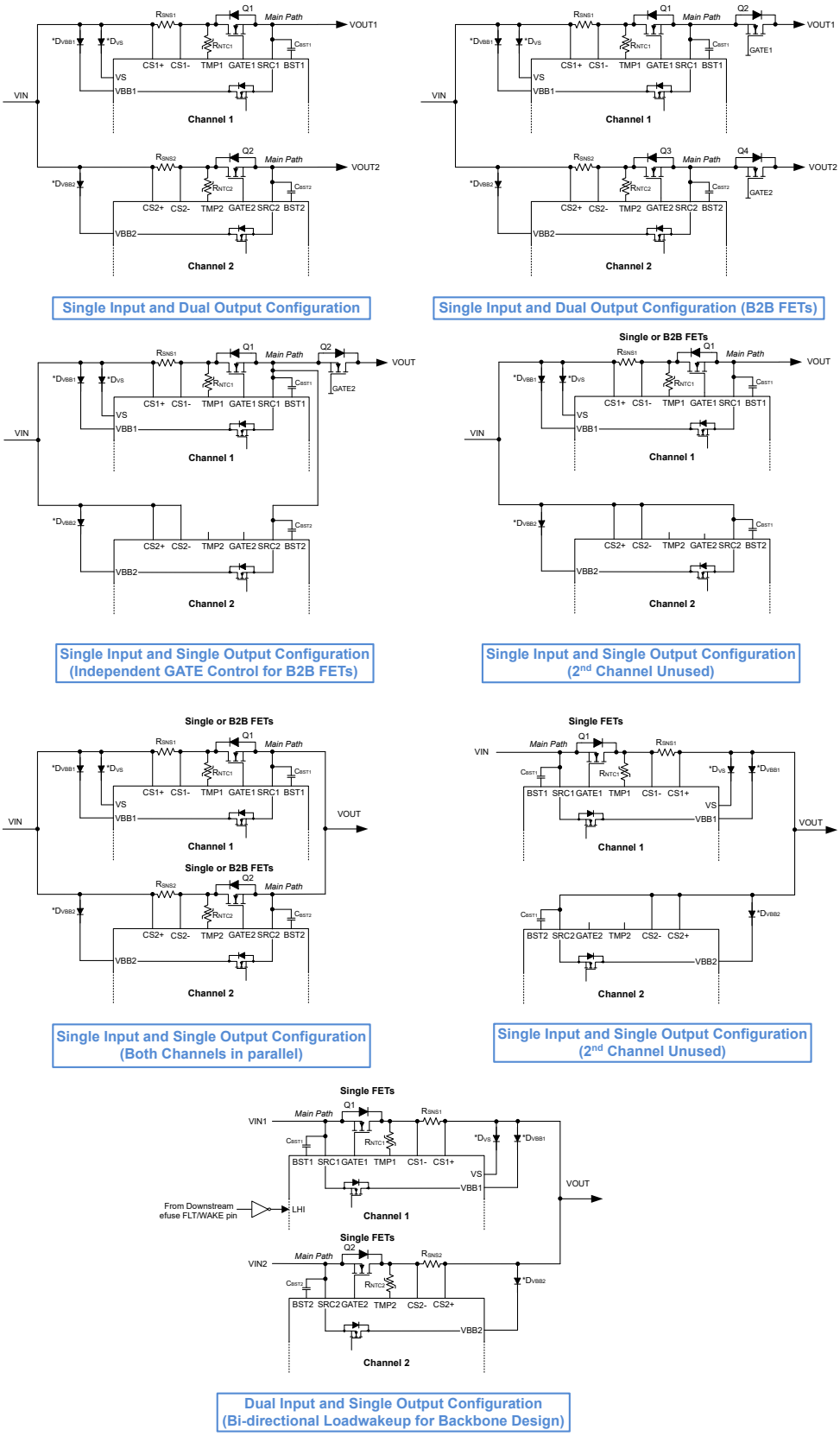


Figure 9-16. System Level Configurations Supported With TPS12S24F-Q1

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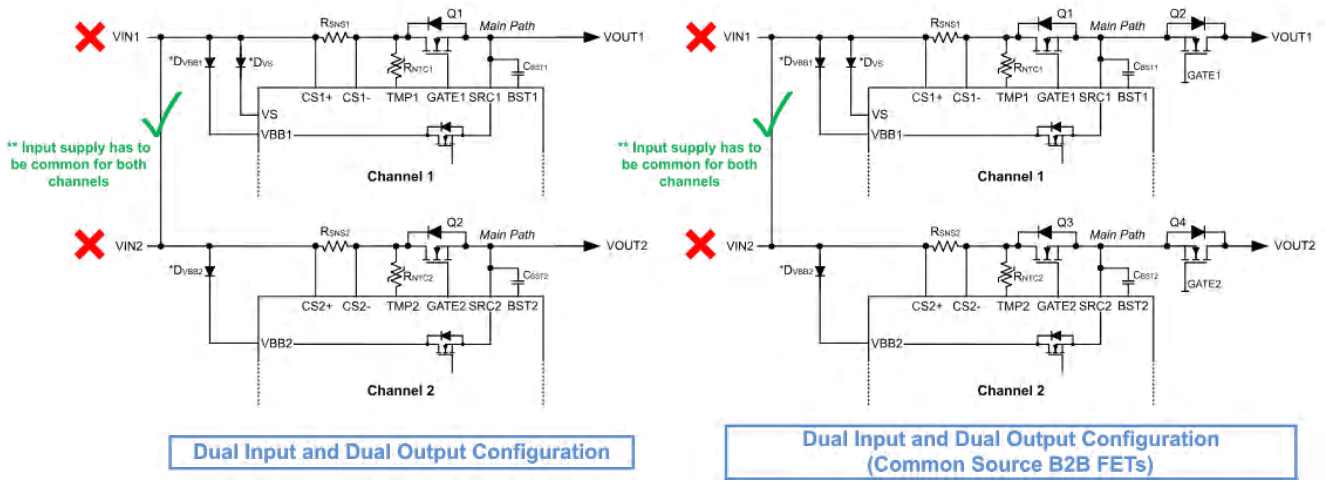


Figure 9-17. System Level Configurations Not Supported With TPS12S24F-Q1

9.4 Power Supply Recommendations

9.4.1 Transient and EMI/EMC Recommendations

When the external MOSFETs turn-OFF during the conditions such as GATEx control, overcurrent or short-circuit or FET overtemperature protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the Absolute Maximum Ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

Figure 9-18 shows the circuit implementation with optional protection components.

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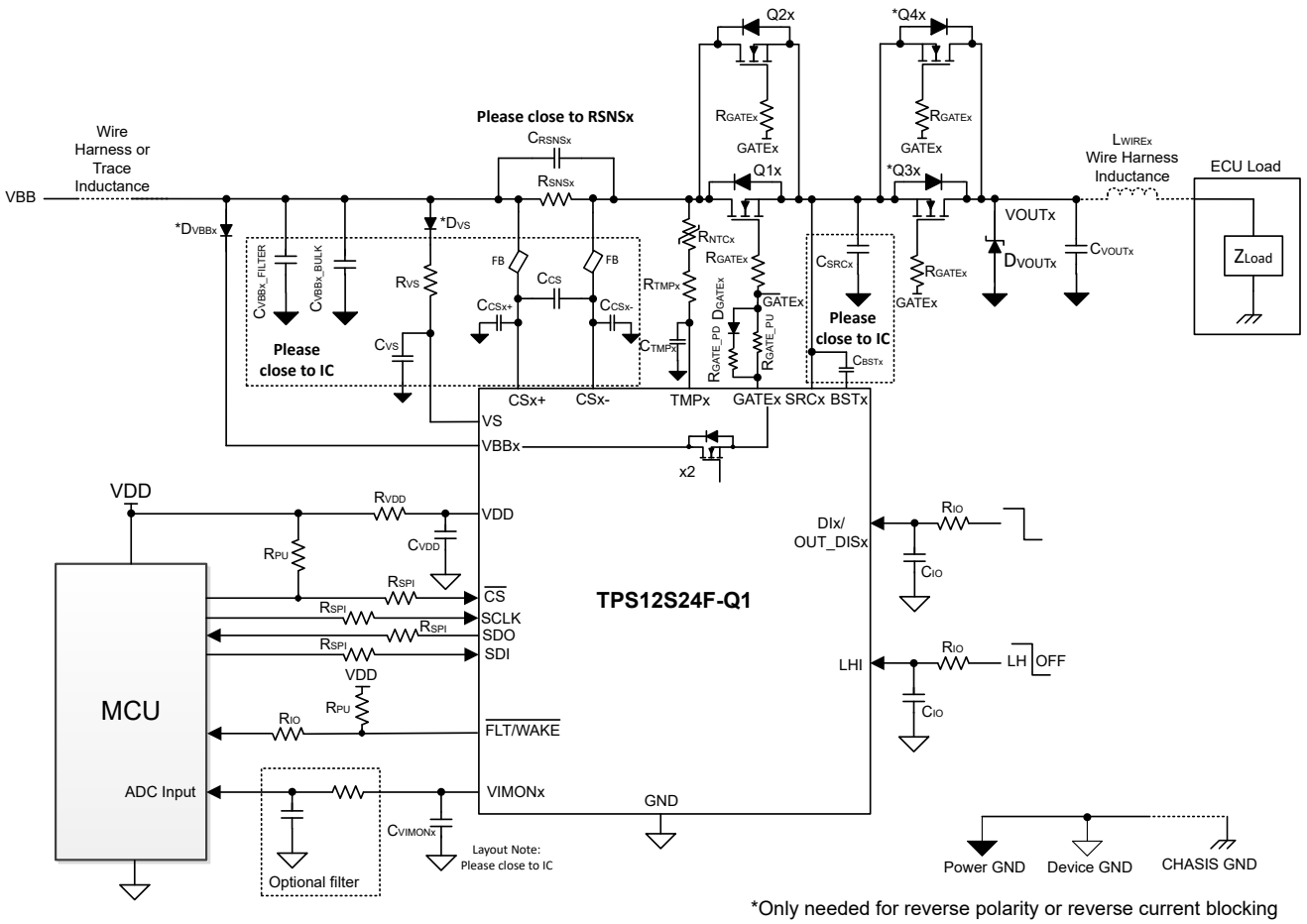


Figure 9-18. Circuit Implementation Protection Components For TPS12SxxF-Q1

Table 9-3. Power Supply and EMI Recommendation Components

COMPONENT DESIGNATOR	DESCRIPTION	RECOMMENDED VALUE
R_{VS}, C_{VS}	Device gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS_PORR)}$ level to provide proper operation during noisy line transients.	100Ω, 1-10µF
R_{VDD}, C_{VDD}	Voltage at this pin must be maintained above $V_{(VDD_PORR)}$ level to provide proper operation during noisy line transients.	4.7 to 10Ω, 1-10µF
C_{VBBx_BULK}	Need to prevent undervoltage for device during fast output hard-short to ground fault. Place close to device CSx+ pin.	10-100µF
C_{VBBx_FILTER}	Need to filter out supply transients. Place close to device CSx+ pin.	0.01-1µF
$*D_{VBBx}$, $*D_{VS}$, $*Q3_x$, $*Q_{4x}$	Needed for input reverse polarity protection	Schottky diode on VS and VBBx
FB1, FB2, C_{CS}, C_{CSx+}, C_{CSx-}, C_{VIMONx}, C_{TMPx}	Ferrite beads (FB1, FB2) can be required at CSx+, CSx- pins for better immunity performance during EMI/EMC testing. Some other filtering is also required based on type of immunity test and frequency band through C_{CS}, C_{CSx+}, C_{CSx-}, C_{TMPx} and C_{VIMONx} to achieve robust immunity performance. Select ferrite beads so that DC Resistance is very low on CSx+ and CSx- pin to avoid significantly impacting ISNS, I2T and SCP accuracy.	MMZ1608B102CTA00, 10pF for C_{TMPx} and 10pF - 100nF for others
R_{GATE_PU}, R_{GATE_PD}, D_{GATEx}, R_{GATEx}	Resistors on GATE pins can be used for controlling rise and fall time of external FETs. Separate R_{GATE_PU} must be used for individual external FETs connected in parallel.	Any value

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Table 9-3. Power Supply and EMI Recommendation Components (continued)

COMPONENT DESIGNATOR	DESCRIPTION	RECOMMENDED VALUE
C_{SRCx}, C_{VOUTx}	Limit slew rate on SRCx pin <200V/us during fast output hard-short to ground fault. Use I = C × dV/dt for C_{SRCx} calculation where I = Peak current, dV is maximum input voltage, dt = turn off time of GATEx	0.1-10µF
R_{SPI}	All SPI or I/O pins must connect to MCU or other HI/LO source through a resistor for protection transient events. *Higher series resistor can limit SPI communication frequency so series resistor must be selected carefully based on equivalent parasitic capacitance on SPI lines.	100 - 500Ω
R_{SDO}	SDO pin must connect to MCU or other HI/LO source through a resistor for protection transient events.	100 - 1000Ω
R_{IO}, C_{IO}	Filters out transient on LHI and DIx/OUT_DISx pins	0.01 - 10kΩ, 1-10nF
R_{PU}	Pull up resistor	1 - 10kΩ

ADVANCE INFORMATION

9.5 Layout

9.5.1 Layout Guidelines

- The sense resistor (R_{SNSx}) must be placed close to the TPS12S24F-Q1 and then connect R_{SNSx} using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.
- For all the applications, TI recommends 1µF or higher and 0.1µF in parallel ceramic decoupling capacitor between VS terminal and GND. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- For all the applications, TI recommends 0.1µF ceramic decoupling capacitor between SRCx terminal and GND to limit the slew rate on SRCx during GATEx turn off.
- The high current path from the board's input to the load, and the return path, must be parallel and close to each other to minimize loop inductance.
- The external MOSFETs must be placed close to the controller such that the gate of the MOSFETs are close to GATEx pin to form short GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high-frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- The external bootstrap capacitor must be placed close to BSTx and SRCx pins to form very short loop.
- The ground connections for the various components around the TPS12S24F-Q1 must connect directly to each other, the GNS of the TPS12S24F-Q1, and then the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

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9.5.2 Layout Example

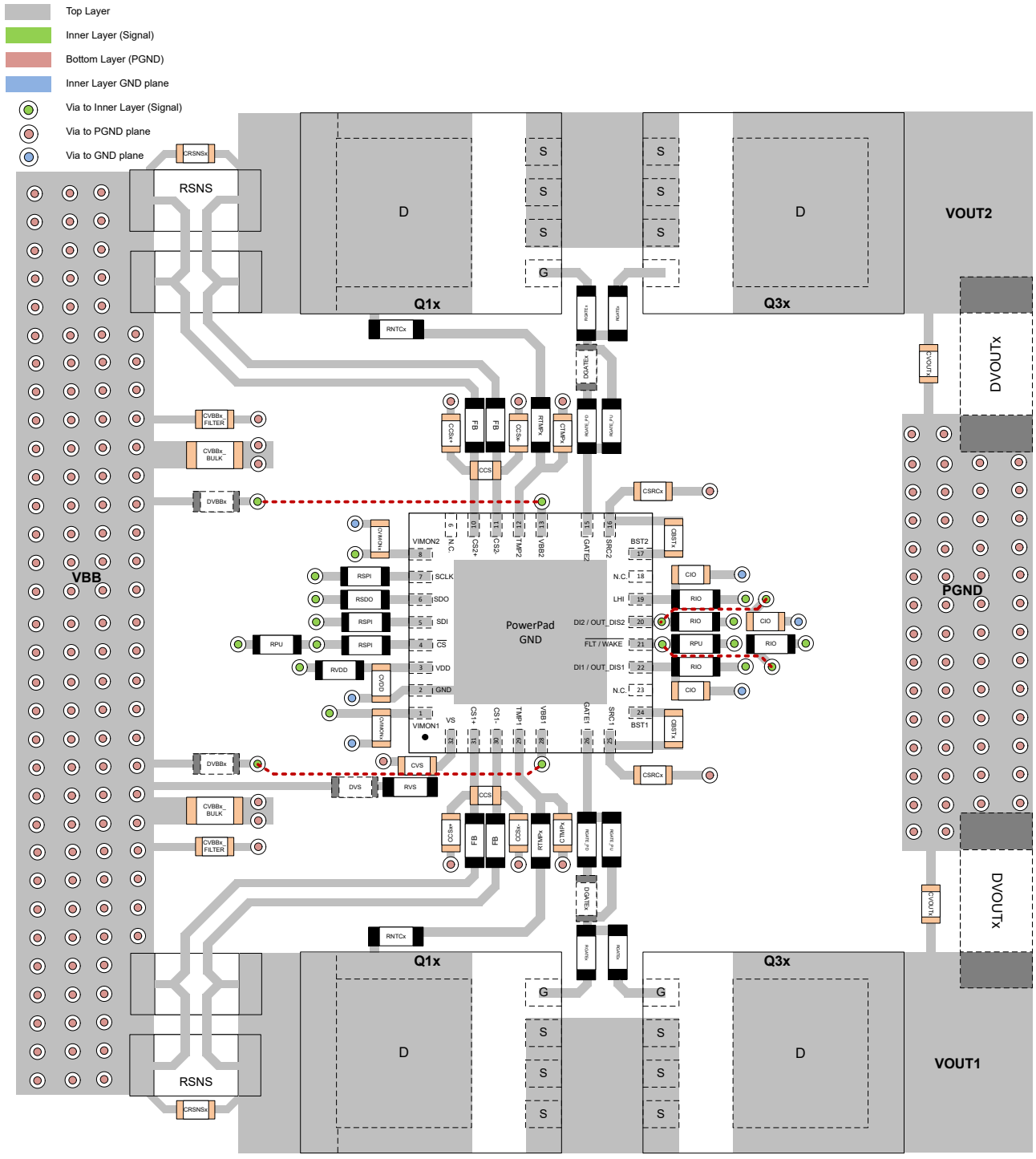


Figure 9-19. Typical PCB Layout Example of TPS12S24F-Q1

ADVANCE INFORMATION

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

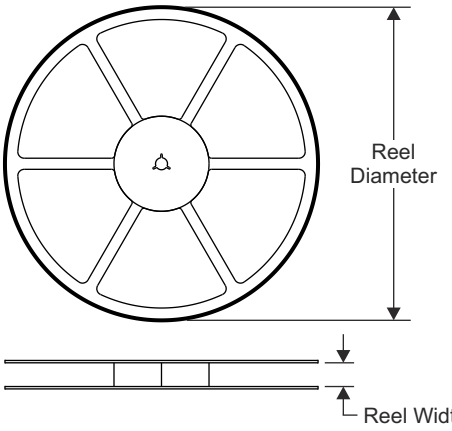
Changes from Revision * (August 2026) to Revision A (November 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated absolute maximum ratings	6
• Updated recommended operating conditions	6
• Updated electrical characteristics	7
• Updated switching characteristics	9
• Updated using PWM control method (GATEx) section	22
• Updated resistive or inductive load driving section	23
• Updated Table 7-2	30
• Updated SPI section	47
• Updated figures in SPI frame format section	47
• Updated Table 7-11	55
• Updated registers	57

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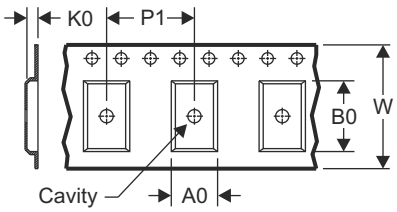
12 Mechanical, Packaging, and Orderable Information

12.1 Tape and Reel Information

REEL DIMENSIONS

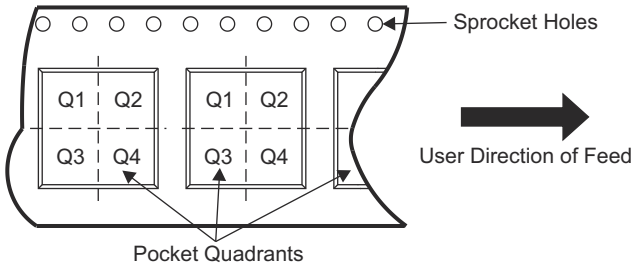


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



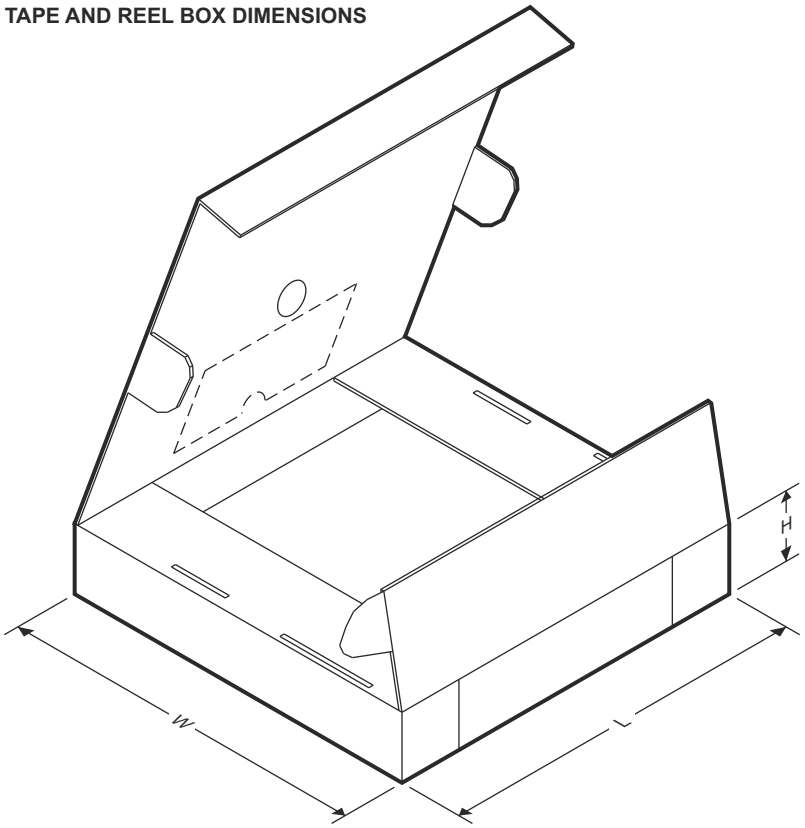
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS12S24FQRHBRQ1	VQFN	RHB	30	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS12S24FQRHBRQ1	VQFN	RHB	30	3000	367.0	367.0	35.0

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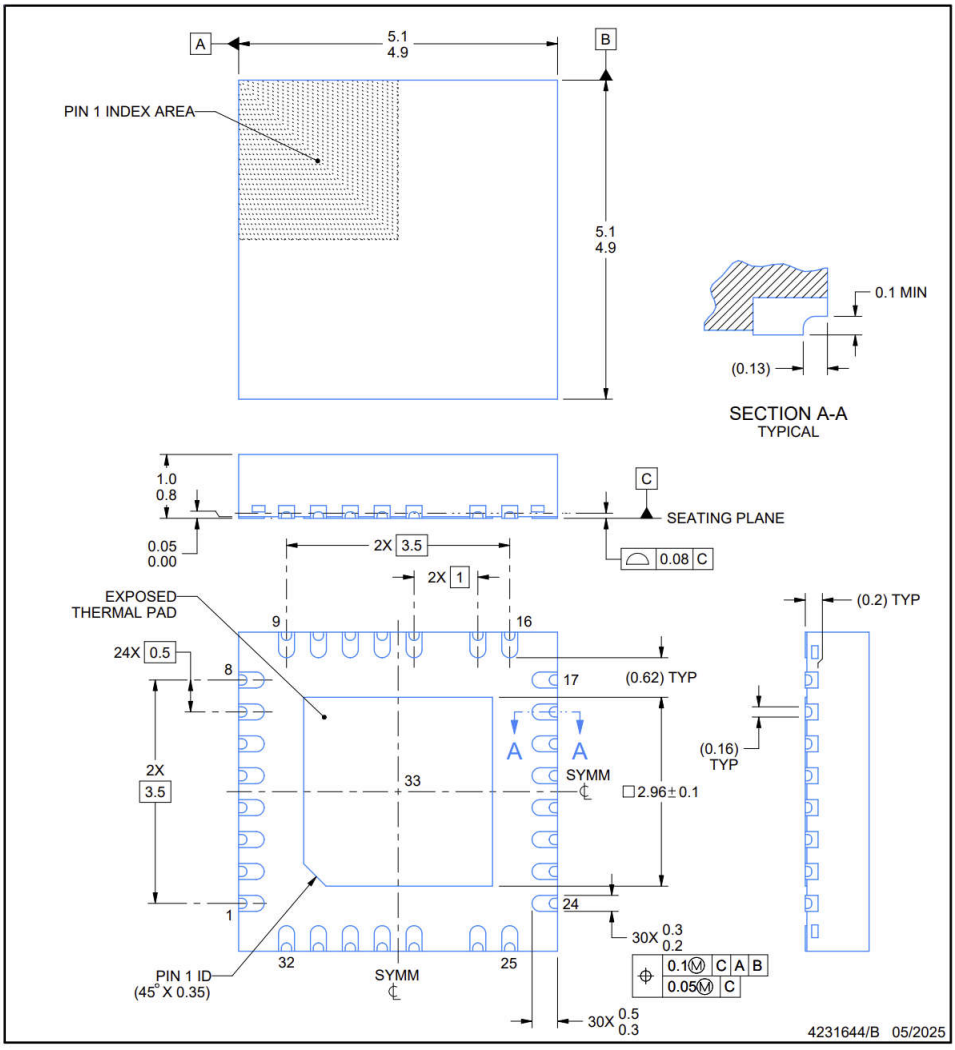
12.2 Mechanical Data

RHB0032AB

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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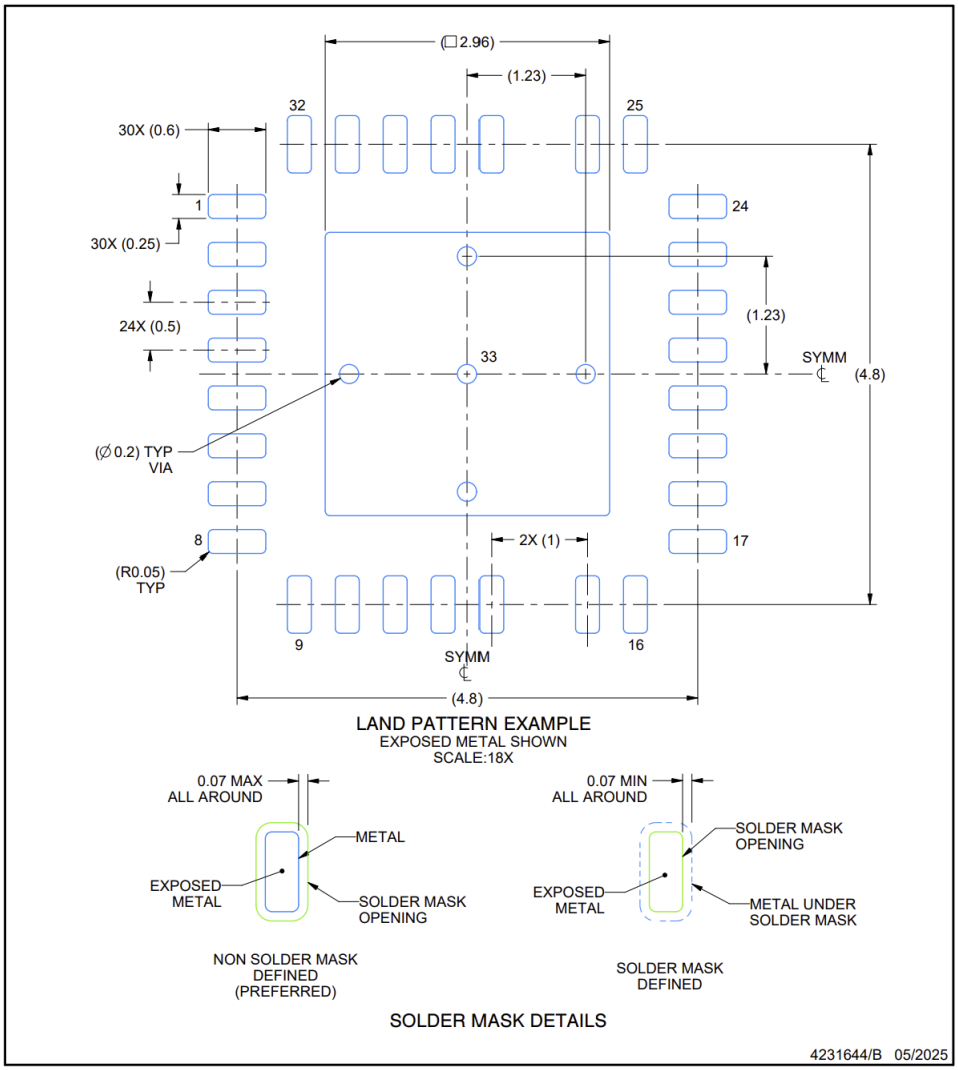
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ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RHB0032AB — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

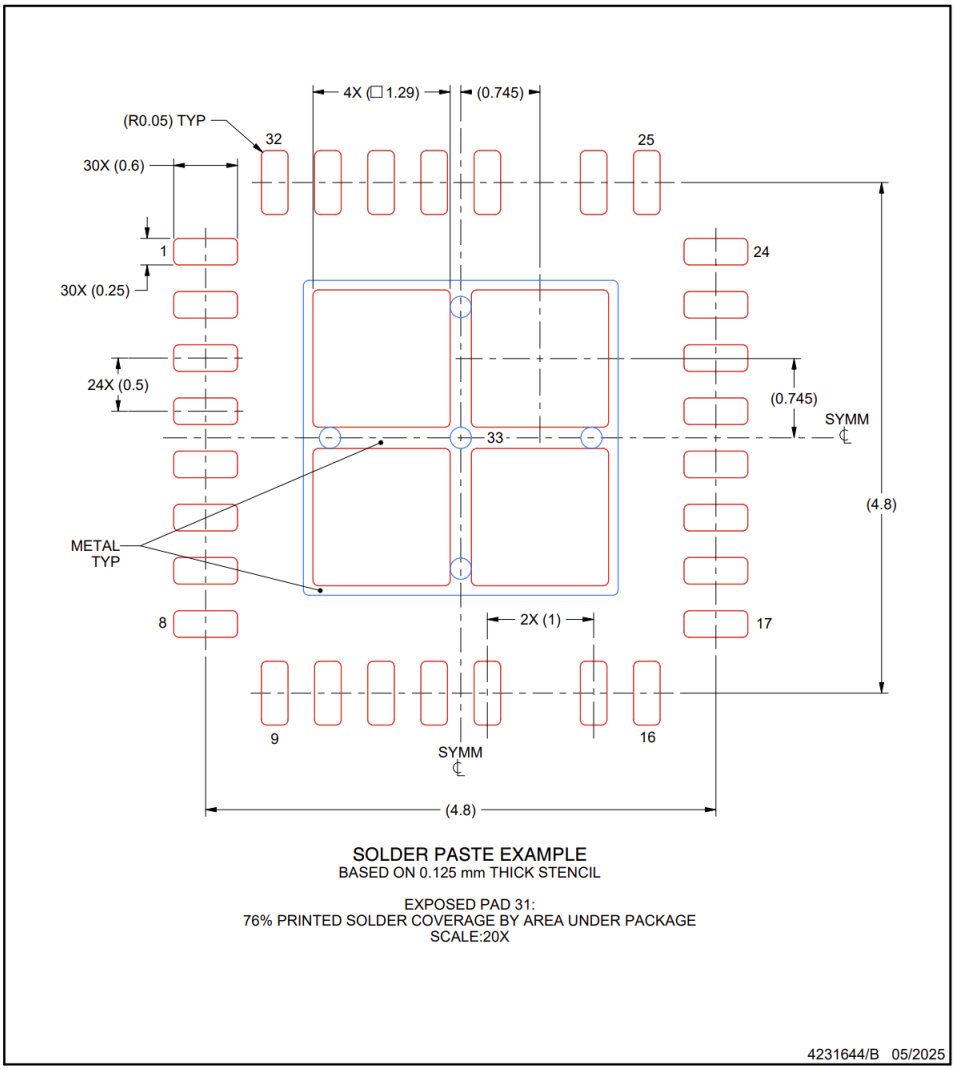
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RHB0032AB — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 31:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4231644/B 05/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS12S24FQRHBRQ1	Active	Preproduction	VQFN (RHB) | 30	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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