TPS1HTC100-Q1, 83mΩ, 4A Single-Channel Automotive Smart High-Side Switch

1 Features

- Single-channel smart high-side power switch for 24V automotive systems with full diagnostics
- Wide operating voltage range: 6V to 60V
- Low R_{ON}: 83mΩ typical, 180mΩ maximum
- Low standby current: < 0.5µA
- Low quiescent current (Iq): < 2mA
- Improve system-level reliability through adjustable current limiting
  - Current limit: 1A to 5A or 7.3A
- Accurate current sensing: ±5% at 1A
- Protection
  - Overload and short-circuit protection
  - Integrated inductive discharge clamp
  - Undervoltage lockout (UVLO) protection
  - Loss of GND, loss of supply protection
  - Reverse battery protection with external components
- Diagnostics
  - On and off state output open-load and short-to-battery detection
  - Overload and short to ground detection
  - Absolute and relative thermal shutdown detection
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Operating junction temperature: –40 to 125°C
- Input control: 1.8V, 3.3V and 5V logic compatible
- Integrated fault sense voltage scaling for ADC protection
- Qualifications
  - AEC-Q100 qualified for automotive applications
    - Temperature grade 1: –40°C to +125°C, T_A
- 14-pin 5mm × 6.4mm thermally-enhanced HTSSOP package

2 Applications

- General resistive, inductive, and capacitive loads

3 Description

TPS1HTC100-Q1 is a single-channel, smart high-side switch, with integrated NMOS power FET and charge pump, designed to meet the requirements of 24V automotive battery systems. The low R_{ON} (83mΩ) minimizes device power dissipation driving a wide range of output load current up to 4A DC, and the 60V DC operating range improves system robustness.

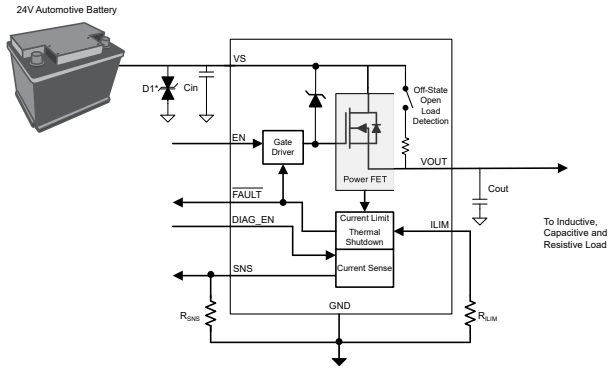
The device integrates protection features such as thermal shutdown, output clamp, and current limit. These features improve system robustness during fault events such as short circuit. TPS1HTC100-Q1 implements an adjustable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The device also provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection enabling better predictive maintenance.

TPS1HTC100-Q1 is available in a small 14-pin, 5mm × 6.4mm HTSSOP leaded package with 0.65mm pin pitch minimizing the PCB footprint.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS1HTC100-Q1	PWP (HTSSOP, 14)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

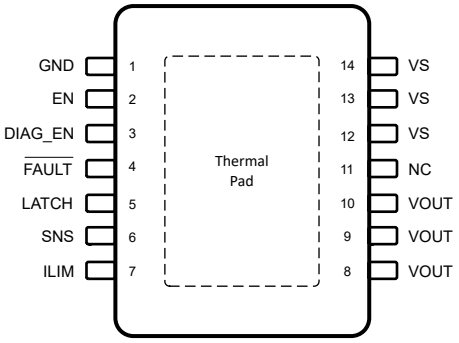


Figure 4-1. PWP Package, 14-Pin HTSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	GND	Power	Ground of device. Connect to resistor- diode ground network to have reverse battery protection.
2	EN	I	Input control for channel activation, internal pulldown.
3	DIAG_EN	I	Enable-disable pin for diagnostics, internal pulldown.
4	$\overline{\text{FAULT}}$	O	Open drain global fault output. Referred to $\overline{\text{FLT}}$, or fault pin.
5	LATCH	I	Thermal shutdown behavior, latch off or auto retry, internal pull down.
6	SNS	O	Output corresponding sense value based on sense ratio.
7	ILIM	O	Adjustable current limit. Short to ground or leave floating if external current limit is not used.
11	NC	N/A	No internal connection.
8, 9, 10	VOUT	Power	Output of high side switch, connected to load.
12, 13, 14	VS	Power	Power supply.
Thermal Pad	Pad	—	Thermal pad, internally shorted to ground.

(1) I = input, O = output, N/A = not applicable

4.1 Recommended Connections for Unused Pins

TPS1HTC100-Q1 is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins can be considered as optional.

Table 4-2. Connections for Optional Pins

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SNS	Ground through 1kΩ resistor	Analog sense is not available.
LATCH	Float or ground through R_{PROT} resistor	With LATCH unused, the device performs an auto-retry after a fault. If latched behavior is desired, but the system describes limited I/O, it is possible to use one microcontroller output to control the latch function of several high-side channels.
ILIM	Float	If the ILIM pin is left floating, the device is set to the default internal current-limit threshold. This is considered a fault state for the device.
$\overline{\text{FAULT}}$	Float	If the $\overline{\text{FAULT}}$ pin is unused, the system cannot read faults from the output.
DIAG_EN	Float or ground through R_{PROT} resistor	With DIAG_EN unused, the analog sense, open-load, and short-to-battery diagnostics are not available.

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Continuous supply voltage, V_S with respect to IC GND		-0.7	70	V
Continuous output voltage, V_{OUT} with respect to IC GND		-60	70	V
Maximum transient (< 100 us) voltage at the supply pin, V_S with respect to IC GND		-0.7	81	V
Enable pin voltage, V_{EN}		–1	7	V
LATCH pin voltage, V_{LATCH}		–1	7	V
DIAG_EN pin voltage, V_{DIAG_EN}		–1	7	V
Sense pin voltage, V_{SNS}		–1	7	V
$\overline{FAULT}$ pin voltage, $V_{\overline{FAULT}}$		–1	7	V
Reverse ground current, I_{GND}	V_S < 0V		–50	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except VS and VOUT	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	VS and VOUT with respect to GND	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	All pins	±750	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
$V_{S_OP_NOM}$	Nominal supply voltage	6.0	60	V
V_{EN}	Enable voltage	–1	5.5	V
V_{LATCH}	LATCH pin voltage, V_{LATCH}	–1	5.5	V
V_{DIAG_EN}	Diagnostic Enable voltage	–1	5.5	V
V_{FAULT}	$\overline{FAULT}$ pin voltage	–1	5.5	V
V_{SNS}	Sense voltage	–1	5.5	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND

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5.4 Thermal Information

THERMAL METRIC(1)(2)		TPS1HTC100-Q1 PWP (HTSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.7	°C/W

(1) For more information about traditional and new thermal metrics, see the SPRA953 application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

5.5 Electrical Characteristics

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VS SUPPLY VOLTAGE AND CURRENT							
IL_{NOM}	Continuous load current	V_{EN} = 0V	T_{AMB} = 85°C		4		A
$I_{Q, VS}$	V_S quiescent current	V_{EN} = 5V, I_{OUT} = 0A	V_{DIAG_EN} = 0V		0.98	1.3	mA
			V_{DIAG_EN} = 5V		1.2	1.65	mA
$I_{STBY, VS}$	Total device standby current (including MOSFET)	V_{EN} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_J = –40°C to 85°C		0.25	0.7	µA
			T_J = 150°C		0.83	11	µA
$I_{OUT(STBY)}$	Output leakage current	V_{EN} = 0V, V_{OUT} = 0V, V_{DIAG} = 0V	T_J = -40°C to 85°C			0.65	µA
			T_J = 150°C		0.28	10	µA
t_{STBY}	Standby mode delay time	V_{EN} = V_{DIAG_EN} = 0V to standby			20		ms
VS UNDERVOLTAGE LOCKOUT (UVLO) INPUT							
$V_{S,UVLOR}$	V_S undervoltage lockout rising	Measured with respect to the GND pin of the device		5.0	5.4	5.75	V
$V_{S,UVLOF}$	V_S undervoltage lockout falling			4.1	4.5	4.85	V
VDS CLAMP							
$V_{DS,Clamp}$	V_{DS} clamp voltage	FET current = 10mA	V_S = 24V	70	78.9	84.5	V
			V_S = 6V	48	53	58	V
RON CHARACTERISTICS							
R_{ON}	On-resistance	0.5A ≤ I_{OUT} ≤ 3A	T_J = 25°C		83		mΩ
			T_J = 125°C			168	mΩ
			T_J = 150°C			180	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	0.5A ≤ I_{OUT} ≤ 3A, V_S = –24V	T_J = –40°C to 150°C			180	mΩ
CURRENT LIMIT CHARACTERISTICS							
K_{CL}	Current Limit Ratio		$I_{CL, typ}$ = 0.92A		46		A × kΩ
K_{CL}	Current Limit Ratio		$I_{CL, typ}$ = 1.96A		48.9		A × kΩ
K_{CL}	Current Limit Ratio		$I_{CL, typ}$ = 3.0A		50.1		A × kΩ
K_{CL}	Current Limit Ratio		$I_{CL, typ}$ = 5.3A		53.2		A × kΩ

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5.5 Electrical Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CL}	Current Limit level	Short circuit condition, V_{DS} = 1V	R_{ILIM} = 50kΩ	0.73	0.92	1.11	A
			R_{ILIM} = 25kΩ	1.5	1.96	2.3	A
			R_{ILIM} = 16.7kΩ	2.3	3.0	3.5	A
			R_{ILIM} = 10kΩ	4	5.3	6.3	A
			R_{ILIM} = Open or Out of range	3.05	3.5	4.3	A
			R_{ILIM} = GND	6.1	7.3	8.6	A
I_{CL_LINPK}	Overcurrent Limit Threshold(1)	Overload condition	R_{ILIM} = 25kΩ			1.5 × I_{CL}	A
I_{ILIM_ENPS}	Peak current enabling into permanent short		R_{ILIM} = 10kΩ			1.2 × I_{CL}	A
t_{IOS}	Short circuit response time	VS = 24V			0.5		µs
THERMAL SHUTDOWN CHARACTERISTICS							
T_{ABS}	Thermal shutdown				165		°C
T_{REL}	Relative thermal shutdown				60		°C
t_{RETRY}	Retry time (2)	Time from fault shutdown until switch re-enable (thermal shutdown).			2		ms
Fault Response	Fault reponse to Thermal Shutdown				Configurable via Latch pin		
T_{HYS}	Absolute Thermal shutdown hysteresis				10		°C
FAULT PIN CHARACTERISTICS							
V_{FAULT}	$\overline{FAULT}$ low output voltage	$I_{\overline{FAULT}}$ = 2.5mA				0.5	V
t_{FAULT_FLT}	Fault indication-time	Time between fault and $\overline{FAULT}$ asserting				75	µs
t_{FAULT_SNS}	Fault indication-time	V_{DIAG_EN} = 5V Time between fault and I_{SNS} settling at V_{SNSFH}				106	µs
CURRENT SENSE CHARACTERISTICS							
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}	I_{OUT} = 1A			800		A/A

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5.5 Electrical Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SNS}	Current sense current	V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 4A		5		mA
				–5		6	%
			I_{OUT} = 3A		3.75		mA
				–5		5	%
			I_{OUT} = 2A		2.5		mA
				–5		5	%
			I_{OUT} = 1A		1.25		mA
				–5		5	%
			I_{OUT} = 0.5A		0.625		mA
				–6		6	%
			I_{OUT} = 250mA		0.3125		mA
				–10		10	%
			I_{OUT} = 150mA		0.1875		mA
				–10		10	%
			I_{OUT} = 60mA		0.075		mA
				–25		25	%
			I_{OUT} = 30mA		0.0375		mA
				–25		25	%
			I_{OUT} = 25mA		0.03125		mA
				–30		30	%
			I_{OUT} = 10mA		0.011		mA
				–30		30	%
SNS PIN CHARACTERISTICS							
V_{SNSFH}	V_{SNS} fault high-level	V_{DIAG_EN} = 5V		4.5	5	5.77	V
		V_{DIAG_EN} = 3.3V, R_{SNS}=Open		3.3	3.95	4.4	V
		V_{DIAG_EN} = V_{IH}		2.9	3.2	3.5	V
I_{SNSFLT}	I_{SNS} fault high-level	V_{DIAG_EN} > $V_{IH,DIAG_EN}$		5.2	6.4		mA
$I_{SNSleak}$	I_{SNS} leakage	V_{DIAG_EN} = 5V, IL = 0mA				1.3	µA
V_{S_ISNS}	V_S for full current sense and fault functionality	V_{DIAG_EN} = 3.3V		5.9			V
		V_{DIAG_EN} = 5V		7.1			V
OPEN LOAD DETECTION CHARACTERISTICS							
V_{OL_OFF}	OFF state open-load (OL) detection voltage	V_{EN} = 0V, V_{DIAG_EN} = 5V		1.4	2	2.6	V
R_{OL_OFF}	OFF state open-load (OL) detection internal pull-up resistor	V_{EN} = 0V, V_{DIAG_EN} = 5V	V_S = 6V	110	133	150	kΩ
			V_S = 24V	114	140	166	kΩ
			V_S = 48V	120	140	166	kΩ
t_{OL_OFF}	OFF state open-load (OL) detection deglitch time	V_{EN} = 0V, V_{DIAG_EN} = 5V, When Vs – V_{OUT} < V_{OL}, duration longer than t_{OL}. Open load detected.			480	1050	µs
$t_{OL_OFF_1}$	OL_OFF and STB indication-time from EN falling	V_{EN} = 5V to 0V, V_{DIAG_EN} = 5V I_{OUT} = 0mA, V_{OUT} = Vs - V_{OL}			310	905	µs
$t_{OL_OFF_2}$	OL and STB indication-time from DIA_EN rising	V_{EN} = 0V, V_{DIAG_EN} = 0V to 5V I_{OUT} = 0mA, V_{OUT} = V_S - V_{OL}				1080	µs
DIAG_EN PIN CHARACTERISTICS							
$V_{IL,\ DIAG_EN}$	Input voltage low-level	No GND Network				0.8	V

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5.5 Electrical Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH, DIAG_EN}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, DIAG_EN}$	Input voltage hysteresis			270		mV
R_{DIAG_EN}	Internal pulldown resistor		200	350	500	kΩ
$I_{IL, DIAG_EN}$	Input current low-level	V_{DIAG_EN} = 0.8V, V_{EN}=0V		0.8		µA
$I_{IH, DIAG_EN}$	Input current high-level	V_{DIAG_EN} = 5V		14		µA
EN PIN CHARACTERISTICS						
$V_{IL, EN}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, EN}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, EN}$	Input voltage hysteresis			300		mV
R_{EN}	Internal pulldown resistor		200	350	500	kΩ
$I_{IL, EN}$	Input current low-level	V_{EN} = 0.8V		2.2		µA
$I_{IH, EN}$	Input current high-level	V_{EN} = 5V		14		µA
LATCH PIN CHARACTERISTICS						
$V_{IL, LATCH}$	Input voltage low-level	No GND Network			0.8	V
$V_{IH, LATCH}$	Input voltage high-level	No GND Network	1.5			V
$V_{IHYS, LATCH}$	Input voltage hysteresis			270		mV
R_{LATCH}	Internal pulldown resistor		0.7	1	1.3	MΩ
$I_{IL, LATCH}$	Input current low-level	V_{LATCH} = 0.8V		0.77		µA
$I_{IH, LATCH}$	Input current high-level	V_{LATCH} = 5V		5		µA

(1) The maximum current output under overload condition before current limit regulation.
(2) Data not tested in production.

5.6 SNS Timing Characteristics

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted), parameters not tested in production

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIAG_EN 50% of V_{DIAG_EN} to 90% of settled ISNS	V_{EN}= 5V, V_{DIAG_EN} = 0V to 5V, R_{SNS} = 1kΩ, I_L = 1A			15	µs
		V_{EN} = 5V, V_{DIAG_EN} = 0V to 5V, R_{SNS} = 1kΩ, I_L = 50mA			80	µs
$t_{SNSION2}$	Settling time from rising edge of EN and DIAG_EN 50% of V_{DIAG_EN} V_{EN} to 90% of settled ISNS	V_{EN} = V_{DIAG_EN} = 0V to 5V V_S = 24V R_{SNS} = 1kΩ, I_L = 1A			200	µs
$t_{SNSION3}$	Settling time from rising edge of EN 50% of V_{EN} to 90% of settled ISNS	V_{EN} = 0V to 5V, V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_L = 1A			200	µs
$t_{SNSIOFF}$	Settling time from falling edge of DIAG_EN	V_{EN} = 5V, V_{DIAG_EN} = 5V to 0V R_{SNS} = 1kΩ, R_L = 48Ω			20	µs
$t_{SETTLEH}$	Settling time from rising edge of load step.	V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 0.5A to 3A			20	µs
$t_{SETTLEL}$	Settling time from falling edge of load step.	V_{EN} = V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 3A to 0.5A			20	µs

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5.6 SNS Timing Characteristics (continued)

V_S = 6V to 60V, T_A = –40°C to 125°C (unless otherwise noted), parameters not tested in production

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SNSFH}	Assertion time for SNSFH From 50% rising edge of VSNSFH to 50% of falling edge of VSNSFH	V_{DIAG_EN} = V_{EN} = 0V to 5V R_{SNS} = 1kΩ, I_{OUT} = 5mA C_{OUT} =15µF	60			µs

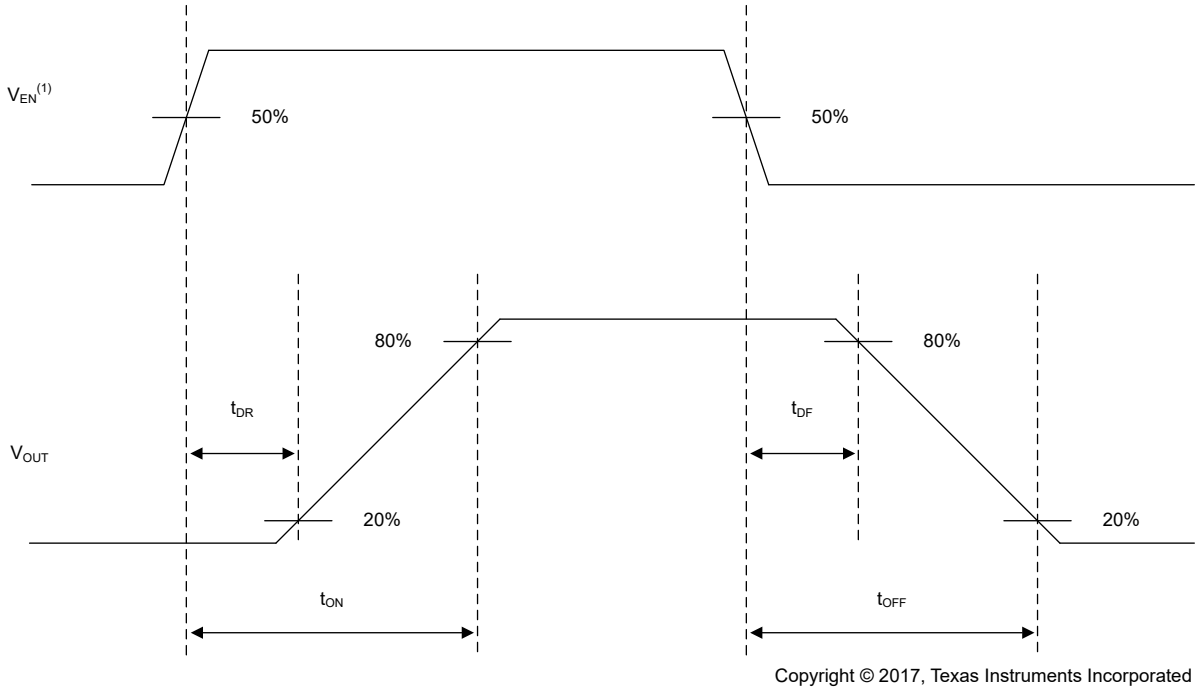
5.7 Switching Characteristics

V_S = 48V, R_L = 120Ω, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Turn-on delay time (from standby)	50% of EN to 20% of VOUT	28	55	70	µs
	Turn-on delay time (from active, diagnostic, or standby delay)		20	47	65	µs
t_{DF}	Turn-off delay time	50% of EN to 80% of VOUT	20	65	98	µs
SR_R	VOUT rising slew rate	20% to 80% of V_{OUT}	0.1	0.47	0.7	V/µs
SR_F	VOUT falling slew rate	80% to 20% of V_{OUT}	0.1	0.56	0.82	V/µs
t_{ON}	Turn-on time (from standby)	50% of EN to 80% of VOUT		120	200	µs
t_{OFF}	Turnoff time	50% of EN to 20% of VOUT		117	200	µs
t_{ON} - t_{OFF}	Turn-on and off matching	1ms ON time switch enable pulse	–25		70	µs
t_{ON_pw}	Minimum VOUT ON pulse width	200µs ON time switch enable pulse, VOUT @90% of VS, F = f_{max}	60		134	µs
t_{OFF_pw}	Minimum VOUT OFF pulse width	200µs OFF time switch enable pulse, VOUT @20% of VS, F = f_{max}	82	130	175	µs
Δ_{PWM}	PWM accuracy - average load current	200µs enable pulse, F = f_{max}	–15		15	%

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5.8 Timing Diagrams

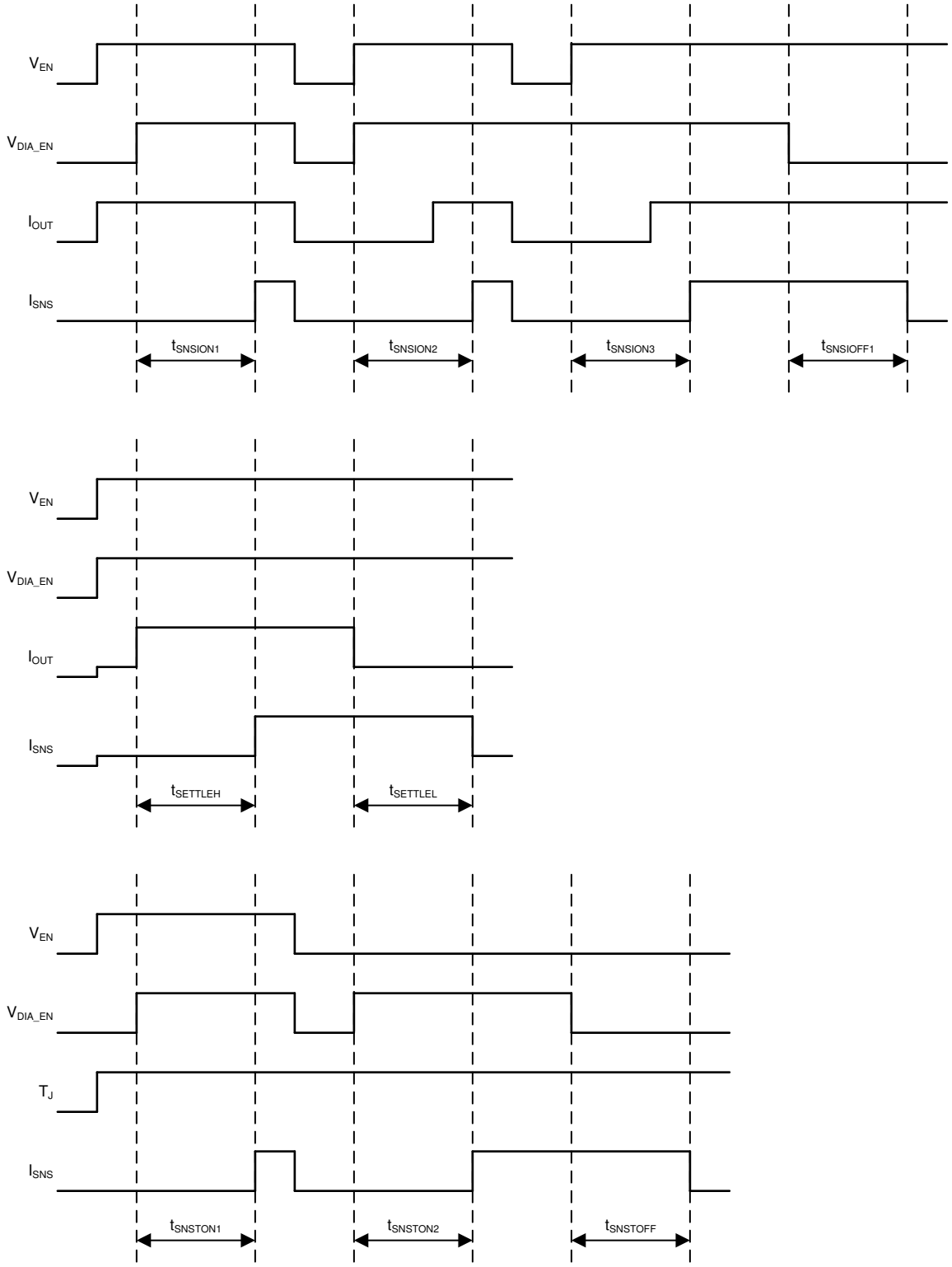


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Rise and fall time of V_{EN} is 100ns.

Figure 5-1. Switching Characteristics Definitions

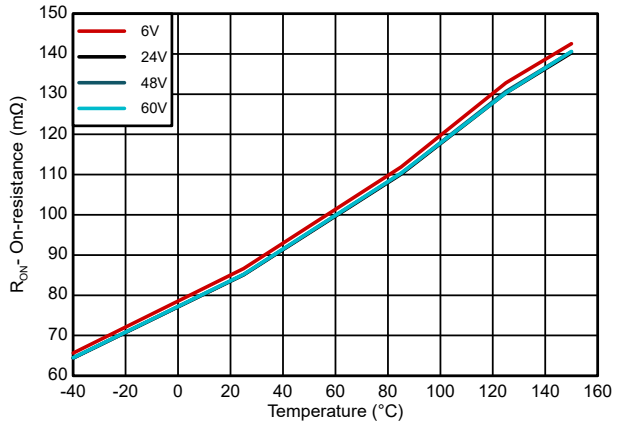
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Rise and fall times of control signals are 100ns. Control signals include: EN, DIA_EN.

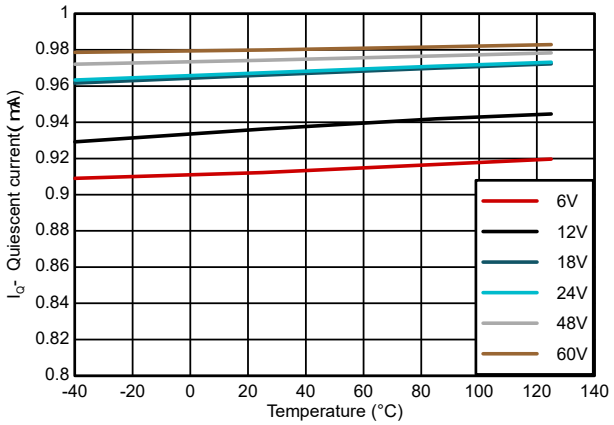
Figure 5-2. SNS Timing Characteristics Definitions

5.9 Typical Characteristics



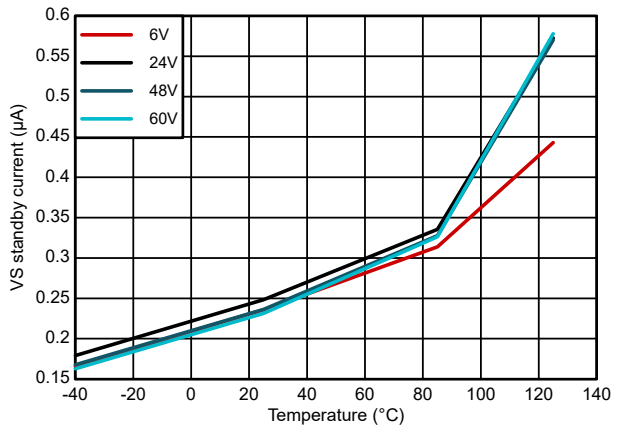
I_{OUT} = 0.9A

Figure 5-3. On-Resistance (R_{ON}) vs Temperature vs VS Supply Voltage



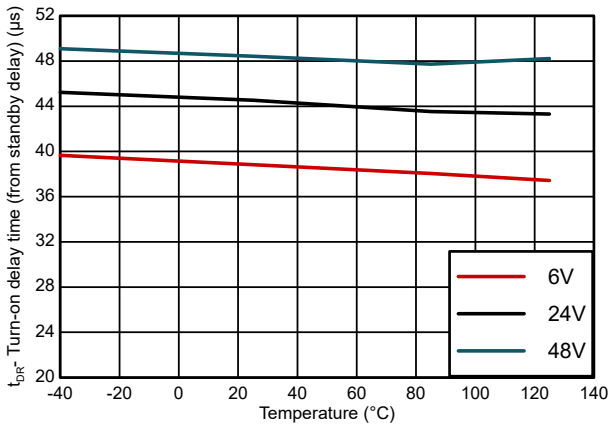
V_{EN} = 5V V_{DIAG_EN} = 0V

Figure 5-4. Quiescent Current ($I_{Q,\ VS}$) From VS Input Supply vs Temperature vs VS Voltage



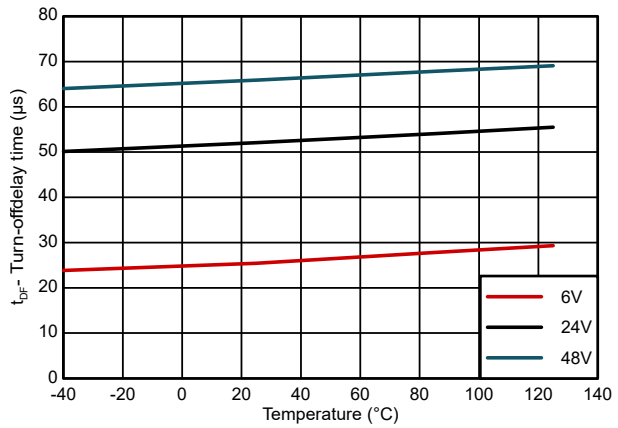
V_{EN} = 0V V_{DIAG_EN} = 0V

Figure 5-5. Standby Current ($I_{STBY,\ VS}$) From VS Input Supply vs Temperature vs VS Voltage



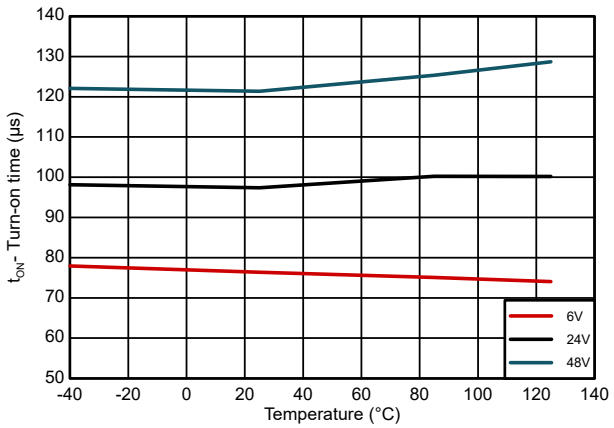
R_L= 120Ω

Figure 5-6. Turn-on Delay Time (t_{DR}) vs Temperature vs VS Voltage



R_L= 120Ω

Figure 5-7. Turn-off Delay Time (t_{DF}) vs Temperature vs VS Voltage

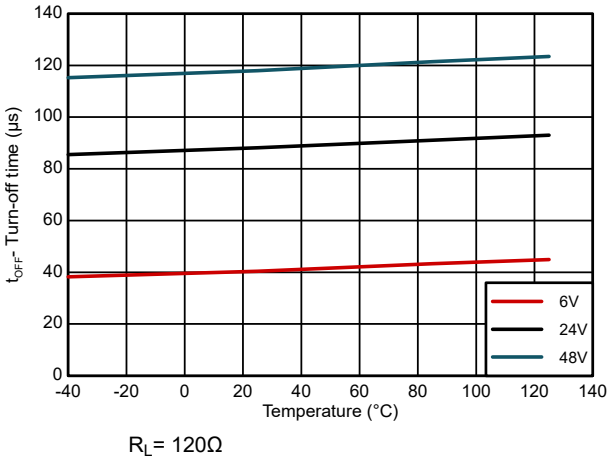


R_L= 120Ω

Figure 5-8. Turn-on Time (t_{ON}) vs Temperature vs VS Voltage

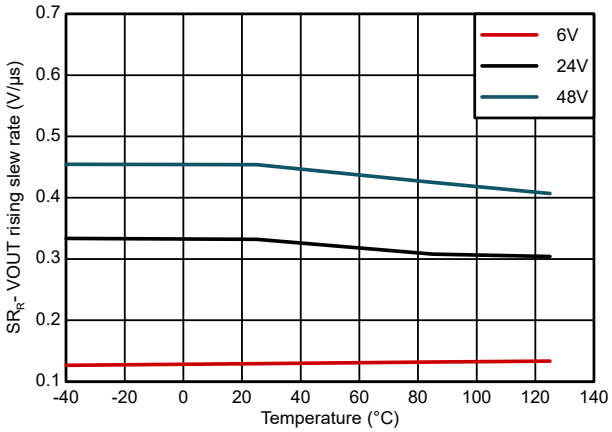
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5.9 Typical Characteristics (continued)



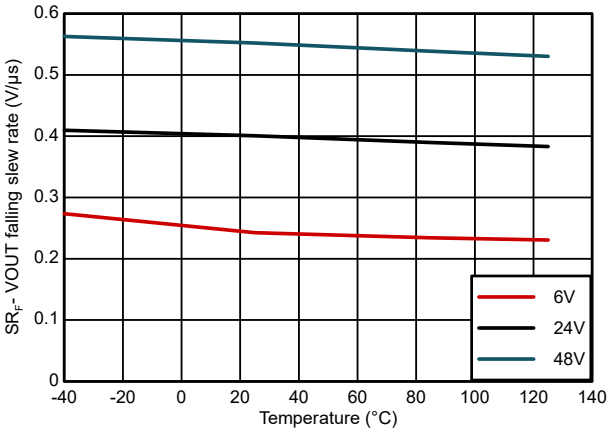
R_L= 120Ω

Figure 5-9. Turn-off Time (t_{OFF}) vs Temperature vs VS Voltage



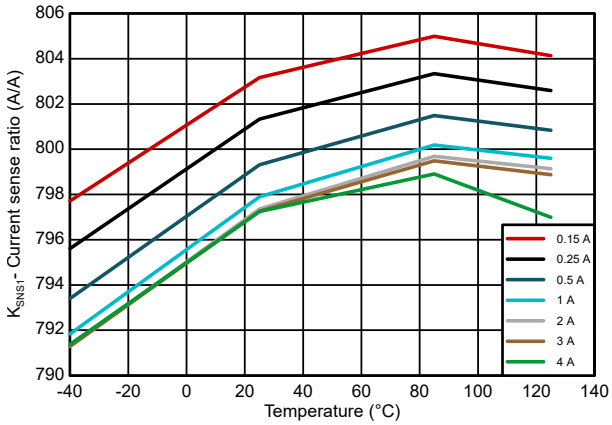
R_L= 120Ω

Figure 5-10. VOUT Rising Slew Rate (SR_R) vs Temperature vs VS Voltage



R_L= 120Ω

Figure 5-11. VOUT Falling Slew Rate (SR_F) vs Temperature vs VS Voltage



VS = 24V

Figure 5-12. Current Sense Ratio (K_{SNS}) vs Temperature vs Load Current

6 Parameter Measurement Information

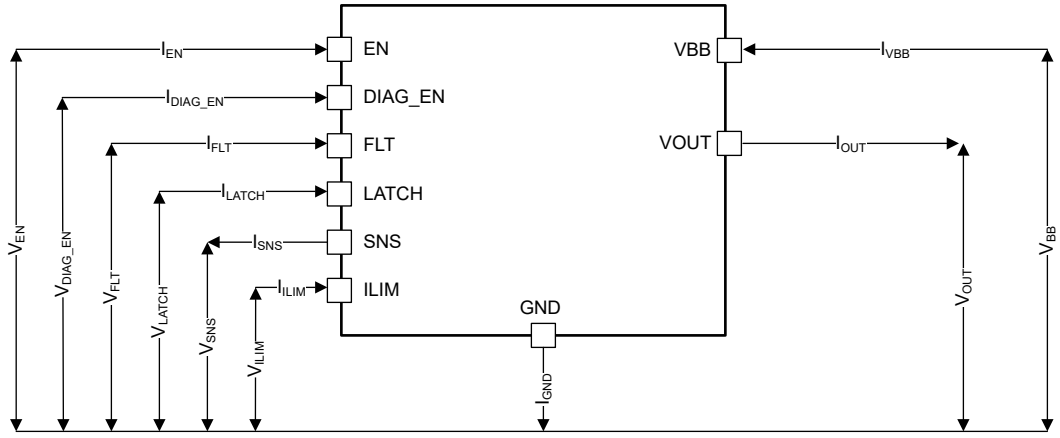


Figure 6-1. Parameter Definitions

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7 Detailed Description

7.1 Overview

The TPS1HTC100-Q1 is a automotive, single-channel, fully-protected, high-side power switch with an integrated NMOS power FET and charge pump rated to 60V DC tolerance. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. Low logic high threshold, V_{IH}, of 1.5V on the input pins allow use of MCUs down to 1.8V. A programmable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two pins to support both digital status and analog current-sense output, for multiplexing the MCU analog or digital interface among devices.

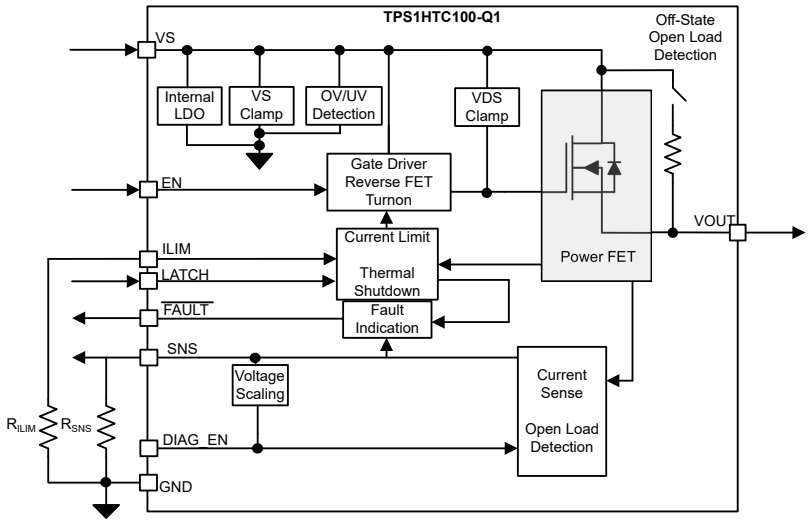
The digital status report is implemented with an open-drain structure on the fault pin. When a fault condition occurs, the pin is pulled down to GND. An external pullup is required to match the microcontroller supply level. High-accuracy current sensing allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, which is reflected as voltage on the SNS pin. K_{SNS} is a constant value across temperature and supply voltage. The SNS pin can also report a fault by forcing a voltage equal to I_{SNSFLT} × R_{SNS} clamped to a maximum of V_{SNSFH} that scales with the diagnostic enable voltage so that the maximum voltage seen by the system ADC is within an acceptable value. This removes the need for an external Zener diode or resistor divider on the SNS pin.

The external high-accuracy current limit allows setting the current limit value by application. The external high-accuracy current limit highly improves the reliability of the system by clamping the inrush current effectively under start-up or short-circuit conditions. Also, the external high-accuracy current limit can save system costs by reducing PCB trace, connector size, and the preceding power-stage capacity. An internal current limit can also be implemented in this device. The lower value of the external or internal current-limit value is applied.

An active drain to source voltage clamp is built in to address switching off the energy of inductive loads, such as relays, solenoids, pumps, motors, and so forth. During the inductive switching-off cycle, both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch. With the benefits of process technology and excellent IC layout, the TPS1HTC100-Q1 device can achieve excellent energy dissipation capacity, which can help save the need of using external free-wheeling circuitry in most cases.

The TPS1HTC100-Q1 device can be used as a high-side power switch for a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, and heaters.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Accurate Current Sense

The high-accuracy current-sense function is internally implemented, which allows real-time monitoring and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

K_{SNS} is the ratio of the output current and the sense current. The accuracy values of K_{SNS} quoted in the electrical characteristics do take into consideration temperature and supply voltage. Each device is internally calibrated while in production, so post-calibration by users is not required in most cases.

The maximum voltage out on the SNS pin is clamped to V_{SNSFH}, which is the fault voltage level. To make sure that this voltage is not higher than the system can tolerate, TI has correlated the voltage coming in on the DIAG_EN pin with the maximum voltage out on the SNS pin. If DIAG_EN is between V_{IH} and 3.3V, the maximum output on the SNS pin is approximately 3.3V. However, if the voltage at DIAG_EN is above 3.3V, then the fault SNS voltage, V_{SNSFH}, tracks that voltage up to 5V. Tracking is done because the GPIO voltage output that is powering the diagnostics through DIAG_EN is close to the maximum acceptable ADC voltage within the same microcontroller. Therefore, the sense resistor value, R_{SNS}, can be selected to maximize the range of currents needed to be measured by the system. The R_{SNS} value must be selected based on application need. The minimum R_{SNS} value is usually bounded by the ADC minimum acceptable voltage, $V_{ADC,min}$, for the smallest load current needed to be measured by the system, $I_{LOAD,min}$. The maximum R_{SNS} value is selected to establish the V_{SNS} voltage is below the V_{SNSFH} value so that the system can determine faults. This difference between the maximum readable current through the SNS pin, $I_{LOAD,max} \times R_{SNS}$, and the V_{SNSFH} is called the headroom voltage, V_{HR}. The headroom voltage is determined by the system but is important so that there is a difference between the maximum readable current and a fault condition. Therefore, the maximum R_{SNS} value can be the V_{SNSFH} minus the V_{HR} times the sense current ratio, K_{SNS} divided by the maximum load current the system must measure, $I_{LOAD,max}$. In most cases the following boundary equation can be used to determine the R_{SNS} value.

$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \leq R_{SNS} \leq (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (1)$$

In some applications, where there is a higher load current range the above boundary equation can only satsify either the lower or upper bound. In these cases, more emphasis can be put on the lower measurable current values which increases R_{SNS}. Likewise, if the higher currents are of more interest the R_{SNS} can be decreased.

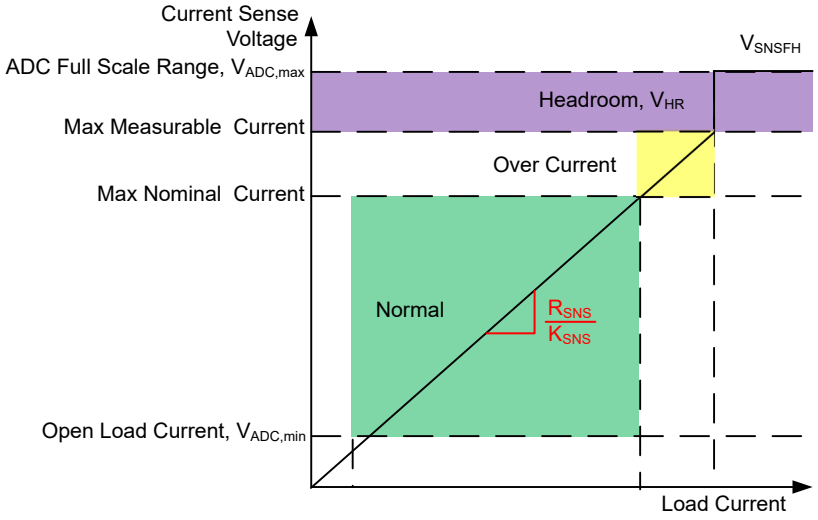


Figure 7-1. Voltage Indication on the Current-Sense Pin

The maximum current the system wants to read, $I_{LOAD,max}$, must be below the current-limit threshold because after the current-limit threshold is tripped the V_{SNS} value goes to V_{SNSFH}. Additionally, currents being measured

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can be up to the maximum ILIM value but the current sense output accuracy is not specified above the maximum rated value in the Current Sense Characteristics.

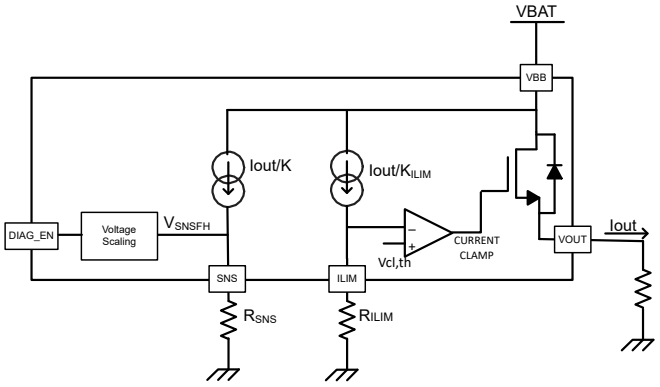


Figure 7-2. Current-Sense and Current-Limit Block Diagram

Because this scheme adapts based on the voltage coming in from the MCU, there is no need to have a Zener diode on the SNS pin to protect from high voltages.

7.3.2 Programmable Current Limit

A high-accuracy current limit allows higher reliability, which protects the power supply during short circuit or power up. Also, a high-accuracy current limit can save system costs by reducing PCB traces, connector size, and the capacity of the preceding power stage.

Current limit offers protection from over-stressing to the load and integrated power FET. Current limit holds the current at the set value, and pulls up the SNS pin to V_{SNSFH} and asserts the $\overline{FAULT}$ pin as diagnostic reports. The three current-limit thresholds are:

- External programmable current limit -- An external resistor, R_{ILIM} is used to set the channel current limit. When the current through the device exceeds I_{LIM_REG} (current limit threshold), a closed loop steps in immediately. V_{GS} voltage regulates accordingly, leading to the V_{DS} voltage regulation. When the closed loop is set up, the current is clamped at the set value. The external programmable current limit provides the capability to set the current-limit value by application.

  Additionally this value can be dynamically changed by changing the resistance on the ILIM pin. This can be seen in the Applications Section.
- Internal current limit: I_{LIM} pin shorted to ground -- If the external current limit is out of range on the lower end or the I_{LIM} pin is shorted to ground, the internal current limit is fixed. To use the internal current limit for large-current applications, tie the I_{LIM} pin directly to the device GND.
- Internal current limit: I_{LIM_REG} pin open -- If the external resistor is out of range on the higher end or the ILIM pin is open, the current limit reverts to half the nominal current limit range. This level is still above the nominal operation for the device to operate in DC steady state but is low enough that if a pin fault occurs and the R_{ILIM} opens up, the current does not default to the highest rating and put additional stress on the power supply.

Both the internal current limit ($I_{lim,nom}$) and external programmable current limit are always active when V_S is powered and EN is high. The lower value one (of I_{LIM} and the external programmable current limit) is applied as the actual current limit. The typical deglitch time for the current limit to assert is 2.5µs.

Note that if a GND network is used (which leads to the level shift between the device GND and board GND), the ILIM pin must connect with device GND. Calculate R_{LIM} with Equation 2.

$$R_{LIM_REG} = K_{CL} / I_{LIM_REG} \quad (2)$$

For better protection from a hard short-to-GND condition (when V_S and input are high and a short to GND occurs suddenly), an open-loop fast-response behavior is set to turn off the channel, before the current-limit closed loop is set up. With this fast response, the device can achieve better inrush-suppression performance.

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For more information about the current limiting feature, see *Section 7.3.4.1*.

7.3.2.1 Capacitive Charging

Figure 7-3 shows the typical setup for a capacitive load application and the internal blocks that function when the device is used. Note that all capacitive loads have an associated "load" in parallel with the capacitor that is described as a resistive load but in reality it can be inductive or resistive.

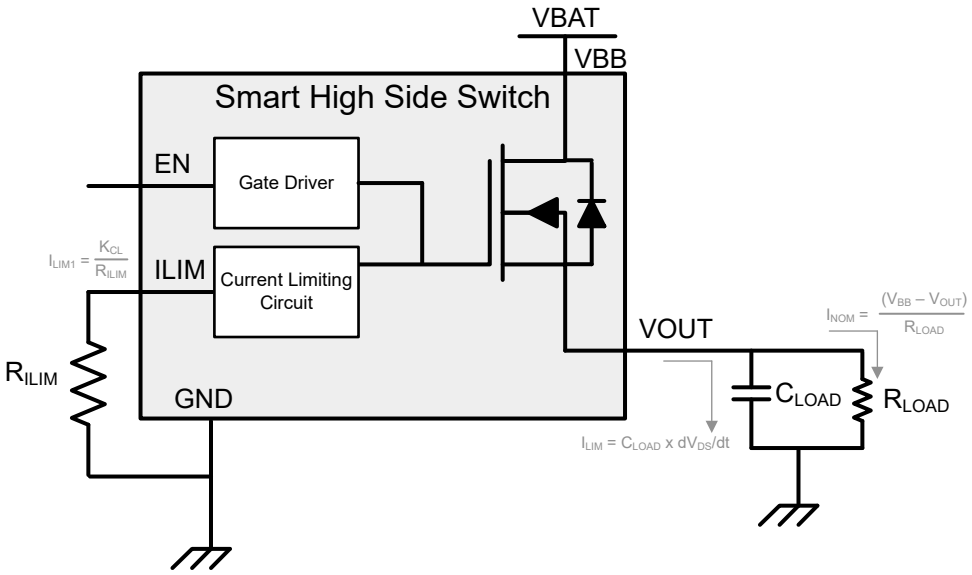


Figure 7-3. Capacitive Charging Circuit

The first thing to check is that the nominal DC current, I_{NOM}, is acceptable for the TPS1HTC100-Q1 device. This can easily be done by taking the $R_{\theta JA}$ from Section 5.4 and multiplying the R_{ON} of the TPS1HTC100-Q1 and the I_{NOM} with it, add the ambient temperature and if that value is below the thermal shutdown value, then the device can operate with that load current. For an example of this calculation see the Section 8.2.

The second key care about for this application is to make sure that the capacitive load can be charged up completely without the device hitting thermal shutdown. This is because if the device hits thermal shutdown during the charging, the resistive nature of the load in parallel with the capacitor starts to discharge the capacitor over the duration the TPS1HTC100-Q1 is off. Note that there are some applications with high enough load impedance that the TPS1HTC100-Q1 hitting thermal shutdown and trying again is acceptable; however, for most applications the system must be designed so that the TPS1HTC100-Q1 does not hit thermal shutdown while charging the capacitor.

With the current clamping feature of the TPS1HTC100-Q1, capacitors can be charged up at a lower inrush current than other high current limit switches. This lower inrush current means that the capacitor takes a little longer to charge all the way up.

For more information about capacitive charging with high side switches, see the *How to Drive Resistive, Inductive, Capacitive, and Lighting Loads* application note. This application note has information about the thermal modeling available along with quick ways to estimate if a high side switch can charge a capacitor to a given voltage.

7.3.3 Inductive-Load Switching-Off Clamp

When an inductive load is switching off, the output voltage is pulled down to negative, due to the inductance characteristics. The power FET can break down if the voltage is not clamped during the current decay period. To protect the power FET in this situation, an internal drain to gate clamp, namely the $V_{DS,clamp}$ is used to clamp the voltage between the drain and source of the device.

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$$V_{DS,clamp} = V_{BAT} - V_{OUT} \quad (3)$$

During the current-decay period (T_{DECAY}), the power FET is turned on for inductive energy dissipation. Both the energy of the power supply (E_{BAT}) and the load (E_{LOAD}) are dissipated on the high-side power switch itself, which is called E_{HSD}. If resistance is in series with inductance, some of the load energy is dissipated in the resistance.

$$E_{HSD} = E_{BAT} + E_{LOAD} = E_{BAT} + E_L - E_R \quad (4)$$

From the high-side power switch view, E_{HSD} equals the integration value during the current decay period.

$$E_{HSD} = \int_0^{T_{DECAY}} V_{DS,clamp} \times I_{OUT}(t)\,dt \quad (5)$$

$$T_{DECAY} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right) \quad (6)$$

$$E_{HSD} = L \times \frac{V_{BAT} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(MAX)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(MAX)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (7)$$

When R approximately equals 0, E_{HSD} can be given simply as:

$$E_{HSD} = \frac{1}{2} \times L \times I^2_{OUT(MAX)} \frac{V_{BAT} + |V_{OUT}|}{R^2} \quad (8)$$

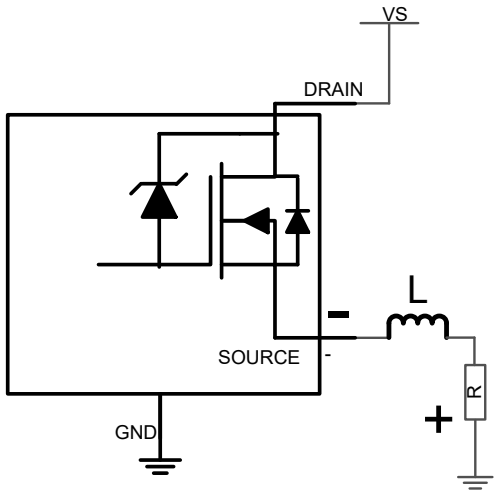


Figure 7-4. Driving Inductive Load

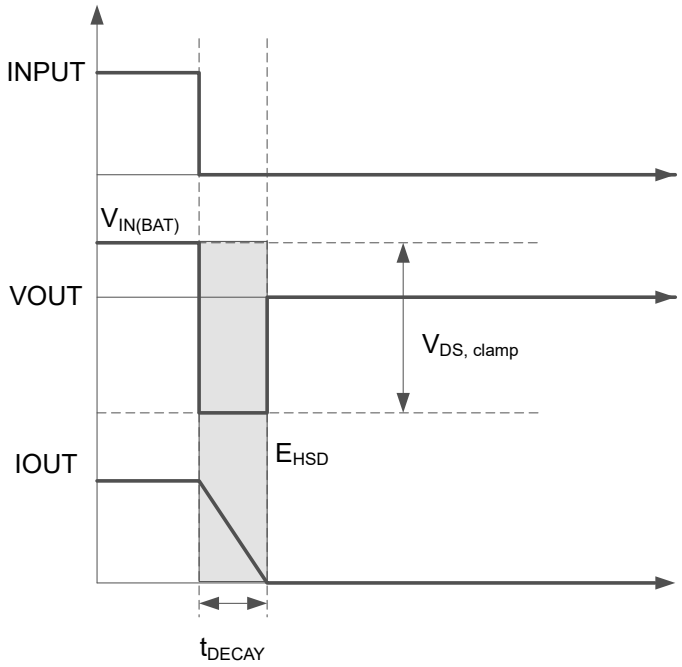


Figure 7-5. Inductive-Load Switching-Off Diagram

As discussed previously, when switching off, battery energy and load energy are dissipated on the high-side power switch, which leads to the large thermal variation. For each high-side power switch, the upper limit of the maximum safe power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

7.3.4 Full Protections and Diagnostics

Current Sensing is active when DIAG_EN enabled. When DIAG_EN is low, current sense is disabled. The SNS output is in high-impedance mode.

Table 7-1. DIAG_EN Logic Table

DIAG_EN	EN CONDITION	PROTECTIONS AND DIAGNOSTICS
HIGH	HIGH	See Fault Table
	LOW	
LOW	HIGH	Diagnostics disabled, $\overline{\text{FAULT}}$ and SNS output set to high impedance. Protection is normal.
	LOW	

Table 7-2. DIAG_EN=HIGH Status Table

CONDITIONS	EN	VOUT	$\overline{\text{FAULT}}$	SNS	BEHAVIOR	RECOVERY
Normal	L	L	Hi-Z	0	Normal	
	H	H	Hi-Z	I_{Load} / K_{SNS}	Normal	
Overcurrent	H	V_S - I_{LIM} × R_{LOAD}	L	V_{SNSFH}	Holds the current at the current limit until thermal shutdown	
STG, Relative Thermal Shutdown, Absolute Thermal Shutdown	H	H→L	L	V_{SNSFH}	Shuts down when devices hits relative or absolute thermal shutdown	Auto retries when T_{HYS} is met and time has been longer than t_{RETRY} amount of time

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Table 7-2. DIAG_EN=HIGH Status Table (continued)

CONDITIONS	EN	VOUT	$\overline{\text{FAULT}}$	SNS	BEHAVIOR	RECOVERY
Open load	H	H	Hi-Z	I_{Load} / K_{SNS} = approximately 0	Normal behavior, user can judge if it is an open load or not	
	L	H	L	V_{SNSFH}	Internal pullup resistor is active. If $V_S - V_{OUT} < V_{OL}$ then fault active	Clears when fault goes away
Reverse Polarity	x	x	x	x	Channel turns on to lower power dissipation. Current into ground pin is limited by external ground network	

7.3.4.1 Short-Circuit and Overload Protection

TPS1HTC100-Q1 provides output short-circuit protection to make sure that the device prevents current flow in the event of a low impedance path to GND, removing the risk of damage or significant supply droop. The device is specified to protect against short-circuit events regardless of the state of the ILIM pins and with up to 60V supply at 125°C.

Figure 7-6 shows the behavior of TPS1HTC100-Q1 when a short-circuit occurs and the device is in the on-state and already outputting current. When the internal pass FET is fully enabled, the current clamping settling time is slower so to make sure overshoot is limited, the device implements a fast trip level at a level I_{OVCR}. When this fast trip threshold is hit, the device immediately shuts off for a short period of time before quickly re-enabling and clamping the current to I_{CL} level after a brief transient overshoot to the higher peak current (I_{CL_ENPS}) level. The device then keeps the current clamped at the regulation current limit until the thermal shutdown temperature is hit and the device safely shuts off.

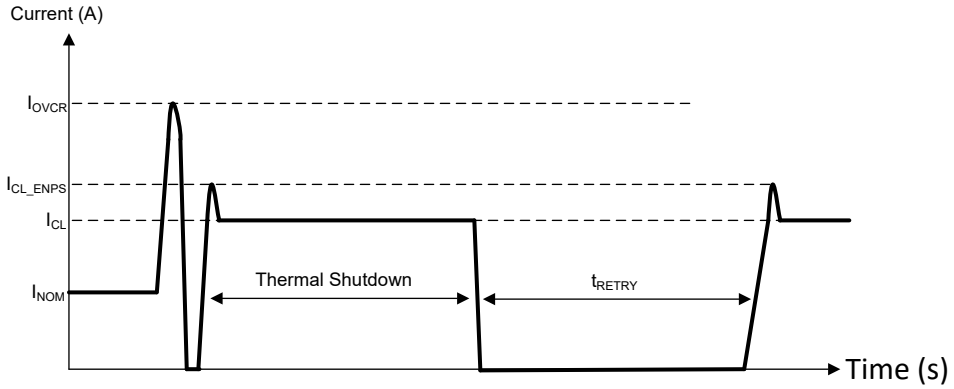


Figure 7-6. On-State Short-Circuit Behavior

Overload Behavior shows the behavior of the TPS1HTC100-Q1 when there is a small change in impedance that sends the load current above the I_{CL} threshold. The current rises to I_{CL_LINPK} above the regulation level. Then the current limit regulation loop kicks in and the current drops to the I_{CL} value.

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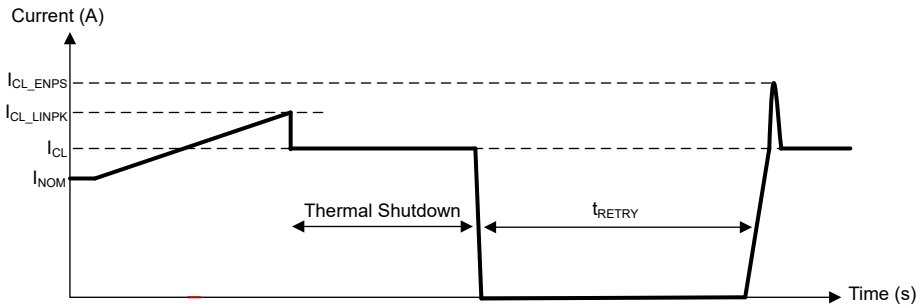


Figure 7-7. Overload Behavior

In all of these cases, the internal thermal shutdown is safe to hit repetitively. There is no device risk or lifetime reliability concerns from repeatedly hitting this thermal shutdown level.

7.3.4.2 Open-Load Detection

When the main channel is enabled faults are diagnosed by reading the voltage on the SNS pin and judged by the user.

In the off state, if a load is connected, the output voltage is pulled to 0V. In the case of an open load, the output voltage is close to the supply voltage, $V_S - V_{OUT} < V_{ol,off}$. The FLT pin goes low to indicate the fault to the MCU, and the SNS pin is pulled up to V_{SNSFH}. There is always a leakage current $I_{ol,off}$ present on the output, due to the internal logic control path or external humidity, corrosion, and so forth. Thus, TI implemented an internal pullup resistor to offset the leakage current. This pullup current must be less than the output load current to avoid false detection in the normal operation mode. To reduce the standby current, TI implemented a switch in series with the pullup resistor controlled by the DIAG_EN pin. The pull up resistor value is R_{pu} = 150kΩ.

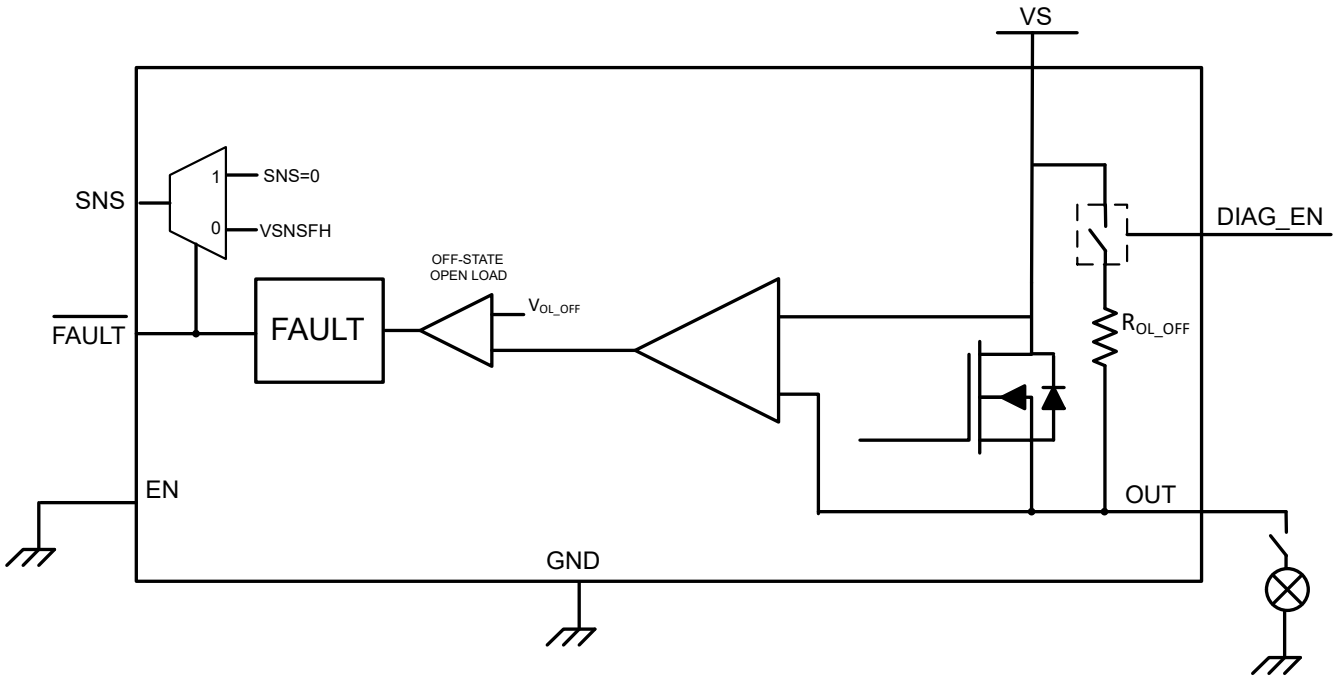


Figure 7-8. Open-Load Detection Circuit

7.3.4.3 Thermal Protection Behavior

The thermal protection behavior can be split up into three categories of events that can happen. Figure 7-9 shows each of these categories.

1. **Relative thermal shutdown**: The device is enabled into an overcurrent event. The DIAG_EN pin is high so that diagnostics can be monitored on SNS and FLT (however, DIAG_EN being high is not necessary for all

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protection features to function). The output current rises up to the I_{ILIM} level and the FLT goes low while the SNS goes to V_{SNSFH}. With this large amount of current going through, the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises T_{REL} amount above the controller junction temperature $\Delta T = T_{FET} - T_{CON} > T_{REL}$, the device shuts down. The faults are continually shown on SNS and FLT and the part waits for the t_{RETRY} timer to expire. When t_{RETRY} timer expires, because the LATCH pin is low and EN is still high, the device comes back on into this I_{ILIM} condition.

2. **Absolute thermal shutdown**: The device is still enabled in an overcurrent event with DIAG_EN high and LATCH still low. However, in this case the junction temperature rises up and hits an absolute reference temperature, T_{ABS}, and then shuts down. The device does not recover until both $T_J < T_{ABS} - T_{hys}$ and the t_{RETRY} timer has expired.
3. **Latch-off mode**: The device is enabled into an overcurrent event. The DIAG_EN pin is high so that diagnostics can be monitored on SNS and FLT. The output current rises up to the I_{ILIM} level and the FLT goes low while the SNS goes to V_{SNSFH}. If the part shuts down due to a thermal fault, either relative thermal shutdown or absolute thermal shutdown, the device does not enable the channel until either the LATCH pin OR the EN pin is toggled.

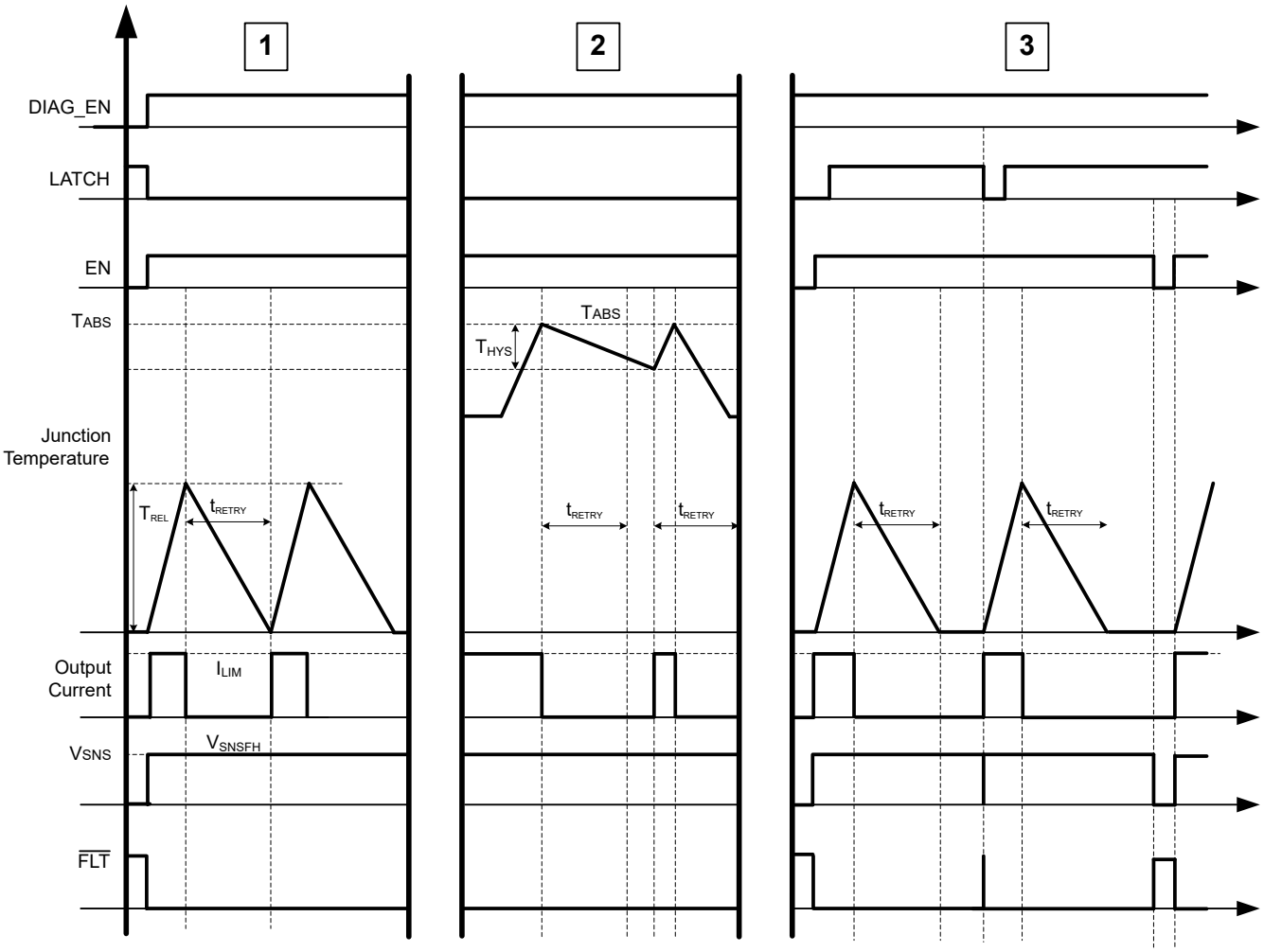


Figure 7-9. Thermal Behavior

7.3.4.4 UVLO Protection

The device monitors the supply voltage V_S to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{UVLOF}, the output stage is shut down automatically. When

the supply rises up to V_{UVLOR}, the device turns on. If an overcurrent event trips the UVLO threshold, the device shuts off and comes back on into a current limit normally.

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7.3.4.5 Reverse Polarity Protection

Method 1: Blocking diode connected with V_S. Both the device and load are protected when in reverse polarity.

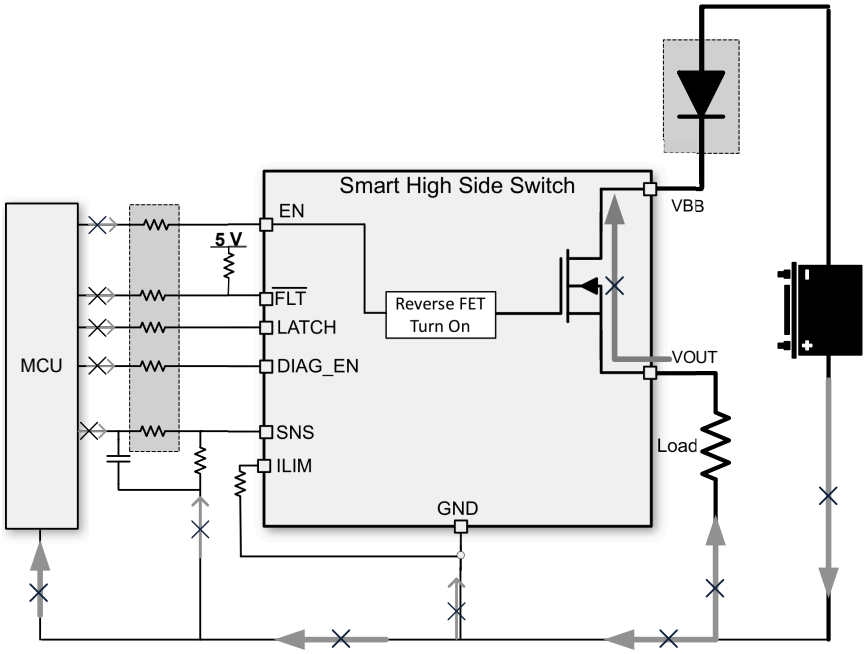


Figure 7-10. Reverse Protection With Blocking Diode

Method 2 (GND network protection): Only the high-side device is protected under this connection. The load reverse loop is limited by the load. Note when reverse polarity occurs, the continuous reverse current through the power FET must be less than I_{rev}. Of the three types of ground pin networks, TI strongly recommends type three (the resistor and diode in parallel). No matter what types of connection are between the device GND and the board GND, if a GND voltage shift occurs, make sure the following proper connections for the normal operation:

- TI recommends to leave floating.
- Connect the current limit programmable resistor to the device GND.

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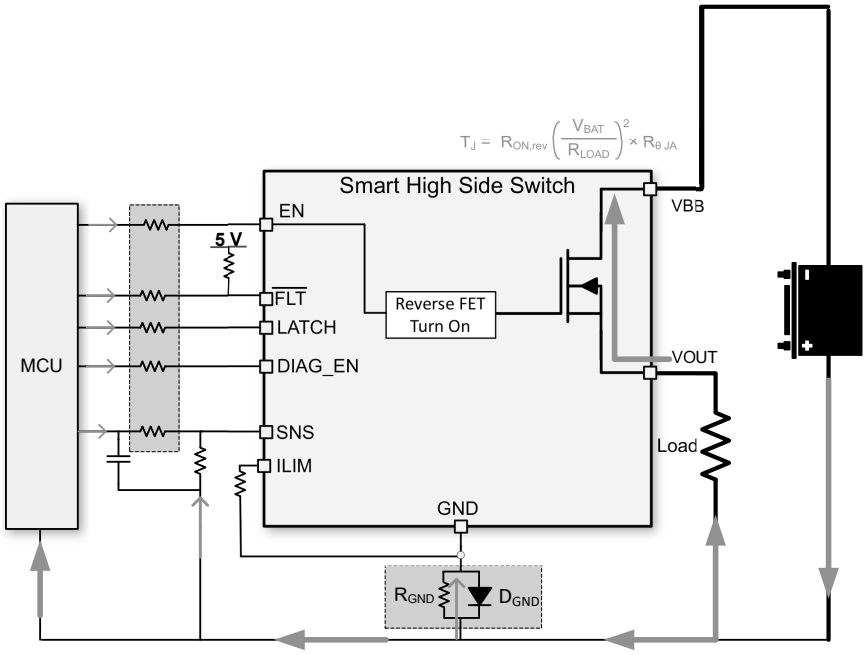


Figure 7-11. Reverse Protection With GND Network

- **Type 1 (resistor):** The higher resistor value contributes to a better current limit effect during the reverse battery event or negative ISO pulses. However, the higher resistor leads to higher GND shift during normal operation mode. Also, consider the resistor power dissipation.

$$R_{GND} \leq \frac{V_{GNDshift}}{I_{nom}} \quad (9)$$

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \quad (10)$$

  where

  - $V_{GNDshift}$ is the maximum value for the GND shift, determined by the HSS and microcontroller. TI suggests a value ≤ 0.6V.
  - I_{nom} is the nominal operating current.
  - $–V_{CC}$ is the maximum reverse voltage seen on the battery line.
  - $–I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in Section 5.1.

  If multiple high-side power switches are used, the resistor can be shared among devices.
- **Type 2 (diode):** A diode is needed to block the reverse voltage, which also brings a ground shift (≈ 600mV). However, an inductive load is not acceptable to avoid an abnormal status when switching off.
- **Type 3 (resistor and diode in parallel (recommended)):** A peak negative spike can occur when the inductive load is switching off, which can damage the HSD or the diode. So, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are 4.7kΩ resistor in parallel with an I_F > 200mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices.

7.3.4.6 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin can damage the MCU I/O pins [more likely, the internal circuitry connected to the pins]. Therefore, the serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10kΩ resistance for the R_{PROT} resistors.

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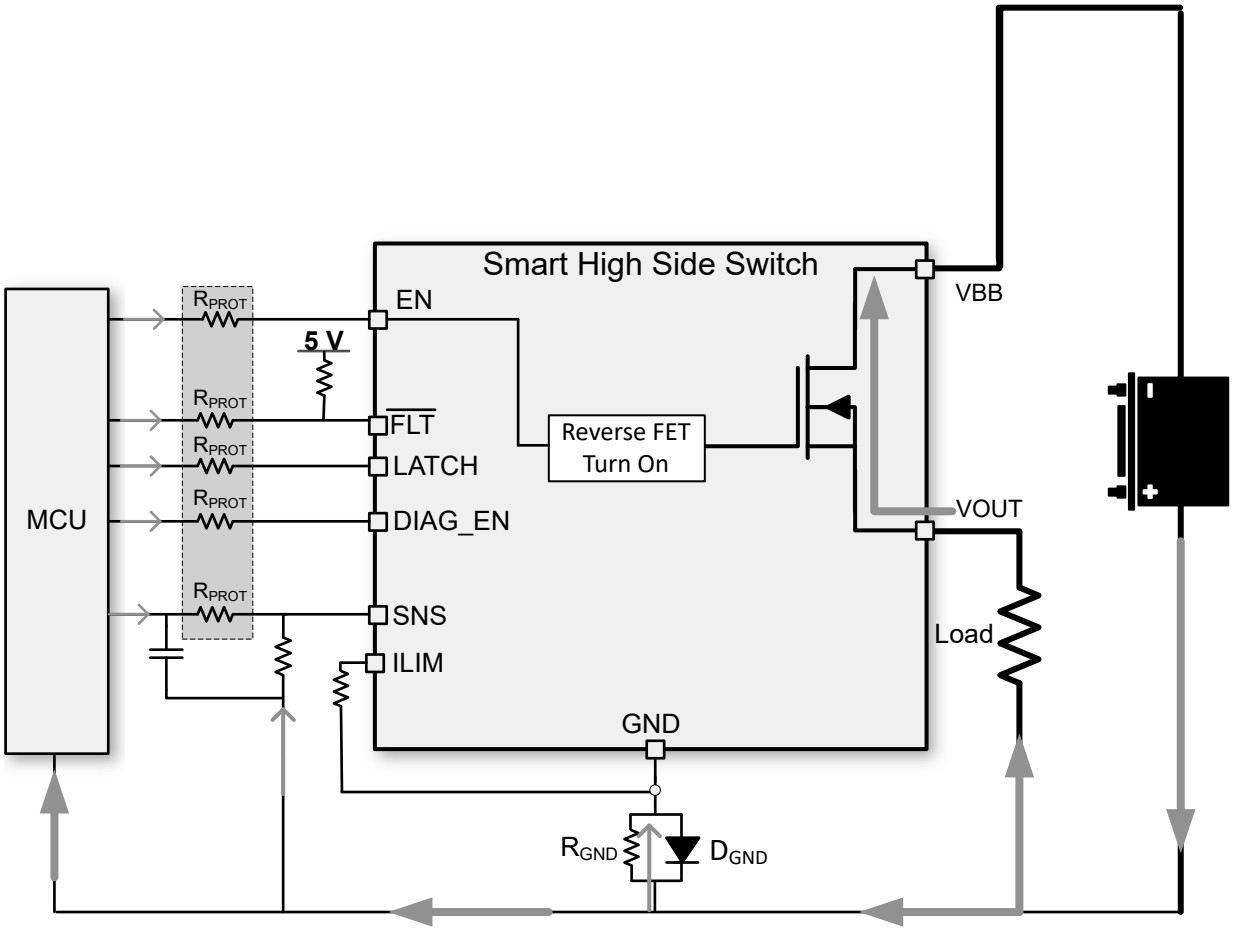


Figure 7-12. MCU IO Protections

7.3.5 Diagnostic Enable Function

The diagnostic enable pin, DIAG_EN, offers multiplexing of the microcontroller diagnostic input for current sense or digital status, by sharing the same sense resistor and ADC line or I/O port among multiple devices.

In addition, during the output-off period, the diagnostic disable function lowers the current consumption for the standby condition. The three working modes in the device are normal mode, standby mode, and standby mode with diagnostic. If off-state power saving is required in the system, the standby current is <500nA with DIAG_EN low. If the off-state diagnostic is required in the system, the typical standby current is around 1mA with DIAG_EN high.

7.4 Device Functional Modes

7.4.1 Device Functional Modes

During typical operation, the TPS1HTC100-Q1 can operate in several states that are described below and shown as a state diagram in Figure 7-13.

OFF - Off state occurs when the device is not powered.

STANDBY - Standby state is a low-power mode used to reduce power consumption to the lowest level. Diagnostic capabilities are not available in standby mode.

STANDBY DELAY - The standby delay state is entered when EN and DIAG_EN are low. After t_{STBY}, if the EN and DIAG_EN pins are still low, the device goes to standby state.

DIAGNOSTIC - Diagnostic state can be used to perform diagnostics while the switch is disabled.

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ACTIVE - In active state, the switch is enabled. The diagnostic functions can be turned on or off during active state.

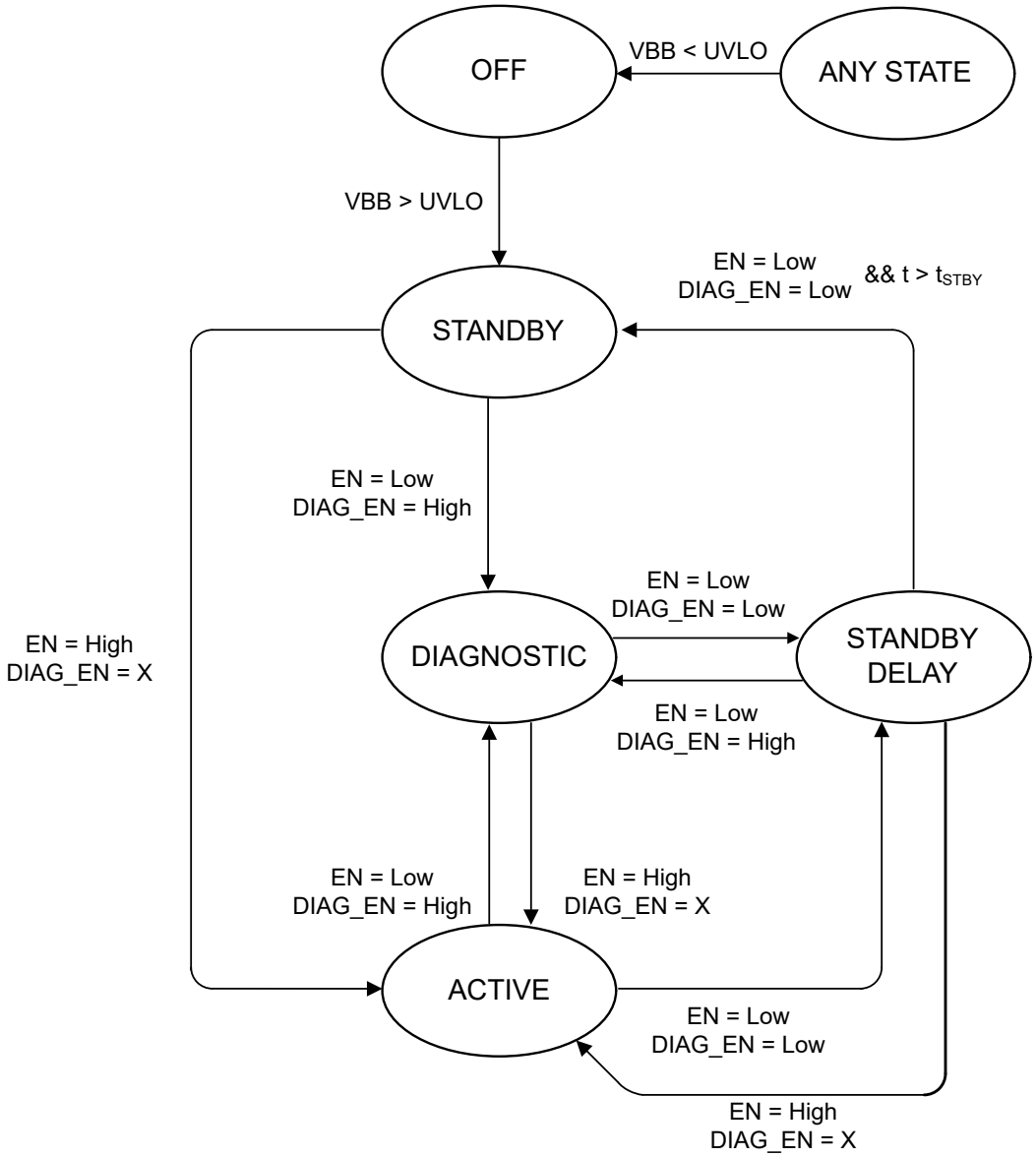


Figure 7-13. State Diagram

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following discussion notes how to implement the device in a typical application with recommended external components.

8.2 Typical Application

Figure 8-1 shows an example of how to design the external circuitry parameters.

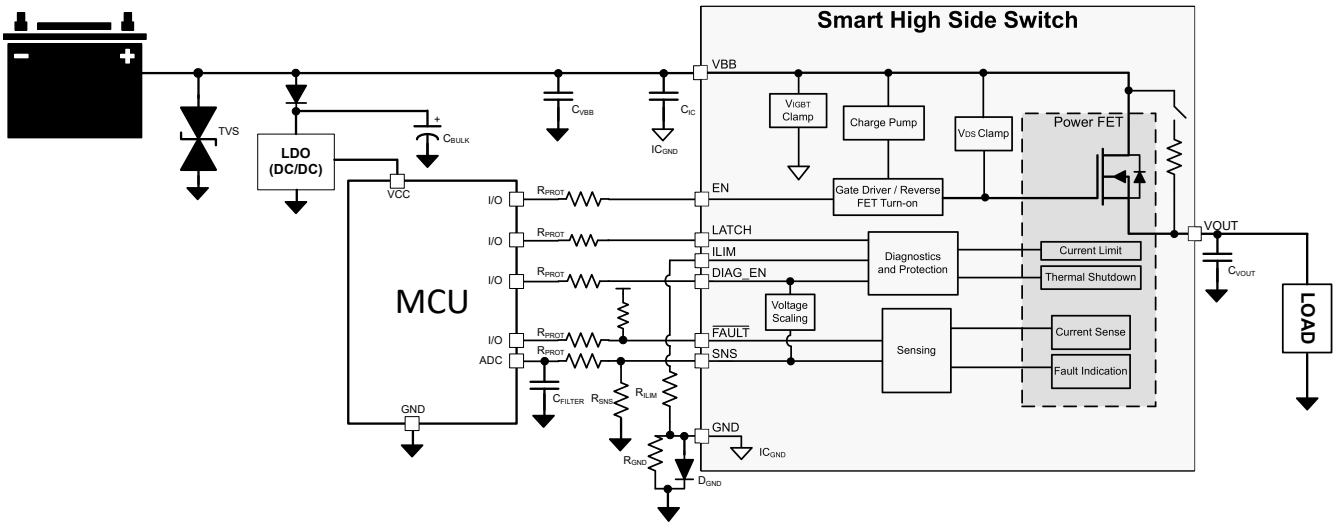


Figure 8-1. Typical Application Circuitry

8.2.1 Design Requirements

COMPONENT	DESCRIPTION	PURPOSE
TVS	SMBJ60CA (optional)	Filter voltage transients coming from battery (ISO7637-2).
C_{VS}	220nF (optional)	Better EMI performance.
C_{IC}	100nF	Minimal amount of capacitance on input for EMI mitigation.
C_{BULK}	10µF (optional)	There to hold the rail for the LDO; however, helps to filter voltage transients on supply rail. Not a requirement.
R_{PROT}	10k	Protection resistor for microcontroller and device I/O pins.
R_{ILIM}	10kΩ–50kΩ	Set current limit threshold.
R_{SNS}	1k	Translate the sense current into sense voltage.
C_{FILTER}	100pF	Coupled with RPROT on the SNS line creates a low-pass filter to filter out noise going into the ADC of the MCU.
C_{VOUT}	22nF	Improves EMI performance, filtering of voltage transients.
R_{GND}	4.7kΩ	Stabilize GND potential during turn-off of inductive load.
D_{GND}	MSX1PJ	Keeps GND close to system ground during normal operation.

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8.2.2 Detailed Design Procedure

To keep maximum voltage on the SNS pin at an acceptable range for the system, use the following equation to calculate the R_{SNS}. To achieve better current sense accuracy. A 1% accuracy or better resistor is preferred.

$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \leq R_{SNS} \leq (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (11)$$

Table 8-1. Typical Application

PARAMETER	VALUE
V_{DIAG_EN}	5V
$I_{LOAD,max}$	4A
$I_{LOAD,min}$	20mA
$V_{ADC,min}$	5mV
V_{HR}	1V

For this application, an RSNS value of approximately 800Ω can be selected to satisfy the equation requirements.

$$5mV \times 800 / 20mA \leq \cong 800\Omega \leq (5V - 1V) \times 800 / 4A \quad (12)$$

In other applications, where there is a higher dynamic current range either more emphasis can be put on the lower end measurable values which increases RSNS. Likewise, if the higher currents are of more interest the RSNS can be decreased.

Having the maximum SNS voltage scale with the DIAG_EN voltage removes the need for a Zener diode on the SNS pin going to the ADC.

To set the programmable current limit value at 5A, use the following equation to calculate the R_{LIM}.

$$R_{LIM} = K_{CL} / I_{LIM} = 50 / 5 = 10k\Omega \quad (13)$$

TI recommends R_{PROT} = 10kΩ to establish the current going into the digital pins (EN, DIAG_EN, LATCH) is limited.

TI recommends a 4.7kΩ resistor and 600V, 0.2A diode for the GND network.

8.2.2.1 Dynamically Changing Current Limit

The current limit threshold can be changed dynamically by altering the resistance going from the current limit pin to the ground of the device unpremeditatedly. This alteration allows the system to have a different current limit for start-up, when there can be significant inrush current, and during normal operation. The way this is commonly done is by putting two resistors in parallel on the ILIM pin and having a switch to enable or disable one of the resistors. This set-up can be seen in Figure 8-2. Alternatively, a digital potentiometer can be used to adjust the impedance on the ILIM pin unpremeditatedly. Take care so that the capacitance on the ILIM pin is below approximately 100pF to keep the current regulation loop stable. The most common application where this feature is useful is capacitive loads.

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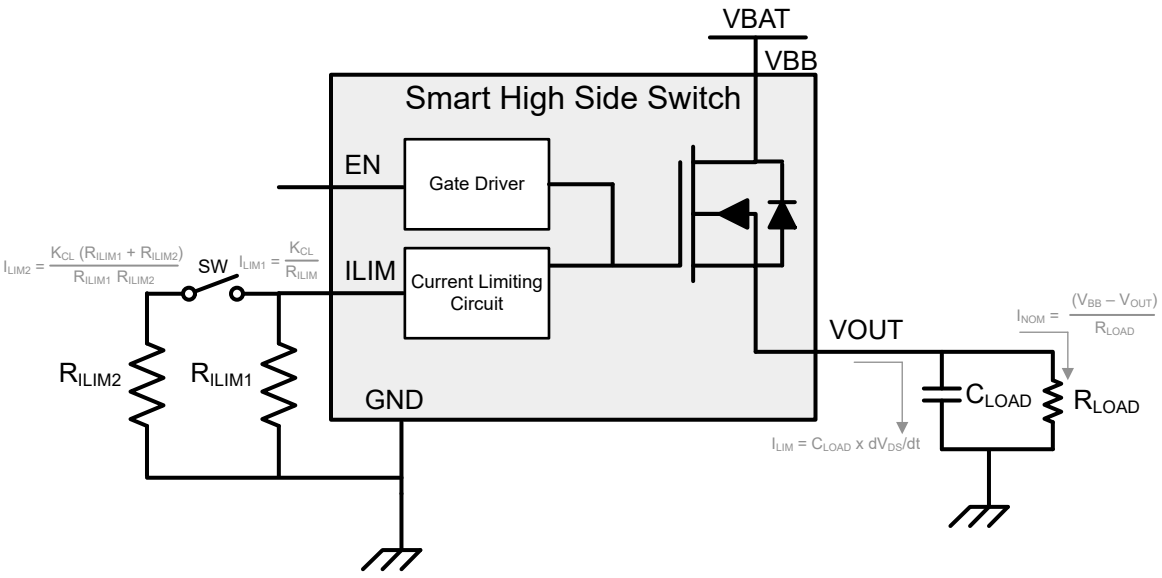


Figure 8-2. Dynamic Changing Current Limit Setup

In a capacitive charging case, the initial current to charge the capacitor is the inrush current. Depending on the system requirements, dynamically changing the current limit can help either charge up a capacitor faster or charge up a larger capacitor. To allow a higher inrush level of current through in the beginning, the switch can be closed making the current limit be according to the equation below.

$$I_{LIM2} = K_{CL}(R_{ILIM1} + R_{ILIM2}) / (R_{ILIM1} \times R_{ILIM2}) \quad (14)$$

When the inrush event is over and the output voltage is charged up, the switch opens and the current limit is just the R_{ILIM1} equivalent level. This timing can be seen in Figure 8-3.

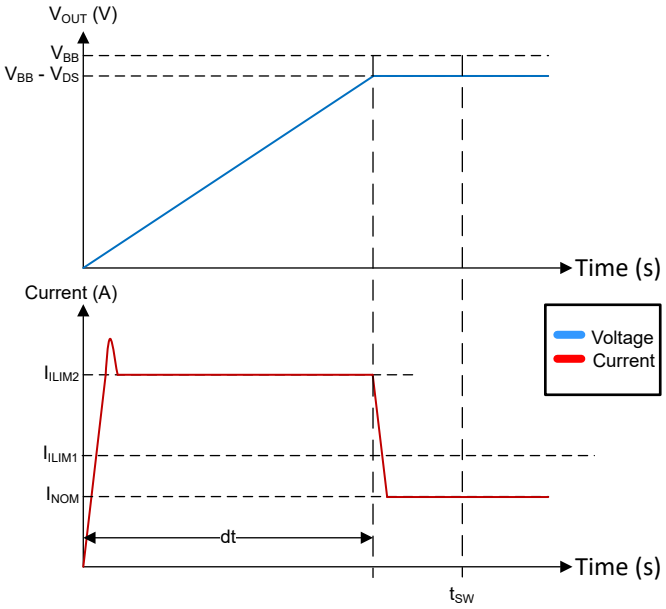


Figure 8-3. Capacitive Charging Changing Current Limit

Alternatively, if the switch is open, the current limit starts out at a lower value and then the switch can be closed when the capacitance gets charged up. This lower current limit level allows higher value capacitance to be charged up. The timing diagram can be seen in Figure 8-4.

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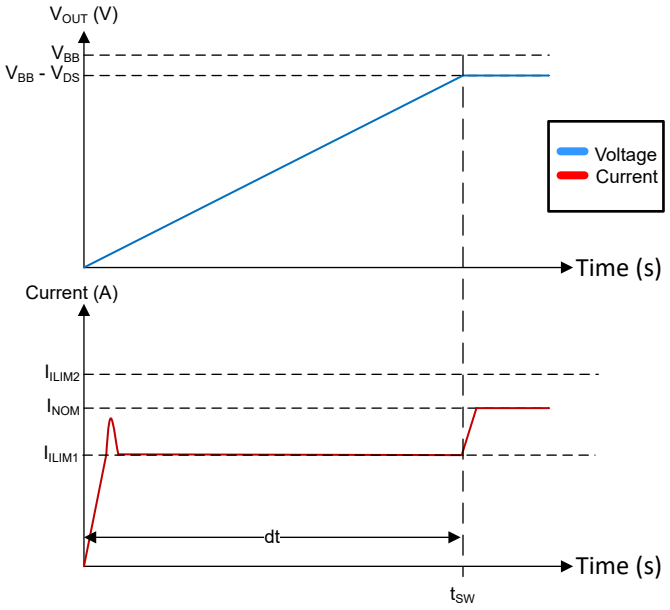


Figure 8-4. Large Capacitive Charging Changing Current Limit

8.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 24V automotive system. The supply voltage must be within the range specified in Section 5.3.

Table 8-2. Voltage Operating Ranges

VS VOLTAGE RANGE	NOTE
6V to 10V	Extended lower 24V automotive battery operation such as cold crank and start-stop. Device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy and timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for.
10V to 32V	Nominal 24V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.
32V to 60V	Extended upper 24V automotive battery operation such as double battery. Device is fully functional and protected but some parametrics such as timing parameters can deviate from specifications. Check the individual specifications in the Electrical Characteristics to confirm the voltage range it is applicable for.
60V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged and is fully protect against short circuits.

8.4 Layout

8.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. If the output current is very high, the power dissipation can be large. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat-flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the board opposite the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.

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- Make sure all thermal vias are either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To make sure of reliability and performance, the solder coverage must be at least 85%.

8.4.2 Layout Example

8.4.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

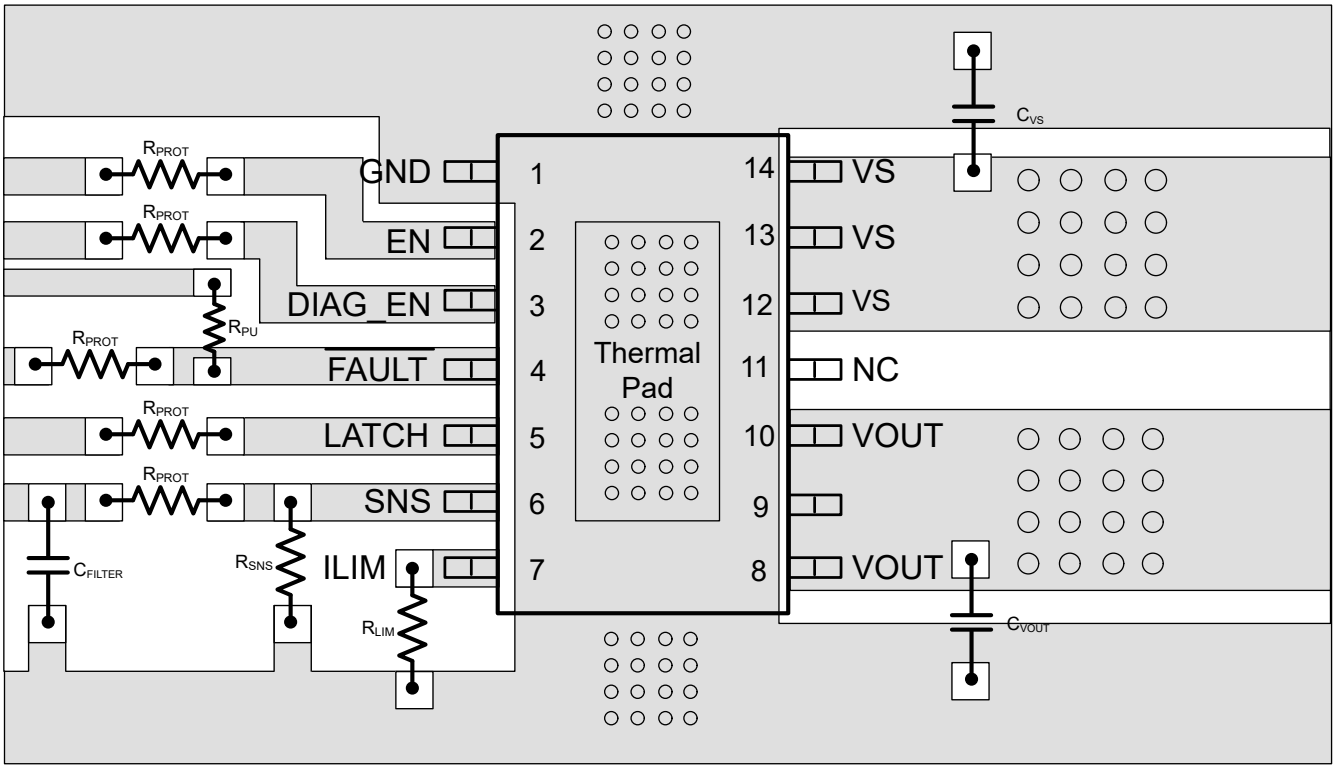


Figure 8-5. Layout Without a GND Network

8.4.2.2 With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper.

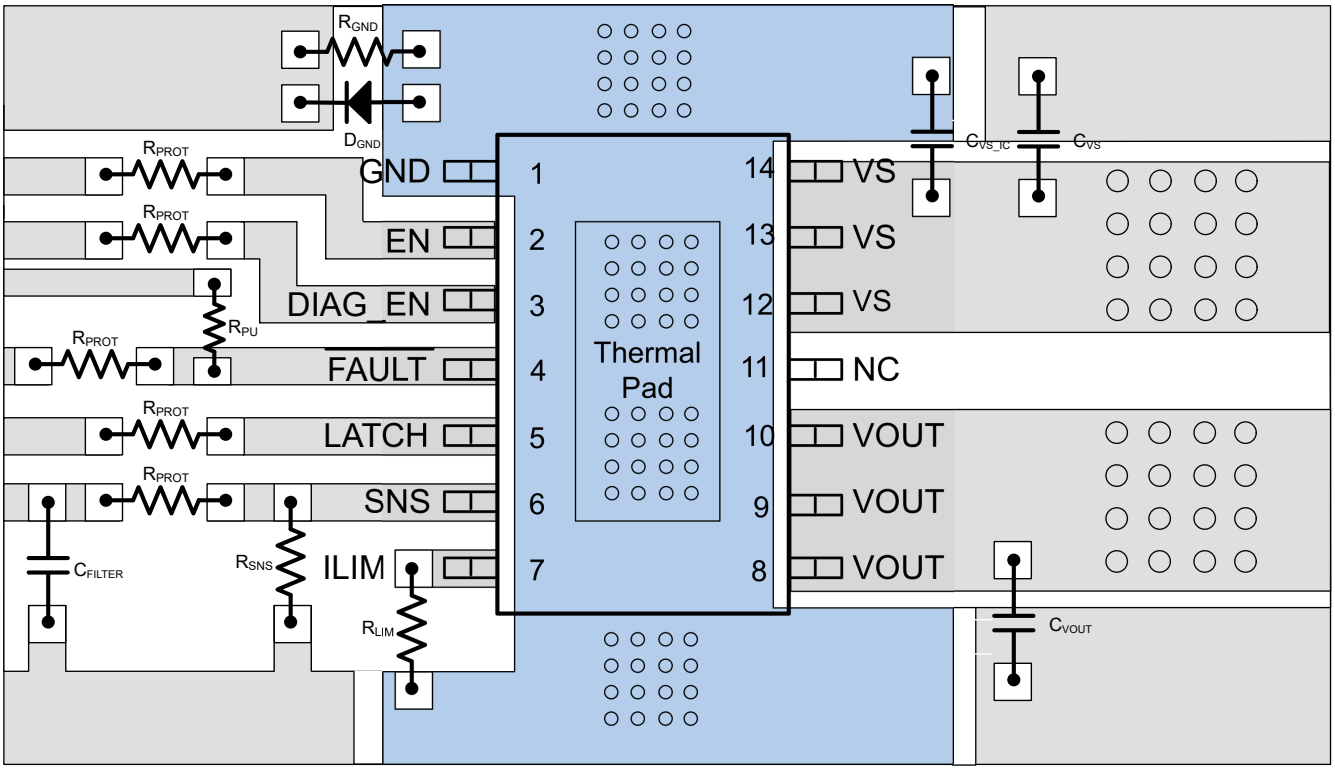


Figure 8-6. Layout With a GND Network

8.4.2.3 Thermal Considerations

This device has thermal shutdown (TABS) circuitry as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the thermal-shutdown trip point. If the junction temperature exceeds the thermal-shutdown trip point, the output turns off. When the junction temperature falls below the thermal-shutdown trip point, the output turns on again.

Calculate the power dissipated by the device according to Equation 15.

$$P_T = I_{OUT}^2 \times R_{DSON} + V_S \times I_{Q,\,VS} \quad (15)$$

where

- P_T = Total power dissipation of the device

After determining the power dissipated by the device, calculate the junction temperature from the ambient temperature and the device thermal impedance.

$$T_J = T_A + R_{\theta JA} \times P_T \quad (16)$$

For more information, please see *How to Drive Resistive, Inductive, Capacitive, and Lighting Loads* application note.

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

Texas Instruments, *How to Drive Resistive, Inductive, Capacitive, and Lighting Loads* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2025) to Revision B (October 2026)	Page
• Changed SNS pin fault reporting from a voltage of V_{SNSFH} to a voltage equal to $I_{SNSFLT} \times R_{SNS}$	15
• Deleted Overvoltage condition from Table 7-2	20
• Changed from I_{NOM} to $I_{Q,\ VS}$ in Equation 15	34

Changes from Revision * (June 2024) to Revision A (July 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed Continuous supply voltage, V_S with respect to IC GND max value from 64V to 70V	4
• Changed Continuous output voltage, V_{OUT} with respect to IC GND max value from from 64V to 70V	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS1HTC100QPWPRQ1	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPSHT00
TPS1HTC100QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPSHT00

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

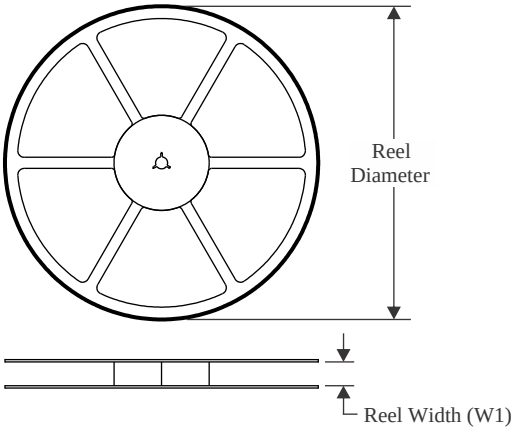
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

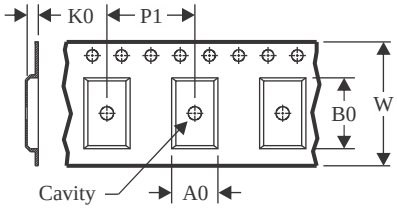
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

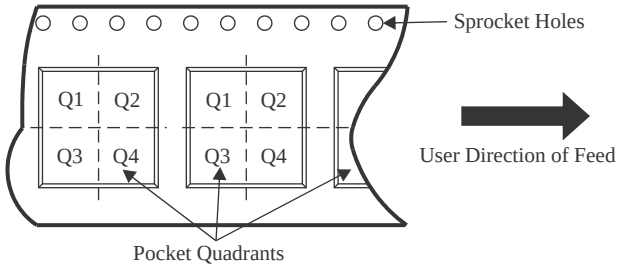


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

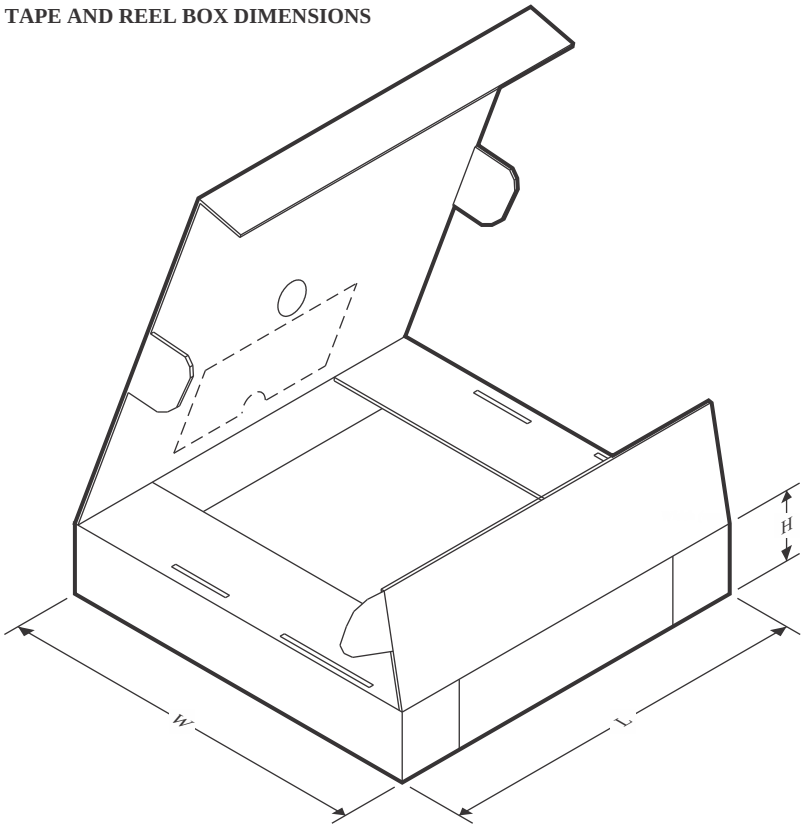
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS1HTC100QPWPRQ1	HTSSOP	PWP	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1HTC100QPWPRQ1	HTSSOP	PWP	14	3000	353.0	353.0	32.0

GENERIC PACKAGE VIEW

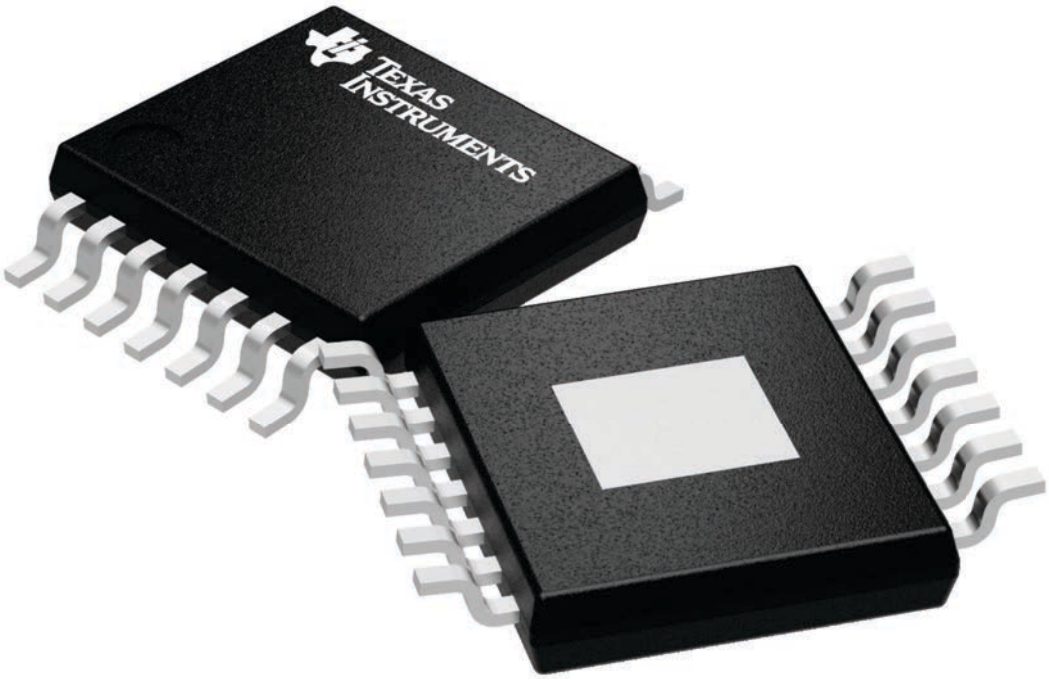
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



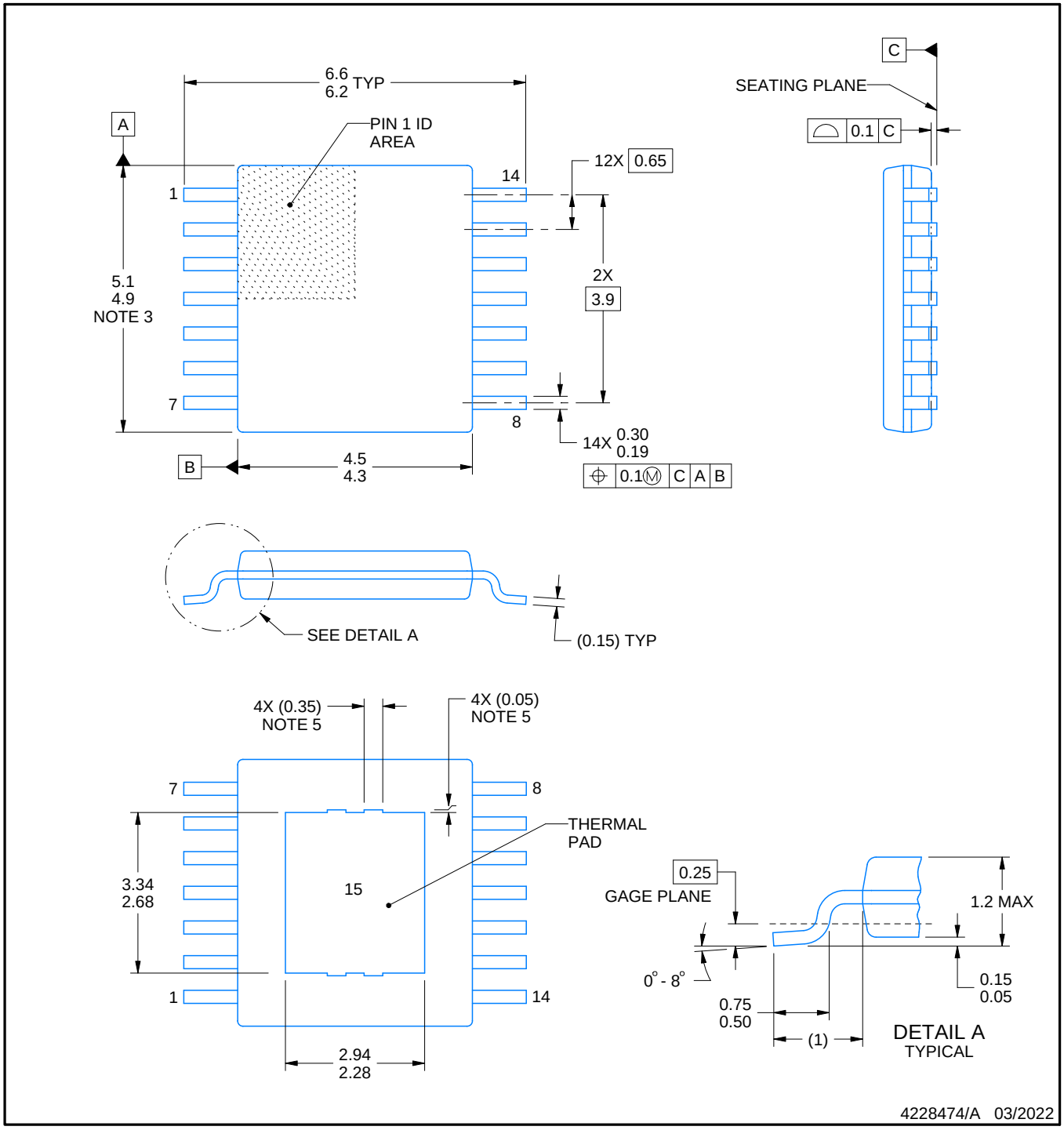
4224995/A

PACKAGE OUTLINE

PWP0014J

PowerPAD™ TSSOP - 1.2 mm max height

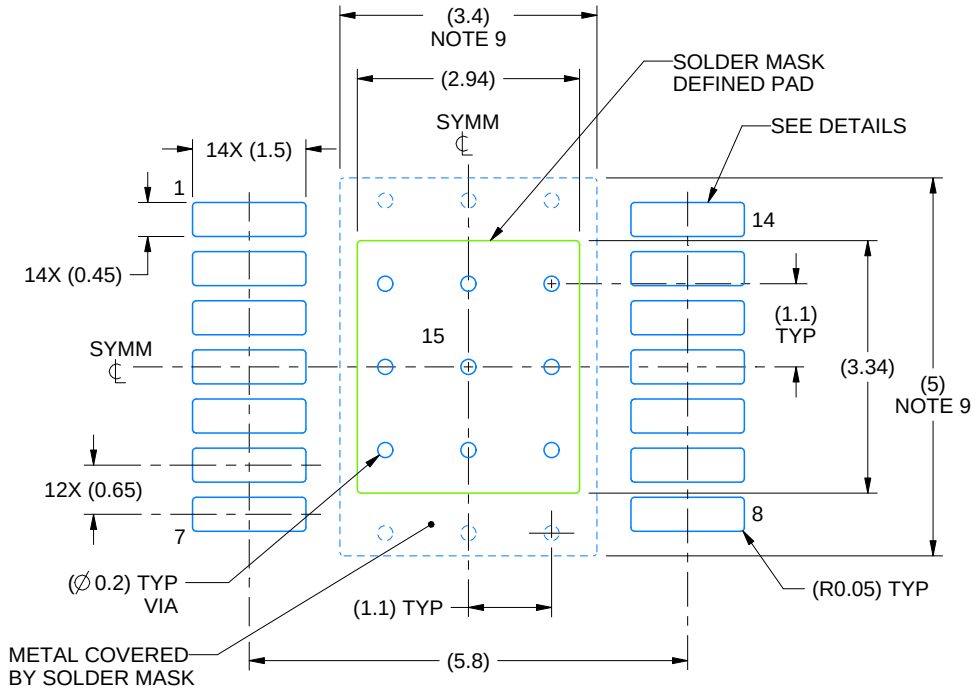
PLASTIC SMALL OUTLINE



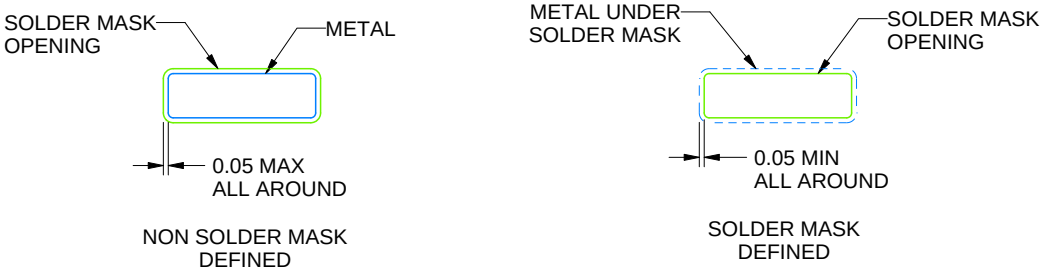
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
SCALE:10X

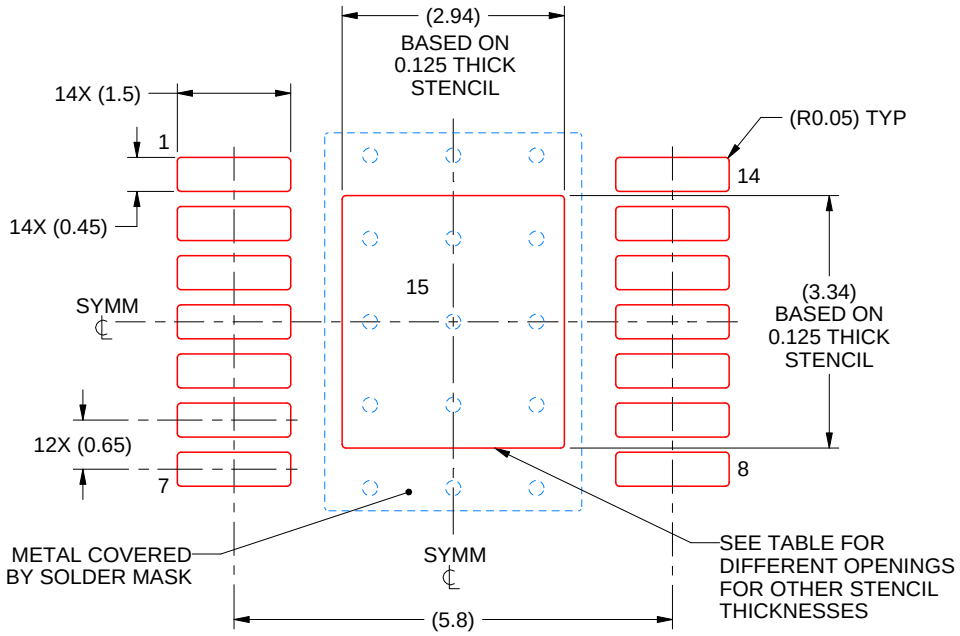


SOLDER MASK DETAILS
PADS 1-14

4228474/A 03/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.29 X 3.73
0.125	2.94 X 3.34 (SHOWN)
0.15	2.69 X 3.05
0.175	2.49 X 2.82

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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