TPS22924x 3.6-V, 2-A, 18.3-mΩ On-Resistance Load Switch

1 Features

- Integrated Single Load Switch
- Input Voltage: 0.75 V to 3.6 V
- On-Resistance
  - R_{ON} = 18.3 mΩ at V_{IN} = 3.6 V
  - R_{ON} = 19.6 mΩ at V_{IN} = 1.8 V
  - R_{ON} = 19.4 mΩ at V_{IN} = 1.2 V
  - R_{ON} = 22.7 mΩ at V_{IN} = 0.75 V
- Small CSP-6 package 0.9 mm x 1.4 mm, 0.5-mm Pitch
- 2 A Maximum Continuous Switch Current
- Low Shutdown Current
- Low Threshold Control Input
- Controlled Slew Rate to Avoid Inrush Currents
- Quick Output Discharge Transistor
- ESD Performance Tested Per JESD 22
  - 5000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Battery Powered Equipment
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Point Of Sales Terminal
- GPS Devices
- Digital Cameras
- Notebooks / Tablet PCs / eReaders
- Smartphones

3 Description

The TPS22924x is a small, low R_{ON} load switch with controlled turn on. The device contains a N-channel MOSFET that can operate over an input voltage range of 0.75 V to 3.6 V. An integrated charge pump biases the NMOS switch to achieve a minimum switch ON resistance. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

A 1250 Ω on-chip load resistor is added for output quick discharge when the switch is turned off. The rise time of the device is internally controlled to avoid inrush current. The TPS22924B features a rise time of 100 µs at V_{IN} = 3.6 V while the TPS22924C has a rise time of 800 µs at V_{IN} = 3.6 V.

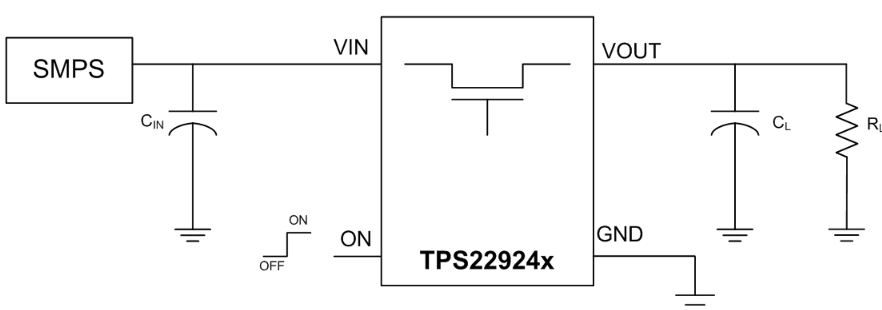
The TPS22924x is available in an ultra-small space-saving 6-pin CSP package and is characterized for operation over the free-air temperature range of –40ºC to 85ºC.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22924B	DSBGA (6)	1.40 mm × 0.90 mm
TPS22924C	DSBGA (6)	1.40 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



NOTE: SMPS = Switched-mode power supply

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2014) to Revision E	Page
• Added device TPS22924C	1
• Deleted *Features*: r_{ON} = 18.5 mΩ at V_{IN} = 2.5 V	1
• Deleted *Features*: r_{ON} = 20.3 mΩ at V_{IN} = 1.0 V	1
• Added text to the *Description* "while the TPS22924C has a rise time of 800 µs at V_{IN} = 3.6 V. "	1
• Added: TPS22924CYZPR and TPS22924CYZPRB information to *Device Comparison Table*	3
• Added "Storage temperature" to the *Absolute Maximum Ratings* [(1)] table	4
• Changed *Handling Ratings* to *ESD Ratings*	4
• Added section *AC Characteristics (TPS22924C)*	10
• Changed the *Application Curve* section	17

Changes from Revision C (July 2014) to Revision D	Page
• Added *Pin Configuration and Functions* section, *Overview* section, *Feature Description* section, *Power Supply Recommendations* section	1

Changes from Revision B (June 2013) to Revision C	Page
• Added Device Information table.	1
• Added *Handling Ratings* table.	4
• Added Detailed Description section.	14

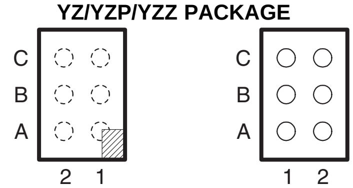
5 Device Comparison Table

T_A	PACKAGE (1)	ORDERABLE PART NUMBER	TOP-SIDE MARKING (2)	BACKSIDE COATING (3)	RISE TIME AT VIN = 3.3V (TYP.)
–40°C to 85°C	YZ (0.4mm height)	TPS22924BYZR	_ _ _ 5N _	No	96µs
–40°C to 85°C	YZP (0.5mm height)	TPS22924BYZPRB	_ _ _ 5N _	Yes	96µs
–40°C to 85°C	YZZ (0.35mm height)	TPS22924BYZZR	_ _ _ 7A _	No	96µs
–40°C to 85°C	YZP (0.5mm height)	TPS22924CYZPR	_ _ _ 5L _	No	800µs
–40°C to 85°C	YZP (0.4mm height)	TPS22924CYZPRB	_ _ _ 5L _	Yes	800µs

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).
(3) CSP (DSBGA) devices manufactured with backside coating have an increased resistance to cracking due to the increased physical strength of the package. Devices with backside coating are highly encouraged for new designs.

6 Pin Configuration and Functions

YZ/YZP/YZZ PACKAGE



Laser Marking View Bump View

Table 1. Pin Assignments (YZ/YZP/YZZ Package)

C	GND	ON
B	VOUT	VIN
A	VOUT	VIN
	1	2

Pin Functions

NO.	NAME	DESCRIPTION
C1	GND	Ground
C2	ON	Switch control input, active high. Do not leave floating
A1, B1	VOUT	Switch output
A2, B2	VIN	Switch input, bypass this input with a ceramic capacitor to ground

7 Specifications

7.1 Absolute Maximum Ratings [(1)]

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	4	V
V_{OUT}	Output voltage range		V_{IN} + 0.3	V
V_{ON}	Input voltage range	–0.3	4	V
I_{MAX}	Maximum continuous switch current, T_A = –40°C to 85°C		2	A
I_{PLS}	Maximum pulsed switch current, 100-µs pulse, 2% duty cycle, T_A = –40°C to 85°C		4	A
T_A	Operating free-air temperature range	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [(1)]	±5000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.75	3.6	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{IN} = 2.5 V to 3.6 V	1.2	3.6	V
		V_{IN} = 0.75 V to 2.5 V	0.9	3.6	
V_{IL}	Low-level input voltage, ON	V_{IN} = 2.5 V to 3.6 V		0.6	V
		V_{IN} = 0.75 V to 2.49 V		0.4	
C_{IN}	Input capacitance		1 [(1)]		µF

(1) See the *Input Capacitor* section in Application Information.

7.4 Thermal Information

THERMAL METRIC [(1)]		TPS22924x YZ/YZZ/YZP 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.8	
ψ_{JT}	Junction-to-top characterization parameter	5.7	
ψ_{JB}	Junction-to-board characterization parameter	22.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 0.75 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP (1)	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0, V_{IN} = V_{ON}	V_{IN} = 3.6 V	Full		75	160	µA
			V_{IN} = 2.5 V			42	70	
			V_{IN} = 1.8 V			50	350	
			V_{IN} = 1.2 V			95	200	
			V_{IN} = 1.0 V			65	110	
			V_{IN} = 0.75 V			35	70	
$I_{IN(LEAK)}$	OFF-state supply current	V_{ON} = GND, OUT = 0V		Full			3.5	µA
R_{ON}	ON-state resistance	I_{OUT} = –200 mA	V_{IN} = 3.6 V	25°C		18.3	19.7	mΩ
				Full			26.0	
			V_{IN} = 2.5 V	25°C		18.5	19.5	
				Full			25.8	
			V_{IN} = 1.8 V	25°C		19.6	21.8	
				Full			27.4	
			V_{IN} = 1.2 V	25°C		19.4	21.8	
				Full			28.0	
			V_{IN} = 1.0 V	25°C		20.3	21.2	
				Full			28.6	
			V_{IN} = 0.75 V	25°C		22.7	25.3	
				Full			34.8	
R_{PD}	Output pulldown resistance (2)	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 3 mA		25°C		1250	1500	Ω
I_{ON}	ON-state input leakage current	V_{ON} = 0.9 V to 3.6 V or GND		Full			0.1	µA

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.
(2) See *Output Pulldown* in the Application and Implementation section.

7.6 Switching Characteristics, V_{IN} = 3.6 V

V_{IN} = 3.6 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS22924B (TYP)	TPS22924C (TYP)	UNIT
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6V	111	800	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6V	3	3	µs
t_r	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6V	96	800	µs
t_f	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 3.6V	2.5	2.5	µs

7.7 Switching Characteristics, V_{IN} = 0.9 V

V_{IN} = 0.9 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS22924B (TYP)	TPS22924C (TYP)	UNIT
t_{ON}	Turn-ON time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9V	160	865	µs
t_{OFF}	Turn-OFF time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9V	20	20	µs
t_r	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9V	81	500	µs
t_f	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, V_{IN} = 0.9V	5	5	µs

7.8 Typical Characteristics

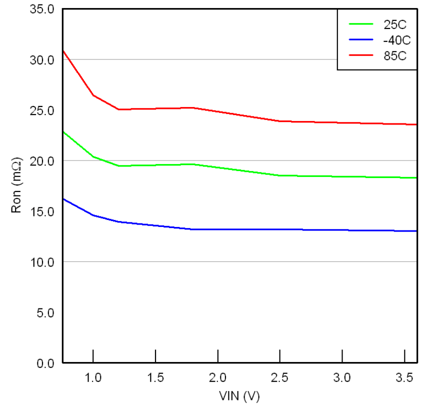


Figure 1. On-State Resistance vs Input Voltage

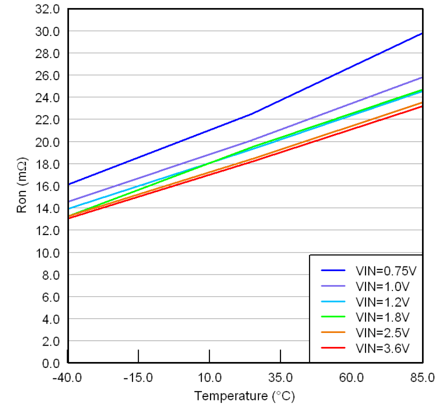


Figure 2. On-State Resistance vs Temperature

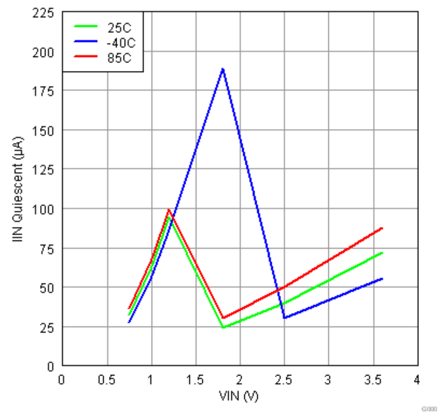


Figure 3. Input Current, Quiescent vs Input Voltage

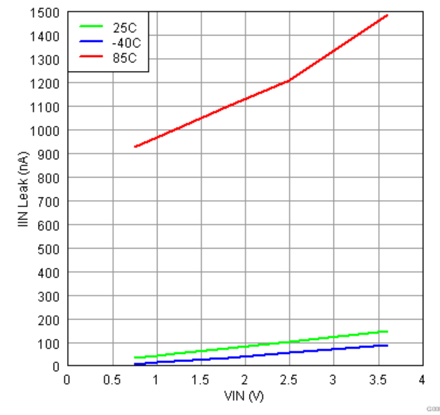


Figure 4. Input Current, Leak vs Input Voltage

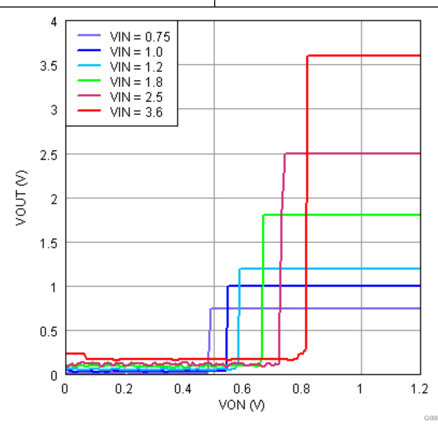
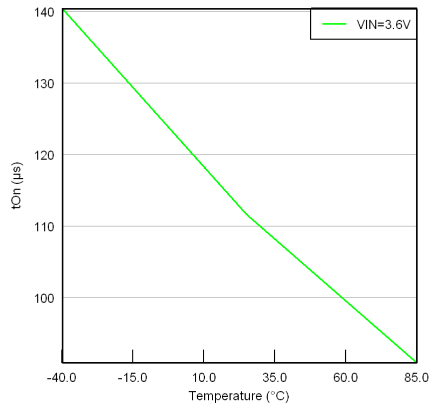


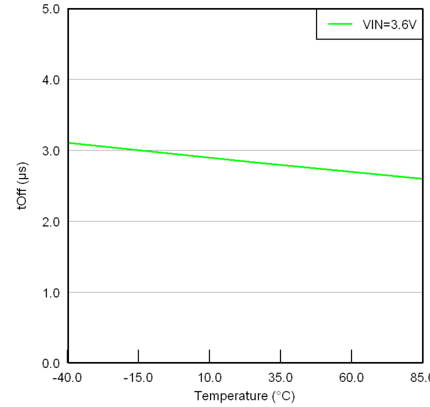
Figure 5. On Input Threshold

7.9 AC Characteristics (TPS22924B)



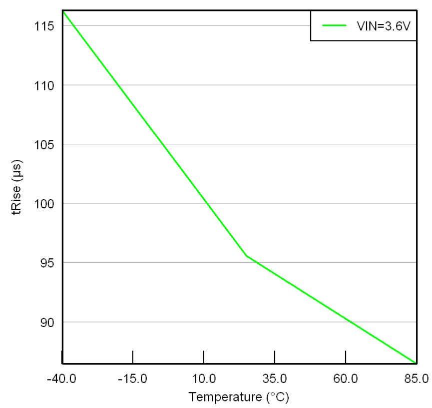
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 6. Turn-On Time vs Temperature



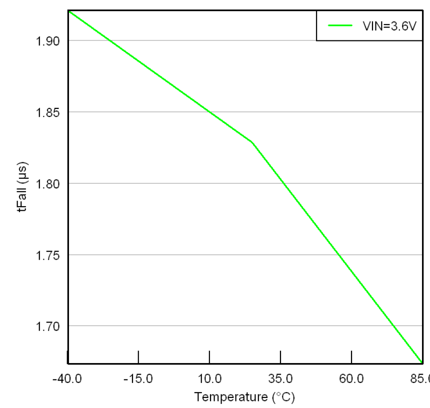
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 7. Turn-Off Time vs Temperature



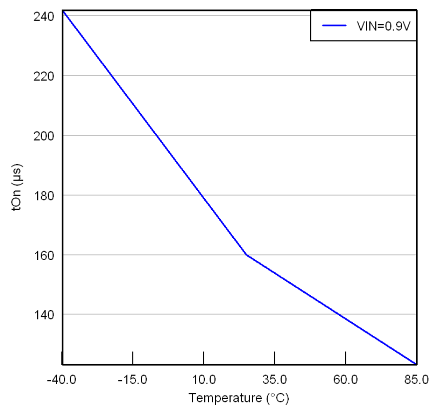
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 8. Rise Time vs Temperature



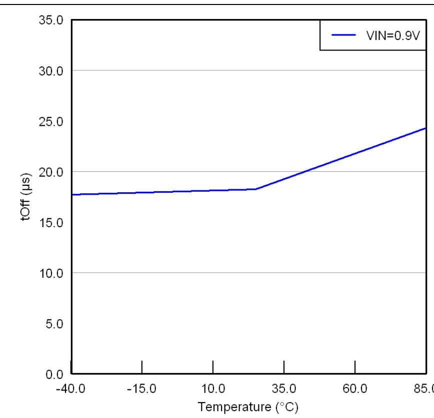
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 9. Fall Time vs Temperature



V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

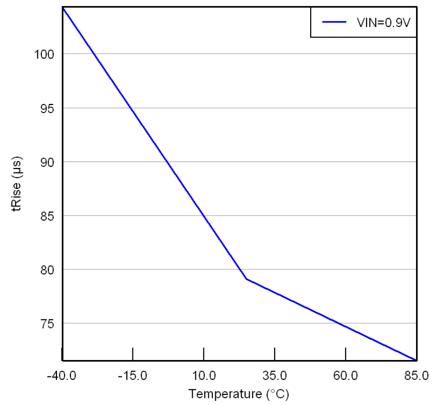
Figure 10. Turn-On Time vs Temperature



V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

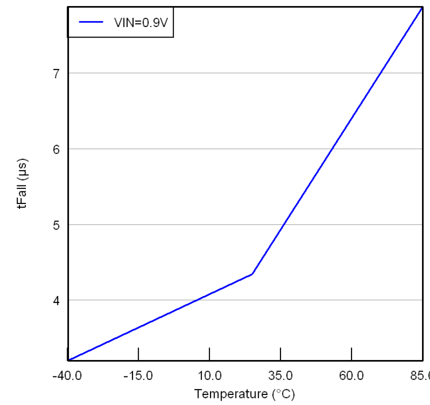
Figure 11. Turn-Off Time vs Temperature

AC Characteristics (TPS22924B) (continued)



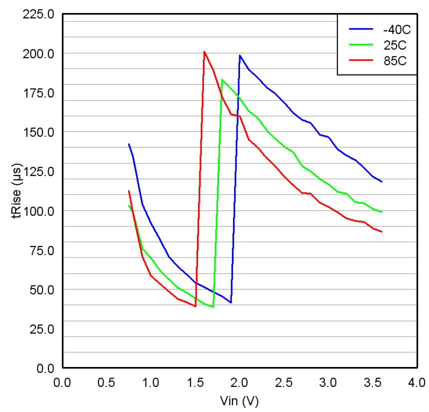
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 12. Rise Time vs Temperature



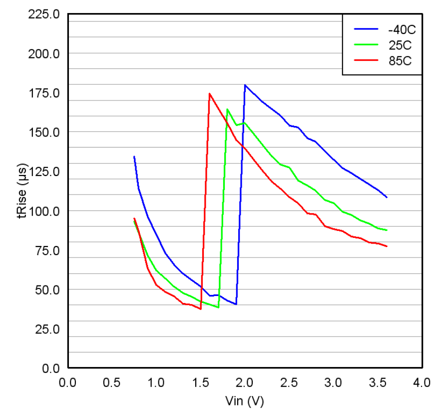
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 13. Fall Time vs Temperature



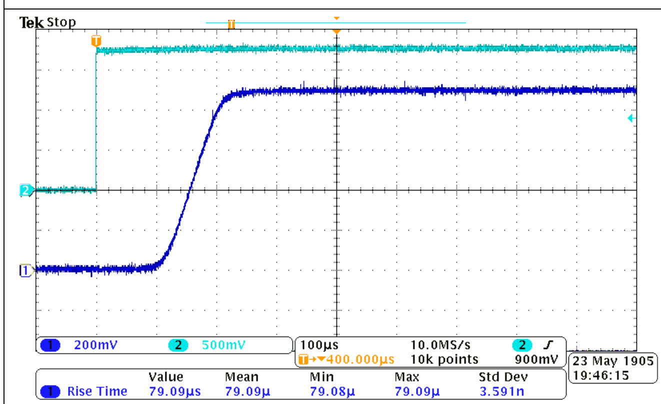
V_{ON} = 1.8 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 14. Rise Time vs Input Voltage



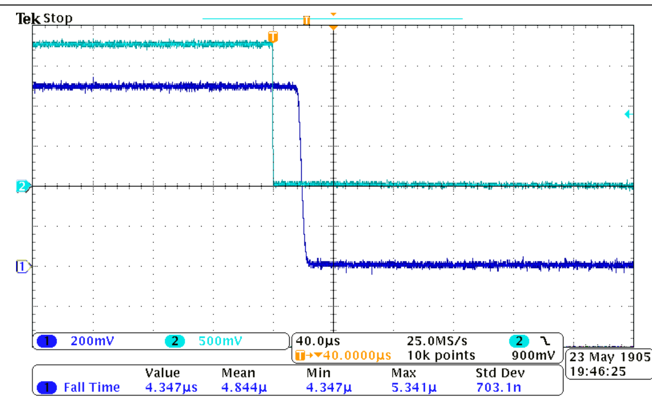
V_{ON} = 1.8 V, C_L = 20 µF, R_L = 10 Ω

Figure 15. Rise Time vs Input Voltage



C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

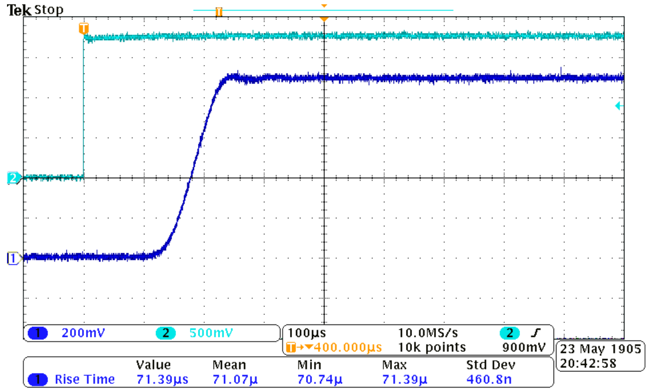
Figure 16. Turn-On Response



C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

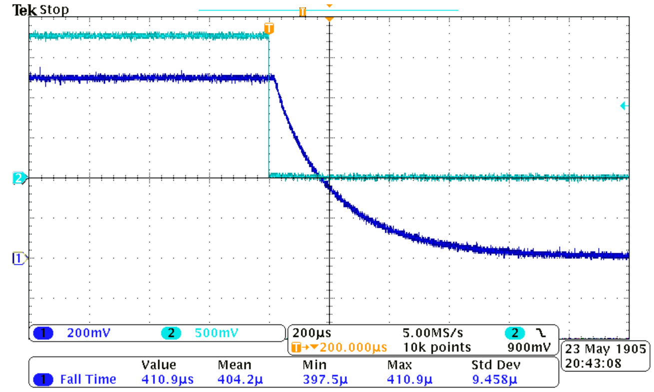
Figure 17. Turn-Off Response

AC Characteristics (TPS22924B) (continued)



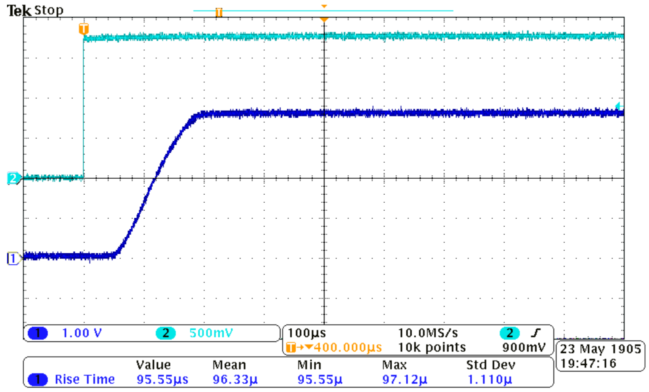
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

Figure 18. Turn-On Response



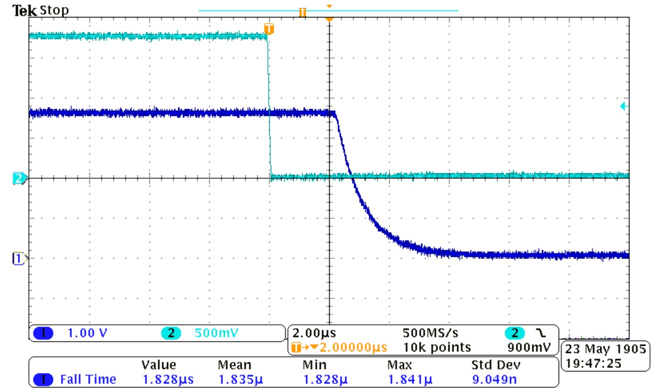
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

Figure 19. Turn-Off Response



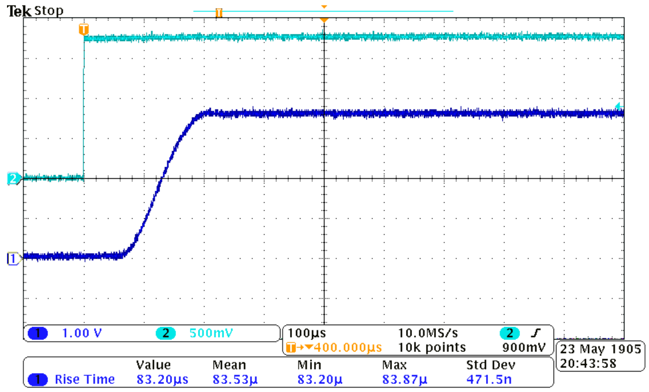
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

Figure 20. Turn-On Response



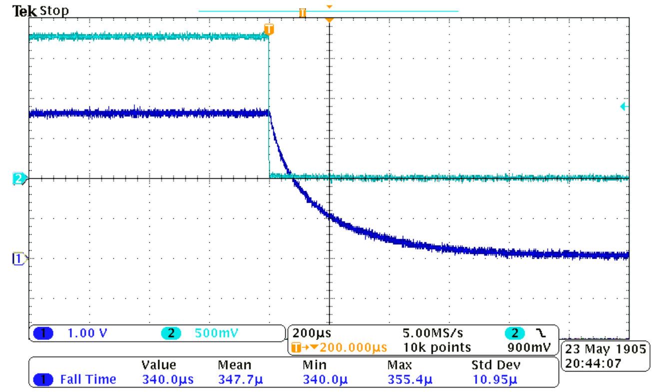
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

Figure 21. Turn-Off Response



C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

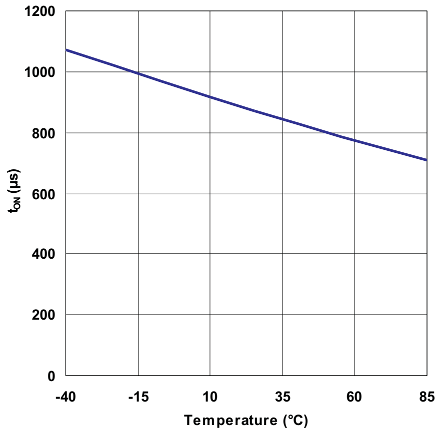
Figure 22. Turn-On Response



C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

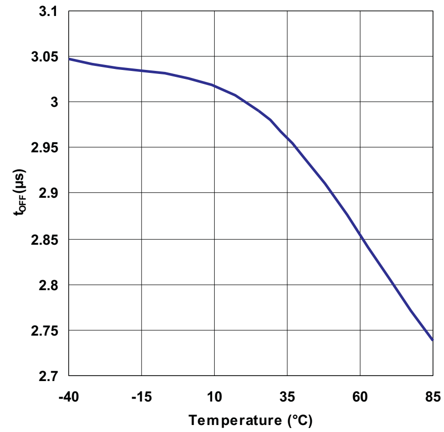
Figure 23. Turn-Off Response

7.10 AC Characteristics (TPS22924C)



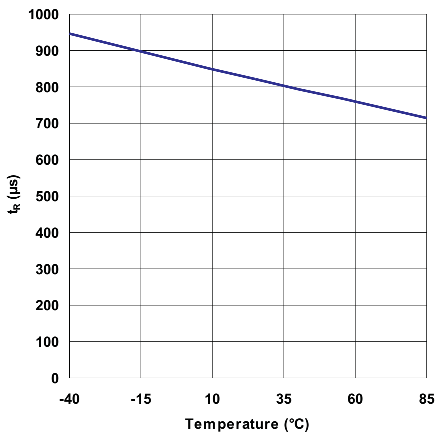
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 24. Turn-On Time vs Temperature



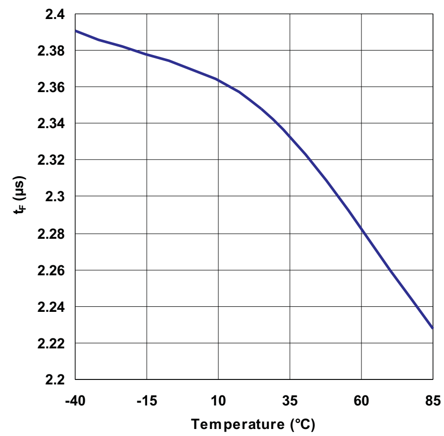
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 25. Turn-Off Time vs Temperature



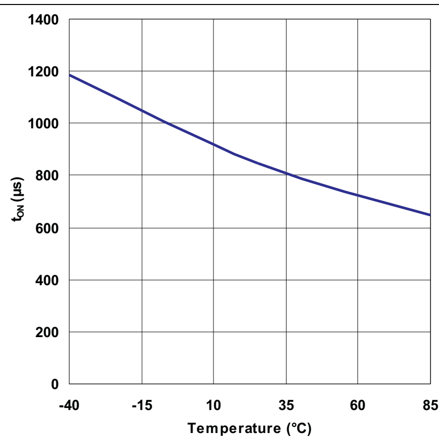
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 26. Rise Time vs Temperature



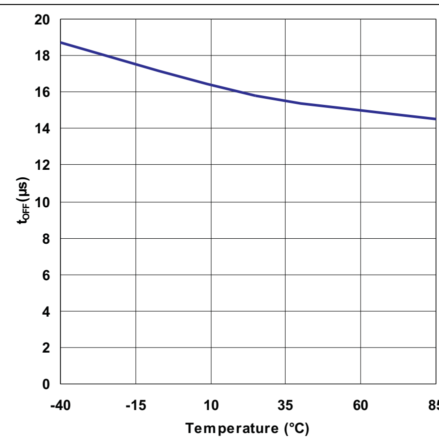
V_{IN} = 3.6 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 27. Fall Time vs Temperature



V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

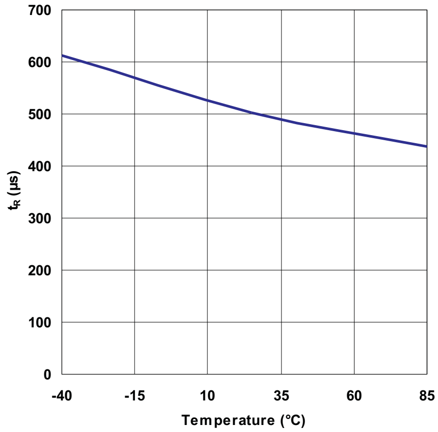
Figure 28. Turn-On Time vs Temperature



V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

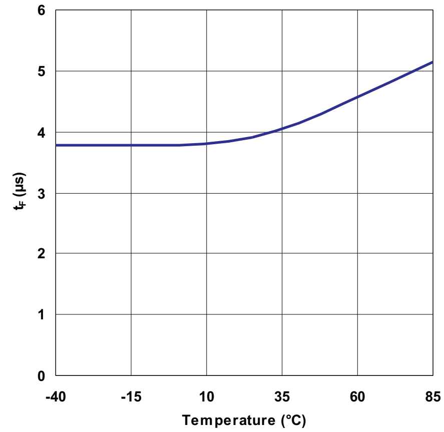
Figure 29. Turn-Off Time vs Temperature

AC Characteristics (TPS22924C) (continued)



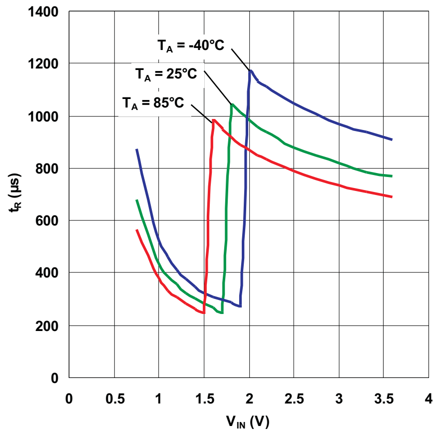
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 30. Rise Time vs Temperature



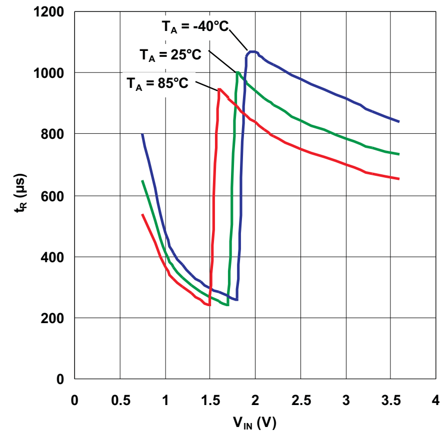
V_{IN} = 0.9 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 31. Fall Time vs Temperature



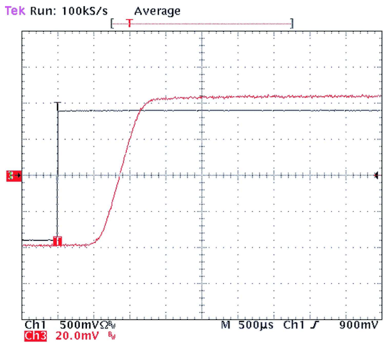
V_{ON} = 1.8 V, C_L = 0.1 µF, R_L = 10 Ω

Figure 32. Rise Time vs Input Voltage



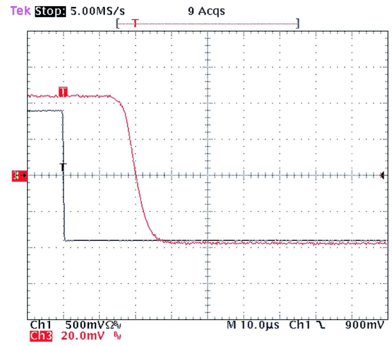
V_{ON} = 1.8 V, C_L = 20 µF, R_L = 10 Ω

Figure 33. Rise Time vs Input Voltage



C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

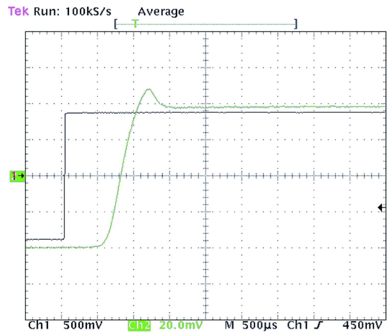
Figure 34. Turn-On Response



C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

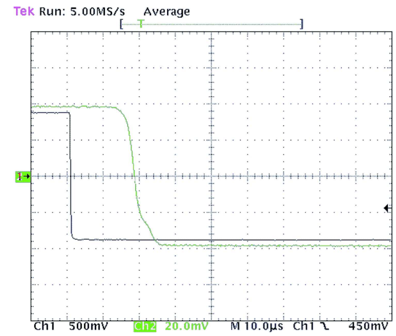
Figure 35. Turn-Off Response

AC Characteristics (TPS22924C) (continued)



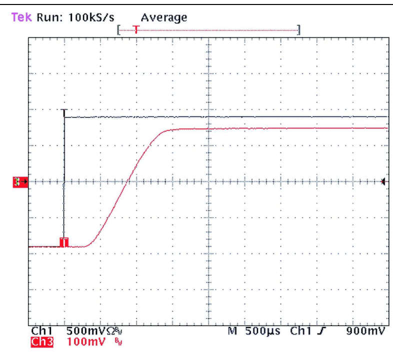
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

Figure 36. Turn-On Response



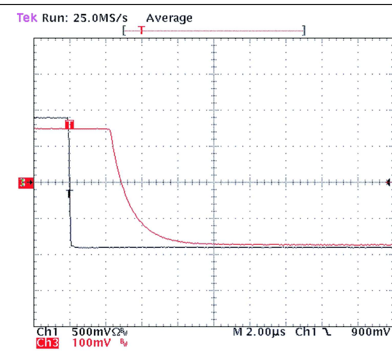
C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 0.9 V, T_A = 25°C

Figure 37. Turn-Off Response



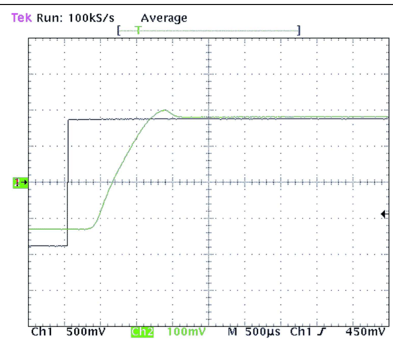
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

Figure 38. Turn-On Response



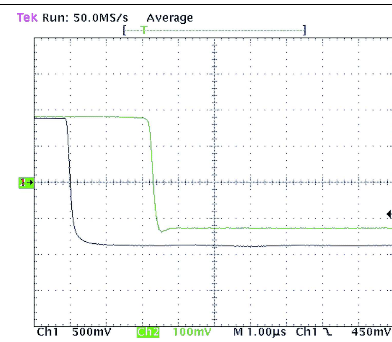
C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

Figure 39. Turn-Off Response



C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

Figure 40. Turn-On Response



C_{IN} = 47 µF, C_L = 20 µF, R_L = 10 Ω, V_{IN} = 3.6 V, T_A = 25°C

Figure 41. Turn-Off Response

8 Parameter Measurement Information

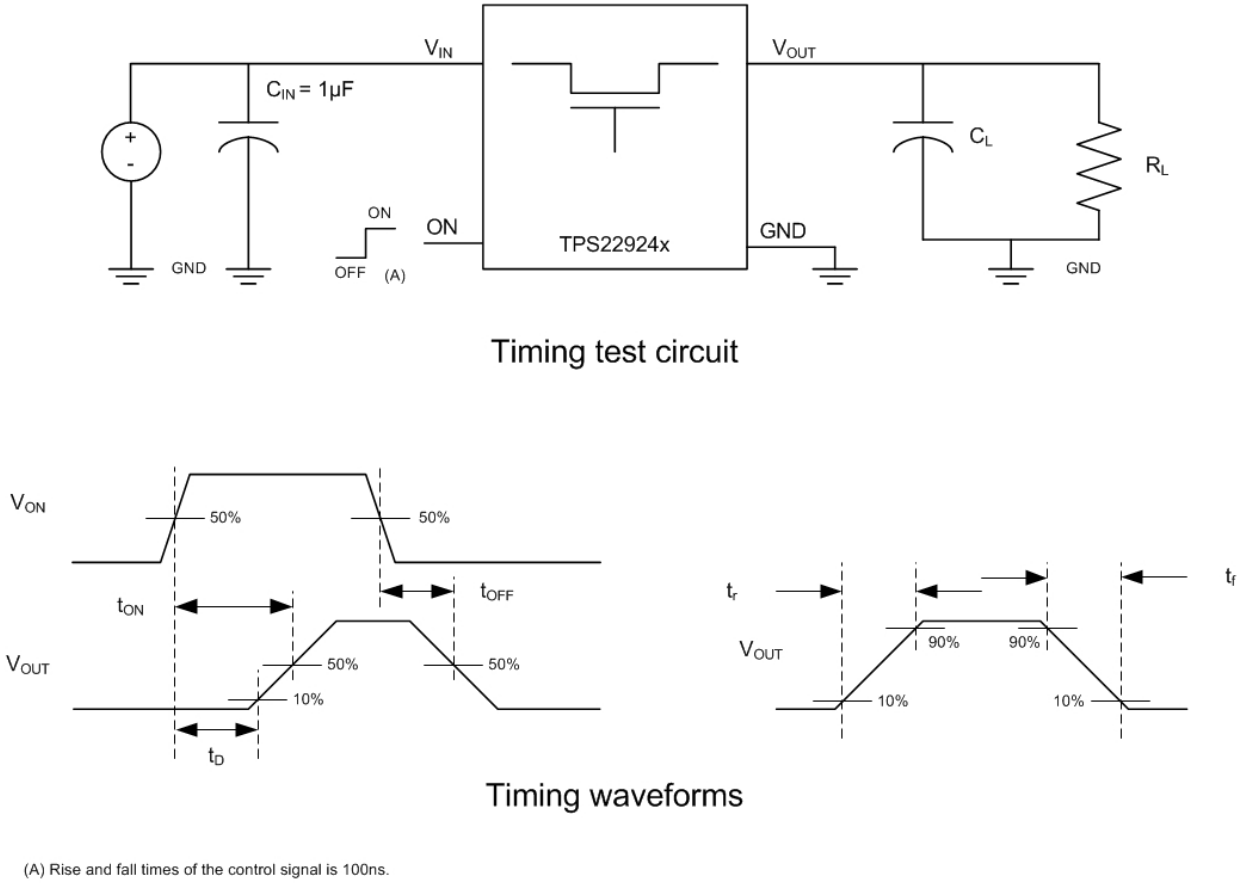


Figure 42. Test Circuit and t_{ON}/t_{OFF} Waveforms

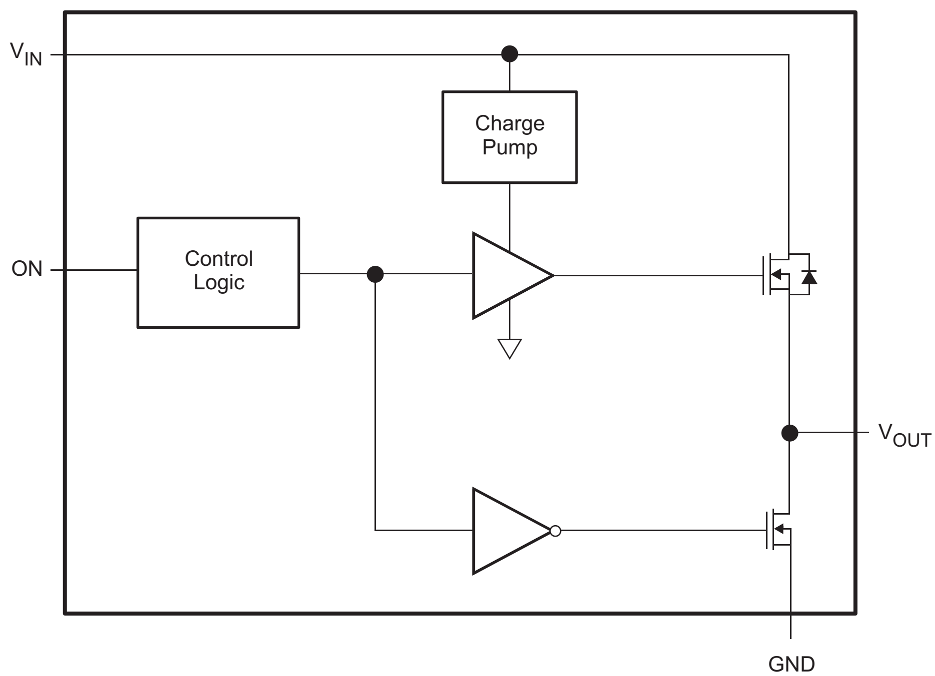
9 Detailed Description

9.1 Overview

The TPS22924x is a single channel, 2-A load switch in a small, space-saving CSP-6 package. This device implements a low resistance N-channel MOSFET with a controlled rise time for applications that need to limit the inrush current.

This device is also designed to have very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

9.3.2 Output Capacitor

Due to the integral body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

9.3.3 Output Pulldown

The output pulldown is active when the user is turning off the main pass FET. The pulldown discharges the output rail to approximately 10% of the rail, then the output pulldown is automatically disconnected to optimize the shutdown current.

9.4 Device Functional Modes

ON (CONTROL SIGNAL)	VIN to VOUT	VOUT to GND (1)
L	OFF	ON
H	ON	OFF

(1) See application section *Output Pulldown* .

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN condition of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this datasheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV = Voltage drop from VIN to VOUT
- I_{LOAD} = Load current
- R_{ON} = On-resistance of the device for a specific V_{IN}
- An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated. (1)

10.1.2 Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

10.1.3 Output Capacitor

A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup.

10.2 Typical Application

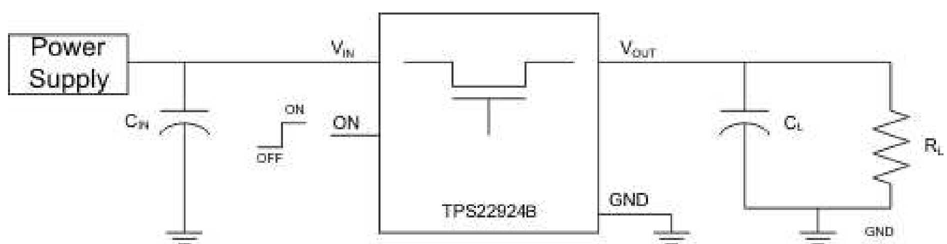


Figure 43. Typical Application

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.6 V
C_L	1 µF
Maximum Acceptable Inrush Current	40 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Managing Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to V_{IN}. This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times \frac{dv}{dt}$$

where

- C = Output capacitance
- $\frac{dv}{dt}$ = Output slew rate (2)

The TPS22924B offers a very slow controlled rise time for minimizing inrush current. This device can be selected based upon the maximum acceptable slew rate which can be calculated using the design requirements and the inrush current equation. An output capacitance of 1.0 µF will be used since the amount of inrush increases with output capacitance:

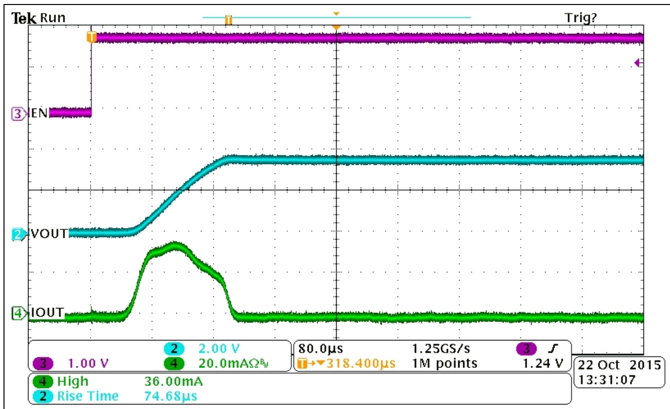
$$40\text{ mA} = 1.0\ \mu\text{F} \times \frac{dv}{dt} \tag{3}$$

$$\frac{dv}{dt} = 40\text{ V/ms} \tag{4}$$

To ensure an inrush current of less than 40 mA, a device with a slew rate less than 40 V/ms must be used.

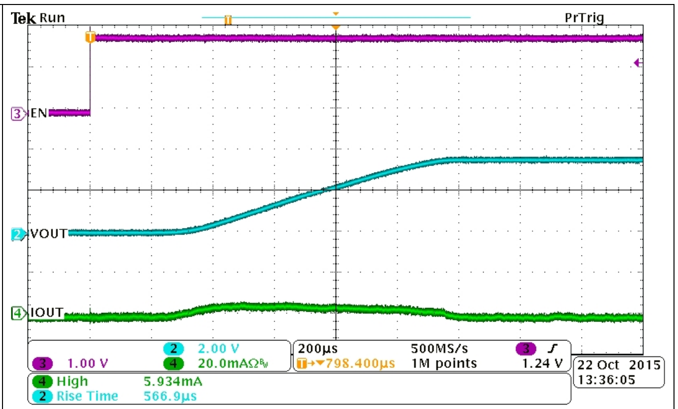
The TPS22924B has a typical rise time of 96 µs at 3.6 V. This results in a slew rate of 37.5 V/ms which meets the above design requirements. For an even lower inrush current requirement, the TPS22924C can be used. The slower rise time of 800 µs at 3.6V results in a slew rate of 4.5 V/ms, well below the design requirements.

10.2.3 Application Curve



V_{IN} = 3.6 V C_L = 1 µF T_A = 25°C

Figure 44. TPS22924B Inrush Current With a 1 µF Capacitor



V_{IN} = 3.6 V C_L = 1 µF T_A = 25°C

Figure 45. TPS22924C Inrush Current With a 1 µF Capacitor

11 Power Supply Recommendations

The device is designed to operate with a VIN range of 0.75 V to 3.6 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1 µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects.

12.2 Layout Example

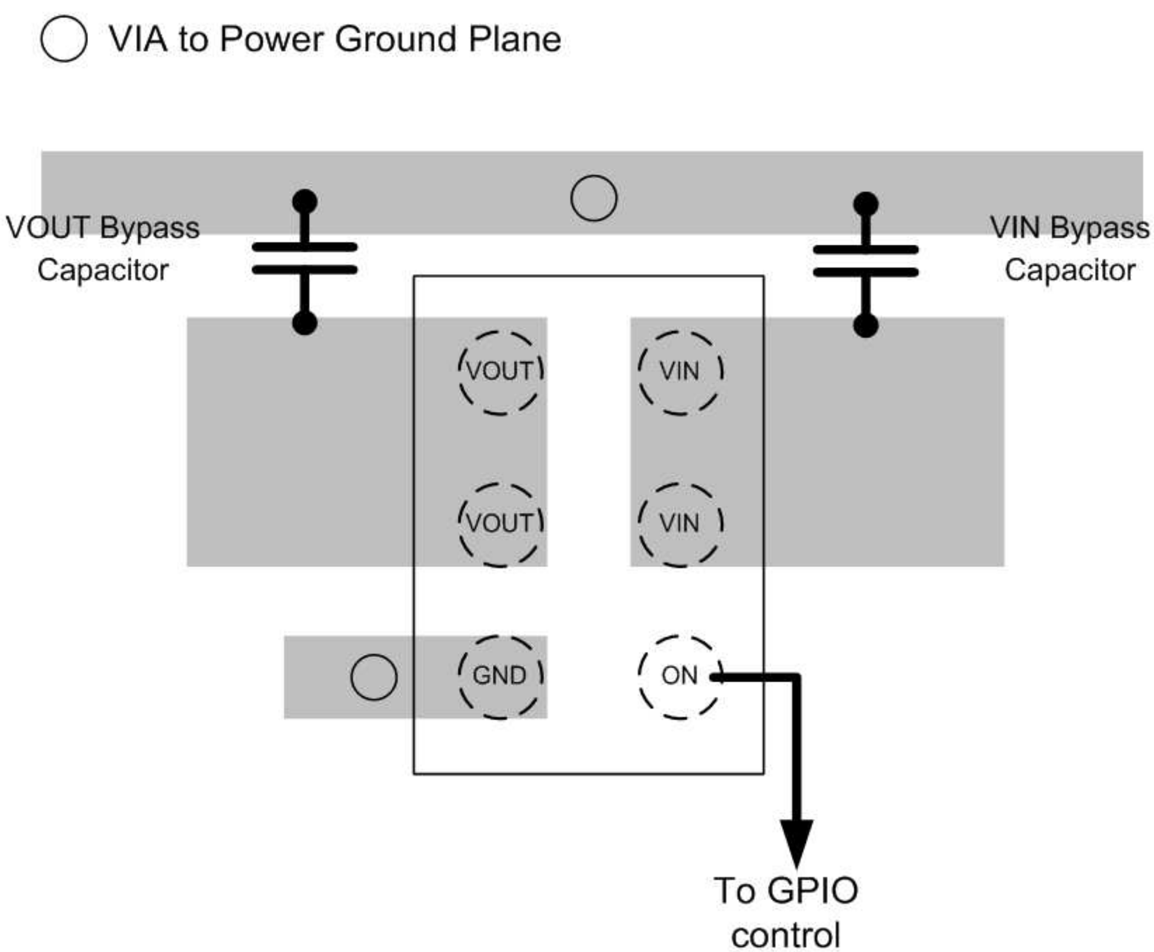


Figure 46. TPS22924x Layout Example

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS22924B	Click here	Click here	Click here	Click here	Click here
TPS22924C	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22924BYZPRB	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5N	Samples
TPS22924BYZR	ACTIVE	DSBGA	YZ	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5N	Samples
TPS22924BYZT	ACTIVE	DSBGA	YZ	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5N	Samples
TPS22924BYZZR	ACTIVE	DSBGA	YZZ	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7A	Samples
TPS22924BYZZT	ACTIVE	DSBGA	YZZ	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7A	Samples
TPS22924CYZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(5L, 5LG)	Samples
TPS22924CYZPRB	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5L	Samples
TPS22924CYZPT	ACTIVE	DSBGA	YZP	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(5LF, 5LG)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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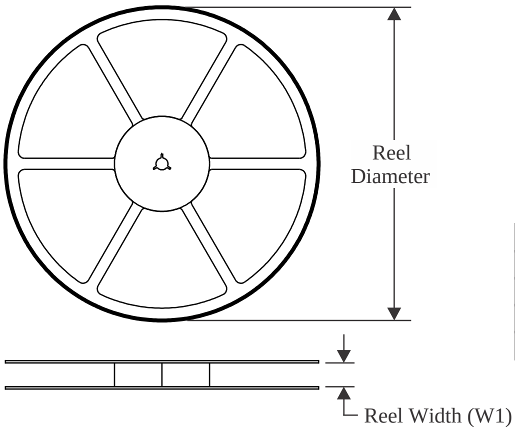
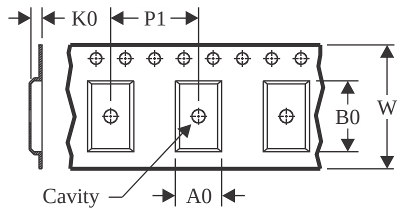
TAPE AND REEL INFORMATION

REEL DIMENSIONS

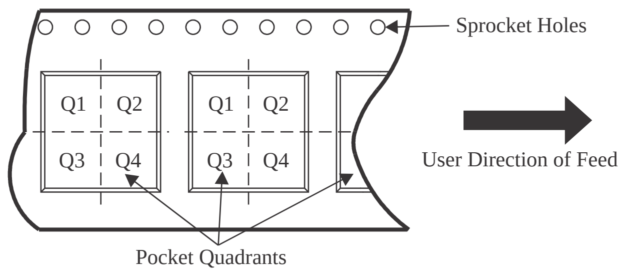


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

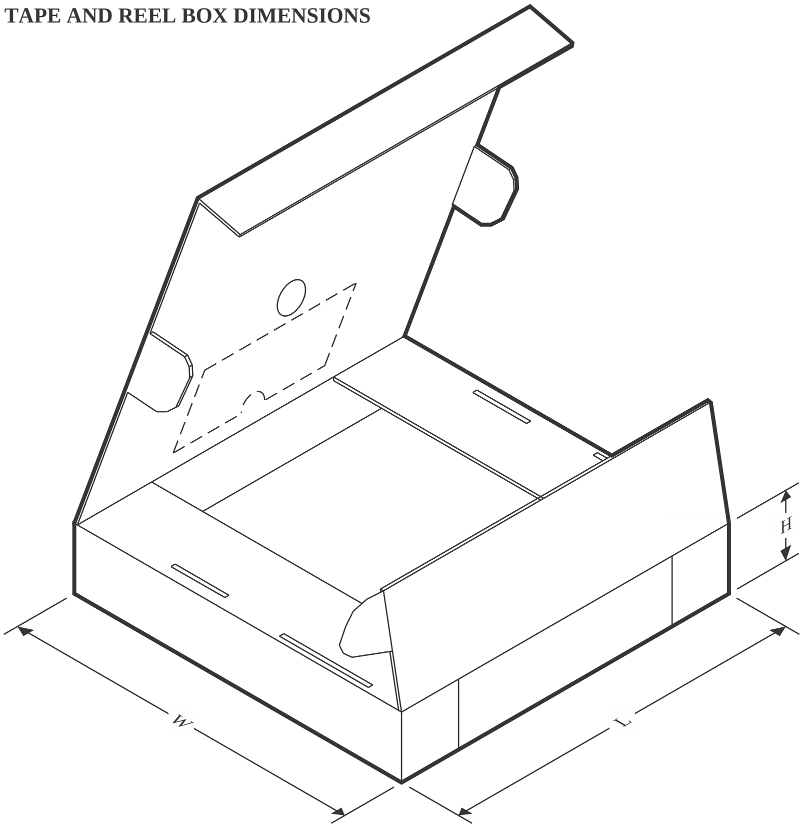
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22924BYZPRB	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924BYZR	DSBGA	YZ	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924BYZT	DSBGA	YZ	6	250	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924BYZZR	DSBGA	YZZ	6	3000	178.0	9.2	1.02	1.52	0.5	4.0	8.0	Q1
TPS22924BYZZT	DSBGA	YZZ	6	250	178.0	9.2	1.02	1.52	0.5	4.0	8.0	Q1
TPS22924CYZPRB	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
TPS22924CYZPT	DSBGA	YZP	6	250	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

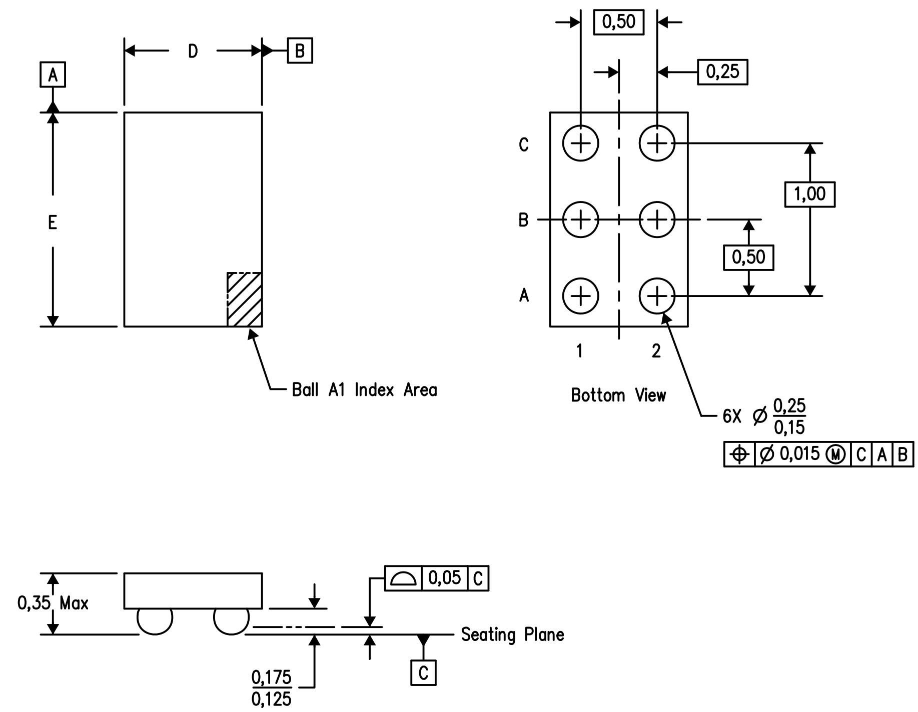
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22924BYZPRB	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924BYZR	DSBGA	YZ	6	3000	220.0	220.0	35.0
TPS22924BYZT	DSBGA	YZ	6	250	220.0	220.0	35.0
TPS22924BYZZR	DSBGA	YZZ	6	3000	220.0	220.0	35.0
TPS22924BYZZT	DSBGA	YZZ	6	250	220.0	220.0	35.0
TPS22924CYZPRB	DSBGA	YZP	6	3000	220.0	220.0	35.0
TPS22924CYZPT	DSBGA	YZP	6	250	220.0	220.0	35.0

YZZ (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



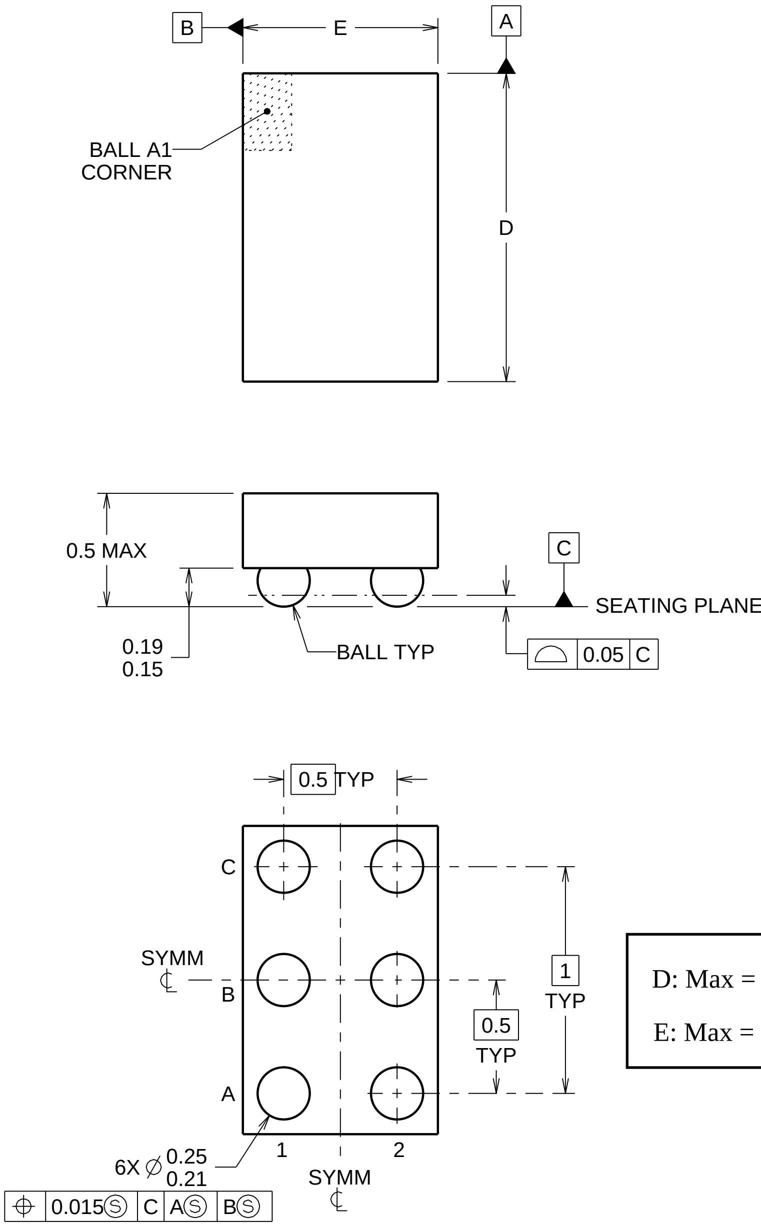
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

4212038/B 07/13

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments



D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

4219524/A 06/2014

NOTES:

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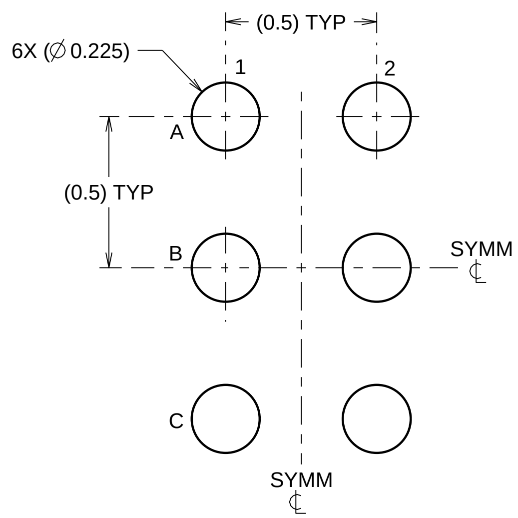
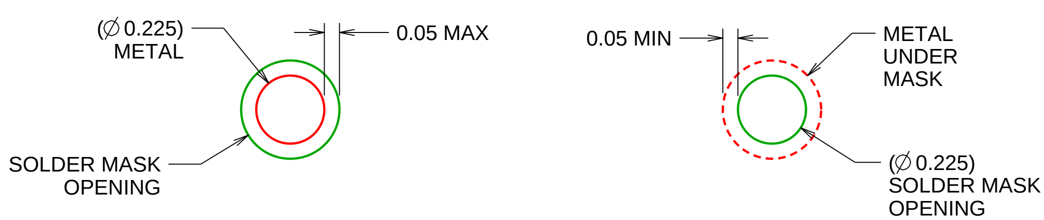
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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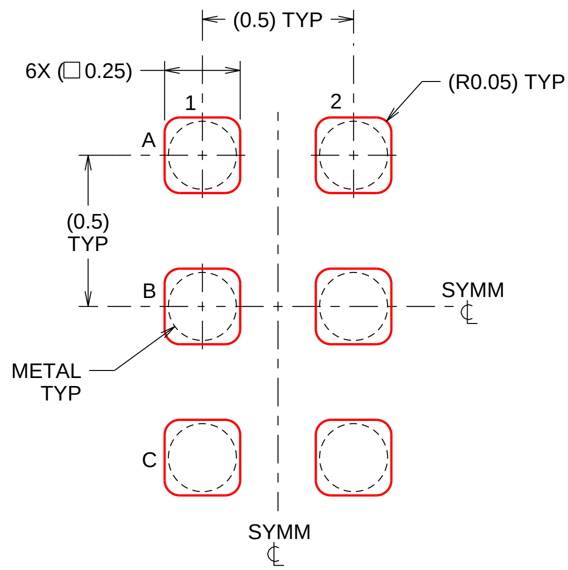
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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