TEXAS INSTRUMENTS
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# Ultra-Low Supply-Current/Supply-Voltage Supervisory Circuits

## FEATURES

- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Precision Supply Voltage Supervision Range: 0.9 V, 1.2 V, 1.5 V, 1.6 V, 2 V, and 3.3 V**
- **High Trip-Point Accuracy: 0.75%**
- **Supply Current of 1.2 μA (Typ)**
- **$\overline{\text{RESET}}$ Defined With Input Voltages as Low as 0.4 V**
- **Power-On Reset Generator With a Delay Time of 130 ms**
- **Push/Pull or Open-Drain $\overline{\text{RESET}}$ Outputs**
- **SOT23-6 Package**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## APPLICATIONS

- **Applications Using Low-Power DSPs, Microcontrollers, or Microprocessors**
- **Portable- and Battery-Powered Equipment**
- **Intelligent Instruments**
- **Wireless Communication Systems**
- **Industrial Equipment**
- **Notebook/Desktop Computers**

## DESCRIPTION

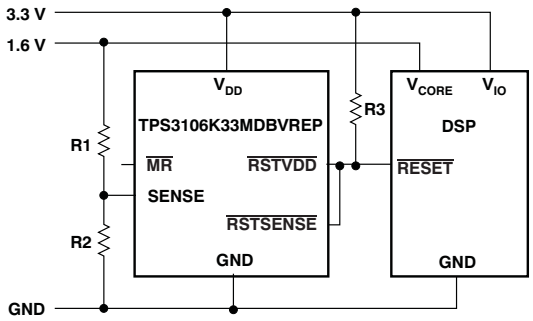
The TPS310x and TPS311x families of supervisory circuits provide circuit initialization and timing supervision, primarily for DSP and processor-based systems.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage ($V_{DD}$) becomes higher than 0.4 V. Thereafter, the supervisory circuit monitors $V_{DD}$ and keeps the $\overline{\text{RESET}}$ output active as long as $V_{DD}$ remains below the threshold voltage ($V_{IT}$). An internal timer delays the return of the output to the inactive state to ensure proper system reset. The delay time starts after $V_{DD}$ has risen above $V_{IT}$. When $V_{DD}$ drops below $V_{IT}$, the output becomes active again.

All the devices of this family have a fixed-sense threshold voltage ($V_{IT}$) set by an internal voltage divider.

The TPS3103 and TPS3106 have an active-low, open-drain $\overline{\text{RESET}}$ output. The TPS3110 has an active-low push/pull $\overline{\text{RESET}}$.

The product spectrum is designed for supply voltages of 0.9 V up to 3.3 V. The circuits are available in SOT23-6 packages. The TPS31xx family is characterized for operation over a temperature range of –55°C to 125°C.



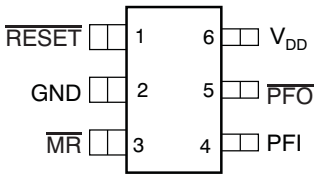

**Typical Application Circuit**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

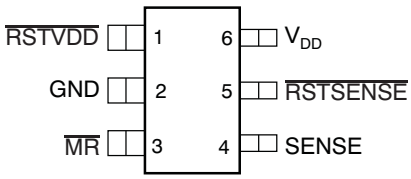
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PIN DESCRIPTIONS

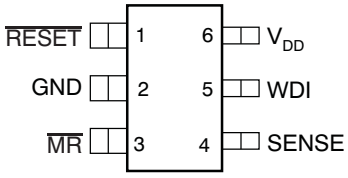
**TPS3103**
**DBV PACKAGE**
**(TOP VIEW)**




**TPS3106**
**DBV PACKAGE**
**(TOP VIEW)**




**TPS3110**
**DBV PACKAGE**
**(TOP VIEW)**




## TERMINAL FUNCTIONS

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| NAME | DEVICE | NO. | |
| GND | All | 2 | Ground |
| $\overline{MR}$ | All | 3 | Manual reset input. Pull low to force a reset. $\overline{RESET}$ remains low as long as $\overline{MR}$ is low and for the timeout period after $\overline{MR}$ goes high. Leave unconnected or connect to $V_{DD}$ when unused. |
| PFI | TPS3103 | 4 | Power-fail input. Compares to 0.551 V with no additional delay. Connect to $V_{DD}$ if not used. |
| $\overline{PFO}$ | TPS3103 | 5 | Power-fail output. Goes high when voltage at PFI rises above 0.551 V. |
| $\overline{RESET}$ | TPS3103, TPS3110 | 1 | Active-low reset output. Either push-pull or open-drain output stage. |
| $\overline{RSTSENSE}$ | TPS3106 | 5 | Active-low reset output. Logic level at $\overline{RSTSENSE}$ only depends on the voltage at SENSE and the status of $\overline{MR}$. |
| $\overline{RSTVDD}$ | TPS3106 | 1 | Active-low reset output. Logic level at $\overline{RSTVDD}$ only depends on the voltage at $V_{DD}$ and the status of $\overline{MR}$. |
| SENSE | TPS3106, TPS3110 | 4 | Sense. A reset is asserted if the voltage at SENSE is lower than 0.551 V. Connect to $V_{DD}$ if unused. |
| $V_{DD}$ | All | 6 | Supply voltage. Powers the device and monitors its own voltage. |
| WDI | TPS3110 | 5 | Watchdog timer input. If WDI remains high or low longer than the time-out period, reset is triggered. The timer clears when reset is asserted or when WDI sees a rising edge or a falling edge. |

## ORDERING INFORMATION(1)

| ORDERABLE PART NUMBER | NOMINAL SUPPLY VOLTAGE | THRESHOLD VOLTAGE, $V_{IT}$(2) | SYMBOL |
|---|---|---|---|
| TPS3103E12MDBVREP(3) | 1.2 V | 1.142 V | TBD |
| TPS3103E15MDBVREP(3) | 1.5 V | 1.434 V | TBD |
| TPS3103H20MDBVREP(3) | 2 V | 1.84 V | TBD |
| TPS3103K33MDBVREP(3) | 3.3 V | 2.941 V | TBD |
| TPS3106E09MDBVREP(3) | 0.9 V | 0.86 V | TBD |
| TPS3106E16MDBVREP(3) | 1.6 V | 1.521 V | TBD |
| TPS3106K33MDBVREP | 3.3 V | 2.941 V | AAVM |
| TPS3110E09MDBVREP(3) | 0.9 V | 0.86 V | TBD |
| TPS3110E12MDBVREP(3) | 1.2 V | 1.142 V | TBD |
| TPS3110E15MDBVREP(3) | 1.5 V | 1.434 V | TBD |
| TPS3110K33MDBVREP(3) | 3.3 V | 2.941 V | TBD |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Custom threshold voltages are available. Minimum order quantities apply. Contact TI for details and availability.
(3) Product Preview

### AVAILABLE OPTIONS

| DEVICE | $\overline{\text{RESET}}$ OUTPUT | $\overline{\text{RSTSENSE}}$, $\overline{\text{RSTVDD}}$ OUTPUT | SENSE INPUT | WDI INPUT | $\overline{\text{PFO}}$ OUTPUT |
|---|---|---|---|---|---|
| TPS3103 | Open drain | | | | Open drain |
| TPS3106 | | Open drain | ü | | |
| TPS3110 | Push-pull | | ü | ü | |

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | VALUE | UNIT |
|---|---|---|
| Supply voltage range, $V_{DD}$(2) | –0.3 to 3.6 | V |
| All other pins(2) | –0.3 to 3.6 | V |
| Maximum low output current, $I_{OL}$ | 5 | mA |
| Maximum high output current, $I_{OH}$ | –5 | mA |
| Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{DD}$) | ±10 | mA |
| Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{DD}$) | ±10 | mA |
| Operating temperature range, $T_A$ | –55 to 125 | °C |
| Storage temperature range, $T_{stg}$ | –65 to 150 | °C |
| Soldering temperature | 260 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 3.6 V for more than t = 1000h continuously

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{DD}$(1) | 0.4 | 3.3 | V |
| Input voltage, $V_I$ | 0 | $V_{DD}$ + 0.3 | V |
| High-level input voltage, $V_{IH}$ at $\overline{\text{MR}}$, WDI | $0.7 \times V_{DD}$ | | V |
| Low-level input voltage, $V_{IL}$ at $\overline{\text{MR}}$, WDI | | $0.3 \times V_{DD}$ | V |
| Input transition rise and fall rate at $\Delta t/\Delta V$ at $\overline{\text{MR}}$, WDI | | 100 | ns/V |
| Operating temperature, $T_A$ | –55 | 125 | °C |

(1) For proper operation of SENSE, PFI, and WDI functions: $V_{DD} \geq 0.8$ V.

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | | $V_{DD}$ = 3.3 V, $I_{OH}$ = –3 mA | $0.8 \times V_{DD}$ | | | V |
| | | | $V_{DD}$ = 1.8 V, $I_{OH}$ = –2 mA | | | | |
| | | | $V_{DD}$ = 1.5 V, $I_{OH}$ = –1 mA | | | | |
| | | | $V_{DD}$ = 0.9 V, $I_{OH}$ = –0.4 mA | | | | |
| | | | $V_{DD}$ = 0.5 V, $I_{OH}$ = –5 µA | $0.7 \times V_{DD}$ | | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{DD}$ = 3.3 V, $I_{OL}$ = 3 mA | | | 0.3 | V |
| | | | $V_{DD}$ = 1.5 V, $I_{OL}$ = 2 mA | | | | |
| | | | $V_{DD}$ = 1.2 V, $I_{OL}$ = 1 mA | | | | |
| | | | $V_{DD}$ = 0.9 V, $I_{OL}$ = 500 µA | | | | |
| $V_{OL}$ | Low-level output voltage | $\overline{\text{RESET}}$ only | $V_{DD}$ = 0.4 V, $I_{OL}$ = 5 µA | | | 0.1 | V |

## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT-}$ | Negative-going input threshold voltage(1) | TPS31xxE09 | $T_A$ = 25°C | 0.854 | 0.86 | 0.866 | V |
| | | TPS31xxE12 | | 1.133 | 1.142 | 1.151 | |
| | | TPS31xxE15 | | 1.423 | 1.434 | 1.445 | |
| | | TPS31xxE16 | | 1.512 | 1.523 | 1.534 | |
| | | TPS31xxH20 | | 1.829 | 1.843 | 1.857 | |
| | | TPS31xxK33 | $T_A$ = 25°C | 2.905 | 2.941 | 2.970 | |
| | | | $T_A$ = Full Range | 2.867 | | 3.005 | |
| $V_{IT-(S)}$ | Negative-going input threshold voltage(2) | SENSE, PFI | $V_{DD} \geq 0.8$ V, $T_A$ = 25°C | 0.540 | 0.551 | 0.569 | V |
| | | | $V_{DD} \geq 0.8$ V, $T_A$ = Full Range | 0.530 | 0.551 | 0.575 | |
| $V_{HYS}$ | Hysteresis at $V_{DD}$ input | | 0.8 V ≤ $V_{IT}$ < 1.5 V | | 20 | | mV |
| | | | 1.6 V ≤ $V_{IT}$ < 2.4 V | | 30 | | |
| | | | 2.5 V ≤ $V_{IT}$ < 3.3 V | | 60 | | |
| $T_{(K)}$ | Temperature coefficient of $V_{IT-}$, PFI, SENSE | | $T_A$ = –55°C to 125°C | | –0.012 | –0.019 | %/K |
| $V_{HYS}$ | Hysteresis at SENSE, PFI input | | $V_{DD} \geq 0.8$ V | | 15 | | mV |
| $I_{IH}$ | High-level input current | $\overline{MR}$ | $\overline{MR}$ = $V_{DD}$, $V_{DD}$ = 3.3 V | –30 | | 25 | nA |
| | | SENSE, PFI, WDI | SENSE, PFI, WDI = $V_{DD}$, $V_{DD}$ = 3.3 V | –25 | | 25 | |
| $I_{IL}$ | Low-level input current | $\overline{MR}$ | $\overline{MR}$ = 0 V, $V_{DD}$ = 3.3 V | –47 | –33 | –25 | µA |
| | | SENSE, PFI, WDI | SENSE, PFI, WDI = 0 V, $V_{DD}$ = 3.3 V | –25 | | 25 | nA |
| $I_{OH}$ | High-level output current at $\overline{RESET}$(3) | Open drain | $V_{DD}$ = $V_{IT}$ + 0.2 V, $V_{OH}$ = 3.3 V | | | 200 | nA |
| $I_{DD}$ | Supply current | | $V_{DD}$ > $V_{IT}$ (average current), $V_{DD}$ < 1.8 V | | 1.2 | 3 | µA |
| | | | $V_{DD}$ > $V_{IT}$ (average current), $V_{DD}$ > 1.8 V | | 2 | 4.5 | |
| | | | $V_{DD}$ < $V_{IT}$, $V_{DD}$ < 1.8 V | | | 29 | |
| | | | $V_{DD}$ < $V_{IT}$, $V_{DD}$ > 1.8 V | | | 32 | |
| | Internal pullup resistor at $\overline{MR}$ | | | 70 | 100 | 130 | kΩ |
| $C_I$ | Input capacitance at $\overline{MR}$, SENSE, PFI, WDI | | $V_I$ = 0 V to $V_{DD}$ | | 1 | | pF |

(1) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed close to the supply terminals.
(2) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed close to the supply terminals.
(3) Also refers to $\overline{RSTVDD}$ and $\overline{RSTSENSE}$.

## SWITCHING CHARACTERISTICS

$R_L$ = 1 MΩ, $C_L$ = 50 pF, and $T_A$ = –55°C to 125°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_d$ | Delay time | | $V_{DD} \geq 1.1 \times V_{IT}$, $\overline{MR}$ = 0.7 × $V_{DD}$, See Timing Diagrams | 65 | 130 | 195 | ms |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | $V_{DD}$ to $\overline{RESET}$ or $\overline{RSTVDD}$ delay | $V_{IH}$ = 1.1 × $V_{IT}$, $V_{IL}$ = 0.9 × $V_{IT}$ | | | 40 | µs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | SENSE to $\overline{RESET}$ or $\overline{RSTSENSE}$ delay | $V_{DD} \geq 0.8$ V, $V_{IH}$ = 1.1 × $V_{IT}$, $V_{IL}$ = 0.9 × $V_{IT}$ | | | 40 | µs |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | PFI to $\overline{PFO}$ delay | $V_{DD} \geq 0.8$ V, $V_{IH}$ = 1.1 × $V_{IT}$, $V_{IL}$ = 0.9 × $V_{IT}$ | | | 40 | µs |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | PFI to $\overline{PFO}$ delay | $V_{DD} \geq 0.8$ V, $V_{IH}$ = 1.1 × $V_{IT}$, $V_{IL}$ = 0.9 × $V_{IT}$ | | | 300 | µs |

## SWITCHING CHARACTERISTICS (continued)

$R_L$ = 1 MΩ, $C_L$ = 50 pF, and $T_A$ = –55°C to 125°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation delay time, high_to_low-level output | $\overline{MR}$ to $\overline{RESET}$, $\overline{RSTVDD}$, $\overline{RSTSENSE}$ delay | $V_{DD} \geq 1.1 \times V_{IT}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$ | | 1 | 5 | µs |

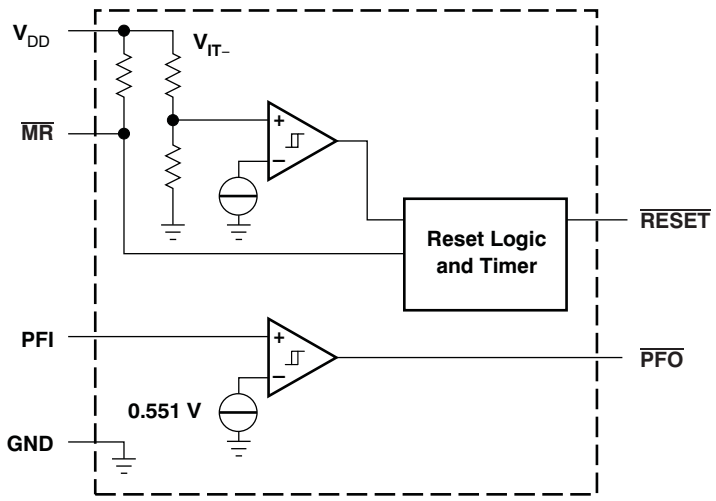
## TIMING REQUIREMENTS

$R_L$ = 1 MΩ, $C_L$ = 50 pF, and $T_A$ = –55°C to 125°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{T(OUT)}$ | Time-out period | at WDI | $V_{DD} \geq 0.85$ V | 0.55 | 1.1 | 1.65 | s |
| $t_W$ | Pulse width | at $V_{DD}$ | $V_{IH} = 1.1 \times V_{IT}$, $V_{IL} = 0.9 \times V_{IT–}$, $V_{IT–} = 0.86$ V | 20 | | | µs |
| | | at $\overline{MR}$ | $V_{DD} \geq V_{IT} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$ | 0.1 | | | |
| | | at SENSE | $V_{DD} \geq V_{IT}$, $V_{IH} = 1.1 \times V_{IT – (S)}$, $V_{IL} = 0.9 \times V_{IT – (S)}$ | 20 | | | |
| | | at PFI | $V_{DD} \geq 0.85$ V, $V_{IH} = 1.1 \times V_{IT – (S)}$, $V_{IL} = 0.9 \times V_{IT – (S)}$ | 20 | | | |
| | | at WDI | $V_{DD} \geq V_{IT}$, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$ | 0.3 | | | |

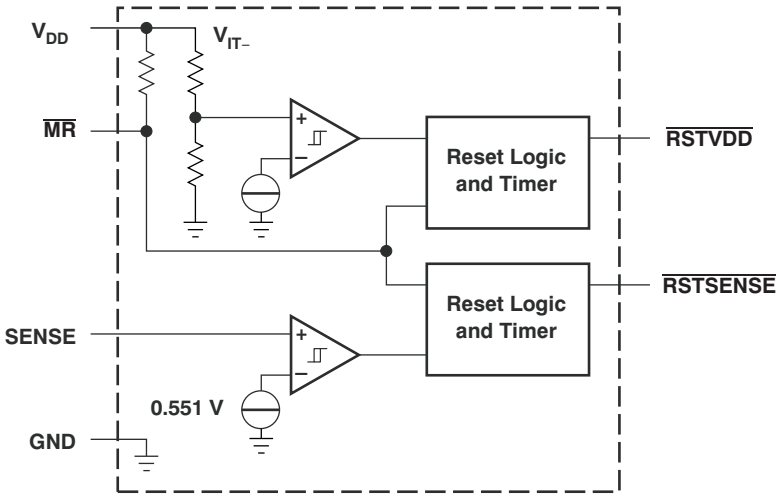
## FUNCTIONAL BLOCK DIAGRAMS

**TPS3103**



## FUNCTIONAL BLOCK DIAGRAMS (continued)

TPS3106




TPS3110

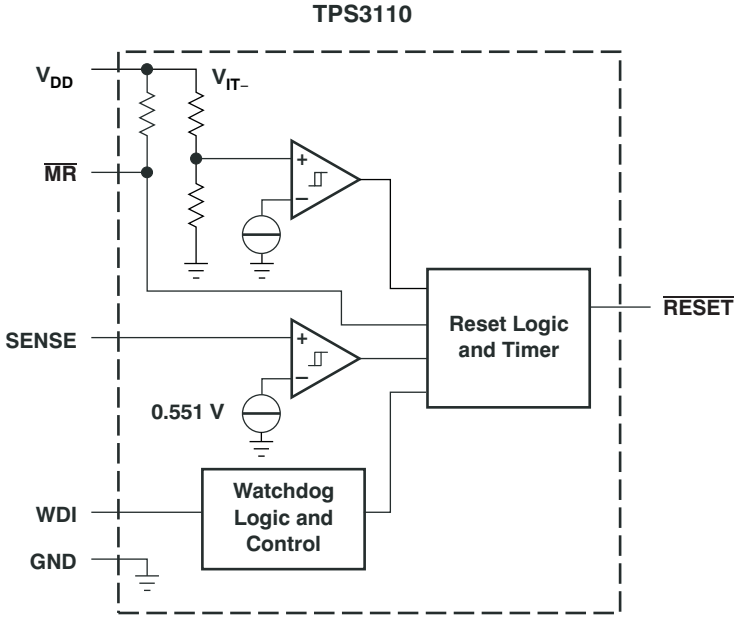



**Table 1. TPS3103 FUNCTION TABLE**

| $\overline{MR}$ | $V_{(PFI)}$ > 0.551 V | $V_{DD}$ > $V_{IT}$ | $\overline{RESET}$ | $\overline{PFO}$ |
|---|---|---|---|---|
| L | 0 | X(1) | L | L |
| L | 1 | X | L | H |
| H | 0 | 0 | L | L |
| H | 0 | 1 | H | L |
| H | 1 | 0 | L | H |
| H | 1 | 1 | H | H |

(1) X = Don't care

**Table 2. TPS3106 FUNCTION TABLE**

| $\overline{MR}$ | $V_{(SENSE)}$ > 0.551 V | $V_{DD} > V_{IT}$ | $\overline{RSTVDD}$ | $\overline{RSTSENSE}$ |
|---|---|---|---|---|
| L | X(1) | X | L | L |
| H | 0 | 0 | L | L |
| H | 0 | 1 | H | L |
| H | 1 | 0 | L | H |
| H | 1 | 1 | H | H |

(1) X = Don't care

**Table 3. TPS3110 FUNCTION TABLE(1)**

| $\overline{MR}$ | $V_{(SENSE)}$ > 0.551 V | $V_{DD} > V_{IT}$ | $\overline{RESET}$ |
|---|---|---|---|
| L | X(2) | X | L |
| H | 0 | 0 | L |
| H | 0 | 1 | L |
| H | 1 | 0 | L |
| H | 1 | 1 | H |

(1) Function of watchdog timer not shown
(2) X = Don't care

## TIMING DIAGRAMS

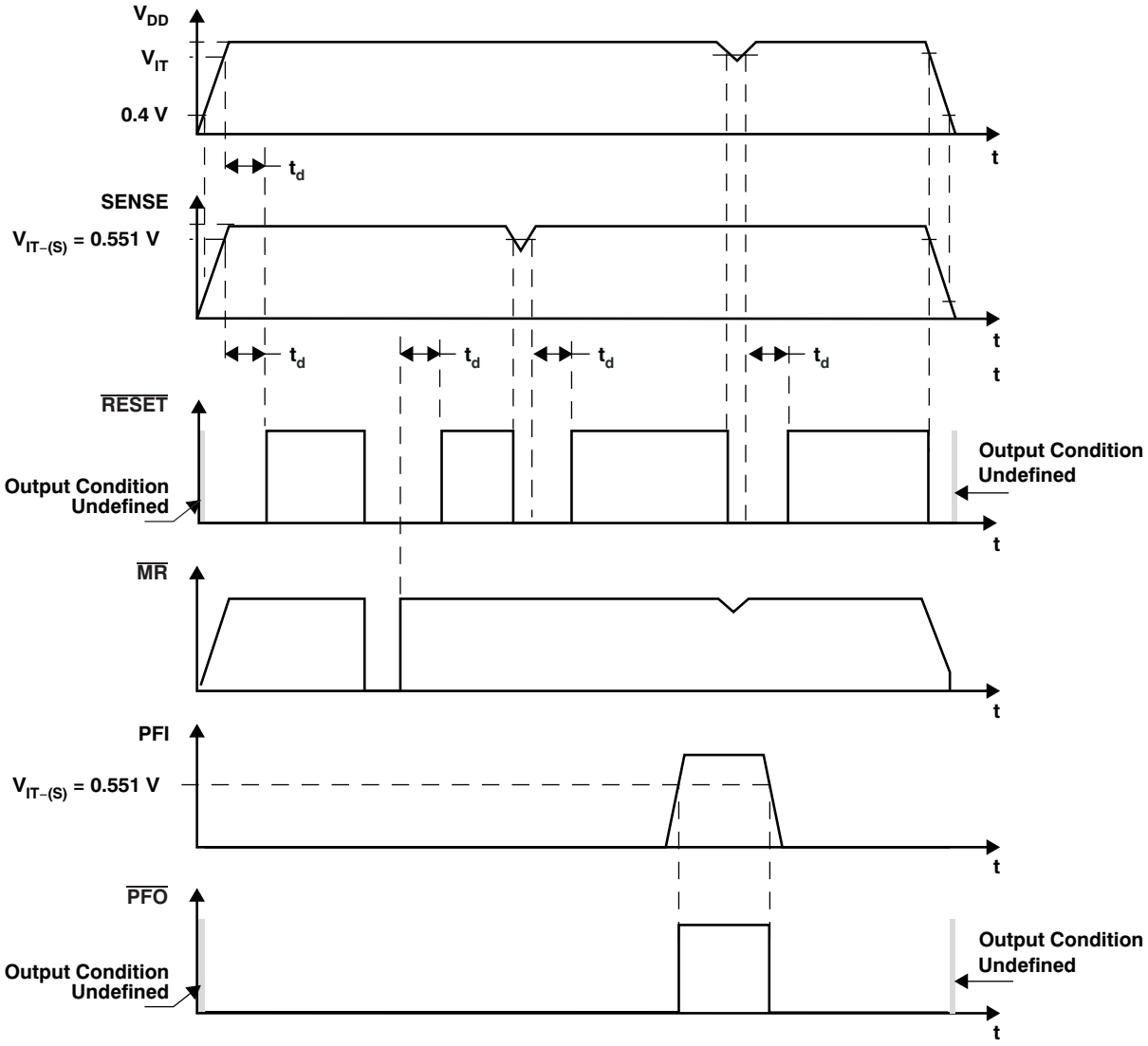



**Figure 1. TPS3103 Timing**

## TIMING DIAGRAMS (continued)

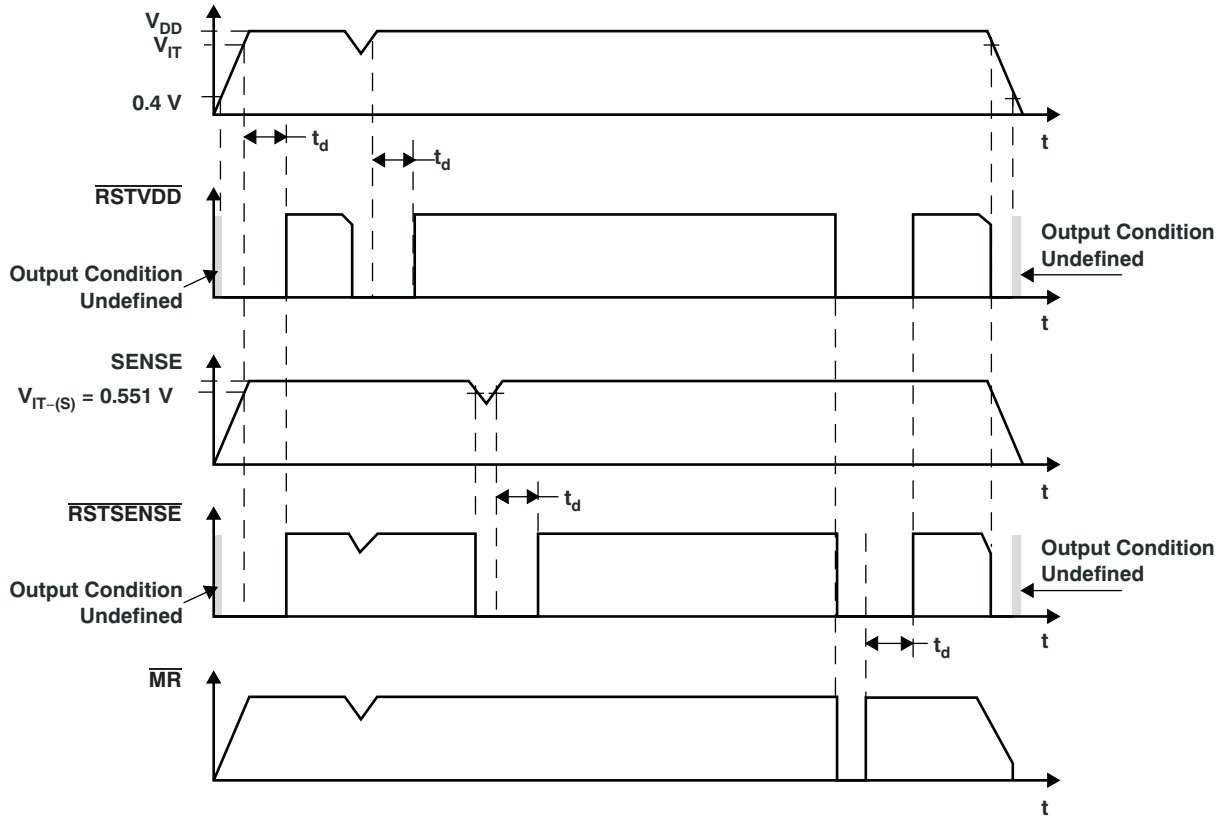



**Figure 2. TPS3106 Timing**

## TIMING DIAGRAMS (continued)

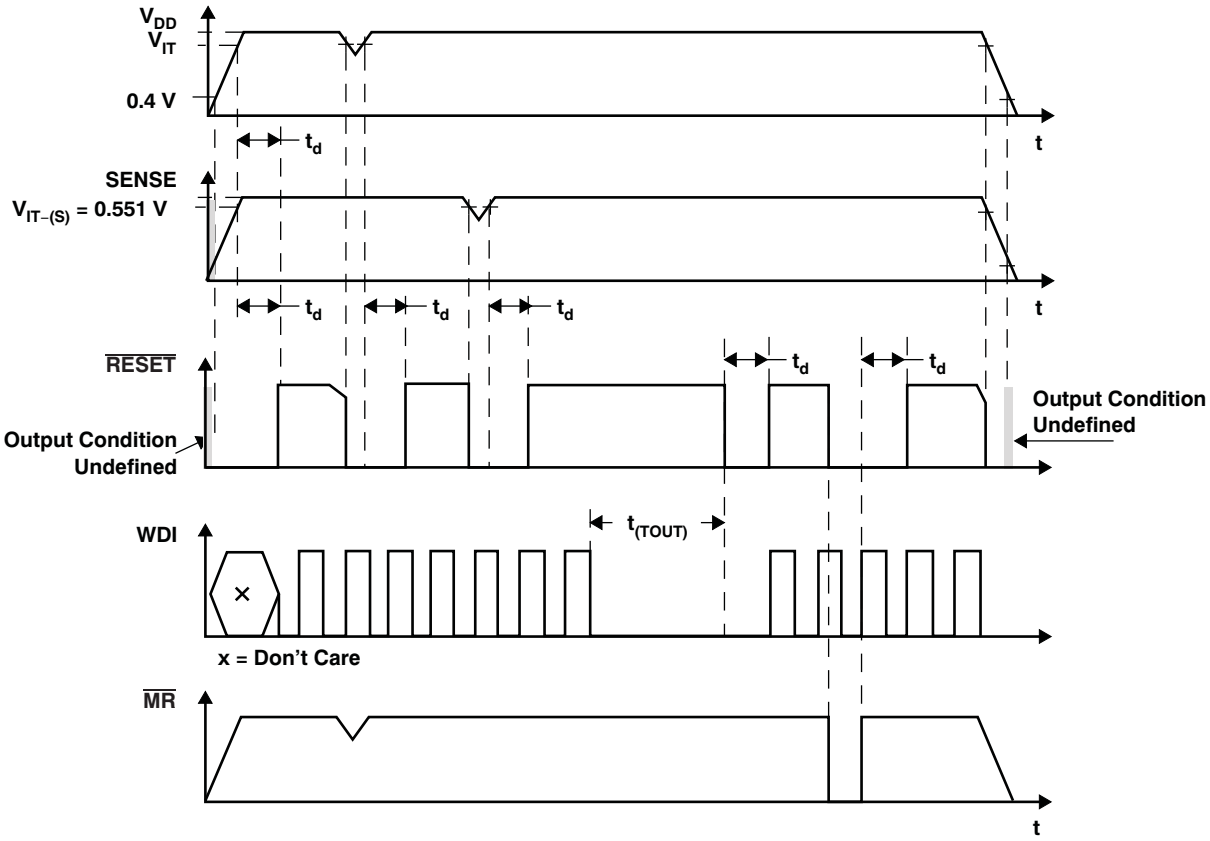



**Figure 3. TPS3110 Timing**

## TYPICAL CHARACTERISTICS

**TPS3110E09**
**SUPPLY CURRENT**
**vs**
**SUPPLY VOLTAGE**

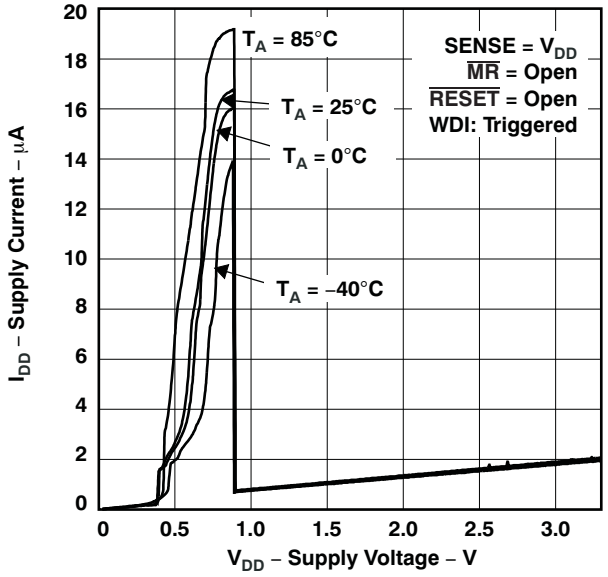



Figure 4.

**TPS3110E09**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**

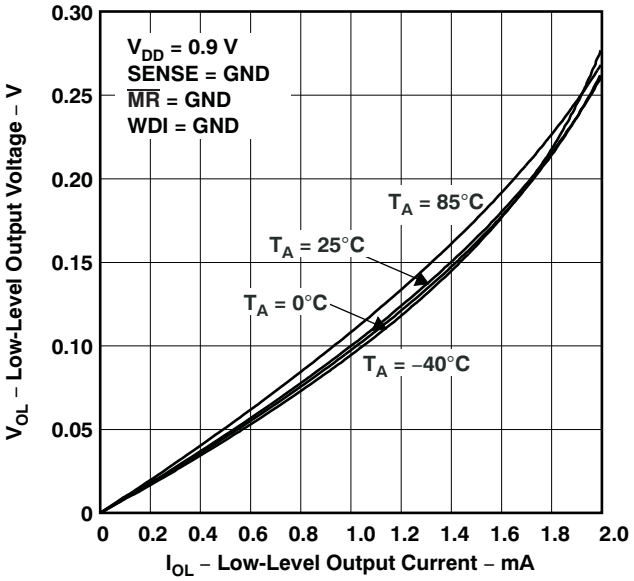



Figure 5.

**TPS3110E09**
**LOW-LEVEL OUTPUT VOLTAGE**
**vs**
**LOW-LEVEL OUTPUT CURRENT**

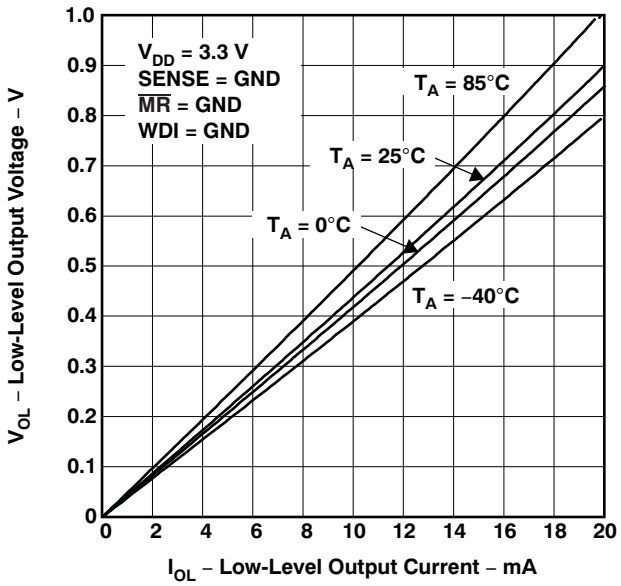



Figure 6.

**TPS3110E09**
**HIGH-LEVEL OUTPUT VOLTAGE**
**vs**
**HIGH-LEVEL OUTPUT CURRENT**

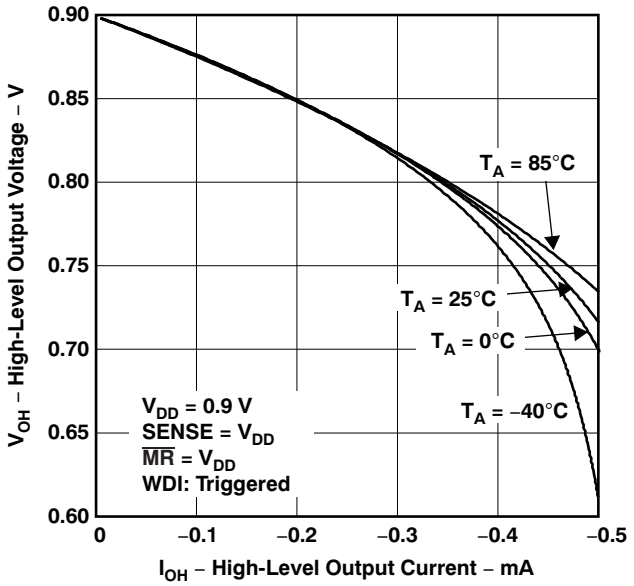



Figure 7.

## TYPICAL CHARACTERISTICS (continued)

TPS3110K33
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

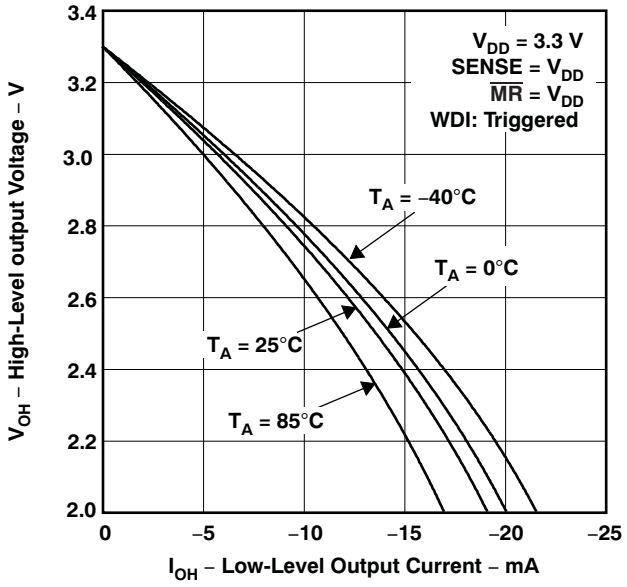



Figure 8.

MINIMUM PULSE DURATION AT $V_{DD}$
vs
THRESHOLD OVERDRIVE VOLTAGE

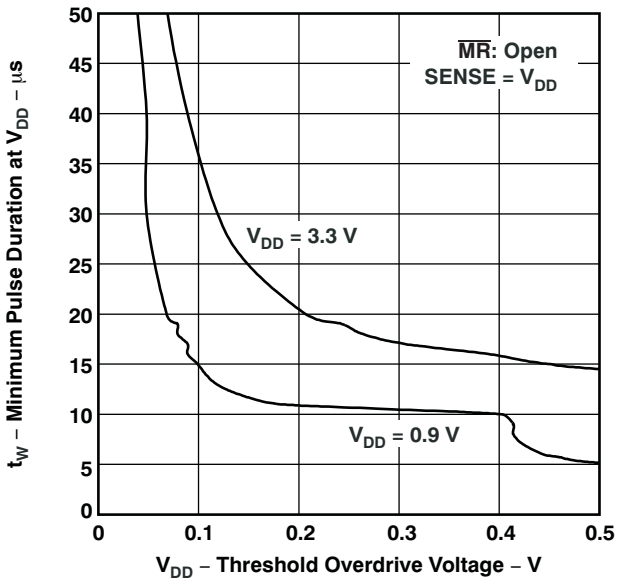



Figure 9.

NORMALIZED THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

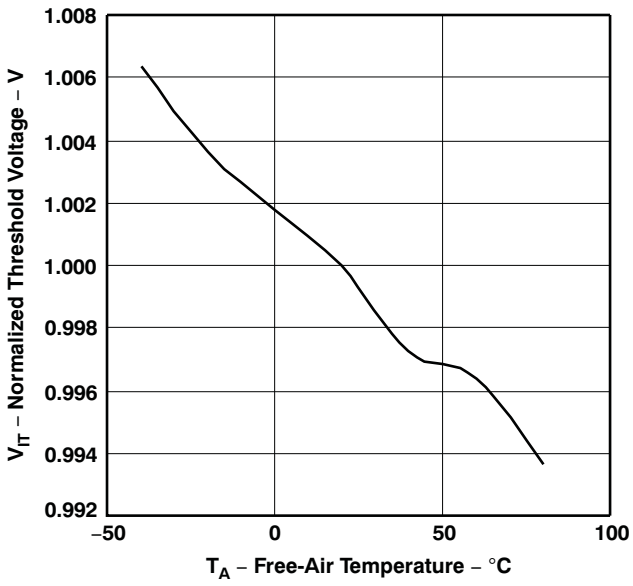



Figure 10.

## APPLICATION INFORMATION

The TPS31xx family has a quiescent current in the 1-μA to 2-μA range. When $\overline{\text{RESET}}$ is active, triggered by the voltage monitored at $V_{DD}$, the quiescent current increases to about 20 μA (see the Electrical Characteristics).

In some applications, it is necessary to minimize the quiescent current even during the reset period. This is especially true when the voltage of a battery is supervised and the $\overline{\text{RESET}}$ is used to shut down the system or for an early warning. In this case, the reset condition lasts for a longer period of time. The current drawn from the battery should almost be zero, especially when the battery is discharged.

For this kind of application, either the TPS3103 or TPS3106 is a good fit. To minimize current consumption, select a version where the threshold voltage is lower than the voltage monitored at $V_{DD}$. The TPS3106 has two reset outputs. One output ($\overline{\text{RSTVDD}}$) is triggered from the voltage monitored at $V_{DD}$. The other output ($\overline{\text{RSTSENSE}}$) is triggered from the voltage monitored at SENSE. In the application shown in Figure 11, the TPS3106E09 is used to monitor the input voltage of two NiCd or NiMH cells. The threshold voltage ($V_{(TH)}$ = 0.86 V) was chosen as low as possible to ensure that the supply voltage is always higher than the threshold voltage at $V_{DD}$. The voltage of the battery is monitored using the SENSE input. The voltage divider was calculated to assert a reset using the $\overline{\text{RSTSENSE}}$ output at 2 × 0.8 V = 1.6 V.

$$R1 = R2 \times \left( \frac{V_{TRIP}}{V_{IT(S)}} - 1 \right) \quad (1)$$

where:

$V_{TRIP}$ is the voltage of the battery at which a reset is asserted and

$V_{IT(S)}$ is the threshold voltage at SENSE = 0.551 V.

R1 was chosen for a resistor current in the 1-μA range.

With $V_{TRIP}$ = 1.6 V:

$R1 \approx 1.9 \times R2$

R1 = 820 kΩ, R2 = 430 kΩ

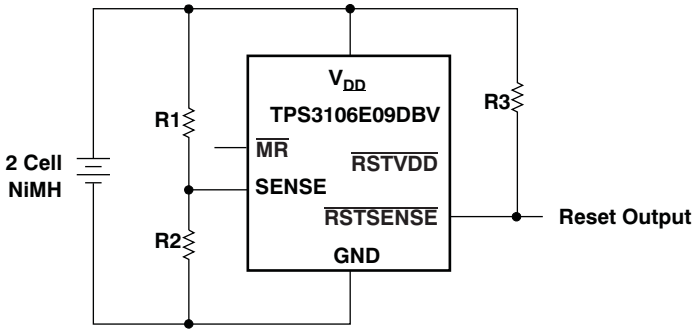



**Figure 11. Battery Monitoring with 3-μA Supply Current for Device and Resistor Divider**

## APPLICATION INFORMATION (continued)

### Watchdog

The TPS3110 device integrates a watchdog timer that must be periodically triggered by a positive or negative transition of WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $\overline{\text{RESET}}$ becomes active for the time period ($t_D$). This event also reinitializes the watchdog timer.

### Manual Reset ($\overline{\text{MR}}$)

Many μC-based products require manual-reset capability, allowing an operator or logic circuitry to initiate a reset. Logic low at $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low and for a time period ($t_D$) after $\overline{\text{MR}}$ returns high. The input has an internal 100-kΩ pullup resistor, so it can be left open if it is unused.

Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual reset function. External debounce is not required. If $\overline{\text{MR}}$ is driven from long cables or if the device is used in noisy environments, connecting a 0.1-μF capacitor from $\overline{\text{MR}}$ to GND provides additional noise immunity.

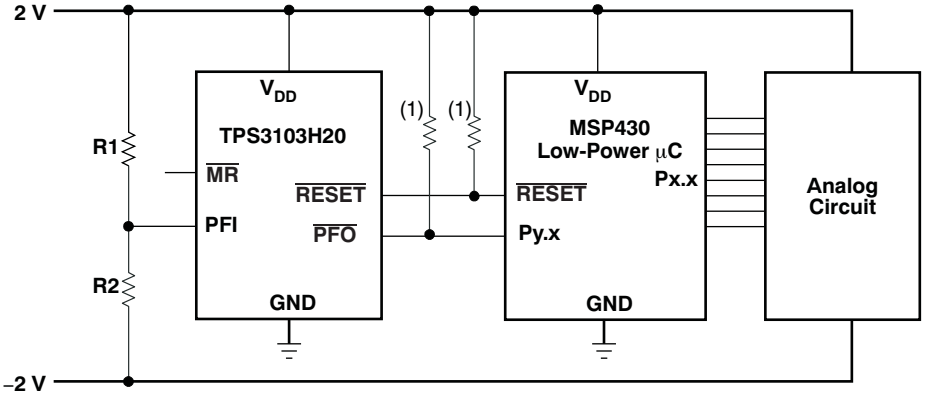
### PFI, $\overline{\text{PFO}}$

The TPS3103 has an integrated power-fail input (PFI) comparator with a separate open-drain power-fail output ($\overline{\text{PFO}}$). The PFI and $\overline{\text{PFO}}$ can be used for low-battery detection, power-fail warning, or for monitoring a power supply other than the main supply.

An additional comparator is provided to monitor voltages other than the nominal supply voltage. The PFI is compared with an internal voltage reference of 0.551 V. If the input voltage falls below the power-fail threshold ($V_{IT\ -\ (S)}$), the $\overline{\text{PFO}}$ goes low. If it goes above 0.551 V plus approximately 15-mV hysteresis, the output returns to high. By connecting two external resistors, it is possible to supervise any voltage above 0.551 V. The sum of both resistors should be approximately 1 MΩ, to minimize power consumption and to ensure that the current into the PFI pin can be neglected, compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of sensed voltage. If the power-fail comparator is unused, connect PFI to GND and leave $\overline{\text{PFO}}$ unconnected. For proper operation of the PFI comparator, the supply voltage ($V_{DD}$) must be higher than 0.8 V.

### SENSE

The voltage at the SENSE input is compared with a reference voltage of 0.551 V. If the voltage at SENSE falls below the sense-threshold ($V_{IT-(S)}$), reset is asserted. On the TPS3106, a dedicated $\overline{\text{RSTSENSE}}$ output is available. On the TPS3110, the logic signal from SENSE is OR-wired with the logic signal from $V_{DD}$ or $\overline{\text{MR}}$. An internal timer delays the return of the output to the inactive state, once the voltage at SENSE goes above 0.551 V plus about 15 mV of hysteresis. For proper operation of the SENSE comparator, the supply voltage must be higher than 0.8 V.




$$V_{(NEG\_TH)} = 0.551\ V - \frac{R2}{R1}\ (V_{DD} - 0.551\ V)$$

(1) Resistor may be integrated in μC.

**Figure 12. TPS3103 Monitoring a Negative Voltage**

## APPLICATION INFORMATION (continued)

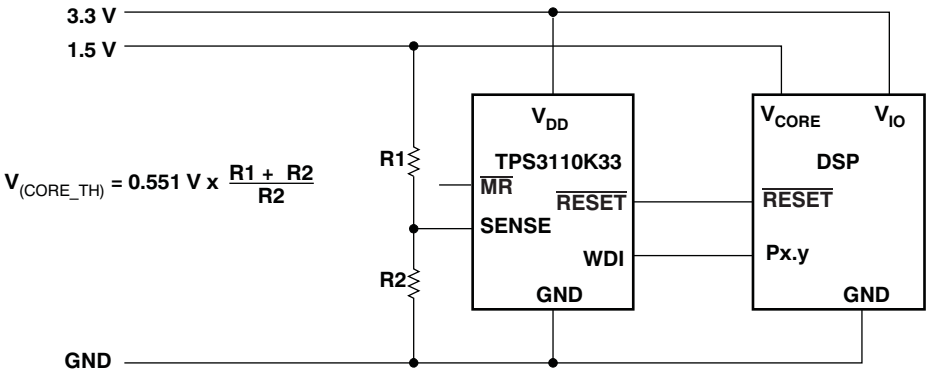



**Figure 13. TPS3110 in a DSP System Monitoring Both Supply Voltages**

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS3106K33MDBVREP | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AAVM |
| V62/06643-07XE | Active | Production | SOT-23 (DBV) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AAVM |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TPS3106-EP :**

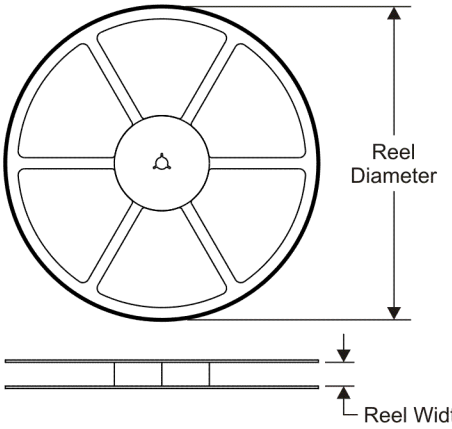
- Catalog : TPS3106

NOTE: Qualified Version Definitions:

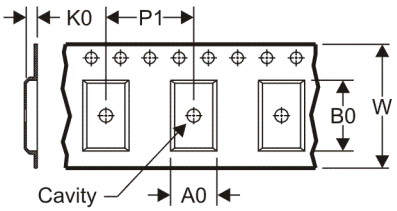
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

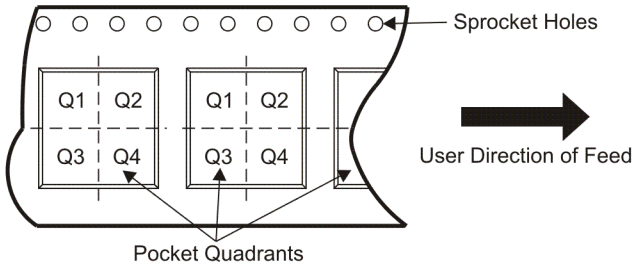



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

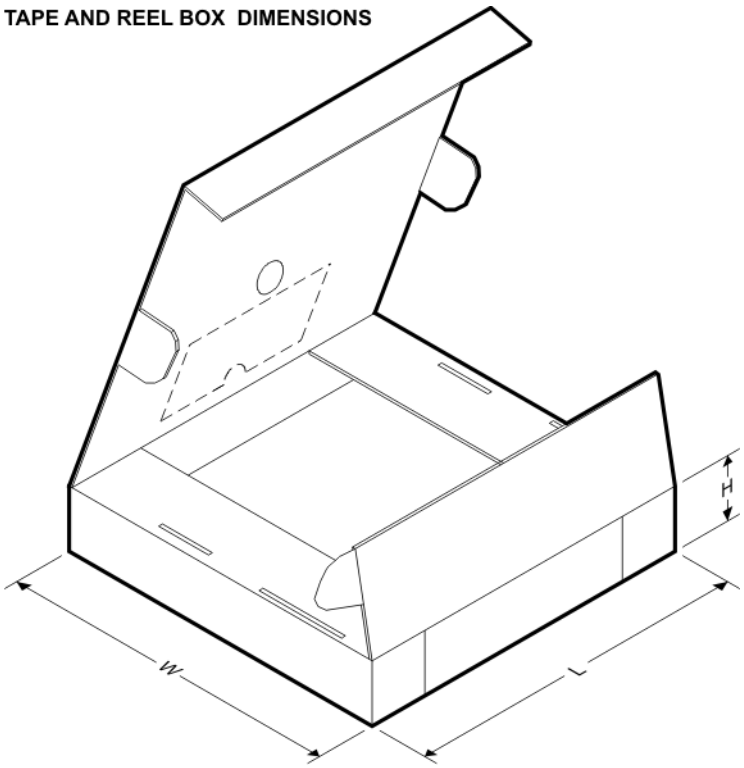
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS3106K33MDBVREP | SOT-23 | DBV | 6 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

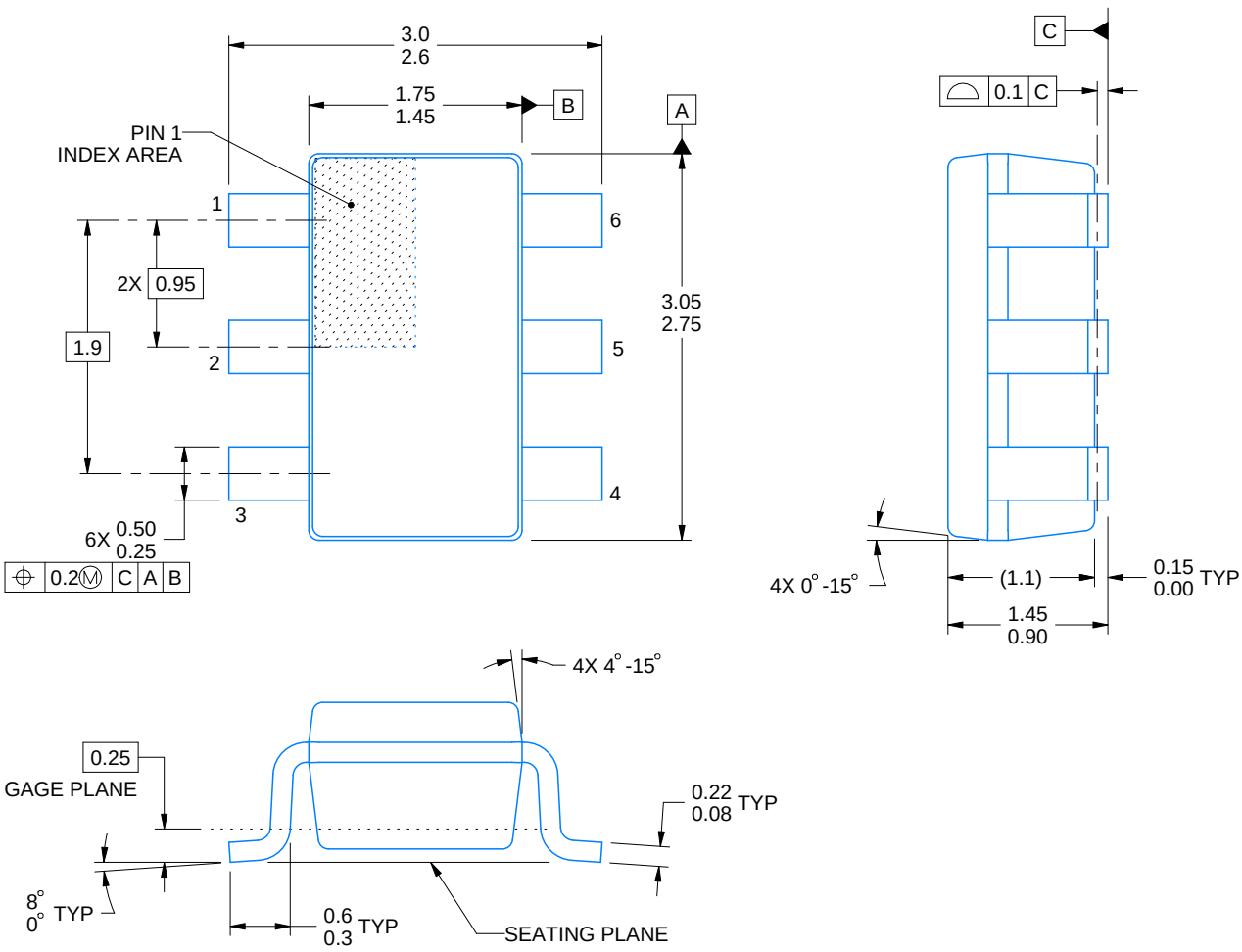
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS3106K33MDBVREP | SOT-23 | DBV | 6 | 3000 | 182.0 | 182.0 | 20.0 |

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

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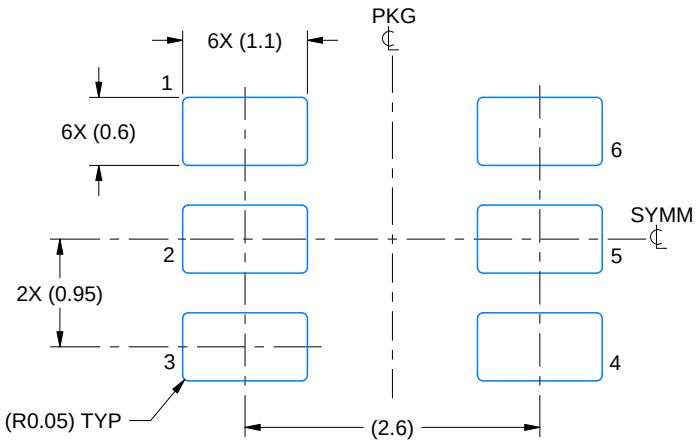
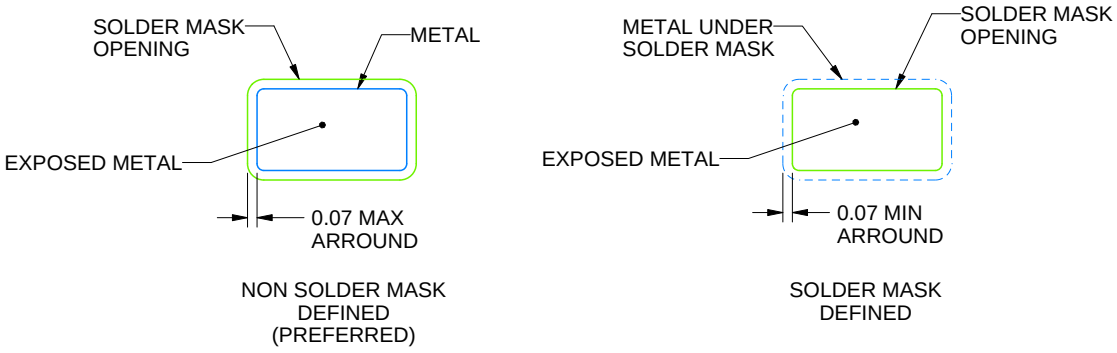
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X




SOLDER MASK DETAILS

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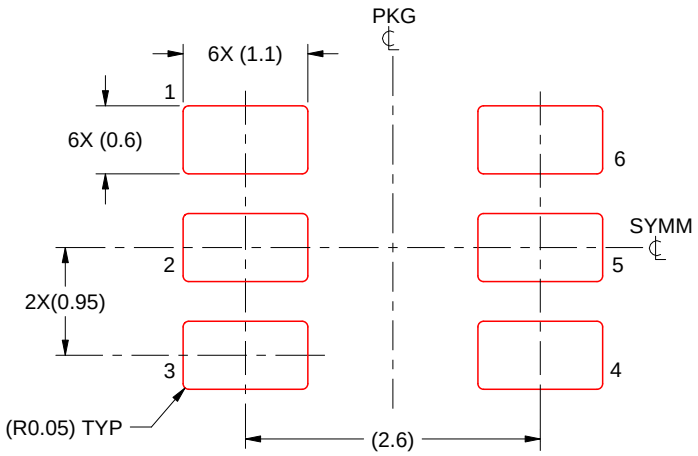
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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