

TPS3436 Nano IQ Precision Window Watchdog Timer

1 Features

- Factory programmed or user-programmable watchdog timeout
 - $\pm 10\%$ accurate timer (maximum)
 - Factory programmed close window: 1ms to 100s
- Factory programmed or user-programmable reset delay
 - $\pm 10\%$ Accurate timer (maximum)
 - Factory programmed option: 2ms to 10s
- Input voltage range: $V_{DD} = 1.04V$ to $6.0V$
- Ultra low supply current: $I_{DD} = 250nA$ (typical)
- Open-drain, push-pull; active-low outputs
- Various programmability options:
 - Watchdog enable-disable
 - Watchdog startup delay: no delay to 10s
 - Open window to close window ratio option: 1X to 511X
 - Latched output option
- MR functionality support

2 Applications

- Robot servo drive
- Mixed module (AI, AO, DI, DO)
- HVAC controller
- Electricity meter
- Infusion pump
- Surgical equipment

3 Description

The TPS3436 is an ultra-low-power consumption (250nA typical) device offering a programmable window watchdog timer.

The TPS3436 offers a high accuracy window watchdog timer with host of features for a wide variety of applications. The close window timer can be factory programmed or user programmed using an external capacitor. The open window to close window ratio can change unpremeditatedly using a combination of logic pins. The watchdog also offers unique features such as enable-disable, start-up delay.

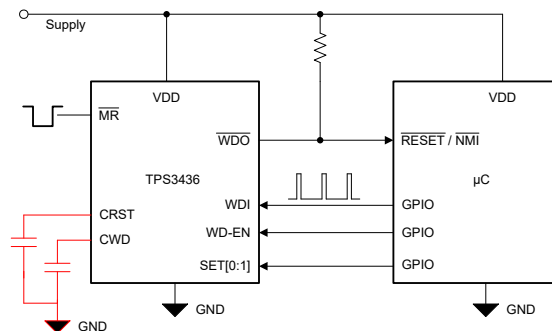
The $\overline{WDO}$ delay can be set by factory-programmed default delay settings or programmed by an external capacitor. The device also offers a latched output operation where the output is latched until the watchdog fault is cleared.

The TPS3436 provides a performance upgrade alternative to the [TPS3430](#) device family. The TPS3436 is available in small 6-pin WSON and 5-pin and 8-pin SOT-23 package.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽³⁾
TPS3436	DDF (SOT-23 8)	2.90mm × 1.60mm
TPS3436	DSE (WSON 6) ⁽²⁾	1.50mm × 1.50mm

- (1) For all available packages, see the orderable addendum at the end of the datasheet.
- (2) Package preview.
- (3) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS3436 offers various pinout options to support different features.
Choose suitable pinout based on application needs

Typical Application Circuit

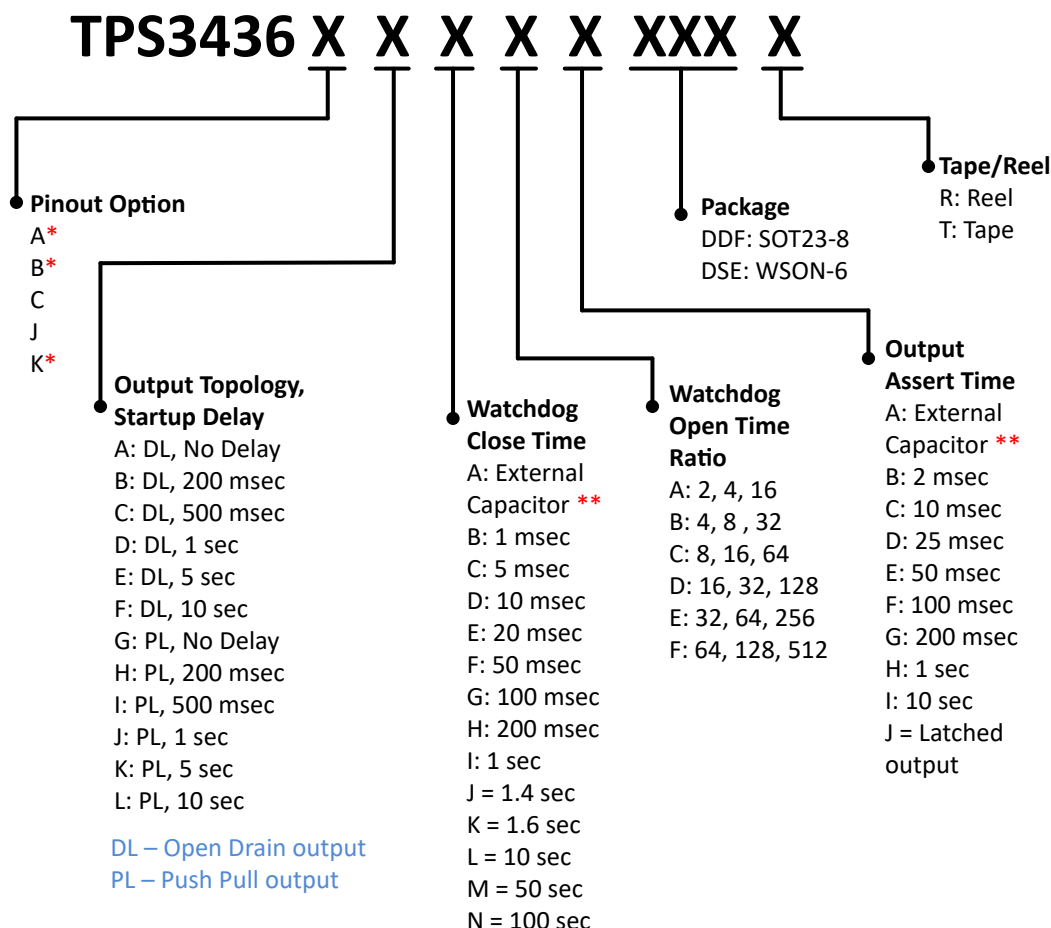


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4 Device Comparison

Figure 4-1 shows the device naming nomenclature of the TPS3436. For all possible output types, watchdog time options and output assert delay options, see Section 7 for more details. Contact TI sales representatives or on TI's E2E™ forums for detail and availability of other options.



* Pinout option supports Start up Delay settings of “No Delay” and “10 sec” only.

** Capacitor programmable time feature available with pinout options A, B & K. For fixed time and latched output features use pinout options C & J.

Refer ‘Mechanical, Packaging and Orderable Information’ section for list of released orderable. For any other orderable, contact local TI support.

Figure 4-1. Device Naming Nomenclature

TPS3436 belongs to family of pin compatible devices offering different feature sets as highlighted in Table 4-1.

Table 4-1. Pin Compatible Device Families

DEVICE	VOLTAGE SUPERVISOR	TYPE OF WATCHDOG
TPS35	Yes	Timeout
TPS36	Yes	Window
TPS3435	No	Timeout
TPS3436	No	Window

5 Pin Configuration and Functions

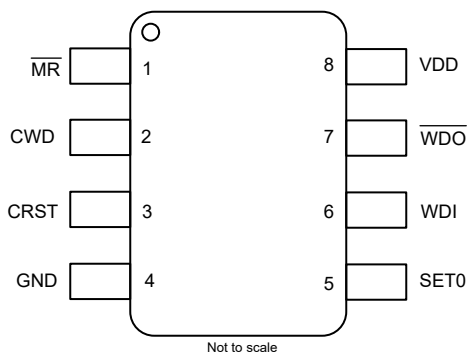


Figure 5-1. Pin Configuration Option A
DDF Package, 8-Pin SOT-23,
TPS3436 Top View

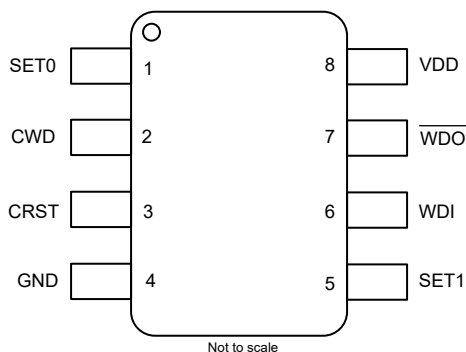


Figure 5-2. Pin Configuration Option B
DDF Package, 8-Pin SOT-23,
TPS3436 Top View

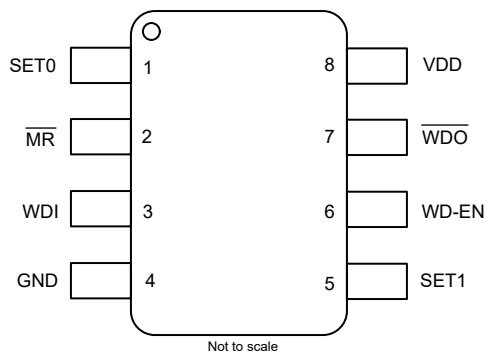


Figure 5-3. Pin Configuration Option C
DDF Package, 8-Pin SOT-23,
TPS3436 Top View

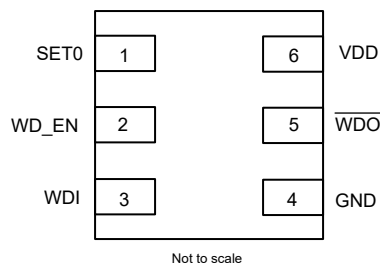


Figure 5-4. Pin Configuration Option J
DSE Package, 6-Pin WSON,
TPS3436 Top View

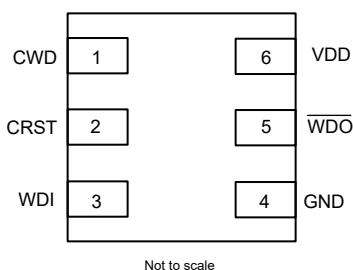


Figure 5-5. Pin Configuration Option K
DSE Package, 6-Pin WSON,
TPS3436 Top View

Table 5-1. Pin Functions

PIN NAME	PIN NUMBER					TYPE ⁽¹⁾	DESCRIPTION
	PINOUT A	PINOUT B	PINOUT C	PINOUT J	PINOUT K		
CRST	3	3	—	—	2	I	Programmable WDO assert time pin. Connect a capacitor between this pin and GND to program the WDO assert time period. See Section 7.3.3 for more details.
CWD	2	2	—	—	1	I	Programmable watchdog timeout input. Watchdog close time is set by connecting a capacitor between this pin and ground. See Section 7.3.1.1 for more details.
GND	4	4	4	4	4	—	Ground pin

Table 5-1. Pin Functions (continued)

PIN NAME	PIN NUMBER					TYPE ⁽¹⁾	DESCRIPTION
	PINOUT A	PINOUT B	PINOUT C	PINOUT J	PINOUT K		
MR	1	—	2	—	—	I	Manual reset pin. A logic low on this pin asserts the $\overline{\text{WDO}}$ output. See Section 7.3.2 for more details.
$\overline{\text{WDO}}$	7	7	7	5	5	O	Watchdog output. Connect $\overline{\text{WDO}}$ to VDD using pullup resistance when using open-drain output. $\overline{\text{WDO}}$ is asserted when a watchdog error occurs or MR pin is driven LOW. See Section 7.3.3 for more details.
SET0	5	1	1	1	—	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog window ratios and enable-disable the watchdog; see Section 7.3.1.5 for more details.
SET1	—	5	5	—	—	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog window ratios and enable-disable the watchdog; see Section 7.3.1.5 for more details.
VDD	8	8	8	6	6	I	Supply voltage pin. For noisy systems, connecting a 0.1µF bypass capacitor is recommended.
WD-EN	—	—	6	2	—	I	Logic input. Logic high input enables the watchdog monitoring feature. See Section 7.3.1.3 for more details.
WDI	6	6	3	3	3	I	Watchdog input. A falling transition (edge) must occur at this pin during the open window for $\overline{\text{WDO}}$ to not assert. See Section 7.3.1 for more details.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted⁽¹⁾

		MIN	MAX	UNIT
Voltage	VDD	−0.3	6.5	V
Voltage	C _{WD} , C _{RST} , WD–EN, SETx, WDI, $\overline{\text{MR}}$ ⁽²⁾ , $\overline{\text{WDO}}$ (Push Pull)	−0.3	V _{DD} +0.3 ⁽³⁾	V
	$\overline{\text{WDO}}$ (Open Drain)	−0.3	6.5	
Current	$\overline{\text{WDO}}$ pin	−20	20	mA
Temperature ⁽⁴⁾	Operating ambient temperature, T _A	−40	125	°C
Temperature	Storage, T _{stg}	−65	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) If the logic signal driving $\overline{\text{MR}}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{\text{MR}}$.
- (3) The absolute maximum rating is (V_{DD} + 0.3)V or 6.5V, whichever is smaller
- (4) As a result of the low dissipated power in this device, it is assumed that T_J = T_A.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 750	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (Active Low output)	0.9		6	V
	C _{WD} , C _{RST} , WD–EN, SETx, WDI, $\overline{\text{MR}}$ ⁽¹⁾	0		VDD	
	$\overline{\text{WDO}}$ (Open Drain)	0		6	
	$\overline{\text{WDO}}$ (Push Pull)	0		VDD	
Current	$\overline{\text{WDO}}$ pin current	−5		5	mA
C _{RST}	C _{RST} pin capacitor range	1.5		1800	nF
C _{WD}	C _{WD} pin capacitor range	1.5		1000	nF
T _A	Operating ambient temperature	−40		125	°C

- (1) If the logic signal driving $\overline{\text{MR}}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{\text{MR}}$. V_{MR} should not be higher than V_{DD}.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3436	UNIT
		DDF (SOT23-8)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	91.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3436	UNIT
		DSE (WSON-6)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	199.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	121.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	104.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	103.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

6.6 Electrical Characteristics

At $1.04\text{V} \leq V_{DD} \leq 6\text{V}$, $\overline{\text{MR}} = \text{Open}$, $\overline{\text{WDO}}$ pull-up resistor ($R_{\text{pull-up}}$) = $100\text{k}\Omega$ to V_{DD} , output load (C_{LOAD}) = 10pF and over operating free-air temperature range -40°C to 125°C , unless otherwise noted. V_{DD} ramp rate $\leq 1\text{V}/\mu\text{s}$. Typical values are at $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V _{DD}	Input supply voltage	Active LOW output	1.04		6	V
I _{DD}	Supply current into VDD pin ⁽¹⁾	T _A = −40°C to 85°C		0.25	0.8	μA
				0.25	3	
V _{IL}	Low level input voltage WD–EN, WDI, SETx, MR ⁽¹⁾				0.3V _{DD}	V
V _{IH}	High level input voltage WD–EN, WDI, SETx, MR ⁽¹⁾		0.7V _{DD}			V
R _{MR}	Manual reset internal pull-up resistance			100		kΩ
WDO (Open-drain active-low)						
V _{OL}	Low level output voltage	V _{DD} = 1.5V I _{OUT(Sink)} = 500μA			300	mV
		V _{DD} = 3.3V I _{OUT(Sink)} = 2mA			300	
I _{lkg(OD)}	Open-Drain output leakage current	V _{DD} = V _{PULLUP} = 6V T _A = −40°C to 85°C		10	30	nA
		V _{DD} = V _{PULLUP} = 6V		10	60	nA
WDO (Push-pull active-low)						
V _{POR}	Power on WDO voltage ⁽²⁾	V _{OH(min)} = 0.8VDD I _{out(source)} = 15μA			900	mV
V _{OL}	Low level output voltage	V _{DD} = 1.5V I _{OUT(Sink)} = 500μA			300	mV
		V _{DD} = 3.3V I _{OUT(Sink)} = 2mA			300	
V _{OH}	High level output voltage	V _{DD} = 1.8V I _{OUT(Source)} = 500μA	0.8V _{DD}			V
		V _{DD} = 3.3V I _{OUT(Source)} = 500μA	0.8V _{DD}			
		V _{DD} = 6V I _{OUT(Source)} = 2mA	0.8V _{DD}			

(1) If the logic signal driving $\overline{\text{MR}}$ is less than V_{DD} , then additional current flows into V_{DD} and out of $\overline{\text{MR}}$.

(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

6.7 Timing Requirements

At $1.04\text{V} \leq V_{DD} \leq 6\text{V}$, $\overline{\text{MR}} = \text{Open}$, $\overline{\text{WDO}}$ pull-up resistor ($R_{\text{pull-up}}$) = 100k Ω to VDD, output RESET / WDO load (C_{LOAD}) = 10pF and over operating free-air temperature range -40°C to 125°C , unless otherwise noted. VDD ramp rate $\leq 1\text{V}/\mu\text{s}$. Typical values are at $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\overline{\text{MR_PW}}}$	MR pin pulse duration to assert output			100		ns
$t_{\text{P-WD}}$	WDI pulse duration to start next frame ⁽¹⁾		500			ns
$t_{\text{HD-WDEN}}$	WD-EN hold time to enable or disable WD operation ⁽¹⁾		200			μs
$t_{\text{HD-SETx}}$	SETx hold time to change WD timer setting ⁽¹⁾		150			μs
t_{WC}	Watchdog close window time period	Orderable Option TPS3436xxB	0.8	1	1.2	ms
		Orderable Option TPS3436xxC	4	5	6	
		Orderable Option TPS3436xxD	9	10	11	
		Orderable Option TPS3436xxE	18	20	22	
		Orderable Option TPS3436xxF	45	50	55	
		Orderable Option TPS3436xxG	90	100	110	
		Orderable Option TPS3436xxH	180	200	220	
		Orderable Option TPS3436xxI	0.9	1	1.1	s
		Orderable Option TPS3436xxJ	1.26	1.4	1.54	
		Orderable Option TPS3436xxK	1.44	1.6	1.76	
		Orderable Option TPS3436xxL	9	10	11	
		Orderable Option TPS3436xxM	45	50	55	
		Orderable Option TPS3436xxN	90	100	110	
t_{WO}	Watchdog open window time period	SETx pin decide multiplier n	$(n-1) \times t_{\text{WC}}$			ms

(1) Not production tested

6.8 Switching Characteristics

At $1.04\text{V} \leq V_{DD} \leq 6\text{V}$, $\overline{\text{MR}} = \text{Open}$, $\overline{\text{WDO}}$ pull-up resistor ($R_{\text{pull-up}}$) = 100k Ω to VDD, output RESET / WDO load (C_{LOAD}) = 10pF and over operating free-air temperature range -40°C to 125°C , unless otherwise noted. VDD ramp rate $\leq 1\text{V}/\mu\text{s}$. Typical values are at $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup delay ⁽¹⁾	C_{CRST} pin = Open or NC			500	μs
t_{SD}	Watchdog startup delay	Orderable part number TPS3436xA, TPS343xG		0		ms
		Orderable part number TPS3436xB, TPS3436xH	180	200	220	
		Orderable part number TPS3436xC, TPS3436xI	450	500	550	
		Orderable part number TPS3436xD, TPS3436xJ	0.9	1	1.1	s
		Orderable part number TPS3436xE, TPS3436xK	4.5	5	5.5	
		Orderable part number TPS3436xF, TPS3436xL	9	10	11	
t_{WDO}	Watchdog assert time delay	Orderable part number TPS3436xxxxB	1.6	2	2.4	ms
		Orderable part number TPS3436xxxxC	9	10	11	ms
		Orderable part number TPS3436xxxxD	22.5	25	27.5	ms
		Orderable part number TPS3436xxxxE	45	50	55	ms
		Orderable part number TPS3436xxxxF	90	100	110	ms
		Orderable part number TPS3436xxxxG	180	200	220	ms
		Orderable part number TPS3436xxxxH	0.9	1	1.1	s
		Orderable part number TPS3436xxxxI	9	10	11	s
$t_{\text{MR_WDO}}$	Propagation delay from $\overline{\text{MR}}$ low to WDO assertion	$V_{DD} \geq 1.25\text{V}$, $\overline{\text{MR}} = V_{\text{MR_H}}$ to $V_{\text{MR_L}}$		100		ns

(1) Specified by design parameter.

6.9 Timing Diagrams

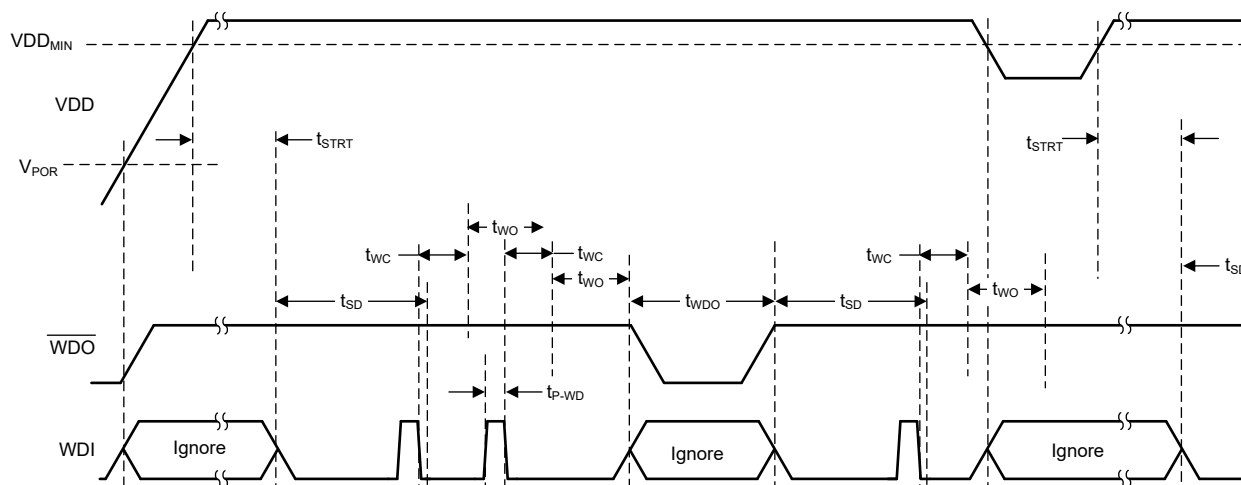


Figure 6-1. Functional Timing Diagram

6.10 Typical Characteristics

all curves are taken at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

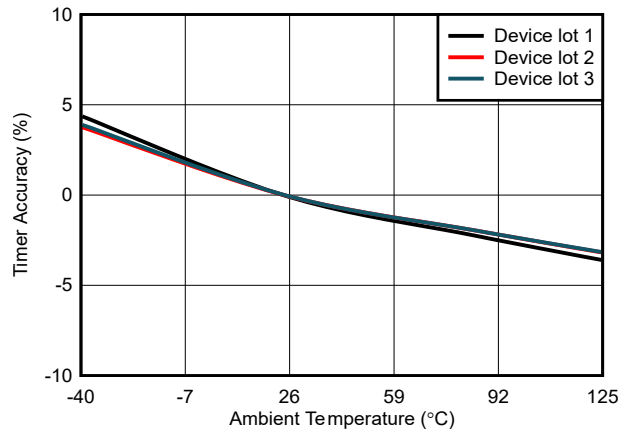


Figure 6-2. Timer Accuracy vs Temperature

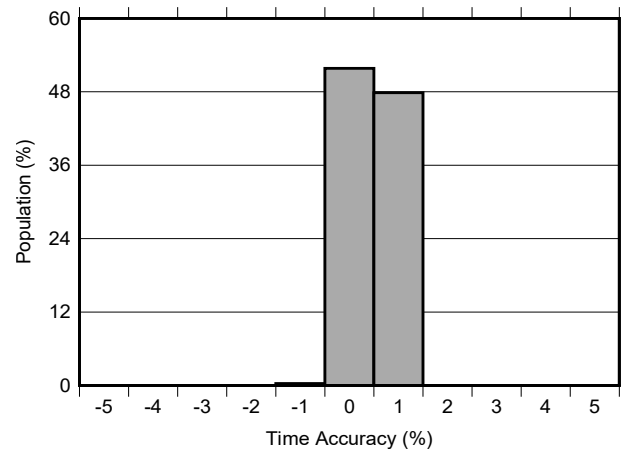


Figure 6-3. Timer Accuracy Histogram

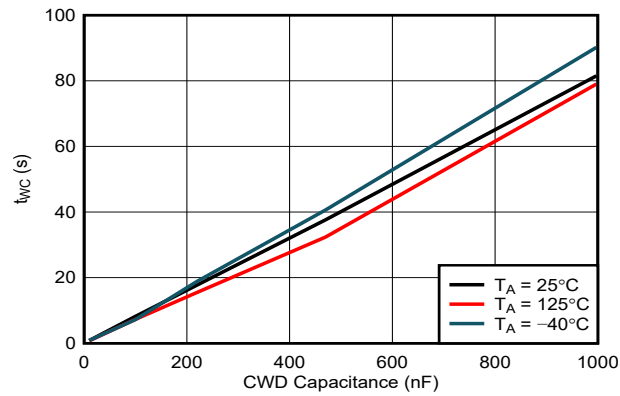


Figure 6-4. t_{WC} vs Capacitance

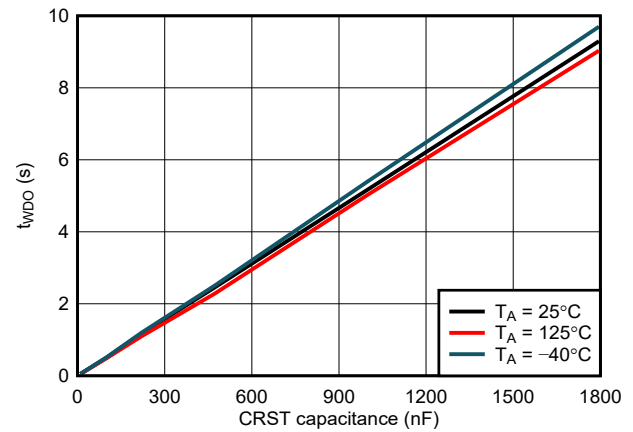


Figure 6-5. t_{WD0} vs Capacitance

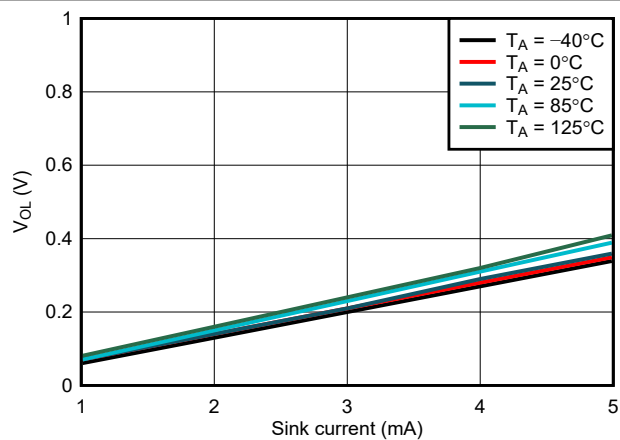


Figure 6-6. WDO V_{OL} vs I_{sink} , $V_{DD} = 1.5\text{V}$

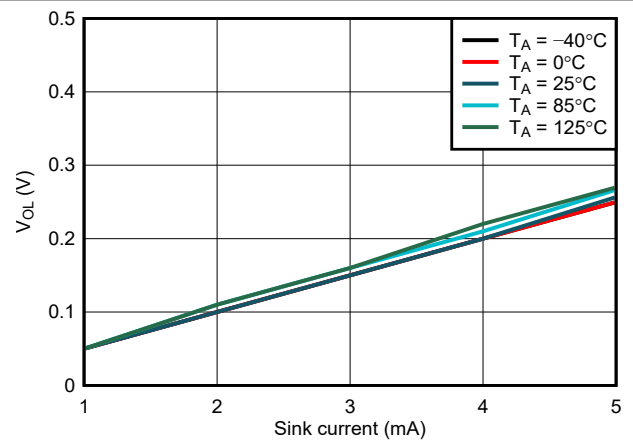


Figure 6-7. WDO V_{OL} vs I_{sink} , $V_{DD} = 3.3\text{V}$

6.10 Typical Characteristics (continued)

all curves are taken at $T_A = 25^\circ\text{C}$ (unless otherwise noted)

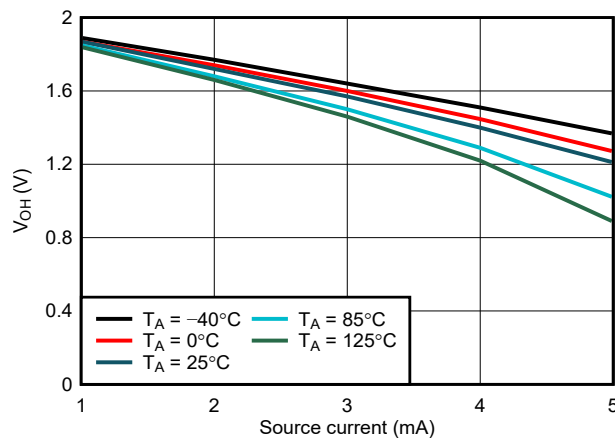


Figure 6-8. WDO V_{OH} vs I_{source} , $V_{DD} = 2.0\text{V}$

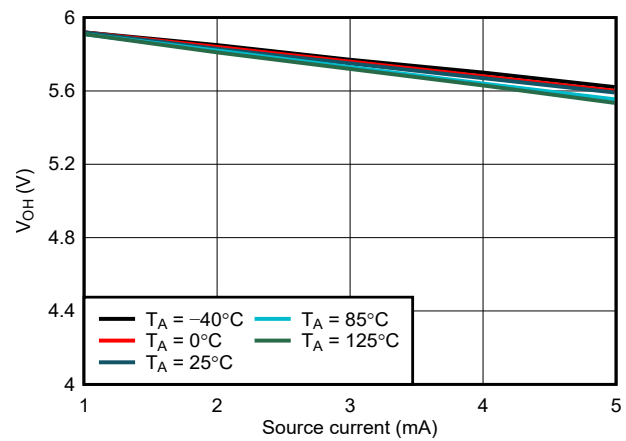


Figure 6-9. WDO V_{OH} vs I_{source} , $V_{DD} = 6.0\text{V}$

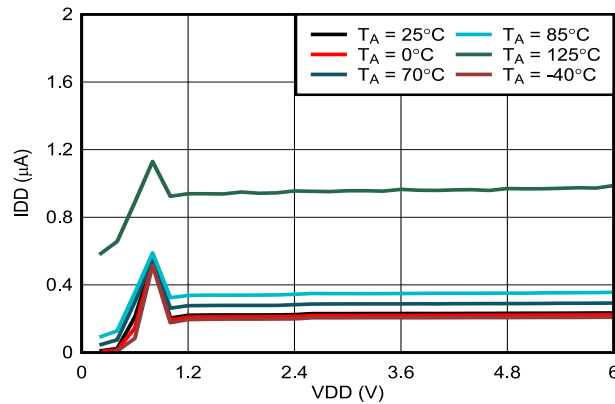


Figure 6-10. Supply Current vs Power-Supply Voltage

7 Detailed Description

7.1 Overview

The TPS3436 is a high-accuracy window watchdog timer device. The device family supports multiple features related to watchdog operation in a compact 6 pin WSON and 8 pin SOT23 package. The devices are available in 5 different pinout configurations. Each pinout offers access to different features to meet the various application requirements.

7.2 Functional Block Diagrams

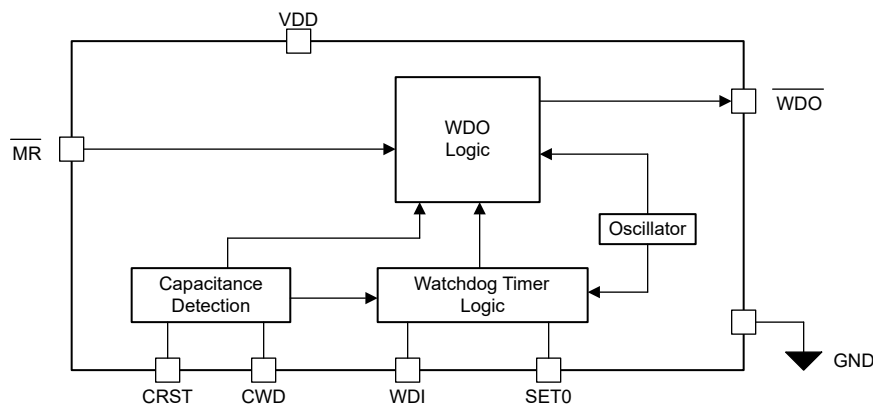


Figure 7-1. Pinout Option A

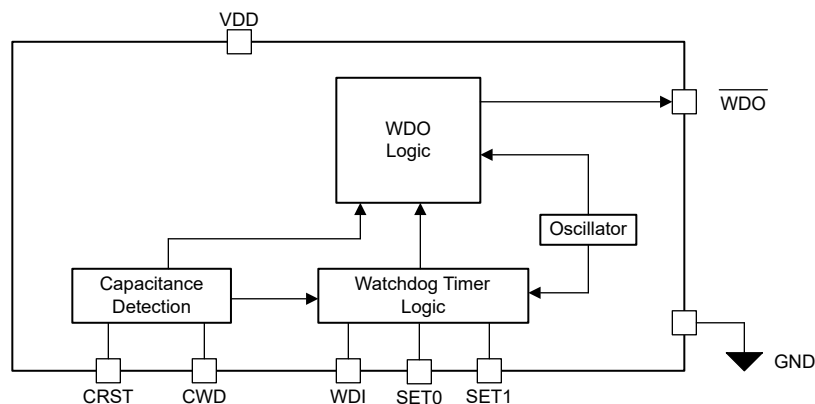


Figure 7-2. Pinout Option B

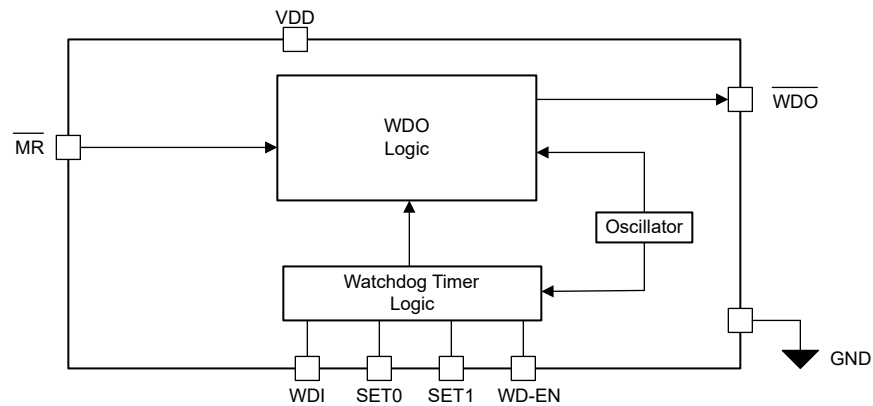


Figure 7-3. Pinout Option C

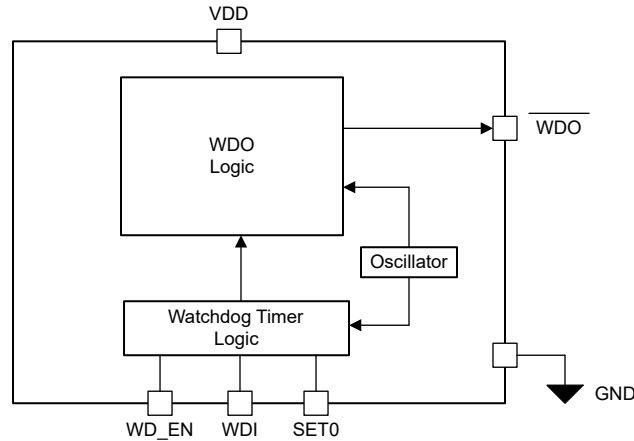


Figure 7-4. Pinout Option J

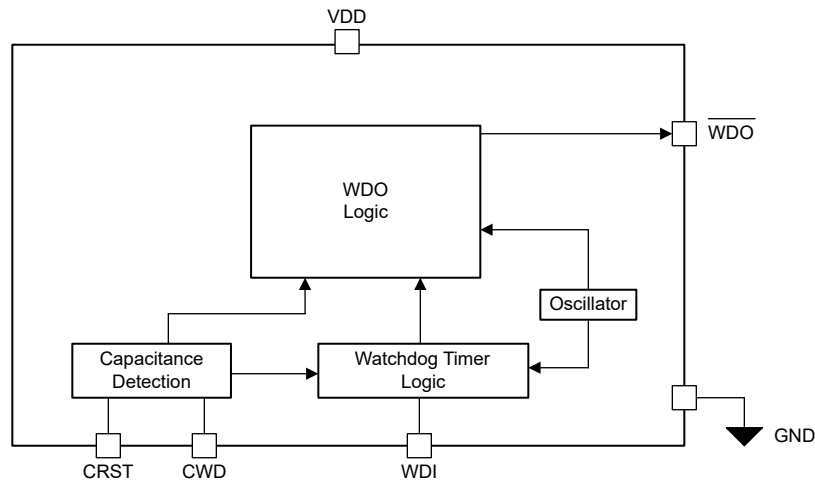


Figure 7-5. Pinout Option K

7.3 Feature Description

7.3.1 Window Watchdog Timer

The TPS3436 offers high precision window watchdog timer monitoring. The device is available in multiple pinout options A to K which support multiple features to meet ever expanding needs of various applications. Select a correct pinout to meet the application needs.

The window watchdog is active when the VDD voltage is higher than the VDD_{MIN} , $\overline{MR}$ voltage is held higher than $0.7 \times VDD$ and watchdog is enabled. TPS3436 family offers various startup time delay options to make sure enough time is available for the host to complete boot operation. Please refer [Section 7.3.1.4](#) section for additional details.

The window watchdog timer frame consists of two windows namely close window (t_{WC}) followed by open window (t_{WO}). The device monitors the WDI pin for falling edge. User is expected to provide a valid falling edge on WDI pin in the open window. Refer [Section 4](#) to arrive at the relevant close window and open window values needed for application. The timer value is reset when a valid falling edge is detected on WDI pin in the t_{WO} time duration. An early fault is reported if a WDI falling edge is detected in close window. A late fault is reported if WDI falling edge is not detected in both close and open window. The device asserts WDO output for time t_{WDO} in event of watchdog fault. Refer [Section 7.3.3](#) to arrive at the relevant t_{WDO} value needed for application.

[Figure 7-6](#) shows the basic operation for window watchdog timer operation. The TPS3436 watchdog functionality supports multiple features. Details are available in following sub sections.

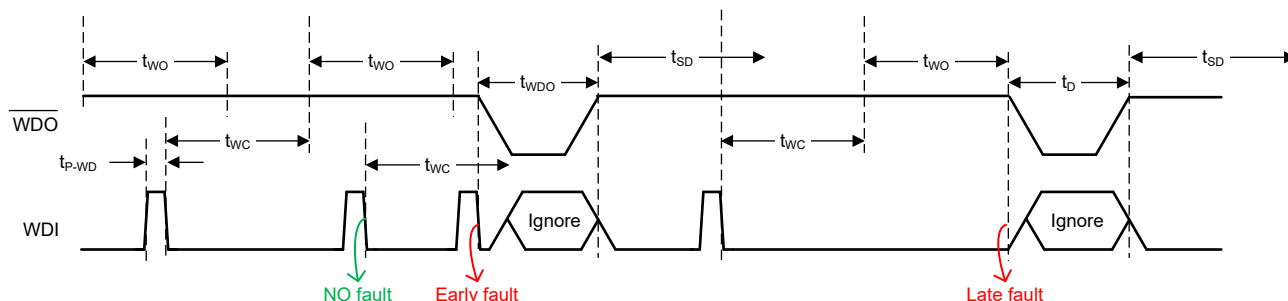


Figure 7-6. Window Watchdog Timer Operation

7.3.1.1 t_{WC} (Close Window) Timer

The window watchdog frame consists of two sub frames t_{WC} followed by t_{WO} . The host is not expected to drive valid WDI transition during t_{WC} time. A valid WDI transition during t_{WC} frame results in early fault condition and the WDO output is asserted. The t_{WC} timer for TPS3436 can be set using an external capacitor connected between CWD pin and GND pin. This feature is available with pinout options A or B or K. Applications which are space constrained or need timer values which meet offered timer options, can benefit when using pinout options C or J. The TPS3436 offers multiple fixed timer options ranging from 1ms up to 100sec.

The TPS3436 when using capacitance based timer, senses the capacitance value during the power up. The capacitor is charged and discharged with known internal current source for one cycle to sense the capacitance value. The sensed value is used to arrive at t_{WC} timer for the watchdog operation. This unique implementation helps reduce the continuous charge and discharge current for the capacitor, thus reducing overall current consumption. Continuous charge and discharge of capacitance creates wider dead time (no watchdog monitor functionality) when capacitor is discharging. The dead time is higher for high value of capacitance. The unique implementation of TPS3436 helps avoid the dead time as the capacitance is not continuously charging or discharging under normal operation. Make sure C_{CWD} is $< 200 \times C_{CRST}$ for accurate calibration of capacitance. The close time window is decided based on SETx pin combination and the CWD capacitance. [Table 7-1](#) to [Table 7-2](#) highlights the relationship between t_{WC} in second and CWD capacitance in farad. The t_{WC} timer is 20% accurate for an ideal capacitor. Accuracy of the capacitance provides additional impact on the t_{WC} time. Make sure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

Table 7-1. t_{WC} Equation 1 SET Pin (Pin Configuration A)

SET PIN VALUE	EQUATION
0	$t_{WC}(\text{sec}) = 79.2 \times 10^6 \times C_{CWD}(\text{F})$ (1)
1	$t_{WC}(\text{sec}) = 39.6 \times 10^6 \times C_{CWD}(\text{F})$ (2)

Table 7-2. t_{WC} Equation 2 SET Pin, WD-EN Not Available (Pin Configuration B)

SET PIN VALUE	EQUATION
00	$t_{WC}(\text{sec}) = 79.2 \times 10^6 \times C_{CWD}(\text{F})$ (3)
01	Watchdog disabled
10	$t_{WC}(\text{sec}) = 39.6 \times 10^6 \times C_{CWD}(\text{F})$ (4)
11	$t_{WC}(\text{sec}) = 9.9 \times 10^6 \times C_{CWD}(\text{F})$ (5)

The TPS3436 also offers wide selection of high accuracy fixed t_{WC} timer options starting from 1msec to 100sec including various industry standard values. The TPS3436 fixed time options are $\pm 10\%$ accurate for $t_{WC} \geq 10\text{msec}$. For $t_{WC} < 10\text{msec}$, the accuracy is $\pm 20\%$. t_{WC} value relevant to application is identifiable from the orderable part number (OPN). Refer [Section 4](#) to identify mapping of orderable part number to t_{WC} value.

7.3.1.2 t_{WO} (Open Window) Timer

The window watchdog frame consists of two sub frames t_{WC} followed by t_{WO} . The host is expected to drive valid WDI transition during t_{WO} time. A valid WDI transition before beginning of t_{WO} frame causes early fault condition. Failure to offer valid WDI transition during t_{WC} and t_{WO} frames results in late fault condition. When a fault condition is detected the WDO output is asserted.

The t_{WO} value is derived using t_{WC} value and the window open time ratio value n . [Equation](#) highlights the relationship between t_{WO} and t_{WC} . Refer [Section 4](#) to select available ratio options.

$$t_{WO} = (n - 1) \times t_{WC} \quad (6)$$

Each orderable can offer up to 3 ratio options based on the available SET pins. Refer [Section 7.3.1.5](#) to identify mapping of ratio value to SET pin control. The maximum t_{WO} value is limited to 640 seconds. Make sure selected t_{WC} and ratio combination does not lead to t_{WO} value greater than 640 seconds.

7.3.1.3 Watchdog Enable Disable Operation

The TPS3436 supports watchdog enable or disable functionality. This functionality is critical for different use cases as listed below.

- Disable watchdog during firmware update to avoid host RESET.
- Disable watchdog during software step-by-step debug operation.
- Disable watchdog when performing critical task to avoid watchdog error interrupt.
- Keep watchdog disabled until host boots up.

The TPS3436 supports watchdog enable or disable functionality through either WD-EN pin (pin configuration C, J) or SET[1:0] = 0b'01 (pin configuration B) logic combination. For a given pinout only one of these two methods is available for the user to disable watchdog operation.

For a pinout which offers a WD-EN pin, the watchdog enable disable functionality is controlled by the logic state of WD-EN pin. Drive WD-EN = 1 to enable the watchdog operation or drive WD-EN = 0 to disable the watchdog operation. The WD-EN pin can be toggled any time during the device operation. The [Figure 7-7](#) diagram shows timing behavior with WD-EN pin control.

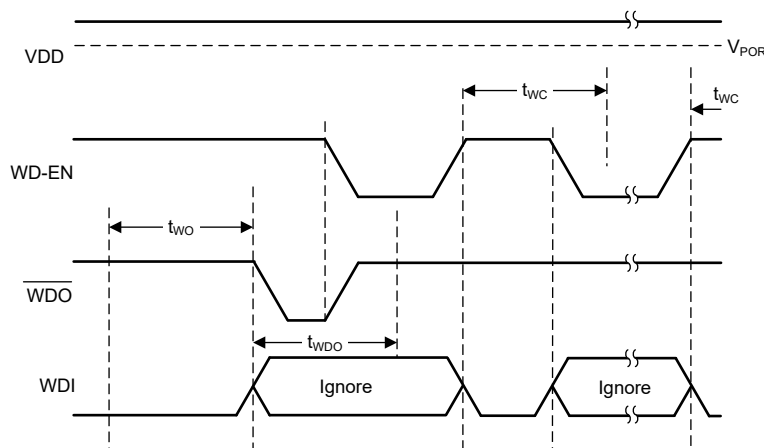


Figure 7-7. Watchdog Enable: WD-EN Pin Control

SET[1:0] = 0b'01 combination can be used to disable watchdog operation with a pinout which offers SET1 and SET0 pins, but does not include WD-EN pin. The SET pin logic states can be changed at any time during watchdog operation. Refer [Section 7.3.1.5](#) section for additional details regarding SET[1:0] pin behavior.

Pinout options A, B, K offer watchdog timer control using a capacitance connected between CWD and GND pin. A capacitance value higher than recommended or connect to GND leads to watchdog functionality getting disabled. Capacitance based disable operation overrides the other two options mentioned above. Changing capacitance on the fly does not enable or disable watchdog operation. A power supply recycle is needed to detect change in capacitance.

Ongoing watchdog frame is terminated when watchdog is disabled. WDO stays deasserted when watchdog operation is disabled. When enabled the device immediately enters t_{WC} frame and start watchdog monitoring operation.

7.3.1.4 t_{SD} Watchdog Start Up Delay

The TPS3436 supports watchdog startup delay feature. This feature is activated after power up or after WDO assert event. When t_{SD} frame is active, the device monitors the WDI pin but the WDO output is not asserted. This feature allows time for the host complete boot process before watchdog monitoring can take over. The start up delay helps avoid unexpected WDO assert events during boot. The t_{SD} time is predetermined based on the device part number selected. Refer [Section 4](#) section for details to map the part number to t_{SD} time. Pinout option A, B, K are available only in no delay or 10sec start up delay options.

To exit t_{SD} frame, one of the following event must occur:

- The host provides a valid pulse transition on the WDI pin.
- Change in logic state of SET[1:0].
- Toggling of the WD_EN pin.

The device enters watchdog monitoring phase after the device exits the t_{SD} frame.

Failure to provide one of the exit condition within t_{SD} triggers the watchdog error by asserting the WDO output pin for t_D , this is observed in [Figure 7-8](#).

The t_{SD} frame is not initiated when the watchdog functionality is enabled using WD-EN pin or SET[1:0] pin combination as described in [Section 7.3.1.3](#) section.

[Figure 7-8](#) shows the operation for t_{SD} time frame.

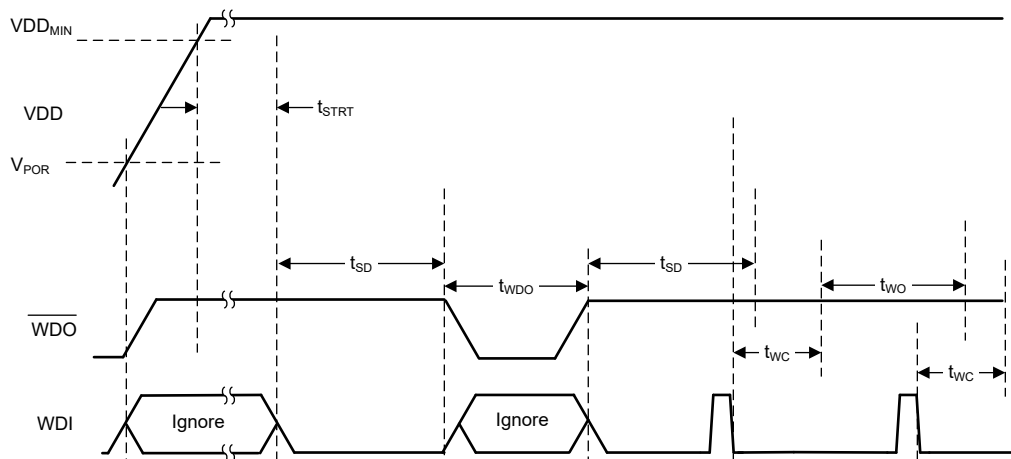


Figure 7-8. t_{SD} Frame Behavior

7.3.1.5 SET Pin Behavior

The TPS3436 offers one or two SET pins based on the pinout option selected. SET pins offer flexibility to the user to program the t_{WO} timer unpremeditatedly to meet various application requirements. Typical use cases for the SET pin are:

- Use wide open window timer when host is in sleep mode, change to small timeout operation when host is operational. Watchdog can be used to wake up the host after long duration to perform the application related activities before going back to sleep.
- Change to wide open window timer when performing system critical tasks to make sure the watchdog does not interrupt the critical task. Change timer to application specified interval after the critical task is complete.

The t_{WO} timer value for the device is combination of t_{WC} timer selection based on the CWD pin or fixed timer value along with SET pin logic level. The t_{WC} timer value is decided based on the Watchdog Close Time selector in the [Section 4](#) section. The SET pin logic level is decoded during the device power up. The SET pin value can be changed any time during the operation. SETx pin change which leads to change of watchdog timer value or enable/disable state, ends the ongoing watchdog frame immediately. SETx pins can be updated when WDO output is asserted as well. The updated t_{WO} timer value is applied after the output is deasserted and the t_{SD} timer is over or ends.

For a pinout which offers only SET0 pin to the user, the t_{WO} ratio value is decided based on the Watchdog Open Time Ratio selector field in the orderable part number. Refer [Section 4](#) for available options. [Table 7-3](#) showcases an example of the t_{WO} values for different SET0 logic levels when using Watchdog Close Time setting as option D = 10msec.

Table 7-3. t_{WO} Values with SET0 Pin Only (Pin Configuration A, J)

Watchdog Open Time Ratio Selection	t_{WO}	
	SET0 = 0	SET0 = 1
A	10msec	30msec
B	30msec	70msec
C	70msec	150msec
D	150msec	310msec
E	310msec	630msec
F	630msec	1270msec

Pinout which offer both SET0 and SET1 pins to the user, the t_{WO} ratio value is decided based on the Watchdog Open Time Ratio selector field in the orderable part number. Refer [Section 4](#) for available options. Two SETx pins offer 3 different time scaling options. The SET[1:0] = 0b'01 combination disables the watchdog operation. [Table 7-4](#) showcases an example of the t_{WO} values for different SET[1:0] logic levels when using Watchdog Close Time setting as option G = 100msec. The package pin out selected does not offer WD-EN pin.

Table 7-4. t_{WO} Values with SET0 and SET1 Pins, WD-EN Pin Not Available (Pin Configuration B)

Watchdog Open Time Ratio selection	t_{WO}			
	SET[1:0] = 0b'00	SET[1:0] = 0b'01	SET[1:0] = 0b'10	SET[1:0] = 0b'11
A	100msec	Watchdog disable	300msec	1500msec
B	300msec	Watchdog disable	700msec	3100msec
C	700msec	Watchdog disable	1500msec	6300msec
D	1500msec	Watchdog disable	3100msec	12700msec
E	3100msec	Watchdog disable	6300msec	25500msec
F	6300msec	Watchdog disable	12700msec	51100msec

Selected pinout option can offer WD-EN pin along with SET[1:0] pins (Pin Configuration C). With this pinout, the WD-EN pin controls watchdog enable and disable operation. The SET[1:0] = 0b'01 combination operates as SET[1:0] = 0b'00.

Make sure the t_{WO} value with SETx ratio does not exceed 640sec. If a selection of close window timer and ratio results in $t_{WO} > 640\text{sec}$, the timer value is restricted to 640sec.

Figure 7-9 to Figure 7-11 show the timing behavior with respect to SETx status changes.

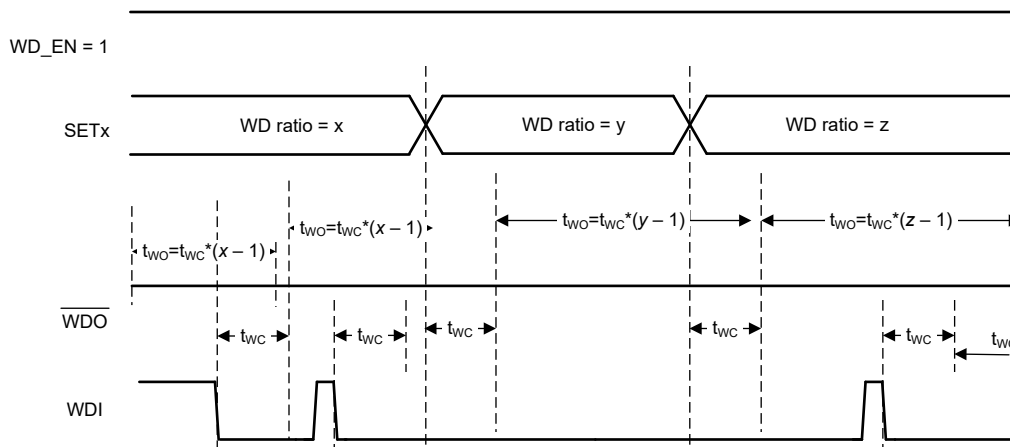
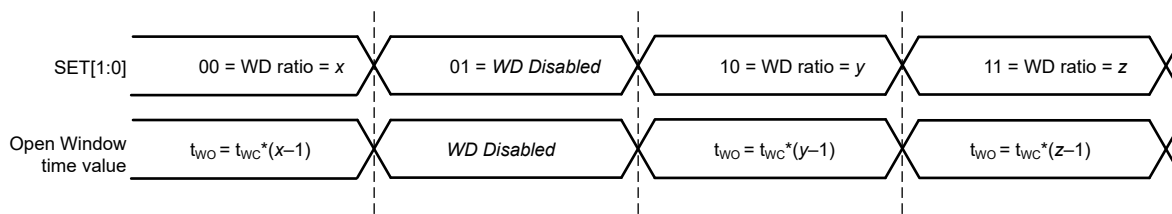
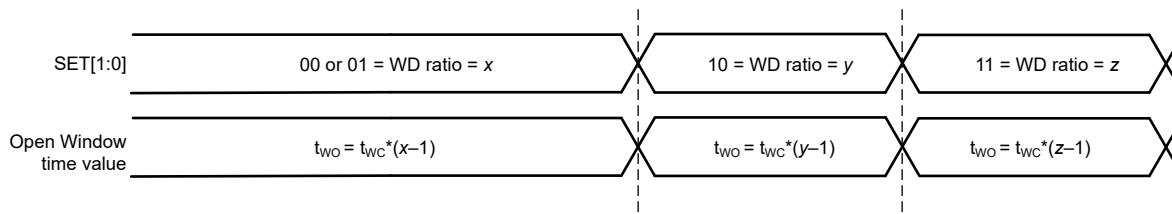


Figure 7-9. Watchdog Behavior with SETx Pin Status

SET Pin (2 Pins) Operation; WD_EN Pin Not Available

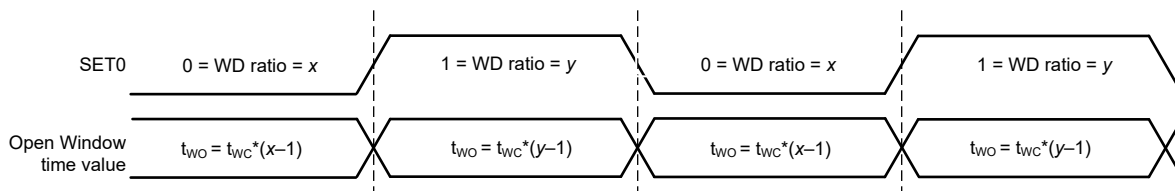


SET Pin (2 Pins) Operation; WD_EN Available = 1



t_{WC} = Fixed based on OPN or programmable using capacitor
x, y, z = Fixed based on ratio chosen

Figure 7-10. Watchdog Operation with 2 SET Pins



t_{WC} = Fixed based on OPN or programmable using capacitor
X, y = Fixed based on ratio chosen

Figure 7-11. Watchdog Operation with 1 SET Pin

7.3.2 Manual RESET

The TPS3436 supports manual reset functionality using $\overline{\text{MR}}$ pin. $\overline{\text{MR}}$ pin when driven with voltage lower than $0.3 \times \text{V}_{\text{DD}}$, asserts the WDO output. The $\overline{\text{MR}}$ pin has $100\text{k}\Omega$ pull up to V_{DD} . The $\overline{\text{MR}}$ pin can be left floating. The internal pullup makes sure the output is not asserted due to $\overline{\text{MR}}$ pin trigger.

The output is deasserted after $\overline{\text{MR}}$ pin voltage rises above $0.7 \times \text{V}_{\text{DD}}$ voltage. Refer [Figure 7-12](#) for more details.

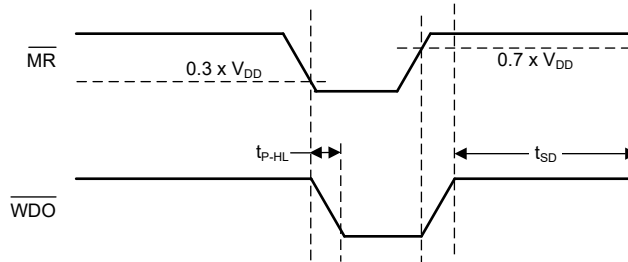


Figure 7-12. $\overline{\text{MR}}$ Pin Response

7.3.3 WDO Output

The TPS3436 device offers WDO output pin. WDO output is asserted when $\overline{\text{MR}}$ pin voltage is lower than $0.3 \times \text{V}_{\text{DD}}$ or watchdog timer error is detected.

The output is asserted for t_{WDO} time when any relevant events described above are detected, except for $\overline{\text{MR}}$ event. The time t_{WDO} can be programmed by connecting a capacitor between CRST pin and GND or the device asserts t_{WDO} for fixed time duration as selected by orderable part number. Refer [Section 4](#) section for all available options.

[Equation 7](#) describes the relationship between capacitor value and the time t_{WDO} . Make sure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_{\text{WDO}} (\text{sec}) = 4.95 \times 10^6 \times C_{\text{CRST}} (\text{F}) \quad (7)$$

TPS3436 also offers a unique option of latched output. An orderable with latched output holds the output in asserted state indefinitely until the device is power cycled or the error condition is addressed. If the output is latched due to $\overline{\text{MR}}$ pin low voltage, the output latch is released when $\overline{\text{MR}}$ pin voltage rises above $0.7 \times \text{V}_{\text{DD}}$ level. If the output is latched due to watchdog timer error, the output latch is released when a WDI negative edge is detected or the device is shutdown and powered up again. [Figure 7-13](#) shows timing behavior of the device with latched output configuration.

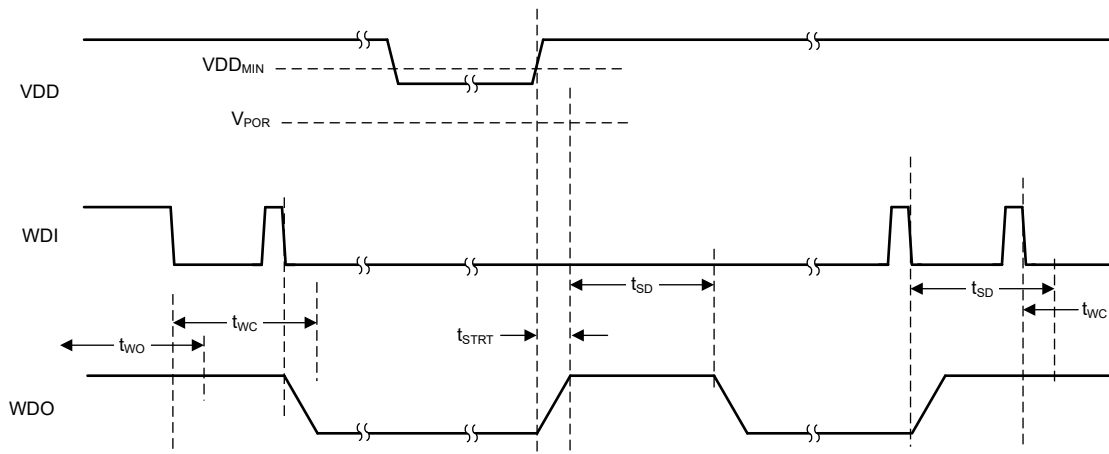


Figure 7-13. Output Latch Timing Behavior

7.4 Device Functional Modes

Table 7-5 summarizes the functional modes of the TPS3436.

Table 7-5. Device Functional Modes

VDD	WATCHDOG STATUS	WDI	WDO
$V_{DD} < V_{POR}$	Not Applicable	—	Undefined
$V_{POR} \leq V_{DD} < V_{DDmin}$	Not Applicable	Ignored	High
$V_{DD} \geq V_{DDmin}$	Disabled	Ignored	High
	Enabled	$t_{WC(max)} \leq t_{pulse}^1 \leq t_{WC(max)} + t_{WO(min)}$	High
	Enabled	$t_{WC(max)} > t_{pulse}^1$	Low
	Enabled	$t_{WC(max)} + t_{WO(max)} < t_{pulse}^1$	Low

(1) Where t_{pulse} is the time between falling edges on WDI.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.1.1 Output Assert Delay

The TPS3436 features two options for setting the output assert delay (t_{WDO}): using a fixed timing and programming the timing through an external capacitor.

8.1.1.1 Factory-Programmed Output Assert Delay Timing

Fixed output assert delay timings are available using pinout C and J. Using these timings enables a high-precision, 10% accurate output assert delay timing.

8.1.1.2 Adjustable Capacitor Timing

The TPS3436 also utilizes a programmable output assert delay, using a precision current source to charge an external capacitor upon device startup. The typical delay time resulting from a given external capacitance on the CRST pin can be calculated by Equation 8, where t_{WDO} is the output assert delay time in seconds and C_{CRST} is the capacitance in microfarads.

$$t_{WDO} \text{ (sec)} = 4.95 \times 10^6 \times C_{CRST} \text{ (F)} \quad (8)$$

Note that to minimize the difference between the calculated output assert delay time and the actual output assert delay time, use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. Table 8-1 lists the output assert delay time for typical capacitor values.

Table 8-1. Output Assert Delay Time for Common Capacitor Values

C_{CRST}	OUTPUT ASSERT DELAY TIME (t_{WDO})			UNIT
	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	
10nF	39.6	49.5	59.4	ms
100nF	396	495	594	ms
1μF	3960	4950	5940	ms

(1) Minimum and maximum values are calculated using capacitor's typical value.

8.1.2 Watchdog Window Functionality

The TPS3436 features two options for setting the close window watchdog timer (t_{WC}): using a fixed timing and programming the timing through an external capacitor.

8.1.2.1 Factory-Programmed Timing Options

Fixed watchdog timeout options are available using pinout C and J. Using these timings enables a high-precision, 10% accurate watchdog timer t_{WC} .

8.1.2.2 Adjustable Capacitor Timing

Adjustable t_{WC} timing is achievable by connecting a capacitor to the CWD pin. If this method is used, please consult Table 7-1 to Table 7-2 for equations to calculate typical t_{WC} values using ideal capacitors as the effect

of C_{CWD} depends on the SETx pin values. Capacitor tolerances cause the actual device timing to vary such that the minimum of t_{WC} can decrease and the maximum of t_{WC} can increase by the capacitor tolerance. For the most accurate timing, use ceramic capacitors with COG dielectric material.

8.2 Typical Applications

8.2.1 Design 1: Monitoring a Microcontroller Watchdog During Operational and Sleep Modes

The TPS3436 can utilize high-accuracy voltage monitoring and on-the-fly SETx assigning to monitor a microcontroller that has both an operational and sleep mode.

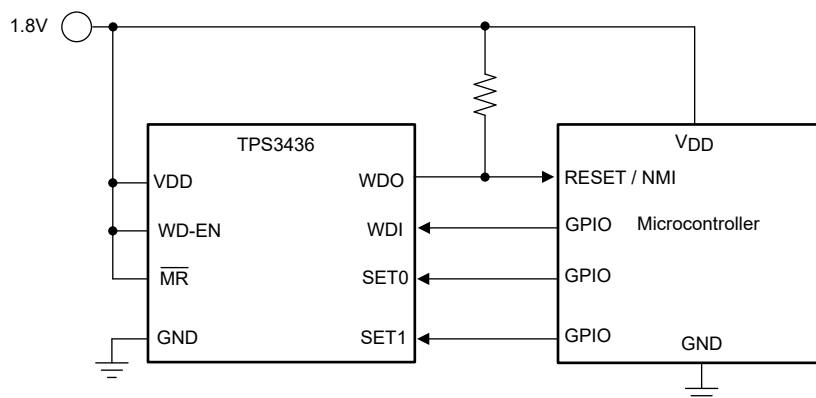


Figure 8-1. Microcontroller Window Watchdog Monitoring with Sleep Watchdog Mode

8.2.1.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Window Close Time During Operation	Typical t_{WC} of 50ms during operation	Typical t_{WC} of 50ms
Window Open Time During Operation	Typical t_{WO} of 1.4s during operation	Typical t_{WO} of 1.55s
Window Close Time During Sleep	Typical t_{WC} of 50ms during sleep	Typical t_{WC} of 50ms
Window Open Time During Sleep	Typical t_{WO} of 12s during sleep	Typical t_{WO} of 12.75s
Output Assert Delay	Typical t_{WDO} of 200ms	Typical t_{WDO} of 200ms
Output logic voltage	Open-drain	Open-drain
Maximum device current consumption	20 μ A	250nA typical current consumption

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Determining Window Timings During Operation and Sleep Modes

The TPS3436 allows for precise 10% accurate watchdog timings. This application requires two different window timings to maximize power efficiency: one for the microcontroller's operational state and one for the sleep state. To achieve this, the host can reassign the SETx pins when transitioning between states. A window close time, t_{WC} , of 50ms typical is chosen because of the application's 50ms typical t_{WC} requirement. The application requires a typical watchdog open time, t_{WO} , of 1.4s during operation and a t_{WO} of 12s during sleep. Thus, the possible variant options are narrowed to TPS3436xxFExDDFR.

8.2.1.2.2 Meeting the Output Assert Delay

The TPS3436 features two options for selecting reset delays: fixed delays and capacitor-programmable delays. The TPS3436 supports only fixed watchdog timings and fixed output assert delays or programmable watchdog timings and programmable output assert delays. The application requires a 200ms minimum output assert delay, thus output assert delay option G is used. Because of these requirements and no need for a startup delay, the TPS3436CAFEGDDFR is used.

8.2.1.2.3 Setting the Watchdog Window

In this application, the watchdog timing options are based on the WDI signal that is provided to the TPS3436. A watchdog WDI setting must be chosen such that a transition must always occur within the open watchdog window. There are several ways to achieve these window parameters. An external capacitor can be placed on the CWD pin and calculated to have a sufficient window close time. Another option is to use one of the factory-programmed timing options. An additional advantage of choosing one of the factory-programmed options is the ability to reduce the number of components required, thus reducing overall BOM cost.

8.2.1.2.4 Calculating the $\overline{WDO}$ Pullup Resistor

The TPS3436 uses an open-drain configuration for the $\overline{WDO}$ circuit, as shown in Figure 8-2. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to make sure that V_{OL} is below the maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{WDO}$ pin current (I_{RST}), and V_{OL} . The maximum V_{OL} is 0.3V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.3V with I_{RST} kept below 2mA for $V_{DD} \geq 3V$ and 500 μ A for $V_{DD} = 1.5V$. For this example, with a $V_{PU} = V_{DD} = 1.5V$, a resistor must be chosen to keep I_{RST} below 500 μ A because this value is the maximum consumption current allowed. To make sure this specification is met, a pullup resistor value of 10k Ω was selected, which sinks a maximum of 180 μ A when $\overline{WDO}$ is asserted.

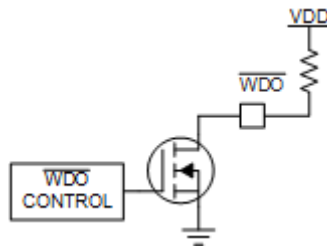


Figure 8-2. Open-Drain $\overline{RESET}$ Configuration

8.3 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.04V and 6V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1 μ F capacitor between the VDD pin and the GND pin.

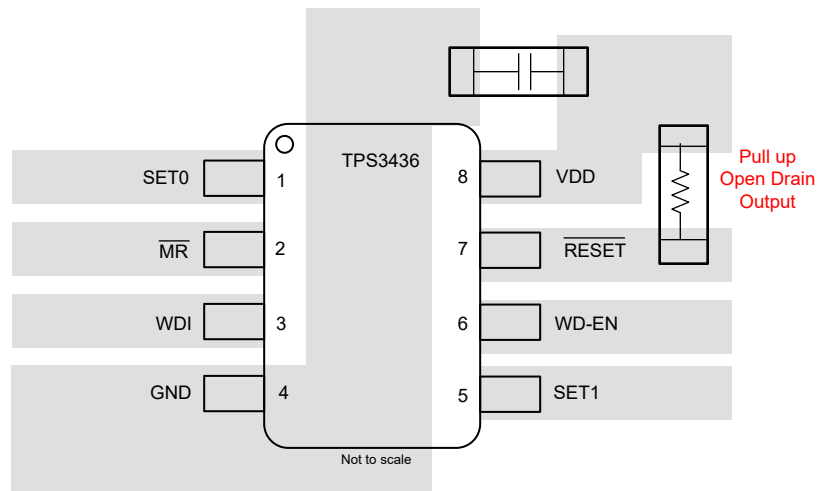
8.4 Layout

8.4.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1 μ F ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{WDO}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1 μ F ceramic capacitor as near as possible to the VDD pin.
- Place C_{CRST} capacitor as close as possible to the CRST pin.
- Place C_{CWD} capacitor as close as possible to the CWD pin.
- Place the pullup resistor on the $\overline{WDO}$ pin as close to the pin as possible.

8.4.2 Layout Example



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Figure 8-3. Typical Layout for the Pinout C of TPS3436

9 Device and Documentation Support

9.1 Device Nomenclature

OPN	PINOUT OPTION	OUTPUT TOPOLOGY, STARTUP DELAY	WATCHDOG CLOSE TIME	WATCHDOG OPEN TIME RATIO	OUTPUT ASSERT TIME
TPS3436CDCDCDDF RQ1 (Preview)	C	Open Drain, 1 second	5ms	16, 32, 12	10ms

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2022) to Revision A (October 2026)	Page
• Updated datasheet status from <i>Advanced Information</i> to <i>Production Data</i>	1
• Added Thermal Information table for DSE package.....	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3436CGEAJDDFR	Active	Production	SOT-23-THIN (DDF) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CNLLP

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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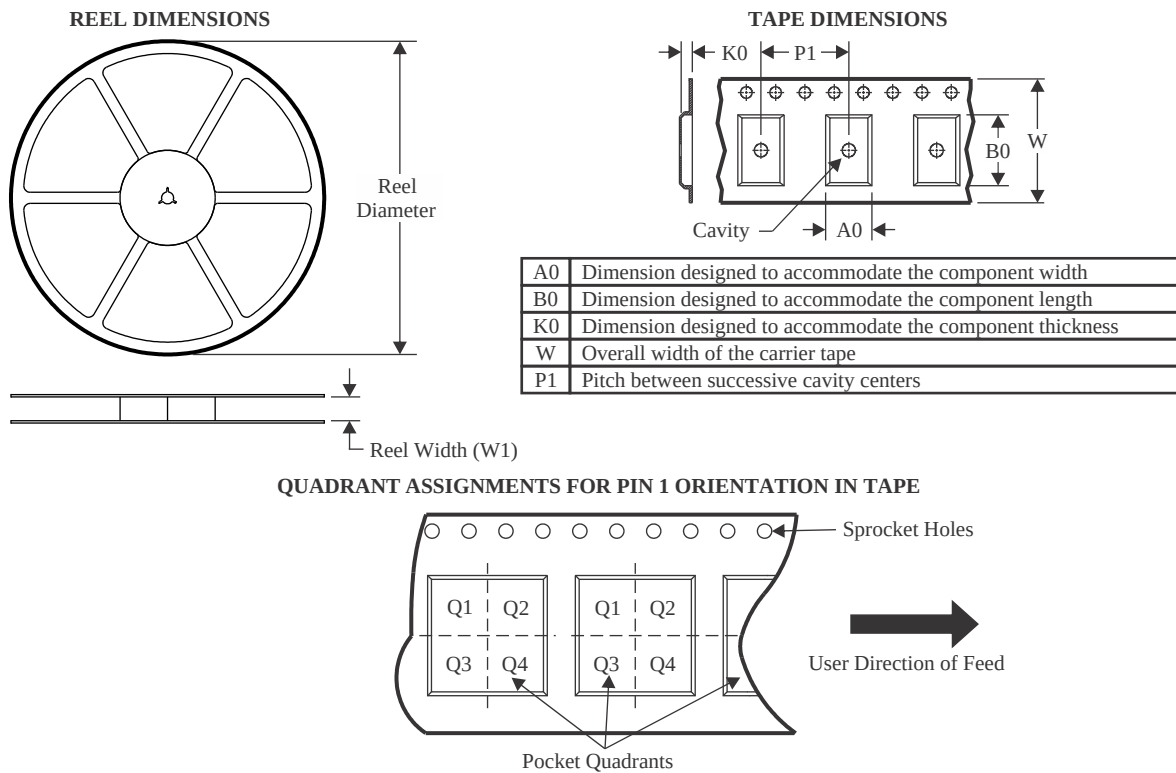
OTHER QUALIFIED VERSIONS OF TPS3436 :

- Automotive : [TPS3436-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

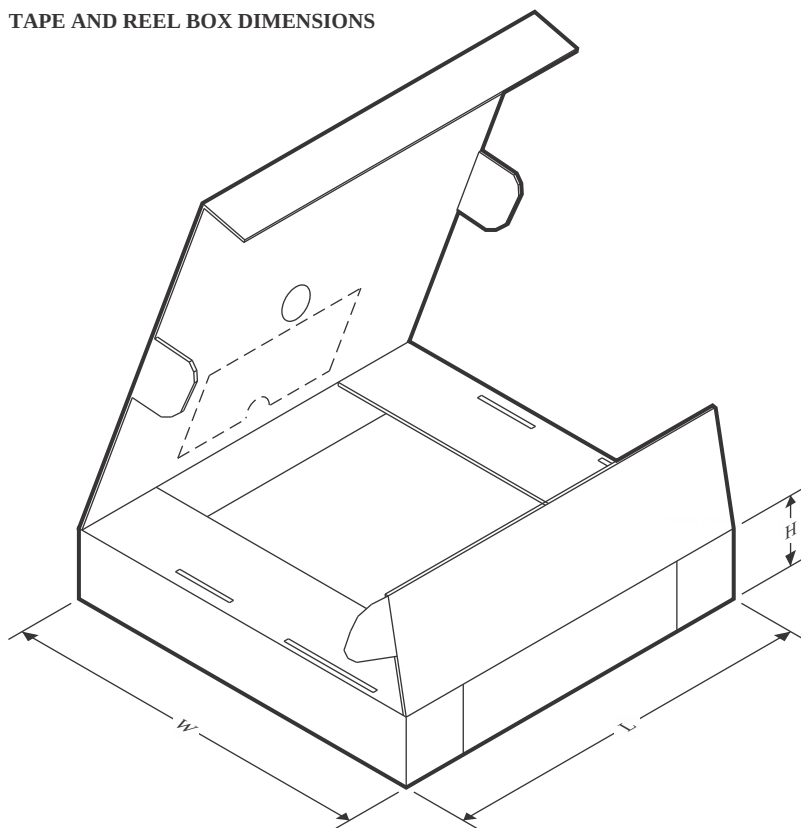
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3436CGEAJDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3436CGEAJDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

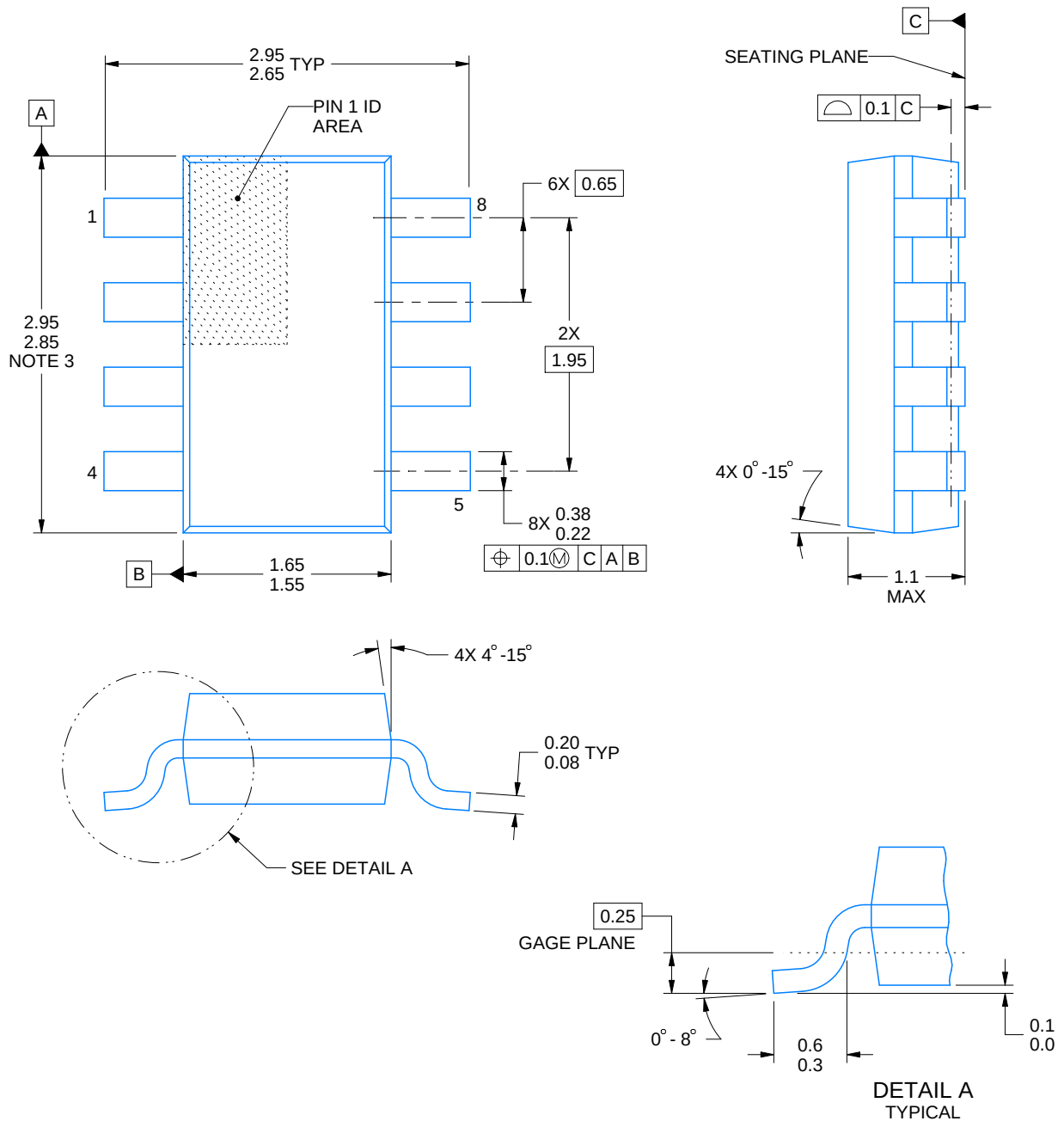
DDF0008A



PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

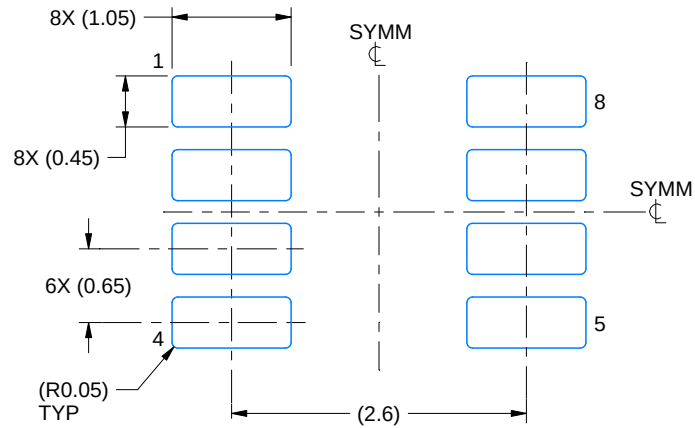
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

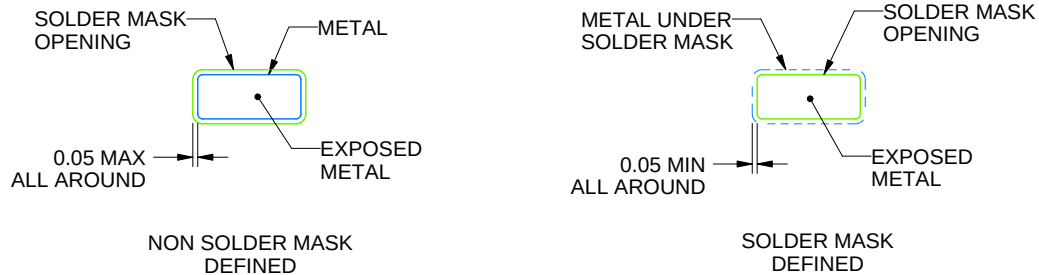
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

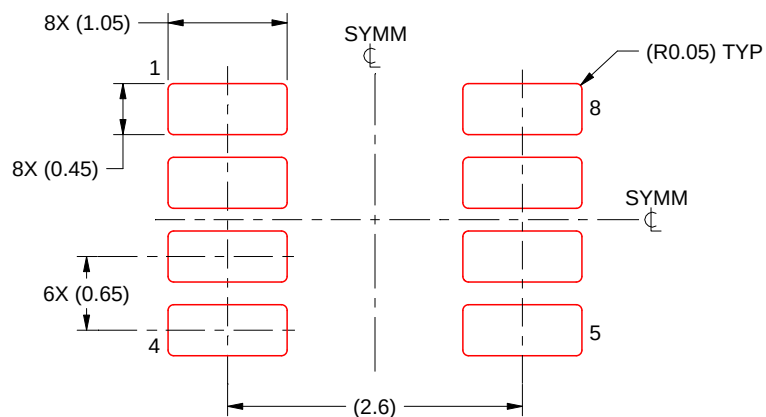
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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