

## ADJUSTABLE BATTERY-BACKUP SUPERVISOR FOR RAM RETENTION

### FEATURES

- Supply Current of 40  $\mu\text{A}$  (Max)
- Battery Supply Current of 100 nA (Max)
- Supply Voltage Supervision Range:
  - Adjustable
  - Other Versions Available on Request
- Backup-Battery Voltage Can Exceed  $V_{DD}$
- Power-On Reset Generator With Fixed 100-ms Reset Delay Time
- Active-High and Active-Low Reset Output
- Chip-Enable Gating: 3 ns (at  $V_{DD} = 5\text{ V}$ ) Max Propagation Delay
- 10-Pin MSOP Package
- Temperature Range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

### APPLICATIONS

- Fax Machines
- Set-Top Boxes
- Advanced Voice Mail Systems
- Portable Battery-Powered Equipment
- Computer Equipment
- Advanced Modems
- Automotive Systems
- Portable Long-Time Monitoring Equipment
- Point-of-Sale Equipment

### DESCRIPTION

The TPS3613-01 supervisory circuit monitors and controls processor activity by providing backup-battery switchover for data retention of CMOS RAM.

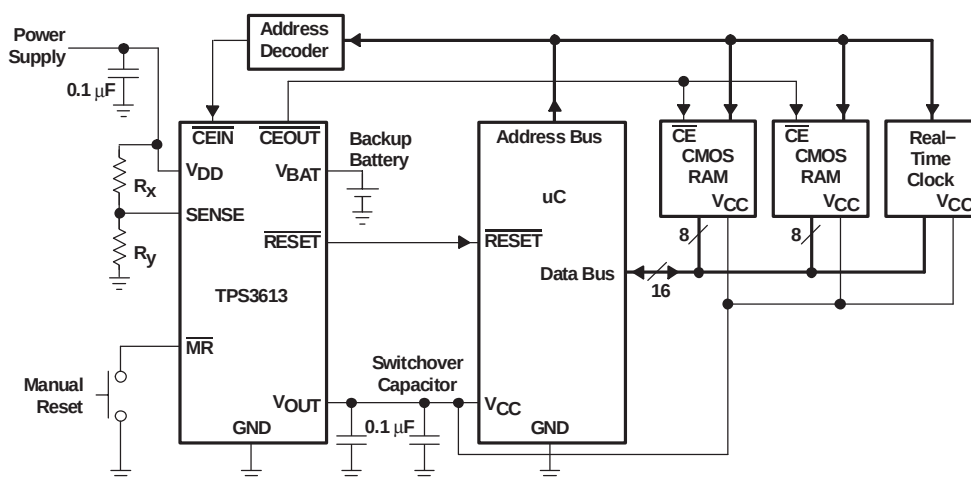
During power-on, reset (RESET and  $\overline{\text{RESET}}$ ) is asserted when the supply voltage ( $V_{DD}$  or  $V_{BAT}$ ) becomes higher than 1.1 V.

Thereafter, the supply voltage supervisor monitors  $V_{DD}$  at the SENSE pin through external feedback resistors and keeps reset active as long as SENSE remains below the threshold voltage,  $V_{IT}$ .

An internal timer delays the release of the reset state to ensure proper system reset. The delay time starts after SENSE rises above the threshold voltage,  $V_{IT}$ .

When SENSE drops below  $V_{IT}$ , reset becomes active again.

The TPS3613-01 is available in a 10-pin MSOP package and is characterized for operation over a temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

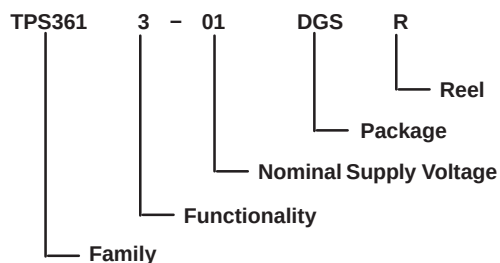
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## PACKAGE INFORMATION

| $T_A$          | DEVICE NAME     | MARKING |
|----------------|-----------------|---------|
| -40°C to +85°C | TPS3613-01DGSR† | AFK     |

† The DGSR passive indicates tape and reel of 2500 parts.

## ordering information application specific versions



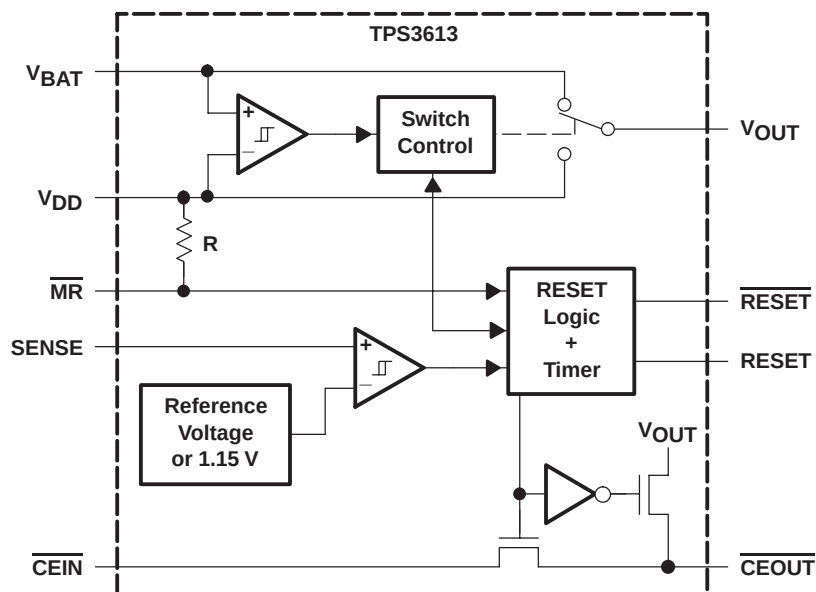
| DEVICE NAME    | NOMINAL VOLTAGE‡, $V_{NOM}$ |
|----------------|-----------------------------|
| TPS3613-01 DGS | Adjustable                  |

‡ For other threshold voltages, contact the local TI sales office for availability and lead-time.

## FUNCTION TABLE

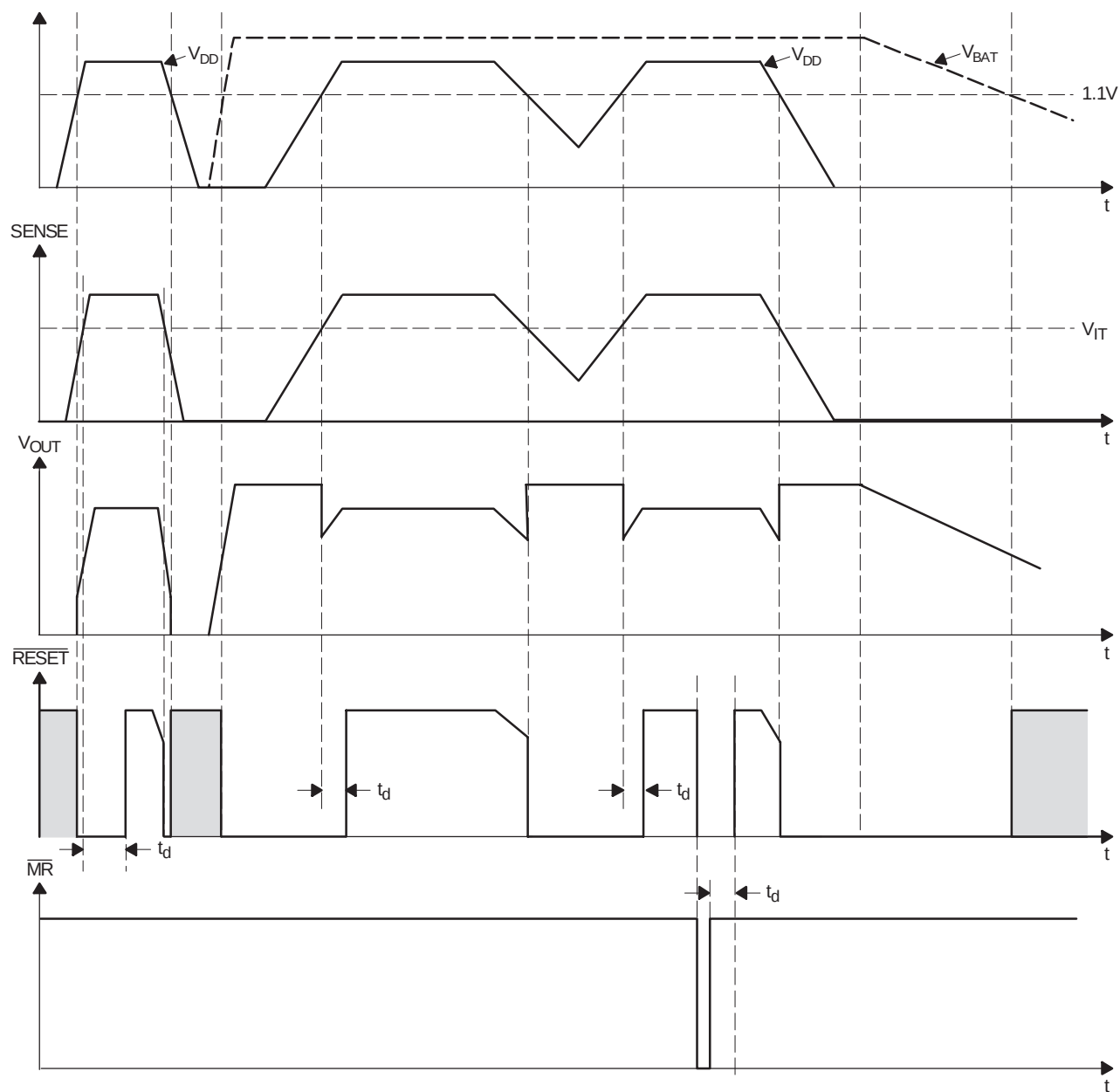
| SENSE > $V_{IT}$ | $V_{DD} > V_{BAT}$ | $\overline{MR}$ | $\overline{CEIN}$ | $V_{OUT}$ | $\overline{RESET}$ | RESET | $\overline{CEOUT}$ |
|------------------|--------------------|-----------------|-------------------|-----------|--------------------|-------|--------------------|
| 0                | 0                  | 0               | 0                 | $V_{BAT}$ | 0                  | 1     | DIS                |
| 0                | 0                  | 0               | 1                 | $V_{BAT}$ | 0                  | 1     | DIS                |
| 0                | 0                  | 1               | 0                 | $V_{BAT}$ | 0                  | 1     | DIS                |
| 0                | 0                  | 1               | 1                 | $V_{BAT}$ | 0                  | 1     | DIS                |
| 0                | 1                  | 0               | 0                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 0                | 1                  | 0               | 1                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 0                | 1                  | 1               | 0                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 0                | 1                  | 1               | 1                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 1                | 0                  | 0               | 0                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 1                | 0                  | 0               | 1                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 1                | 0                  | 1               | 0                 | $V_{DD}$  | 1                  | 0     | 0                  |
| 1                | 0                  | 1               | 1                 | $V_{DD}$  | 1                  | 0     | 1                  |
| 1                | 1                  | 0               | 0                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 1                | 1                  | 0               | 1                 | $V_{DD}$  | 0                  | 1     | DIS                |
| 1                | 1                  | 1               | 0                 | $V_{DD}$  | 1                  | 0     | 0                  |
| 1                | 1                  | 1               | 1                 | $V_{DD}$  | 1                  | 0     | 1                  |

## FUNCTIONAL SCHEMATIC



## Terminal Functions

| TERMINAL           |     | I/O | DESCRIPTION                                                                                                                                         |
|--------------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME               | NO. |     |                                                                                                                                                     |
| $\overline{CEIN}$  | 5   | I   | Chip-enable input                                                                                                                                   |
| $\overline{CEOUT}$ | 6   | O   | Chip-enable output                                                                                                                                  |
| GND                | 3   | I   | Ground                                                                                                                                              |
| $\overline{MR}$    | 4   | I   | Manual reset input                                                                                                                                  |
| RESET              | 7   | O   | Active-high reset output                                                                                                                            |
| $\overline{RESET}$ | 9   | O   | Active-low reset output                                                                                                                             |
| SENSE              | 8   | I   | Adjustable sense input, assumed to be connect to $V_{DD}$ through feedback resistences. Call your local contacts for other application connections. |
| $V_{BAT}$          | 10  | I   | Backup-battery input                                                                                                                                |
| $V_{DD}$           | 2   | I   | Input supply voltage                                                                                                                                |
| $V_{OUT}$          | 1   | O   | Supply output                                                                                                                                       |

**TIMING DIAGRAM**

NOTE: Shaded area in  $\overline{\text{RESET}}$  is undefined.

## detailed description

### backup-battery switchover

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at  $V_{BAT}$ , the device automatically switches the connected RAM to backup power when  $V_{DD}$  fails. In order to allow the backup battery (for example, 3.6-V lithium cells) to have a higher voltage than  $V_{DD}$ , these

supervisors do not connect  $V_{BAT}$  to  $V_{OUT}$  when  $V_{BAT}$  is greater than  $V_{DD}$ .  $V_{BAT}$  only connects to  $V_{OUT}$  (through a 15- $\Omega$  switch) when  $V_{DD}$  falls below  $V_{IT}$  and  $V_{BAT}$  is greater than  $V_{DD}$ . When  $V_{DD}$  recovers, switchover is deferred either until  $V_{DD}$  crosses  $V_{BAT}$ , or when  $V_{DD}$  rises above the reset threshold  $V_{IT}$ .  $V_{OUT}$  connects to  $V_{DD}$  through a 1- $\Omega$  (max) PMOS switch when  $V_{DD}$  crosses the reset threshold.

| $V_{DD} > V_{BAT}$ | $V_{DD} > V_{IT}$ | $V_{OUT}$ |
|--------------------|-------------------|-----------|
| 1                  | 1                 | $V_{DD}$  |
| 1                  | 0                 | $V_{DD}$  |
| 0                  | 1                 | $V_{DD}$  |
| 0                  | 0                 | $V_{BAT}$ |

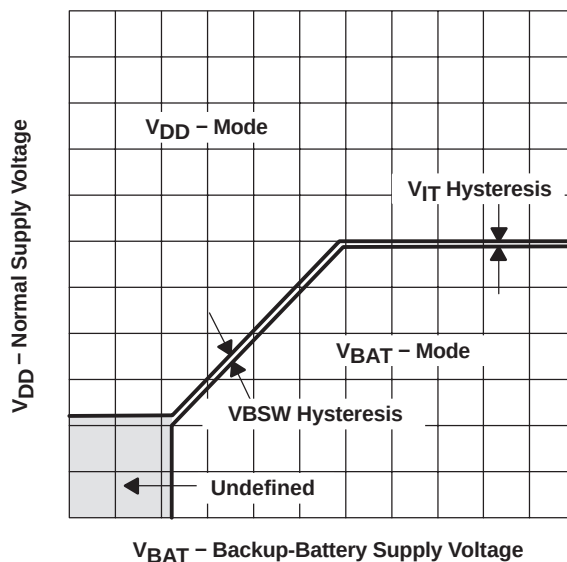


Figure 1.  $V_{DD}$  -  $V_{BAT}$  Switchover

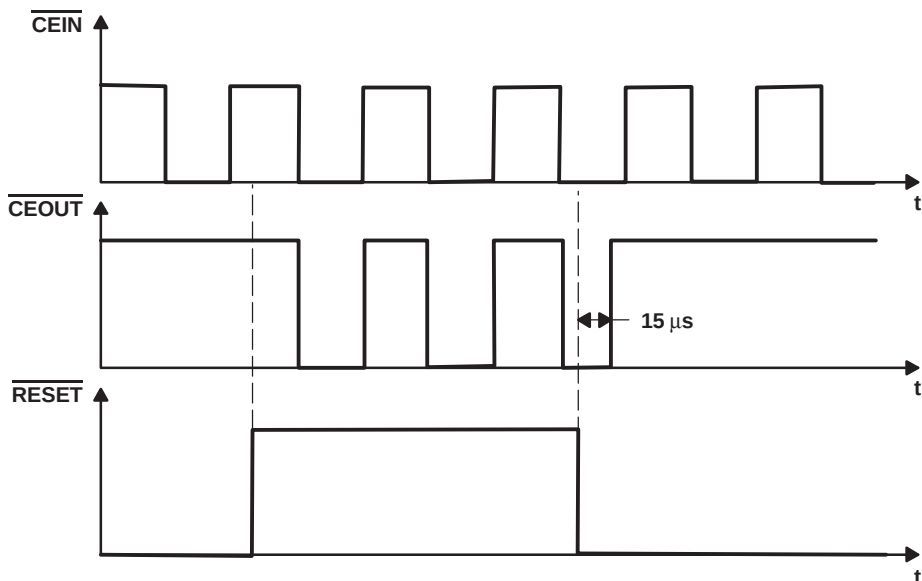
**detailed description (continued)****chip-enable signal gating**

The internal gating of chip-enable ( $\overline{CE}$ ) signals prevents erroneous data from corrupting CMOS RAM during an under-voltage condition. The TPS3613 uses a series transmission gate from  $\overline{CEIN}$  to  $\overline{CEOUT}$ . During normal operation (reset not asserted), the CE transmission gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The short CE propagation delay from  $\overline{CEIN}$  to  $\overline{CEOUT}$  enables the TPS3613 device to be used with most processors.

The CE transmission gate is disabled and  $\overline{CEIN}$  is in high impedance (disable mode) while reset is asserted. During a power-down sequence when  $V_{DD}$  crosses the reset threshold, the CE transmission gate is disabled and  $\overline{CEIN}$  immediately becomes high impedance if the voltage at  $\overline{CEIN}$  is high. If  $\overline{CEIN}$  is low when reset

is asserted, the CE transmission gate is disabled when  $\overline{CEIN}$  goes high, or 15  $\mu s$  after reset asserts, whichever occurs first. This allows the current write cycle to complete during power down. When the CE transmission gate is enabled, the impedance of  $\overline{CEIN}$  appears as a resistor in series with the load at  $\overline{CEOUT}$ . The overall device propagation delay through the CE transmission gate depends on  $V_{OUT}$ , the source impedance of the drive connected to  $\overline{CEIN}$ , and the load at  $\overline{CEOUT}$ . To achieve minimum propagation delay, the capacitive load at  $\overline{CEOUT}$  should be minimized, and a low-output-impedance driver is used.

In the disabled mode, the transmission gate is off and an active pullup connects  $\overline{CEOUT}$  to  $V_{OUT}$ . This pullup turns off when the transmission gate is enabled.

**Figure 2. Chip-Enable Timing**

## ABSOLUTE MAXIMUM RATINGS

### OVER OPERATING FREE-AIR TEMPERATURE (unless otherwise noted)<sup>(1)</sup>

|                                                                        |                               |
|------------------------------------------------------------------------|-------------------------------|
| Supply voltage: $V_{DD}$ <sup>(2)</sup>                                | 7 V                           |
| MR and SENSE pins <sup>(2)</sup>                                       | –0.3 V to ( $V_{DD} + 0.3$ V) |
| Continuous output current at $V_{OUT}$ : $I_O$                         | 400 mA                        |
| All other pins, $I_O$                                                  | ±10 mA                        |
| Continuous total power dissipation                                     | See Dissipation Rating Table  |
| Operating free-air temperature range, $T_A$                            | –40°C to +85°C                |
| Storage temperature range, $T_{stg}$                                   | –65°C to +150°C               |
| Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds | +260°C                        |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation the device must not operate at 7 V for more than  $t = 1000$ h continuously.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq +25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = +25^\circ\text{C}$ | $T_A = +70^\circ\text{C}$<br>POWER RATING | $T_A = +85^\circ\text{C}$<br>POWER RATING |
|---------|----------------------------------------------|----------------------------------------------------|-------------------------------------------|-------------------------------------------|
| DGS     | 424 mW                                       | 3.4 mW/°C                                          | 271 mW                                    | 220 mW                                    |

## RECOMMENDED OPERATING CONDITIONS

|                                                                | MIN                 | MAX                 | UNIT       |
|----------------------------------------------------------------|---------------------|---------------------|------------|
| Supply voltage, $V_{DD}$                                       | 1.65                | 5.5                 | V          |
| Battery supply voltage, $V_{BAT}$                              | 1.5                 | 5.5                 | V          |
| Input voltage, $V_I$                                           | 0                   | $V_{DD} + 0.3$      | V          |
| High-level input voltage, $V_{IH}$                             | $0.7 \times V_{DD}$ |                     | V          |
| Low-level input voltage, $V_{IL}$                              |                     | $0.3 \times V_{DD}$ | V          |
| Continuous output current at $V_{OUT}$ , $I_O$                 |                     | 300                 | mA         |
| Input transition rise and fall rate at MR, $\Delta t/\Delta V$ |                     | 100                 | ns/V       |
| Slew rate at $V_{DD}$ or $V_{bat}$                             |                     | 1                   | V/ $\mu$ s |
| Operating free-air temperature range, $T_A$                    | –40                 | +85                 | °C         |

**ELECTRICAL CHARACTERISTICS****OVER RECOMMENDED OPERATING CONDITIONS (unless otherwise noted)**

| PARAMETER           |                                                    | TEST CONDITIONS                           | MIN                                                                                  | TYP                       | MAX     | UNIT     |
|---------------------|----------------------------------------------------|-------------------------------------------|--------------------------------------------------------------------------------------|---------------------------|---------|----------|
| V <sub>OH</sub>     | High-level output voltage                          | $\overline{\text{RESET}}$                 | V <sub>DD</sub> = 1.8 V, I <sub>OH</sub> = -400 $\mu$ A                              | V <sub>DD</sub> - 0.2 V   |         | V        |
|                     |                                                    |                                           | V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = -2 mA                                     | V <sub>DD</sub> - 0.4 V   |         |          |
|                     |                                                    |                                           | V <sub>DD</sub> = 5 V, I <sub>OH</sub> = -3 mA                                       |                           |         |          |
|                     |                                                    | $\overline{\text{RESET}}$                 | V <sub>DD</sub> = 1.8 V, I <sub>OH</sub> = -20 $\mu$ A                               | V <sub>DD</sub> - 0.3 V   |         |          |
|                     |                                                    |                                           | V <sub>DD</sub> = 3.3 V, I <sub>OH</sub> = -80 $\mu$ A                               | V <sub>DD</sub> - 0.4 V   |         |          |
|                     |                                                    |                                           | V <sub>DD</sub> = 5 V, I <sub>OH</sub> = -120 $\mu$ A                                |                           |         |          |
| V <sub>OL</sub>     | Low-level output voltage                           | $\overline{\text{CEOUT}}$                 | V <sub>OUT</sub> = 1.8 V, I <sub>OH</sub> = -1 mA                                    | V <sub>OUT</sub> - 0.2 V  |         | V        |
|                     |                                                    | Enable mode<br>CEIN = V <sub>OUT</sub>    | V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = -2 mA                                    | V <sub>OUT</sub> - 0.3 V  |         |          |
|                     |                                                    |                                           | V <sub>OUT</sub> = 5 V, I <sub>OH</sub> = -5 mA                                      |                           |         |          |
|                     |                                                    | $\overline{\text{CEOUT}}$<br>Disable mode | V <sub>OUT</sub> = 3.3 V, I <sub>OH</sub> = -0.5 mA                                  | V <sub>OUT</sub> - 0.4 V  |         |          |
|                     |                                                    | $\overline{\text{RESET}}$                 | V <sub>DD</sub> = 1.8 V, I <sub>OL</sub> = 400 $\mu$ A                               |                           | 0.2     |          |
|                     |                                                    | $\overline{\text{RESET}}$                 | V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA                                      |                           | 0.4     |          |
| V <sub>OUT</sub>    | Normal mode                                        |                                           | V <sub>DD</sub> = 5 V, I <sub>OL</sub> = 3 mA                                        |                           | 0.2     | V        |
|                     |                                                    | $\overline{\text{CEOUT}}$                 | V <sub>OUT</sub> = 1.8 V, I <sub>OL</sub> = 1.0 mA                                   |                           | 0.2     |          |
|                     |                                                    | Enable mode<br>CEIN = 0 V                 | V <sub>OUT</sub> = 3.3 V, I <sub>OL</sub> = 2 mA                                     |                           | 0.3     |          |
|                     | Battery-backup mode                                |                                           | V <sub>OUT</sub> = 5 V, I <sub>OL</sub> = 5 mA                                       |                           | 0.3     |          |
|                     |                                                    | Power-up reset<br>voltage (see Note 1)    | V <sub>DD</sub> > 1.1 V or V <sub>BAT</sub> > 1.1 V,<br>I <sub>OL</sub> = 20 $\mu$ A |                           | 0.4     |          |
|                     |                                                    |                                           |                                                                                      |                           | 0.4     |          |
| R <sub>DS(on)</sub> | V <sub>DD</sub> to V <sub>OUT</sub> on-resistance  |                                           | I <sub>O</sub> = 8.5 mA,<br>V <sub>DD</sub> = 1.8 V, V <sub>BAT</sub> = 0 V          | V <sub>DD</sub> - 50 mV   |         | V        |
|                     |                                                    |                                           | I <sub>O</sub> = 125 mA,<br>V <sub>DD</sub> = 3.3 V, V <sub>BAT</sub> = 0 V          | V <sub>DD</sub> - 150 mV  |         |          |
|                     |                                                    |                                           | I <sub>O</sub> = 200 mA,<br>V <sub>DD</sub> = 5 V, V <sub>BAT</sub> = 0 V            | V <sub>DD</sub> - 200 mV  |         |          |
|                     | V <sub>BAT</sub> to V <sub>OUT</sub> on-resistance |                                           | I <sub>O</sub> = 0.5 mA,<br>V <sub>BAT</sub> = 1.5 V, V <sub>DD</sub> = 0 V          | V <sub>BAT</sub> - 20 mV  |         |          |
|                     |                                                    |                                           | I <sub>O</sub> = 7.5 mA,<br>V <sub>BAT</sub> = 3.3 V, V <sub>DD</sub> = 0 V          | V <sub>BAT</sub> - 113 mV |         |          |
|                     |                                                    |                                           |                                                                                      |                           |         |          |
| V <sub>IT</sub>     | Negative-going input threshold<br>(see Note 2)     |                                           | V <sub>DD</sub> = 5 V                                                                | 0.6                       | 1       | $\Omega$ |
|                     |                                                    |                                           | V <sub>BAT</sub> = 3.3 V                                                             | 8                         | 15      |          |
| V <sub>hys</sub>    | Hysteresis                                         | Sense                                     | 1.1 V < V <sub>IT</sub> < 1.65 V                                                     | 12                        |         | mV       |
|                     |                                                    | V <sub>BSW</sub> (see Note 3)             | V <sub>DD</sub> = 1.8 V                                                              | 55                        |         |          |
| I <sub>IH</sub>     | High-level input current                           | $\overline{\text{MR}}$                    | $\overline{\text{MR}}$ = 0.7 x V <sub>DD</sub> , V <sub>DD</sub> = 5 V               | -33                       | -76     | $\mu$ A  |
| I <sub>IL</sub>     | Low-level input current                            | $\overline{\text{MR}}$                    | $\overline{\text{MR}}$ = 0 V, V <sub>DD</sub> = 5 V                                  | -110                      | -255    |          |
| I <sub>I</sub>      | Input current                                      | SENSE                                     | V <sub>DD</sub> = 1.15 V                                                             | -25                       | 25      | nA       |
| I <sub>DD</sub>     | V <sub>DD</sub> supply current                     |                                           | V <sub>OUT</sub> = V <sub>DD</sub>                                                   |                           | 40      | $\mu$ A  |
|                     |                                                    |                                           | V <sub>OUT</sub> = V <sub>BAT</sub>                                                  |                           | 40      |          |
| I <sub>BAT</sub>    | V <sub>BAT</sub> supply current                    |                                           | V <sub>OUT</sub> = V <sub>DD</sub>                                                   | -0.1                      | 0.1     | $\mu$ A  |
|                     |                                                    |                                           | V <sub>OUT</sub> = V <sub>BAT</sub>                                                  |                           | 0.5     |          |
| I <sub>lkg</sub>    | CEIN leakage current                               |                                           | Disable mode, V <sub>I</sub> < V <sub>DD</sub>                                       |                           | $\pm 1$ | $\mu$ A  |
| C <sub>i</sub>      | Input capacitance                                  |                                           | V <sub>I</sub> = 0 V to 5 V                                                          | 5                         |         | pF       |

(1) The lowest voltage at which  $\overline{\text{RESET}}$  becomes active.  $t_r(\text{VDD}) \geq 15 \mu\text{s/V}$ .(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1  $\mu\text{F}$ ) should be placed near to the supply terminals.(3) For V<sub>DD</sub> < 1.6 V, V<sub>OUT</sub> switches to V<sub>BAT</sub> regardless of V<sub>BAT</sub>

**TIMING REQUIREMENTS AT  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = -40^\circ\text{C}$  TO  $+85^\circ\text{C}$** 

| PARAMETER |             |       | TEST CONDITIONS                                                        | MIN | TYP | MAX | UNIT          |
|-----------|-------------|-------|------------------------------------------------------------------------|-----|-----|-----|---------------|
| $t_w$     | Pulse width | SENSE | $V_{IH} = V_{IT} + 0.2\text{ V}$ ,<br>$V_{IL} = V_{IT} - 0.2\text{ V}$ | 6   |     |     | $\mu\text{s}$ |

**SWITCHING CHARACTERISTICS AT  $R_L = 1\text{ M}\Omega$ ,  $C_L = 50\text{ pF}$ ,  $T_A = -40^\circ\text{C}$  TO  $+85^\circ\text{C}$** 

| PARAMETER |                                                       |                                                                                                           | TEST CONDITIONS                                                                                            | MIN | TYP | MAX | UNIT          |
|-----------|-------------------------------------------------------|-----------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-----|-----|-----|---------------|
| $t_d$     | Delay time                                            |                                                                                                           | $V_{SENSE} \geq V_{IT} + 0.2\text{ V}$ ,<br>$MR \geq 0.7 \times V_{DD}$ ,<br>See timing diagram            | 60  | 100 | 140 | ms            |
| $t_{PLH}$ | Propagation (delay) time,<br>low-to-high-level output | 50% $\overline{\text{RESET}}$ to 50% $\overline{\text{CEOUT}}$                                            | $V_{OUT} = V_{IT}$                                                                                         |     | 15  |     | $\mu\text{s}$ |
| $t_{PHL}$ | Propagation (delay) time,<br>high-to-low-level output | 50% $\overline{\text{CEIN}}$ to 50% $\overline{\text{CEOUT}}$ ,<br>$C_L = 50\text{ pF}$ only (see Note 5) | $V_{DD} = 1.8\text{ V}$                                                                                    |     | 5   | 15  | ns            |
|           |                                                       |                                                                                                           | $V_{DD} = 3.3\text{ V}$                                                                                    |     | 1.6 | 5   |               |
|           |                                                       |                                                                                                           | $V_{DD} = 5\text{ V}$                                                                                      |     | 1   | 3   |               |
|           |                                                       | $\overline{\text{SENSE}}$ to $\overline{\text{RESET}}$                                                    | $V_{IL} = V_{IT} - 0.2\text{ V}$ ,<br>$V_{IH} = V_{IT} + 0.2\text{ V}$                                     |     | 2   | 5   | $\mu\text{s}$ |
|           |                                                       | $\overline{\text{MR}}$ to $\overline{\text{RESET}}$                                                       | $V_{SENSE} \geq V_{IT} + 0.2\text{ V}$ ,<br>$V_{IL} = 0.3 \times V_{DD}$ ,<br>$V_{IH} = 0.7 \times V_{DD}$ |     | 0.1 | 1   | $\mu\text{s}$ |
|           | Transition time                                       | $V_{DD}$ to $V_{BAT}$                                                                                     | $V_{IH} = V_{BAT} + 0.2\text{ V}$ ,<br>$V_{IL} = V_{BAT} - 0.2\text{ V}$ ,<br>$V_{BAT} < V_{IT}$           |     |     | 3   | $\mu\text{s}$ |

(1) Assured by design

## TYPICAL CHARACTERISTICS

Table of Graphs

|              |                                                                    |                              | FIGURE         |
|--------------|--------------------------------------------------------------------|------------------------------|----------------|
| $r_{DS(on)}$ | Static drain-source on-state resistance ( $V_{DD}$ to $V_{OUT}$ )  | vs Output current            | 3              |
|              | Static drain-source on-state resistance ( $V_{BAT}$ to $V_{OUT}$ ) | vs Output current            | 4              |
|              | Static drain-source on-state resistance ( $CEIN$ to $CEOUT$ )      | vs Input voltage at $CEIN$   | 5              |
| $I_{DD}$     | Supply current                                                     | vs Supply voltage            | 6              |
| $V_{IT}$     | Input threshold voltage at $\overline{RESET}$                      | vs Free-air temperature      | 7              |
| $V_{OH}$     | High-level output voltage at $\overline{RESET}$                    | vs High-level output current | 8, 9           |
|              | High-level output voltage at $\overline{CEOUT}$                    |                              | 10, 11, 12, 13 |
| $V_{OL}$     | Low-level output voltage at $\overline{RESET}$                     | vs Low-level output current  | 14, 15         |
|              | Low-level output voltage at $\overline{CEOUT}$                     | vs Low-level output current  | 16, 17         |

STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
( $V_{DD}$  to  $V_{OUT}$ )  
vs  
OUTPUT CURRENT

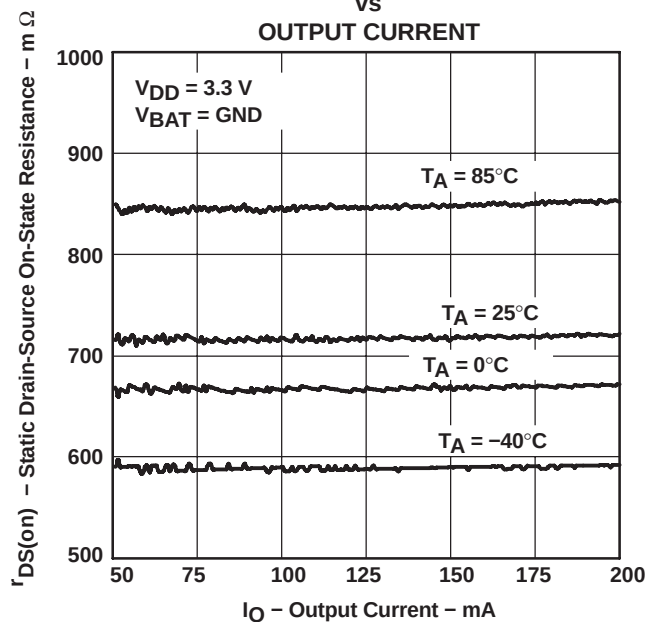


Figure 3

STATIC DRAIN-SOURCE ON-STATE RESISTANCE  
( $V_{BAT}$  to  $V_{OUT}$ )  
vs  
OUTPUT CURRENT

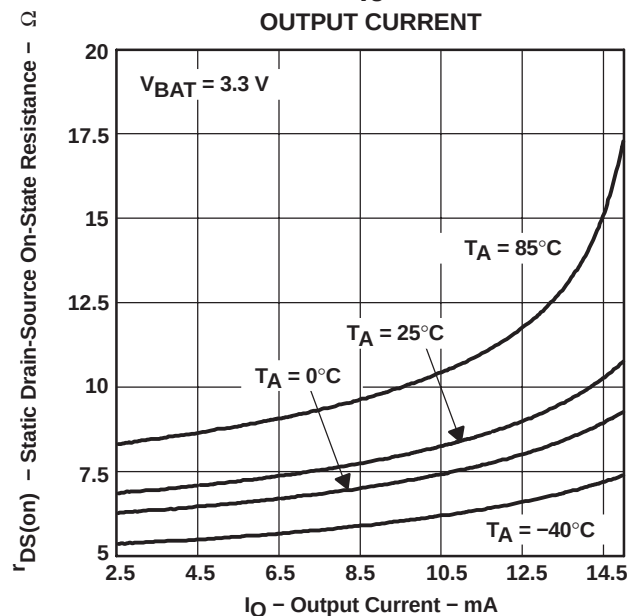


Figure 4

## TYPICAL CHARACTERISTICS

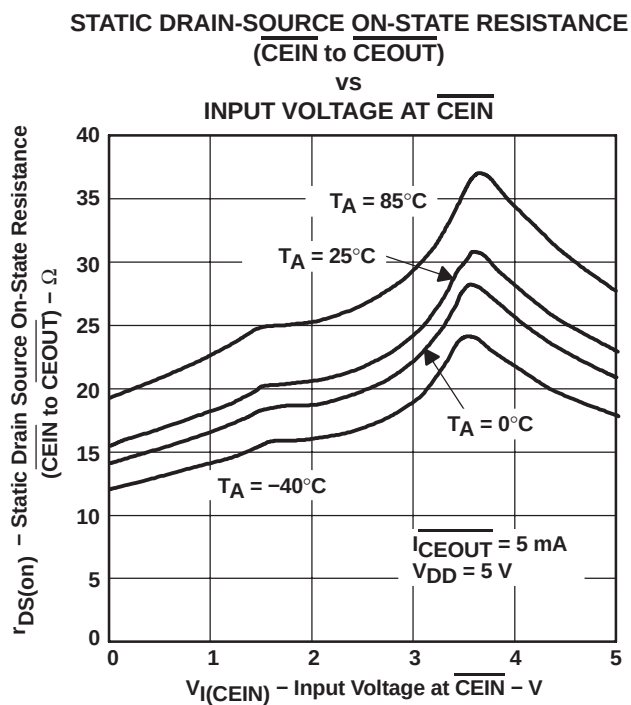


Figure 5

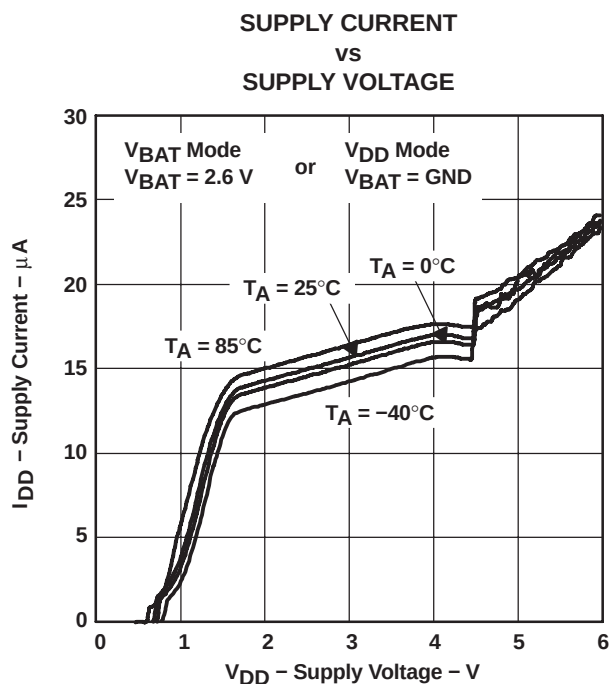


Figure 6

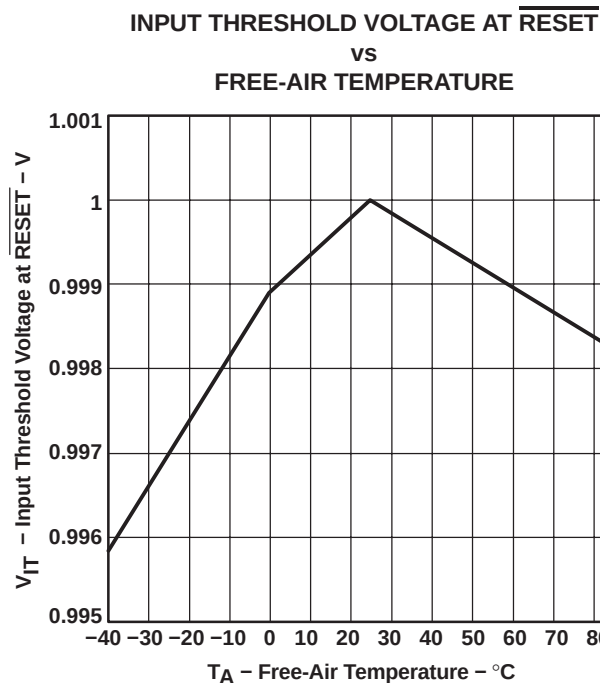


Figure 7

## TYPICAL CHARACTERISTICS

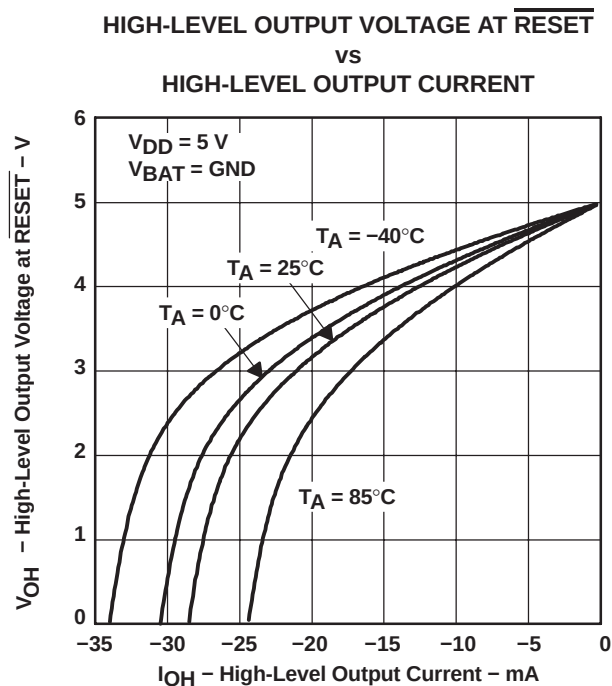


Figure 8

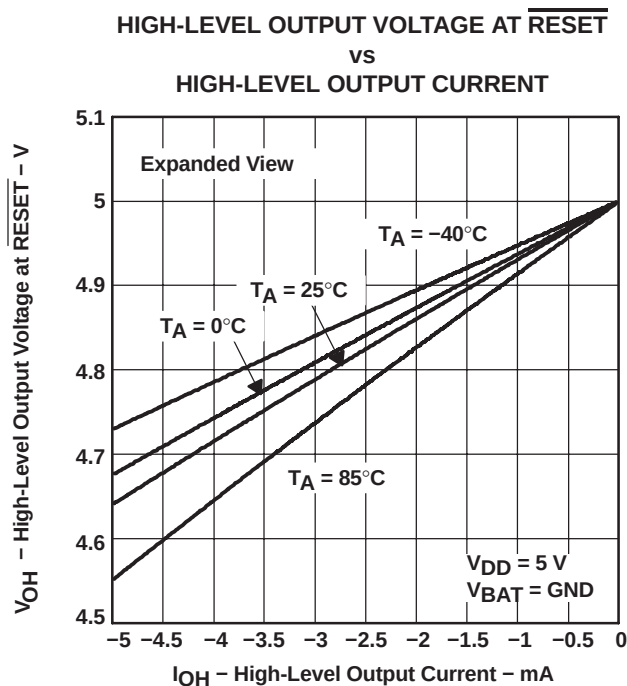


Figure 9

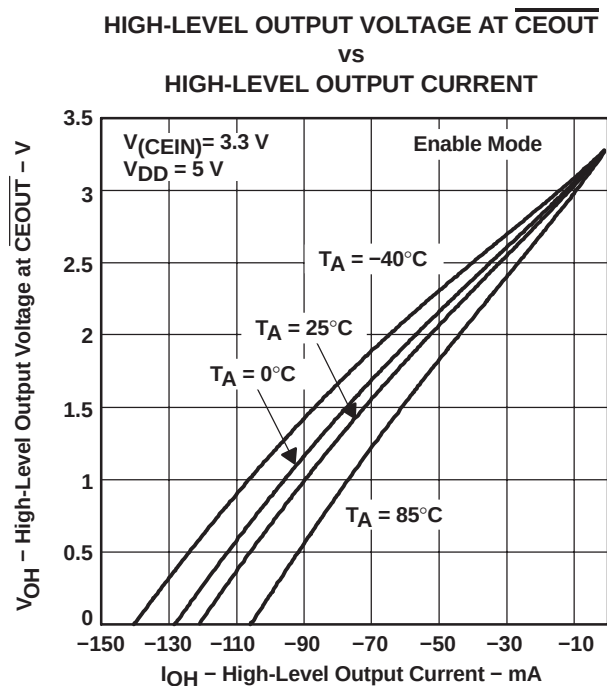


Figure 10

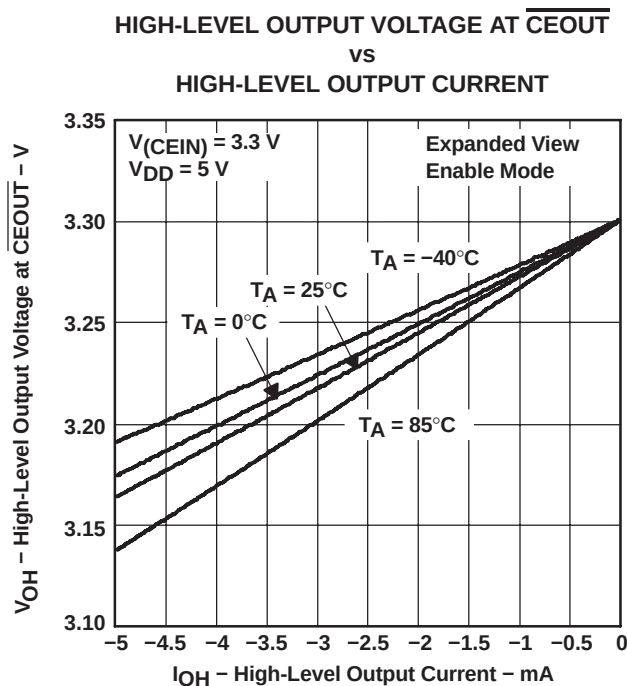
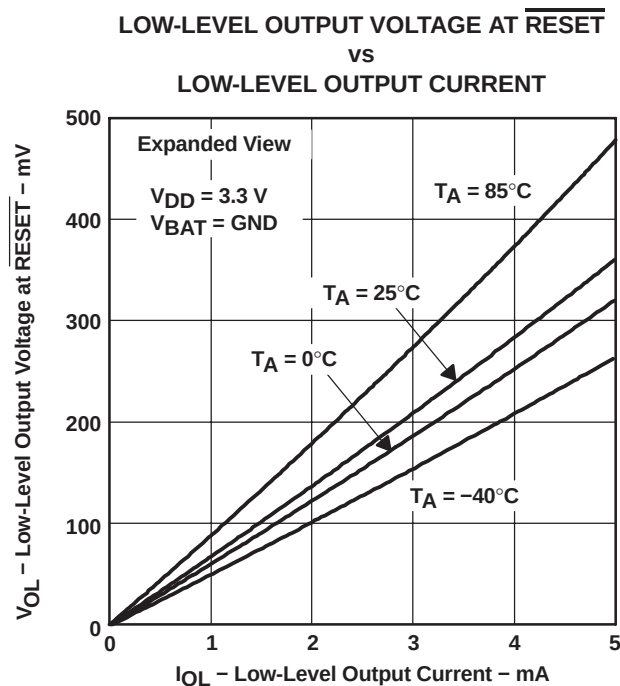
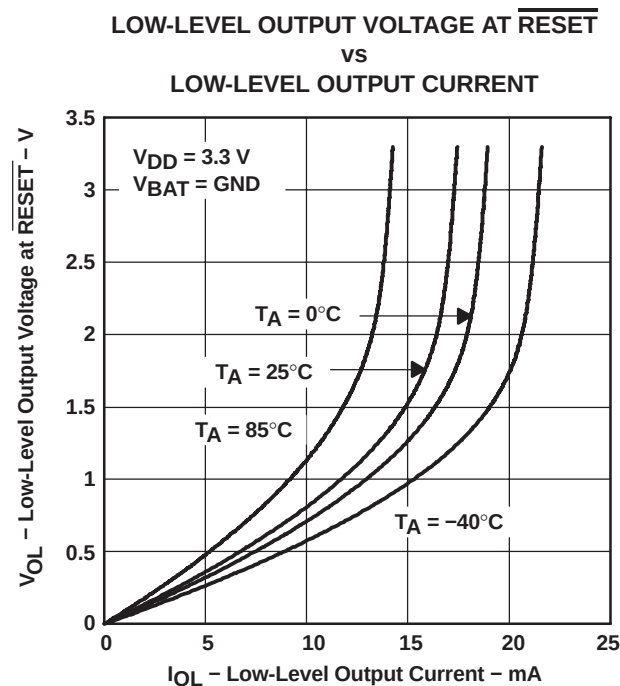
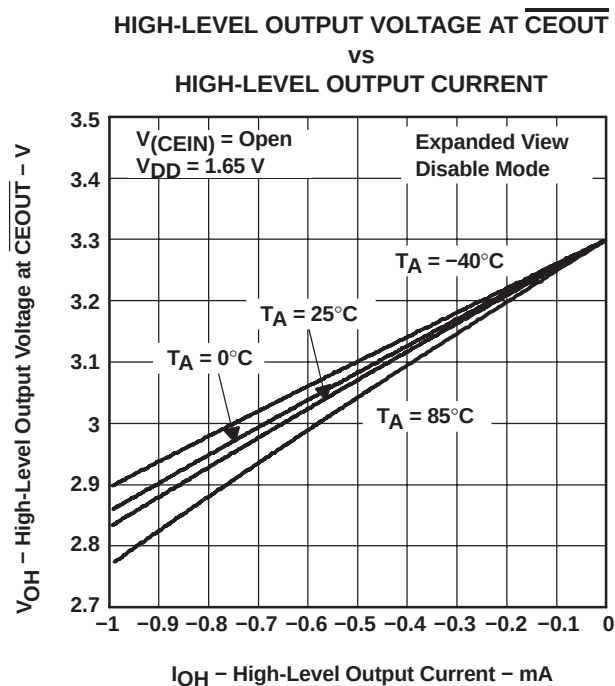
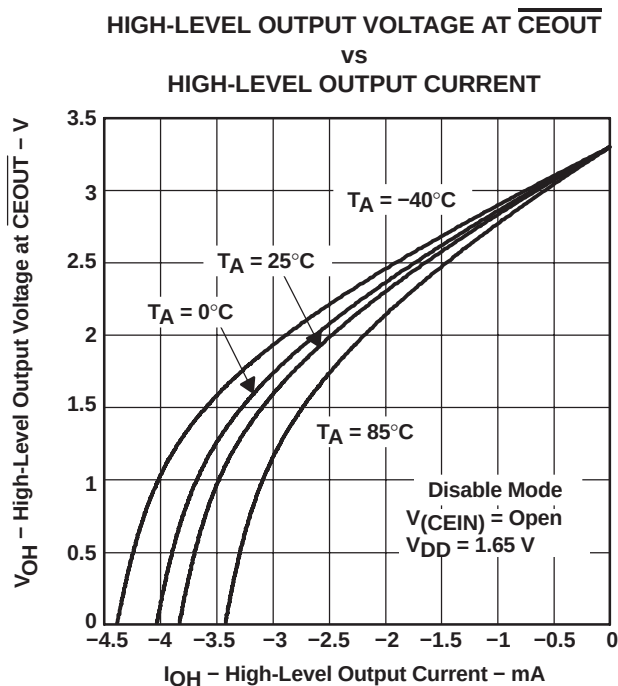


Figure 11

## TYPICAL CHARACTERISTICS



# TYPICAL CHARACTERISTICS

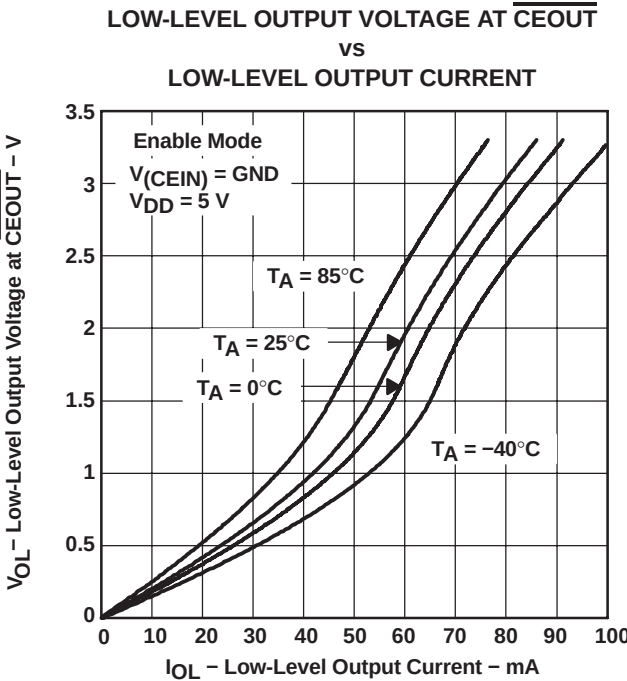


Figure 16

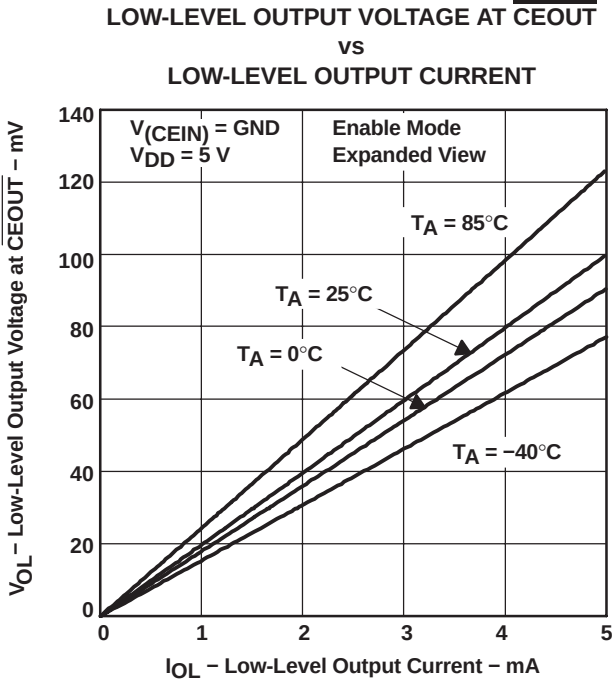


Figure 17

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS3613-01DGS</a>  | Active        | Production           | VSSOP (DGS)   10 | 80   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AFK                 |
| TPS3613-01DGS.A                | Active        | Production           | VSSOP (DGS)   10 | 80   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AFK                 |
| <a href="#">TPS3613-01DGSR</a> | Active        | Production           | VSSOP (DGS)   10 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AFK                 |
| TPS3613-01DGSR.A               | Active        | Production           | VSSOP (DGS)   10 | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AFK                 |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

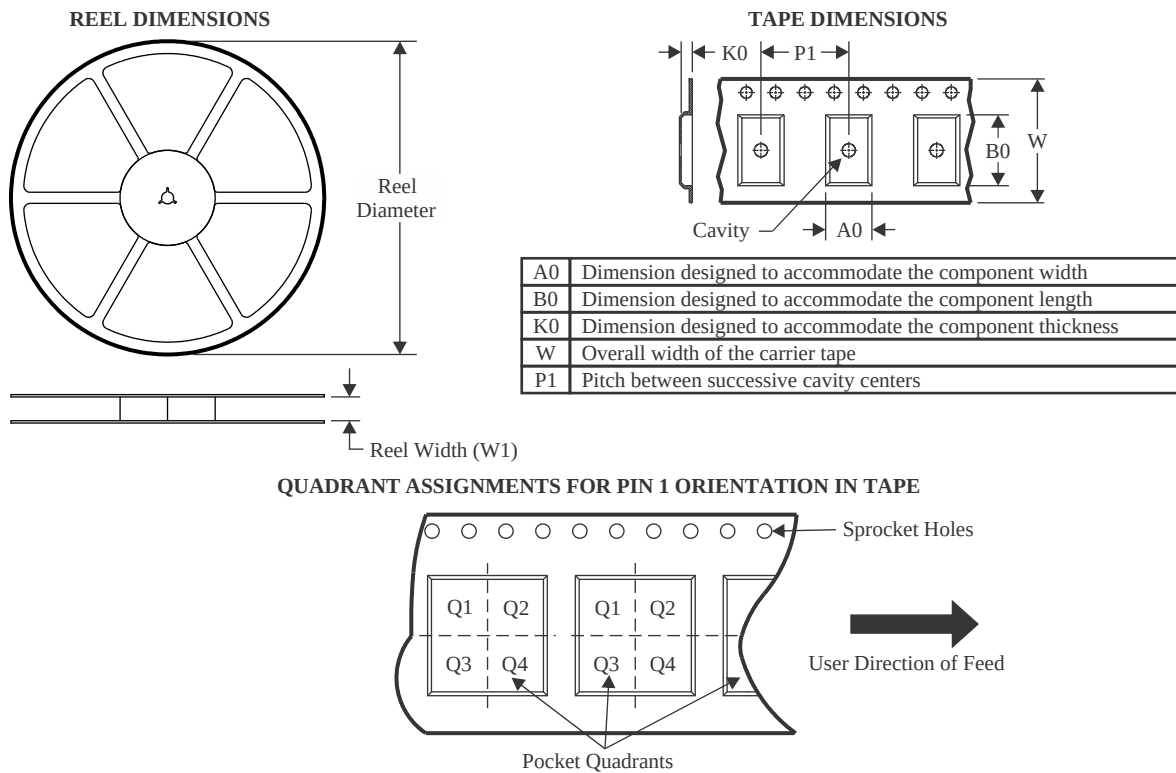
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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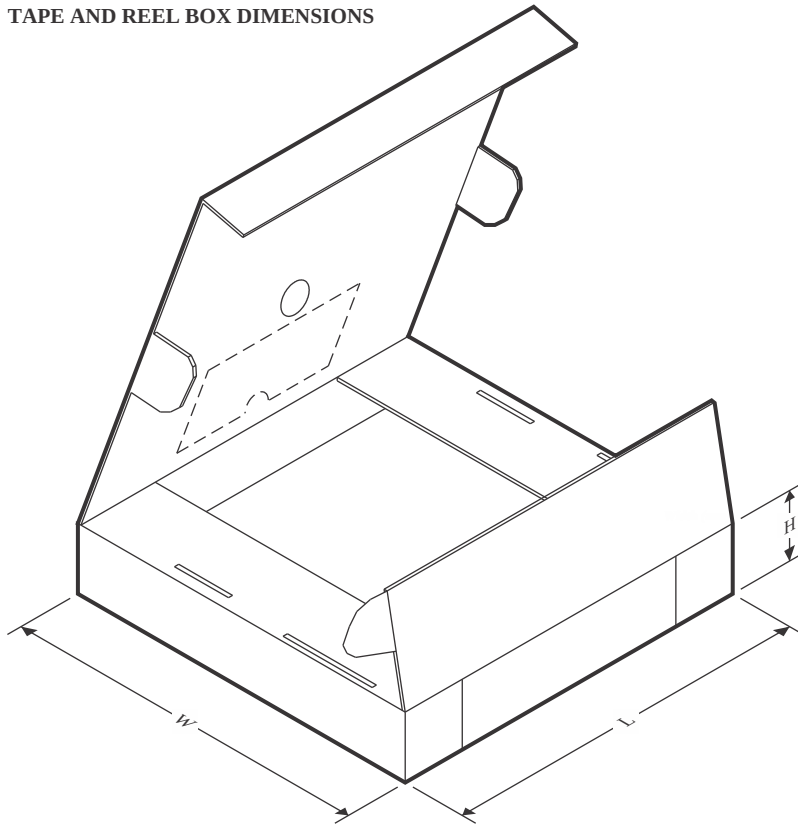
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS3613-01DGSR | VSSOP        | DGS             | 10   | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |

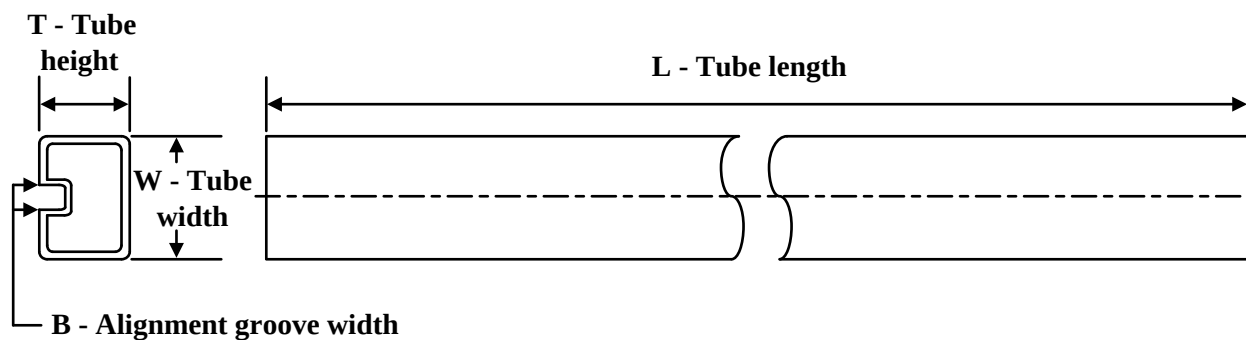
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

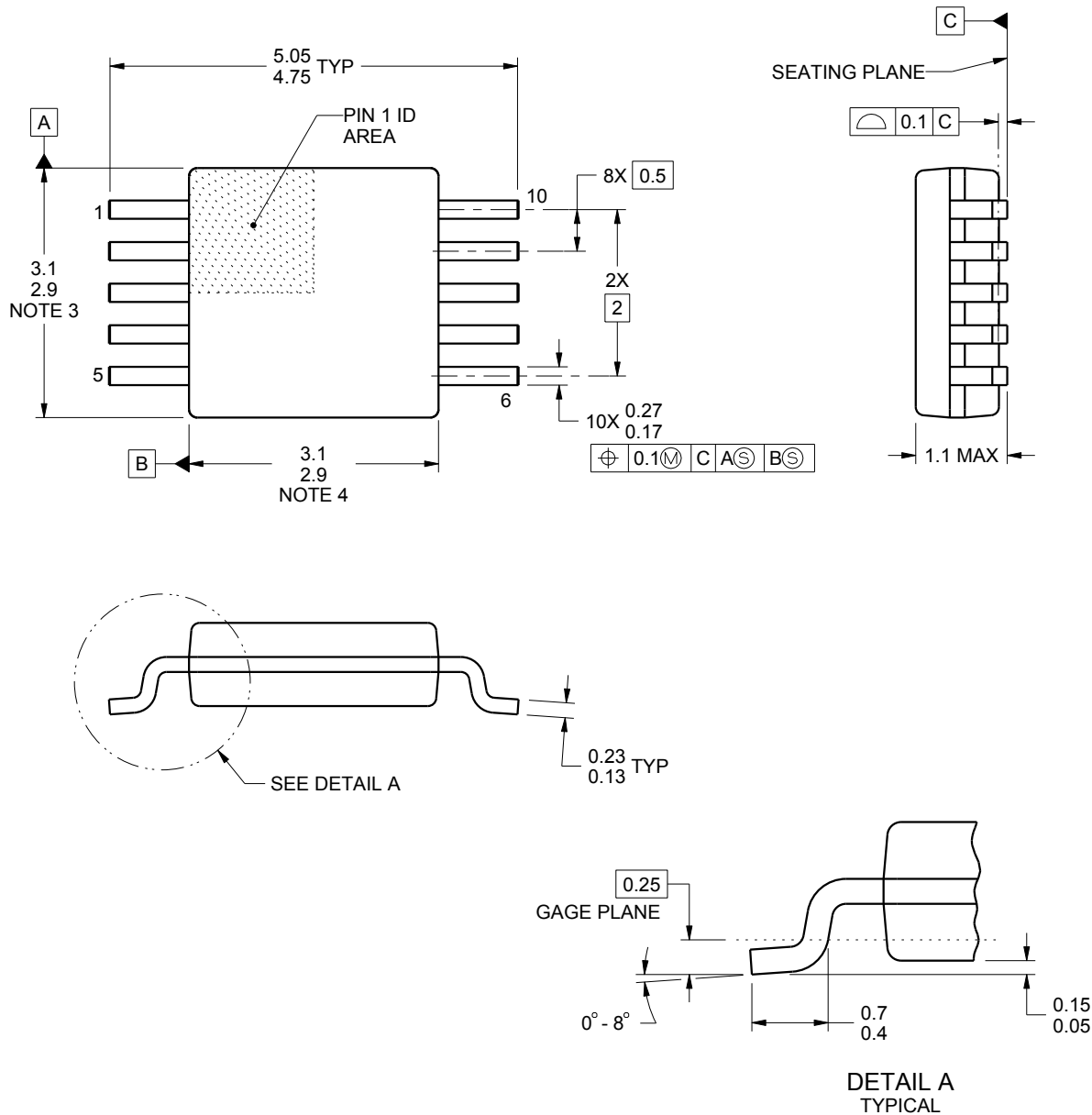
| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS3613-01DGSR | VSSOP        | DGS             | 10   | 2500 | 358.0       | 335.0      | 35.0        |

## TUBE



\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TPS3613-01DGS   | DGS          | VSSOP        | 10   | 80  | 274    | 6.2    | 2540   | 2.5    |
| TPS3613-01DGS.A | DGS          | VSSOP        | 10   | 80  | 274    | 6.2    | 2540   | 2.5    |



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## NOTES:

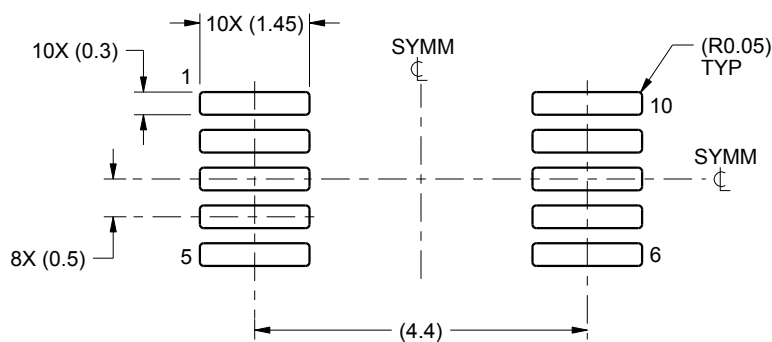
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

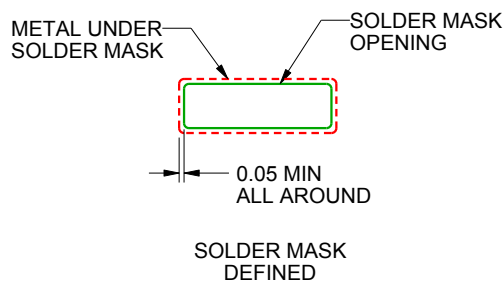
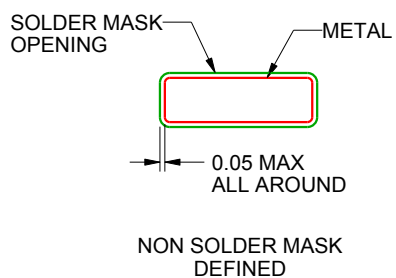
DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

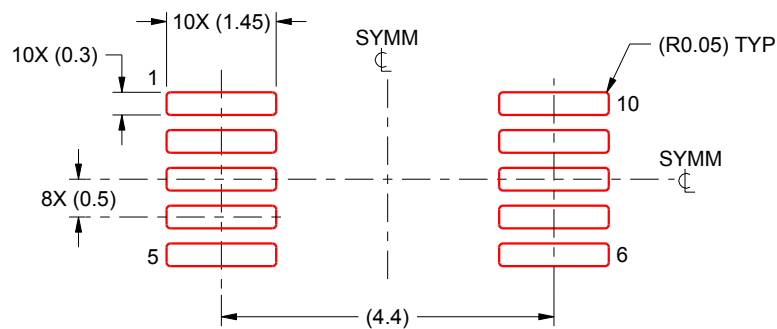
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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