TPS3762-Q1 Automotive 65V, 4µA, Window, Overvoltage or Undervoltage, Supervisor With Built-in Self-Test and Latch

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C
- Functional Safety-Compliant
  - Developed for functional safety applications
  - Documentation to aid ISO 26262 system design
  - Systematic capability up to ASIL-D
  - Hardware capability up to ASIL-D
- Wide input voltage range: 2.7V to 65V
- Low quiescent current: 2µA
- High threshold accuracy: 1% (Max)
- -65V reverse polarity protection on SENSE
- 3µs fast OV/UV monitor for 12V/24V systems
- Fixed and programmable reset time delay
- Fixed and programmable detection delay
- TPS3762-Q1: Integrated Built-in Self-test for diagnostics
  - Built-In Self-Test monitors device for internal faults for functional safety
  - Output reset latching feature

2 Applications

- Sensor fusion and cameras
- Digital cockpit processing unit
- On-board charger
- ADAS domain controller

3 Description

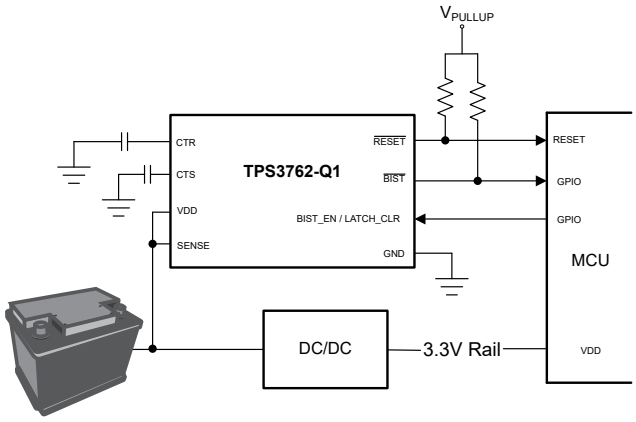
The TPS3762-Q1 is a family of 65V input voltage supervisor with 4µA I_{DD}, 0.9% accuracy, fast detection time (3µs) and a Built-In Self-Test feature. This family of devices can be connected directly to 12V / 24V automotive battery systems for continuous monitoring of overvoltage (OV) and undervoltage (UV) conditions. Wide hysteresis voltage options are available to ignore large voltage transients and prevent false reset signals.

The TPS3762-Q1 output (Reset) that is used for OV and UV faults enabling system to take action if a fault occurs. The TPS3762-Q1 comes with BIST which is implemented at start-up to verify device health as well as an optional latching feature to help the system bring into a safe state when critical faults occurs.

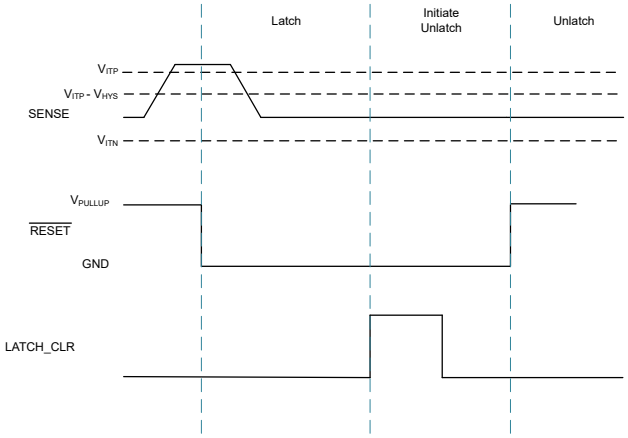
Package Information

PART NUMBER	PACKAGE (1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
TPS3762-Q1	DDF(SOT-23, 8)	2.9mm × 2.8mm	2.9mm × 1.6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Applications Circuit



Latch Functionality Waveform

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

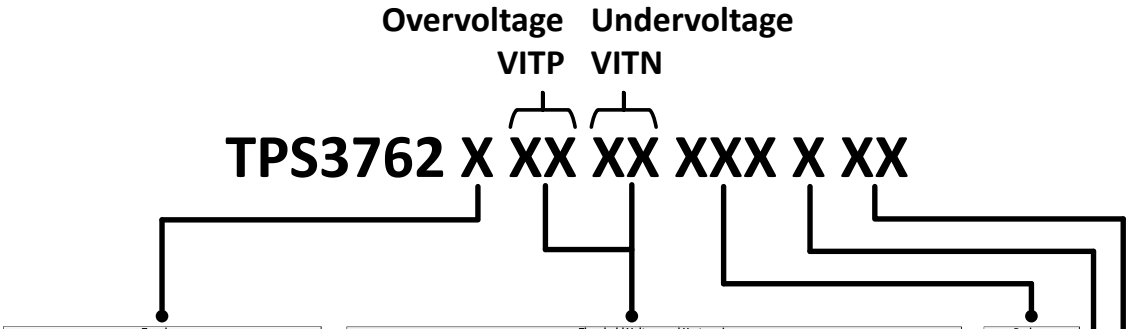
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4 Device Comparison

Device Decoder shows some of the device naming nomenclature of the TPS3762-Q1. Not all device namings follow this nomenclature table. For a detailed breakdown of every device part number by threshold voltage options, BIST configurations, Latch configurations, CTR options, CTS options, and UV bypass, see Section 4.1 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.



Topology

Suffix	RESET Time Delay	Sense Time Delay	Latch / UVbypass	RESET assertion during BIST
A	CTR	CTS	Disabled	Yes
B	CTR	CTS	Latch	Yes
C	CTR	CTS	UVBypass	Yes
D	CTR	CTS	Both Enabled	Yes
E	CTR	Fixed	Disabled	Yes
F	CTR	Fixed	Latch	Yes
G	CTR	Fixed	UVBypass	Yes
H	CTR	Fixed	Both Enabled	Yes
I	CTR	CTS	Disabled	No
J	CTR	CTS	Latch	No
K	CTR	CTS	UVBypass	No
L	CTR	CTS	Both Enabled	No
M	CTR	Fixed	Disabled	No
N	CTR	Fixed	Latch	No
O	CTR	Fixed	UVBypass	No
P	CTR	Fixed	Both Enabled	No
Q	200ms	Fixed	Disabled	Yes
R	200ms	Fixed	Latch	Yes

Threshold Voltage and Hysteresis

2% Hysteresis Option

Suffix	VIT	Suffix	VIT
02	800mV	D7	8.5V
A7	2.7V	D8	9V
A8	2.8V	D9	9.5V
A9	2.9V	E0	10V
B0	3V	E1	11V
B1	3.1V	E2	12V
B2	3.2V	E3	13V
B3	3.3V	E4	14V
B4	3.4V	E5	15V
B5	3.5V	E6	16V
BG	3.6V	E7	17V
B7	3.7V	E8	18V
B8	3.8V	E9	20V
B9	3.9V	F0	22V
C0	4V	F1	24V
C1	4.1V	F2	26V
C2	4.2V	F3	28V
C3	4.3V	F4	30V
C4	4.4V	F5	32V
C5	4.5V	F6	34V
C6	4.6V	F7	35V
C7	4.7V	F8	36V
C8	4.8V	F9	40V
C9	4.9V	G0	45V
D0	5V	G1	50V
D1	5.5V	G2	55V
D2	6V	G3	60V
D3	6.5V		
D4	7V		
D5	7.5V		
D6	8V		
UV	UV Only	OV	OV Only

5% Hysteresis Option

Suffix	VIT	Suffix	VIT
05	800mV	K7	8.5V
H7	2.7V	K8	9V
H8	2.8V	K9	9.5V
H9	2.9V	L0	10V
I0	3V	L1	11V
I1	3.1V	L2	12V
I2	3.2V	L3	13V
I3	3.3V	L4	14V
I4	3.4V	L5	15V
I5	3.5V	L6	16V
IG	3.6V	L7	17V
I7	3.7V	L8	18V
I8	3.8V	L9	20V
I9	3.9V	M0	22V
J0	4V	M1	24V
J1	4.1V	M2	26V
J2	4.2V	M3	28V
J3	4.3V	M4	30V
J4	4.4V	M5	32V
J5	4.5V	M6	34V
J6	4.6V	M7	35V
J7	4.7V	M8	36V
J8	4.8V	M9	40V
J9	4.9V	N0	45V
K0	5V	N1	50V
K1	5.5V	N2	55V
K2	6V	N3	60V
K3	6.5V	N4	65V
K4	7V		
K5	7.5V		
K6	8V		

10% Hysteresis Option

Suffix	VIT	Suffix	VIT
10	800mV	R7	8.5V
O7	2.7V	R8	9V
O8	2.8V	R9	9.5V
O9	2.9V	S0	10V
P0	3V	S1	11V
P1	3.1V	S2	12V
P2	3.2V	S3	13V
P3	3.3V	S4	14V
P4	3.4V	S5	15V
P5	3.5V	S6	16V
PG	3.6V	S7	17V
P7	3.7V	S8	18V
P8	3.8V	S9	20V
P9	3.9V	T0	22V
Q0	4V	T1	24V
Q1	4.1V	T2	26V
Q2	4.2V	T3	28V
Q3	4.3V	T4	30V
Q4	4.4V	T5	32V
Q5	4.5V	T6	34V
Q6	4.6V	T7	35V
Q7	4.7V	T8	36V
Q8	4.8V	T9	40V
Q9	4.9V	U0	45V
R0	5V	U1	50V
R1	5.5V	U2	55V
R2	6V	U3	60V
R3	6.5V	U4	65V
R4	7V		
R5	7.5V		
R6	8V		

0.65% Hysteresis Option

Suffix	VIT	Suffix	VIT
07	800mV	CF	3.6V
AG	2.7V	CG	3.7V
AH	2.8V	CH	3.8V
AI	2.9V	CI	3.9V
AJ	3V	DA	4V
CA	3.1V	DB	4.1V
CB	3.2V	DC	4.2V

Suffix	VIT	Suffix	VIT
CC	3.3V	DD	4.3V
CD	3.4V	DE	4.4V
CE	3.5V	DF	4.5V
DG	4.6V	EG	8V
DH	4.7V	EH	8.5V
DI	4.8V	EI	9V
DJ	4.9V	EJ	9.5V

Suffix	VIT	Suffix	VIT
EA	5V	FA	10V
EB	5.5V	FB	11V
EC	6V	FC	12V
ED	6.5V	FD	13V
EE	7V	FE	14V
EF	7.5V	FF	15V

Package

Suffix	Name
DDF	SOT-23

Reel

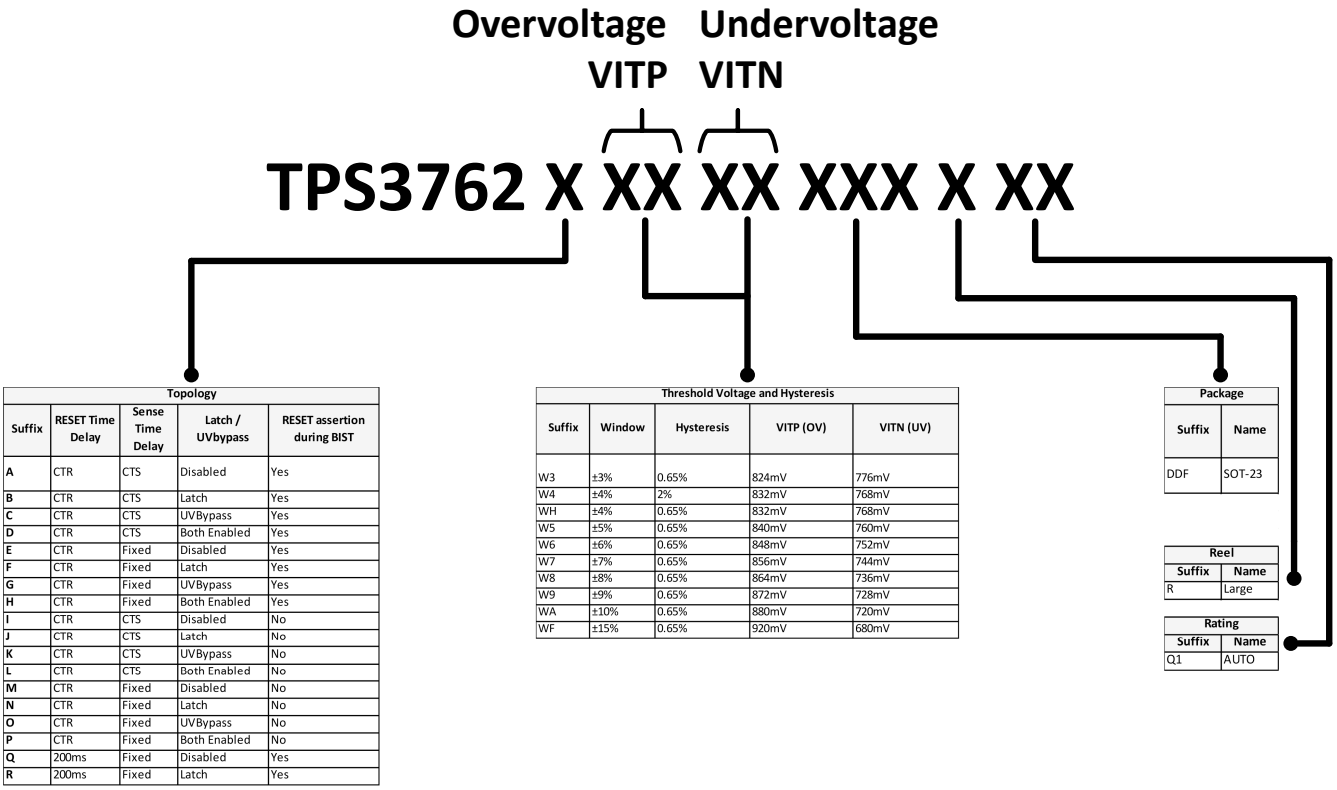
Suffix	Name
R	Large

Rating

Suffix	Name
Q1	AUTO

1. Suffix 02, 05, and 10 with VIT of 800mV corresponds to the adjustable variant, do not have internal voltage divider
2. Refer to Section 4.1 for a decoding table by part number.
3. Refer to Switching Characteristics for Fixed SENSE time delay timing.

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Topology				
Suffix	RESET Time Delay	Sense Time Delay	Latch / UVbypass	RESET assertion during BIST
A	CTR	CTS	Disabled	Yes
B	CTR	CTS	Latch	Yes
C	CTR	CTS	UVBypass	Yes
D	CTR	CTS	Both Enabled	Yes
E	CTR	Fixed	Disabled	Yes
F	CTR	Fixed	Latch	Yes
G	CTR	Fixed	UVBypass	Yes
H	CTR	Fixed	Both Enabled	Yes
I	CTR	CTS	Disabled	No
J	CTR	CTS	Latch	No
K	CTR	CTS	UVBypass	No
L	CTR	CTS	Both Enabled	No
M	CTR	Fixed	Disabled	No
N	CTR	Fixed	Latch	No
O	CTR	Fixed	UVBypass	No
P	CTR	Fixed	Both Enabled	No
Q	200ms	Fixed	Disabled	Yes
R	200ms	Fixed	Latch	Yes

Threshold Voltage and Hysteresis				
Suffix	Window	Hysteresis	VITP (OV)	VITN (UV)
W3	±3%	0.65%	824mV	776mV
W4	±4%	2%	832mV	768mV
WH	±4%	0.65%	832mV	768mV
W5	±5%	0.65%	840mV	760mV
W6	±6%	0.65%	848mV	752mV
W7	±7%	0.65%	856mV	744mV
W8	±8%	0.65%	864mV	736mV
W9	±9%	0.65%	872mV	728mV
WA	±10%	0.65%	880mV	720mV
WF	±15%	0.65%	920mV	680mV

Package	
Suffix	Name
DDF	SOT-23

Reel	
Suffix	Name
R	Large

Rating	
Suffix	Name
Q1	AUTO

4.1 Device Nomenclature

Device Decoder in Section 4 describe how to decode certain device function of the device based on the part number. Not all part numbers follow this nomenclature. Use Table 4-1 as the part number decoding table for all devices.

Table 4-1. Device Configuration Table

ORDERABLE PART NAME	OVERVOLTAGE	UNDERVOLTAGE	SENSE TIME DELAY RESET TIME DELAY	Latch / UVbypass	RESET ASSERTION DURING BIST
TPS3762D02OVDDFRQ1	V_{ITP}: 800mV V_{HYS}: 2%	N/A	SENSE: CTS RESET: CTR	Latch: Enabled UVBypass: Enabled	Enabled
TPS3762EUVF4DDFRQ1	N/A	V_{ITN}: 30.0V V_{HYS}: 2%	SENSE: Fixed RESET: CTR	Latch: Disabled UVBypass: Disabled	Enabled
TPS3762EG4OVDDFRQ1	V_{ITP}: 54.0V V_{HYS}: 2%	N/A	SENSE: Fixed RESET: CTR	Latch: Disabled UVBypass: Disabled	Enabled
TPS3762BUV05DDFRQ1	N/A	V_{ITN}: 800mV V_{HYS}: 5%	SENSE: CTS RESET: CTR	Latch: Enabled UVBypass: Disabled	Enabled
TPS3762EUV02DDFRQ1 Section 4.1	N/A	V_{ITN}: 800mV V_{HYS}: 2%	SENSE: Fixed RESET: CTR	Latch: Disabled UVBypass: Disabled	Enabled

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Table 4-1. Device Configuration Table (continued)

ORDERABLE PART NAME	OVERVOLTAGE	UNDERVOLTAGE	SENSE TIME DELAY RESET TIME DELAY	Latch / UVbypass	RESET ASSERTION DURING BIST
TPS3762F02OVDDFRQ1 1	V_{ITP}: 800mV V_{HYS}: 2%	N/A	SENSE: Fixed RESET: CTR	Latch: Enabled UVBypass: Disabled	Enabled
TPS3762DW4W4DDFRQ1 1	V_{ITP}: 832mV V_{HYS}: 2%	V_{ITN}: 768mV V_{HYS}: 2%	SENSE: CTS RESET: CTR	Latch: Enabled UVBypass: Enabled	Enabled

1. Contact TI sales representatives or on TI's E2E forum for details and availability of other options
2. Refer to Switching Characteristics for Fixed SENSE time delay timings.
3. Product preview. Please check with a Texas Instruments representative for availability

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5 Pin Configuration and Functions

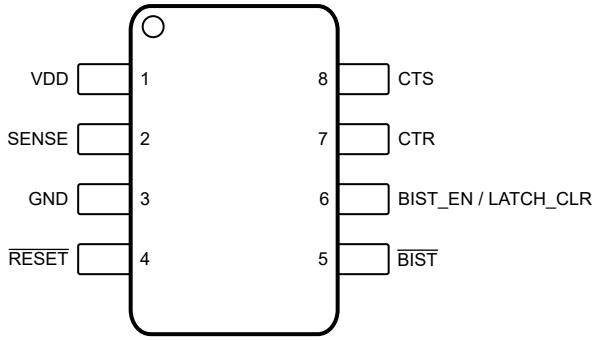


**Figure 5-1. DDF Package,
8-Pin SOT-23,
TPS3762-Q1 (Top View)**

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VDD	1	I	**Input Supply Voltage:** Supply voltage pin. For noisy systems, bypass with a 0.1µF capacitor to GND.
SENSE	2	I	**Sense Voltage:** Connect this pin to the supply rail that must be monitored. See Section 8.3.2 for more details. Sensing Topology: **Overvoltage (OV) or Undervoltage (UV) or Window (OV + UV)**
GND	3	-	**Ground.** Ground pin. All GND pins must be electrically connected to the board ground.
$\overline{\text{RESET}}$	4	O	**Output Reset Signal:** $\overline{\text{RESET}}$ asserts when SENSE crosses the voltage threshold after the sense time delay, set by CTS, and remains asserted for the reset time delay period, set by CTR, after SENSE transitions out of a fault condition. For latch variants $\overline{\text{RESET}}$ remains asserted until the latch is cleared. The active low open-drain reset output requires an external pullup resistor. See Section 8.3.3.2 for more details. Output topology: **Open-Drain Active-Low**
$\overline{\text{BIST}}$	5	O	**Built-In Self-Test:** $\overline{\text{BIST}}$ asserts when a logic high input occurs on the BIST_EN / LATCH_CLR or BIST_EN pin, this initiates the internal BIST testing. $\overline{\text{BIST}}$ recovers after $t_{\overline{\text{BIST}}}$ to signify BIST completed successfully. $\overline{\text{BIST}}$ remains asserted for a time period longer than $t_{\overline{\text{BIST}}}$ if there is a failure during BIST. $\overline{\text{BIST}}$ active-low open-drain output requires an external pullup resistor. See Section 8.3.6 for more details.
BIST_EN / LATCH_CLR	6	I	**Built-in Self-test Enable and Latch Clear:** A rising edge input must occur on the BIST_EN / LATCH_CLR to initiate BIST. For devices with latch enabled, a logic low input enables latch and a logic high input disables/clears latch. Pin 6 features an internal 100kΩ pulldown resistor which enables latch a startup. See Section 8.3.6 for more details.
CTR	7	O	**RESET Time Delay:** User-programmable reset time delay for $\overline{\text{RESET}}$. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section8.3.4 for more details.
CTS	8	O	**SENSE Time Delay:** User-programmable sense time delay for SENSE. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 8.3.5 for more details.

(1) I = Input; O = Output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted (1)

		MIN	MAX	UNIT
Voltage	V_{DD}, $V_{SENSE(Adjustable)}$, $V_{\overline{RESET}}$	–0.3	70	V
Voltage	$V_{SENSE(Fixed)}$	–65	70	V
Voltage	V_{CTS}, V_{CTR}	–0.3	6	V
Voltage	V_{BIST}, V_{BIST_EN}, $V_{BIST_EN/LATCH_CLR}$	–0.3	6	V
Current	I_{RESET}, I_{BIST}		10	mA
Temperature (2)	Operating junction temperature, T_J	–40	150	°C
Temperature (2)	Operating Ambient temperature, T_A	–40	150	°C
Temperature (2)	Storage, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) As a result of the low dissipated power in this device, T_J is assumed to be equal to T_A.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	2.7		65	V
Voltage	V_{DD} (50ms transient)(2)			70	V
Voltage	V_{SENSE}, $V_{\overline{RESET}}$	0		65	V
Voltage	V_{CTS}, V_{CTR}	0		5.5	V
Voltage	$V_{\overline{BIST}}$, V_{BIST_EN}, $V_{BIST_EN/LATCH_CLR}$	0		5.5	V
Current	$I_{\overline{RESET}}$, $I_{\overline{BIST}}$	0		5	mA
T_J (1)	Junction temperature (free air temperature)	–40		125	°C

(1) As a result of the low dissipated power in this device, T_J is assumed to be equal to T_A.
(2) This is a transient specification, operating the device repeatedly under this condition can affect device lifetime.

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6.4 Thermal Information

THERMAL METRIC (1)		TPS3762-Q1	UNIT
		DDF	
		8-PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.5 Electrical Characteristics

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, output $\overline{RESET}$ pullup resistor R_{PU} = 10kΩ, voltage V_{PU} = 5.5V, output $\overline{BIST}$ pullup resistor $R_{PU_\overline{BIST}}$ = 10kΩ, voltage $V_{PU_\overline{BIST}}$ = 5.5V, and load C_{LOAD} = 10pF. The operating free-air temperature range T_A = –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12V and V_{IT} = 6.5V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{DD}	Supply Voltage		2.7		65	V
UVLO (1)	Undervoltage Lockout	V_{DD} rising above $V_{DD\ (MIN)}$			2.6	V
UVLO(HYS) (1)	Undervoltage Lockout Hysteresis	V_{DD} falling below $V_{DD\ (MIN)}$		500		mV
$V_{POR(\overline{RESET})}$	Power on Reset Voltage (2) $\overline{RESET}$, Active Low (Open-Drain)	$V_{OL(MAX)}$ = 300mV $I_{OUT\ (Sink)}$ = 15µA			1.4	V
$V_{POR(\overline{BIST})}$	Power on Reset Voltage (2) $\overline{BIST}$, Active Low (Open-Drain)	$V_{OL(MAX)}$ = 300mV $I_{OUT\ (Sink)}$ = 15µA			1.4	V
I_{DD}	Supply current into V_{DD} pin	V_{IT} = 800mV $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$		4	8.1	µA
I_{DD}	Supply current into VDD pin	V_{IT} = 2.7V to 65V $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$			8.1	µA
SENSE (Input)						
I_{SENSE}	Input current	V_{IT} = 800mV			200	nA
I_{SENSE}	Input current	V_{IT} = 2.7V to 65V		1.5	5	µA
V_{ITN}	Input Threshold Negative (Undervoltage)	V_{ITN} = 2.7V to 65V	-1		1	%
V_{ITN}	Input Threshold Negative (Undervoltage)	V_{ITN} = 800mV (3)	-0.9		0.9	%
V_{ITP}	Input Threshold Positive (Overvoltage)	V_{ITP} = 2.7V to 65V	-1		1	%
V_{ITP}	Input Threshold Positive (Overvoltage)	V_{ITP} = 800mV (3)	-0.9		0.9	%
V_{HYS}	Hysteresis Accuracy (4)	V_{IT} = 0.8V and 2.7V to 65V V_{HYS} Range = 0.7%	0.6	0.7	0.8	%
V_{HYS}	Hysteresis Accuracy (4)	V_{HYS} Range = 2%	1.5	2	2.5	%
V_{HYS}	Hysteresis Accuracy (4)	V_{HYS} Range = 5%	4.5	5	6	%
V_{HYS}	Hysteresis Accuracy (4)	V_{HYS} Range = 10%	9	10	11	%
$\overline{RESET}$ (Output)						
$I_{lkg(OD)}$	Open-Drain leakage	$V_{\overline{RESET}}$ = 5.5V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$I_{lkg(OD)}$	Open-Drain leakage	$V_{\overline{RESET}}$ = 65V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
V_{OL} (5)	Low level output voltage	2.7V ≤ VDD ≤ 65V $I_{\overline{RESET}}$ = 2.7mA			350	mV

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6.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, output $\overline{RESET}$ pullup resistor R_{PU} = 10kΩ, voltage V_{PU} = 5.5V, output $\overline{BIST}$ pullup resistor $R_{PU_\overline{BIST}}$ = 10kΩ, voltage $V_{PU_\overline{BIST}}$ = 5.5V, and load C_{LOAD} = 10pF. The operating free-air temperature range T_A = –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12V and V_{IT} = 6.5V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR)		2.96	3.7	4.44	MΩ
R_{CTS}	Internal resistance (CTS)		2.96	3.7	4.44	MΩ
Built-in Self-test						
$I_{lkg(\overline{BIST})}$	Open-Drain leakage	$V_{\overline{BIST}}$ = 5.5V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$I_{lkg(\overline{BIST})}$	Open-Drain leakage	$V_{\overline{BIST}}$ = 3.3V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$V_{\overline{BIST}_OL}$	Low level output voltage	2.7V ≤ VDD ≤ 65V $I_{\overline{BIST}}$ = 5mA			300	mV
V_{BIST_EN}	BIST_EN pin logic low input				500	mV
V_{BIST_EN}	BIST_EN pin logic high input		1300			mV
$V_{BIST_EN/LATCH_CLR}$	LATCH_CLR pin logic low input				500	mV
$V_{BIST_EN/LATCH_CLR}$	LATCH_CLR pin logic high input		1300			mV

(1) When V_{DD} voltage falls below UVLO, $\overline{RESET}$ is asserted. V_{DD} slew rate ≤ 100 mV / µs
(2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below V_{POR}, the output cannot be determined. V_{DD} slew rate ≤ 100mV/µs
(3) For adjustable voltage guidelines and resistor selection refer to Adjustable Voltage Thresholds in Application and Implementation section
(4) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.
(5) For V_{OH} and V_{OL} relation to output variants refer to Timing Figures after the Timing Requirement Table

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6.6 Switching Requirements

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, output $\overline{RESET}$ pullup resistor R_{PU} = 10kΩ, voltage V_{PU} = 5.5V, output $\overline{BIST}$ pullup resistor $R_{PU_\overline{BIST}}$ = 10kΩ, voltage $V_{PU_\overline{BIST}}$ = 5.5V, and load C_{LOAD} = 10pF. The operating free-air temperature range T_A = –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12V and V_{IT} = 6.5V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Switching Requirements						
$t_{CTR(No\ Cap)}$	$\overline{RESET}$ release time delay (CTR) (1)	VIT = 800mV C_{CTR} = Open 20% Overdrive from Hysteresis		350	600	µs
$t_{CTR(No\ Cap)}$	$\overline{RESET}$ release time delay (CTR) (1)	VIT = 2.7V to 65V C_{CTR} = Open 20% Overdrive from Hysteresis			670	µs
t_{pd}	CTS = Disabled (5)	VITP = 800mV 20% Overdrive from V_{IT}		1.2	3	µs
t_{pd}	CTS = Disabled (5)	VITN = 800mV 20% Overdrive from V_{IT}		2	5	µs
t_{pd}	CTS = Disabled	VITP = 2.7V to 65V 20% Overdrive from V_{IT}		10	36	µs
t_{pd}	CTS = Disabled	VITN = 2.7V to 65V 20% Overdrive from V_{IT}		10	36	µs
t_{CTS}	Sense detect time delay (CTS) (2) (4)	VIT = 800mV C_{CTS} = Open 20% Overdrive from V_{IT}		85	100	µs
t_{CTS}	Sense detect time delay (CTS) (2) (4)	VIT = 2.7V to 65V C_{CTS} = Open 20% Overdrive from V_{IT}		85	120	µs
t_{SD}	Startup Delay (3)	C_{CTR} = Open		1		ms
BIST Switching Requirements						
$t_{BIST_en_pd}$	Rising edge of BIST_EN to BIST asserting			2.3		µs
$t_{BIST_en_pd}$	Rising edge of BIST_EN to RESET asserting			2.3		µs
$t_{\overline{BIST}_recover}$	Rising edge of $\overline{BIST}$ to SENSE input valid	C_{CTR} = Open, BIST = Enabled		350	600	µs
$t_{\overline{BIST}}$	BIST run time				3.5	ms
$t_{SD+\overline{BIST}}$	Startup time with BIST run time				4.5	ms
LATCH Switching Requirements						
$t_{BIST_EN/LATCH_CLR_Recover}$	Rising edge of $\overline{BIST}$ to SENSE input valid	C_{CTR} = Open, BIST = Disabled		10		µs

(1) **CTR Reset detect time delay:**
Overvoltage active-low output is measure from $V_{ITP\ -\ HYS}$ to V_{OH}
Undervoltage active-low output is measure from $V_{ITN\ +\ HYS}$ to V_{OH}

(2) **CTS Sense detect time delay:**
Overvoltage active-low output is measure from V_{ITP} to V_{OL}
Undervoltage active-low output is measure from V_{ITN} to V_{OL}

(3) During the power-on sequence, V_{DD} must be at or above $V_{DD\ (MIN)}$ for at least $t_{SD+\overline{BIST}} + t_{CTR}$ before the output is in the correct state based on V_{SENSE}.
t_{SD} time includes the propagation delay (C_{CTR} = Open). Capacitor on CTR will add time to t_{SD}.

(4) C_{CTS} = Open assumes there is less than 20pF of parasitic capacitance on the pin.

(5) This parameter is established by design or characterization and is not tested in production.

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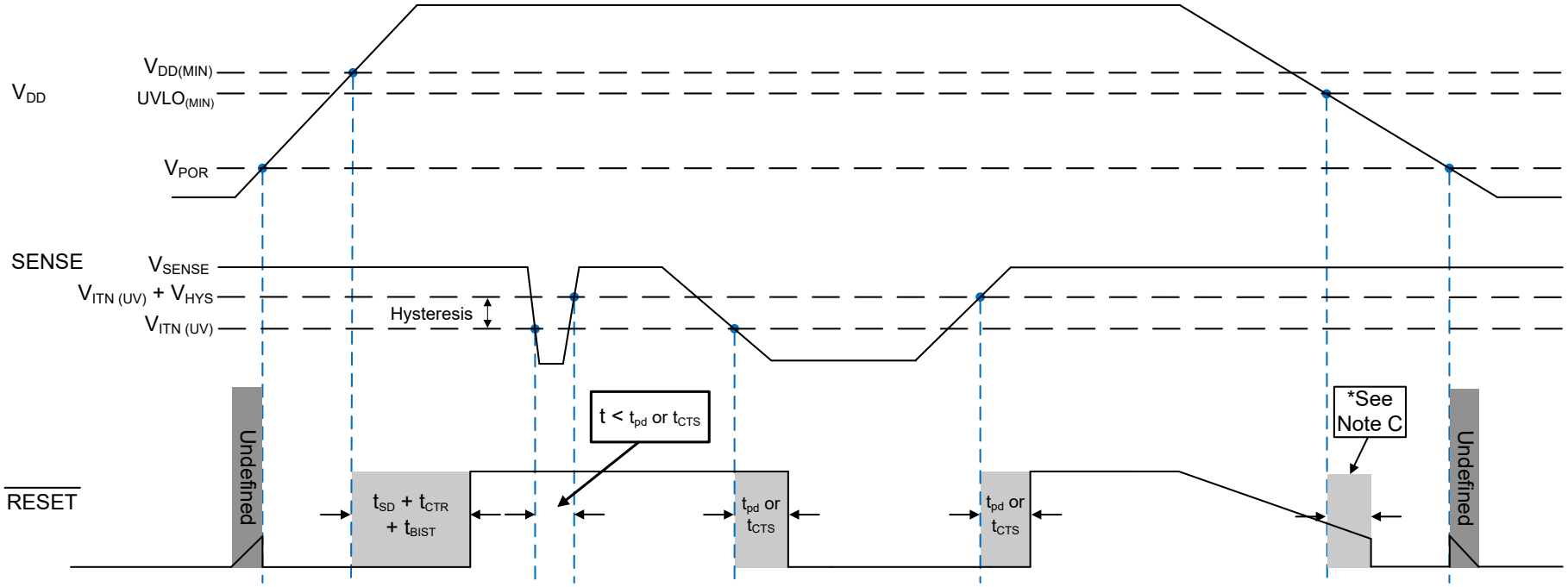
6.7 Timing Requirements

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, output $\overline{RESET}$ pullup resistor R_{PU} = 10 kΩ, voltage V_{PU} = 5.5 V, output $\overline{BIST}$ pullup resistor $R_{PU_\overline{BIST}}$ = 10 kΩ, voltage $V_{PU_\overline{BIST}}$ = 5.5 V, and load C_{LOAD} = 10 pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and V_{DD} = 12 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIST timing parameters						
$t_{BIST_en\ Glitch}$	BIST_EN Glitch immunity			1.1		µs
t_{BIST_en}	Minimum BIST_EN input width to initiate BIST			1.2	8	µs
LATCH timing parameters						
$t_{BIST_EN/LATCH_CLR\ Glitch}$	Latch Glitch immunity			1.5		µs
$t_{BIST_EN/LATCH_CLR}$	Latch input width to clear latch			1.6		µs

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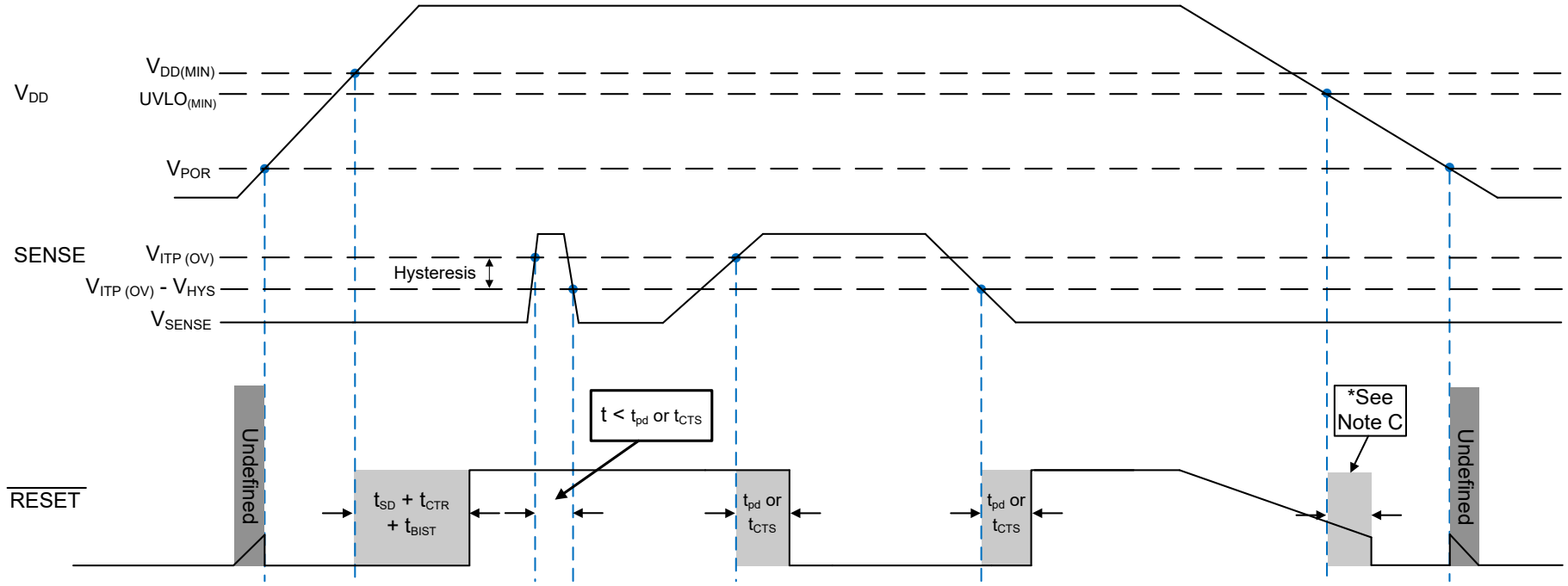
6.8 Timing Diagrams



A. The timing diagram assumes the open-drain output $\overline{\text{RESET}}$ pin is connected via an external pull-up resistor to V_{DD}.
B. Be advised that Figure 6-1 shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay or t_{CTR} time.
C. $\overline{\text{RESET}}$ is asserted when V_{DD} goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{pd} or t_{CTR}, is reached.

Figure 6-1. SENSE Undervoltage (UV) Timing Diagram

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A. The timing diagram assumes the open-drain output $\overline{\text{RESET}}$ pin is connected via an external pull-up resistor to V_{DD}.
B. Be advised that Figure 6-2 shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay or t_{CTR} time.
C. $\overline{\text{RESET}}$ is asserted when V_{DD} goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{pd} or t_{CTR}, is reached.

Figure 6-2. SENSE Overvoltage (OV) Timing Diagram

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6.9 Typical Characteristics

Typical characteristics show the typical performance of the TPS3762-Q1 device. Test conditions are taken at T_A = 25°C, unless otherwise noted.

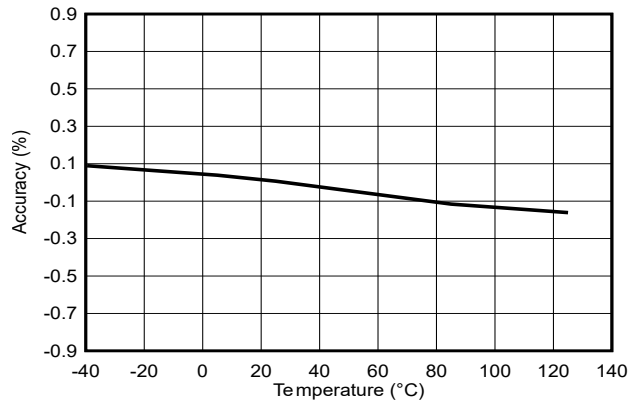


Figure 6-3. Undervoltage Accuracy vs Temperature (V_{IT} = 0.8V)

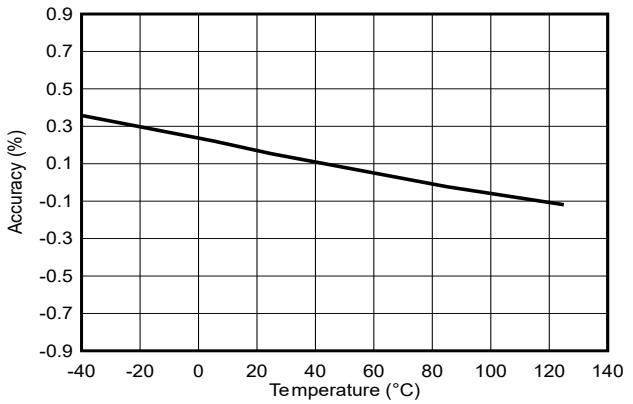


Figure 6-4. Overvoltage Accuracy vs Temperature (V_{IT} = 0.8V)

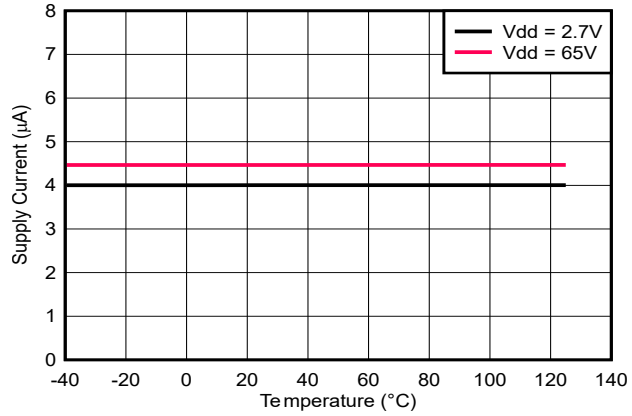


Figure 6-5. I_{DD} vs Temperature ($\overline{RESET}$ = High, V_{IT} = 0.8V)

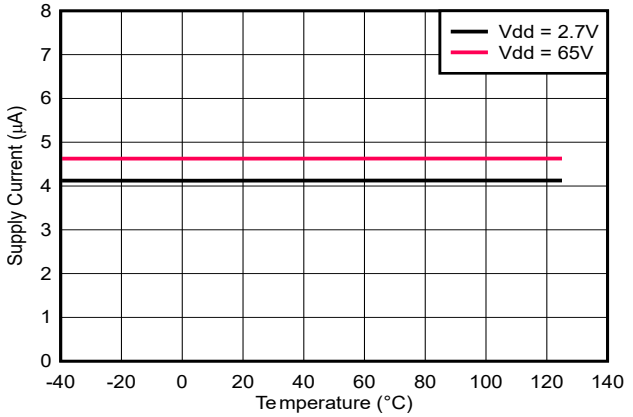


Figure 6-6. I_{DD} vs V_{DD} ($\overline{RESET}$ = Low, V_{IT} = 0.8V)

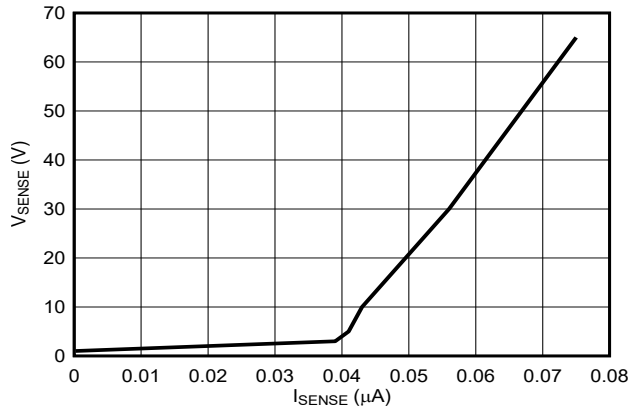


Figure 6-7. V_{SENSE} vs I_{SENSE} (V_{DD} = 2.7V)

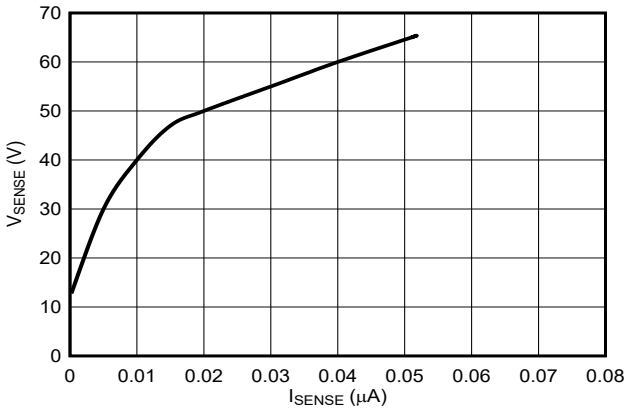


Figure 6-8. V_{SENSE} vs I_{SENSE} (V_{DD} = 65V)

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6.9 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3762-Q1 device. Test conditions are taken at T_A = 25°C, unless otherwise noted.

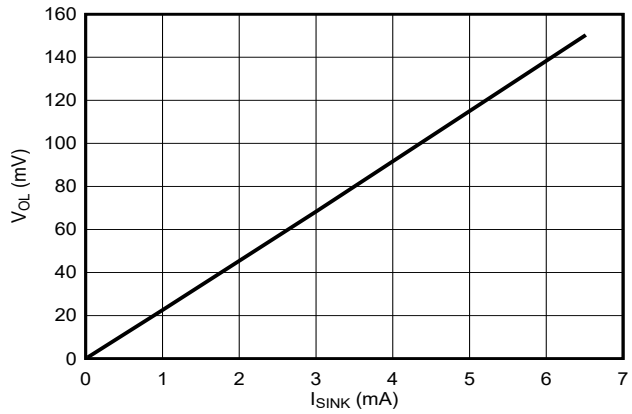


Figure 6-9. Open-Drain Active Low V_{OL} vs $I_{\overline{RESET}}$ (V_{DD} = 2.7V)

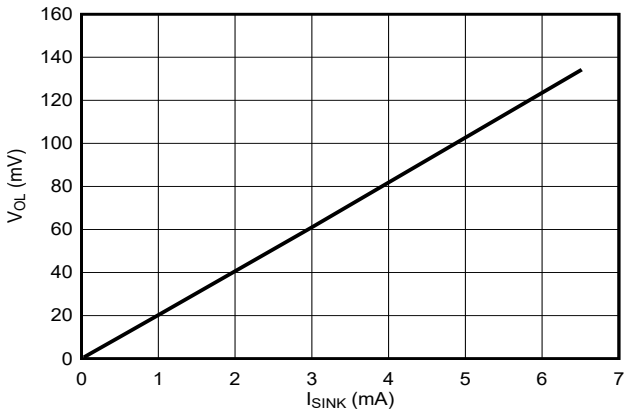


Figure 6-10. Open-Drain Active Low V_{OL} vs $I_{\overline{RESET}}$ (V_{DD} = 65V)

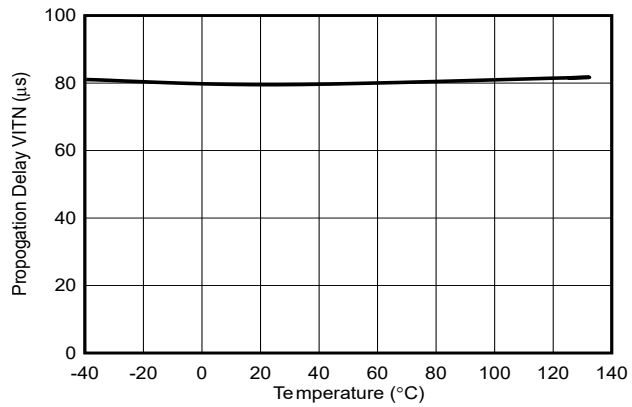


Figure 6-11. Propagation Delay (Undervoltage) vs Temperature (V_{IT} = 0.8V, CTS = Enabled = 50pF)

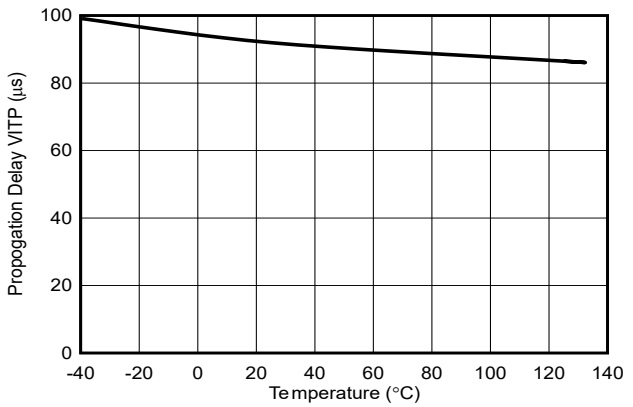


Figure 6-12. Propagation Delay (Overvoltage) vs Temperature (V_{IT} = 0.8V, CTS = Enabled = 50pF)

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7 Detailed Description

7.1 Overview

The TPS3762-Q1 is a family of high voltage and low quiescent current voltage supervisors with overvoltage and undervoltage threshold voltage options, delay timings, Built-In Self-Test, and latch. The TPS3762-Q1 over and undervoltage thresholds are device specific and are offered in either adjustable thresholds or fixed thresholds. The adjustable threshold option uses an external resistor ladder to make a voltage divider on SENSE pin which uses the internal 800mV threshold to trigger overvoltage and undervoltage faults. The benefit of using an adjustable option with external resistors is the faster reaction speed compared to a fixed internal threshold variant. The TPS3762-Q1 fixed threshold option utilizes an integrated voltage divider to eliminate the need for external resistors and provides a lower system leakage current.

VDD, SENSE and $\overline{\text{RESET}}$ pins can support 65V continuous operation. SENSE has -65V reverse polarity protection. VDD, SENSE, and $\overline{\text{RESET}}$ voltage levels can be independent of each other. TPS3762-Q1 includes a reset output latching feature that holds the output active to help system achieve safe state. Fixed and programmable sense and reset delay are available to avoid false resets and false reset releases.

7.2 Functional Block Diagram

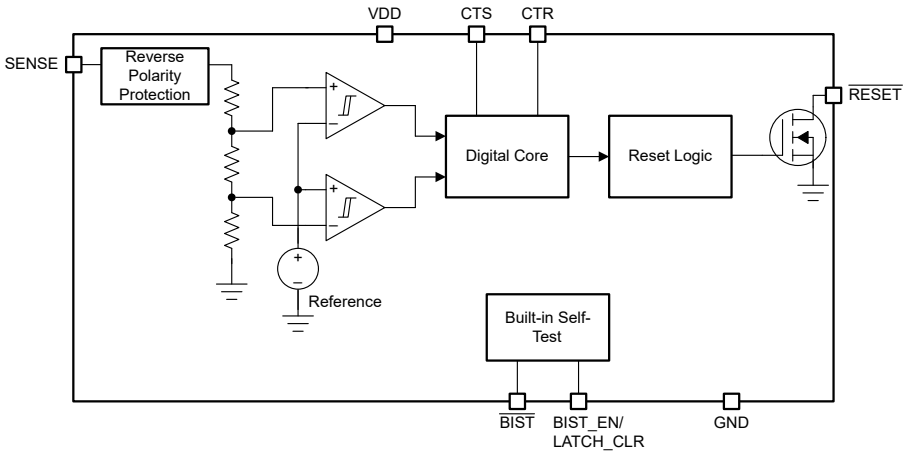


Figure 7-1. Fixed Threshold Functional Block Diagram

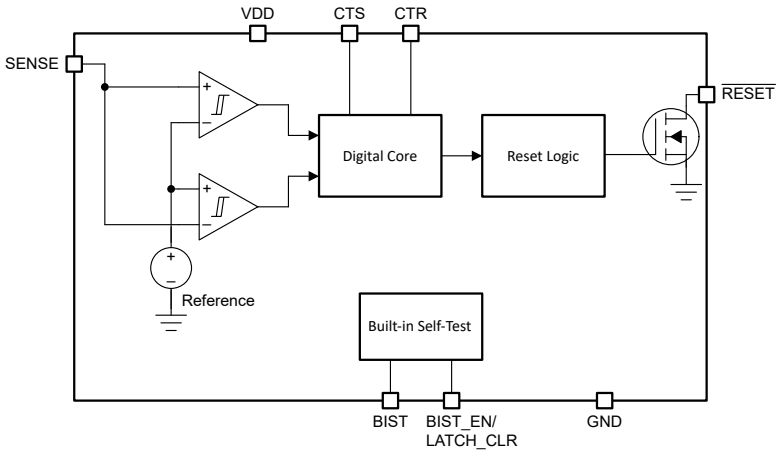


Figure 7-2. Adjustable Threshold Functional Block Diagram

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7.3 Feature Description

7.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7V to 65V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1µF capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET}, meaning that VDD can be higher or lower than the other pins.

7.3.1.1 Undervoltage Lockout (V_{POR} < V_{DD} < UVLO)

When the voltage on V_{DD} is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the $\overline{\text{RESET}}$ and $\overline{\text{BIST}}$ pins is asserted, regardless of the voltage at SENSE pin.

7.3.1.2 Power-On Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

Note: Figure 7-3 and Figure 7-4 assume an external pull-up resistor is connecting the $\overline{\text{RESET}}$ pin to VDD.

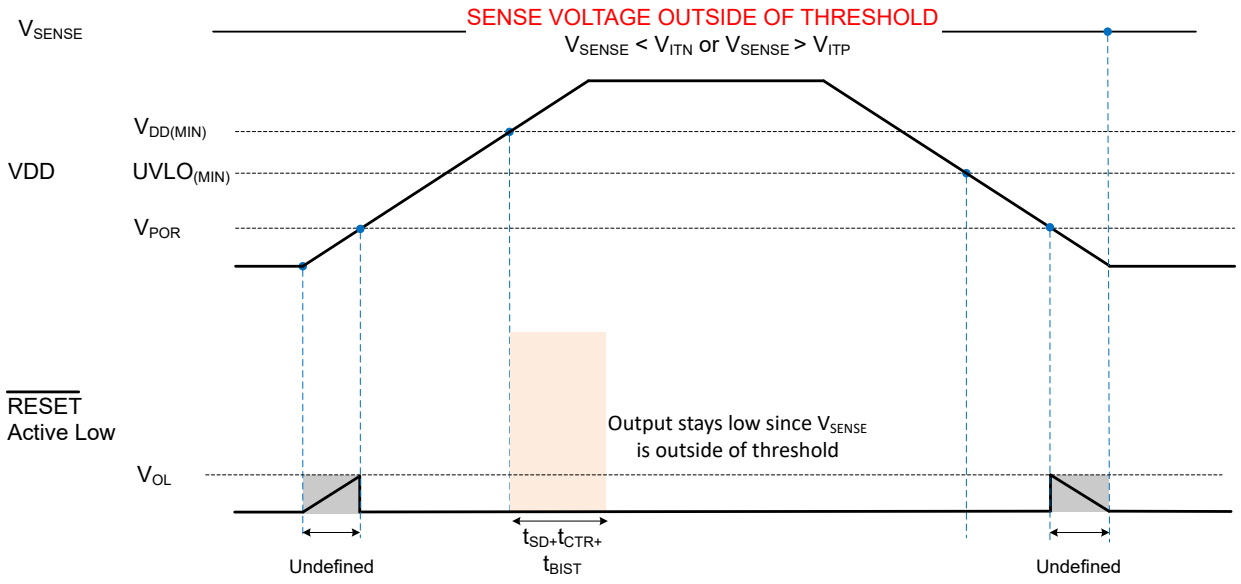


Figure 7-3. Power Cycle (SENSE Outside of Nominal Voltage)

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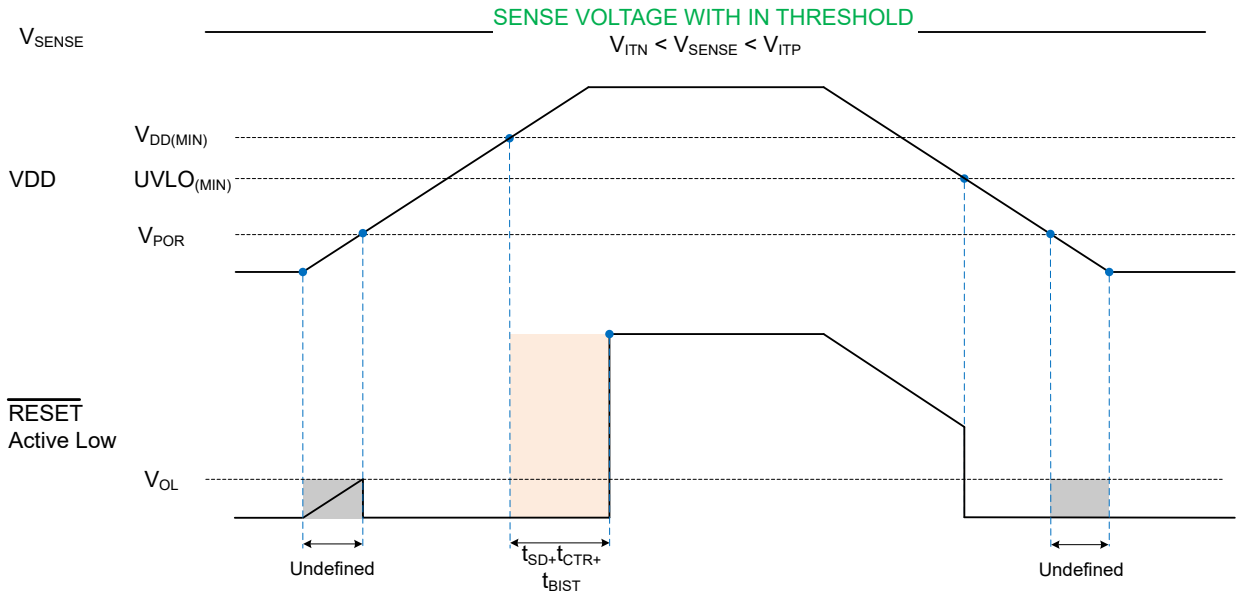


Figure 7-4. Power Cycle (SENSE Within Nominal Voltage)

7.3.2 SENSE

The SENSE pin connects to the supply rail that is to be monitored. The sense pin on each device is configured to monitor either overvoltage (OV), undervoltage (UV), or window (OV&UV) conditions. TPS3762-Q1 device offers built-in hysteresis that provides noise immunity and maintains stable operation.

Although not required in most cases, for noisy applications where t_{CTS} is not sufficient glitch rejection, good analog design practice is to place a 10nF to 100nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal. SENSE can be connected directly to VDD pin.

7.3.2.1 Reverse Polarity Protection

The TPS3762-Q1 has reverse polarity protection on the sense pin up to -65V. This allows the TPS3762-Q1 to support accidental or test simulated reverse connections without damaging the device. This protection permits the TPS3762-Q1 to connect directly off of the supply prior to any reverse polarity protection diodes for accurate voltage measurement.

7.3.2.2 SENSE Hysteresis

TPS3762-Q1 device offers built-in hysteresis around the UV and OV thresholds to avoid erroneous $\overline{\text{RESET}}$ deassertions. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

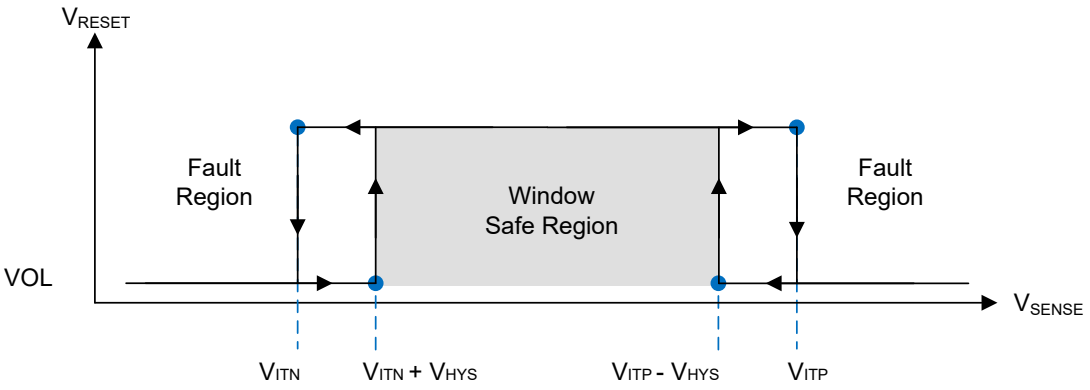


Figure 7-5. Hysteresis (Undervoltage & Overvoltage Active-Low)

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Table 7-1. Common Adjustable Hysteresis Lookup Table

TARGET			DEVICE HYSTERESIS OPTION
ADJUSTABLE THRESHOLD	TOPOLOGY	RELEASE VOLTAGE (V)	
800mV	Overvoltage	784mV	-2%
800mV	Overvoltage	760mV	-5%
800mV	Overvoltage	720mV	-10%
800mV	Undervoltage	816mV	2%
800mV	Undervoltage	840mV	5%
800mV	Undervoltage	880mV	10%

Table 7-1 shows a sample of hysteresis for the 800mV adjustable variant of TPS3762-Q1.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is (V_{ITN} + V_{HYS}) and for the overvoltage (OV) channel is (V_{ITP} - V_{HYS}).

Undervoltage (UV)

V_{ITN} = 800mV

Voltage Hysteresis (V_{HYS}) = 2% = 16mV

Hysteresis Accuracy = +1.5% to +2.5% = 16.24mV to 16.4mV

Release Voltage = V_{ITN} + V_{HYS} = 816.24mV to 816.4mV

Overvoltage (OV)

V_{ITP} = 800mV

Voltage Hysteresis (V_{HYS}) = 2% = 16mV

Hysteresis Accuracy = +1.5% to +2.5% = 16.24mV to 16.4mV

Release Voltage = V_{ITP} - V_{HYS} = 783.6mV to 783.76mV

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7.3.3 Output Logic Configurations

TPS3762-Q1 is a single channel device that has a single input SENSE pin and a single $\overline{\text{RESET}}$ pin. The single $\overline{\text{RESET}}$ is available only with open drain topology.

7.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pullup resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pullup resistor consider system V_{OH} and the Open-Drain Leakage Current (I_{lkg}) provided in the electrical characteristics, high resistors values have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS3762-Q1 open-drain output pin.

7.3.3.2 Active-Low ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ (active low) denoted with a bar above the pin label. $\overline{\text{RESET}}$ remains high voltage (V_{OH}, deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage the SENSE voltage needs to cross the upper boundary (V_{ITP}).

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7.3.3.3 Latch

The TPS3762-Q1 comes with the optional output reset latching feature, check the Section 4 to verify variant specific latch functionality. Pin 6 features an internal 100kΩ pulldown resistor which enables latch a startup. When using a variant with latch enabled ($V_{BIST_EN/LATCH_CLR}$ <0.5V), whenever a fault, OV or UV, occurs $\overline{RESET}$ asserts and goes low and remains low until cleared by a logic high input ($V_{BIST_EN/LATCH_CLR}$ > 1.3V) on the BIST_EN / LATCH_CLR pin. If the SENSE pin is in a safe region and latch is disabled, the $\overline{RESET}$ deasserts after a delay. This delay is dependent on BIST and CTR timing. See Section 7.3.6 for more details. While $V_{BIST_EN/LATCH_CLR}$ > 1.3V, the device is in latch disabled mode and the $\overline{RESET}$ does not latch for OV and UV on SENSE pin. While the device is in latch disabled mode the $\overline{RESET}$ asserts for OV and UV faults for the reset delay time. When $V_{BIST_EN/LATCH_CLR}$ < 0.5V, latch mode is enabled.

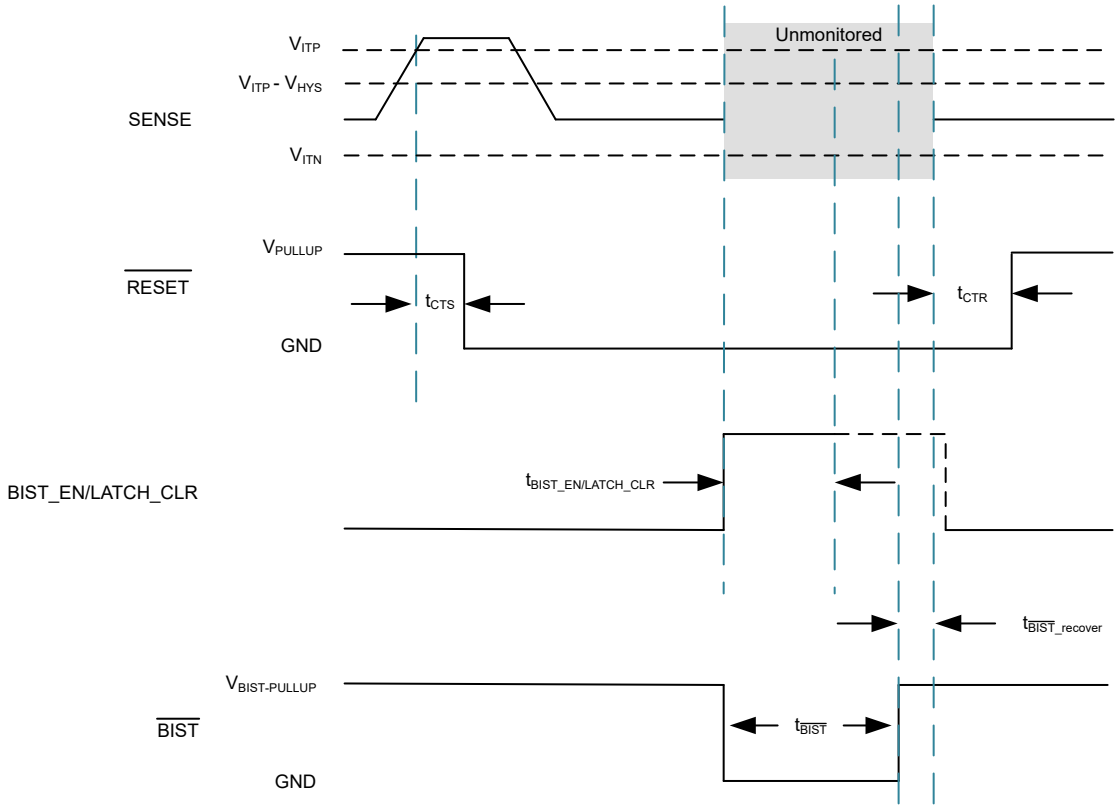


Figure 7-6. $\overline{RESET}$ Latch & Unlatch

7.3.3.4 UVBypass

The TPS3762-Q1 comes with the optional undervoltage bypass (UVbypass) feature, check Section 4 to verify variant specific UVbypass functionality. When using a variant with UVbypass enabled, the first undervoltage event after V_{DD} > V_{POR} is ignored. In cases where an undervoltage event has not occurred UVbypass can be cleared by running BIST.

UVbypass is targeted at specific applications in which the TPS3762-Q1 is powered Off-battery and is monitoring the Off-battery DC-DC output, as shown in Figure 7-7. If the Off-battery DCDC output is outside of threshold the TPS3762-Q1 resets this device. See Figure 7-8 and Figure 7-9 for more details.

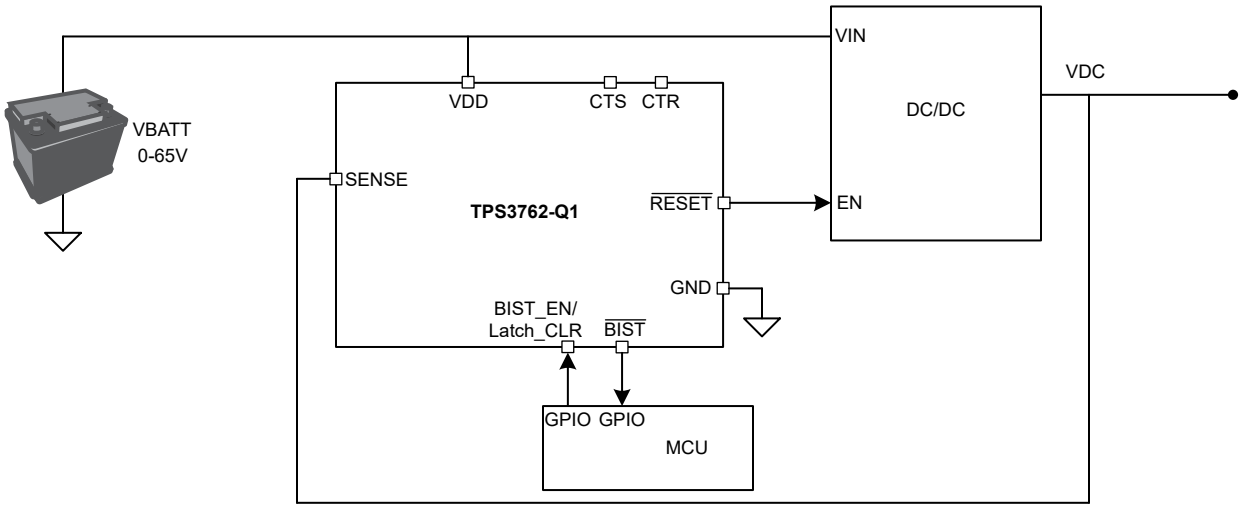


Figure 7-7. UVbypass Schematic

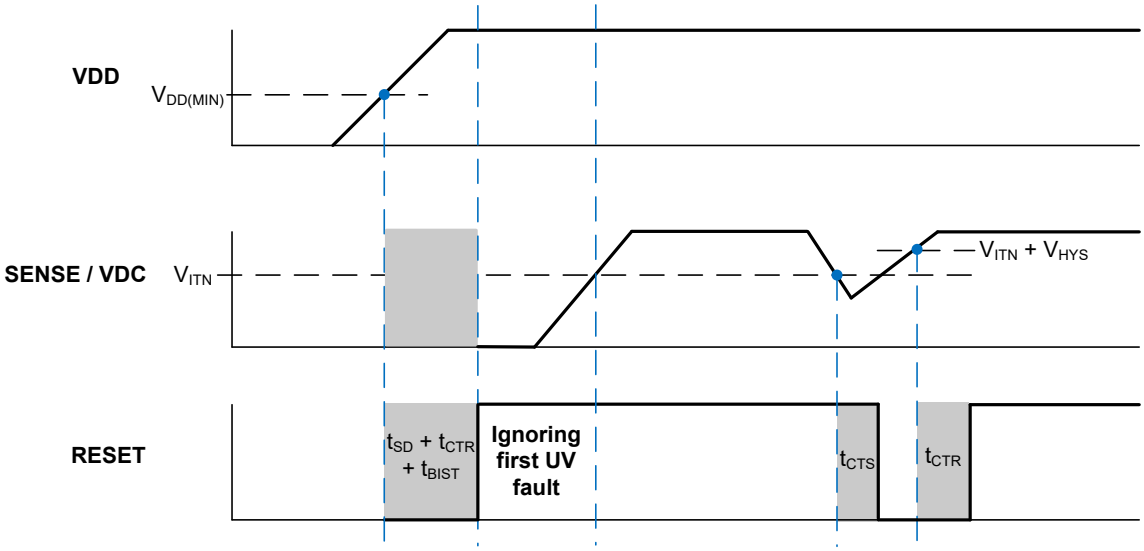


Figure 7-8. UVbypass Enabled

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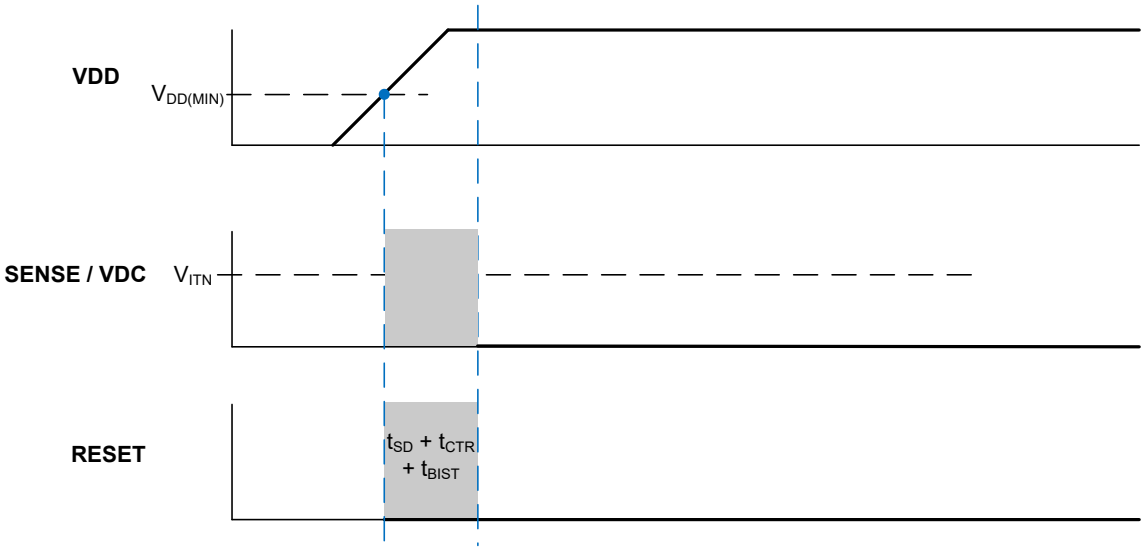


Figure 7-9. UVbypass Disabled

7.3.4 User-Programmable Reset Time Delay

TPS3762-Q1 has adjustable reset release time delay with external capacitors.

- A capacitor on CTR programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time indicated by t_{CTR} in Section 6.6.
- Variants such as TPS3762Q use a fixed internal time delay. check the Section 4 to verify variant specific timing.

7.3.4.1 Reset Time Delay Configuration

RESET time delay (t_{CTR}) occurs when the $\overline{\text{RESET}}$ is transitioning from a fault state (V_{OL}) to a non-fault state (V_{OH}). The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND. For situations with a fault on SENSE after $\overline{\text{RESET}}$ recovers, the TPS3762-Q1 makes sure that the CTR capacitor is fully discharged before starting the recovery sequence. This makes sure that the programmed CTR time is maintained for consecutive faults.

The relationship between external capacitor $C_{CTR_EXT\ (typ)}$ in µF and the time delay $t_{CTR\ (typ)}$ in seconds is given by Equation 1.

$$t_{CTR\ (typ)} = 3.7 \times C_{CTR_EXT\ (typ)} + 0.00035 \quad (1)$$

$C_{CTR_EXT\ (typ)}$ is given in microfarads (µF)

$t_{CTR\ (typ)}$ is given in seconds (s)

The reset delay varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in Section 6.5, and the constant ($t_{CTR\ (no\ cap)}$) provided in Section 6.6. The minimum and maximum variance due to the constant is show in Equation 2 and Equation 3:

$$t_{CTR\ (min)} = 2.96 \times C_{CTR_EXT\ (min)} \quad (2)$$

$$t_{CTR\ (max)} = 4.44 \times C_{CTR_EXT\ (max)} + 0.00067 \quad (3)$$

There is no limit to the capacitor on CTR pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold $\overline{\text{RESET}}$ active.

* Leakages on the capacitor can effect accuracy of reset time delay.

Table 7-2. Reset Time Delay for Common Ideal Capacitor Values

C_{CTR_EXT}	RESET TIME DELAY (t_{CTR})			UNIT
	MIN (1)	TYP	MAX (1)	
33nF	97.68	122.45	147.12	ms
100nF	296	370.35	444.6	ms
1µF	2960	3700.35	4440.6	ms

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7.3.5 User-Programmable Sense Delay

TPS3762-Q1 has adjustable sense release time delay with external capacitors.

- A capacitor on CTS programs the sense time delay of the input.
- No capacitor on this pin gives the fastest sense delay time indicated by t_{CTS} in Section 6.7.
- The TPS3762-Q1 comes with an optional fixed internal time delay that ignores the capacitor value at the CTS pin, check the Section 4 to verify variant specific functionality.

7.3.5.1 Sense Time Delay Configuration

SENSE time delay (t_{CTS}) occurs when the $\overline{RESET}$ is transitioning from a non-fault state (V_{OH}) to a fault state (V_{OL}). The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS_EXT\ (typ)}$ in µF and the time delay $t_{CTS\ (typ)}$ in seconds is given by Equation 4.

$$t_{CTS\ (typ)} = 3.7 \times C_{CTS_EXT\ (typ)} + 0.000085 \quad (4)$$

$C_{CTS_EXT\ (typ)}$ = is given in microfarads (µF)

$t_{CTS\ (typ)}$ = is given in seconds (s)

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTS}) provided in Section 6.5, and the constant ($t_{CTS\ (no\ cap)}$) provided in Section 6.6. The minimum and maximum variance due to the constant is show in Equation 5 and Equation 6:

$$t_{CTS\ (min)} = 2.96 \times C_{CTS_EXT\ (min)} \quad (5)$$

$$t_{CTR\ (max)} = 4.44 \times C_{CTS_EXT\ (max)} + 0.0001 \quad (6)$$

The recommended maximum sense delay capacitor for the TPS3762-Q1 is 10µF as this makes sure there is enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip unpredictably. This leads to a variation in time delay where the delay accuracy can be worse in the presence of system noise.

* Leakages on the capacitor can effect accuracy of sense time delay.

Table 7-3. Reset Sense Delay for Common Ideal Capacitor Values

C_{CTS_EXT}	SENSE TIME DELAY (t_{CTS})			UNIT
	MIN (1)	TYP	MAX (1)	
33nF	97.68	122.185	146.62	ms
100nF	296	370.085	444.1	ms
1µF	2960	3700.085	4440.1	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

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7.3.6 Built-In Self-Test

The TPS3762-Q1 has a Built-In Self-Test (BIST) feature that runs diagnostics internally in the device. During power-up BIST is initiated automatically after crossing $V_{DD(min)}$. If BIST RESET trigger is enabled in the selected device orderable, during BIST the $\overline{BIST}$ pin and $\overline{RESET}$ output asserts low and only deasserts if the $\overline{BIST}$ test completes successfully indicating no internal faults in the device. If BIST RESET trigger is disabled only the $\overline{BIST}$ pin asserts low and deasserts if the $\overline{BIST}$ test completes successfully indicating no internal faults in the device. The length of the BIST and $\overline{BIST}$ assertion is specified by $t_{\overline{BIST}}$. If BIST is not successful, the $\overline{BIST}$ pin stays asserted low signifying an internal fault. For BIST RESET trigger enabled device orderables, the $\overline{RESET}$ output stays asserted on $\overline{BIST}$ failure. During BIST, the device is not monitoring the SENSE pin for faults and the $\overline{RESET}$ is not dependent on the SENSE pin voltage. The $\overline{BIST}$ sequence of internal tests verifies the internal signal chain of the device by checking for faults on the internal comparators on the SENSE pin, bandgap voltage, and the $\overline{RESET}$ output. See Figure 7-10 for more details.

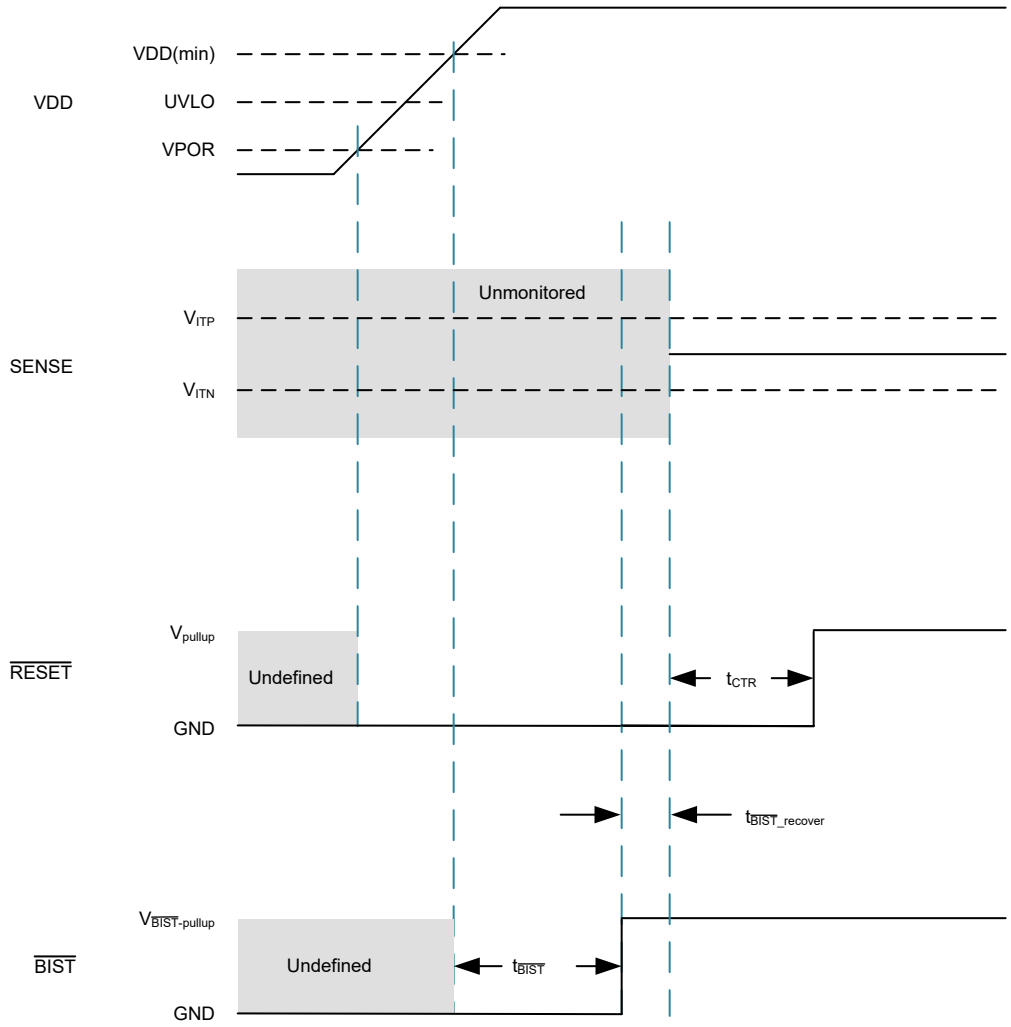


Figure 7-10. TPS3762-Q1 Start-Up Sequence

After a successful power-up sequence, BIST can be initiated any time with a logic high input (V_{BIST_EN} or $V_{BIST_EN/LATCH_CLR}$ > 1.3V) on the BIST_EN / LATCH_CLR pin. BIST initiates and the $\overline{BIST}$ pin asserts only if the SENSE pin is not in a overvoltage or undervoltage fault mode. During this BIST test time period, $t_{\overline{BIST}}$, $\overline{BIST}$ pin asserts low to signify that $\overline{BIST}$ has started and $\overline{RESET}$ assertion is dependent on the device variant. Upon a successful BIST the $\overline{BIST}$ pin and $\overline{RESET}$ pin are deasserted. If BIST is not successful due to an internal device not working properly, the $\overline{RESET}$ pin and $\overline{BIST}$ pin remain asserted low signifying a fault internal to the device. See Figure 7-11 and Figure 7-12 for more details.

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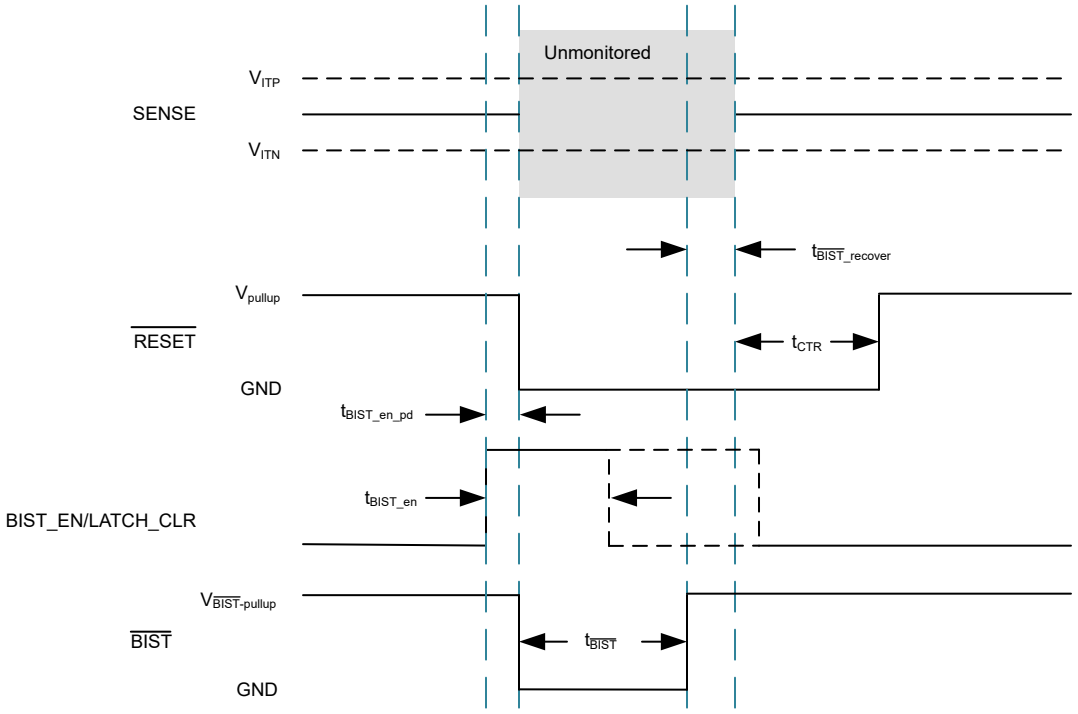


Figure 7-11. $\overline{BIST}$ With $\overline{RESET}$ Assertion

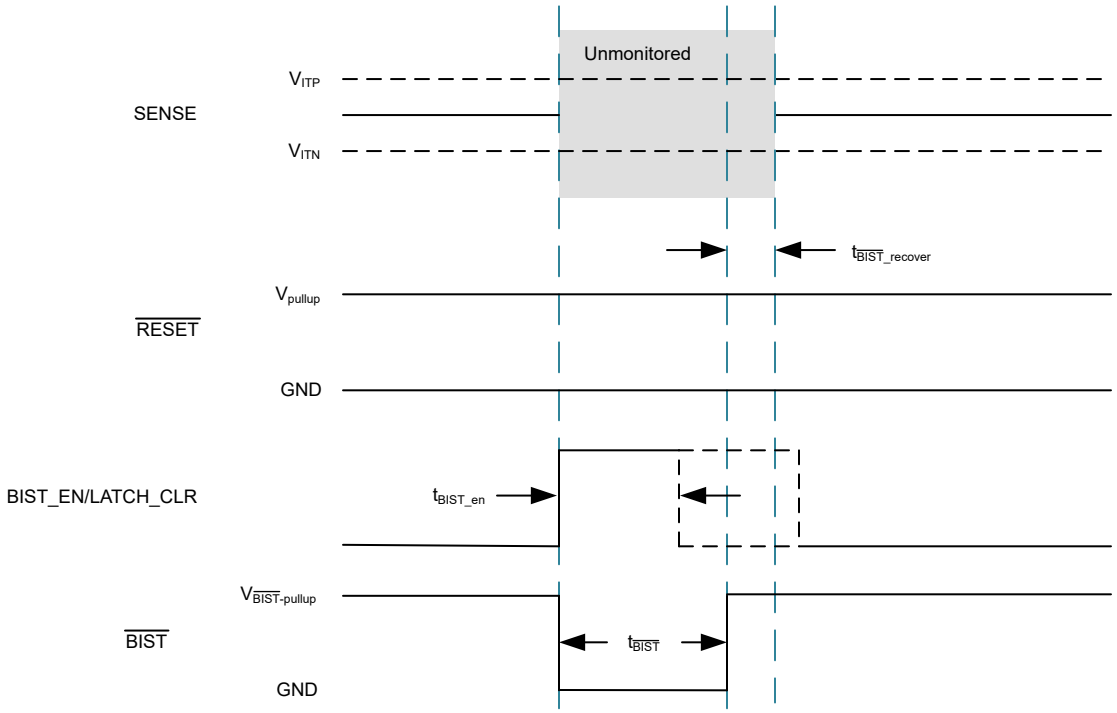


Figure 7-12. $\overline{BIST}$ With No $\overline{RESET}$ Assertion

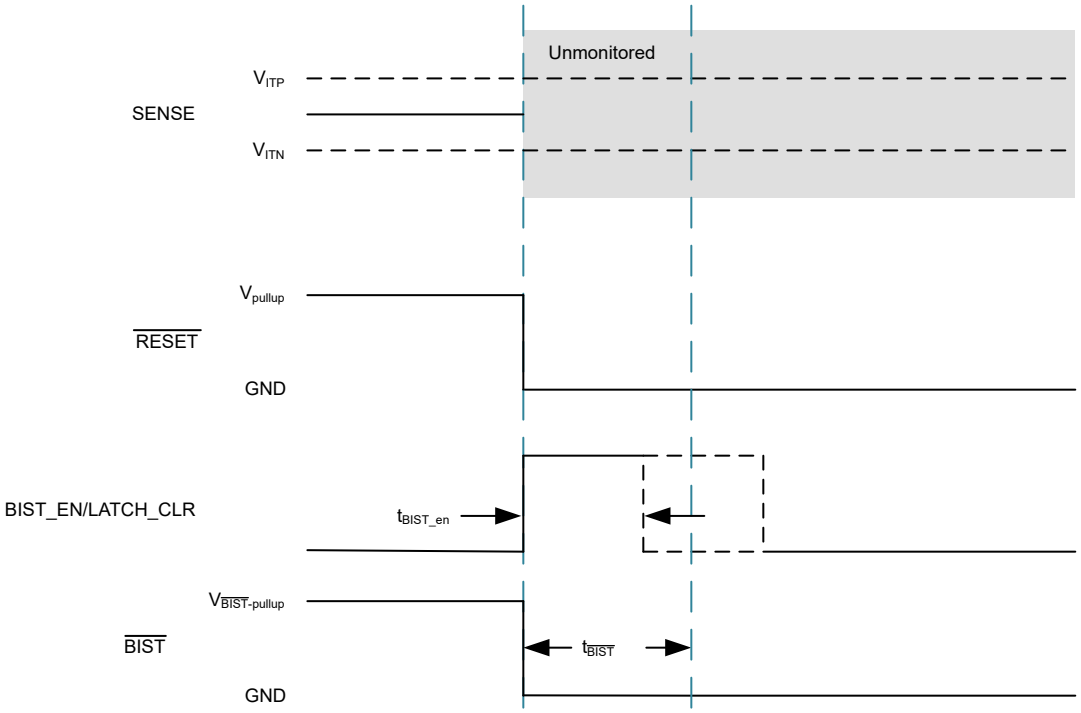


Figure 7-13. $\overline{\text{BIST}}$ Fail With $\overline{\text{RESET}}$ Assertion

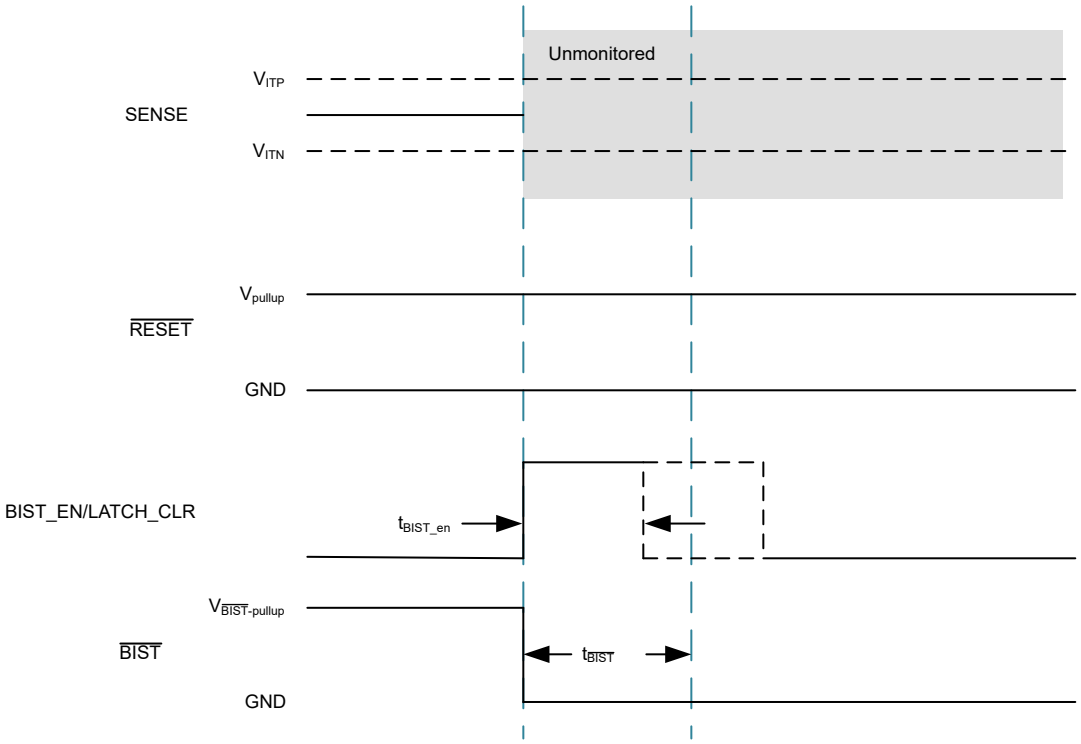


Figure 7-14. $\overline{\text{BIST}}$ Fail With No $\overline{\text{RESET}}$ Assertion

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7.4 Device Functional Modes

Table 7-4. Undervoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR (1)	V_{DD} PIN	OUTPUT (2) ($\overline{RESET}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE > V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Undervoltage Detection	SENSE > V_{ITN}	SENSE < V_{ITN}	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Undervoltage Detection	SENSE < V_{ITN}	V_{ITN} < SENSE < V_{ITN} + HYS	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Normal Operation	SENSE < V_{ITN}	SENSE > V_{ITN} + HYS	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
UVLO Engaged	SENSE > V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	V_{POR} < V_{DD} < $V_{DD(MIN)}$	Low
Below V_{POR}, Undefined Output	SENSE > V_{ITN}	SENSE > V_{ITN}	Open or capacitor connected	V_{DD} < V_{POR}	Undefined

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pullup resistor to a pull-up voltage.

Table 7-5. Overvoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR (1)	V_{DD} PIN	OUTPUT (2) ($\overline{RESET}$ PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	SENSE < V_{ITP}	SENSE < V_{ITP}	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
Overvoltage Detection	SENSE < V_{ITP}	SENSE > V_{ITP}	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Overvoltage Detection	SENSE > V_{ITP}	V_{ITP} - HYS < SENSE < V_{ITP}	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	Low
Normal Operation	SENSE > V_{ITP}	SENSE < V_{ITP} - HYS	Open or capacitor connected	V_{DD} > $V_{DD(MIN)}$	High
UVLO Engaged	SENSE < V_{ITP}	SENSE < V_{ITP}	Open or capacitor connected	V_{POR} < V_{DD} < UVLO	Low
Below V_{POR}, Undefined Output	SENSE < V_{ITP}	SENSE < V_{ITP}	Open or capacitor connected	V_{DD} < V_{POR}	Undefined

(1) Reset time delay is ignored in the truth table.
(2) Open-drain active low output requires an external pullup resistor to a pull-up voltage.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

8.2 Adjustable Voltage Thresholds

Figure 8-1 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the adjustable (0.8V voltage threshold device) when setting adjustable voltage thresholds. This variant bypasses the internal resistor ladder.

For example, consider a 12V rail, V_{MON}, being monitored for overvoltage (OV) using of the TPS3762D02OVDDFRQ1 variant, as shown in Figure 8-1. The monitored OV threshold, denoted as V_{MON+}, is the desired voltage where the device asserts the reset. For this example V_{MON+} = 35V. To assert an overvoltage reset the voltage at the sense pin, V_{SENSE}, needs to be equal to the input threshold positive, V_{ITP}. For this example variant V_{SENSE} = V_{ITP} = 0.8V. Using R_1 and R_2 the correlation between V_{MON+} and V_{SENSE} can be seen in Equation 8. Assuming R_2 = 10kΩ, and R_1 can be calculated as R_1 = 427.5kΩ.

$$V_{SENSE} = V_{MON+} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

The TPS3762D02OVDDFRQ1 comes with variant specific 2%, 5%, or 10% voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} must go below V_{ITP} - V_{HYS}. For this example variant a 2% voltage threshold hysteresis is selected. Therefore, V_{MON} equals 34.3V when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is the internal resistance of the SENSE pin that can affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance (R_{SENSE}) can be calculated by the SENSE voltage (V_{SENSE}) divided by the SENSE current (I_{SENSE}) as shown in Equation 9. V_{SENSE} can be calculated using Equation 7 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using Equation 8.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (8)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (9)$$

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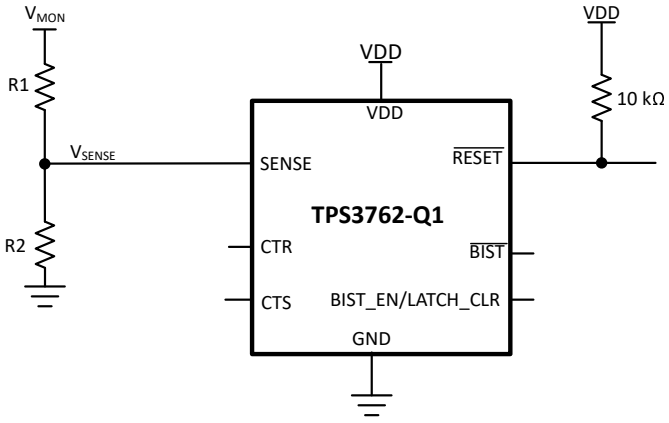


Figure 8-1. Adjustable Voltage Threshold With External Resistor Dividers

8.3 Typical Application

8.3.1 Design 1: Off-Battery Monitoring

This application is intended for the initial power stage in applications with the 12V batteries. The TPS3762-Q1 utilizes high-voltage SENSE and V_{DD} inputs to monitor an automotive battery.

Figure 8-6 illustrates an example of how the TPS3762-Q1 is monitoring the battery voltage while being powered by the battery, as well.

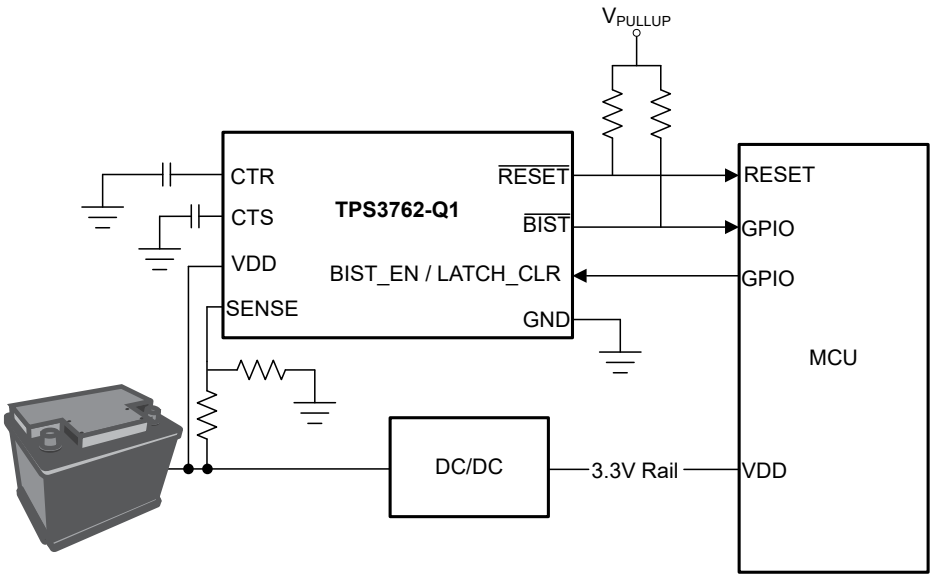


Figure 8-2. Off-Battery Monitoring

8.3.1.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Voltage Threshold	Typical OV voltage threshold 30V.
Maximum Input Power	Operate with power supply input up to 65V
Output Logic	Open-Drain
SENSE Delay	>100ms
$\overline{\text{RESET}}$ Delay	>300ms
Output Features	Output latching and built-in self-test

8.3.1.2 Detailed Design Procedure

The TPS3762-Q1 utilizes high-voltage SENSE and V_{DD} inputs to monitor an automotive battery. In this design example TPS3762D02OVDDFRQ1 is used.

8.3.1.2.1 Setting Voltage Threshold

The positive-going threshold voltage, V_{ITP}, is set by the device variant. In this example, the nominal supply voltage from the battery is 12V. Setting a overvoltage threshold of 30V makes sure that the device resets before supply voltage violates the allowed boundary. The adjustable voltage variant is chosen and R_1 and R_2 are adjusted to meet the threshold. Assuming R_2 equal to 10kΩ and R_1 is calculated as 365kΩ. For additional information on selecting resistor values see Section 8.2. TPS3762-Q1 also supports fixed voltage threshold variants. Threshold voltage decoding can be found in Device Decoder.

8.3.1.2.2 Meeting the Sense and Reset Delay

The TPS3762-Q1 features both reset assertion (sense) delay, t_{CTS}, and reset deassertion (reset) delay, t_{CTR}. The TPS3762-Q1 features two options for selecting sense and reset delays: fixed delays and capacitor-programmable delays. For the device variant used in this design, TPS3762D02OVDDFRQ1, the capacitor programmable delay is chosen. Section 7.3.5 and Section 7.3.4 show how to set the timings for the capacitor-programmable delays. The application requires greater than 100ms sense delay, thus a 0.033µF capacitor is used. The application requires greater than 300ms reset delay, thus a 0.1µF capacitor is used.

8.3.1.2.3 Setting Supply Voltage

Setting the supply voltage is done by connecting the V_{DD} input directly to the battery rail without the need for external circuitry. The device being able to handle 65V on V_{DD} means the monitored voltage rail can handle any voltage transience up to 65V. Good analog design practice recommends using a 0.1µF capacitor on the V_{DD} pin.

8.3.1.2.4 Initiating Built-In Self-Test and Clearing Latch

Built-In Self-Test (BIST) is asserted on device power-up, as outlined in Figure 7-10. BIST can also be initiated any time by a rising edge that crosses the voltage logic high input (V_{BIST_EN} or $V_{BIST_EN/LATCH_CLR}$ > 1.3V) on the BIST_EN / LATCH_CLR pin, as outlined in Figure 7-11. Output reset latching is set by the device variant. For the device variant used in this design, TPS3762D02OVDDFRQ1, the output has latch. Device specific output reset latching feature can be found in Device Decoder. To clear the latch a logic high input on the BIST_EN / LATCH_CLR pin is required. When clearing latch, BIST is initiated and the $\overline{\text{RESET}}$ returns logic level high once $t_{\overline{BIST}}$ + $t_{\overline{BIST}_recover}$ + t_{CTR} has expired, outlined in Figure 7-6. While $V_{BIST_EN/LATCH_CLR}$ > 1.3V, the device is in latch disabled mode and the $\overline{\text{RESET}}$ does not latch for OV and UV on SENSE pin. While the device is in latch disabled mode the $\overline{\text{RESET}}$ still asserts for OV and UV faults.

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8.3.1.3 Application Curves

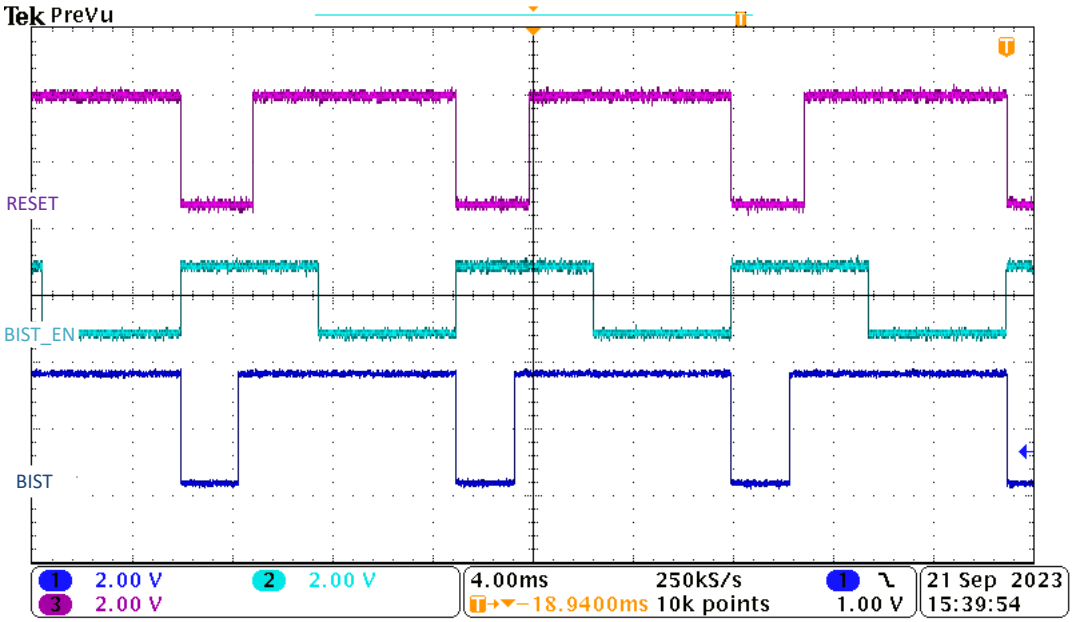


Figure 8-3. BIST With $\overline{\text{RESET}}$ Assertion Waveform

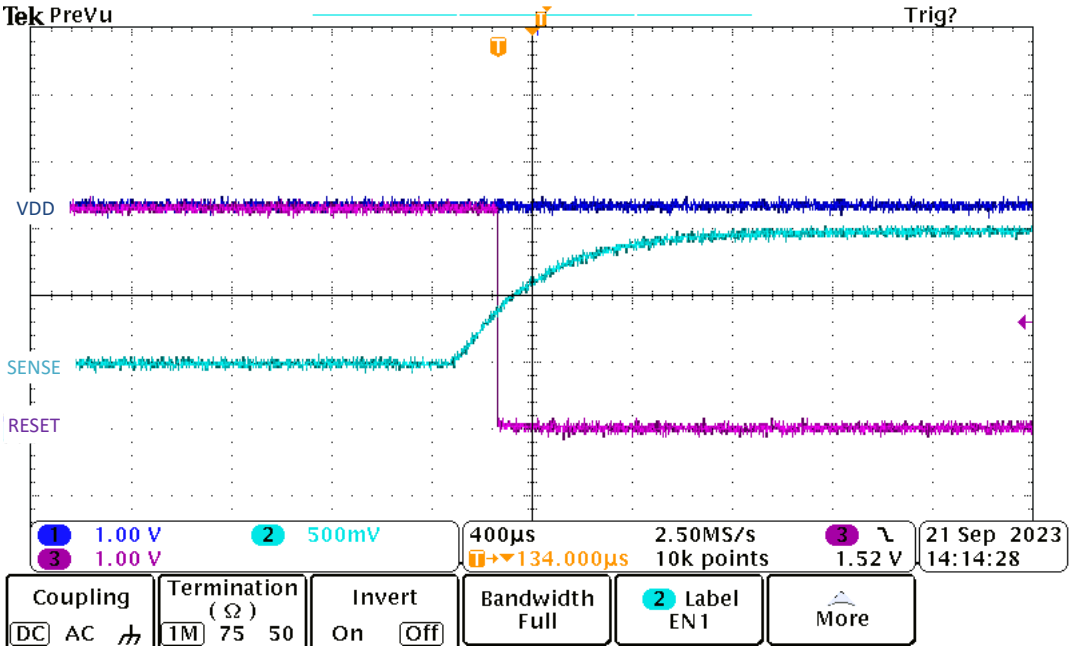


Figure 8-4. Overvoltage $\overline{\text{RESET}}$ Latching Waveform

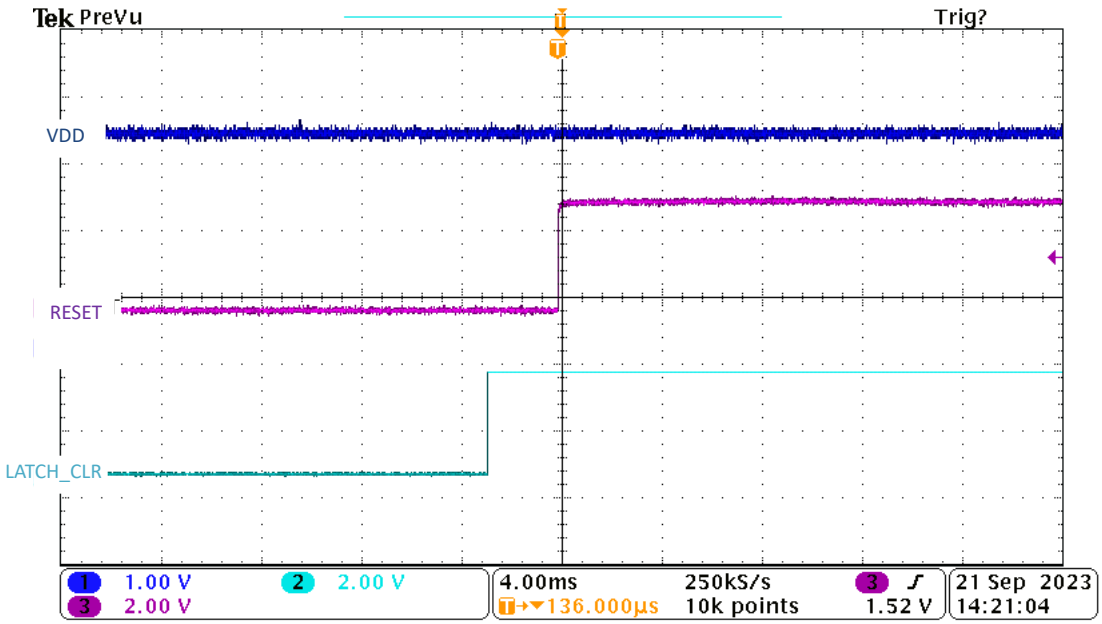


Figure 8-5. Overvoltage $\overline{\text{RESET}}$ Unlatching Waveform

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8.4 Power Supply Recommendations

TPS3762-Q1 is designed to operate from an input supply with a V_{DD} voltage between 2.7V (minimum operation) to 65V (maximum operation). Good analog design practice recommends placing a minimum 0.1µF ceramic capacitor as near as possible to the V_{DD} pin.

8.4.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using Equation 10:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} – T_A) / R_{\theta JA}) \quad (10)$$

The actual power being dissipated in the device can be represented by Equation 11:

$$P_D = V_{DD} \times I_{DD} + p_{RESET} \quad (11)$$

p_{RESET} is calculated by Equation 12 or Equation 13

$$p_{RESET\ (PUSHPULL)} = V_{DD} - V_{RESET} \times I_{RESET} \quad (12)$$

$$p_{RESET\ (OPEN\text{-}DRAIN)} = V_{RESET} \times I_{RESET} \quad (13)$$

Equation 10 and Equation 11 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations must be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be increased.

In applications where high power dissipation or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can require de-rating. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to-ambient thermal resistance of the part or package in the application ($R_{\theta JA}$), as given by Equation 14:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (14)$$

8.5 Layout

8.5.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1µF ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSE pins, placing a 10nF to 100nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces must be greater than 20mils (0.5mm).

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- Do not have high voltage metal pads or traces closer than 20 mils (0.5mm) to the low voltage metal pads or traces.

8.5.2 Layout Example

The layout example in Figure 8-6 shows how the TPS3762-Q1-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.

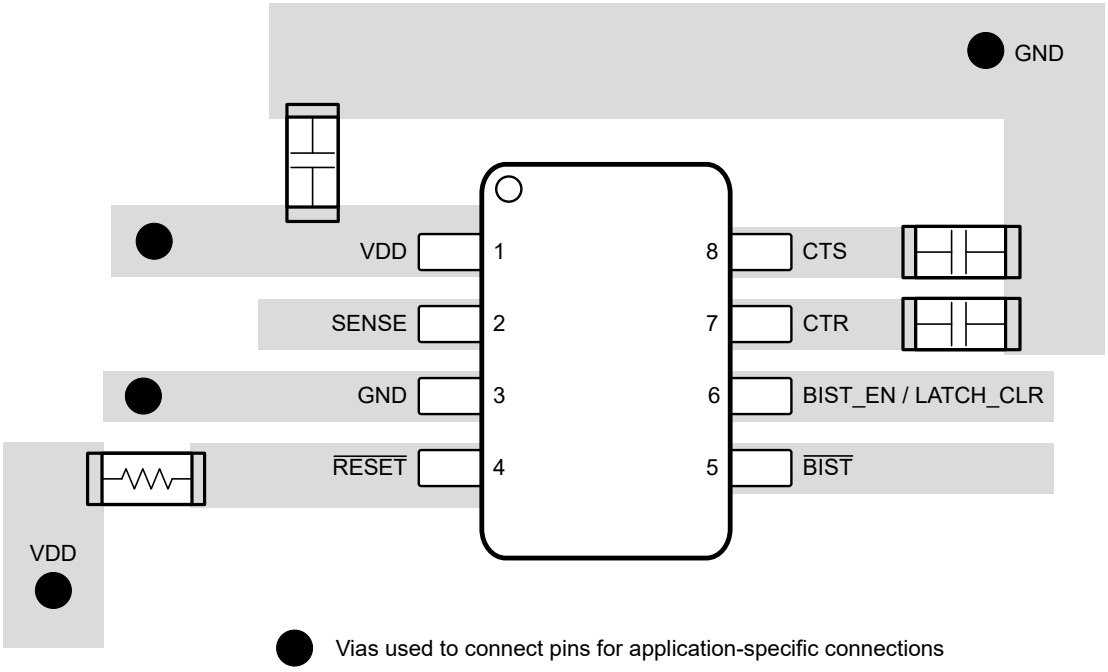


Figure 8-6. TPS3762-Q1-Q1 Recommended Layout

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9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The following related documents are available for download at www.ti.com:

- *Optimizing Resistor Dividers at a Comparator Input*, SLVA450
- *Sensitivity Analysis for Power Supply Design*, SLVA481
- *Getting Started With TMS320C28x Digital Signal Controllers*, SPRAAM0
- TPS3762-Q1B-Q1EVM-775 Evaluation Module User Guide, SBVU030
- C2000 Delfino Family of Microprocessors
- TMS320F2833x microcontroller, SPRS439

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2024) to Revision B (February 2026)	Page
• Changed Features for better clarity	1
• Changed 5µs to 3µs	1
• Updated Description wording for clarity	1
• Added Package Size to Package Information	1
• Moved Device Nomenclature as a subsection of Device Comparison	3
• Added additional devices to Device Nomenclature	3
• Added additional device decoder	3
• Updated pin description for BIST_EN / LATCH_CLR	6
• Updated Absolute Maximum Ratings, Recommended Operating Conditions, Electrical Characteristics, Timing Requirements, and Switching Characteristics with additional specifications for fixed voltage threshold variants	7

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- Updated table note 1 in Absolute Maximum Ratings to the latest standard....7
- Updated test condition wording for clarity in Electrical Characteristics and Switching Requirements....7
- Changed "TCTS" to "Tpd or TCTS"....13
- Removed Reverse Polarity Protection from Adjustable Threshold Functional Block Diagram....17
- Updated wording in Latch section for clarity....23
- Changed title from Latching to Latch....23
- Updated CTR equations for clarity....26
- Added example Reset Time Delay capacitor values....26
- Updated CTS equations for clarity....27
- Added example Sense Time Delay capacitor values....27
- Updated Built-In Self-Test for clarity....28

Changes from Revision * (October 2023) to Revision A (May 2024)	Page
• Production Data release	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3762BM6OVDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62BM6
TPS3762BUV05DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62BUV
TPS3762D02OVDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62D02
TPS3762D02OVDDFRQ1.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62D02
TPS3762D02OVDDFRQ1.B	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS3762DW4W4DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62DW4
TPS3762EG4OVDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62EG4
TPS3762EUV02DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62EU2
TPS3762EUVF4DDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62EF4
TPS3762F02OVDDFRQ1	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	62F02

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS3762-Q1 :

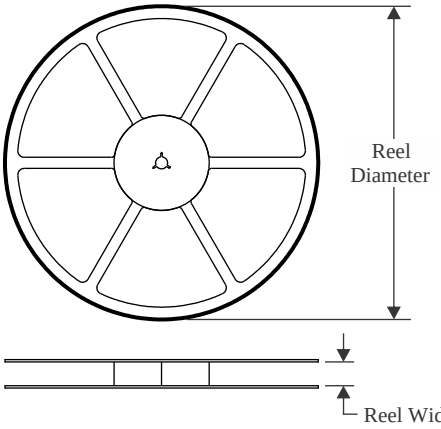
- Catalog : TPS3762

NOTE: Qualified Version Definitions:

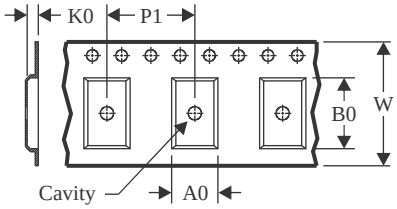
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

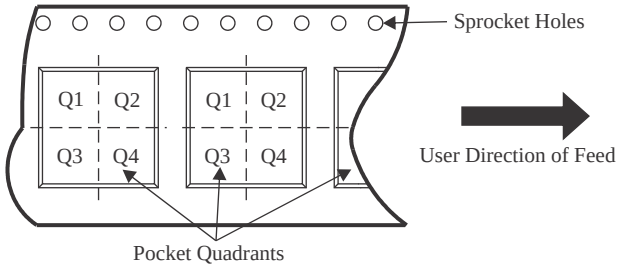


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

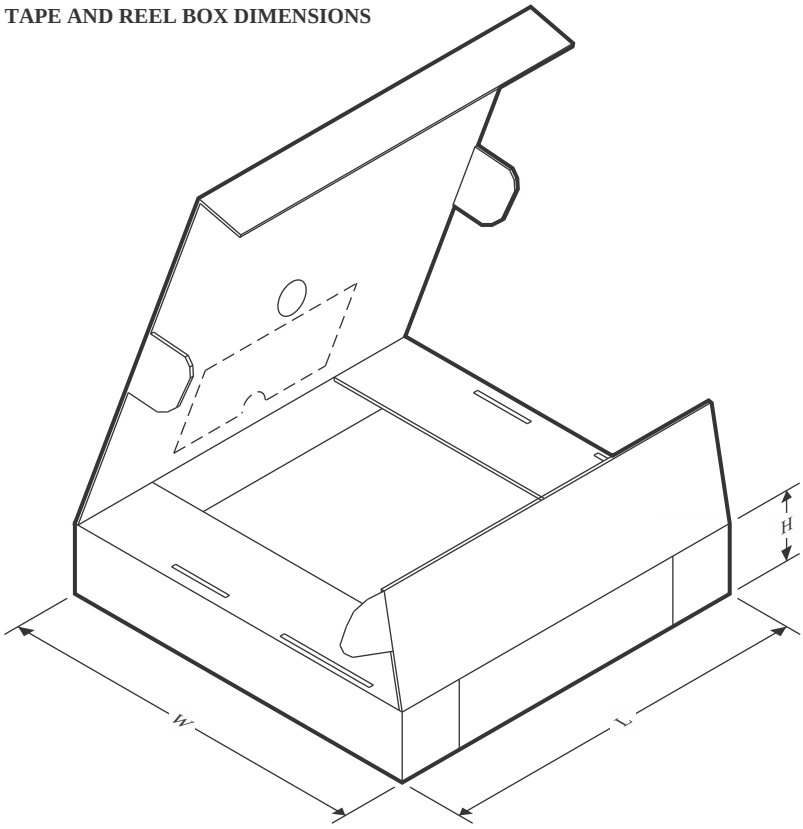
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3762BM6OVDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3762BUV05DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3762D02OVDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3762DW4W4DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3762EG4OVDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3762EUV02DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3762EUVF4DDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3762F02OVDDFRQ1	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

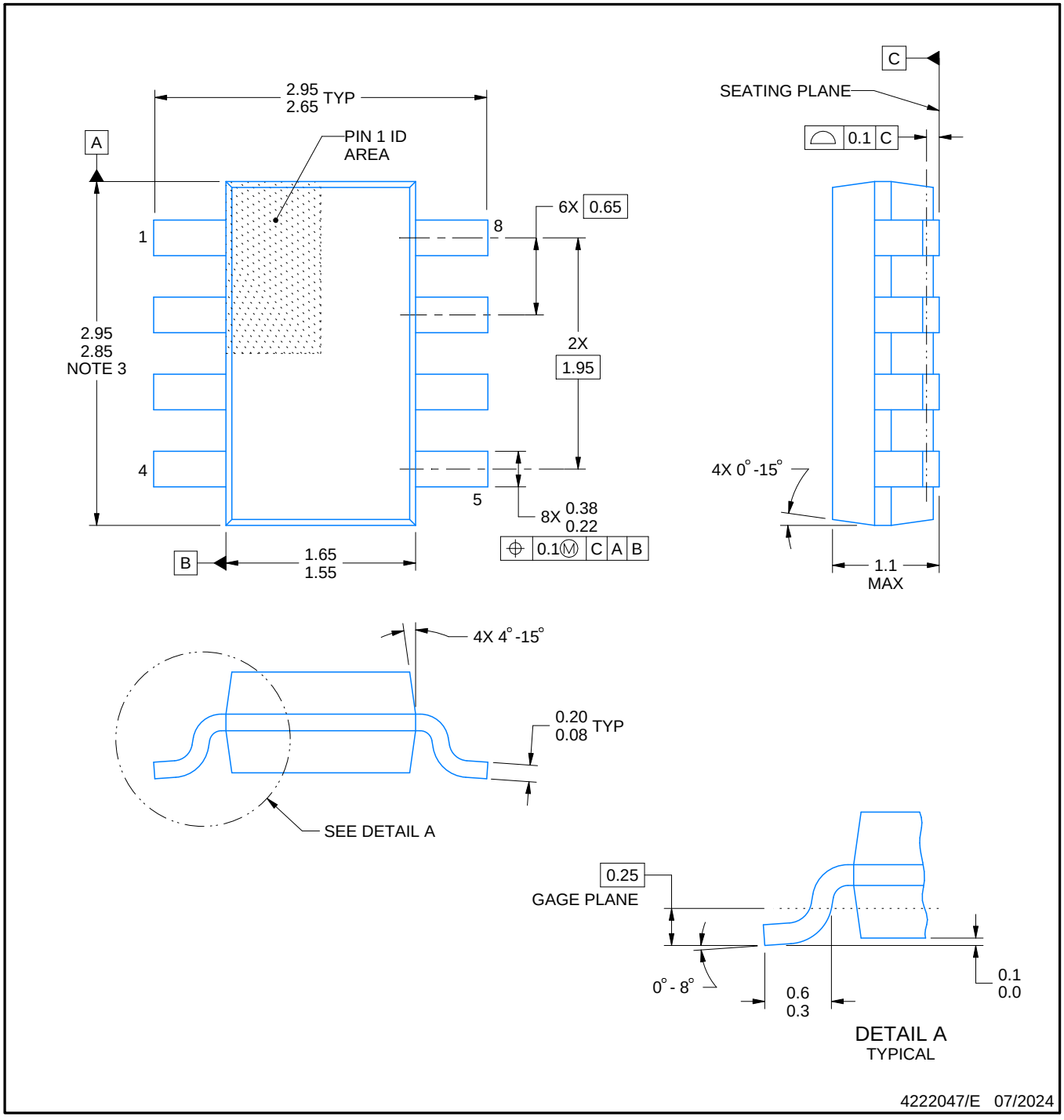
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3762BM6OVDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3762BUV05DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3762D02OVDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3762DW4W4DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3762EG4OVDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3762EUV02DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3762EUVF4DDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TPS3762F02OVDDFRQ1	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DDF0008A

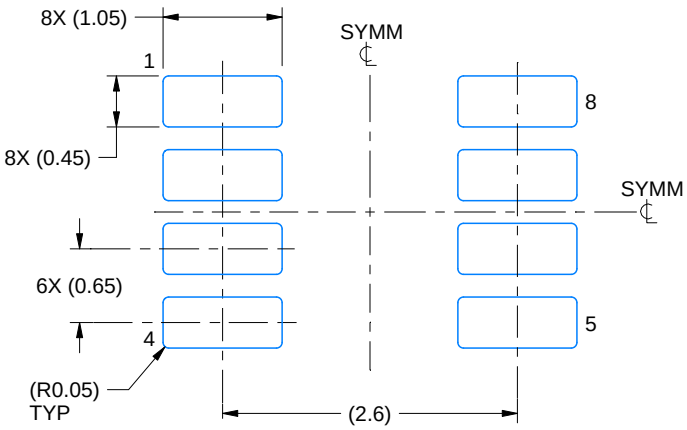
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

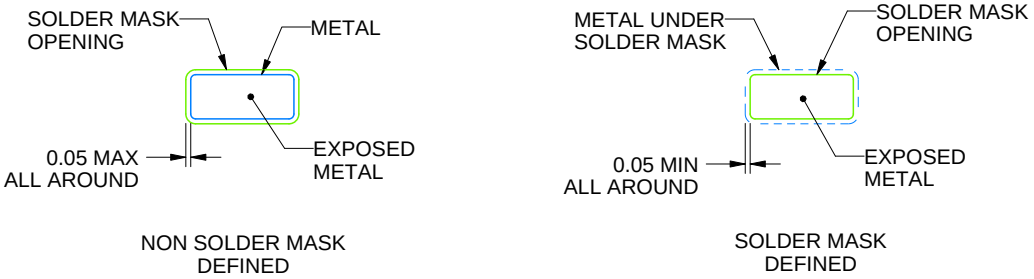


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

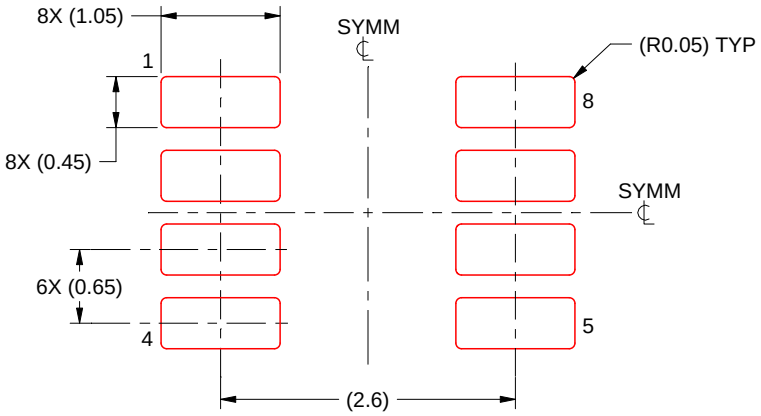
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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