# TPS4800-Q1 100V Automotive Low $I_Q$ High Side Driver With Reverse Polarity Protection, Short-Circuit Protection and Diagnostics

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 3.5V to 95V input range (100V absolute maximum)
- Reverse input protection down to –65V
- Integrated 11V charge pump
- Low quiescent current, 46μA in operation
- Low 1μA shutdown current (EN/UVLO = Low)
- Strong gate driver (1.69A source, 2A sink)
- Adjustable short circuit protection (ISCP) using external Rsense or MOSFET VDS sensing with adjustable delay (TMR)
- High / low-side current sense (CS_SEL)
- Fault indication ($\overline{\text{FLT}}$) during short circuit fault, input under voltage and short-circuit comparator diagnosis (SCP_TEST)
- Fault indication (FLT_GD) for gate drive UVLO
- Adjustable input undervoltage lockout (UVLO) and overvoltage protection (OV)

## 2 Applications

- Automotive 48V BMS
- DC/DC converter
- Power tools

## 3 Description

The TPS48000-Q1 is a 100V low $I_Q$ smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5V–95V, the device is suitable for 12V, 24V, and 48V system designs. The device can withstand and protect the loads from negative supply voltages down to –65V. It has a strong gate drive that enables power switching using parallel MOSFETs in high current system designs.

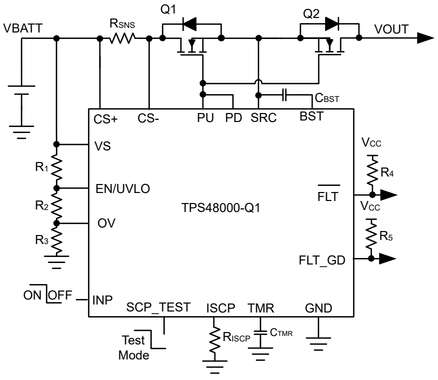
The device provides adjustable short circuit protection. Auto-retry and latch-off fault behavior can be configured. By using CS+ and CS– pins, current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. The device also features diagnosis of the internal short circuit comparator using external control on SCP_TEST input.

Low quiescent current of 46μA (typical) in operation enables always ON system designs. Quiescent current reduces to 1μA (typical) with EN/UVLO low. The device is available in a 19-pin VSSOP package.

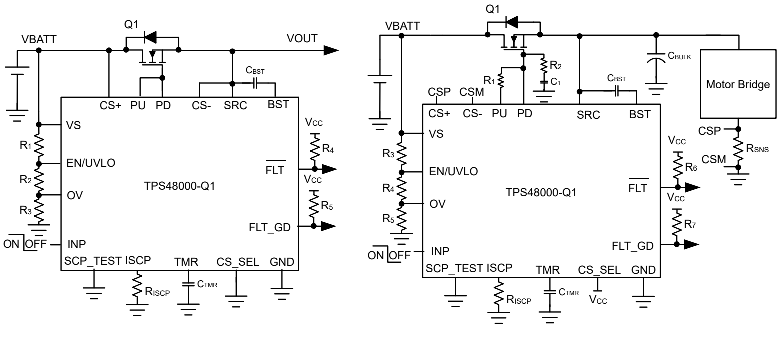
**Package Information**

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] |
|---|---|---|
| TPS48000-Q1 | DGX (VSSOP, 19) | 5.1mm × 3.0mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Smart High Side Driver for DC-DC**



**Configurations With High Side VDS Sensing and Low Side Current Sensing**

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# 4 Pin Configuration and Functions

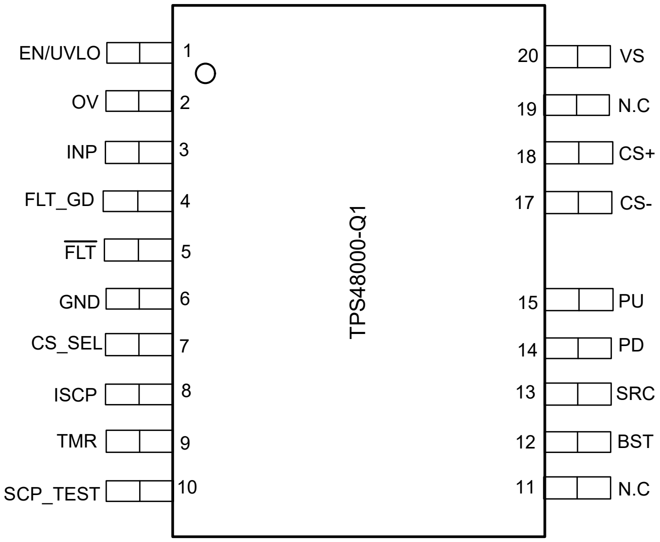


**Figure 4-1. DGX Package, 19-Pin VSSOP (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| **NAME** | **NO.** | | |
| EN/UVLO | 1 | I | EN/UVLO Input. A voltage higher than 1V on this pin enables normal operation. Forcing this pin below 0.3V shuts down the device reducing quiescent current to 1µA (typical). Optionally connect to the input supply through a resistive divider to set the undervoltage lockout.<br>When EN/UVLO is left floating an internal pull down pulls EN/UVLO low and keeps the device in shutdown state. |
| OV | 2 | I | Adjustable overvoltage threshold input. Connect a resistor ladder from input supply, OV to GND. When the voltage at OVP exceeds the overvoltage cut-off threshold then the PD is pulled down to SRC turning OFF the external FET. When the voltage at OV goes below OV falling threshold then PU gets pulled up to BST, turning ON the external FET.<br>OV must be connected to GND when not used. When OV is left floating an internal pull down pulls OV low and keeps PU pulled up to BST. |
| INP | 3 | I | Input Signal for external discharge FET control. CMOS compatible input reference to GND that sets the state of PD and PU pins.<br>INP has an internal weak pull down to GND to keep PD pulled to SRC when INP is left floating. |
| FLT_GD | 4 | O | Open Drain Fault Output for gate drive UVLO. This pin asserts low when gate drive across PD to SRC is above 7V (typ.). |
| $\overline{\text{FLT}}$ | 5 | O | Open Drain Fault Output. This pin asserts low during short circuit fault, input UVLO, overvoltage and during SCP comparator diagnosis. If $\overline{\text{FLT}}$ feature is not desired then connect it to GND. |
| GND | 6 | G | Connect GND to system ground. |
| CS_SEL | 7 | I | Current sense select input. Connect this pin to ground to activate high side current sense. Drive this pin to >1.58V to activate low side current sensing.<br>CS_SEL has an internal weak pull down to GND. |

### Table 4-1. Pin Functions (continued)

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| **NAME** | **NO.** | | |
| ISCP | 8 | I | Short circuit detection setting. A resistor across ISCP to GND sets the short circuit current comparator threshold.<br>If short-circuit protection feature is not desired then connect CS+, CS–, VS pins together and connect ISCP, TMR pins to GND. |
| TMR | 9 | I | Fault Timer Input. A capacitor across TMR pin to GND sets the times for fault turn-off.<br>Leave it open for fastest setting.<br>If short-circuit protection feature is not desired then connect CS+, CS–, VS pins together and connect ISCP, TMR pins to GND. |
| SCP_TEST | 10 | I | Internal short circuit comparator (SCP) diagnosis input. When SCP_TEST is driven low to high with INP pulled high, the internal SCP comparator operation is checked. $\overline{\text{FLT}}$ goes low and PD gets pulled to SRC if SCP comparator is functional.<br>Connect SCP_TEST pin to GND if this feature is not desired. SCP_TEST has an internal weak pull down to GND. |
| N.C | 11 | — | No connect. |
| BST | 12 | O | High Side Bootstrapped Supply. An external capacitor with a minimum value of $>Q_{g(tot)}$ of the external FET must be connected between this pin and SRC. |
| SRC | 13 | O | Source connection of the external FET. |
| PD | 14 | O | High Current Gate Driver Pull-Down. This pin pulls down to SRC. For the fastest turn-off, tie this pin directly to the gate of the external high side MOSFET. |
| PU | 15 | O | High Current Gate Driver Pull-Up. This pin pulls up to BST. Connect this pin to PD for maximum gate drive transition speed. A resistor can be connected between this pin and the gate of the external MOSFET to control the in-rush current during turn-on. |
| CS- | 17 | I | Current sense negative input. |
| CS+ | 18 | I | Current sense positive input. |
| N.C | 19 | — | No connect. |
| VS | 20 | P | Supply pin of the controller. |

(1) I = input, O = output, I/O = input and output, P = power, G = Ground

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input Pins | VS, CS+, CS– to GND | –65 | 100 | V |
| | SRC to GND | –65 | 100 | |
| | PU, PD, BST to SRC | –0.3 | 19 | |
| | ISCP, TMR, SCP_TEST to GND | –0.3 | 5.5 | |
| | EN/UVLO, OV, INP, CS_SEL, $V_{(VS)} > 0$ V | –1 | 70 | |
| | EN/UVLO, OV, INP, CS_SEL, $V_{(VS)} \le 0$ V | $V_{(VS)}$ | $(70 + V_{(VS)})$ | |
| | CS+ to CS– | –1 | 100 | V |
| | $\overline{\text{FLT}}$, FLT_GD to GND | –1 | 20 | V |
| Sink current | $I_{(\overline{FLT})}$ | | 10 | mA |
| | $I_{(CS+)}$, $I_{(CS–)}$, 1msec | –100 | 100 | mA |
| Output Pins | PU, PD, G2, BST to GND | –65 | 112 | V |
| Operating junction temperature, $T_j$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | Corner pins (EN/UVLO, VS, SCP_TEST) | ±750 | |
| | | | Other pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Pins | VS to GND | 3.5 | | 95 | V |
| | Minimum voltage on VS pin for Short Circuit Protection | 4 | | | |
| | EN/UVLO, INP, CS_SEL to GND | 0 | | 65 | |
| Output Pins | $\overline{\text{FLT}}$ to GND | 0 | | 15 | V |
| External Capacitor | VS, SRC to GND | 22 | | | nF |
| | BST to SRC | 0.1 | | | µF |
| Tj | Operating Junction temperature | –40 | | 150 | °C |

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see Electrical Characteristics.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TPS4800-Q1 | UNIT |
|---|---|---|---|
| | | DGX | |
| | | 19 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 92.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 28.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 47.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.6 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 47.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

$T_J$ = –40 °C to +150°C. $V_{(VS)}$ = 48 V, $V_{(BST – SRC)}$ = 11 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| VS | Operating input voltage | | 3.5 | | 95 | V |
| $V_{(S\_PORR)}$ | Input supply POR threshold, rising | | 1.7 | 2.5 | 3.34 | V |
| $V_{(S\_PORF)}$ | Input supply POR threshold, falling | | 1.7 | 2.4 | 3.16 | V |
| $I_{(GND)}$ | Total System Quiescent current | $V_{(EN/UVLO)}$ = 2 V | | 46 | 56 | µA |
| | | $V_{(EN/UVLO)}$ = 2 V, –40°C ≤ $T_J$ ≤ +85°C | | | 53 | µA |
| $I_{(SHDN)}$ | SHDN current, $I_{(GND)}$ | $V_{(EN/UVLO)}$ = 0 V, $V_{(SRC)}$ = 0 V | | 1 | 4.3 | µA |
| $I_{(REV)}$ | $I_{(VS)}$ leakage current during Reverse Polarity | 0 V ≤ $V_{(VS)}$ ≤ – 65 V | 15 | 22.1 | 38 | µA |
| **ENABLE, UNDERVOLTAGE LOCKOUT (EN/UVLO), SHORT CIRCUIT COMPARATOR TEST (SCP_TEST) INPUT** | | | | | | |
| $V_{(UVLOR)}$ | UVLO threshold voltage, rising | | 1.17 | 1.23 | 1.29 | V |
| $V_{(UVLOF)}$ | UVLO threshold voltage, falling | | 1.09 | 1.14 | 1.19 | V |
| $V_{(ENR)}$ | Enable threshold voltage, rising | | | | 1 | V |
| $V_{(ENF)}$ | Enable threshold voltage, falling | | 0.3 | | | V |
| $I_{(EN/UVLO)}$ | Enable input leakage current | $V_{(EN/UVLO)}$ = 70 V | | 174 | 490 | nA |
| $V_{(SCP\_TEST\_H)}$ | SCP test mode rising threshold | | | | 2 | V |
| $V_{(SCP\_TEST\_L)}$ | SCP test mode falling threshold | | 0.8 | | | V |
| $I_{(SCP\_TEST)}$ | SCP_TEST input leakage current | | | 90 | 730 | nA |
| **OVER VOLTAGE PROTECTION (OV) INPUT** | | | | | | |
| $V_{(OVR)}$ | Overvoltage threshold input, risIng | | 1.17 | 1.23 | 1.28 | V |
| $V_{(OVF)}$ | Overvoltage threshold input, falling | | 1.08 | 1.14 | 1.19 | V |
| $I_{(OV)}$ | OV Input leakage current | | | 86 | 205 | nA |
| **CHARGE PUMP (BST–SRC)** | | | | | | |
| $I_{(BST)}$ | Charge Pump Supply current | $V_{(BST – SRC)}$ = 10 V, $V_{(EN/UVLO)}$ = 2 V | 100 | 345 | 555 | µA |
| $V_{(BST\_UVLOR)}$ | $V_{(BST – SRC)}$ UVLO voltage threshold, rising | $V_{(EN/UVLO)}$ = 2 V | 7.19 | 9 | 10.81 | V |
| $V_{(BST\_UVLOF)}$ | $V_{(BST – SRC)}$ UVLO voltage threshold, falling | $V_{(EN/UVLO)}$ = 2 V | 6.54 | 8.2 | 9.64 | V |
| $V_{(BST–SRC\_ON)}$ | Charge Pump Turn ON voltage | $V_{(EN/UVLO)}$ = 2 V | 8.24 | 10.3 | 12.46 | V |
| $V_{(BST–SRC\_OFF)}$ | Charge Pump Turn OFF voltage | $V_{(EN/UVLO)}$ = 2 V | 9.34 | 11.6 | 13.86 | V |
| $V_{(BST–SRC)}$ | Charge Pump Voltage at $V_{(VS)}$ = 3.5 V | $V_{(EN/UVLO)}$ = 2 V | 8.9 | 10.5 | 11.82 | V |
| **GATE DRIVER OUTPUTS (G1PU, G1PD)** | | | | | | |

## 5.5 Electrical Characteristics (continued)

$T_J$ = –40 °C to +150°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{(PU)}$ | Peak Source Current | | | 1.69 | | A |
| $I_{(PD)}$ | Peak Sink Current | | | 2 | | A |
| $V_{(G\_GOOD)}$ | VGS good threshold | | 5.32 | 7 | 8.48 | V |
| **SHORT CIRCUIT PROTECTION (ISCP)** | | | | | | |
| $I_{SCP}$ | SCP Input Bias current | | 8.22 | 10 | 12.51 | µA |
| $V_{(SCP)}$ | SCP threshold | $R_{(ISCP)}$ = 140.5 kΩ | 283 | 300 | 318 | mV |
| | | $R_{(ISCP)}$ = 28 kΩ | 58.4 | 75 | 91.6 | mV |
| | | $R_{(ISCP)}$ = 10.5 kΩ | 31.1 | 40 | 48.9 | mV |
| | | $R_{(ISCP)}$ = 500 Ω | 14.9 | 20 | 25.2 | mV |
| | | $R_{(ISCP)}$ = Open | 468 | 560 | 651 | mV |
| $V_{(SCP)}$ | SCP threshold with external bias on ISCP pin | $V_{(ISCP)}$ = 3 V | 470 | 563 | 642 | mV |
| | | $V_{(ISCP)}$ = 1.405 V | 279 | 300 | 319 | mV |
| | | $V_{(ISCP)}$ = 280 mV | 67 | 75 | 83 | mV |
| | | $V_{(ISCP)}$ = 105 mV | 33 | 40 | 47 | mV |
| **DELAY TIMER (TMR)** | | | | | | |
| $I_{(TMR\_SRC\_CB)}$ | TMR source current | | 65 | 87 | 106 | µA |
| $I_{(TMR\_SRC\_FLT)}$ | TMR source current | | 1.33 | 2.73 | 3.87 | µA |
| $I_{(TMR\_SNK)}$ | TMR sink current | | 2.14 | 2.8 | 3.43 | µA |
| $V_{(TMR\_SC)}$ | TMR input clamp level | | 0.87 | 1.1 | 1.26 | V |
| $V_{(TMR\_LOW)}$ | TMR input low level | | 0.14 | 0.21 | 0.26 | V |
| $N_{(A\text{-}R\ Count)}$ | Number of TMR charge-discharge cycles | | | 32 | | |
| **INPUT CONTROL (INP), FAULT FLAGS ($\overline{\text{FLT}}$, FLT_GD)** | | | | | | |
| $R_{(\overline{FLT})}$, $R_{(FLT\_GD)}$ | $\overline{\text{FLT}}$, FLT_GD Pull-down resistance | | 52 | 85 | 107 | Ω |
| $I_{(\overline{FLT})}$, $I_{(FLT\_GD)}$ | $\overline{\text{FLT}}$, FLT_GD Input leakage current | 0 V ≤ $V_{(\overline{FLT})}$ ≤ 20 V | | | 410 | nA |
| $V_{(INP\_H)}$ | INP Input logic high level | | | | 2 | V |
| $V_{(INP\_L)}$ | INP input logic low level | | 0.8 | | | V |
| $I_{(INP)}$ | INP Input leakage current | | | 89 | 210 | nA |
| $V_{(CS\_SEL\_H)}$ | CS_SEL threshold for low side sensing | | 1.25 | | 1.58 | V |
| $V_{(CS\_SEL\_L)}$ | CS_SEL threshold for high side sensing | | 0.66 | | 1.14 | V |
| $I_{(CS\_SEL)}$ | CS_SEL Input leakage current | | 10 | 88.8 | 210 | nA |

## 5.6 Switching Characteristics

$T_J$ = –40 °C to +150°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PU(INP\_H)}$ | INP Turn ON propagation Delay | INP ↑ to PU ↑, $C_L$ = 47 nF | 0.32 | | 1.68 | µs |
| $t_{PD(INP\_L)}$ | INP Turn OFF propagation Delay | INP ↓ to PD ↓, $C_L$ = 47 nF | | 0.36 | 1.05 | µs |
| $t_{PD(EN\_OFF)}$ | EN Turn OFF Propagation Delay | EN ↓ to PD ↓, $C_L$ = 47 nF | 1.68 | 4.6 | 6.52 | µs |
| $t_{PD(UVLO\_OFF)}$ | UVLO Turn OFF Propagation Delay | UVLO ↓ to PD ↓ and $\overline{\text{FLT}}$ ↓, $C_L$ = 47 nF | 2.22 | 4.8 | 6.58 | µs |
| $t_{PD(OV\_OFF)}$ | OV Turn Off propagation Delay | OV ↑ to PD ↓ and $\overline{\text{FLT}}$ ↓, $C_L$ = 47 nF | | 4.5 | 5.55 | µs |
| $t_{SC}$ | Hard Short-circuit protection propagation delay | $V_{(CS+-CS-)}$↑ $V_{(SCP)}$ to PD ↓, CL = 47 nF, $C_{(TMR)}$ = Open | | | 4 | µs |

## 5.6 Switching Characteristics (continued)

$T_J$ = –40 °C to +150°C. $V_{(VS)}$ = 48 V, $V_{(BST-SRC)}$ = 11 V

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{SC\_PUS}$ | Short-circuit protection propagation delay during power up with output short circuit | $C_{TMR}$ = Open | | | 10 | µs |
| $t_{PD(\overline{FLT}\_SC)}$ | $\overline{FLT}$ assertion delay during short circuit | $V_{(CS+-CS-)}$↑ $V_{(SCP)}$ to $\overline{FLT}$ ↓, $C_{(TMR)}$ = Open | | 10.5 | 15 | µs |
| $F_{ISCP}$ | ISCP Pulse current frequency | | | 1.18 | | kHz |
| $t_{PD(FLT\_GD)}$ | FLT assertion delay during Gate Drive UVLO | $V_{(PD-SRC)}$ ↑ $V_{(BSTUVLOR)}$ to FLT_GD ↓ | | 120 | | µs |
| $t_{PD(FLT\_GD)}$ | FLT de-assertion delay during Gate Drive UVLO | $V_{(PD-SRC)}$ ↓ $V_{(BSTUVLOR)}$ to FLT_GD ↑ | | 127 | | µs |

## 5.7 Typical Characteristics

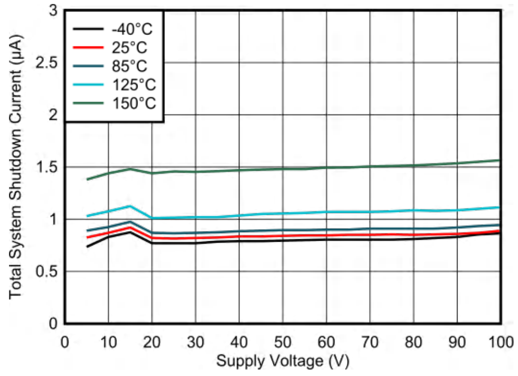


Figure 5-1. Shutdown Supply Current vs Supply Voltage

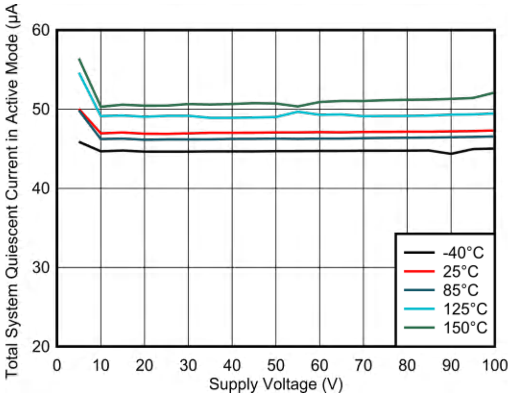


Figure 5-2. Operating Quiescent Current in Active Mode vs Supply Voltage

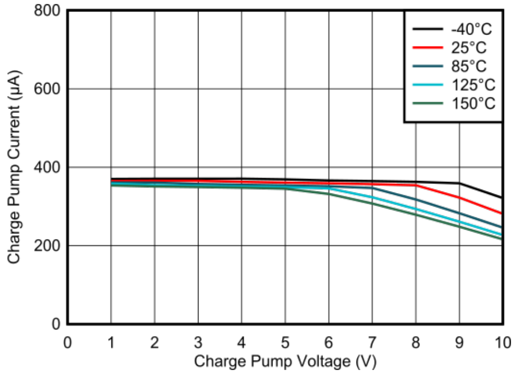
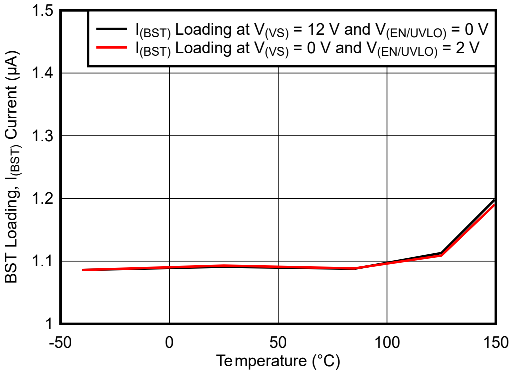


Figure 5-3. Charge Pump Current vs Charge Pump Voltage



$V_{(BST)}$ = 15 V $V_{(SRC)}$ = 0 V

Figure 5-4. BST Loading Current ($I_{(BST)}$) vs Temperature

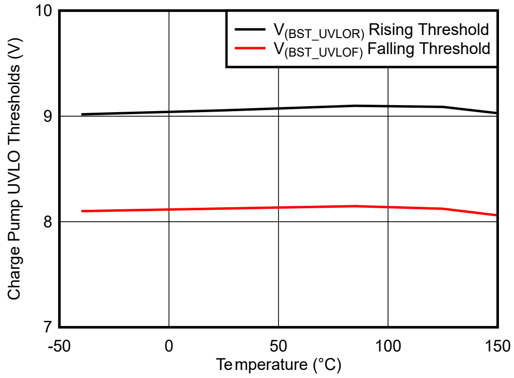


Figure 5-5. Charge Pump UVLO Thresholds vs Temperature

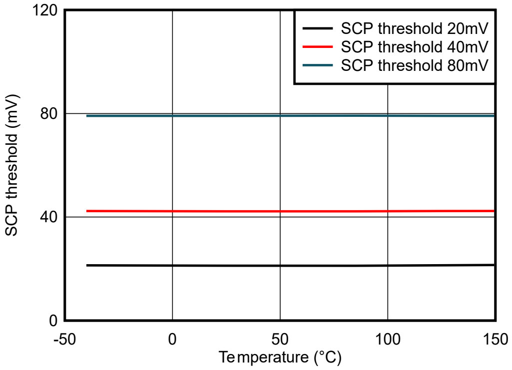


Figure 5-6. Short-Circuit Threshold ($V_{(SCP)}$) vs Temperature

## 5.7 Typical Characteristics (continued)

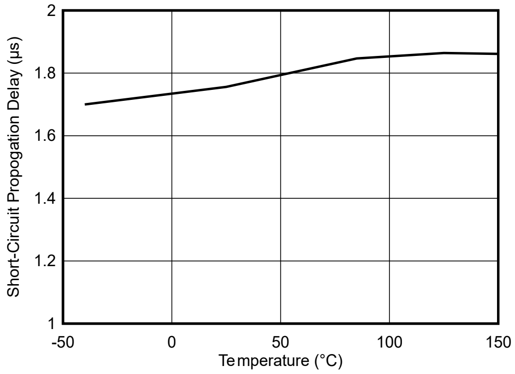


**Figure 5-7. Short Circuit Protection Response Time ($t_{SC}$) vs Temperature**

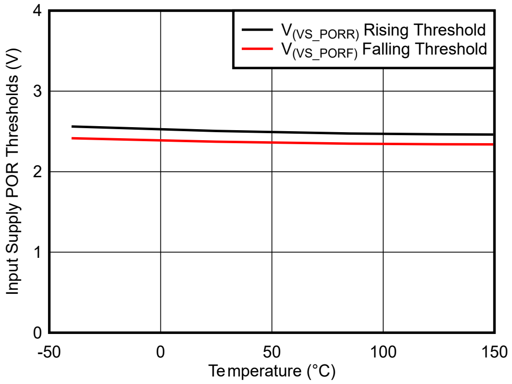


**Figure 5-8. Input Supply POR Thresholds vs Temperature**

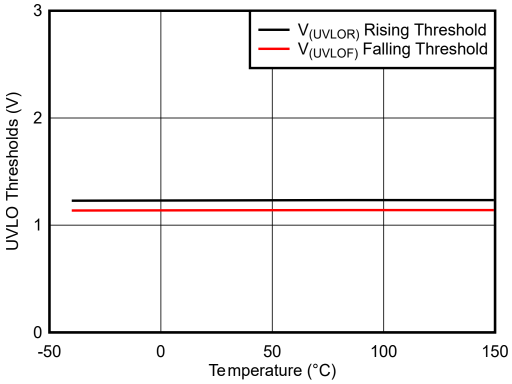


**Figure 5-9. Input Supply UVLO Thresholds vs Temperature**

# 6 Parameter Measurement Information

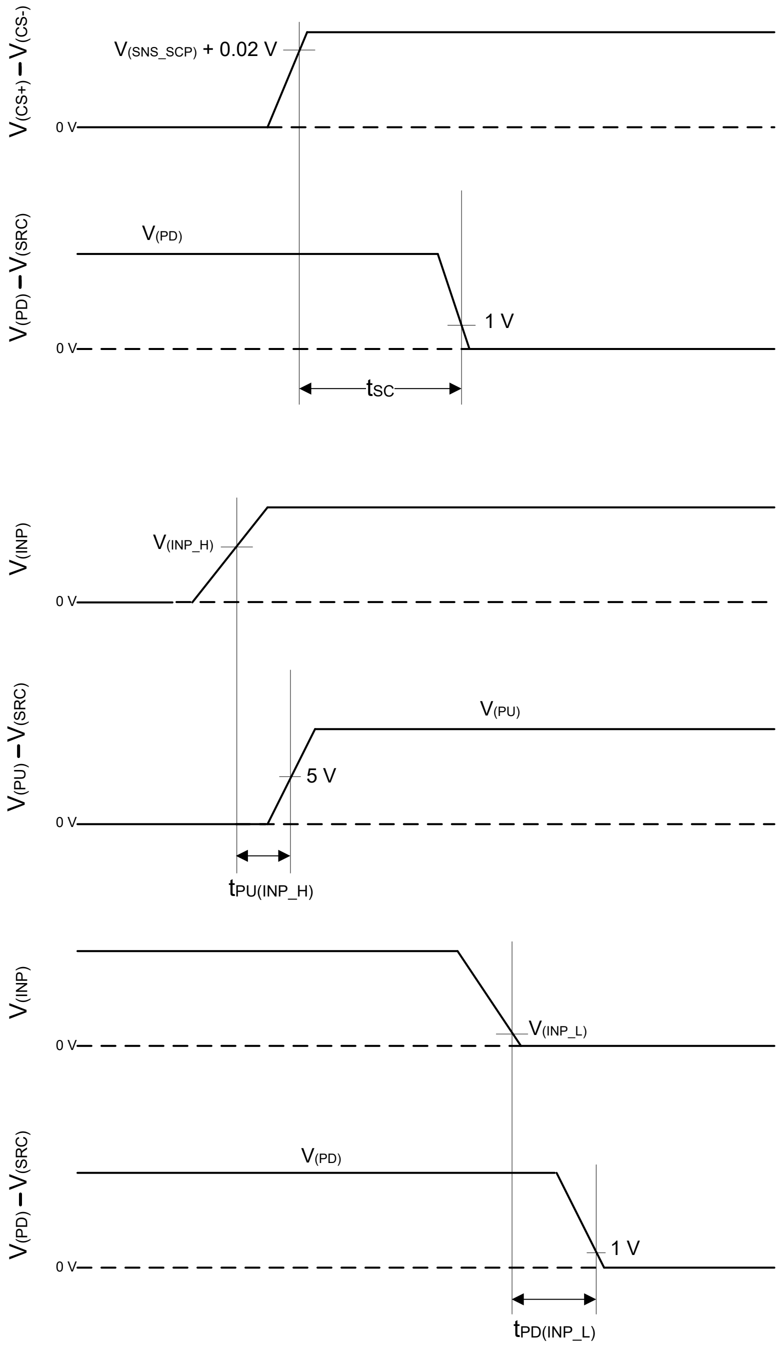


**Figure 6-1. Timing Waveforms**

# 7 Detailed Description

## 7.1 Overview

The TPS48000-Q1 is a 100-V low IQ smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V–95V, the device is suitable for 12V, 24V and 48V system designs. The device can withstand and protect the loads from negative supply voltages down to –65V.

It has a strong 1.69A/2A peak source/sink gate driver that enables power switching using parallel FETs in high current system designs.

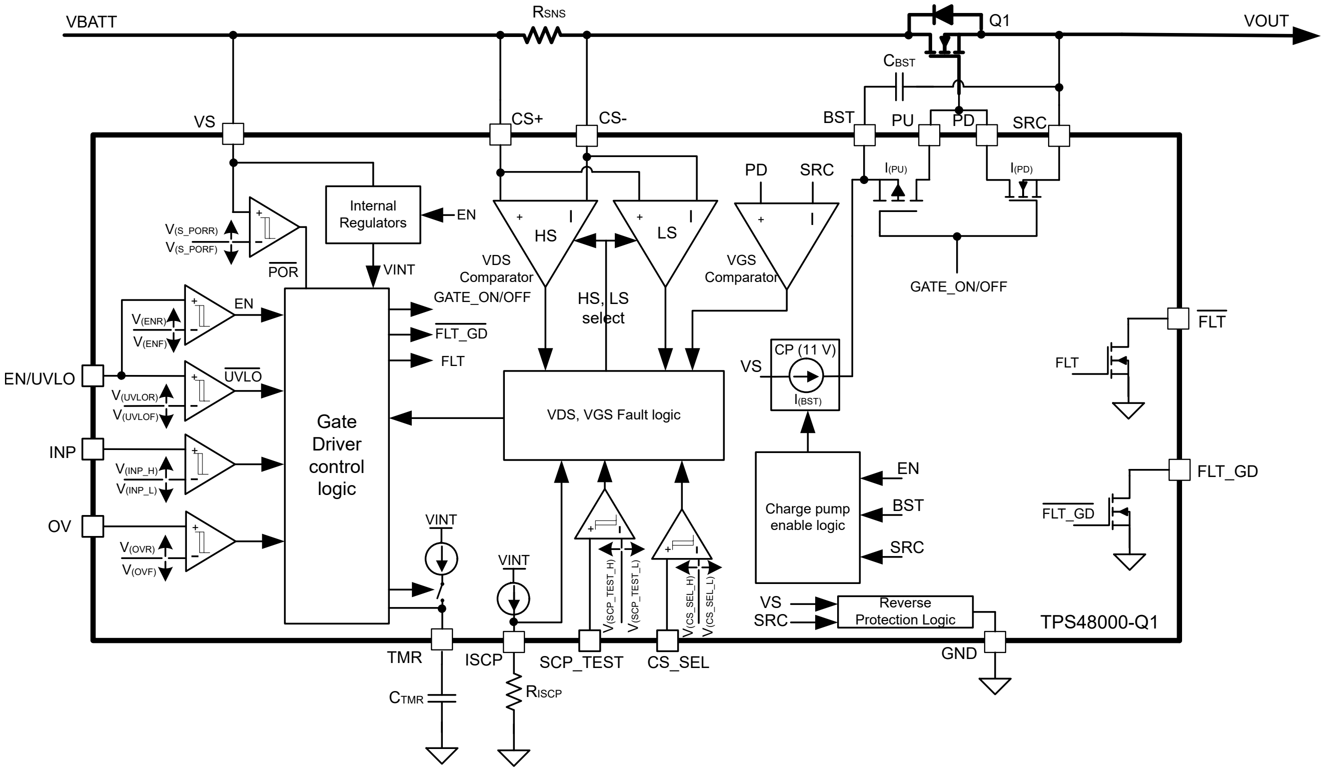
The device provides configurable short circuit protection using ISCP and TMR pins for adjusting the threshold and response time respectively. Auto-retry and latch-off fault behavior can be configured. Current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High side or low side current sense resistor configuration is possible by using CS_SEL pin input. Diagnosis of the integrated short circuit comparator is possible using external control on SCP_TEST input.

The device has adjustable under voltage and overvoltage protection.

The device indicates fault ($\overline{\text{FLT}}$) on open drain output during during short circuit and input under voltage, overvoltage conditions. It also have a dedicate fault indication (FLT_GD) to indicate the gate drive UVLO condition.

Low Quiescent Current 46µA (typical) in operation enables always ON system designs. Quiescent current reduces to 1µA (typical) with EN/UVLO low.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### *7.3.1 Charge Pump and Gate Driver Output (VS, PU, PD, BST, SRC)*

Figure 7-1 shows a simplified diagram of the charge pump and gate driver circuit implementation. The device houses a strong 1.69A/2A peak source/sink gate driver (PU, PD) for driving power FET. The strong gate drivers enable paralleling of FETs in high power system designs ensuring minimum transition time in saturation region. A 11V, 345µA charge pump is derived from VS terminal and charges the external boot-strap capacitor, $C_{BST}$ that is placed across the gate driver (BST and SRC).

VS is the supply pin to the controller. With VS applied and EN/UVLO pulled high, the charge pump turns ON and charges the $C_{BST}$ capacitor. After the voltage across $C_{BST}$ crosses $V_{(BST\_UVLOR)}$, the GATE driver section is activated. The UVLO hysteresis ensures chattering less performance during initial GATE turn ON. Choose $C_{BST}$ based on the external FET $Q_G$ and allowed dip during FET turn-ON. The charge pump remains enabled until the BST to SRC voltage reaches $V_{(BST–SRC\_OFF)}$, at which point the charge pump is disabled decreasing the current draw on the VS pin. The charge pump remains disabled until the BST to SRC voltage discharges to $V_{(BST–SRC\_ON)}$ at which point the charge pump is enabled. The voltage between BST and SRC continue to charge and discharge between these two limits as shown in the Figure 7-2.

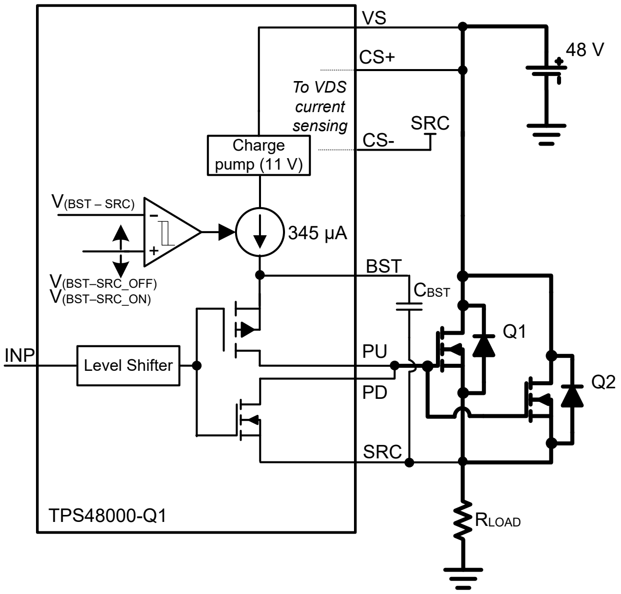


**Figure 7-1. Gate Driver**

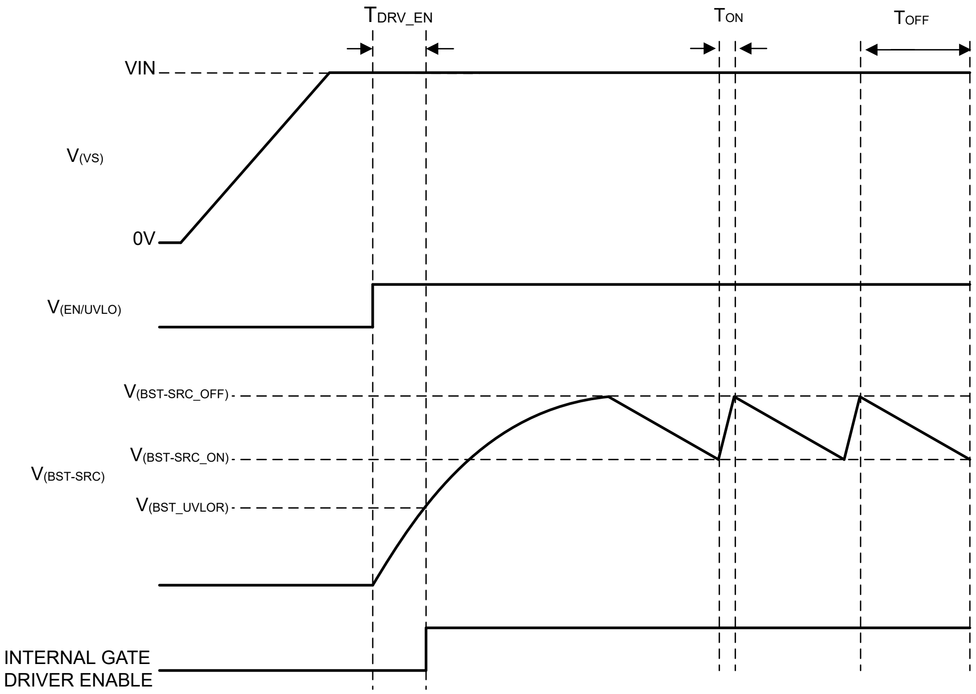


**Figure 7-2. Charge Pump Operation**

Use the following equation to calculate the initial gate driver enable delay:

$$T_{DRV\_EN} = \frac{C_{BST} \times V_{(BST\_UVLOR)}}{345\ \mu A} \tag{1}$$

Where,

$C_{BST}$ is the charge pump capacitance connected across BST and SRC pins.

$V_{(BST\_UVLOR)}$ = 10.81V (max).

If $T_{DRV\_EN}$ must be reduced then pre-bias BST terminal externally using an external $V_{AUX}$ supply through a low leakage diode $D_1$ as shown in Figure 7-3. TPS48000-Q1 application circuit with external supply to BST is shown in Figure 7-3.

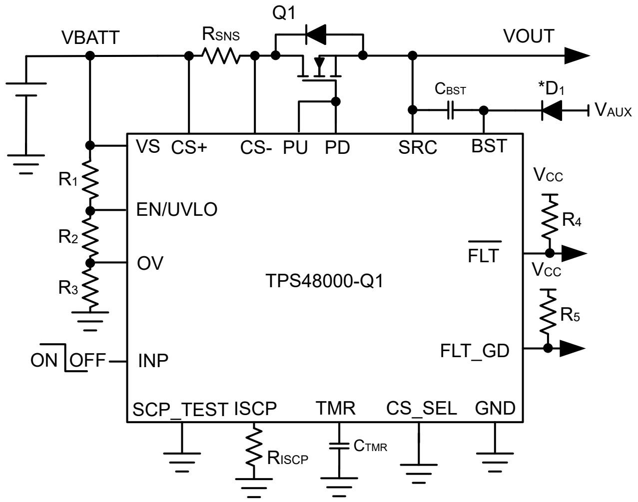


**Figure 7-3. TPS48000-Q1 Application Circuit With External Supply to BST**

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**Note**

$V_{AUX}$ can be supplied by external regulated supply ranging between 8V and 18V.

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### 7.3.2 Capacitive Load Driving Using FET Gate (PU, PD) Slew Rate Control

Certain end equipments like automotive power distribution unit power different loads including other ECUs. These ECUs can have large input capacitances. If power to the ECUs is switched on in uncontrolled way, large inrush currents can occur potentially damaging the power FETs. To limit the inrush current during capacitive load switching, the following system design technique can be used with TPS48000-Q1.

For limiting inrush current during turn ON of the FET with capacitive loads, use $R_1$, $R_2$, $C_1$ as shown in Figure 7-4. The $R_1$ and $C_1$ components slow down the voltage ramp rate at the gate of the FET. The FET source follows the gate voltage resulting in a controlled voltage ramp across the output capacitors.

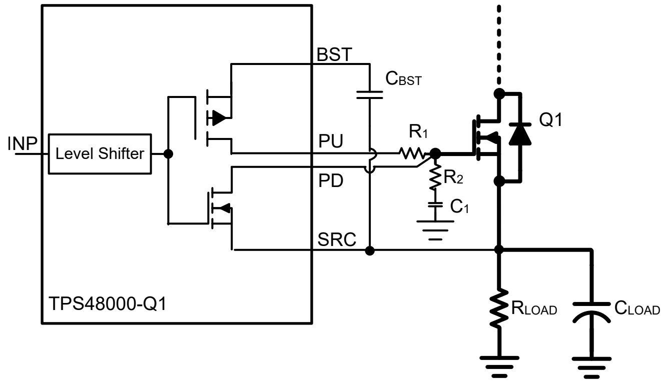


**Figure 7-4. Inrush Current limiting**

Use the Equation 2 to calculate the inrush current during turn-ON of the FET.

$$I_{INRUSH} = C_{LOAD} \times \frac{V_{BATT}}{T_{charge}} \tag{2}$$

$$C_1 = \frac{0.63 \times V_{(BST\ -\ SRC)} \times C_{LOAD}}{R_1 \times I_{INRUSH}} \tag{3}$$

Where,

$C_{LOAD}$ is the load capacitance,

VBATT is the input voltage and $T_{charge}$ is the charge time,

$V_{(BST\text{-}SRC)}$ is the charge pump voltage (11V),

Use a damping resistor $R_2$ (~ 10Ω) in series with $C_1$. Equation 3 can be used to compute required $C_1$ value for a target inrush current. A 100kΩ resistor for $R_1$ can be a good starting point for calculations.

Connecting PD pin of TPS48000-Q1 directly to the gate of the external FET ensures fast turn OFF without any impact of $R_1$ and $C_1$ components.

$C_1$ results in an additional loading on $C_{BST}$ to charge during turn-ON. Use below equation to calculate the required $C_{BST}$ value:

$$C_{BST} = \frac{Q_{g(total)}}{\Delta V_{BST}} + 10 \times C_1 \tag{4}$$

Where,

$Q_{g(total)}$ is the total gate charge of the FET.

$\Delta V_{BST}$ (1V typical) is the ripple voltage across BST to SRC pins.

### *7.3.3 Short-Circuit Protection*

The TPS48000-Q1 feature adjustable short circuit protection. The threshold and response time can be adjusted using $R_{ISCP}$ resistor and $C_{TMR}$ capacitor respectively. The device senses the voltage across CS+ and CS– pins. These pins can be connected across the FET drain and source terminals for FET $R_{DSON}$ sensing or across an external high and low side current sense resistor ($R_{SNS}$) as shown in Figure 7-5, Figure 7-6, , Figure 7-7 and Figure 7-8 respectively.

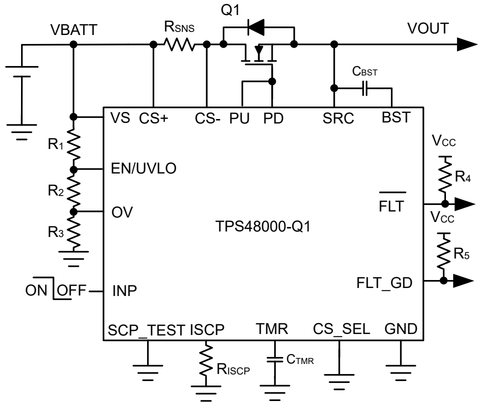


**Figure 7-5. TPS48000-Q1 Application Circuit With External Sense Resistor RSNS Based High Side Current Sensing**

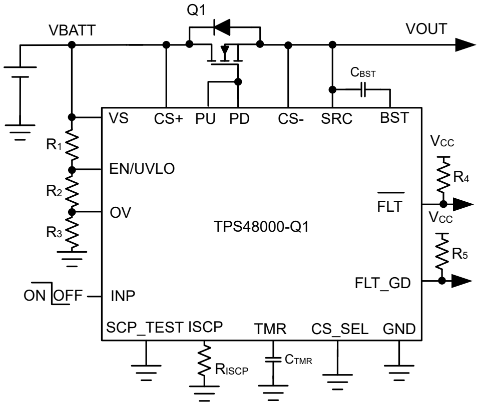


**Figure 7-6. TPS48000-Q1 Application Circuit With MOSFET RDSON Based Current Sensing**

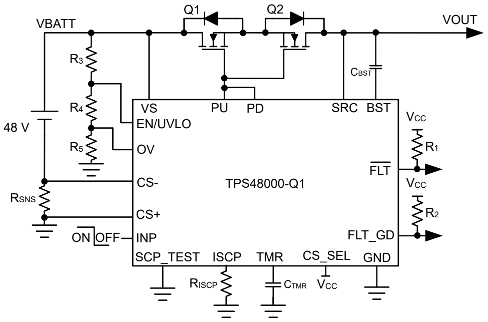


Figure 7-7. TPS48000-Q1 Application Circuit With External Sense Resistor RSNS Based Low Side Current Sensing on Battery Side

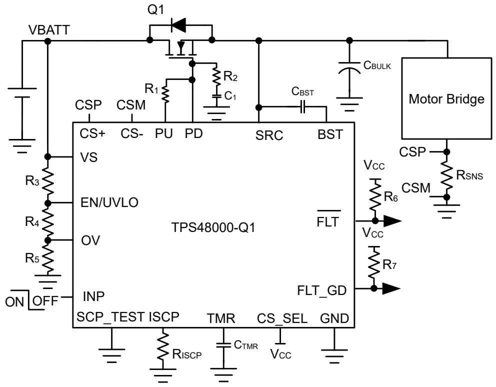


Figure 7-8. TPS48000-Q1 Application Circuit With External Sense Resistor RSNS Based Low Side Current Sensing

Set the short-circuit detection threshold using an external $R_{ISCP}$ resistor across ISCP and GND pins. Use Equation 5 to calculate the required $R_{ISCP}$ value:

$$R_{ISCP}\left(\Omega\right) = \frac{(I_{SC} \times R_{SNS} - 19\ \text{mV})}{2\ \mu\text{A}} \tag{5}$$

Where,

$R_{SNS}$ is the high or low side current sense resistor value or the FET $R_{DSON}$ value.

$I_{SC}$ is the desired short circuit current level.

The short circuit protection response is fastest with no $C_{TMR}$ cap connected across TMR and GND pins.

With device powered ON and EN/UVLO, INP pulled high, During $Q_1$ turn ON, first VGS of external FET is sensed by monitoring the voltage across PD to SRC. Once PD to SRC voltage raises above $V_{(G\_GOOD)}$ (7V typical) threshold which ensures that the external FET is enhanced, then the SCP comparator output is monitored. If the sensed voltage across CS+ and CS– exceeds the short-circuit set point ($V_{SCP}$), PD pulls low to SRC and $\overline{\text{FLT}}$ asserts low. Subsequent events can be set either to be auto-retry or latch off as described in following sections.

VGS of external FET ($Q_1$) is only monitored when CS_SEL is pulled low. VGS of external FET ($Q_1$) is not monitored for low side current sensing as shown in Figure 7-7 and Figure 7-8.

**Note**

Short-circuit threshold can also be set by connecting external bias voltage on ISCP pin via buffer instead of $R_{ISCP}$ resistor enabling system design with improved SCP threshold accuracy as mentioned in electrical characteristics table. The external bias voltage to be forced on ISCP pin can be calculated by below eqaution:

$V_{(SCP\_BIAS)}$ in mV = $I_{SC}$ x $R_{SNS}$ x 5 - 95mV

**External bias voltage on ISCP pin should not exceed 3V.**

#### 7.3.3.1 Short-Circuit Protection With Auto-Retry

The $C_{TMR}$ programs the short-circuit protection delay ($t_{SC}$) and auto-retry time ($t_{RETRY}$). Once the voltage across CS+ and CS– exceeds the set point, the $C_{TMR}$ starts charging with $I_{(TMR\_SRC\_CB)}$ pull-up current.

After $C_{TMR}$ charges to $V_{(TMR\_SC)}$, PD pulls low to SRC and $\overline{\text{FLT}}$ asserts low providing warning on impending FET turn OFF. Post this event, the auto-retry behavior starts. The $C_{TMR}$ capacitor starts discharging with $I_{(TMR\_SNK)}$ pulldown current. After the voltage reaches $V_{(TMR\_LOW)}$ level, the capacitor starts charging with $I_{(TMR\_SRC\_FLT)}$ pullup. After 32 charging-discharging cycles of $C_{TMR}$ the FET turns ON back and $\overline{\text{FLT}}$ de-asserts.

The device retry time ($t_{RETRY}$) is based on $C_{TMR}$ for the first time as per Equation 7.

Use Equation 6 to calculate the $C_{TMR}$ capacitor to be connected across TMR and GND.

$$C_{TMR} = \frac{I_{TMR} \times t_{SC}}{1.1} \tag{6}$$

Where,

$I_{TMR}$ is internal pull-up current of 80μA.

$t_{SC}$ is desired short-circuit response time.

Leave TMR floating for fastest short-circuit response time.

$$t_{RETRY} = 22.7 \times 10^{6} \times C_{TMR} \tag{7}$$

If the short-circuit pulse duration is below $t_{SC}$ then the FET remains ON and $C_{TMR}$ gets discharged using internal pull down switch.

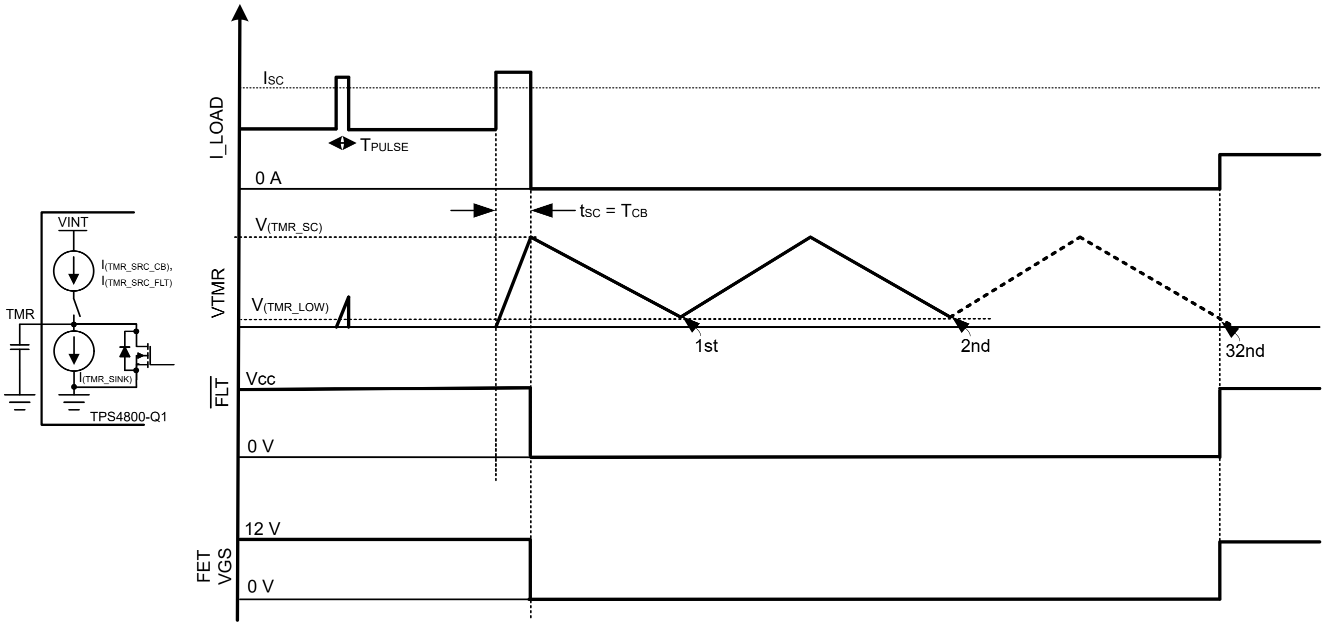


**Figure 7-9. Short-Circuit Protection With Auto-Retry**

### 7.3.3.2 Short-Circuit Protection With Latch-Off

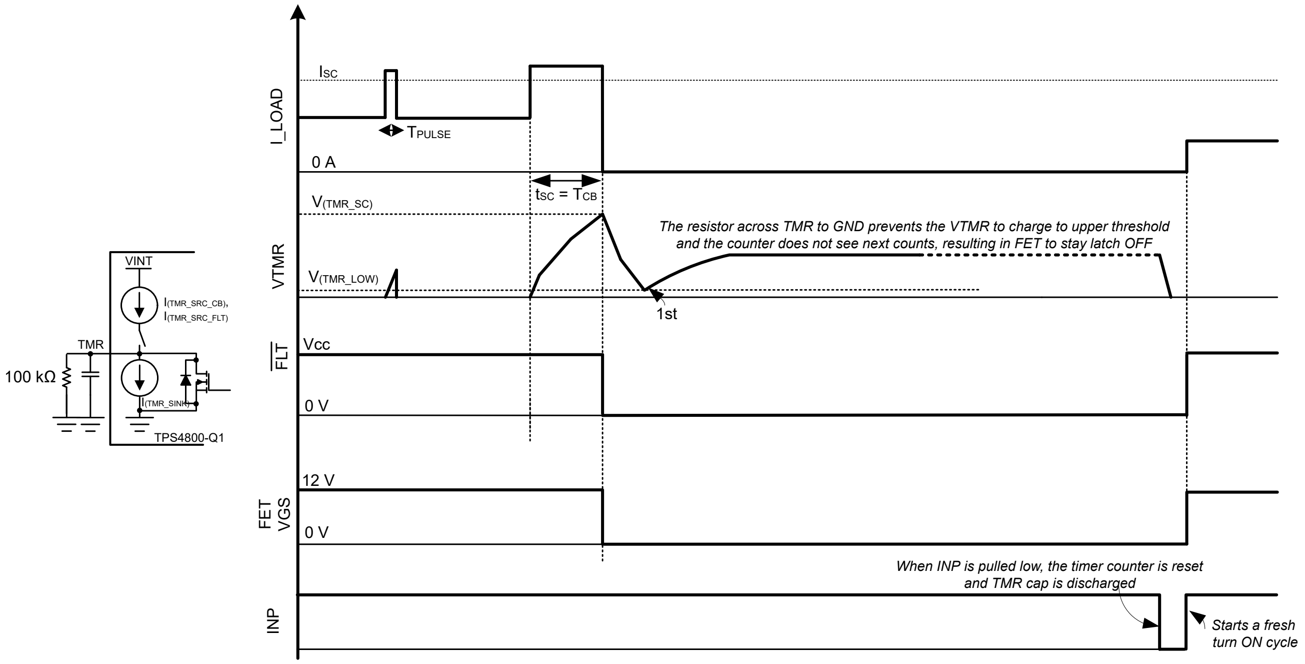
Connect an approximately 100kΩ resistor across $C_{TMR}$. With this resistor, during the charging cycle, the voltage across $C_{TMR}$ gets clamped to a level below $V_{(TMR\_SC)}$ resulting in a latch-off behavior and $\overline{\text{FLT}}$ asserts low at same time.

Use Equation 8 to calculate $C_{TMR}$ capacitor to be connected between TMR and GND for $R_{TMR}$ = 100kΩ.

$$C_{TMR} = \frac{t_{SC}}{R_{TMR} \times \ln\left(\frac{1}{1 - \frac{1.1}{R_{TMR} \times I_{TMR\_SRC\_CB}}}\right)} \tag{8}$$

Where, $t_{SC}$ is desired short-circuit response time.

Toggle INP or EN/UVLO (below $V_{(ENF)}$) or power cycle VS below $V_{(VS\_PORF)}$ to reset the latch. At low edge, the timer counter is reset and $C_{TMR}$ is discharged. PU pulls up to BST when INP is pulled high.



*The resistor across TMR to GND prevents the VTMR to charge to upper threshold and the counter does not see next counts, resulting in FET to stay latch OFF*

*When INP is pulled low, the timer counter is reset and TMR cap is discharged*

*Starts a fresh turn ON cycle*

**Figure 7-10. Short-Circuit Protection With Latch-Off**

### *7.3.4 Overvoltage (OV) and Undervoltage Protection (UVLO)*

TPS48000-Q1 has an accurate undervoltage protection using EN/UVLO pin and an accurate overvoltage protection, providing robust load protection. $\overline{\text{FLT}}$ is asserted when input undervoltage or overvoltage fault is detected. Connect a resistor ladder as shown in Figure 7-11 for undervoltage and overvoltage protection threshold programming.

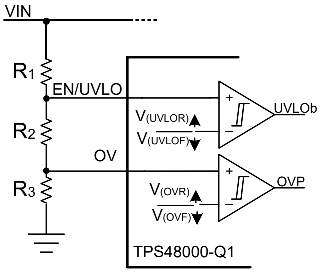


**Figure 7-11. Programming Overvoltage and Undervoltage Protection Threshold**

### *7.3.5 Reverse Polarity Protection*

The TPS48000-Q1 devices features integrated reverse polarity protection to protect the device from failing during input and output reverse polarity faults. Reverse polarity faults can occur during jump start, installation and maintenance of the end equipment's.

The device is tolerant to reverse polarity voltages down to -65V both on input and output.

On the output side, the device can see transient negative voltages during regular operation due to output cable harness inductance kickbacks when the switches are turned OFF. In such systems, the output negative voltage level is limited by the output side TVS or a diode.

### *7.3.6 Short-Circuit Protection Diagnosis (SCP_TEST)*

In the safety critical designs, short-circuit protection (SCP) feature and its diagnosis is important.

The TPS48000-Q1 features the diagnosis of the internal short circuit protection. When SCP_TEST is driven low to high then, a voltage is applied internally across the SCP comparator inputs to simulate a short circuit event. The comparator output controls the gate drive (PU/PD) and also the $\overline{\text{FLT}}$. If the gate drive goes low (with initially being high) and $\overline{\text{FLT}}$ alos goes low then it indicates that the SCP is good otherwise it is to be treated as SCP feature is not functional.

If the SCP_TEST feature is not used, then connect SCP_TEST pin to GND.

### *7.3.7 TPS48000-Q1 as a Simple Gate Driver*

Figure 7-12 shows application schematics of TPS48000-Q1 as a simple gate driver in load disconnect switch as well as back-to-back FETs driving topologies. The short-circuit protection feature is disabled.

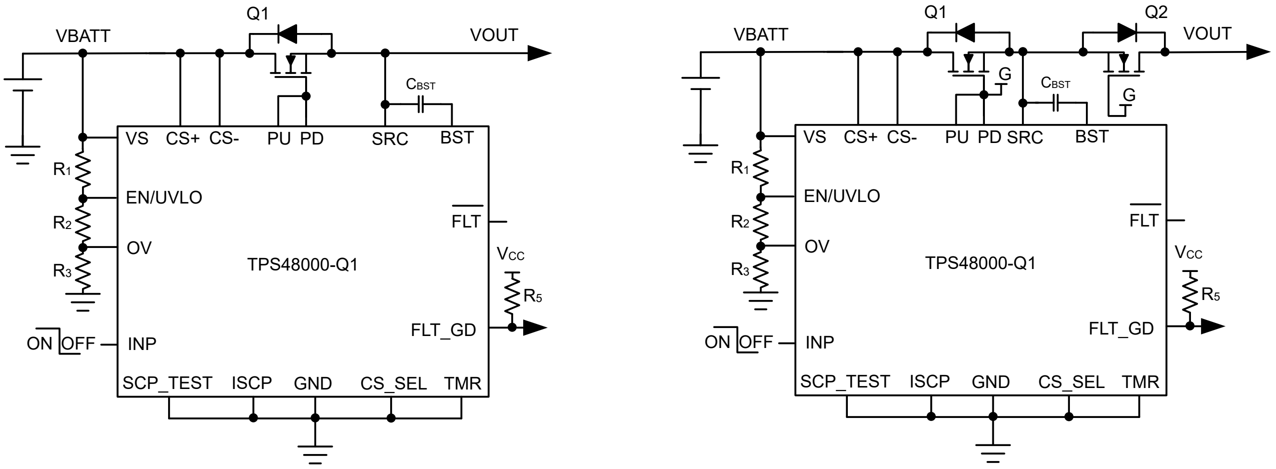


**Figure 7-12. TPS48000-Q1 Application Circuit for Simple Gate Driver Design**

## 7.4 Device Functional Modes

The TPS48000-Q1 has two modes of operation. Active mode and low IQ shutdown mode.

If the EN/UVLO pin voltage is greater than $V_{(ENR)}$ rising threshold, then the device is in active mode. In active state the internal charge pump is enabled, gate drivers, all the protection and diagnostic features are enabled.

If the EN/UVLO voltage is pulled below $V_{(ENF)}$ falling threshold, the device enters into low IQ shutdown mode. In this mode, the charge pump, gate drivers and all the protection features are disabled. The gate drive and external FETs turn OFF. The TPS48000-Q1 consumes low IQ of 1 µA (typical) in this mode.

# 8 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TPS48000-Q1 is a 100V low IQ smart high side driver with protection and diagnostics. With wide operating voltage range of 3.5 V–95V, the device is suitable for 12V, 24V and 48V system designs. The device can withstand and protect the loads from negative supply voltages down to –65V. It has strong 1.69A/2A peak source/sink gate driver enabling power switching using parallel FETs in high current system designs.

The device provides configurable short circuit protection using ISCP and TMR pins for adjusting the threshold and response time respectively. Auto-retry and latch-off fault behavior can be configured. With TPS48000-Q1, current sensing can be done either by an external sense resistor or by MOSFET VDS sensing. High or low side current sense resistor configuration is possible by using CS_SEL pin input.

Diagnosis of the integrated short circuit comparator can be done using external control on SCP_TEST input.The device indicates fault ($\overline{\text{FLT}}$) on open drain output during during short circuit and input under voltage, overvoltage conditions. It also have a dedicate fault indication (FLT_GD) to indicate the gate drive UVLO condition.

Low Quiescent Current 46µA operation enables always ON system designs. Quiescent current reduces to 1µA (typical) with EN/UVLO low.

## 8.2 Typical Application: Driving Power at all Times (PAAT) Loads

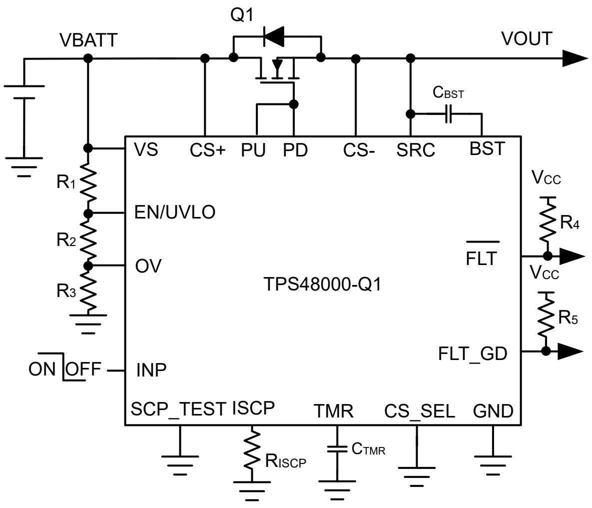


Figure 8-1. TPS48000-Q1 Application Circuit for driving PAAT loads with VDS based Current Sensing

### *8.2.1 Design Requirements*

Table 8-1. Design Parameters

| PARAMETER | VALUE |
|---|---|
| Input Voltage Range, $V_{IN}$ | 16 to 60V |

### Table 8-1. Design Parameters (continued)

| PARAMETER | VALUE |
|---|---|
| Undervoltage lockout set point, $VIN_{UVLO}$ | 16V |
| Overvoltage set point, $VIN_{OVP}$ | 60V |
| Maximum load current, $I_{OUT}$ | 20A |
| Short-circuit protection threshold, $I_{SC}$ | 60A |
| Fault timer period, $t_{SC}$ | 50µs |
| Fault response | Auto-Retry |
| Current sensing | MOSFET VDS |

#### 8.2.2 Detailed Design Procedure

##### Selection of MOSFET, $Q_1$

For selecting the MOSFET $Q_1$, important electrical parameters are the maximum continuous drain current $I_D$, the maximum drain-to-source voltage $V_{DS(MAX)}$, the maximum drain-to-source voltage $V_{GS(MAX)}$, and the drain-to-source ON resistance $R_{DSON}$.

The maximum continuous drain current, $I_D$, rating must exceed the maximum continuous load current.

The maximum drain-to-source voltage, $V_{DS(MAX)}$, must be high enough to withstand the highest voltage seen in the application. Considering 60V as the maximum application voltage due to load dump, MOSFETs with $V_{DS}$ voltage rating of 80V is chosen for this application.

The maximum $V_{GS}$ TPS48000-Q1 can drive is 11V, so a MOSFET with 15V minimum $V_{GS}$ rating must be selected.

To reduce the MOSFET conduction losses, an appropriate $R_{DS(ON)}$ is preferred.

Based on the design requirements, IAUS200N08S5N023 is selected and its ratings are:

- 80V $V_{DS(MAX)}$ and ±20V $V_{GS(MAX)}$
- $R_{DS(ON)}$ is 2.3mΩ typical at 10V $V_{GS}$
- MOSFET $Q_{g(total)}$ is 85nC typical

TI recommends to make sure that the short-circuit conditions such max $V_{IN}$ and $I_{SC}$ are within SOA of selected FET ($Q_1$) for at-least > $t_{SC}$ timing.

##### Selection of Bootstrap Capacitor, $C_{BST}$

The internal charge pump charges the external bootstrap capacitor (connected between BST and SRC pins) with approximately 345µA. Use the following equation to calculate the minimum required value of the bootstrap capacitor for driving IAUS200N08S5N023 MOSFET

$$C_{BST} = \frac{Q_{g(total)}}{1\ \mathrm{V}} = 85\ \mathrm{nF} \tag{9}$$

Choose closest available standard value: 100nF, 10%.

##### Programming the Short-Circuit Protection Threshold – $R_{ISCP}$ Selection

The $R_{ISCP}$ sets the short-circuit protection threshold, whose value can be calculated using below equation:

$$R_{ISCP}\left(\Omega\right) = \frac{\left(I_{SC} \times R_{DS\_ON} - 19\ \mathrm{mV}\right)}{2\ \mu\mathrm{A}} \tag{10}$$

To set 60 A as short-circuit protection threshold, $R_{ISCP}$ value is calculated to be 50.5kΩ.

Choose the closest available standard value: 51kΩ, 1%.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor ($R_{SNS}$) and tweak the values during test in the real system. The RC filter components should not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

### Programming the Fault timer Period – $C_{TMR}$ Selection

For the design example under discussion, overcurrent transients are allowed for 50µs duration. This blanking interval, $t_{SC}$ (or circuit breaker interval, $T_{CB}$) can be set by selecting appropriate capacitor $C_{TMR}$ from TMR pin to ground. The value of $C_{TMR}$ to set 50µs for $t_{SC}$ can be calculated using following equation:

$$C_{TMR} = \frac{87\ \mu A \times t_{SC}}{1.1} \tag{11}$$

Choose closest available standard value: 3.3nF, 10%.

### Setting the Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage set point are adjusted using an external voltage divider network of $R_1$, $R_2$ and $R_3$ connected between VS, EN/UVLO, OV and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 12 and Equation 13.

$$V_{(OVR)} = \frac{R_3}{(R_1 + R_2 + R_3)} \times VIN_{OVP} \tag{12}$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{(R_1 + R_2 + R_3)} \times VIN_{UVLO} \tag{13}$$

For minimizing the input current drawn from the power supply, TI recommends to use higher values of resistance for $R_1$, $R_2$ and $R_3$. However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20 times greater than the leakage current of UVLO and OV pins.

From the device electrical specifications, $V_{(OVR)}$ = 1.225V and $V_{(UVLOR)}$ = 1.23V. From the design requirements, $VIN_{OVP}$ is 60V and $VIN_{UVLO}$ is 16V. To solve the equation, first choose the value of $R_1$ = 470kΩ and use Equation 12 to solve for ($R_2$ + $R_3$) = 39.1+470kΩ. Use Equation 13 and value of ($R_2$ + $R_3$) to solve for $R_3$ = 10.4kΩ and finally $R_2$ = 28.7kΩ. Choose the closest standard 1% resistor values: $R_1$ = 470kΩ, $R_2$ = 29.4kΩ, and $R_3$ = 10kΩ.

### 8.2.3 Application Curves

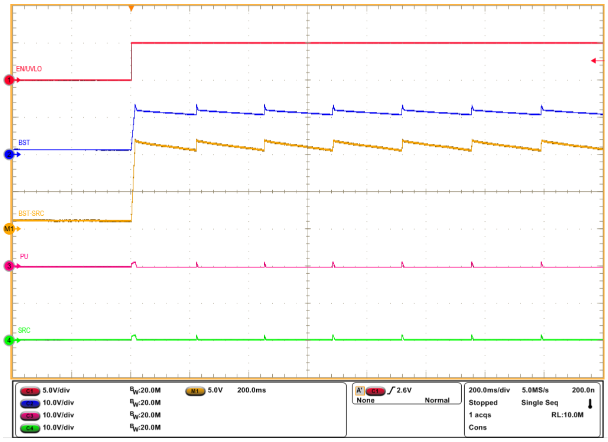


Figure 8-2. Start-Up Profile of Bootstrap Voltage with INP = GND and $C_{BST}$ = 470nF

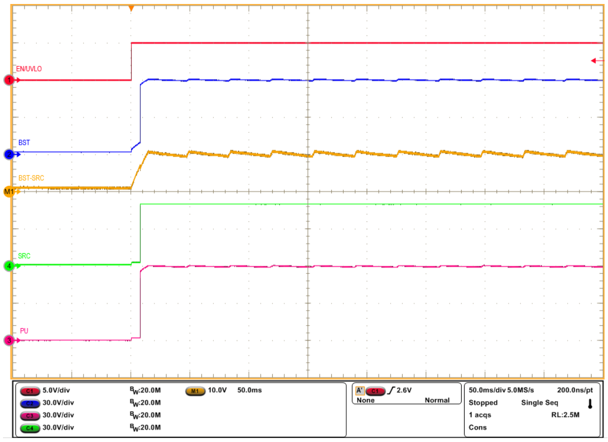


Figure 8-3. Start-Up Profile of Bootstrap Voltage with INP = HIGH and $C_{BST}$ = 470nF

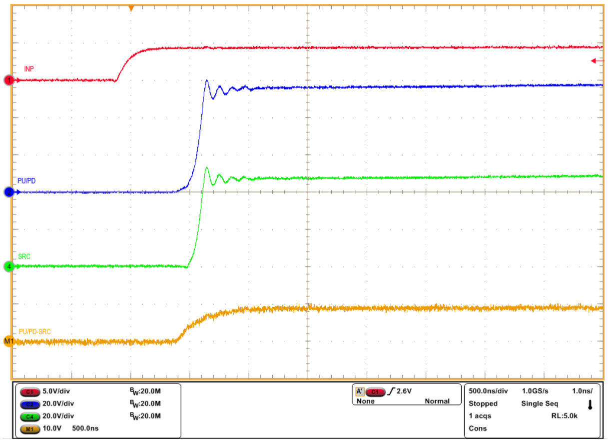


Figure 8-4. Turn-ON Response of TPS48000-Q1 for INP -> LOW to HIGH and $C_{BST}$ = 470nF

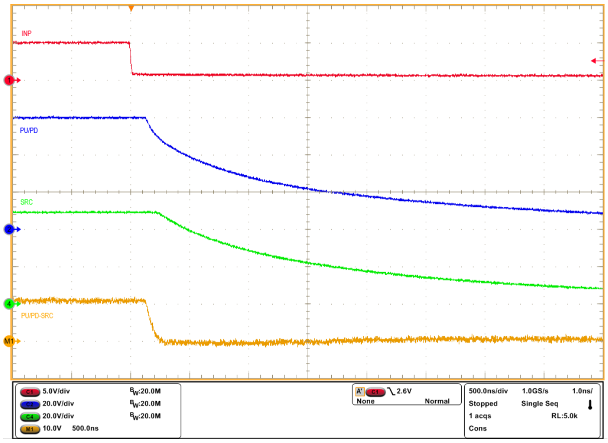


Figure 8-5. Turn-OFF Response of TPS48000-Q1 for INP -> HIGH to LOW and $C_{BST}$ = 470nF

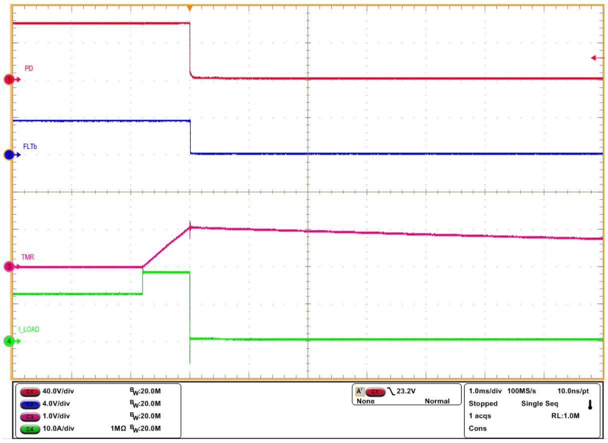


Figure 8-6. Overcurrent Response of TPS48000-Q1 for a Load Step from 12A to 18A with 15A Shortcircuit Protection Setting and $t_{sc}$ = 1ms

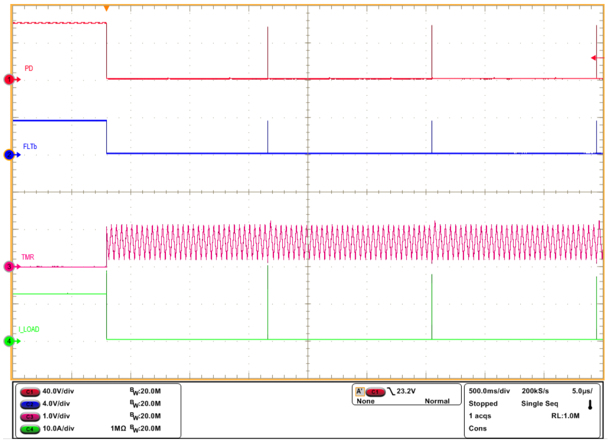


Figure 8-7. Auto-Retry Response of TPS48000-Q1 for an Overcurrent Fault

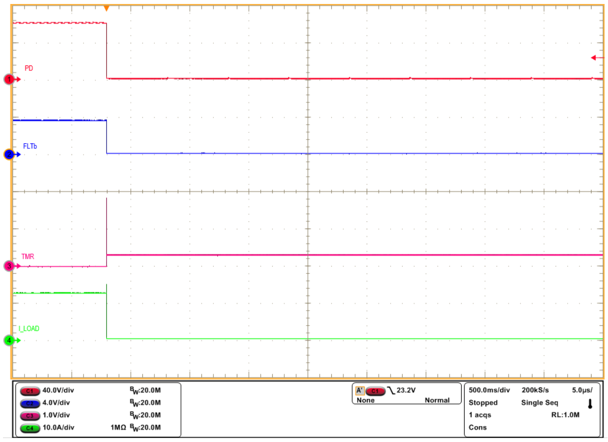


Figure 8-8. Latch-Off Response of TPS48000-Q1 for an Overcurrent Fault

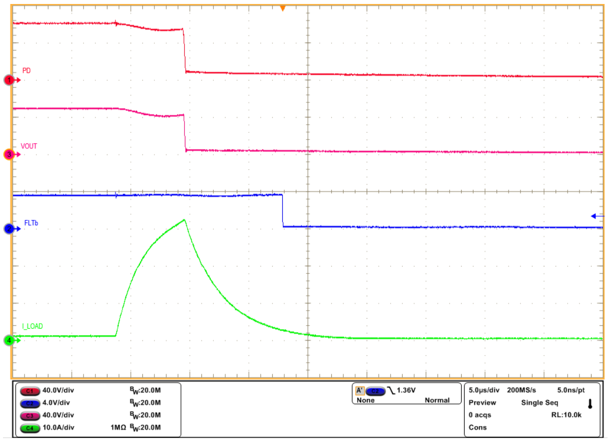


Figure 8-9. Output Short-Circuit Response of TPS48000-Q1 Device with 15A Shortcircuit Protection Setting and TMR = OPEN

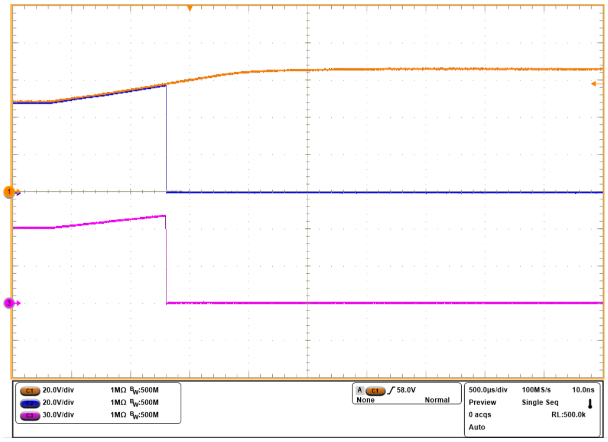


Figure 8-10. Overvoltage Cutoff Response of TPS48000-Q1 at 58V Level

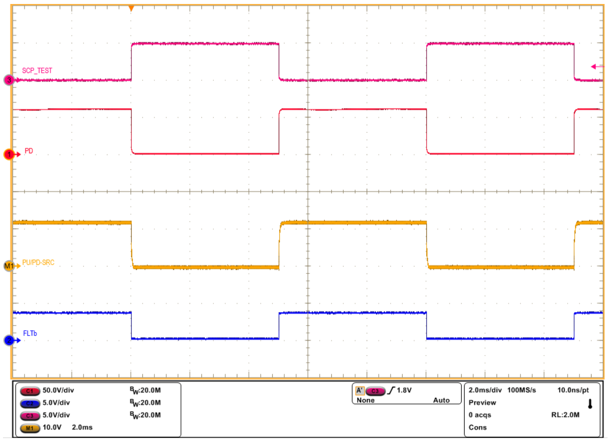


Figure 8-11. Short-Circuit Protection Diagnosis Test Response of TPS48000-Q1

## 8.3 Power Supply Recommendations

When the external MOSFETs turn-OFF during the conditions such as INP1 control, overcurrent protection causing an interruption of the current flow, the input parasitic line inductance generates a positive voltage spike on the input and output parasitic inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Use of a TVS diode and input capacitor filter combination across input to and GND to absorb the energy and dampen the positive transients.
- Use of a diode or a TVS diode across the output and GND to absorb negative spikes.

The TPS48000-Q1 gets powered from the VS pin. Voltage at this pin must be maintained above $V_{(VS\_PORR)}$ level to ensure proper operation. If the input power supply source is noisy with transients, then TI recommends to place a $R_{VS}$ – $C_{VS}$ filter between the input supply line and VS pin to filter out the supply noise. TI recommends $R_{VS}$ value around 100Ω.

In case where large di/dt is involved, the system and layout parasitic inductances can generate large differential signal voltages between CS+ and CS– pins. This action can trigger false short-circuit protection and nuisance trips in the system. To overcome such scenario, TI suggests to add placeholder for RC filter components across sense resistor ($R_{SNS}$) and tweak the values during test in the real system. The RC filter components must not be used in current sense designs by MOSFET VDS sensing to avoid impact on the short-circuit protection response.

The following figure shows the circuit implementation with optional protection components.

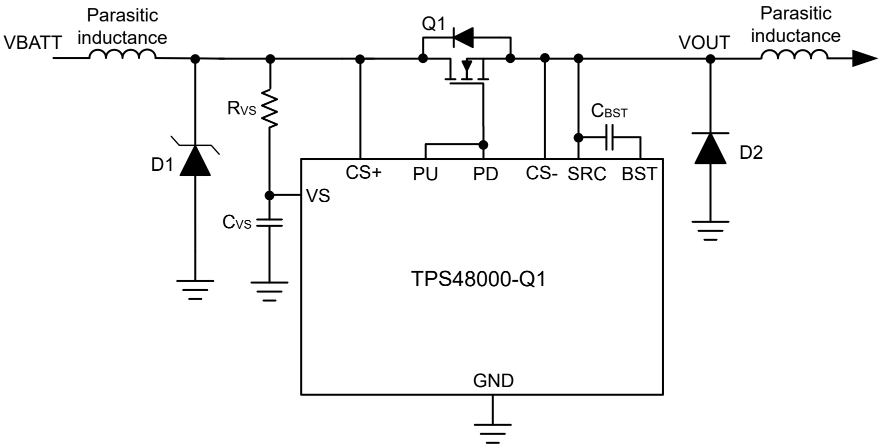


**Figure 8-12. Circuit Implementation With Optional Protection Components For TPS48000-Q1**

## 8.4 Layout

### *8.4.1 Layout Guidelines*

- Place the sense resistor ($R_{SNS}$) close to the TPS48000-Q1 and then connect $R_{SNS}$ using the Kelvin techniques. Refer to *Choosing the Right Sense Resistor Layout* for more information on the Kelvin techniques.

  For VDS based Current Sensing, follow the same kevlin techniques across the MOSFET.
- Choose a 0.1 µF or higher value ceramic decoupling capacitor between VS terminal and GND for all the applications. Consider adding RC network at the supply pin (VS) of the controller to improve decoupling against the power line disturbances.
- Make the high-current path from the board input to the load, and the return path, parallel and close to each other to minimize loop inductance.
- Place the external MOSFETs close to the controller GATE drive pins (PU/PD) such that the GATE of the MOSFETs are close to the controller GATE drive pins and forms a shorter GATE loop. Consider adding a place holder for a resistor in series with the Gate of each external MOSFET to damp high frequency oscillations if need arises.
- Place a TVS diode at the input to clamp the voltage transients during hot-plug and fast turn-off events.
- Place the external boot-strap capacitor close to BST and SRC pins to form very short loop.
- Connect the ground connections for the various components around the TPS48000-Q1 directly to each other, and to the TPS48000-Q1 GND, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high current ground line.

### 8.4.2 Layout Example

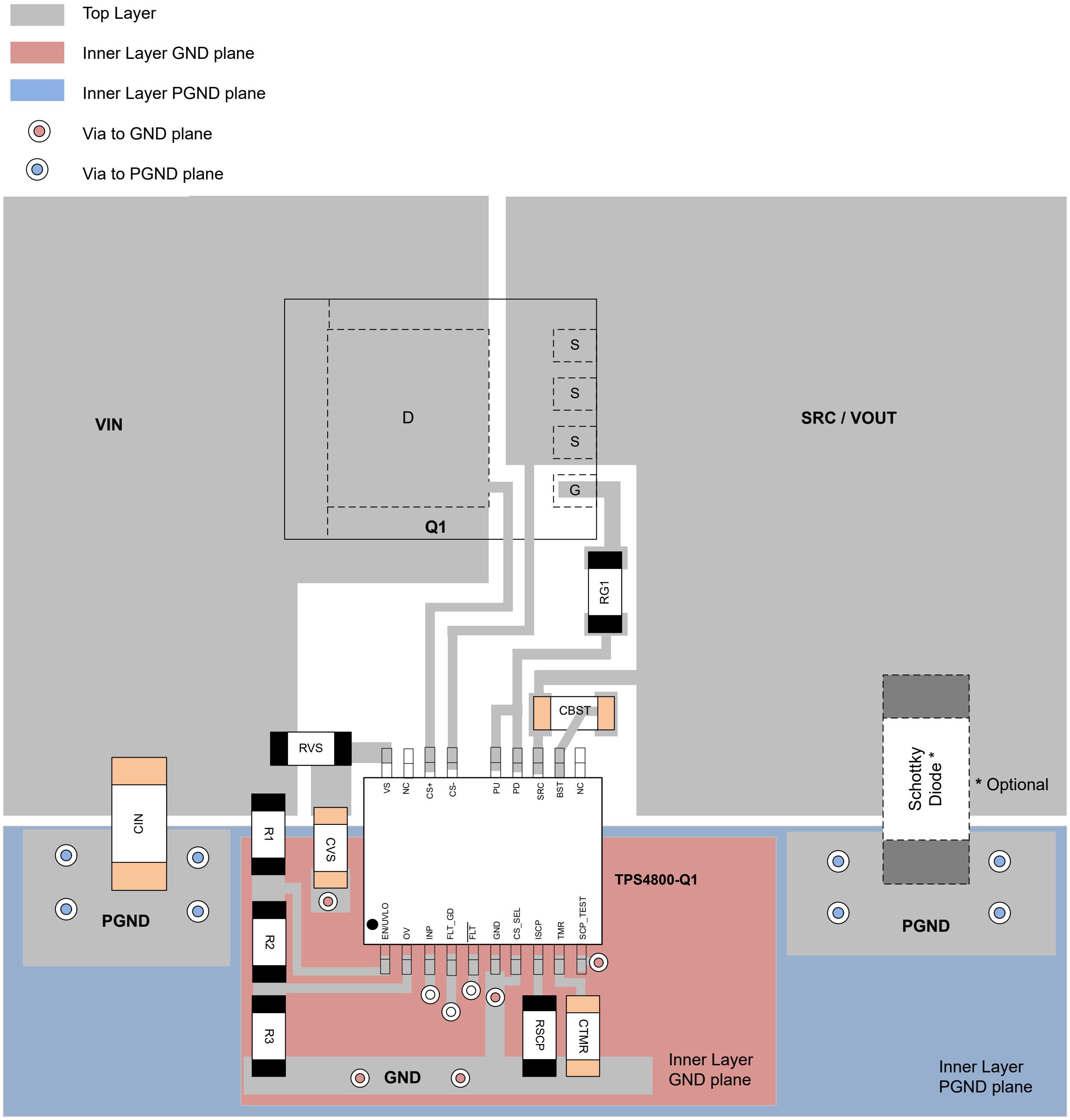


Figure 8-13. Typical PCB Layout Example for TPS48000-Q1 With VDS based Current Sensing

# 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.3 Trademarks

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## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (December 2024) to Revision B (March 2026) Page**

- Change MIN from 1.78V to 1.7V and MAX from 3.27V to 3.34V.......... 6
- Change MIN from 1.71V to 1.7V and MAX from 3.1V to 3.16V.......... 6
- Changed MAX from 55μA to 56μA.......... 6
- Changed TYP from 0.75μA to 1μA and MAX from 3.3μA to 4.3μA.......... 6
- Changed MIN from 19μA to 15μA, TYP from 22.1μA to 22.4μA and MAX from 37μA to 38μA.......... 6
- Changed MIN from 1.176V to 1.17V and MAX from 1.287V to 1.29V.......... 6
- Changed TYP from 1.136V to 1.14V and MAX from 1.184V to 1.19V.......... 6
- Changed MAX from 478nA to 490nA.......... 6
- Changed MAX from 700nA to 730nA.......... 6
- Changed MIN from 1.171V to 1.17V, TYP from 1.225V to 1.23V and MAX from 1.278V to 1.28V.......... 6
- Changed MIN from 1.088V to 1.08V, TYP from 1.138V to 1.14V and MAX from 1.186V to 1.19V.......... 6
- Changed MAX from 200nA to 205nA.......... 6
- Changed MIN from 190μA to 100μA and MAX from 466μA to 555μA.......... 6
- Changed MIN from 8.1V to 7.19V and MAX from 9.9V to 10.81V.......... 6
- Changed MIN from 7.28V to 6.54V and MAX from 8.9V to 9.64V.......... 6
- Changed MIN from 9.3V to 8.24V and MAX from 11.4V to 12.46V.......... 6
- Changed MIN from 9.34V to 9.3V and MAX from 12.8V to 13.86V.......... 6
- Changed MIN from 9.1V to 8.9V and MAX from 11.62V to 11.82V.......... 6
- Changed MIN from 5.5V to 5.32V and MAX from 8.3V to 8.48V.......... 6
- Changed MIN from 8.4μA to 8.22μA and MAX from 12.33μA to 12.51A.......... 6
- Added MIN and MAX value.......... 6
- Changed MIN from 60mV to 58.4mV and MAX from 90mV to 91.6mV.......... 6

- Changed MIN from 32mV to 31.1mV and MAX from 48mV to 48.9mV.................................................. 6
- Changed MIN from 15mV to 14.9mV and MAX from 25mV to 25.2mV.................................................. 6
- Added MIN, TYP values and Changed MAX from 757mV to 651mV.................................................. 6
- New Line item.................................................. 6
- Changed MIN from 283mV to 279mV and MAX from 315mV to 319mV.................................................. 6
- Changed MIN from 67.8mV to 67mV and MAX from 81.7mV to 83mV.................................................. 6
- Changed MIN from 33.3mV to 33mV and MAX from 46.2mV to 47mV.................................................. 6
- Changed MIN from 67µA to 65µA and MAX from 104µA to 106µA.................................................. 6
- Changed MIN from 1.4µA to 1.33µA and MAX from 3.8µA to 3.87µA .................................................. 6
- Changed MIN from 2.17µA to 2.14µA and MAX from 3.4µA to 3.43µA .................................................. 6
- Changed MIN from 0.93V to 0.87V and MAX from 1.2V to 1.26V.................................................. 6
- Changed MIN from 0.15V to 0.14V and MAX from 0.25V to 0.26V.................................................. 6
- Changed MIN from 53Ω to 52Ω.................................................. 6
- Changed MAX from 206nA to 210nA.................................................. 6
- Changed MIN from 1.35V to 1.25V and MAX from 2V to 1.58V .................................................. 6
- Changed MIN from 0.8V to 0.66V and MAX from 1.36V to 1.14V .................................................. 6
- Changed MAX from 200nA to 210nA.................................................. 6
- Changed MAX from 1.53µs to 1.68µs.................................................. 7
- Changed MAX from 1µs to 1.05µs.................................................. 7
- Changed MIN from 2.2µs to 1.68µs and MAX from 6µs to 6.52µs.................................................. 7
- Changed MIN from 2.8µs to 2.22µs and MAX from 6µs to 6.58µs.................................................. 7
- Changed MAX from 5.4µs to 5.55µs.................................................. 7

**Changes from Revision * (December 2023) to Revision A (December 2024)** **Page**

- Changed the document status From: *Advance Information* To: *Production Data* .................................................. 1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| PTPS48000QDGXRQ1 | Active | Preproduction | VSSOP (DGX) \| 19 | 5000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| PTPS48000QDGXRQ1.A | Active | Preproduction | VSSOP (DGX) \| 19 | 5000 \| LARGE T&R | - | Call TI | Call TI | -40 to 125 | |
| TPS48000QDGXRQ1 | Active | Production | VSSOP (DGX) \| 19 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4800 |
| TPS48000QDGXRQ1.A | Active | Production | VSSOP (DGX) \| 19 | 5000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 4800 |

[1] **Status:** For more details on status, see our product life cycle.

[2] **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

[3] **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

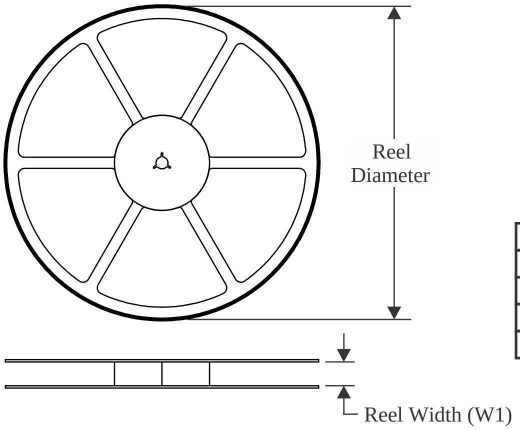
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

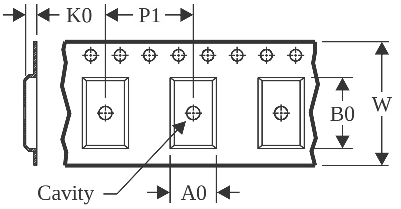
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

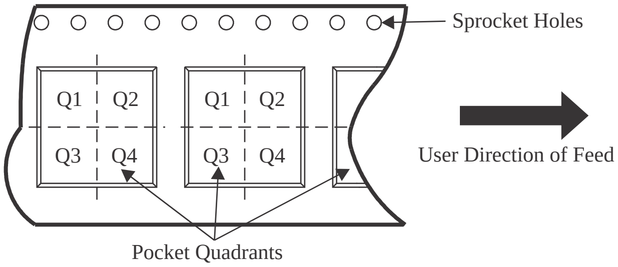


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

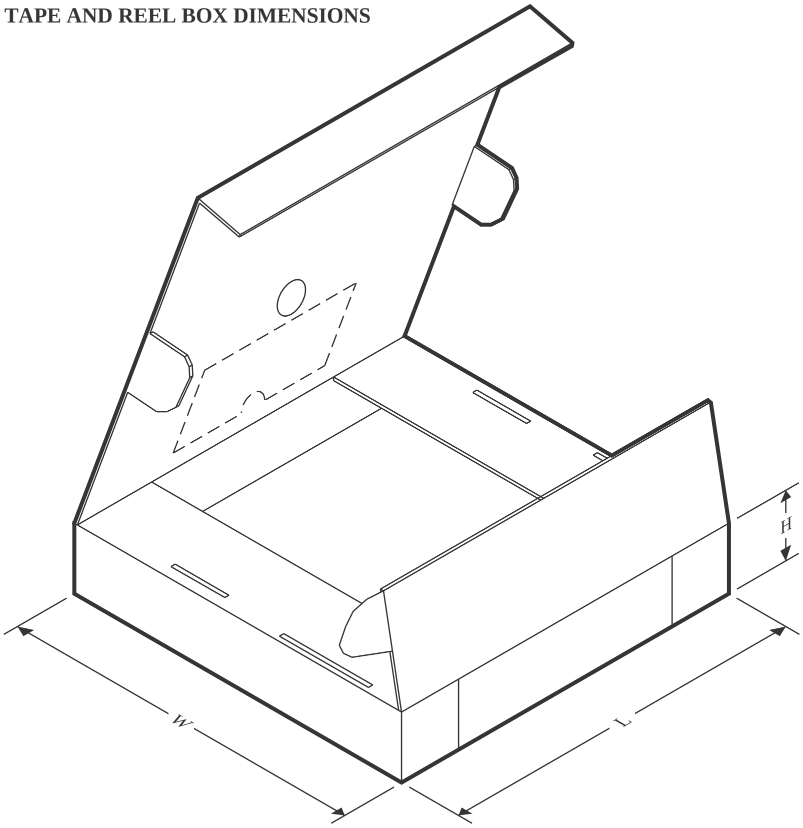
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

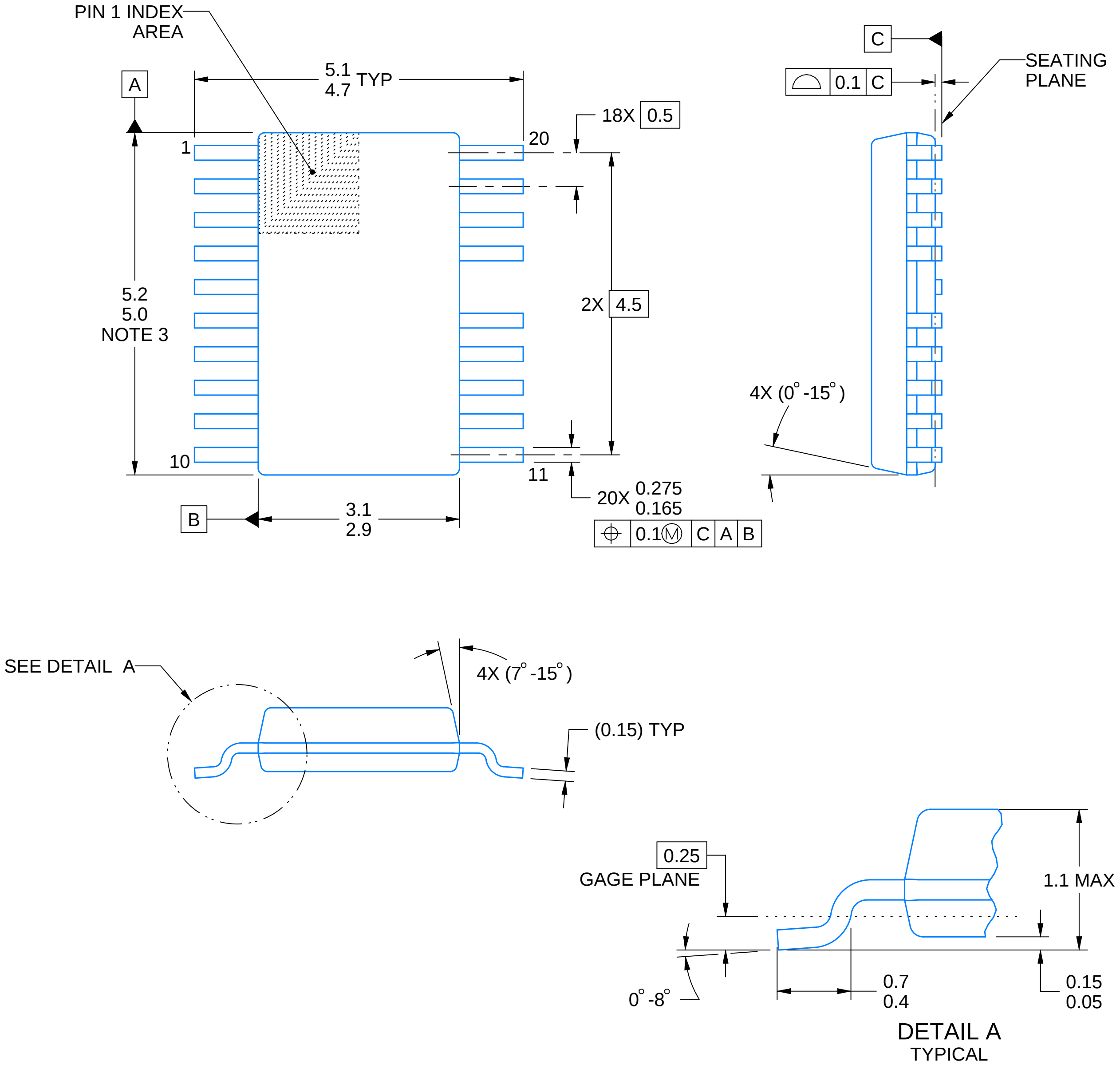
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS48000QDGXRQ1 | VSSOP | DGX | 19 | 5000 | 330.0 | 16.4 | 5.4 | 5.4 | 1.45 | 8.0 | 16.0 | Q1 |

### TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS48000QDGXRQ1 | VSSOP | DGX | 19 | 5000 | 353.0 | 353.0 | 32.0 |

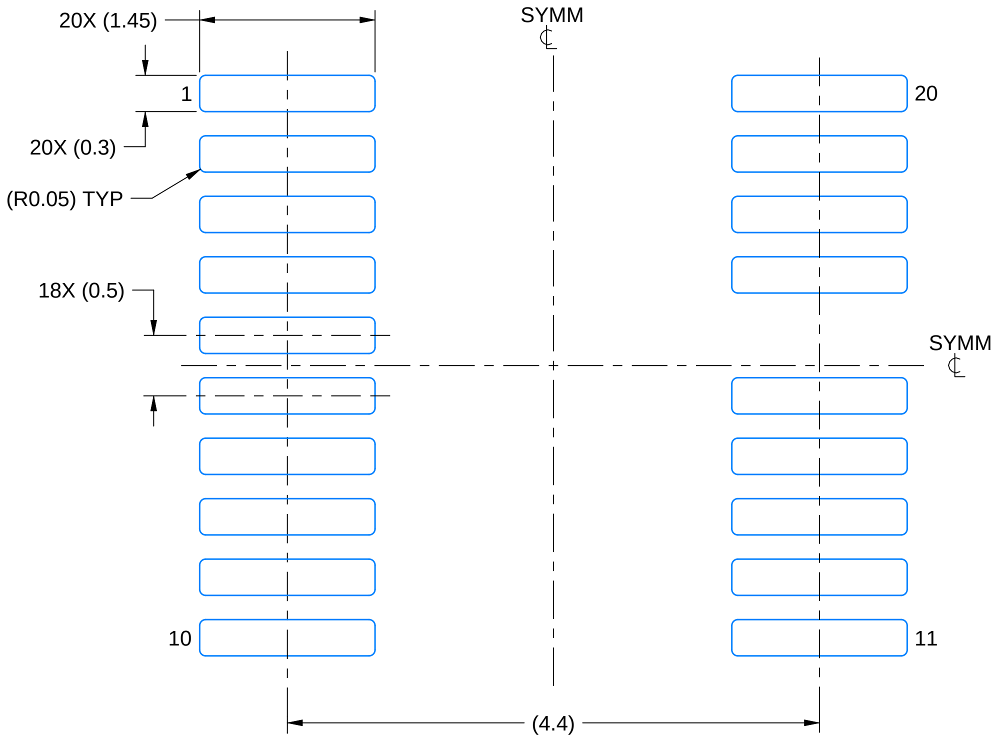


4226944/A 07/2021

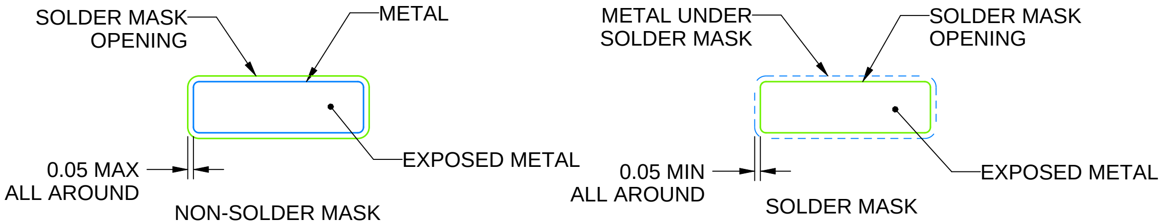
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of July 2021.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X



NON-SOLDER MASK DEFINED (PREFERRED)

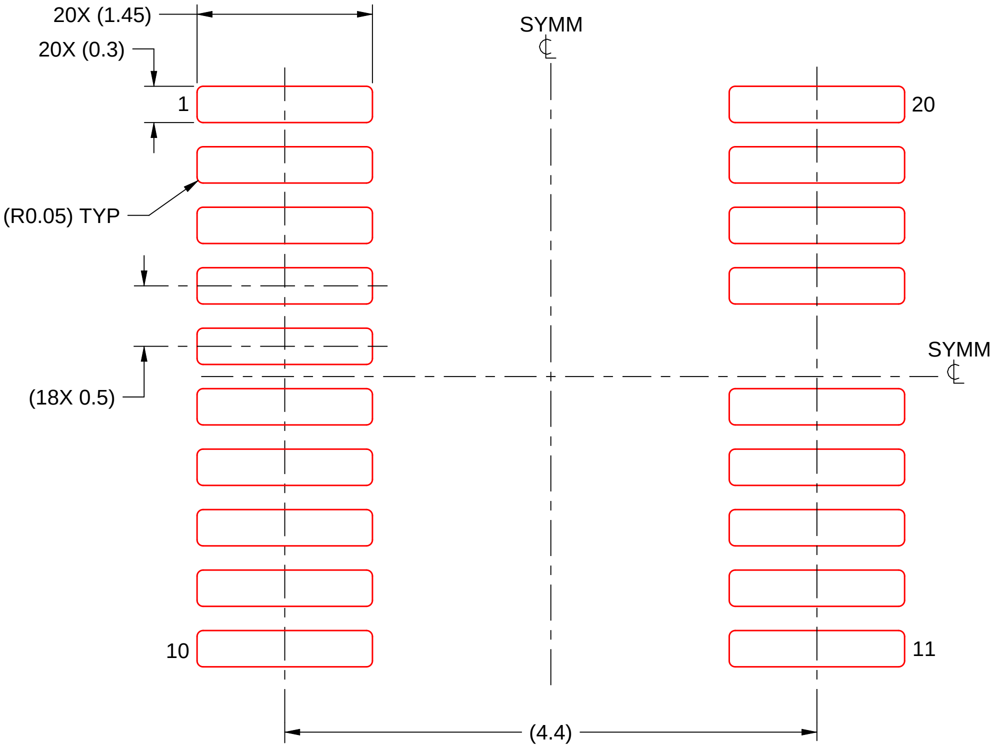
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4226944/A 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025