TPS481HS04-Q1 4mΩ, Automotive Single-Channel, SPI Controlled High-Side Switch with Integrated I^2t Wire Protection and Low Power Mode

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C
  - Withstands 70V load dump
- Single channel SPI controlled smart high-side switch with integrated nFET.
- Integrated wire-harness protection without MCU involvement and a SPI programmable fuse curve
  - Protection against persistent overload condition
- User programmable EEPROM
- Improve system level reliability through SPI programmable adjustable overcurrent protection
- SPI configurable capacitive charging mode to drive a wide range of capacitive input ECUs load current needs.
- Low quiescent current, low power ON-state to supply always-ON loads with automatic wake on load current increase with wake signal to MCU
- Robust integrated output protection:
  - Integrated thermal protection
  - Protection against short-to-ground
  - Protection against reverse battery events including automatic switch on of FET with reverse supply voltage
  - Automatic shut off on loss of battery and ground
  - Integrated output clamp to demagnetize inductive loads
- Digital sense output via SPI can be configured to measure:
  - Load current accurately with integrated ADC
  - Output or supply voltage, FET temperature
- Provides full fault diagnostics through SPI interface and indication through FLT pin
  - Detection of open load and short-to-battery

2 Applications

- Automotive zone ECU
- Power distribution modules
- Body control modules

3 Description

The TPS481HS04-Q1 device is a single channel, smart high-side switch controlled through a serial peripheral interface (SPI) and is intended for power distribution as well as actuator drive applications. The device integrates robust protection to ensure output wire and load protection against short circuit or overload conditions. The device features overcurrent protection which is configurable via SPI with sufficient flexibility to support loads that require large inrush currents, while providing improved protection. Further, the device integrates a programmable fuse profile (current versus time) that turns off the switch under persistent overload condition.

The device supports a SPI-configurable capacitive charging mode for ECU loads in power distribution switch applications. The device also includes two low power mode (LPM) states, an auto entry mode or a manual entry mode, that enables the device to provide current to the load ECU while only consuming about 10-20µA of current.

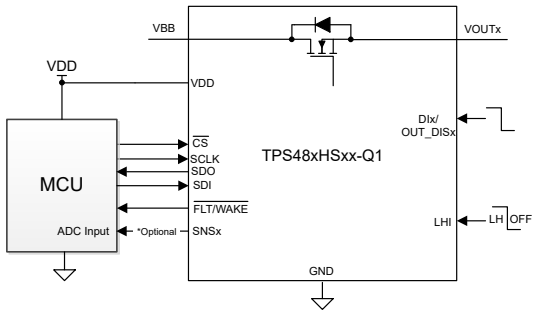
By reporting load current and the channel output voltage and output FET temperature to a system MCU, the device enables diagnosis of switch and load failures.

The TPS481HS04-Q1 is available in a QFN package which allows for reduced PCB footprint.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS481HS04-Q1	RBL (QFN, 21)	5.75mm x 5.5mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Circuit

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Pin Configuration and Functions

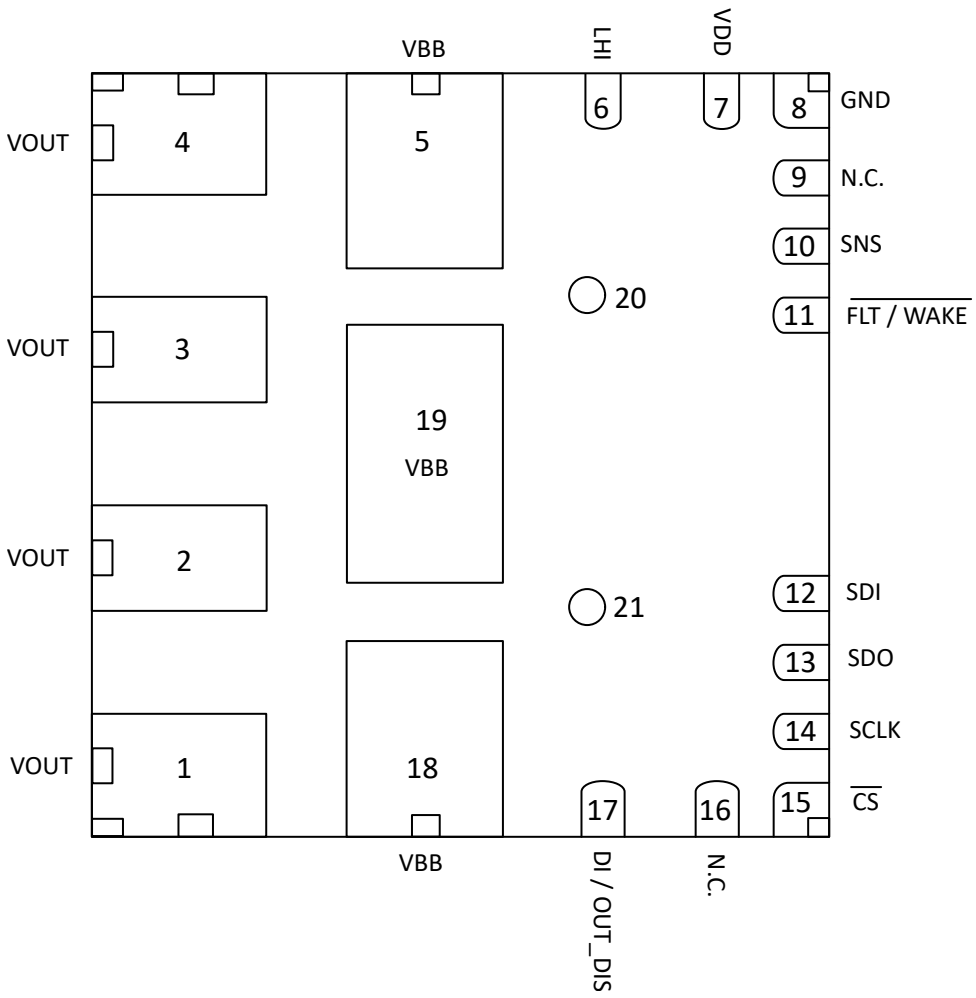


Figure 4-1. RBL Package, 21-Pin QFN-HR (Bottom View) - TPS481HS04-Q1

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1, 2, 3, 4	VOUT	O	High-side switch output, connect to load
5, 18, 19	VBB	Power	Power supply
6	LHI	I	Externally enables limp home mode.
7	VDD	Power	Logic supply input
8	GND	GND	Device ground
9, 16, 20, 21	NC	O	No connect
10	SNS	O	SNS current output, use a parallel RC network to the GND pin of the IC
11	$\overline{\text{FLT}}$ / $\overline{\text{WAKE}}$	O	Fault output – on any (one or more) channel - open drain, pull up with a 4.7K resistor to VDD pin. Also functions as a wake signal to the MCU upon load current demand in key-off mode.

ADVANCE INFORMATION

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
12	SDI	I	SPI device (secondary) data input
13	SDO	O	SPI Data Output from the device. Internally pulled up to VDD.
14	SCLK	I	SPI Clock input
15	CSN	I	Chip select. Internally pulled up to VDD
17	DI / OUT_DIS	I	Configurable through EEPROM through DI_OUT_DIS_FN bit. If programmed as **DI:** Sets the output behavior in the LIMP HOME mode, if configured through the CHx_LH_IN bits If programmed as **OUT_DIS:** Disables VOUTx if asserted high if OUT_DIS_MASK_CHx = 0. *The pin needs to be connected to MCU or other HI/LO source through a 10K resistor tor protection and enabling the reverse polarity FET turn-on function.*

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum transient voltage on VBB pin, V_{BBt}			70	V
Load dump voltage			70	V
VOUT voltage		–60	V_{BB}+0.7	V
Reverse polarity voltage, continuous on VBB pin		–36		V
Low voltage supply pin voltage, V_{DD}		–0.3	7	V
SPI digital input pin voltages, V_{SPI}	SDI, SCLK, $\overline{CS}$	–0.3	7	V
Serial data output pin voltage, V_{SDO}	SDO	–0.3	7	V
Sense pin voltage, V_{SNS}		–0.3	7	V
$\overline{FLT}$ / $\overline{WAKE}$ pin voltage		–0.3	7	V
Limp home activation pin voltage, V_{LHI}			V_{BB}	V
Limp home direct input pin voltage / Output Disable, $V_{DI\_OUT\_DIS}$		–0.3	7	V
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per AEC Q100-002 Classification Level H2	All pins including VBB and VOUTx	±2000	V
		Human-body model (HBM), per AEC Q100-002 Classification Level H3A(2)	VBB and VOUTx	±4000	
		Charged-device model (CDM), per AEC Q100-011 Classification Level C5	All pins	±750	

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.
(2) ESD strikes are with reference from the pin mentioned to GND

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{BB_NOM}	Nominal supply voltage		6	60	V
V_{BB_EXT}	Extended supply voltage		3	70	V
V_{DD}	Low voltage supply voltage		3.0	5.5	V
V_{SPI}	SPI digital input pin voltage (SCLK, SDI, CSN)		–0.3	5.5	V
V_{SDO}	SDO pin voltage	SDO pin voltage	–0.3	5.5	V
$V_{\overline{FLT}/\overline{WAKE\_SIG}}$	$\overline{FLT}$ / $\overline{WAKE\_SIG}$ pin voltage		–0.3	5.5	V
V_{SNS}	SNS pin voltage		–0.3	5.5	V
V_{LHI}	Limp home activation pin voltage, LHI		–0.3	V_{BB}	V
$V_{DI\_OUT\_DIS}$	Limp Home Direct pin input voltage (DI) / Output Disable pin input voltage (OUT_DIS)		–0.3	5.5	V

ADVANCE INFORMATION

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS481HS04-Q1 RBL 21 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24 (est.)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

5.5 Electrical Characteristics

VBB = 8V to 60V @ VDD = 3.0 V to 5.5 V, TJ = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
$V_{(VBB\_UVLO)}$	V_{BB} undervoltage lockout	UVLO_SET = 0x1	V_{BB} rising threshold		5.5		V
			V_{BB} falling threshold		4.5		V
		UVLO_SET = 0x7	V_{BB} rising threshold		17		V
			V_{BB} falling threshold		16		V
		UVLO_SET = 0xC	V_{BB} rising threshold		27		V
			V_{BB} falling threshold		26		V
		UVLO_SET = 0xF	V_{BB} rising threshold		33		V
			V_{BB} falling threshold		32		V
$V_{(VDD\_UVLOR)}$	VDD undervoltage lockout rising				2.9		V
$V_{(VDD\_UVLOF)}$	VDD undervoltage lockout falling				2.6		V
$I_{SLEEP,VBB}$	Sleep current (total device leakage including all MOSFET channels)	Device in SLEEP mode, V_{OUT} = 0V	T_J = 25°C		1		µA
$I_{SLEEP,VDD}$	Sleep current from VDD pin	V_{VDD} [char_not_recognized] 5.5V, device in SLEEP mode, V_{OUT} = 0V	T_J = 25°C		0.3		µA
$I_{OUT(OFF),SLEEP}$	Output leakage current (per channel)	V_{OUT} = 0V, Channel disabled, SLEEP state	T_J = 25°C		0.1		µA
$I_{Q,VDD}$	VDD quiescent current	ACTIVE state, SCLK off	V_{DD} = 5.5V		1.65		mA
			V_{DD} = 3.0V		70		µA

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

VBB = 8V to 60V @ VDD = 3.0 V to 5.5 V, TJ = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q,VBB,ACTIVE}$	V_{BB} quiescent current in ACTIVE state	Channel enabled, IOUTx = 0A, ADC disabled, ACTIVE state	V_{DD} = 5.5V		3.2		mA
		Channel enabled, IOUTx = 0A, ADC enabled, ACTIVE state	V_{DD} = 5.5V		3.3		mA
			V_{DD} = 3.0V		3.3		mA
		Channel enabled, IOUTx = 0A, ADC enabled, ACTIVE state	V_{DD} = 0V		3.3		mA
$I_{L,CONT}$	Continuous load current, per channel	One channel enabled, T_{AMB} = 85°C	T_{AMB} = 85°C		18.5		A
RON CHARACTERISTICS							
R_{ON_OL}	On-resistance, OL ON mode	8V ≤ VBB ≤ 60V, IOUTx = 200mA, OL_ON_EN_CHx = 1	T_J = 25°C		215		mΩ
R_{ON}	On-resistance	8V ≤ VBB ≤ 60V, IOUTx = 2A, OL_ON_EN_CHx = 0	T_J = 25°C		4.9		mΩ
CURRENT SENSE CHARACTERISTICS							
$I_{ENTRY\_OL\_ON}$	I_{OUT} current to enter OL_ON mode (OL_ON_EN_CHx = 1)	I_{OUT} current to enter OL_ON mode (OL_ON_EN_CHx = 1)			1		A
$I_{EXIT\_OL\_ON}$	I_{OUT} current to exit OL_ON mode (OL_ON_EN_CHx = 1)	I_{OUT} current to exit OL_ON mode (OL_ON_EN_CHx = 1)			1.36		A
K_{SNS1}	Current sense ratio I_{OUTx} / I_{SNS}	OL_ON_EN_CHx = 0			11450		
K_{SNS2}	Current sense ratio I_{OUTx} / I_{SNS}	OL_ON_EN_CHx = 1			267		
ADC CHARACTERISTICS							
K_{DIG1}	Current sense ratio I_{OUTx} / I_{SNS} for ADC	OL_ON_EN_CHx = 0			25.88		
K_{DIG2}	Current sense ratio I_{OUTx} / I_{SNS} for ADC	OL_ON_EN_CHx = 1			0.6		
V_{ADC_REF}	ADC reference voltage				2.8		V
I_{ADC}	ADC current consumption				0.5		mA
SNS CHARACTERISTICS							
VBB_{SNS_RANGE}	VBB SNS voltage sensing range			8		65	V
$VOUT_{SNS\_RANGE}$	VOUT SNS voltage sensing range			0		65	V
OVERCURRENT PROTECTION CHARACTERISTICS							
I_{OCP_RANGE}	Overcurrent protection threshold, immediate shutdown mode - range			18.5		74	A

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

VBB = 8V to 60V @ VDD = 3.0 V to 5.5 V, TJ = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OCP}	Overcurrent protection threshold, immediate shutdown mode		ILIMIT_SET_CHx = 0x0		18.5		A
			ILIMIT_SET_CHx = 0x1		22.2		A
			ILIMIT_SET_CHx = 0x2		25.9		A
			ILIMIT_SET_CHx = 0x3		29.6		A
			ILIMIT_SET_CHx = 0x4		33.3		A
			ILIMIT_SET_CHx = 0x5		37		A
			ILIMIT_SET_CHx = 0x6		40.7		A
			ILIMIT_SET_CHx = 0x7		44.4		A
			ILIMIT_SET_CHx = 0x8		48.1		A
			ILIMIT_SET_CHx = 0x9		51.8		A
			ILIMIT_SET_CHx = 0xA		55.5		A
			ILIMIT_SET_CHx = 0xB		59.2		A
			ILIMIT_SET_CHx = 0xC		62.9		A
			ILIMIT_SET_CHx = 0xD		66.6		A
			ILIMIT_SET_CHx = 0xE		70.3		A
			ILIMIT_SET_CHx = 0xF		74		A
t_{OCP_DETECT}	Immediate shutdown detection time	From I_{OUT} = I_{OCP} to I_{OCP} detection R_{OUT} = 150% of I_{OCP} , L_{IN} = 0nH, L_{OUT} = 0nH			1		us
t_{OCP_TOFF}	Immediate shutdown turn off time	From I_{OCP} detection to 10% of V_{OUTx} R_{OUT} = 150% of I_{OCP} , L_{IN} = 0nH, L_{OUT} = 0nH			3		us
CAP CHARGING							
t_{INRUSH_RANGE}	Inrush duration settings range	INRUSH_DURATION_CHx range		0		100	ms

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

VBB = 8V to 60V @ VDD = 3.0 V to 5.5 V, TJ = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CL_Reg}	Current limit regulation mode		INRUSH_LIMIT_CHx = 0x0		1.75		A
			INRUSH_LIMIT_CHx = 0x1		2.38		A
			INRUSH_LIMIT_CHx = 0x2		2.75		A
			INRUSH_LIMIT_CHx = 0x3		3.13		A
			INRUSH_LIMIT_CHx = 0x4		3.50		A
			INRUSH_LIMIT_CHx = 0x5		3.88		A
			INRUSH_LIMIT_CHx = 0x6		4.25		A
			INRUSH_LIMIT_CHx = 0x7		4.63		A
			INRUSH_LIMIT_CHx = 0x8		5.00		A
			INRUSH_LIMIT_CHx = 0x9		5.38		A
			INRUSH_LIMIT_CHx = 0xA		6.35		A
			INRUSH_LIMIT_CHx = 0xB		6.8		A
			INRUSH_LIMIT_CHx = 0xC		7.25		A
			INRUSH_LIMIT_CHx = 0xD		7.7		A
			INRUSH_LIMIT_CHx = 0xE		8.1		A
			INRUSH_LIMIT_CHx = 0xF		8.6		A
CAPACITIVE CHARGING							
FAULT CHARACTERISTICS							
$I_{CHx(OL\_PU)}$	Off state open-load (OL) detection internal pull-up current	Switch disabled, OL_OFF_EN_CHx = enabled	OL_PULLUP_STR=00		25		µA
			OL_PULLUP_STR=01		57		µA
			OL_PULLUP_STR=10		121		µA
			OL_PULLUP_STR=11		256		µA
$I_{CHx(SHRT\_VBB)}$	Off state short to VBB detection pulldown current	Channel disabled, off-state short_VBB diagnostics enabled			6		mA
$V_{DS\_LT\_2V}$	VDS threshold during inrush duration				2		V
$V_{CHx(STB\_OL\_TH)}$	Off state Open-load (OL) and short to battery detection voltage	Channel Disabled, off-state open load or short to battery diagnostics enabled, VOUTx			2		V
T_{ABS}	Thermal shutdown				188		°C
T_{OTW}	Thermal shutdown warning				135		°C
T_{REL}	Relative thermal shutdown temperature				60		°C
T_{HYS}	Thermal shutdown hysteresis				25		°C

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

VBB = 8V to 60V @ VDD = 3.0 V to 5.5 V, TJ = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{RETRY}	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown or I_{OCP}) RETRY_TIME bit			1		ms
					10		
					0.15		
					100		
$t_{LPM\_WAKE\_DEGLITCH}$	Deglitch time to signal FLT/ WAKE after AUTO LPM exit				1		ms
					10		
					20		
					100		
TIMING CHARACTERISTICS							
PWM_{FREQ}	PWM Frequency	PWM_EN_CHx = 1	PWM_FREQ_CHx = 000		0.8		Hz
			PWM_FREQ_CHx = 001		3.2		Hz
			PWM_FREQ_CHx = 010		12.7		Hz
			PWM_FREQ_CHx = 011		100		Hz
			PWM_FREQ_CHx = 100		200		Hz
			PWM_FREQ_CHx = 101		400		Hz
			PWM_FREQ_CHx = 110		816		Hz
			PWM_FREQ_CHx = 111		1650		Hz
LOW POWER MODE CHARACTERISTICS							
$I_{CHx(LWUx)}$	IOUTx current to exit LPM, LPM_MODE = 0		LPM_EXIT_CURR_CHx = 00		0.23		A
			LPM_EXIT_CURR_CHx = 01		0.47		A
			LPM_EXIT_CURR_CHx = 10		0.7		A
			LPM_EXIT_CURR_CHx = 11		0.93		A
$I_{EXIT\_LPM\_AUTO}$	IOUTx current to exit LPM, LPM_MODE = 1		LPM_EXIT_CURR_CHx = 00		1.66		A
			LPM_EXIT_CURR_CHx = 01		2.77		A
			LPM_EXIT_CURR_CHx = 10		3.88		A
			LPM_EXIT_CURR_CHx = 11		5		A
$I_{Q,VDD,LPM}$	VDD quiescent current in MANUAL_LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, LPM_MODE = 0	Channel off		10		µA
			Channel ON		10		
		V_{DD} = 5.0V, I_{OUTx} = 0A, LPM_MODE = 1	Channel off		15		µA
			Channel ON		15		

ADVANCE INFORMATION

5.5 Electrical Characteristics (continued)

VBB = 8V to 60V @ VDD = 3.0 V to 5.5 V, TJ = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{Q,VBB,LPM}$	VBB quiescent current in LPM	V_{DD} = 5.0V, I_{OUTx} = 0A, LPM_MODE = 0	Channel off		10		µA
			Channel ON		10		
		V_{DD} = 5.0V, I_{OUTx} = 0A, LPM_MODE = 1	Channel off		15		µA
			Channel ON		15		
DIGITAL INPUT PIN CHARACTERISTICS							
$V_{IH,SPI}$	Input voltage high-level (SCLK, SDI, CSN)	3.0V ≤ VDD ≤ 5.5V	3.0V ≤ VDD ≤ 5.5V	0.7 x V_{VDD}			V
$V_{IL,SPI}$	Input voltage low-level (SCLK, SDI, CSN)	3.0V ≤ VDD ≤ 5.5V	3.0V ≤ VDD ≤ 5.5V			0.3 x V_{VDD}	V
$R_{PD,SCLK}$	SCLK Internal pulldown resistor				2		MΩ
$I_{IH,\ SCLK}$	Input current high-level	SCLK V_{SCLK} = 5V	V_{SCLK} = 5V		2.5		µA
$I_{IL,SCLK}$	Input current low-level	V_{SCLK} = 0.8V	V_{SCLK} = 0.8V		0.4		µA
$R_{PD,SDI}$	SDI Internal pulldown resistor				2		MΩ
$I_{IH,\ SDI}$	Input current high-level	SDI	V_{SDI} = 5V		2.5		µA
$I_{IL,SDI}$	Input current low-level	V_{SDI} = 0.8V	V_{SDI} = 0.8V		0.4		µA
$R_{PU,CSN}$	CSN Internal pullup resistor				100		kΩ
V_{IH,DI_OUT_DISx}, $V_{IH,LHI}$	LHI and DI/OUT_DISx input voltage high-level			1			V
V_{IL,DI_OUT_DISx}, $V_{IL,LHI}$	LHI and DI/OUT_DISx input voltage low-level					1.5	V
R_{PD,DI_OUT_DISx}, $R_{PD,LHI}$	LHI and DI/OUT_DISx Internal pulldown resistor				10		MΩ
DIGITAL OUTPUT PIN CHARACTERISTICS							
$V_{OH,SDO}$	Output logic high voltage drop	SDO pin current = -2mA	SDO pin current = -2mA			0.2	V
$V_{OL,SDO}$	Output logic low voltage	SDO Pin current = 2mA	SDO Pin current = 2mA			0.2	V
V_{OL_FLT}	Output logic low voltage drop	$\overline{FLT}$ pin current = 4mA	$\overline{FLT}$ pin current = 4mA			0.4	V

5.6 SPI Timing Requirements

Over operating junction temperature T_J = –40°C to 150°C

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SPI}	SPI clock (SCLK) frequency	C_{SDO} = 30 pF, R_{SDO} = 768Ω			8	MHz
t_{SPI}	SPI clock (SCLK) period	C_{SDO} = 30 pF, R_{SDO} = 768Ω	125			ns
t_{high}	High time: SCLK logic high-time duration		45			ns
t_{low}	Low time: SCLK logic low-time duration		45			ns
t_{sucs}	$\overline{CS}$ setup time: time delay between falling edge of $\overline{CS}$ and rising edge of SCLK		45			ns
t_{su_SDI}	SDI setup time: setup time of SDI before the falling edge of SCLK		15			ns
t_{h_SDI}	SDI hold time: hold time of SDI before the falling edge of SCLK		30			ns
t_{d_SDO}	Delay time: time delay from rising edge of SCLK to data valid at SDO				30	ns
t_{hcs}	Hold time: time between the falling edge of SCLK and rising edge of $\overline{CS}$		45			ns
t_{dis_cs}	$\overline{CS}$ disable time, $\overline{CS}$ high to SDO high impedance			10		ns

ADVANCE INFORMATION

5.6 SPI Timing Requirements (continued)

Over operating junction temperature T_J = –40°C to 150°C

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{hics}	SPI transfer inactive time (time between two transfers) during which $\overline{CS}$ must remain high		500			ns

5.7 Switching Characteristics

VBB = 48V, RL = 8.4Ω, (unless otherwise noted) @ TJ = -40°C to 150°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SLEEP}	Delay time from SLEEP state to CONFIG state	50% of falling edge of $\overline{CS}$ or 50% of rising edge of LHI		200		µs
t_{DR}	Channel turnon delay time (from CONFIG State)	50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 0x0		27		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 0x1		20		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 0x2		15.6		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 0x3		13		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 0x4		130		µs
		50% of $\overline{CS}$ or DIx to 10% of VOUT, SLRT_CHx = 0x7		6		µs
t_{DF}	Channel turnoff delay time	50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 0x0		217		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 0x1		156		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 0x2		122		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 0x3		100		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 0x4		930		µs
		50% of $\overline{CS}$ or DIx to 90% of VOUT, SLRT_CHx = 0x7		43		µs
SR_R	VOUT rising slew rate	20% to 80% of VOUT, SLRT_CHx = 0x0		0.27		V/µs
		20% to 80% of VOUT, SLRT_CHx = 0x1		0.36		V/µs
		20% to 80% of VOUT, SLRT_CHx = 0x2		0.43		V/µs
		20% to 80% of VOUT, SLRT_CHx = 0x3		0.5		V/µs
		20% to 80% of VOUT, SLRT_CHx = 0x4		0.057		V/µs
		20% to 80% of VOUT, SLRT_CHx = 0x7		0.8		V/µs
SR_F	VOUT falling slew rate	80% to 20% of VOUT, SLRT_CHx = 0x0		0.29		V/µs
		80% to 20% of VOUT, SLRT_CHx = 0x1		0.41		V/µs
		80% to 20% of VOUT, SLRT_CHx = 0x2		0.53		V/µs
		80% to 20% of VOUT, SLRT_CHx = 0x3		0.65		V/µs
		80% to 20% of VOUT, SLRT_CHx = 0x4		0.13		V/µs
		80% to 20% of VOUT, SLRT_CHx = 0x7		1.5		V/µs

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5.7 Switching Characteristics (continued)

VBB = 48V, RL = 8.4Ω, (unless otherwise noted) @ TJ = -40°C to 150°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Channel turnon time	50% of $\overline{CS}$ or DIx to 80% of VOUT, SLRT_CHx = 0x0		144		µs
		50% of $\overline{CS}$ or DIx to 80% of VOUT, SLRT_CHx = 0x1		108		µs
		50% of $\overline{CS}$ or DIx to 80% of VOUT, SLRT_CHx = 0x2		89		µs
		50% of $\overline{CS}$ or DIx to 80% of VOUT, SLRT_CHx = 0x3		76		µs
		50% of $\overline{CS}$ or DIx to 80% of VOUT, SLRT_CHx = 0x4		698		µs
		50% of $\overline{CS}$ or DIx to 80% of VOUT, SLRT_CHx = 0x7		45		µs
t_{OFF}	Channel turnoff time	50% of $\overline{CS}$ or DIx to 20% of VOUT, SLRT_CHx = 0x0		344		µs
		50% of $\overline{CS}$ or DIx to 20% of VOUT, SLRT_CHx = 0x1		246		µs
		50% of $\overline{CS}$ or DIx to 20% of VOUT, SLRT_CHx = 0x2		191		µs
		50% of $\overline{CS}$ or DIx to 20% of VOUT, SLRT_CHx = 0x3		157		µs
		50% of $\overline{CS}$ or DIx to 20% of VOUT, SLRT_CHx = 0x4		946		µs
		50% of $\overline{CS}$ or DIx to 20% of VOUT, SLRT_CHx = 0x7		67		µs
$t_{OFF\_OUT\_DIS}$	OUT_DIS channel turnoff time	50% of OUT_DIS to 10% of VOUT, DI_OUT_DIS_FN_CHx = 1		10		µs

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6 Parameter Measurement Information

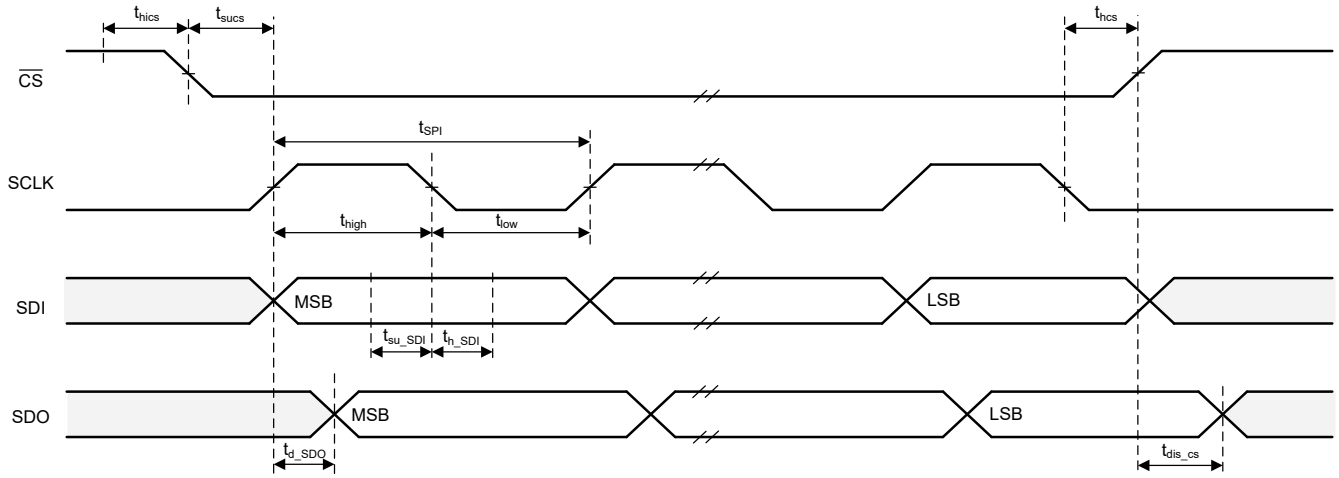

Figure 6-1. SPI Timing Characteristics Definitions

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7 Detailed Description

7.1 Overview

The TPS481HS04-Q1 device is a single-channel smart high-side switch intended for use with 12V automotive batteries. The TPS481HS04-Q1 device integrates SPI control and configuration as well digital readout with an ADC of key device and load diagnostics. The device incorporates all of the specific features needed for a power distribution switch as well as the traditional protective and diganostic functions seen in high side switches for actuator drive applications.

Diagnostics features include a digital current, output voltage and FET temperature sense output that can be read over the SPI serial interface. The high-accuracy load current sense allows for diagnostics of complex loads. The output voltage sense and FET temperature sense fearures in the device enables diagnosis of the switch and load failures.

This device includes protection through thermal shutdown, overcurrent protection, transient withstand, and reverse battery operation. In addition, the device also includes an SPI-configurable wire-harness protection function through a defined fuse or tme-current curve. The protection works in conjunction with an immediate switch-off overcurrent protection with an SPI-configurable threshold to fully protect against overload and short circuit faults.

The TPS481HS04-Q1device also integrates a low quiescent current mode where the device can provide currents in the 100s of mA range while consuming only micro-amps of current. The device automatically switches to the high-current mode on an increase in load current and provide a wake signal to the MCU. Further, the device includes a capacitive charging mode that reduces the peak current load on the supply. Together, the two features support power distribution switch to off-board ECU applications.

For more details on the diagnosis, power distribution and protection features, refer to the *Feature Description* and *Application Information* sections of the document.

The TPS481HS04-Q1 is one device in a family of TI high side switches. For each device, the part number indicates elements of the device behavior. Figure 7-1 gives an example of the device nomenclature.

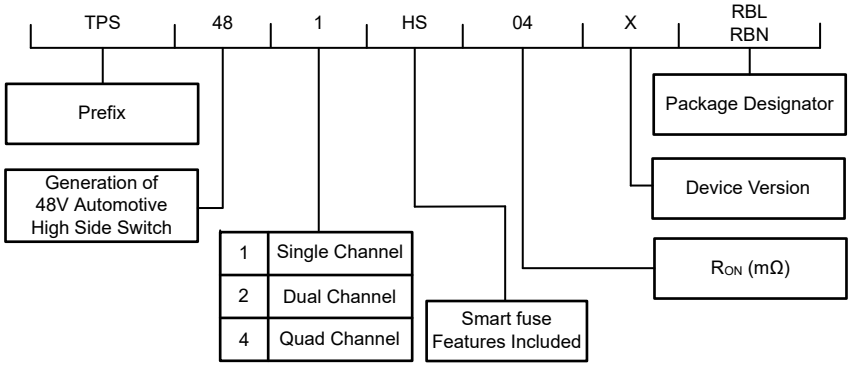

Figure 7-1. Naming Convention

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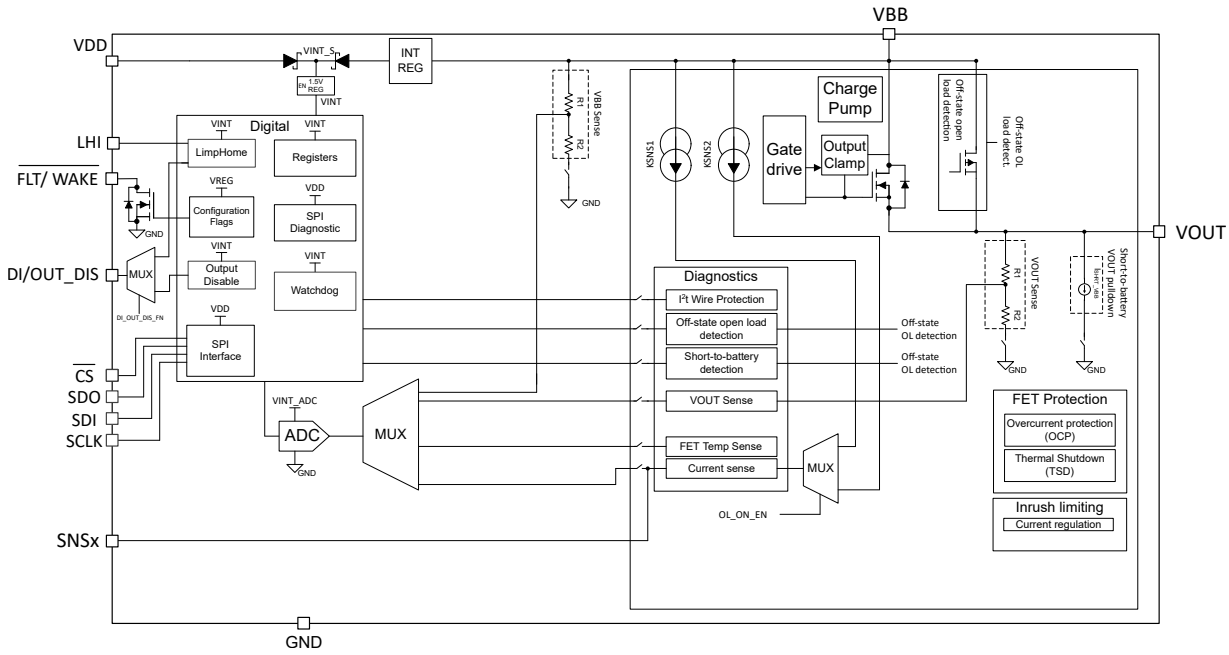
7.2 Functional Block Diagram

The functional block diagram for TPS481HS04-Q1 is shown below.



7.3 Feature Description

7.3.1 Driving Capacitive, Resistive and Inductive Loads

All off-board loads have different type. Each load profile will interact differently with the Smart High Side Switch or Controller and require different considerations to ensure robust protection. Whether the load is resistive, capacitive, inductive, or does not fall neatly into one of those categories such as LEDs will change how driving the load must be approached and designed. A proper output power protection designer needs to understand what load profile will be expected, and then understand how that impacts the design of the output stage.

Table 7-1. Load Driving Using TPS48xHSxx-Q1

TYPE OF LOAD	LOAD DRIVING METHOD	REGISTER SETTING
Capacitive Load, CAP_CHRG_CHx = 0x0, 0x2 or 0x3	Immediate shutdown (IOCP)	CAP_CHRG_CHx = 0x0 ILIMIT_SET_CHx INRUSH_DURATION_CHx *(used only for VOUT_ERR_CHx indication)*
	Current limit regulation (ICL_REG)	CAP_CHRG_CHx = 0x2, INRUSH_LIMIT_CHx, INRUSH_DURATION_CHx *(used only for VOUT_ERR_CHx indication)*
	Using main path PWM mode	CAP_CHRG_CHx = 0x3, PWM_DTY_CHx and PWM_FREQ_CHx INRUSH_DURATION_CHx
Resistive or Inductive Load	Using main path PWM method	CAP_CHRG_CHx = 0x0 PWM_EN_CHx = 0x1, PWM_DTY_CHx and PWM_FREQ_CHx

7.3.2 Protection Mechanisms

7.3.2.1 Overcurrent Protection

The TPS481HS04-Q1 device offers the following functions to protect the device from different overcurrent events:

- Capacitive load charging in inrush period
- Immediate shutdown overcurrent protection (I_{OCP})
- Programmable fuse protection (or I2T protection) in steady state
- Thermal shutdown (T_{REL} and T_{ABS})
- Short-circuit protection ($I_{SCP\_LPM\_MAN}$ or $I_{SCP\_LPM\_AUTO}$) in LPMs

In regards to overcurrent protection, the device has two operation modes, an optional inrush period at channel startup and during steady state operation. The optional inrush period can be configured to allow the device to handle different inrush currents such as bulbs, motor stall currents, or capacitive loads at the initial turn on of a channel. The CAP_CHRG_CHx, INRUSH_DURATION_CHx, and INRUSH_LIMIT_CHx bits in the ILIM_CONFIG_CHx registers control the operation of the device in the inrush period. I2T protection is only active in the inrush period if CAP_CHRG_CHx = 00 and if $V_{DS} < V_{DS\_LT\_2V}$. Steady state operation takes over after the inrush period has completed. During steady state operation, overcurrent protection (I_{OCP}) is active and I2T protection is active (if enabled).

During the inrush period all voltage sensing (VBB, VOUT) and FET temperature sensing can be used if enabled. Current sensing is only available in CAP_CHRG_CHx = 00 when $V_{DS} < V_{DS\_LT\_2V}$ or after the inrush period has completed and the device is in steady state operation. All voltage sensing, FET temperature sensing, and current sensing is available in the steady operation.

Figure 7-2 provides an overview of the overcurrent protection in the optional inrush period and steady state operation.

For more details on the different protections available in the inrush period and in steady state, see the following sections. Overcurrent protection in the LPM is covered in the LPM section.

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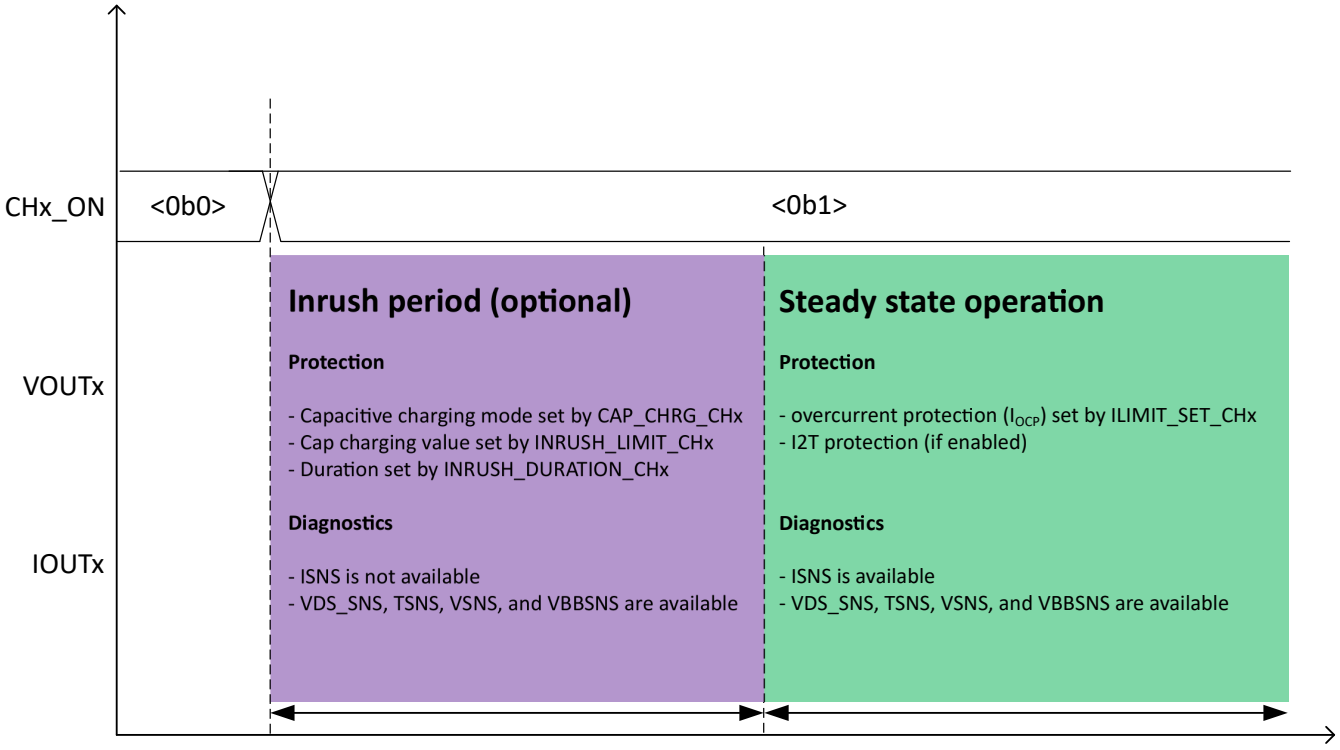

Figure 7-2. Overcurrent Protection Modes Overview

7.3.2.1.1 Inrush Period - Overcurrent Protection

The inrush period is an optional mode of the device where it can be configured to allow the device to handle different inrush currents such as bulbs, motor stall currents, or capacitive loads at the initial turn on of a channel. The inrush period can be configured through the CAP_CHRG_CHx, INRUSH_DURATION_CHx, and INRUSH_LIMIT_CHx bits in the ILIM_CONFIG_CHx registers. If the inrush period is enabled, it will take effect in both the ACTIVE state and the LIMPHOME mode if a channel is enabled in either of these states.

The device offers two different ovecurrent protection settings in the inrush period which can be set through the CAP_CHRG_CHx bits:

- No capacitive charging - immediate shutdown overcurrent protection (I_{OCP}) only
- Current limit regulation (I_{CL_REG})

The no capacitive charging setting, enables the device to have a different overcurrent protection (I_{OCP}) value in the inrush period compared to steady state to allow for bulb current inrush or motor stall current. Additionally, in the no capacitive charging setting, I2T protection (if enabled) is active if $V_{DS} < V_{DS\_LT\_2V}$. The current limit regulation mode, allows for the device to charge up large capacitances such as input capacitors on downstream ECUs. Depending on the CAP_CHRG_CHx bit settings, the values of the INRUSH_LIMIT_CHx will change. The overcurrent protection for each channel is independent and can be set on an per channel basis.

No Capacitive Charging - CAP_CHRG_CHx = 00

The no capacitive charging setting, enables the device to have a different immediate shutdown overcurrent protection (I_{OCP}) value in the inrush period compared to steady state operation to allow for different inrush events at startup such as bulb current inrush or motor stall current.

If CAP_CHRG_CHx [1:0] = 00, the immediate shutdown overcurrent protection (I_{OCP}) value in the inrush period is set by the INRUSH_LIMIT_CHx [3:0] bits and the duration is set by the INRUSH_DURATION_CHx [2:0] bits. Once the inrush period duration timer expires the immediate shutdown overcurrent protection (I_{OCP}) value will be set by the ILIMIT_SET_CHx [3:0] bits in steady state operation.

If CAP_CHRG_CHx [1:0] = 00, I2T protection (if enabled) and current sensing is available if $V_{DS} < V_{DS\_LT\_2V}$.

An example of this is shown in Figure 7-3.

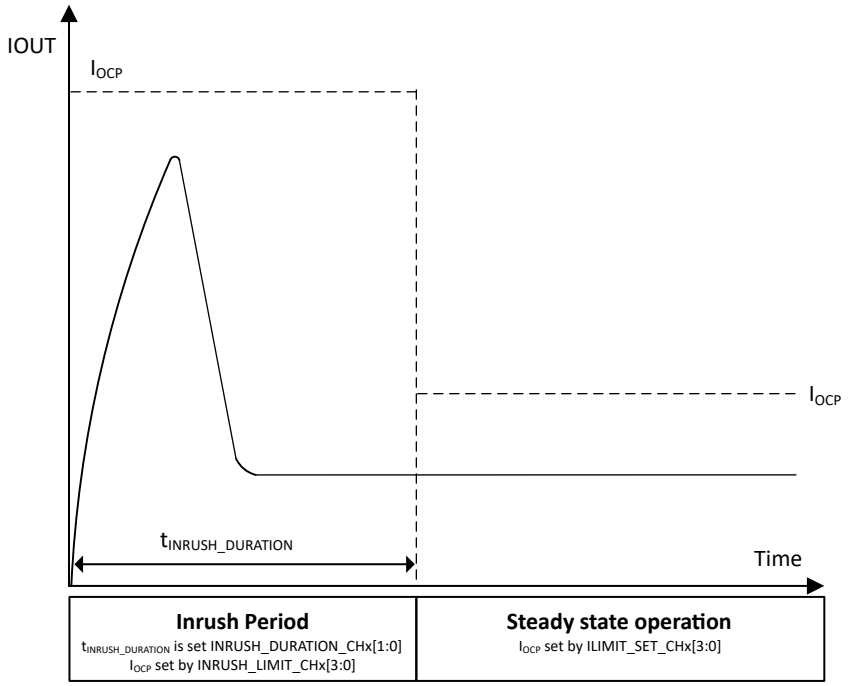

Figure 7-3. No Capacitive Charging (CAP_CHRG_CHx [1:0] = 00) - Bulb Driving Example

Current limit regulation capacitive charging mode - CAP_CHRG_CHx [1:0] = 10

The device offers a current limit regulation capacitive charging mode to charge up large downstream capacitive loads such as bulk input capacitors on ECUs. If CAP_CHRG_CHx [1:0] = 10, the current limit regulation mode will clamp the output current when the channel is initially enabled at a value set by the INRUSH_LIMIT_CHx [3:0]. The device will limit the current continuously until the capacitive load has finished charging, the inrush period expires, or a thermal shutdown has occurred. The range of settings which can be programmed through the INRUSH_LIMIT_CHx [3:0] and are specified in the electrical characteristic table as I_{CL_REG}. If the VOUT voltage is greater than VBB - 2V and the inrush period timer has not expired, the device is able to slowly exit the current limit regulation without a large spike. An example of the current limit regulation capacitive charging mode and the slow exit before the inrush period timer expiration is shown in Figure 7-4.

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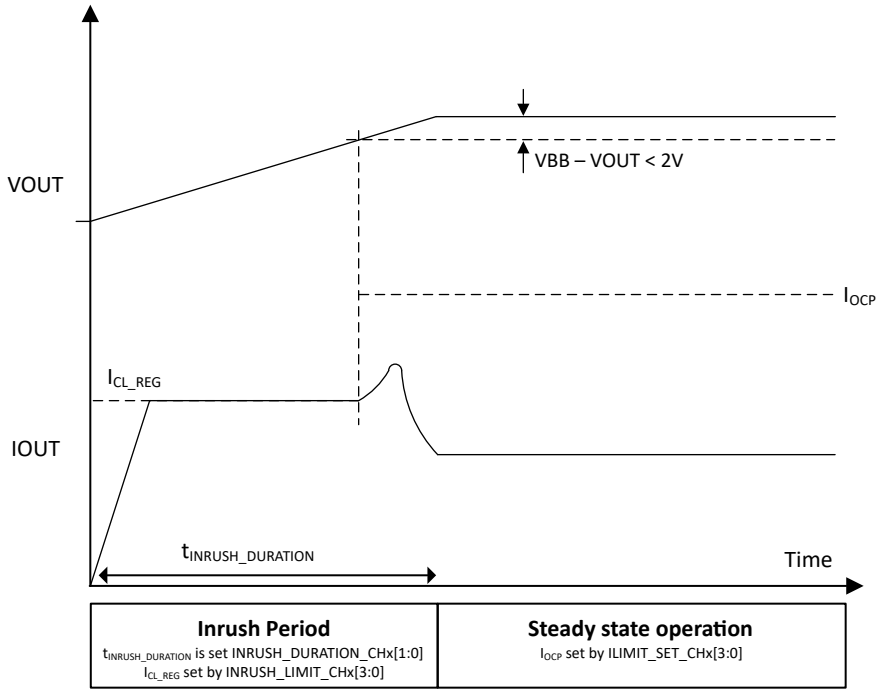

Figure 7-4. Current Limit Regulation Capacitive Charging (CAP_CHRG_CHx [1:0] = 10) - ECU Input Bulk Capacitance Driving Example

7.3.2.1.2 Overcurrent Protection - Steady State Operation

After the device has completed the optional inrush period (if enabled) the device will enter the steady operation. In this operation, the overcurrent protection is provided by the immediate shutdown overcurrent protection (I_{OCP}) and I2T protection (if enabled). The I_{OCP} is an overcurrent protection function that immediately turns off the channel if the output current exceeds I_{OCP} threshold that is set by the ILIMIT_SET_CHx [3:0] bits. The I_{OCP} function can not be disabled and is always active in the steady state operation while the device is enabled. The I2T protection provides a programmable fuse protection that is based on a defined time-current curve. The intent of the I2T protection is to match the behavior of a melting fuse. The time-current curve of the I2T protection can be set through the NOM_CUR_CHx [2:0] bits and I2T_TRIP_CHx [3:0] bits. The ISWCL_CHx [1:0] and I_{OCP} also help to define the time-current curve for the I2T protection. The I_{OCP} and I2T protection (if enabled) are active in the ACTIVE state and the LIMPHOME mode if the channel is in the steady state operation after the inrush period.

The next sections describes the I2T protection and the I_{OCP} protection.

7.3.2.1.3 Programmable Fuse Protection

The device includes a programmable fuse protection for each channel, that is based on a defined time-current curve and is commonly referred to as I2t protection in melting fuse data sheets. The intent is to match the switch turnoff behavior of a melting fuse. The NOM_CUR_CHx [2:0] bits and I2T_TRIP_CHx [3:0] bits set the time-current curve but the device also uses a fixed delay shutdown (I_{SWCL}) and immediate shutdown protection (I_{OCP}) to create the full I2T protection for the device. The I2T protection of the TPS481HS04-Q1 consists of four regions:

1. Nominal current
2. Fuse shutdown
3. Fixed delay shutdown
4. Immediate shutdown protection (I_{OCP})

These operational regions for the I2T protection are shown in Figure 7-5.

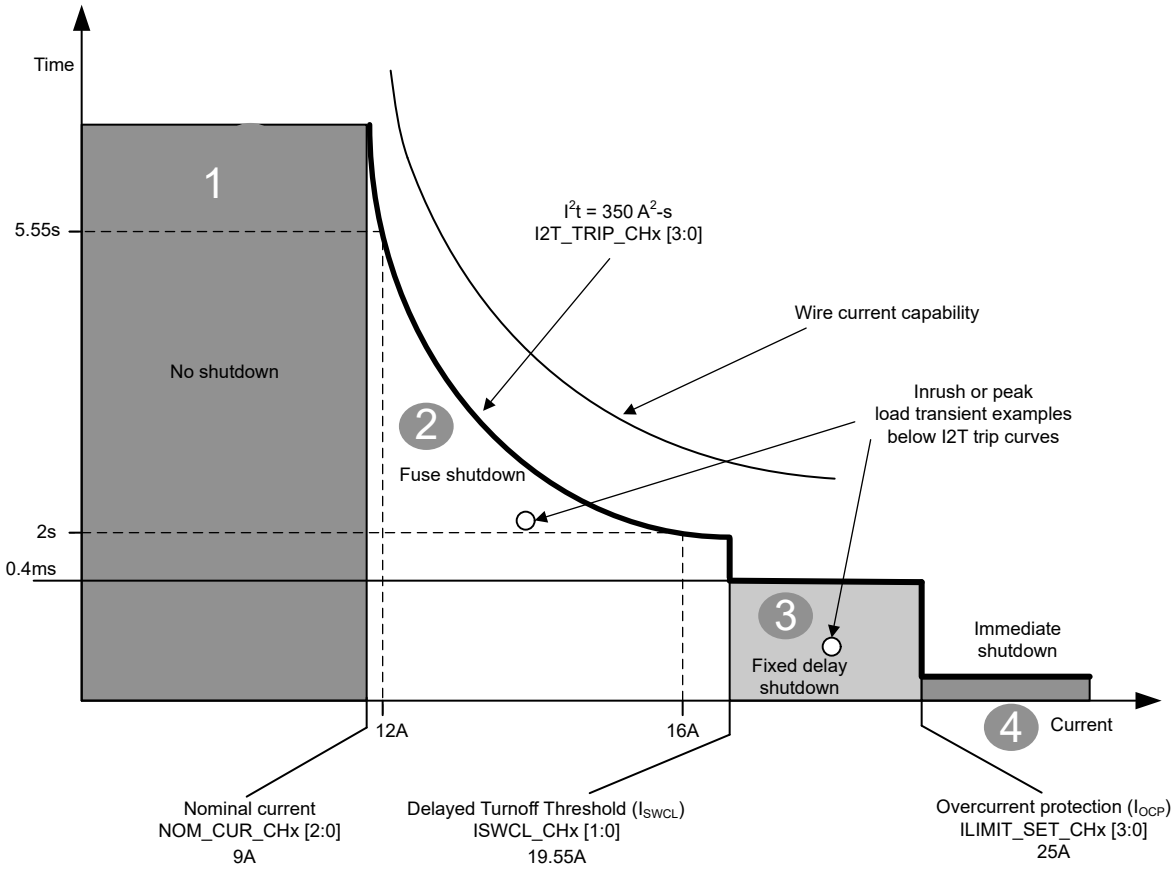

Figure 7-5. Operational Region of Fuse Based Shutdown

The nominal current region (1) defines the region where the device can supply current indefinitely without turning off. This is roughly equivalent to the fuse current rating of a melting fuse. This region is set by the NOM_CUR_CHx [2:0] bits and if the output current is less than the NOM_CUR_CHx setting then the device can supply current indefinitely as previously stated and it will not start the I2T accumulation. If the output current is greater than or equal to the NOM_CUR_CHx setting then the device will enter the I2T accumulation loop and will start to accumulate until the I2T_TRIP_CHx [3:0] threshold is met. If the output current falls back below the NOM_CUR_CHx before the I2T_TRIP_CHx value is reached then the device will stop the I2T accumulation but will still keep track of the accumulated energy as long as power is provided to the device.

Above the nominal current region, is the fuse shutdown region (2) which is set by the I2T_TRIP_CHx [3:0] bits. This region defines the curvature of time-current curve and the region where the I2T accumulation of the device is active. Based on the output current level and the NOM_CUR_CHx setting the device will trip at different time intervals based on the I2T_TRIP value that is set.

Accumulation and De-accumulation for DCR_CHx = '1' setting:

The time-current curve of the device is defined by below equation.

$I2T\_TRIP = (ILOAD^2 - INOM^2) * t$ (Equation 1)

If the accumulation does not exceed the I2T_TRIP value and the current falls below NOM_CUR_CH then equation 1 is used to decrement the accumulated energy based on the ISNS value until the accumulated energy reaches zero. While the device continues to decrement down to zero, the I2T_MOD bit will remain 1 until accumulated energy returns back to zero and then the I2T_MOD bit will be set back to zero. If any conversions were disabled due to a channel entering the I2T loop then they will be re-enabled when I2T_MOD = 0.

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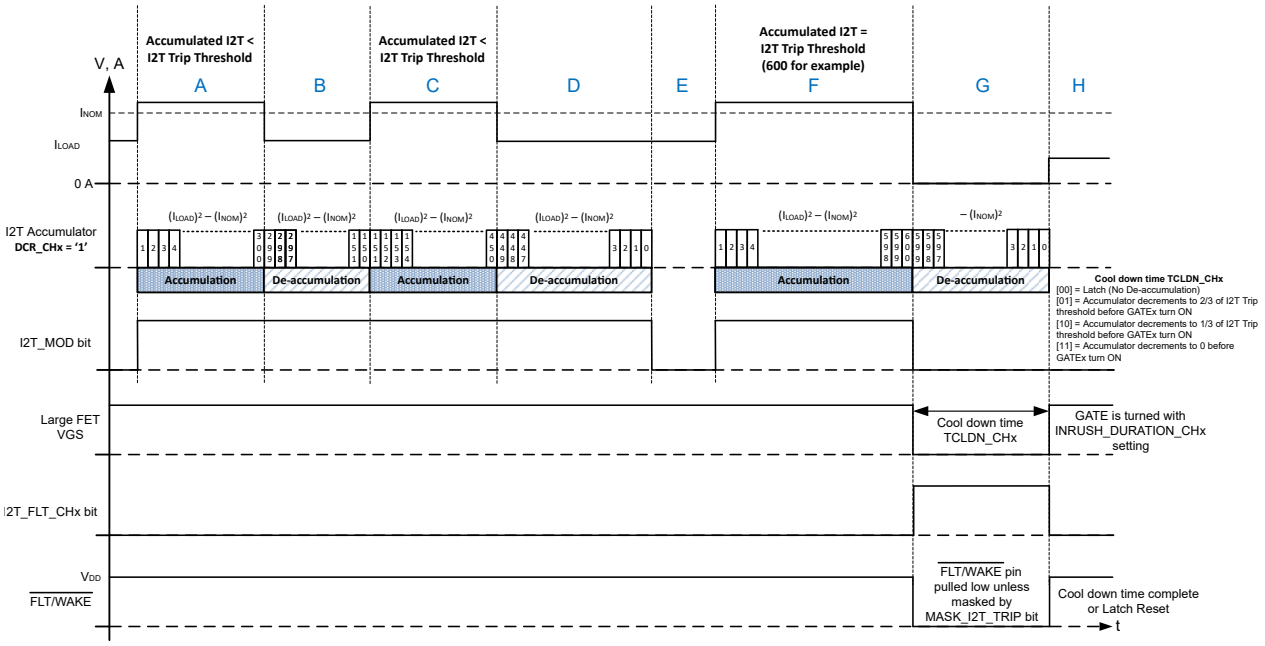

Figure 7-6. I2T Accumulation and De-Accumulation With DCR_CHx = '1' Setting

Accumulation and De-accumulation for DCR_CHx = '0' setting:

I2T_TRIP = (I_{LOAD}^2) * t (Equation 2)

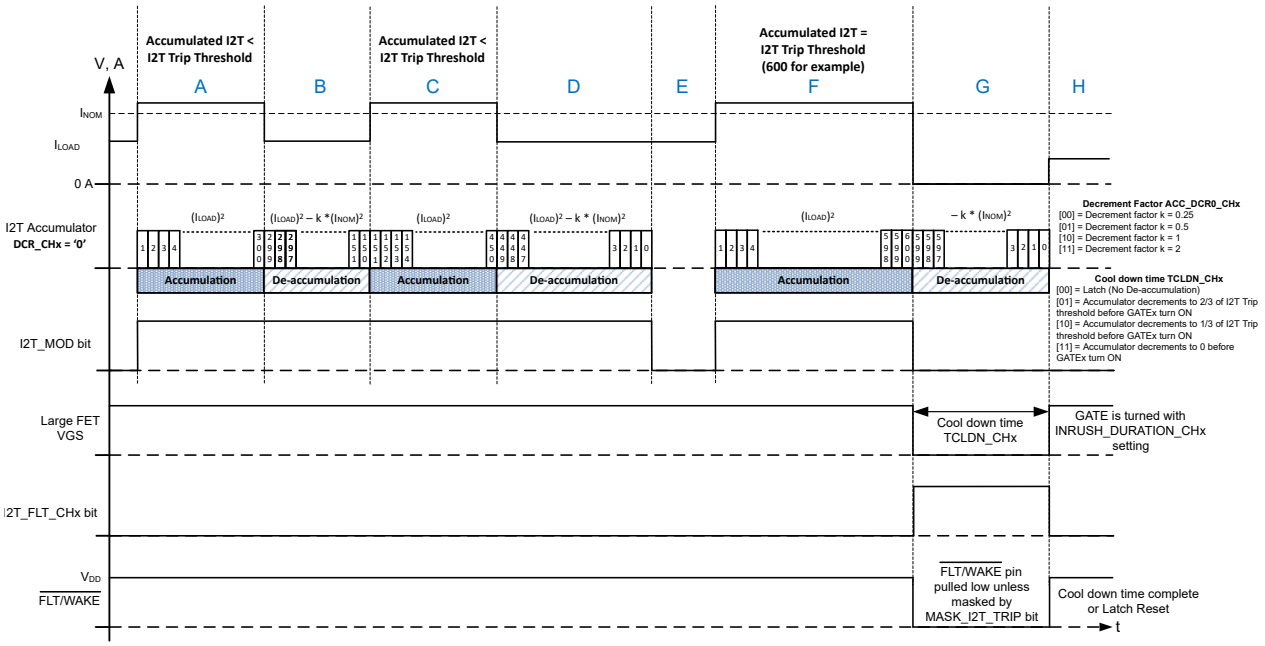

Figure 7-7. I2T Accumulation and De-Accumulation With DCR_CHx = '0' Setting

Above the fuse shutdown region, is the fixed delay shutdown region (3) where the device provides a fixed delayed shutdown that is set by the ISWCL_CHx [1:0] and SWCL_DLY_TMR_CHx [1:0] bits. The ISWCL_CHx [1:0] sets the output current value and the SWCL_DLY_TMR_CHx sets the time. If the output current exceeds the ISWCL_CHx level continously for SWCL_DLY_TMR_CHx then the channel will immediately turn off.

If a shutdown occurs either due to the I2T_TRIP_CHx value being exceeded or due to the ISWCL_CHx function, the device will remain off for a period set by the TCLDN_CHx [1:0]. If the TCLDN_CHx [1:0] = 00 then the device will remain off and will not retry. To retry in this setting, the TCLDN_CHx [1:0] bits need to be changed to another setting. Once the setting has been changed, the device will retry after the defined cool down time of the new setting. Note, when the channel enters the I2T shutdown state the accumulator value will be reset to 0 so the retry time should be adjusted to make sure enough time has elasped for the wire harness to cool down. Also note, when the channel enters the I2T shutdown state, the values for NOM_CUR_CHx, I2T_TRIP_CHx, and ISWCL_CHx can not be changed.

Above the fixed delay shutdown region, is the immediate shutdown overcurrent protection (I_{OCP}) region (4). This region is set by the ILIMIT_SET_CHx [3:0] bits. If the output current exceeds the I_{OCP} level then the device will turn off immediately. The retry or latched off behavior for the I_{OCP} is set by the LATCH_CHx bit and discussed in the next section.

7.3.2.1.4 Immediate Shutdown Overcurrent Protection (I_{OCP})

In steady state operation, the device offers immediate shutdown overcurrent protection (I_{OCP}) which is an overcurrent protection function that immediately turns off the channel if the output current exceeds the I_{OCP} threshold that is set by the ILIMIT_SET_CHx [3:0] bits. The ILIMIT_SET_CHx [3:0] bits enable the I_{OCP} function to be set on a per channel basis. The I_{OCP} function can not be disabled and is always active in the steady state operation while the device is enabled.

If the I_{OCP} level is exceeded, the channel will turn off immediately and the channel will either retry or latch-off based on the setting of the LATCH_CHx bit. If LATCH_CHx = 0, the channel will retry after $t_{RETRY,INT}$. After the retry time expires, the channel will start up into the inrush period if configured. If the short-circuit condition persists, the channel will continue to retry with $t_{RETRY,INT}$ between retries for up to 7 times. If still the short-circuit condition exists, the channel will retry an additional 7 times with $t_{RETRY,EXTD}$ between retries before the channel is latched off. To remove the device out of the latch off state with LATCH_CHx = 0, the CHx_ON bit needs to be toggled or the DIx/OUT_DISx or LHI pin needs to be toggled. If LATCH_CHx = 1 and the I_{OCP} level is exceeded, the device will latch-off and will not retry until the CHx_ON bit is toggled or the DIx/OUT_DISx or LHI pin is toggled or the LATCH_CHx bit is toggled. For more details on how the retry and latch off works for different device settings, see the retry and latch-off behavior section below.

7.3.2.2 Output Disable Function (OUT_DIS)

TPS481HS04-Q1 device provide a function to quickly disable output channel x in t**OFF_OUT_DIS** if the OUT_DISx pin goes high. The output disable (OUT_DIS) function is used to turn off an output quickly due to an emergency situation where the output needs to be quickly turned OFF.

This OUT_DIS function will be multiplexed with the Direct Input (DI) function on a per channel basis. If DI_OUT_DIS_FN_CHx is set to '1' in the DIAG_CONFIG_CHx register, the DIx/OUT_DISx pin will be configured as a OUT_DIS for that channel. The masking time can be programmed using CONFIG_DI_MASK bits in case there are any ground bounce issues in the device.

The table below shows the GATEx state based on the different pin and register configurations for the OUT_DIS function (**OUT_DIS Logic Table when DI_OUT_DIS_FN_CHx = '1'**).

Table 7-2. OUT_DIS Logic Table

OUT_DIS	LHI	VOUTx STATE
L	L	Follow CHx_ON
L	H	Follow CHx_LH_IN
H	L	OFF
H	H	OFF

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If the OUT_DISx pin is high with the output channel off and the OUT_DISx pin is then asserted low, the output channel will follow either the CHx_ON bit if in ACTIVE mode or follow the CHx_LH_IN bits in the LIMPHOME mode. In this scenario, the channel will go through the inrush period (if configured) if the CHx_ON bit or the CHx_LH_IN bits are configured for the channel to be enabled.

7.3.2.3 Thermal Shutdown

The device includes a temperature sensor on the power FET and within the controller portion of the device to monitor the temperature of the FET ($T_{J,FET}$) and the temperature of the controller ($T_{J,CONTROLLER}$). There are two cases that the device will consider to be a thermal shutdown fault:

- **Relative thermal shutdown (T_{REL}):** $T_{J,FET} - T_{J,CONTROLLER} > T_{REL}$
- **Absolute thermal shutdown (T_{ABS}):** $T_{J,FET} > T_{ABS}$

If either of the above faults occur, the switch will be turned off. The device will signal a fault through the $\overline{FLT}$/$\overline{WAKE}$ pin.

Relative thermal shutdown (T_{REL})

A relative thermal shutdown event can occur when there is a large peak power event such as a short-to-ground event where the FET temperature ($T_{J,FET}$) quickly rises relative to the controller temperature ($T_{J,CONTROLLER}$). Once the relative temperature ($T_{J,FET} - T_{J,CONTROLLER}$) exceeds T_{REL} the channel will be turned off.

Absolute thermal shutdown (T_{ABS})

An absolute thermal shutdown occurs when the FET temperature ($T_{J,FET}$) rises above T_{ABS}. This can occur when a channel is subjected to long durations of overcurrent such as a permanent short use case. Once the FET temperature ($T_{J,FET}$) exceeds T_{ABS} the channel will be turned off.

7.3.2.4 Reverse Battery

In the reverse battery condition, the switch will automatically be enabled regardless of the state of the output (set by the SW_STATE register) to prevent excess power dissipation inside the MOSFET body diode. In many applications (for example, resistive loads), the full load current may be present during reverse battery.

7.3.3 Diagnostic Mechanisms

7.3.3.1 Integrated ADC

The TPS481HS04-Q1 provides an integrated successive approximation 10-bit ADC which can convert different analog signals to digital signals which can be read out through SPI. The ADC can convert the following analog signals:

- Current sense (ISNSx)
- MOSFET temperature sense (TSNSx)
- VBB voltage sense (VBB)
- VOUT voltage sense (VOUTx)

Figure 7-8 provides a functional block diagram of the integrated ADC along with the analog signal inputs to the ADC.

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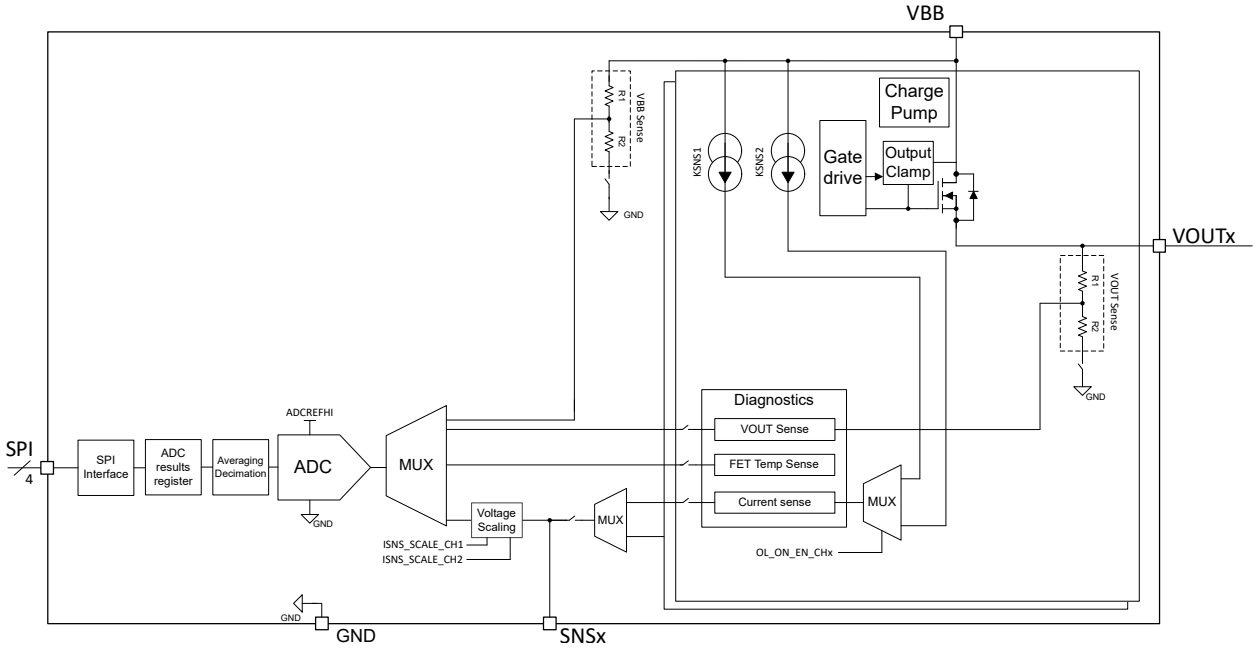

Figure 7-8. Integrated ADC Functional Block Diagram

Conversion of any of the analog signals can either be disabled globally through the ADC_CONFIG register.

The device also provides a configurable delay which can also help to further reduce the quiescent current of the device by reducing the sampling rate of the ADC. The configurable delay is set by the ADC_CONFIG_DELAY [1:0] bits in the ADC_CONFIG register.

If I2T protection is enabled (I2T_EN_CHx = 1) and either channel is not in I2T mode (I2T_MOD_CHx = 0), then the device will convert each of the analog signals in a round robin sequence with the configurable delay. Figure below shows the ADC scheduling if no channel is in I2T mode (I2T_MOD_CHx = 0) and all analog signal conversions are enabled. If I2T protection is disabled then the round robin sequence below also applies.

If I2T protection is enabled (I2T_EN_CHx = 1) and one or both of the channels are in I2T mode (I2T_MOD_CHx = 1), then the device disables all conversions except for the ISNSx conversions which are used for the internal I2T protection. The device also disables the configurable delay function as well. Figure below shows the ADC scheduling if one or both of the channels are in I2T mode (I2T_MOD_CHx = 1).

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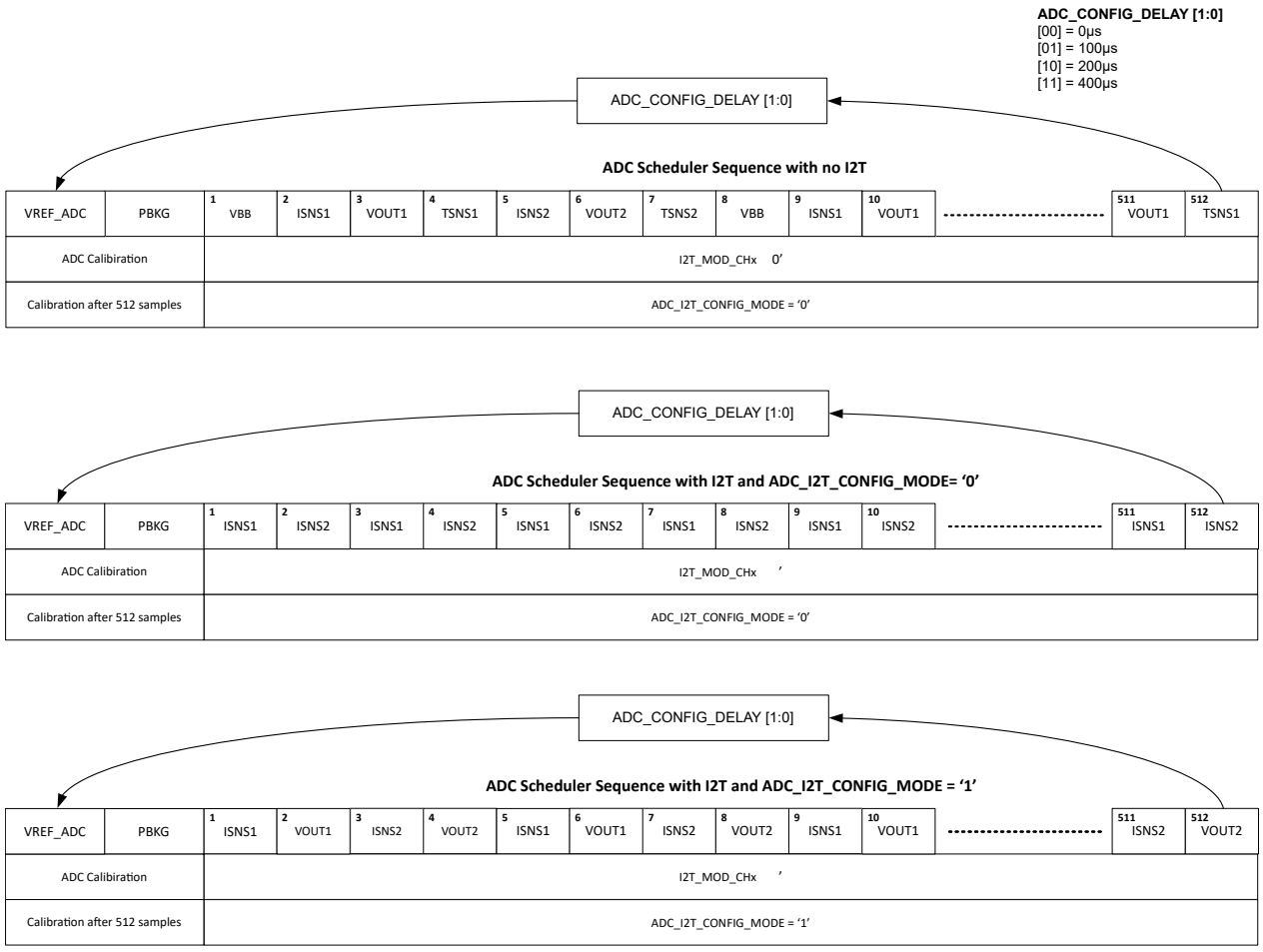

Figure 7-9. ADC Conversion Sequence

7.3.3.2 Analog and Digital Current Sense Output

The integrated current sense circuit of the device provide a sense current (I_{SNS}) proportional to the load current (I_{OUTx}) of each channel. The current sense of each channel is multiplexed internally and is provided to ADC scheduler. The sensed current result of the ADC conversion is stored in ADC_RESULT_CHx_I for each channel. The ISNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register was last read.

To ensure an accurate sensing measurement on SNS pin, the sensing resistor should be connected to the IC GND.

The ADC conversion equation for current sense for different OL_ON_EN_CHx settings are below:

with OL_ON_EN_CHx = 0, applicable to large FET current sense only

$$\text{ADC\_RESULT\_CHx\_I} = \frac{1023}{V_{(\text{ADC\_REF})}} \times \frac{\text{ILOADx}}{\text{KDIG1}} \quad (1)$$

with OL_ON_EN_CHx = 1, applicable to small FET current sense only

$$\text{ADC\_RESULT\_CHx\_I} = \frac{1023}{V_{(\text{ADC\_REF})}} \times \frac{\text{ILOADx}}{\text{KDIG2}} \quad (2)$$

The voltage on SNSx pin is based on RSNSx resistor and can be derived based on below equation

with OL_ON_EN_CHx = 0, applicable to large FET current sense only

$$VSNSx = \frac{ILOADx}{KSNS1} \times R_{SNSx} \quad (3)$$

with OL_ON_EN_CHx = 1, applicable to small FET current sense only

$$VSNSx = \frac{ILOADx}{KSNS2} \times R_{SNSx} \quad (4)$$

The current sense function is enabled for each channel by default. The current sense function can be enabled or disabled globally through the ADC_ISNS_DIS bit in the ADC_CONFIG register.

If I2T protection is used, the current sense function has to be enabled before the I2T protection can be used. The current sense function is only available when the channel is enabled and in the steady state operation. The current sense function is not available in the inrush period.

7.3.3.3 Output Voltage Measurement

The TPS481HS04-Q1 provides an output voltage measurement per channel through the integrated 10-bit ADC.

The output voltage measurement function is disabled by default. To enable the output voltage sense function it needs to be globally enabled in the ADC_CONFIG register through the ADC_VSNS_DIS bit. If the global bit is enabled then the device will enable the output voltage measurement on each channel according to the VSNS_DIS_CHx bit in the respective CHx_CONFIG register.

The conversion equation for the output voltage measurement is given below. The ADC measurement result will be available in the ADC_RESULT_CHx_VOUT register. The VSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register was last read.

$$ADC\_RESULT\_CHx\_V = \frac{1023}{V_{(ADC\_REF)}} \times 0.043 \times VOUTx \quad (5)$$

7.3.3.4 MOSFET Temperature Measurement

The TPS481HS04-Q1 provides a temperature measurement for each of the power MOSFETs through the 10-bit ADC.

The FET temperature sense function is disabled by default. To enable the FET temperature sense function for each channel it needs to be globally enabled in the ADC_CONFIG register through the ADC_TSNS_DIS bit.

The conversion equation for the FET temperature measurement is detailed in Equation 6.

$$ADC\_RESULT\_T = 507.42 - 1.33 \times T \quad (6)$$

The ADC measurement result will be available in the ADC_RESULT_CHx_T register. The TSNS_RDY_CHx bit is set to 1 if a new ADC conversion result exists since the register was last read. If any of the channels are in the I2T loop (I2T_MOD_CHx = 1), the FET temperature measurement, if enabled, will be disabled for all the channels and the TSNS_RDY_CHx bit will be 0. Once the channel(s) exit the I2T loop (I2T_MOD_CHx = 0), then the FET temperature measurement will be automatically re-enabled if previously enabled before the I2T event.

7.3.3.5 VBB Voltage Measurement

The TPS481HS04-Q1 provides a VBB voltage measurement through the 10-bit ADC.

The VBB voltage measurement is disabled by default. The VBB voltage sense function can be enabled through the ADC_VBB_DIS bit in the ADC_CONFIG register.

The conversion equation for the VBB voltage measurement is detailed in Equation 7. The ADC measurement result will be available in the ADC_RESULT_VBB register. The VBB_RDY bit is set to 1 if a new ADC conversion result exists since the register was last read.

ADVANCE INFORMATION

$$ADC\_RESULT\_VBB = \frac{1023}{V_{(ADC\_REF)}} \times 0.045 \times VBB \quad (7)$$

7.3.3.6 VOUT Short-to-Battery and Open-Load

The TPS481HS04-Q1 is capable of detecting short-to-battery and open-load events regardless of whether the channel output is turned on or off, however the two conditions use different methods.

7.3.3.6.1 Measurement With Channel Output (FET) Enabled

When the channel output is enabled and the FET is on, the VOUT short-to-battery and open-load conditions can be measured with the current sense feature. In both cases, the load current is measured using the current sense circuit and the ADC (available in the ADC_RESULT_CHx_I registers). The current sense accuracy can be increased at low current levels by turning off the large FET and turning on the small FET. This is accomplished by setting the OL_ON_EN_CHx bit to 1 in the individual CHx_CONFIG register. However, the load current must be below $I_{ENTRY\_OL\_ON}$ for this bit to take effect. This enables the ADC to measure the low load current with higher accuracy.

The ADC conversion equation for current sense for OL_ON_EN_CHx setting enabled is below:

with OL_ON_EN_CHx = 1,

$$ADC\_RESULT\_CHx\_I = \frac{1023}{V_{(ADC\_REF)}} \times \frac{ILOADx}{KDIG2} \quad (8)$$

It is recommended to only use OL_ON_EN_CHx = 1 mode with I2T disabled (I2T_EN = 0). If OL_ON_EN_CHx = 1 is used with I2T enabled (I2T_EN = 1) this could cause the channel to turn off at unintended lower I2T thresholds.

7.3.3.6.2 Detection With Channel Output Disabled

The device is able to detect an open load or a short-to-battery event when the channel output is disabled (FET is off). These will be referred to below as off state open load detection and off state short-to-battery detection. When the channel output is disabled, the device is able to distinguish between an open load event and a short-to-battery event through a defined sequence that will be discussed below. A block diagram for the off-state open load and off-state short-to-battery detection is shown in Figure 7-10.

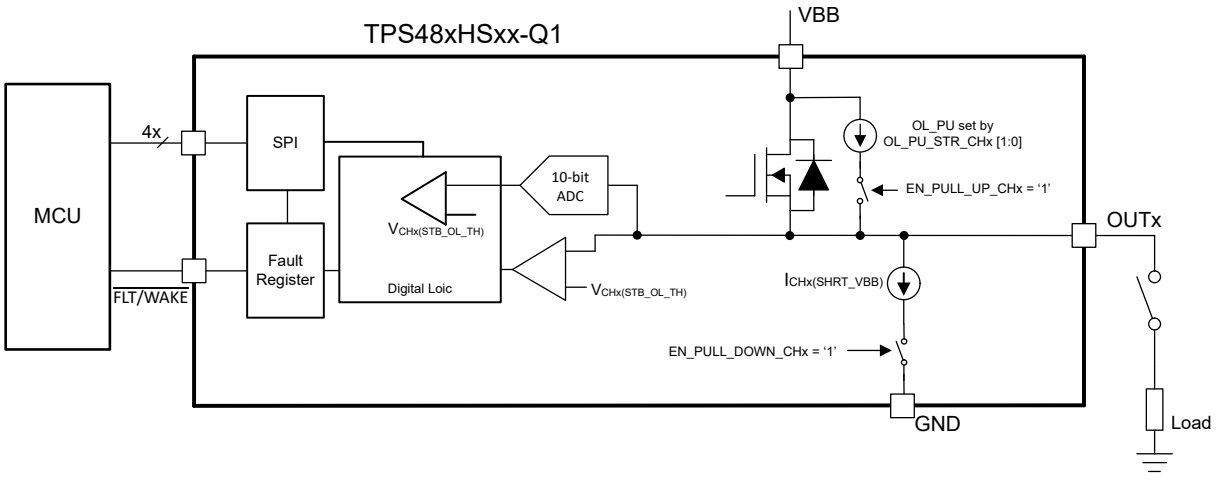

Figure 7-10. Open Load and Short-to-Battery Detection

Note

This figure assumes that the device ground and the load ground are at the same potential. In a real system, there may be a ground shift voltage of the order of 1V.

Off-State Short-to-Battery Detection

The device also integrates a pull-down current (I_{SHRT_VBB}) for each channel which can be used to help distinguish between an open load and a short-to-battery fault when the channel is disabled. The pull-down resistor is enabled when EN_PULL_DOWN_CHx bit is set.

.

After some time delay based on output wire harness inductance, output capacitor and loading, SVBB_DIAG_EN_CHx bit can be enabled by MCU to enable an internal comparator which is used to detect if the VDS is above or below the $V_{CHx(SHRT\_VBB)}$

Off-State Open Load Detection

Once short to battery detection is complete without any fault then pull down resistor can be disabled and open load detection can be run. The device integrates a pull-up current source, OL_PU, for each channel which can be used to pull-up the output to determine if open load fault is present or not. The pull-up current source is enabled via EN_PULL_UP_CHx bit.

The strength of the internal pull-up can be programmed through the OL_PU_STR_CHx bits for each channel in the DIAG_CONFIG_CHx registers.

After some time delay based on output wire harness inductance, output capacitor and loading, OL_DIAG_EN_CHx bit can be enabled by MCU to enable an internal comparator which is used to detect if the output voltage is above or below the $V_{CHx(SHRT\_VBB)}$.

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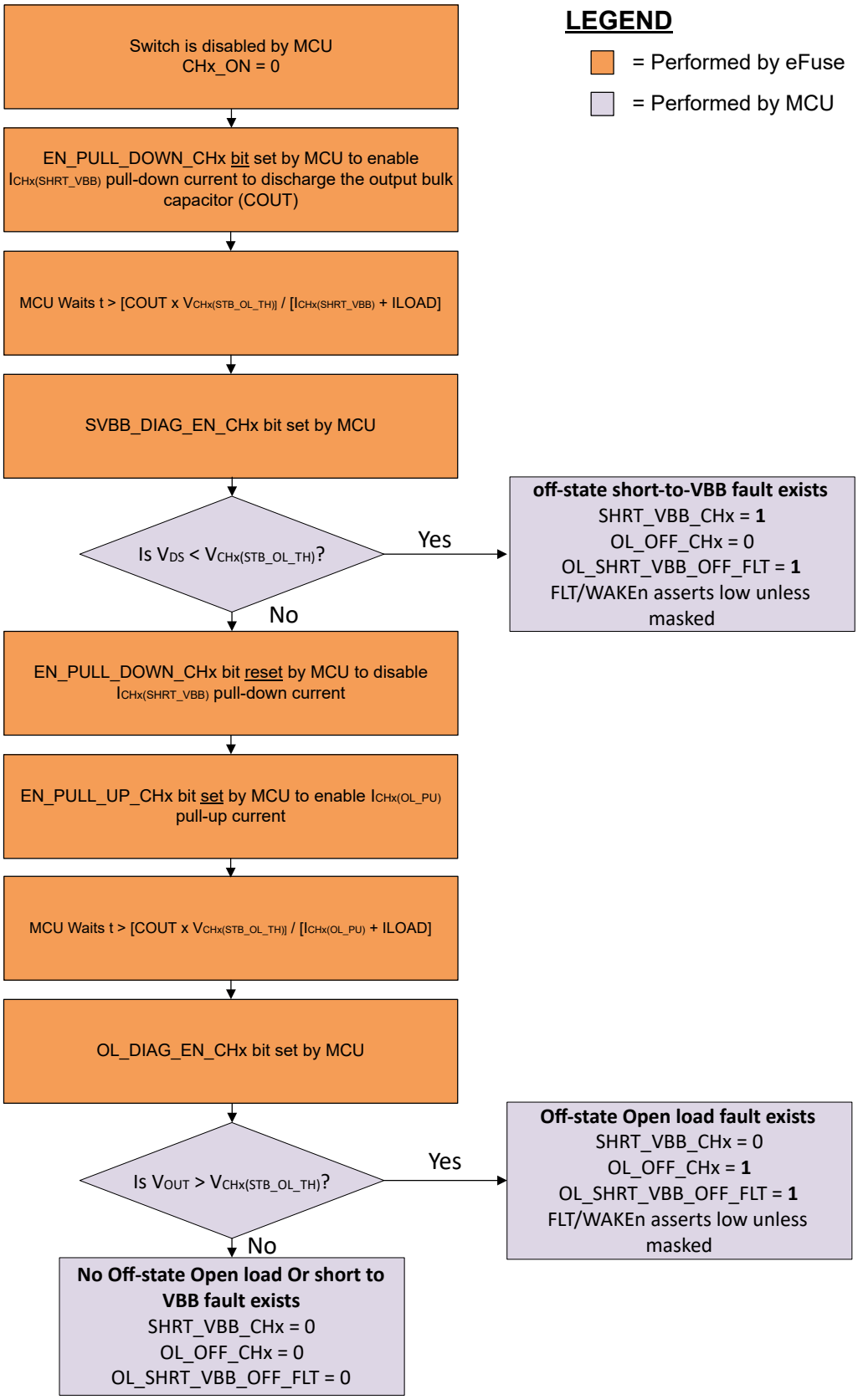

Figure 7-11. Flow Chart For VOUT Short to VBB or FET Short and Open Load Detection With Channel Disabled

7.3.3.7 VOUT Short-to-Battery or FET Short Detection For Power at All Times (PAAT) Loads

The device integrates a pull-down xurrent for each channel which can be used to detect VOUT short-to-battery or FET short fault when the channel is disabled. See below flow chart for detection mechanism

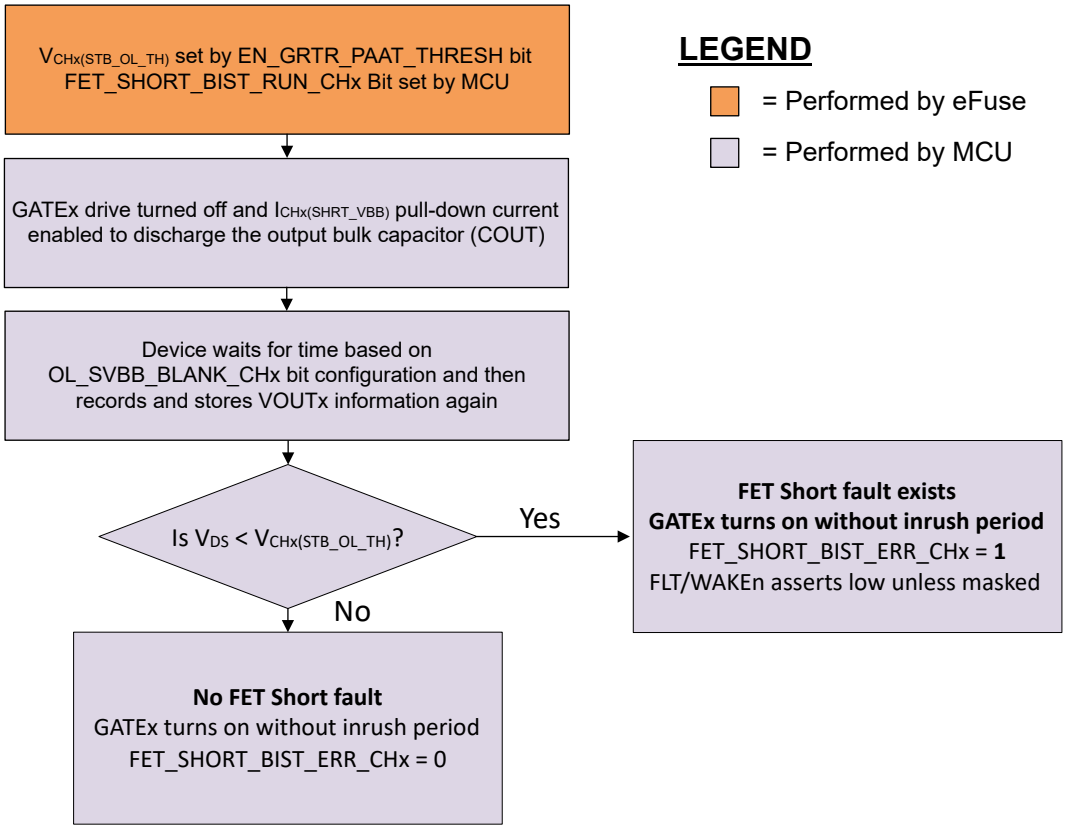

Figure 7-12. Flow Chart for FET Short Diagnosis for PAAT Loads

7.3.4 Fault Indication (FLT / WAKE)

The device provides enhanced fault reporting through a $\overline{\text{FLT/WAKE}}$ status pin and fault status bits through SPI.

The $\overline{\text{FLT/WAKE}}$ status pin allows the device to interrupt the system when a fault has occurred on the device. The $\overline{\text{FLT/WAKE}}$ status pin is an open drain output that asserts low when a fault occurs on the device. For faults which are read clear, the $\overline{\text{FLT/WAKE}}$ pin will go high if the fault no longer exists and the specific register to clear the fault is read. Indication on the $\overline{\text{FLT/WAKE}}$ pin can be masked for some faults through FAULT_MASK register. See the FAULT_MASK register for more details.

The device also provides fault information through SPI through a global fault register (FAULT_GLOBAL) and channel specific fault registers (FLT_STAT_CHx) to enable the system to quickly diagnose what caused the fault in the device. The device outputs the FAULT_GLOBAL [15:8] bits on the SDO header so these status bits can be continosly read for each SPI transaction.

For more details on each of the individual fault status bits see the FAULT_GLOBAL and FLT_STAT_CHx registers in the register map.

Table 7-3 highlights how the device signals different events through the $\overline{\text{FLT/WAKE}}$ pin and the fault status bits.

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Table 7-3. Fault Reporting Table

EVENT / FAULT		DETECTION	PROTECTION	FAULT_GLOBAL REPORTING	FLT_STAT_CHx REPORTING	$\overline{\text{FLT/WAKE}}$ INDICATION
FET - Overtemperature Warning		Y	N	CHx_FLT	THERMAL_WRN_CHx	N
FET - Temperature shutdown (TSD)		Y	Y	CHx_FLT and CHAN_OCP_I2T_TSD	THERMAL_WRN_CHx	Y
I_{OCP} - Immediate shutdown		Y	Y	CHx_FLT and CHAN_OCP_I2T_TSD	ILIMIT_CHx	Y
I_{CL_REG} - Current limit regulation		Y	Y	N/A	N/A	N
I_{CL_REG} - Current limit regulation - inrush period expiry		Y	Y	CHx_FLT and CHAN_OCP_I2T_TSD	ILIMIT_CHx	Y
I_{CL_REG} - Current limit regulation - TSD		Y	Y	CHx_FLT and CHAN_OCP_I2T_TSD	ILIMIT_CHx and THERMAL_SD_CHx	Y
Channel in T_{RETRY} (LATCH_CHx = 0)		Y	N/A	N/A	FLT_CHx	Y
Channel is latched-off (LATCH_CHx = 1)		Y	N/A	N/A	LATCH_STAT_CHx and FLT_CHx	Y
Limp Home Entry (LHI = 1)		Y	N/A	GLOBAL_ERR_WRN and LIMPHOME_STAT	N/A	N
Active I2T Accumulation or Decrement		Y	N/A	N/A	I2T_MOD_CHx	N
I2T Shutdown		Y	Y	CHx_FLT and CHAN_OCP_I2T_TSD	I2T_FLT_CHx and FLT_CHx	Y
VOUT shorted to VBB		Y	N	CHx_FLT and OL_SHRT_VBB_OFF_FLT[1] (if OL_SVBB_EN_CHx = 01)	OL_OFF_CHx (if OL_SVBB_EN_CHx = 01)	Y, unless masked
Open load	Off State	Y	N	CHx_FLT and OL_SHRT_VBB_OFF_FLT (if OL_SVBB_EN_CHx=10)	OL_OFF_CHx (if OL_SVBB_EN_CHx=10)	Y, unless masked
	On State	Y	N	N/A	N/A	N
Reverse battery		Y	Y, with external components	N/A	N/A	N
VBB UV warning		Y	N	GLOBAL_ERR_WRN and VBB_UV_WRN	N/A	N
VBB_UVLO		Y	Y	GLOBAL_ERR_WRN and VBB_UVLO	N/A	Y
VDD_UVLO		Y	Y	GLOBAL_ERR_WRN and VDD_UVLO	N/A	N
Power on Reset (POR)		Y	Y	GLOBAL_ERR_WRN and POR	N/A	Y
Loss of GND		Y	Y, with R_{SDO} ≥ 768Ω	N/A	N/A	N
SPI Watchdog Error		Y	N/A	GLOBAL_ERR_WRN and WD_ERR (if WD_EN = 1)	N/A	Y, unless masked
SPI Frame Error		Y	N/A	GLOBAL_ERR_WRN and SPI_ERR	N/A	Y, unless masked
SPI CRC Error		Y	N/A	GLOBAL_ERR_WRN and SPI_ERR (if CRC_EN = 1)	N/A	Y, unless masked

7.3.5 SPI Mode Operation

The TPS481HS04-Q1 communicates with the host controller through a high-speed SPI serial interface. The interface has three logic inputs: clock (SCLK), chip select ($\overline{CS}$), serial data in (SDI), and one data out (SDO). The SDO is tri-stated when the $\overline{CS}$ pin is high. The maximum SPI clock rate is 8MHz, but is limited in practice by the series protection resistor.

The device supports simple daisy chain SPI. This mode can be used with or without CRC.

The communication between the TPS481HS04-Q1 IC and the controller or MCU is through a SPI bus in a primary-secondary configuration. The external MCU is always an SPI primary device that sends command requests on the SDI pin of the TPS481HS04-Q1 IC and receives device responses on the SDO pin of the IC. The TPS481HS04-Q1 device is always an SPI secondary device that receives command requests over the SDI line and sends responses (such as status and measured values) to the external MCU over the SDO line.

The TPS481HS04-Q1 device can be connected to the primary MCU in the following formats:

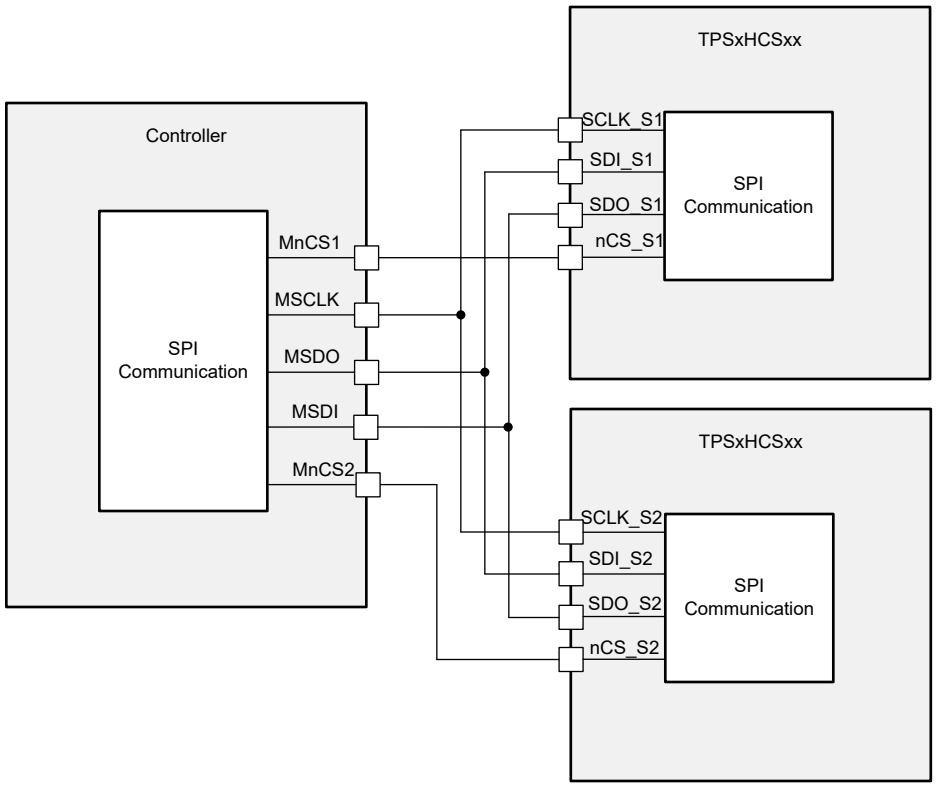

Figure 7-13. Independent Secondary Configuration (Separate $\overline{CS}$ Signal)

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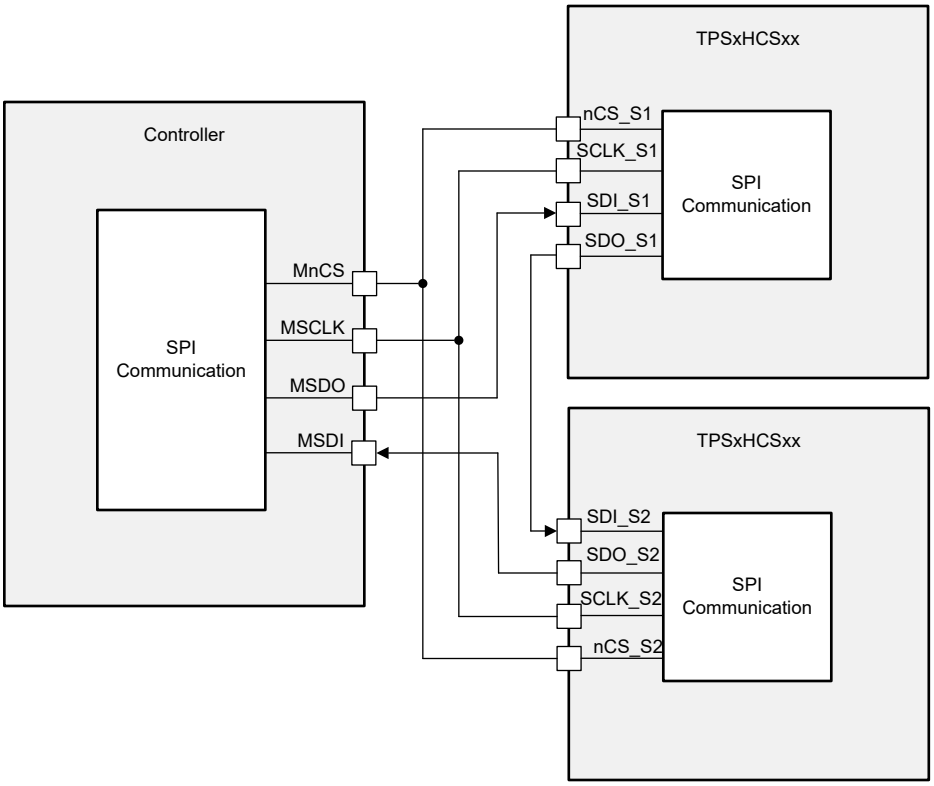

Figure 7-14. Daisy Chain Configuration

SPI interface

The SPI interface pin behavior is described in this section

Chip Select ($\overline{CS}$ or nCS)

The system microcontroller selects the TPS481HS04-Q1 to receive communication using the $\overline{CS}$ pin. With the $\overline{CS}$ pin in a logic LOW state, command/configuration words may be sent to the TPS481HS04-Q1 via the serial input (SDI) pin, and the device information can be retrieved by the microcontroller via the serial output (SDO) pin. The falling edge of the $\overline{CS}$ enables the SDO output and latches the content of the FAULT_GLOBAL register that will be sending out on SDO. The microcontroller may issue a READ command to retrieve information stored in the registers. The rising edge on the $\overline{CS}$ pin initiates the following actions:

1. Addressed registers are updated if there is no SPI communication error and if it is an SPI write command.
2. Read clear register is cleared if a READ command to this register was issued during CS = LOW.

To avoid any corrupted data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. A clean $\overline{CS}$ signal is needed to ensure no incomplete SPI words are sent to the device. This pin is internally pulled up to the VDD rail.

System Clock

The system clock (SCLK) pin clocks the internal shift register of the TPS481HS04-Q1. The SDI data is latched into the input shift register on the falling edge of the SCLK signal. The SDO pin shifts the device stored information out on the rising edge of SCLK. The SDO data is available for the microcontroller to read on the falling edge of SCLK.

False clocking of the shift register must be avoided to ensure validity of data and it is essential the SCLK pin be in a logic LOW state whenever $\overline{CS}$ pin makes any transition. Therefore, it is recommended that the SCLK pin

gets pulled to a logic LOW state as long as the device is not accessed and the $\overline{CS}$ pin is at a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SDI pins will be ignored and the SDO pin remains as a high impedance output.

Serial Data In (SDI) and Serial Data Out (SDO)

The SDI pin is used for serial instruction data input. SDI information is latched into the input shift register on the falling edge of the SCLK when $\overline{CS}$ is low.

The SDO pin is the output from the internal shift register. This pin is internally pulled up to the VDD rail. SDO pin is HiZ when the $\overline{CS}$ pin is high. Each successive **rising** SCLK edge makes the next data bit available for the microcontroller to read on the **falling** edge of SCLK. SDO will go back to high-impedance when $\overline{CS}$ is high.

CRC Error Detection and Checking of clocks

Setting the CRC_EN bit high enables CRC error detection. A CRC-4-ITU-Normal Check Sequence (FCS) is then sent along with each serial transaction. The 4-bit CRC is based on the normal generator polynomial X4+X+1 with CRC starting value = 1111. When CRC is enabled, the TPS481HS04-Q1 expects a check byte appended to the SDI program/configure data that it receives.

To program a complete word, exact bits of information (shown in following table) must be enter into the device. When CRC is disabled, the IC enables register write only if exactly bits have been clocked in. When CRC is enabled, the IC enables register write only if exactly bits have been clocked in with no CRC errors. In case the word length exceeds or does not meet the required length or there is CRC errors, the SPI_ERR bit in the FAULT_GLOBAL register is asserted to logic “1”,and the data received is considered invalid. Note the SPI_ERR bit is not flagged if SCLK is not present. The SPI_ERR will be sent back to SPI Main device on SDO during next chip access. **Note that clear on read applies only when there is no SPI error when the register is read.**

SPI Frame Format

The device uses a 24-bit frame width (when CRC is not used) with the format as shown in Figure 7-15. Please note that the 16-bit wide "Data Out" in the SDO output is always for the previous SPI command frame (Read or Write).

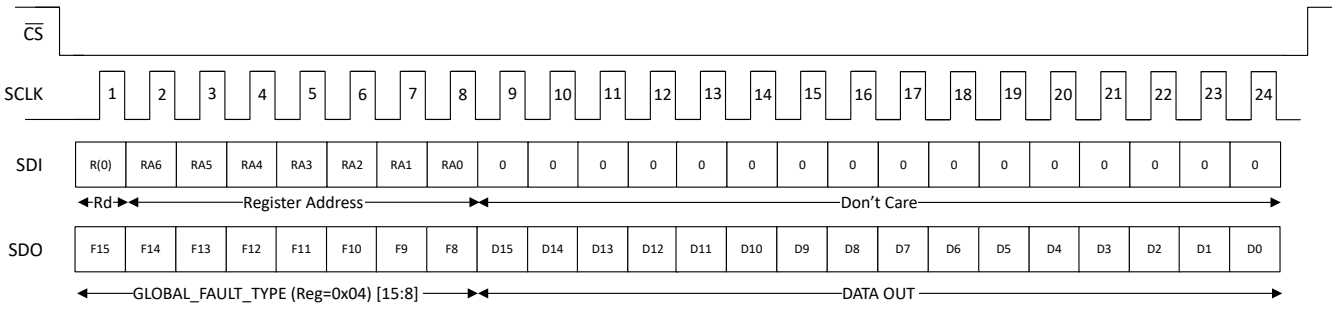

Figure 7-15. 24-Bit Read, No CRC (CRC_EN=0)

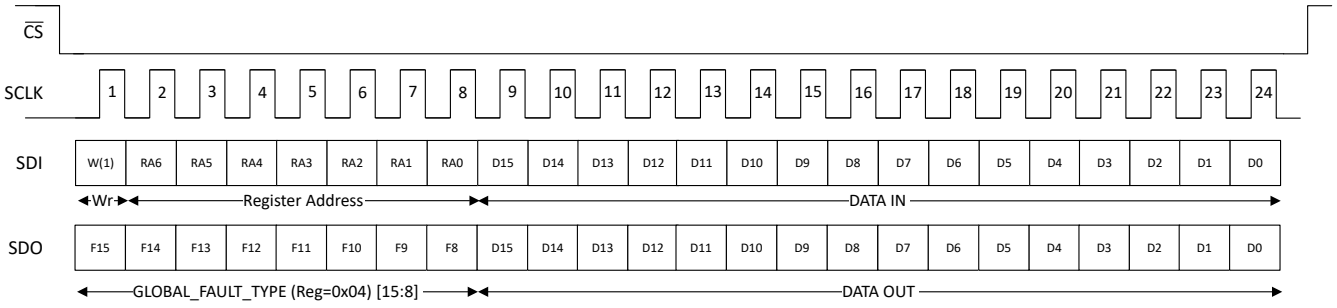

Figure 7-16. 24-Bit Write, No CRC (CRC_EN=0)

ADVANCE INFORMATION

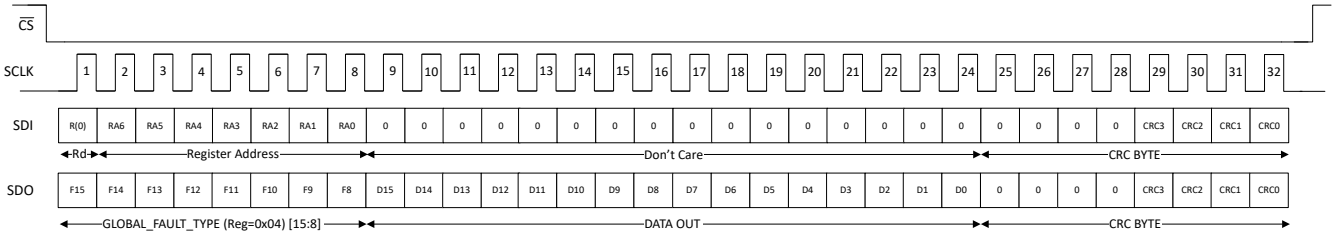

Figure 7-17. 32-Bit Read, CRC enabled (CRC_EN=1)

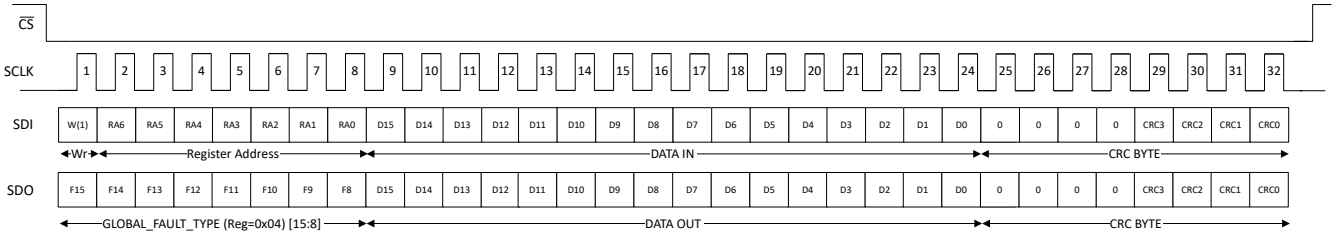

Figure 7-18. 32-Bit Write, CRC enabled (CRC_EN=1)

FAULT_GLOBAL [15:8] bits

The xx device, outputs the FAULT_GLOBAL [15:8] bits on the SDO header so these status bits can be continously read thr during each SPI transaction. The FAULT_GLOBAL [15:8] bits can be configured as read clear or real-time status bits based on the FLT_LTCH_DIS bit setting in the DEV_CONFIG register. The FLT_LTCH_DIS bit however does not apply to the LPM_STATUS bit.

If FLT_LTCH_DIS = 0, then the fault bits are latched and are cleared only when the associated regsiter in the bit description is read and the fault no longer exists. Table 7-4 below highlights which registers need to be read in order to clear each of the different fault bits if the fault no longer exists. This is also detailed in each of the bit descriptions in the register map.

Table 7-4. FAULT_GLOBAL [15:8] Bits Behavior When FLT_LTCH_DIS = 0

BIT	BIT NAME	REGISTER WHICH NEEDS TO BE READ TO CLEAR THE FAULT BIT IF THE FAULT NO LONGER EXISTS
15	Reserved	N/A
14	Reserved	N/A
13	CH2_FLT	FLT_STAT_CH2
12	CH1_FLT	FLT_STAT_CH1
10	CHAN_OCP_I2T_TSD	FLT_STAT_CHx
9	OL_SHRT_VBB_OFF_FLT	FLT_STAT_CHx
8	GLOBAL_ERR_WRN	FAULT_GLOBAL

If FLT_LTCH_DIS = 1, then the fault bits will clear when the fault no longer exists.

SPI Watchdog Function

The TPS481HS04-Q1 device offers an optional SPI watchdog function to monitor for valid SPI transactions from the host controller and loss of the VDD supply. If a valid SPI transaction does not occur in the configurable timeout period, WD_TO, then the FLT pin will go low unless masked and the WD_ERR bit in the FAULT_GLOBAL register will be set to 1. A valid SPI transaction consists of a SPI transaction with no SPI errors and/or CRC errors (if enabled). If the VDD supply to the device drops below the VDD_UVLO threshold then SPI on the device is not operational. If the VDD supply remains below the VDD_UVLO for longer than the watchdog time period, then the device will issue a watchdog error where the WD_ERR bit will be set to 1 and the FLT pin will go low unless masked.

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The watchdog function is enabled through WD_EN bit in the DEV_CONFIG register. Table 7-5 below showcases the different configurable watchdog timeout windows, WD_TO.

Table 7-5. Watchdog Timeout Settings

WD_TO SETTING	WATCHDOG TIMEOUT PERIOD
00	400µs
01	400ms
10	800ms
11	1200ms

If the watchdog function is enabled (WD_EN = 1) and a watchdog error occurs either do to no valid SPI transactions in the watchdog timeout window or due to a loss of VDD supply, WD_ERR = 1, FLT pin will go low unless masked, and the device will transition to the LIMPHOME mode where the output control of the channels will be set by the CHx_LH_IN bits in the DEV_CONFIG_CHx register. Note, the LIMPHOME_STAT bit will be set to 1 as a result of watchdog error. Once a valid SPI transaction has been detected, the $\overline{\text{FLT/WAKE}}$ pin will go high and the device will automatically exit the LIMPHOME mode and will revert the output control of the channel back to the CHx_ON bit. The WD_ERR bit in the FAULT_GLOBAL register will be latched to 1 as a result of a SPI watchdog timeout error and will be cleared only after read and the error no longer exists.

7.4 Device Functional Modes

7.4.1 State Diagram

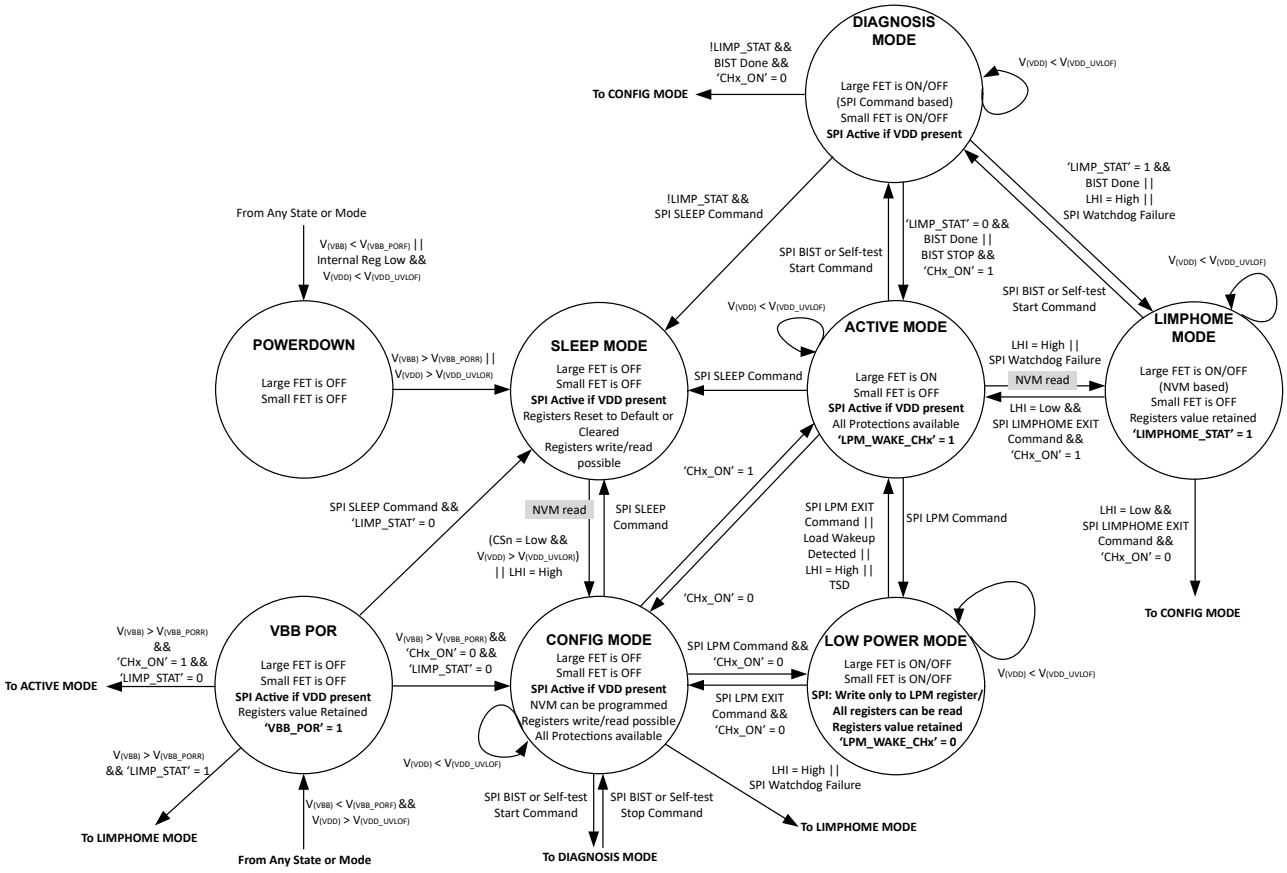

Figure 7-19. State Diagram

7.4.2 Power Down

If applied VBB voltage is below $V_{(VBB\_PORF)}$ and VDD is below $V_{(VDD\_PORF)}$ then the device is in disabled state. In this mode, the charge pump and all the protection features are disabled. The outputs are turned OFF.

7.4.3 SLEEP

The TPS481HS04-Q1 device offers a SLEEP mode where the device is placed into an ultra low current consumption state. When the device is in SLEEP mode, both channels are OFF, registers are cleared, and all digital circuits are powered off. The device will transition to this state if VBB < VBB_UVLO and VDD < VDD_UVLO. The device can manually be put into SLEEP mode by writing a 1 to the SLEEP bit in the SLEEP register.

The device can be woken from the SLEEP mode through the $\overline{CS}$ pin going low. There are two methods to wake the device up from SLEEP through the $\overline{CS}$ pin:

1. Pulse the $\overline{CS}$ pin low for $t < t_{READY}$
2. Hold the $\overline{CS}$ pin low for at least t_{READY} and continue to hold $\overline{CS}$ pin low through the first SPI transaction

Both methods above will result in the device waking up without a SPI_ERR fault. A dummy SPI transaction could be used to sastify method #1 if the dummy SPI transaction is completed in $t < t_{READY}$. Figure 7-20 below shows examples of the two proper wakeup scenarios which will result in no SPI_ERR fault and one improper wakeup scenario which will result in a SPI_ERR fault.

Upon wakeup from SLEEP mode, the values in the registers will be set to their reset values detailed in the register map below. Additionally, the $\overline{FLT/WAKE}$ pin will be asserted low and the POR, VDD_UVLO, and VBB_UVLO fault bits will be asserted and will be cleared when the FAULT_GLOBAL register is read if none of these faults currently exist when read.

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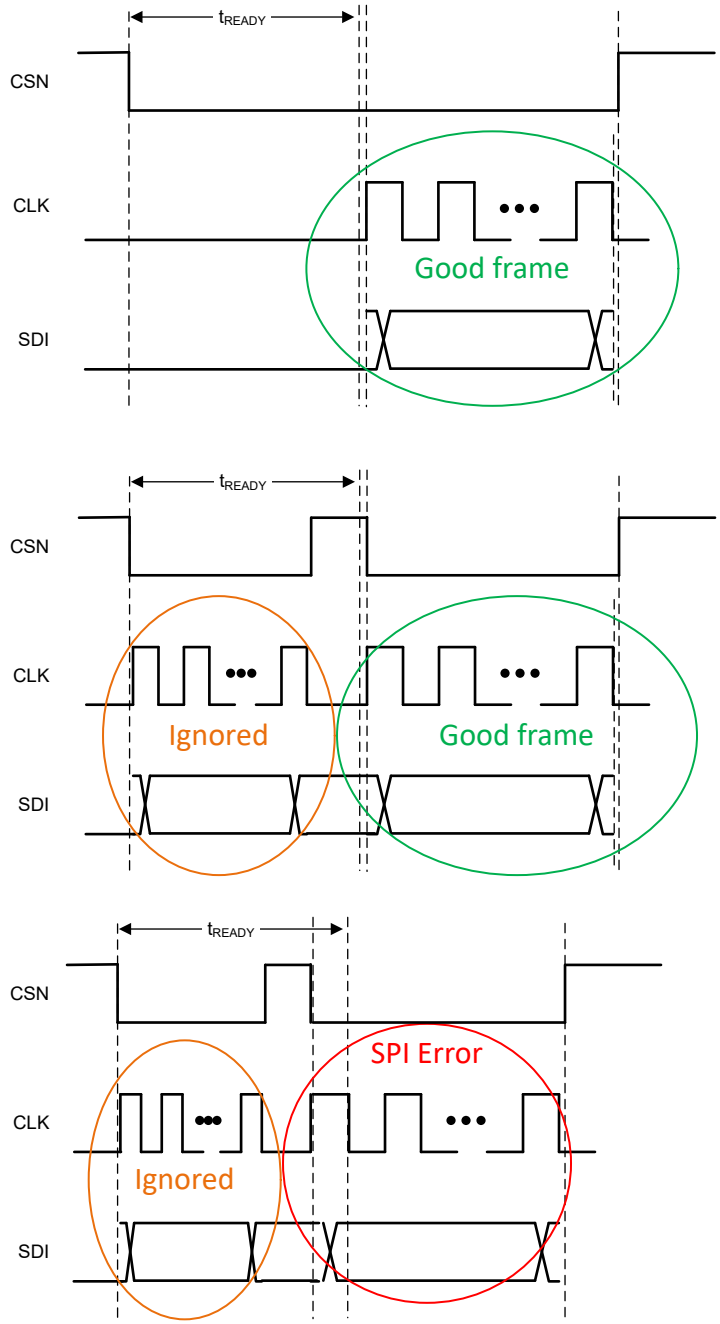

Figure 7-20. Startup Communication Timing

7.4.4 Low Power Mode (LPM)

The device transitions from ACTIVE to low power mode (LPM) whenever LPM_ENTRY bit is set to '1'. In LPM, charge pump is enabled with Large or small FET ON based on LPM_MODE bit in LPM register and $\overline{\text{FLT/WAKE}}$ pin asserted high in this mode.

The device features two types of loadwakeup mechanism described in subsequent sections

Automatic Low Power Mode (LPM) to Active Mode (AUTO_LPM_ENTRY = '0'):

When the device is in low power mode (LPM), LPM_STATUS bit is set '1'. The device transitions from LPM to active mode automatically whenever load current ($I_{CHx(LOAD)}$) exceeds load wakeup trigger threshold

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($I_{CHx(LWUx)}$) setting configured in LPM_EXIT_CURR_CHx. After load current exceeds load wakeup threshold, device automatically asserts $\overline{FLT/WAKE}$ pin low indicating the exit from the LPM. LPM_WAKE_CHx bit is also set to '1' in register map and LPM_STATUS bit is also reset to '0'.

AUTO LPM feature has to be disabled by resetting AUTO_LPM_ENTRY bit to '0'.

Automatic Low Power Mode (LPM) to Active Mode to LPM (AUTO LPM) for ECU polling (AUTO_LPM_ENTRY = '1'):

The TPS481HS04-Q1 has integrated AUTO LPM feature which can be enabled by AUTO_LPM_ENTRY bit in DEV_CONFIG_CHx register. AUTO LPM functionality provides flexibility for the device to automatically transition from active to a low IQ LPM while keeping power available to output at all times.

If AUTO_LPM_ENTRY bit is set to '1' and loadwakeup is detected by device ($I_{CHx(LOAD)}$ > $I_{CHx(LWUx)}$) then device starts internal timer ($t_{LPM\_WAKE\_DEGLITCH}$) based on LPM_WAKE_DEGLITCH timer setting in LPM register.

EVENT1: If ILOADx goes **below** $I_{EXIT\_LPM\_AUTO}$ within LPM_WAKE_DEGLITCH timer and ILOADx stays below $I_{EXIT\_LPM\_AUTO}$ threshold for AUTO_LPM_FILTER setting then device automatically transitions to LPM. $\overline{FLT}$ / $\overline{WAKE}$ is not asserted and remains high.

NOTE: It is recommended to set LPM_WAKE_DEGLITCH time more than loadwakeup current pulse time + AUTO_LPM_FILTER setting otherwise device will stay in active mode and not transition to LPM automatically.

EVENT2: If sensed ILOADx stays **above** $I_{EXIT\_LPM\_AUTO}$ within LPM_WAKE_DEGLITCH timer setting then device remains in active mode. $\overline{FLT/WAKE}$ is asserted low in order to indication WAKE to the MCU. MCU can reset LPM_ENTRY bit to '0' in order to de-assert the $\overline{FLT/WAKE}$ pin to high.

EVENT3: LPM_WAKE_DEGLITCH and AUTO_LPM_FILTER setting is only enabled when load wakeup is detected. These settings are disabled when $\overline{FLT/WAKE}$ is asserted low once.

Note

AUTO LPM feature is only availabe when LPM_MODE bit is set to 1 (Large FET LPM).

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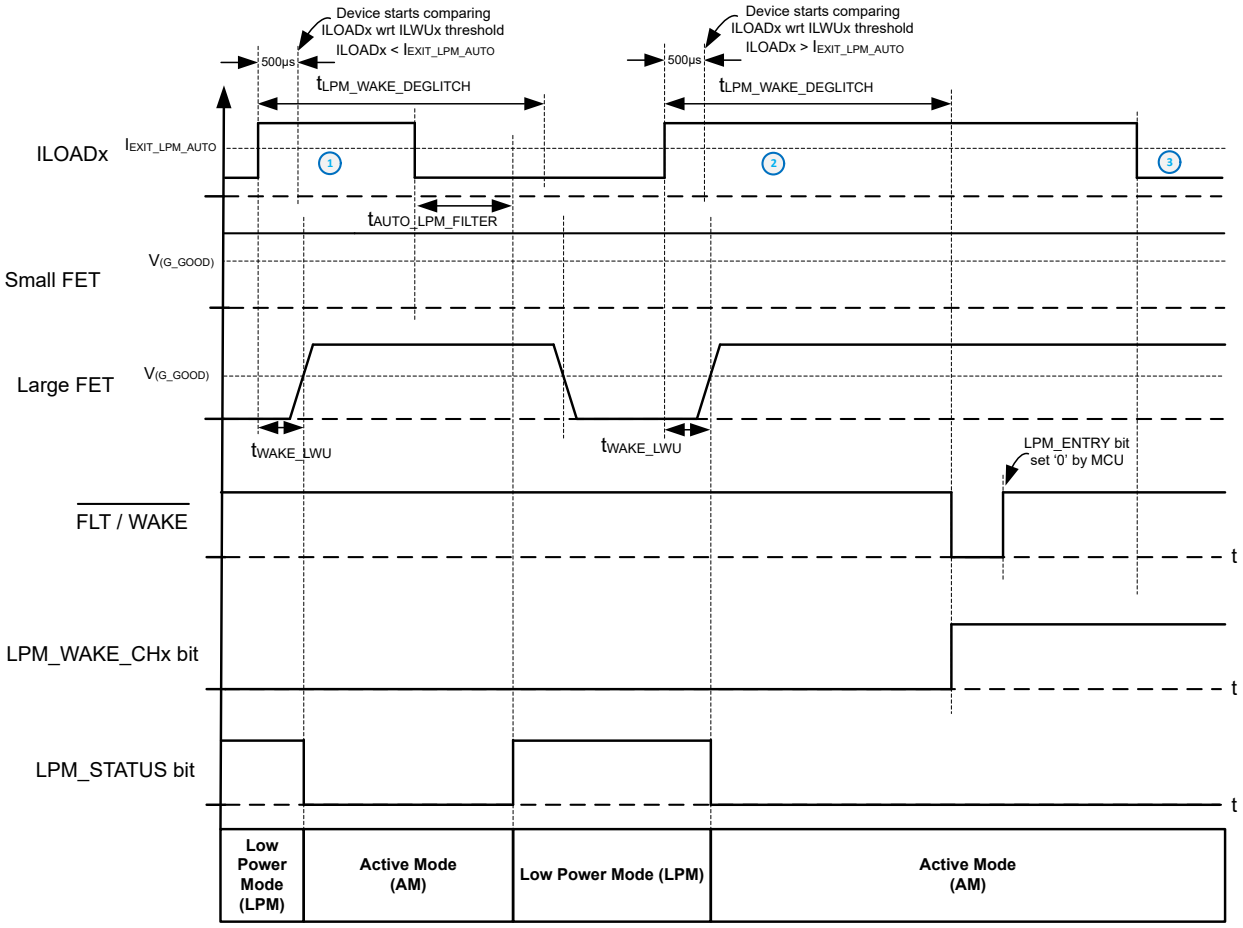

Figure 7-21. Timing Diagram For Loadwakeup With AUTO LPM Entry For ECU Polling

7.4.5 CONFIG or ACTIVE Mode

The CONFIG/ACTIVE state is where the device stays during normal operation when the outputs are OFF (CONFIG) or ON (ACTIVE). The difference between the two is that in the CONFIG state (with the outputs OFF) all of the registers can be configured. The configuration registers (especially ones needed for to successfully enable the channel) are expected to be written to before the outputs can be turned ON, when transitioning from the SLEEP mode (and all the registers are lost). However, the configuration registers are retained while in the LPM and so the device does not need to be reconfigured while tranisitioning from the LPM to the ACTIVE state. The quiescent current draw from VBB, (I_{QVBB}) and VDD, (I_{QVVD}) is higher than in the other states to support the load and device diagnostics. SPI communication and diagnostics checks are fully supported in this state.

7.4.6 LIMPHOME Mode

The device offers a LIMPHOME mode to set the outputs to a desired safe state (high, low, keep state, or according DIx) in case of a SPI communication failure, system level failure (i.e. car crash), or MCU failure (software or hardware). The device can be placed into the LIMPHOME mode through the following ways:

- LHI is pulled high
- Watchdog timeout error

The state of the output(s) in LIMPHOME are determined by the CHx_LH_IN bits. Depending on the DI_OUT_DIS_FN_CHx bit setting the CHx_LH_IN settings can vary. See the below tables for more details on this. See the Output Disable (OUT_DIS) Function section for more details on the DI_OUT_DIS_FN_CHx bit and OUT_DIS function.

ADVANCE INFORMATION

Table 7-6. CHx_LH_IN Bit Settings With DI_OUT_DIS_FN = 0

SETTING	SETTING DESCRIPTION
00	Output state is set by the DI pin when in LIMPHOME mode • If DI = HI, then CHx = ON in LIMPHOME mode • If DI = LO, then CHx = OFF in LIMPHOME mode
01	Keeps the same output state from CHx_ON bit when entering LIMPHOME mode
10	Output will be OFF in LIMPHOME mode
11	Output will be ON in LIMPHOME mode

Table 7-7. CHx_LH_IN Bit Settings With DI_OUT_DIS_FN = 1

SETTING	SETTING DESCRIPTION
00	Output will be OFF in LIMPHOME mode
01	Keeps the same output state from CHx_ON bit when entering LIMPHOME mode
10	Output will be OFF in LIMPHOME mode
11	Output will be ON in LIMPHOME mode

The register values are retained in the LIMPHOME mode. When the device enters LIMPHOME mode, the LIMPHOME_STAT bit in the FAULT_GLOBAL register is set high. In LIMPHOME mode, registers can be read but no write transactions can occur other than to clear the LIMPHOME_STAT bit in the FAULT_GLOBAL register to exit LIMPHOME mode. To clear the LIMPHOME_STAT bit, the LHI pin has to be low and a '1' has to be written to the LIMPHOME_STAT bit to clear the bit and to allow for the device to exit the LIMPHOME mode. Once the device exits LIMPHOME mode to ACTIVE mode, the device has full read/write access.

ADVANCE INFORMATION

7.5 TPS481HS04-Q1 Pre-production Silicon Limitations

PARAMETER	TEST CONDITION/EXPLANATION	OBSERVATION IN PRE-PRODUCTION SILICON	EXPECTED BEHAVIOR/TO BE IMPROVED IN PRODUCTION SILICON
Hot short	Output short to ground with Lin = 5uH and Lout = 5uH	Devices getting damaged.	Active clamp should demagnetize the inductance normally and switch should turn off. **It is not recommended to perform hot short to ground testing on pre-production silicon.**
SDO pin state	CSn pulled low to high	SDO retains LSB of last data value. Can't support parallel SPI interface.	SDO should be tri-state when CSn is pulled low to high.
GND Loss Detection	Device GND floating or high slew rate transient (10V/us) lifting GND pin >2V threshold	Switch turns off. Digital gets stuck (SPI Write doesn't work) because internal oscillator is susceptible to high slew rate on GND which can happen due to poor grounding or hot-swapping	The Switch should turn off. Switch should turn on automatically when GND is restored and SPI Write/Read works normally.

7.5.1 SDO Pin Tristate Discrete Workaround (Only for parallel SPI configuration not for daisy chain)

Figure 7-22 shows discrete NPN-PNP based circuit needed on SDO pin of each slave device when mutiple TPS481HS04-Q1 devices are used in parallel SPI configuration.

- $\overline{CS}$ goes low, Q1 turns on to connect master MCU with respective slave device SDO pin
- $\overline{CS}$ goes high, Q1 turns off disconnecting SDO pin of slave device from master MCU and SDO pins of other slave devices

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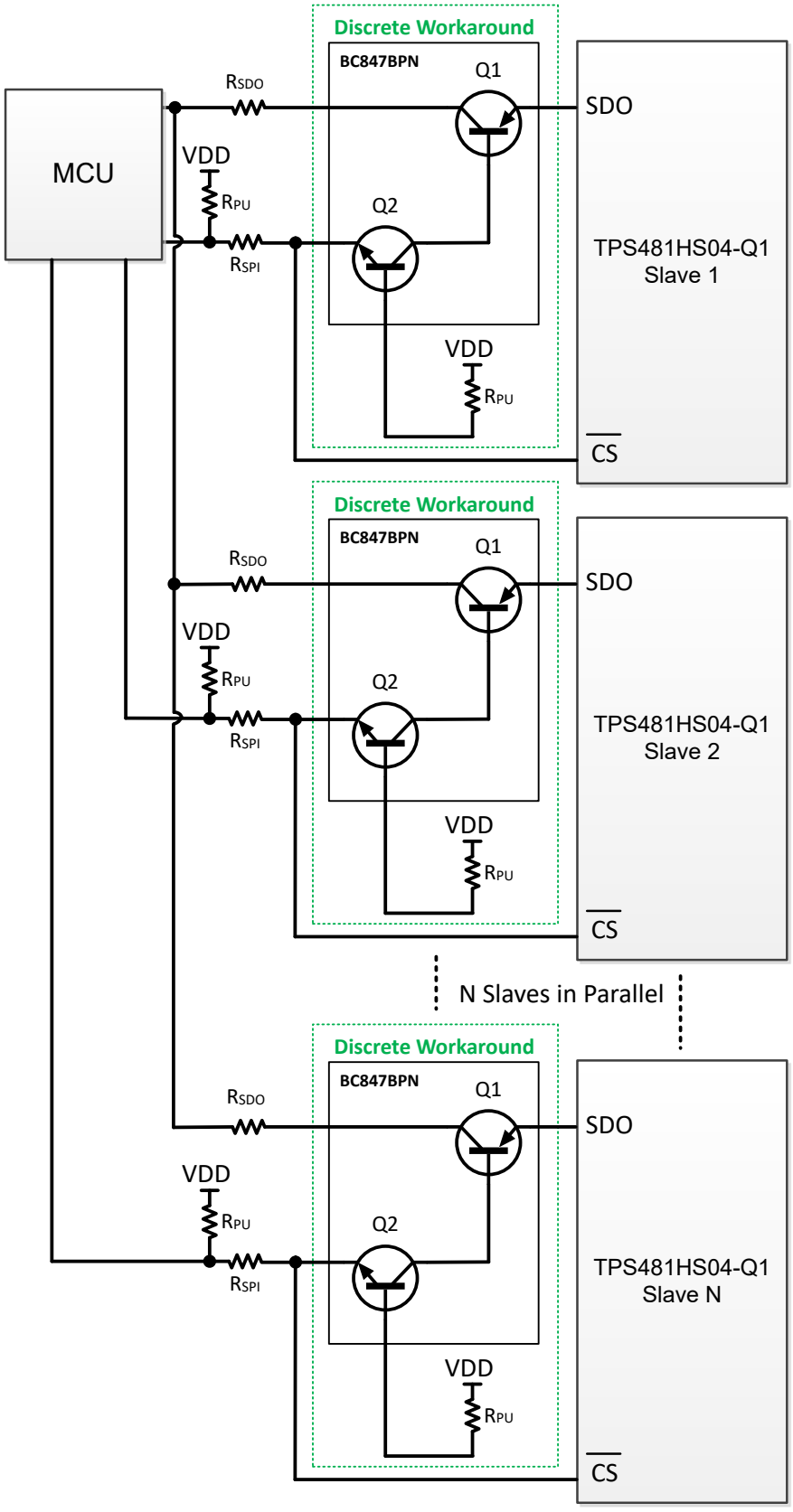

Figure 7-22. SDO Tri-State Discrete Workaround

8 Register Maps

Table 8-1. Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W0CP	W 0C P	W 0 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

ADVANCE INFORMATION

8.1 TPS481HS04-Q1 Registers

Table 8-2 lists the memory-mapped registers for the TPS481HS04-Q1 registers. All register offset addresses not listed in Table 8-2 should be considered as reserved locations and the register contents should not be modified.

Table 8-2. TPS481HS04-Q1 Registers

Offset	Acronym	Register Name	Section
0h	DEV_ID	Read the device ID from NVM	Section 8.1.1
1h	SLEEP	Sets to go into SLEEP sate from ACTIVE or STANDBY state	Section 8.1.2
2h	LPM	Sets to go in or out of Low power mode (LPM STATE)	Section 8.1.3
3h	FAULT_GLOBAL	Faults for any channel and global faults	Section 8.1.4
4h	FAULT_MASK	Mask the reporting of the faults on the fault pin	Section 8.1.5
5h	BIST_RESULT_CH1	BIST Diagnostic status result	Section 8.1.6
6h	SW_STATE	Turn on/off OUTx	Section 8.1.7
7h	DEVICE_TEST_CH1	Device BIST Setup	Section 8.1.8
8h	DEV_CONFIG	Device Configureable settings register	Section 8.1.9
9h	ADC_CONFIG	ADC configuration - disable ADC conversions or ADC entirely	Section 8.1.10
Ah	ADC_RESULT_VBB	ADC conversion result VBB	Section 8.1.11
Bh	ADC_RESULT_BIST	ADC and ISNS BIST conversion result	Section 8.1.12
Ch	FLT_STAT_CH1	Status of the channels and channel faults	Section 8.1.13
Dh	PWM_CH1	Set all PWM configurations for channel 1	Section 8.1.14
Eh	ILIM_CONFIG_CH1	Set all current limit configuration for channel 1	Section 8.1.15
Fh	DIAG_CONFIG_CH1	Configuration register for channel 1	Section 8.1.16
10h	ADC_RESULT_CH1_I	ADC conversion result load current sense CH1	Section 8.1.17
11h	ADC_RESULT_CH1_T	ADC conversion result TJ sense CH1	Section 8.1.18
12h	ADC_RESULT_CH1_V	ADC conversion result VOUT sense CH1	Section 8.1.19
14h	I2T_CONFIG_CH1	Set all I2T configuration bits	Section 8.1.20
1Eh	I2T_TRIP_CONFIG_CH1	I2T_TRIP configuration register for channel 1	Section 8.1.21
1Fh	I2T_ACC_RD_CH1	I2T_ACCUM % related to I2T_TRIP	Section 8.1.22
35h	IOCP_CONFIG_CH1	IOCP configuration for channel 1	Section 8.1.23
37h	UV_CONFIG	UVLO configuration for the device	Section 8.1.24
3Dh	DEV_CONFIG_2	Additional device configuration register	Section 8.1.25
3Fh	EEPROM_PROG	Customer EEPROM program control and status register	Section 8.1.26

Complex bit access types are encoded to fit into small table cells. Table 8-3 shows the codes that are used for access types in this section.

Table 8-3. TPS481HS04-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 DEV_ID Register (Offset = 0h) [Reset = 0000h]

DEV_ID is shown in Table 8-4.

Return to the Summary Table.

Table 8-4. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEVICE_ID	R	0h	Part Number These bits are NOT reprogrammable through EEPROM 1h = TPS481HS04-Q1 Pre-production Silicon

8.1.2 SLEEP Register (Offset = 1h) [Reset = FFFEh]

SLEEP is shown in Table 8-5.

Return to the Summary Table.

Table 8-5. SLEEP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-1	RESERVED	R	7FFFh	Reserved
0	SLEEP	R/W	0h	Set this bit to 1 to send the device to SLEEP state 0h = No change 1h = Sends the device to SLEEP state

8.1.3 LPM Register (Offset = 2h) [Reset = 3FCCh]

LPM is shown in Table 8-6.

Return to the Summary Table.

Table 8-6. LPM Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	LPM_WAKE_DEGLITCH	R/W	0h	Sets the Deglitch time for AUTO LPM exit from loadwakeup to FLT/ WAKEn signal assertion 0h = 1ms 1h = 10ms 2h = 20ms 3h = 100ms
13-12	RESERVED	R	3h	Reserved
11-10	RESERVED	R	3h	Reserved
9-8	RESERVED	R	3h	Reserved
7-6	RESERVED	R	3h	Reserved
5-4	LPM_EXIT_CURR_CH1	R/W	0h	Set the threshold to exit from LPM due to load current increase - CH1 Depending on the LPM_MODE setting the thresholds for the exit will be different. If LPM_MODE = 0, the thresholds are: 0h = 0.23A 1h = 0.47A 2h = 0.7A 3h = 0.93A If LPM_MODE = 1, the thresholds are: 0b00 = 1.66A 0b01 = 2.77A 0b10 = 3.88A 0b11 = 5A
3-2	RESERVED	R	3h	Reserved
1	LPM_MODE	R/W	0h	The bit determines if the large FET or small FET should be used for all channels when the device is in LPM Note: For AUTO LPM entry this bit has to be set to 1 0h = LPM Small FET mode - higher Rdson, lower exit threshold currents 1h = LPM Large FET mode - lower Rdson, higher exit threshold currents
0	LPM_ENTRY	R/W	0h	Setting this bit to 1 puts the device into LPM 0h = No change 1h = Enter LPM from ACTIVE / CONFIG mode

ADVANCE INFORMATION

8.1.4 FAULT_GLOBAL Register (Offset = 3h) [Reset = E147h]

FAULT_GLOBAL is shown in Table 8-7.

Return to the Summary Table.

Table 8-7. FAULT_GLOBAL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1h	Reserved
14	RESERVED	R	1h	Reserved
13	RESERVED	R	1h	Reserved
12	CH1_FLT	R	0h	Fault status of channel 1. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CH1 register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No fault(s) have occurred on CH1 1h = Fault(s) have occurred on CH1
11	LPM_STATUS	R	0h	The bit indicates if the device is in LPM mode and is cleared when the device is not in LPM mode. 0h = Device is not in LPM 1h = Device has entered LPM
10	CHAN_OCP_I2T_TSD	R	0h	This bit indicates if there is an overcurrent protection or I2T protection or thermal shutdown fault in any one of the channels. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FLT_STAT_CHx register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No overcurrent protection, I2T protection, or thermal shutdown fault in any of the channels 1h = Overcurrent protection, I2T protection, or thermal shutdown fault(s) in one or more channels
9	I2T_MOD	R	0h	This bit indicates if any of the channels are currently in I2T mode (I2T_MOD_CHx = 1) 0h = No channels are in I2T mode (I2T_MOD_CHx = 0) 1h = Channel(s) are in I2T mode (I2T_MOD_CHx = 1)
8	GLOBAL_ERR_WRN	R	1h	This bit indicates if there is a global fault reported in FAULT_GLOBAL[7:0] bits. The faults that are reported through this bit are LIMPHOME_STATE, POR, SPI_ERR, WD_ERR, VDD_UVLO, VBB_UV_WRN, or VBB_UVLO. If FLT_LTCH_DIS = 0, then the fault bit is latched and is cleared only when the FAULT_GLOBAL register is read and the fault condition(s) no longer exist If FLT_LTCH_DIS = 1, then the fault bit is cleared when the fault condition(s) no longer exist 0h = No global fault has occurred 1h = One of the following event(s) have occurred: LIMPHOME_STATE, POR, SPI_ERR, WD_ERR, VDD_UVLO, VBB_UV_WRN, or VBB_UVLO

ADVANCE INFORMATION

Table 8-7. FAULT_GLOBAL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	LIMPHOME_STAT	R	0h	This bit indicates if the device is in LIMPHOME mode as a result of the LHI pin going high. Write 1 to clear and exit LIMPHOME mode. The LHI pin must be LOW when the bit is set to 1 to exit LIMPHOME mode. 0h = Device is not in LIMPHOME mode 1h = Device is in LIMPHOME mode due to LHI pin going high or WD_ERR
6	POR	RC	1h	The bit is indicates if a power on reset (POR) has occurred since the last read This bit is cleared on read, so if read again and the bit is 0, this means that no power-on reset has occurred since the read. 0h = No power on reset (POR) has occured since the last register read 1h = A power-on reset has occurred since the last register read.
5	LPM_STATUS_LATCH	RC	0h	This bit indicates if the device is in either LPM. 0h = Device is not in the LPM 1h = Device has entered LPM
4	SPI_ERR	RC	0h	This bit indicates if there is a SPI communication error either from format, clock or CRC. The fault bit is latched and cleared only after read and the error(s) no longer exist. 0h = No SPI communication error(s) fault have occurred 1h = SPI communication error either from format, clock or CRC has occurred
3	WD_ERR	RC	0h	If WD_EN = 1, this bit indicates if there has not been an acceptable SPI command in the watchdog timeout window. The fault bit is latched and cleared only after read and the error no longer exists 0h = No SPI interface watchdog error 1h = SPI watchdog timeout error has occurred
2	VDD_UVLO	RC	1h	This bit indicates if the VDD supply is below VDD_UVLOF at any time. The fault bit is cleared if the FAULT_GLOBAL register is read and the UVLO condition is removed 0h = No VDD_UVLO fault has occurred 1h = VDD_UVLO fault has occurred
1	VBB_UV_WRN	RC	1h	This bit indicates if the VBB supply is below the $V_{BB\_UV\_WRN}$ at any time. If VBB is below $V_{BB\_UV\_WRN}$, the diagnostics in the device are turned off The fault bit is cleared if the FAULT_GLOBAL register is read and the UV condition no longer exists 0h = No VBB_UV_WRN fault has occurred 1h = VBB_UV_WRN fault has occurred
0	VBB_UVLO	RC	1h	This bit indicates if the VBB supply is below the V_{BB_UVLOF} at any time. The fault bit is cleared if the FAULT_GLOBAL register is read and the UVLO condition is removed 0h = No VBB_UVLO fault has occurred 1h = VBB_UVLO fault has occurred

ADVANCE INFORMATION

8.1.5 FAULT_MASK Register (Offset = 4h) [Reset = C000h]

FAULT_MASK is shown in Table 8-8.

Return to the Summary Table.

Table 8-8. FAULT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	3h	Reserved
13	MASK_CPUMP_UVLO	R/W	0h	This bit determines if the device should mask the signaling of a CPUMP UVLO fault on the FLT pin 0h = CPUMP UVLO Fault is signaled on the FLT pin on fault occuring 1h = CPUMP UVLO fault is not signaled (masked from) on the FLT pin
12	MASK_FET_SHORT	R/W	0h	This bit determines if the device should mask the signaling of a FET Short BIST fault on the FLT pin 0h = Fet Short Fault is signaled on the FLT pin on fault occuring 1h = Fet Short fault is not signaled (masked from) on the FLT pin
11	MASK_LPM_HS	R/W	0h	This bit determines if the device should mask the signaling of a LPM Hard Short protection fault on the FLT pin 0h = LPM Hard Short Fault is signaled on the FLT pin on fault occuring 1h = LPM Hard Short fault is not signaled (masked from) on the FLT pin
10	MASK_NVM_CRC_ERR	R/W	0h	This bit determines if the device should mask the signaling of a NVM_CRC_ERR fault on the FLT pin 0h = NVM_CRC_ERR Fault is signaled on the FLT pin on fault occuring 1h = NVM_CRC_ERR fault is not signaled (masked from) on the FLT pin
9	MASK_I2T_TRIP	R/W	0h	This bit determines if the device should mask the signaling of an I2T fault on the FLT pin 0h = I2T Fault is signaled on the FLT pin on I2T Trip protection fault occuring 1h = I2T Trip Protection fault is not signaled (masked from) on the FLT pin
8	MASK_VDD_UVLO	R/W	0h	This bit determines if the device should mask the supply voltage VDD UVLO fault on the FLT pin 0h = VDD UV fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = VDD UV fault is not signaled (masked from) on the FLT pin
7	MASK_IOCP	R/W	0h	This bit determines if the device should mask the signaling of an immediate shutdown overcurrent protection (I_{OCP}) fault on the FLT pin 0h = Fault is signaled on the FLT pin on IOCP protection fault occuring 1h = SCP / CB Protection fault is not signaled (masked from) on the FLT pin
6	MASK_ILIM	R/W	0h	This bit determines if the device should mask the signaling of current limit regulation (I_{CL_REG}) on the FLT pin when CAP_CHRG_CHx = 10 is used 0h = Fault is signaled on the FLT pin on ILIM fault occuring 1h = ILIM fault is not signaled (masked from) on the FLT pin
5	MASK_SHRT_VBB	R/W	0h	This bit determines if the device should mask the signaling of an off-state short-to-battery fault on the FLT pin 0h = Short to VBB Fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = Short to VBB fault is not signaled (masked from) on the FLT pin

Table 8-8. FAULT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	MASK_OL_OFF	R/W	0h	This bit determines if the device should mask the signaling of an off-state open load fault on the FLT pin 0h = Off-state wire-break fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = Off-state wire-break fault is not signaled (masked from) on the FLT pin
3	MASK_TSD	R/W	0h	This bit determines if the device should mask the signaling of a TSD fault on the FLT pin 0h = Fault is signaled on the FLT pin on TSD protection fault occuring 1h = TSD Protection fault is not signaled (masked from) on the FLT pin
2	MASK_SPI_ERR	R/W	0h	This bit determines if the device should mask a SPI error (SPI_ERR) on the FLT pin and in the FAULT_GLOBAL register 0h = SPI error is signaled in FAULT_TYPE_STAT register and FLT pin 1h = FAULT_TYPE_STAT register and FLT pin not impacted by SPI error
1	MASK_WD_ERR	R/W	0h	This bit determines if the device should mask a SPI watchdog error (WD_ERR) on the FLT pin and in the FAULT_GLOBAL register 0h = SPI watchdog error is signaled in FAULT_TYPE_STAT register and FLT pin 1h = FAULT_TYPE_STAT register and FLT pin not impacted by SPI watchdog error
0	MASK_VBB_UVLO	R/W	0h	This bit determines if the device should mask the supply voltage VBB UVLO fault on the FLT pin 0h = VBB UV fault is signaled on the FLT pin on detecting the fault with the diagnostic 1h = VBB UV fault is not signaled (masked from) on the FLT pin

ADVANCE INFORMATION

8.1.6 BIST_RESULT_CH1 Register (Offset = 5h) [Reset = 7D88h]

BIST_RESULT_CH1 is shown in Table 8-9.

Return to the Summary Table.

Table 8-9. BIST_RESULT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIST_FORCED_EXIT	RC	0h	The bit is set to 1 if any of the BISTs exited due to abnormal forced condition, it gets cleared once BIST_RESULT register is read and no more abnormal exit happens 0h = BIST did not exit early 1h = One or more BIST exited early
14	RESERVED	R	1h	Reserved
13	RESERVED	R	1h	Reserved
12	RESERVED	R	1h	Reserved
11	RESERVED	R	1h	Reserved
10	RESERVED	R	1h	Reserved
9	UV_BIST_ERR	RC	0h	This bit indicates if the UVLO BIST passed or failed 0h = BIST for UVLO Passed 1h = BIST for UVLO Failed
8	RESERVED	R	1h	Reserved
7	RESERVED	RC	1h	Reserved
6	TSD_BIST_ERR_CH1	RC	0h	This bit indicates if the TSD BIST for CH1 passed or failed 0h = BIST for TSD CH1 Passed 1h = BIST for TSD CH1 Failed
5	IOCP_BIST_ERR_CH1	RC	0h	This bit indicates if the IOCP BIST for CH1 passed or failed 0h = BIST for IOCP CH1 Passed 1h = BIST for IOCP CH1 Failed
4	OTP_CRC_ERR	R	0h	This bit indicates if the NVM CRC passed or failed 0h = CRC check for EEPROM NVM Passed 1h = CRC check for EEPROM NVM Failed
3	RESERVED	R	1h	Reserved
2	FET_SHORT_BIST_ERR_CH1	RC	0h	This bit indicates if the FET SHORT BIST for CH1 passed or failed 0h = BIST for FET short CH1 Passed 1h = BIST for FET short CH1 Failed
1	ADC_BIST_ERR	RC	0h	This bit indicates if the ADC BIST passed or failed 0h = BIST for ADC Passed 1h = BIST for ADC Failed
0	BG_BIST_ERR	RC	0h	This bit indicates if the BG BIST passed or failed 0h = BIST for BG Passed 1h = BIST for BG Failed

ADVANCE INFORMATION

8.1.7 SW_STATE Register (Offset = 6h) [Reset = EEEEh]

SW_STATE is shown in Table 8-10.

Return to the Summary Table.

Table 8-10. SW_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	1h	Reserved
14	RESERVED	R	1h	Reserved
13	RESERVED	R	1h	Reserved
12	SWEN_S_CH1	R	0h	This bit indicates the status of the SWEN of the CH1 Small FET 0h = CH1 SFET SWEN is Low 1h = CH1 SFET SWEN is High
11	RESERVED	R	1h	Reserved
10	RESERVED	R	1h	Reserved
9	RESERVED	R	1h	Reserved
8	SW_STATE_M_CH1	R	0h	This bit indicates the status of the VGS of the CH1 Large FET 0h = CH1 LFET VGS Comp is Low 1h = CH1 LFET VGS Comp is High
7	RESERVED	R	1h	Reserved
6	RESERVED	R	1h	Reserved
5	RESERVED	R	1h	Reserved
4	SWEN_M_CH1	R	0h	This bit indicates the status of the SWEN of the CH1 Large FET 0h = CH1 LFET SWEN is Low 1h = CH1 LFET SWEN is High
3	RESERVED	R	1h	Reserved
2	RESERVED	R	1h	Reserved
1	RESERVED	R	1h	Reserved
0	CH1_ON	R/W	0h	This bit determines the output state of channel 1 0h = CH1 Output set to OFF (FET is OFF) 1h = CH1 Output set to ON (FET is ON)

8.1.8 DEVICE_TEST_CH1 Register (Offset = 7h) [Reset = 7D18h]

DEVICE_TEST_CH1 is shown in Table 8-11.

Return to the Summary Table.

Table 8-11. DEVICE_TEST_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BIST_CTRL_CHECK	R/W	0h	This bit determines if the FET should turn off when the BIST passes for the I2T, IOCP, UV, and TSD BISTs to test the logic and gate driver circuitry 0h = FET does not turn off if relevant BIST passes 1h = FET turns off if relevant BIST passes
14-13	RESERVED	R/W	3h	Reserved
12	RESERVED	R	1h	Reserved
11	RESERVED	R	1h	Reserved
10	RESERVED	R	1h	Reserved
9	UV_BIST_RUN	R/W	0h	This bit runs the UVLO_BIST and updates the UV_BIST_ERR bit in the BIST_RESULT register with the pass or fail result. This bit is reset back to 0 after the BIST has been run 0h = UV BIST is not running 1h = UV BIST is running
8	RESERVED	R	1h	Reserved
7	TSD_BIST_RUN	R/W	0h	This bit runs the TSD BIST and updates the TSD_BIST_ERR_CH1 bit in the BIST_RESULT register with the pass or fail result. This bit is reset back to 0 after the BIST has been run 0h = TSD BIST is not running 1h = TSD BIST is running
6	I2T_BIST_RUN_CH1	R/W	0h	This bit runs the I2T BIST for channel 1 and updates the I2T_BIST_ERR_CH1 bit in the BIST_RESULT register with the pass or fail result. This bit is reset back to 0 after the BIST has been run 0h = CH1 I2T BIST is not running 1h = CH1 I2T BIST is running
5	SCP_BIST_RUN_CH1	R/W	0h	This bit runs the IOCP BIST for channel 1 and updates the IOCP_BIST_ERR_CH1 bit in the BIST_RESULT register with the pass or fail result. This bit is reset back to 0 after the BIST has been run 0h = CH1 IOCP BIST is not running 1h = CH1 IOCP BIST is running
4	ISNS_BIST_RUN	R/W	1h	This bit runs the ISNS BIST for channel 1 and updates the results in the ADC_RESULT_BIST register. This bit is reset back to 0 after the BIST has been run. Note: The ISNS BIST cannot be run when the device is in the I2T loop (I2T_MOD_CHx = 1) or if there is an active overcurrent or thermal fault condition. . 0h = ISNS BIST is not running 1h = ISNS BIST is running
3	RESERVED	R	1h	Reserved
2	FET_SHORT_BIST_RUN_CH1	R/W	0h	Run the BIST diagnostics for the CH1 FET short failure and update the BIST_RESULT register with the result. Reset bit back to 0 after BIST has been run 0h = BIST for CH1 FET short detection is not running 1h = BIST for CH1 FET short detection is running

Table 8-11. DEVICE_TEST_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	ADC_BIST_RUN	R/W	0h	This bit runs the ADC BIST for channel 1 and updates the results in the ADC_RESULT_BIST register. This bit is reset back to 0 after the BIST has been run. Note: The ADC BIST cannot be run when the device is in the I2T loop (I2T_MOD_CHx = 1) or if there is an active overcurrent or thermal fault condition. . 0h = ADC BIST is not running 1h = ADC BIST is running
0	BG_BIST_RUN	R/W	0h	This bit runs the bandgap BIST diagnostic and updates the BG_BIST_ERR bit in the BIST_RESULT register with the pass or fail result. This bit is reset back to 0 after the BIST has been run 0h = Bandgap BIST is not running 1h = Bandgap BIST is running

ADVANCE INFORMATION

8.1.9 DEV_CONFIG Register (Offset = 8h) [Reset = 7E00h]

DEV_CONFIG is shown in Table 8-12.

Return to the Summary Table.

Table 8-12. DEV_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CRC_EN	R/W	0h	Set this bit to 1 to enable CRC check of SPI command frame. 0h = No CRC check of SPI command frame 1h = CRC check of SPI command frame enabled
14-13	RESERVED	R	3h	Reserved
12-11	RESERVED	R	3h	Reserved
10-9	RESERVED	R	3h	Reserved
8-7	CH1_LH_IN	R/W	0h	These bits determine how the channel 1 output should respond in LIMPHOME mode. If DI_OUT_DIS_FN_CH1 = 0, the values are: 0h = DI pin controls the output when in LIMPHOME mode 1h = Keeps the same output state from CH1_ON bit when entering LIMPHOME mode 2h = Output will be OFF in LIMPHOME mode 3h = Output will be ON in LIMPHOME mode If DI_OUT_DIS_FN_CH1 = 1, the values are: 0h = Output will be OFF in LIMPHOME mode 1h = Keeps the same output state from CH1_ON bit when entering LIMPHOME mode 2h = Output will be OFF in LIMPHOME mode 3h = Output will be ON in LIMPHOME mode
6	LIMPHOME_CONFIG	R/W	0h	Set this bit to enable the reloading of NVM values into the register upon entering into LIMPHOME mode configuration. 0h = Register values in LIMPHOME mode is retained 1h = Register values are reloaded from NVM during Limphome mode transition
5	AUTO_LPM_ENTRY	R/W	0h	Set this bit to 1 to enable the AUTO LPM mode when the LPM_ENTRY bit is set to 1. 0h = Entry into AUTO LPM mode is disabled 1h = Entry into AUTO LPM mode is enabled and the device enters if the LPM_ENTRY bit is set to 1
4	AUTO_LPM_FILTER	R/W	0h	This bit sets the deglitch time for when the device will re-enter AUTO LPM if all the conditions are met to enter AUTO LPM 0h = 1ms 1h = 100µs
3	WD_EN	R/W	0h	The bit determines if the SPI watchdog function is enabled. If enabled, the watchdog timout triggers if there is not a valid SPI command in the watchdog timeout window 0h = Watchdog is disabled 1h = Watchdog function is enabled
2-1	WD_TO	R/W	0h	This bit determines the timeout period for the SPI watchdog function (if enabled). The watchdog timeout triggers if there is not a valid SPI command in the watchdog timeout window. 0h = Watchdog timeout period is 400µs 1h = Watchdog timeout period is 400ms 2h = Watchdog timeout period is 800ms 3h = Watchdog timeout period is 1200ms

Table 8-12. DEV_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	FLT_LTCH_DIS	R/W	0h	This bit determines if the fault bits in FAULT_GLOBAL [13:8] should latch if a fault occurs. 0h = Fault bits [13:8] in FAULT_GLOBAL register latched and cleared only on read of the associated register 1h = Fault bits [13:8] in FAULT_GLOBAL register are not latched and are cleared when the fault no longer exists Note: See each fault bit description for more details on how to clear the individual fault bits when FLT_LTCH_DIS = 0. LPM_STATUS is read only.

ADVANCE INFORMATION

8.1.10 ADC_CONFIG Register (Offset = 9h) [Reset = FD3Ah]

ADC_CONFIG is shown in Table 8-13.

Return to the Summary Table.

Table 8-13. ADC_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	3Fh	Reserved
9	ADC_I2T_CONFIG_MODE	R/W	0h	This bit determines if VSNS is still converted if any of the channels are in I2T accumulation mode (I2T_MOD_CHx = 1). 0h = Only ISNS will be sampled per channel in I2T Mode 1h = ISNS and VOUT both sampled per channel in I2T Mode
8	RESERVED	R	1h	Reserved
7-6	ADC_CONFIG_DELAY	R/W	0h	These bits set the delay time between successive round robin loops to reduce the device IQ due the ADC operation. 0h = 0µs 1h = 100µs 2h = 200µs 3h = 400µs
5	RESERVED	R	1h	Reserved
4	ADC_VSNS_DIS	R/W	1h	This bit determines if the VOUT sense (VSNS) funciton should be disabled for all channels. If disabled, this excludes the VOUT conversion for all channels in the ADC conversion sequence. Note: The VSNS function can also be enabled or disabled per channel through the VSNS_DIS_CHx bit in the CHx_CONFIG register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = VSNS ADC function is enabled 1h = VSNS ADC functionality is disabled for all channels, VSNS ADC conversion is excluded in the ADC conversion sequence for all channels
3	ADC_TSNS_DIS	R/W	1h	This bit determines if the temperature sense function is disabled for all channels. If disabled, this excludes the temperature sense conversion for all channels in the ADC conversion sequence. Note: The temperature sense function can only be enabled or disabled globally 0h = TSNS ADC function is enabled 1h = TSNS ADC functionality is disabled for all channels, TSNS ADC conversion is excluded in the ADC conversion sequence for all channels
2	ADC_ISNS_DIS	R/W	0h	This bit determines if the current sense (ISNS) function is disabled for all channels. If disabled, this excludes the ISNS conversion for all channels in the ADC conversion sequence Note: The ISNS function can also be enabled or disabled per channel through the ISNS_DIS_CHx in the CHx_CONFIG register. This bit must be set to 0 to enable/disable the function on a channel basis. 0h = ISNS ADC function is enabled 1h = ISNS ADC functionality is disabled for all channels, ISNS ADC conversion is excluded in the ADC conversion sequence for all channels
1	ADC_VBB_DIS	R/W	1h	This bit determines if the VBB_SNS function is disabled. If disabled, this excludes supply voltage VBB conversion in the ADC conversion sequence. 0h = VBB_SNS ADC function is enabled, VBB_SNS ADC conversion is included in the ADC conversion sequence 1h = VBB_SNS ADC function is disabled, VBB_SNS ADC conversion is excluded in the ADC conversion sequence

ADVANCE INFORMATION

Table 8-13. ADC_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADC_DIS	R/W	0h	This bit determines if the ADC function should be disabled. If disabled, no VDS_SNS, VSNS, TSNS, or ISNS is possible. The ADC is enabled by default. 0h = ADC function enabled 1h = All ADC functions disabled

8.1.11 ADC_RESULT_VBB Register (Offset = Ah) [Reset = F800h]

ADC_RESULT_VBB is shown in Table 8-14.

Return to the Summary Table.

Table 8-14. ADC_RESULT_VBB Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VBB_RDY	R	0h	This bit indicates if a new ADC result for VBB voltage conversion is available since the last read 0h = VBB ADC value not updated 1h = New VBB ADC value ready since last read
9-0	ADC_RESULT_VBB	R	0h	10-bit ADC result from the conversion of the VBB voltage

8.1.12 ADC_RESULT_BIST Register (Offset = Bh) [Reset = F000h]

ADC_RESULT_BIST is shown in Table 8-15.

Return to the Summary Table.

Table 8-15. ADC_RESULT_BIST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	3h	Reserved
13-12	RESERVED	R	3h	Reserved
11	ADC_ISNS_BIST	RC	0h	This bit will indicate whether ISNS or ADC BIST result is being rerported in the ADC RESULT_BIST register 0h = ADC BIST value is being reported 1h = ISNS BIST value is being reported
10	BIST_RESULT_RDY	R	0h	This bit indicates if a new BIST result conversion is available since the last read 0h = BIST ADC Value not updated 1h = New BIST ADC balue ready since last read
9-0	ADC_RESULT_BIST	R	0h	10-bit ADC result from the conversion of the BIST

ADVANCE INFORMATION

8.1.13 FLT_STAT_CH1 Register (Offset = Ch) [Reset = C000h]

FLT_STAT_CH1 is shown in Table 8-16.

Return to the Summary Table.

Table 8-16. FLT_STAT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	3h	Reserved
13	IOCP_CH1	RC	0h	This bit indicates if an immediate shutdown overcurrent protection (I_{OCP}) fault has occurred on channel 1 The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = No immediate shutdown overcurrent protection fault has occurred on this channel 1h = Immediate shutdown overcurrent protection fault has occurred on this channel
12	I2T_MOD_CH1	R	0h	This bit indicates if channel 1 in the I2T loop and is accumulating. When channel 1 is not in the I2T loop the value will be 0 0h = I2T is off or the channel is not in the I2T loop 1h = Channel is in the I2T loop and is accumulating
11	LATCH_STAT_CH1	RC	0h	This bit indicates if channel 1 has been latch off due to an overcurrent protection, thermal shutdown, or I2T fault. The bit clears when the channel is toggled off and back on. 0h = Channel is not latched off 1h = Channel is currently latched off
10	FLT_CH1	R	0h	This bit indicates if an active fault is still occuring on the channel or the device is in retry time interval or latch off state for I2T, IOCP, or thermal shutdown faults. 0h = This channel does not have an active fault and is not in auto retry wait time, latch off state, or I2T cooldown 1h = This channel has an active fault or is in auto retry wait time, latch off state, or I2T cooldown
9	LPM_HS_CH1	RC	0h	This bit indicates if $I_{SCP\_LPM\_x}$ has been triggered. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = LPM short circuit protection was not triggered
8	VOUT_ERR_CH1	R	0h	This bit indicates if the drain-to-source voltage (V_{DS}) of channel 1 < $V_{DS\_LT\_2V}$ after the channel is enabled and is out of the inrush period (if configured) for t > t_{VDS_DEGL}. 0h = The VDS voltage is correct (< 2V) when this channel is enabled 1h = The VDS voltage is incorrect (>2V) when this channel is supposed to be enabled
7	I2T_FLT_CH1	RC	0h	This bit indicates if an I2T fault has occured on channel 1. I2T_EN must be set to 1 in order for this bit indicate an I2T fault. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists Note: This bit does not indicate an overcurrent protection or thermal shutdown fault 0h = no I2T fault has occurred or I2T is not enabled 1h = I2T fault has occurred on this channel
6	LPM_WAKE_CH1	R	0h	This bit indicates if channel 1 was the cause for the device to come out of LPM regardless of the cause (load step, short-circuit) 0h = The device was not in LPM or this channel was not the cause the device came out of LPM 1h = This channel was the reason the device came out of LPM

Table 8-16. FLT_STAT_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	THERMAL_SD_CH1	RC	0h	This bit indicates if thermal shutdown fault has occurred on channel 1. The fault is latched and cleared when the FLT_STAT_CH1 register is read and the retry timer has expired and the channel temperature has fallen below the thermal shutdown hysteresis threshold 0h = No thermal shutdown fault has occurred on this channel 1h = A thermal shutdown fault has occurred on this channel
4	ILIMIT_CH1	RC	0h	This bit indicates if an overcurrent protection fault has occurred on channel 1 The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = No overcurrent protection fault has occurred on this channel 1h = Overcurrent protection fault has occurred on this channel
3	SHRT_VBB_CH1	RC	0h	This bit indicates if there was a short to VBB in the off-state on channel 1. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists Note: SVBB_EN_CH1 must be enabled for this bit to signal short to VBB in the off state. 0h = No Short to VBB fault in off-state has occurred on this channel or short to VBB in off-state is not enabled 1h = Short to VBB fault in the off-state has occurred on this channel
2	OL_OFF_CH1	R	0h	This bit indicates if there is an open load in the off-state on channel 1. The output of channel 1 is pulled up by the OL_PULLUP_STR setting. Note: OL_OFF_EN_CH1 must be enabled for this bit to signal an open load in the off-state. 0h = No off-state open load fault has occurred on this channel or off-state open load detection in off-state is not enabled 1h = Off-state open load fault has occurred on this channel
1	CPUMP_UVLO_CH1	RC	0h	This bit if there is a charge pump UVLO (CP_UVLO) fault has occurred on channel 1. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = No CPUMP UVLO has occurred on this channel 1h = CPUMP UVLO has occurred on this channel
0	THERMAL_WRN_CH1	RC	0h	This bit indicates if the channel 1 FET temperature is above the overtemperature warning threshold. The fault is latched and cleared when FLT_STAT_CH1 register is read and the fault condition no longer exists 0h = FET temperature is below the over-temperature warning threshold in this channel 1h = FET temperature is above the over-temperature warning threshold in this channel

ADVANCE INFORMATION

8.1.14 PWM_CH1 Register (Offset = Dh) [Reset = F000h]

PWM_CH1 is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. PWM_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-9	PWM_FREQ_CH1	R/W	0h	Set the PWM frequency 0h = 0.8Hz 1h = 3.2Hz 2h = 12.7Hz 3h = 100Hz 4h = 200Hz 5h = 400Hz 6h = 816Hz 7h = 1650Hz
8-1	PWM_DTY_CH1	R/W	0h	8 bit to set duty cycle for PWM operation of CH1. Each bit ~0.39% duty cycle, linearly up to 100% dutycycle. 0x0 = GATEx always ON 0x1 = Reserved 0x2 = 2 x 0.39% 0x3 = 3 x 0.39% 0x4 = 5 x 0.39% 0x5 = 6 x 0.39%
0	PWM_EN_CH1	R/W	0h	Enable PWM for CH1 0h = Output follows CH1_ON setting 1h = Output is PWM according to duty cycle and frequency set if CH1_ON is high

ADVANCE INFORMATION

8.1.15 ILIM_CONFIG_CH1 Register (Offset = Eh) [Reset = 0010h]

ILIM_CONFIG_CH1 is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. ILIM_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LATCH_CH1	R/W	0h	If OCP or TSD fault occurs that channel shuts down, this bit sets if the channel auto retries or latches off 0h = Auto retry after tRETRY 1h = latch off until SW_STATE register is written to again
14	DI_OUT_DIS_FN_CH1	R/W	0h	Set this bit to 1 to use the DI_OUT_DIS pin as Output_Disable 0h = The LH state is determined by a DI_OUT_DIS pin (DI pin function) 1h = Outputs are disabled when DI_OUT_DIS pin is set HI (OUT_DIS function)
13-12	CAP_CHRG_CH1	R/W	0h	These bits set the capacitive charging mode during the inrush period after turn on. When CAP_CHRG_CH1 = 00, these are bits are programmed as the overcurrent protection threshold during the INRUSH_DURATION_CH1 period. The channel will immediately turn off if the threshold is reached. When CAP_CHRG_CH1 = 10, these bits are programmed as the current limit regulation threshold. The channel will turn on into the current limit and will continue to regulate the current until the output is fully charged or there is a thermal shutdown event. When CAP_CHRG_CH1 = 11, these bits are programmed as the pulse mode capacitive charging. The device will turn on the output according to the PWM settings in the PWM_CH1 register. Overcurrent protection is set by the IOCP_SET_CH1 bits Note: I2T is not enabled during the INRUSH_DURATION. 0h = No cap charging mode, IOCP value set by IOCP_SET_CH1 bits 1h = Reserved 2h = Current limit regulation mode, value set by INRUSH_LIMIT_CH1 bits 3h = Pulse mode capacitive mode, values set by PWM_CH1 register settings
11	I2T_EN_CH1	R/W	0h	Enables the I2T functionality for channel 1. I2T can be enabled before the channel is enabled or while it is enabled, but the I2T calculation will only start after the inrush period ends. 0h = I2T functionality not enabled 1h = I2T functionality is enabled
10-8	INRUSH_DURATION_CH1	R/W	0h	These bits determine the inrush period duration during which the INRUSH_LIMIT_CH1 level applies. 0h = 0ms 1h = 2ms 2h = 4ms 3h = 6ms 4h = 10ms 5h = 20ms 6h = 50ms 7h = 100ms
7-6	AUTO_RETRY_DURATION_CH1	R/W	0h	Setting the autoretry time for the channel when it is set as autoretry part and the fault goes away 0h = 1ms 1h = 10ms 2h = 0.15ms 3h = 100ms

ADVANCE INFORMATION

Table 8-18. ILIM_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	FOLDBACK_LOCK_DIS_CH1	R/W	0h	Set this bit for infinite auto retry after OCP or TSD faults. 0h = Finite (13) autoretry then latch the channel to the foldback lock state. The Auto retry time becomes 10x after every 7th cycle. The retry counter resets only when CHx_ON bit, LHI or DIx/OUT_DISx pins are toggled. 1h = Infinite Auto retry. The Auto retry time remains same for infinite cycles.
4	RESERVED	R	1h	Reserved
3-0	INRUSH_LIMIT_CH1	R/W	0h	These bits determine the inrush current limit on channel 1 if the current limit regulation (I_{CL_REG}) mode (CAP_CHRG_CH1 = 10) is used. For any other capacitive charging modes, these settings will be ignored. 0h = 1.75A 1h = 2.38A 2h = 2.75A 3h = 3.13A 4h = 3.5A 5h = 3.88A 6h = 4.25A 7h = 4.63A 8h = 5A 9h = 5.38A Ah = 6.35A Bh = 6.8A Ch = 7.25A Dh = 7.7A Eh = 8.1A Fh = 8.6A

ADVANCE INFORMATION

8.1.16 DIAG_CONFIG_CH1 Register (Offset = Fh) [Reset = 4000h]

DIAG_CONFIG_CH1 is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. DIAG_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VSNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable the VOUT SNS ADC functionality for this channel 0h = VOUT SNS ADC functionality enabled 1h = VOUT SNS ADC functionality is disabled
14	RESERVED	R	1h	Reserved
13	ISNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable ISNS ADC functionality for this channel 0h = ISNS ADC functionality enabled 1h = ISNS ADC functionality is disabled
12-10	SLRT_CH1	R/W	0h	Slew Rate set for ouput of CH1. 6 different slew rate values for adjustable slew rate per electrical characteristics table. The default values loaded from NVM. 0h = 0.27V/µs 1h = 0.36V/µs 2h = 0.43V/µs 3h = 0.5V/µs 4h = 0.057V/µs
9	OL_ON_ENTRY_CH1	R/W	0h	This bit determines if channel 1 should enter a mode with small FET to more accurately detect lower output current. Note: The device can only enter this mode if there are no existing faults on the channel and the output current is below $I_{ENTRY\_OL\_ON}$. 0h = KSNS1, KDIG1 ratio and RON = Large FET 1h = KSNS2, KDIG2 ratio and RON = Small FET
8-7	FET_SHORT_BIST_BLANK	R/W	0h	These bits determine the blanking time for the FET_SHORT BIST for channel 1 0h = 50µs 1h = 250µs 2h = 500µs 3h = 2ms
6-5	OL_PU_STR_CH1	R/W	0h	These bits determine the pull-up current (I_pu) at the VOUT1 for the off-state open load detection circuitry. 0h = 25µA 1h = 57µA 2h = 121µA 3h = 256µA
4	PD_EN_CH1	R/W	0h	This bit will enable the Pulldown in off state for the short to battery detection. Forcing this bit to 0 will disable the pulldown. Bit will automatically be cleared once SVBB algorithm is complete 0h = Pull Down Inactive 1h = Pull Down Enabled
3	PU_EN_CH1	R/W	0h	This bit will enable the Pullup in off state for the Open Load detection. Forcing this bit to 0 will disable the pullup. Bit will automatically be cleared once OL algorithm is complete 0h = Pull Up Inactive 1h = Pull Up Enabled
2	SVBB_EN_CH1	R/W	0h	This bit will enable the algorithm for short to battery in off state. Forcing this bit to 0 will lead to abnormal exit. Bit will automatically be cleared once algorithm is complete. The status is updated in FLT_STAT_CH1 register. 0h = No SVBB running in OFF state 1h = SVBB running in OFF state

ADVANCE INFORMATION

Table 8-19. DIAG_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	OL_EN_CH1	R/W	0h	This bit will enable the algorithm for open load in off state. Forcing this bit to 0 will lead to abnormal exit. Bit will automatically be cleared once algorithm is complete.The status is updated in FLT_STAT_CH1 register. 0h = No OL running in OFF state 1h = OL running in OFF state
0	TSNS_DIS_CH1	R/W	0h	Set this bit to 1 to disable the ADC TSNS functionality for this channel 0h = TSNS ADC functionality enabled 1h = TSNS ADC functionality is disabled

8.1.17 ADC_RESULT_CH1_I Register (Offset = 10h) [Reset = E800h]

ADC_RESULT_CH1_I is shown in Table 8-20.

Return to the Summary Table.

Table 8-20. ADC_RESULT_CH1_I Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	7h	Reserved
12	ISNS_CH1_ONOFF_STAT	R	0h	The bit is set to 1 if the ADC conversion of ISNS is done while the channel is ON 0h = ISNS read is done while the status of the CH1 FET is OFF 1h = ISNS read is done while the status of the CH1 FET is ON
11	RESERVED	R	1h	Reserved
10	ISNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 output current (ISNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_I	R	0h	ADC result (10-bits) from the conversion of the current in CH1

ADVANCE INFORMATION

8.1.18 ADC_RESULT_CH1_T Register (Offset = 11h) [Reset = F800h]

ADC_RESULT_CH1_T is shown in Table 8-21.

Return to the Summary Table.

Table 8-21. ADC_RESULT_CH1_T Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	TSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 TSNS conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_T	R	0h	ADC result (10-bits) from the conversion of the temperature in CH1

8.1.19 ADC_RESULT_CH1_V Register (Offset = 12h) [Reset = F800h]

ADC_RESULT_CH1_V is shown in Table 8-22.

Return to the Summary Table.

Table 8-22. ADC_RESULT_CH1_V Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	1Fh	Reserved
10	VSNS_RDY_CH1	R	0h	This bit indicates if a new ADC result for channel 1 VOUT voltage (VSNS) conversion is available since the last read 0h = ADC value not updated 1h = ADC value ready since last read
9-0	ADC_RESULT_CH1_V	R	0h	ADC result (10-bits) from the conversion of the output voltage in CH1

8.1.20 I2T_CONFIG_CH1 Register (Offset = 14h) [Reset = 00XXh]

I2T_CONFIG_CH1 is shown in Table 8-23.

Return to the Summary Table.

Table 8-23. I2T_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TCLDN_CH1	R/W	0h	These bits determine the cooldown time (or time to retry) based on the accumulator value after an I2T shutdown on channel 1. Note: If setting 0h is used, the channel will remain off after an I2T shutdown with no retry. To retry in this setting, change the bits to 1h, 2h, or 3h to allow the device to retry after the accumulator has reached the defined value. 0h = Latch mode (or no retry) 1h = Acuumulator decrements to 2/3 times of I2T TRIP threshold 2h = Acuumulator decrements to 1/3 times of I2T TRIP threshold 3h = Acuumulator decrements to 0
13	DCR_CH1	R/W	0h	Sets the mode of operation 0h = I2t Mode DCR0_x000D_ 1h = I2t Mode DCR1
12-11	ACC_DCR0_CH1	R/W	0h	Decrement of IACC with IADC <NOM_CUR when DCR_CHx = 0. 0h = Decrement factor k = 0.25 1h = Decrement factor k = 0.5 2h = Decrement factor k = 1 3h = Decrement factor k = 2
10-9	SWCL_DLY_TMR_CH1	R/W	0h	2-bits to set delayed turn-off timer for Channel 1. Sets the time after which the channel shuts down when the current exceeds ISWCL. 0h = 0.05ms 1h = 1.0ms 2h = 2.0ms 3h = No SWCL based turn-off
8-7	ISWCL_CH1	R/W	1h	2bits to set delayed turn-off current threshold value for I2T functionality for Channel 1. The threshold should be set below the maximum current sensed with the sense resistor chosen.
6-5	RESERVED	R	3h	Reserved

ADVANCE INFORMATION

Table 8-23. I2T_CONFIG_CH1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	NOM_CUR_CH1	R/W	X	These bits set the nominal current value for channel 1 for the I2T function. If the I2T function is enabled for channel 1, above this value the device will enter the I2T accumulation mode. Note: The NOM_CUR_CH1 value cannot be modified when the device is in the cool down time period. 00h = 3.6A 01h = 4.3A 02h = 5A 03h = 5.7A 04h = 6.4A 05h = 7.1A 06h = 7.8A 07h = 8.5A 08h = 9.2A 09h = 9.9A 0Ah = 10.6A 0Bh = 11.3A 0Ch = 12A 0Dh = 12.7A 0Eh = 13.4A 0Fh = 14.1A 10h = 14.8A 11h = 15.5A 12h = 16.2A 13h = 16.9A 14h = 17.6A 15h = 18.3A 16h = 18.9A 17h = 19.6A 18h = 20.3A 19h = 21A 1Ah = 21.7A 1Bh = 22.4A 1Ch = 23.1A 1Dh = 23.8A 1Eh = 24.5A 1Fh = 25.2A

ADVANCE INFORMATION

8.1.21 I2T_TRIP_CONFIG_CH1 Register (Offset = 1Eh) [Reset = F8F8h]

I2T_TRIP_CONFIG_CH1 is shown in Table 8-24.

Return to the Summary Table.

Table 8-24. I2T_TRIP_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	Fh	Reserved
11-8	RESERVED	R	8h	Reserved
7-4	RESERVED	R	Fh	Reserved
3-0	I2T_TRIP_CH1	R/W	8h	These bits set the I2T trip value for Channel 1. Note: For reference the equations for the I2T trip value are below If DCR_CH1 = 0: I2T_TRIP = I_{OUT1}^{2} x t If DCR_CH1 = 1: I2T = (I_{OUT1}^{2} - NOM_CUR_CH1^{2}) * t Note: The I2T_TRIP_CH1 value cannot be modified when the device is in the cool down time period. I2T settings with DCR = 0: 0x0 = 256.3 A2s 0x1 = 384.4 A2s 0x2 = 768.7 A2s 0x3 = 1153 A2s 0x4 = 1537.3 A2s 0x5 = 1921.5 A2s 0x6 = 2305.8 A2s 0x7 = 2690.1 A2s 0x8 = 3202.5 A2s 0x9 = 3714.9 A2s 0xA = 4227.2 A2s 0xB = 4867.7 A2s 0xC = 5636.3 A2s 0xD = 6404.9 A2s 0xE = 7685.8 A2s 0xF = 10247.7 A2s I2T settings with DCR = 1: 0h = 112.9 A2s 1h = 169.3 A2s 2h = 338.5 A2s 3h = 507.7 A2s 4h = 677 A2s 5h = 846.2 A2s 6h = 1015.4 A2s 7h = 1184.6 A2s 8h = 1410.3 A2s 9h = 1635.9 A2s Ah = 1861.5 A2s Bh = 2143.6 A2s Ch = 2482 A2s Dh = 2820.5 A2s Eh = 3384.5 A2s Fh = 4512.7 A2s

8.1.22 I2T_ACC_RD_CH1 Register (Offset = 1Fh) [Reset = 0000h]

I2T_ACC_RD_CH1 is shown in Table 8-25.

Return to the Summary Table.

Table 8-25. I2T_ACC_RD_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	I2T_ACC_RD_CH1	R	0h	16 MSB bits I2T Accumulator of CH1

8.1.23 IOCP_CONFIG_CH1 Register (Offset = 35h) [Reset = FFFXh]

IOCP_CONFIG_CH1 is shown in Table 8-26.

Return to the Summary Table.

Table 8-26. IOCP_CONFIG_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	Fh	Reserved
11-8	RESERVED	R/W	Fh	Reserved
7-4	RESERVED	R/W	Fh	Reserved
3-0	IOCP_SET_CH1	R/W	X	These bits determine the overcurrent protection (I_{OCP}) threshold for channel 1. 0h = 18.5A 1h = 22.2A 2h = 25.9A 3h = 29.6A 4h = 33.3A 5h = 37A 6h = 40.7A 7h = 44.4A 8h = 48.1A 9h = 51.8A Ah = 55.5A Bh = 59.2A Ch = 62.9A Dh = 66.6A Eh = 70.3A Fh = 74A

8.1.24 UV_CONFIG Register (Offset = 37h) [Reset = 0XFXh]

UV_CONFIG is shown in Table 8-27.

Return to the Summary Table.

Table 8-27. UV_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	UVLO_SET	R/W	0h	These bits set the UVLO falling thresholds for the device 00h = UVLO Disabled 01h = 4.5V 02h = 5V 03h = 6V 04h = 7V 05h = 8V 06h = 9V 07h = 16V 08h = 18V 09h = 20V 0Ah = 22V 0Bh = 24V 0Ch = 26V 0Dh = 28V 0Eh = 30V 0Fh = 32V
11-10	RESERVED	R/W	3h	Reserved
9-8	UVLO_MASK	R/W	X	These bits set the UVLO masking time setting 0h = 0µs 1h = 10µs 2h = 50µs 3h = 200µs
7-4	RESERVED	R	Fh	Reserved
3-2	RESERVED	R	3h	Reserved
1	UVLO_LPM_EN	R/W	X	This bit sets if UVLO is enabled in LPM 0h = UVLO functionality disabled in LPM 1h = UVLO functionality enabled in LPM
0	RESERVED	R	1h	Reserved

ADVANCE INFORMATION

8.1.25 DEV_CONFIG_2 Register (Offset = 3Dh) [Reset = FFE0h]

DEV_CONFIG_2 is shown in Table 8-28.

Return to the Summary Table.

Table 8-28. DEV_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	7FFh	Reserved
4	LIMPHOME_STAT_FLT_EN	R/W	0h	This bit enable LIMPHOME_STAT bit on FLT pin. 0h = LIMPHOME_STAT bit is not signalled on the FLT pin 1h = LIMPHOME_STAT bit is signalled on the FLT pin
3-2	CONFIG_DI_MASK	R/W	0h	This bit sets the masking time on the DIx/OUT_DISx pin 0h = 0µs 1h = 6.5µs 2h = 10µs 3h = 20µs
1-0	CONFIG_LHI_MASK	R/W	0h	This bit sets the masking time on the LHI pin 0h = 0µs 1h = 6.5µs 2h = 10µs 3h = 20µs

8.1.26 EEPROM_PROG Register (Offset = 3Fh) [Reset = FFFCh]

EEPROM_PROG is shown in Table 8-29.

Return to the Summary Table.

Table 8-29. EEPROM_PROG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	3FFFh	Reserved
1	EEPROM_BUSY	R	0h	EEPROM programming status 0h = Device is not in EEPROM programming procedure 1h = Device is currently in EEPROM programming procedure
0	PROG_NVM	R	0h	EEPROM programming control status bit. This bit will self clear to 0 when the EEPROM programming is complete. 1h = Device is programming EEPROM

8.2 EEPROM (NVM) Overview

TPS48xHSxx-Q1 provides user programmable Electrically Erasable Programmable Read-Only Memory (EEPROM) for some configuration registers and some customer defined programmable registers. This enables the user to reprogram the default values for these registers. Table shows which registers can be programmed through the EEPROM programming procedure.

Table 8-30. Register Overview

Offset	Register Name	EEPROM User Programmable
00h	DEV_ID	N
01h	SLEEP	N
02h	LPM	N
03h	FAULT_GLOBAL	N
04h	FAULT_MASK	Y
05h	BIST_RESULT_CH1	N
06h	SW_STATE	N
07h	DEVICE_TEST_CH1	N
08h	DEV_CONFIG	Y
09h	ADC_CONFIG	N
0Ah	ADC_RESULT_VBB	N
0Bh	ADC_RESULT_BIST	N
0Ch	FLT_STAT_CH1	N
0Dh	PWM_CH1	Y
0Eh	ILIM_CONFIG_CH1	Y
0Fh	DIAG_CONFIG_CH1	Y
10h	ADC_RESULT_CH1_I	N
11h	ADC_RESULT_CH1_T	N
12h	ADC_RESULT_CH1_V	N
14h	I2T_CONFIG_CH1	Y
1Eh	I2T_TRIP_CH1	Y
1Fh	I2T_ACC_RD_CH1	N
35h	IOCP_CONFIG_CH1	Y
37h	UV_CONFIG	Y
3Dh	DEV_CONFIG_2	Y

ADVANCE INFORMATION

Table 8-30. Register Overview (continued)

Offset	Register Name	EEPROM User Programmable
3Fh	EEPROM_PROGRAM_CONTROL_STATUS	Y

EEPROM programming procedure

The default values for the user programmable registers can be reprogrammed through the below procedure. The following conditions need to be met in order to re-program the EEPROM correctly

- VBB voltage ≥ 6V, referenced to device GND
- VDD voltage > VDD_UVLO, referenced to device GND

Figure shows the procedure of how to re-program the default values.

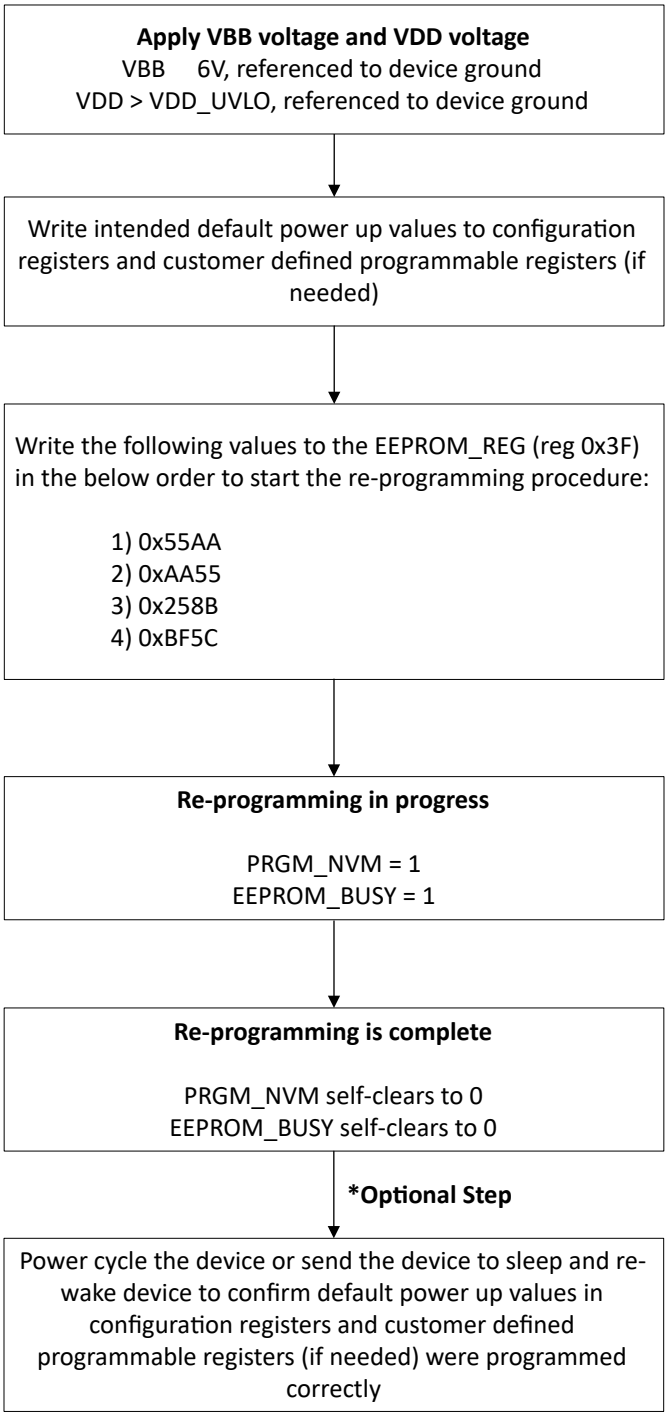

Figure 8-1. EEPROM Re-Programming Procedure

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Figure 9-1 shows the schematic of a typical application of the TPS481HS04-Q1. It includes all standard external components. This section of the data sheet discusses the considerations in implementing commonly required application functionality. The circuit assumes no reverse polarity protection on the input supply, so additional components for protection are required.

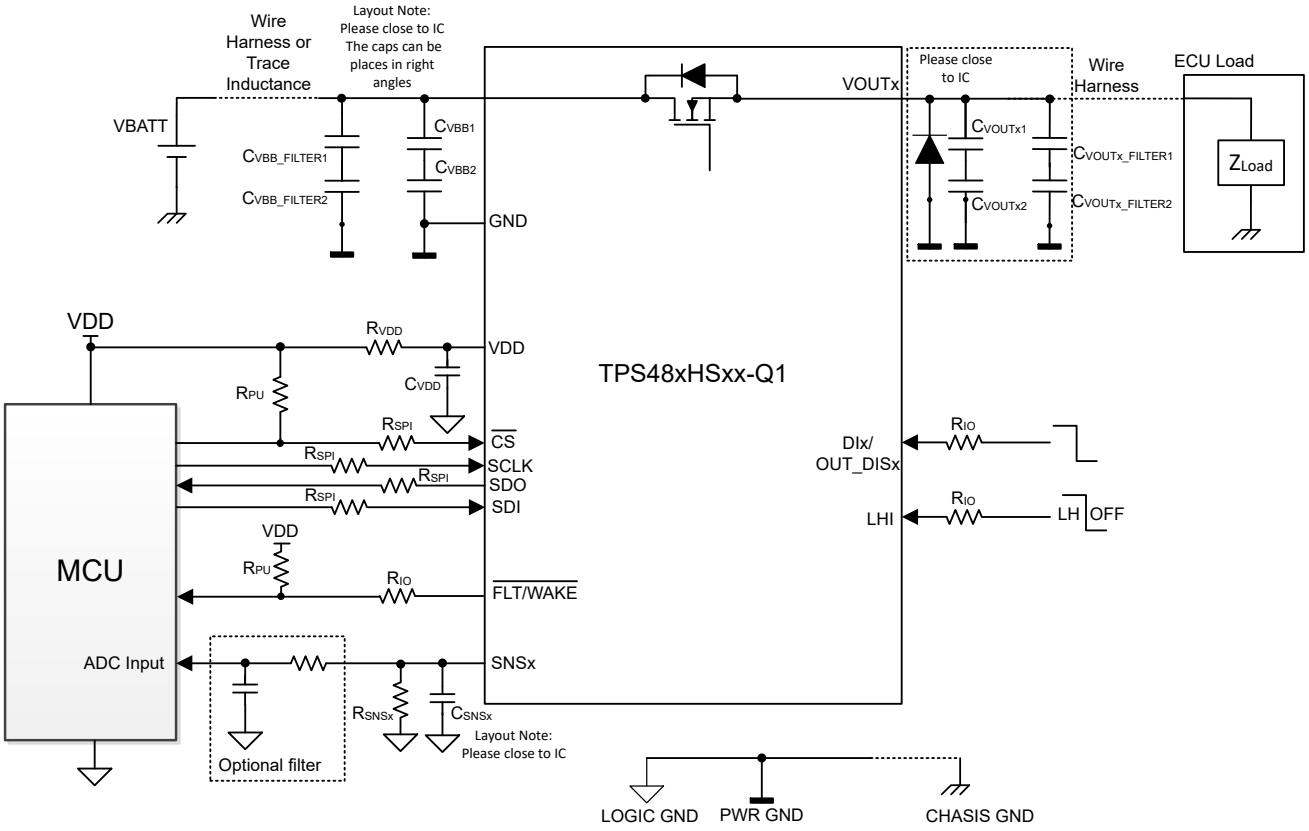


Figure 9-1. System Diagram

Table 9-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{SPI}	10 to 1000Ω	For EMI or other transient limits on the SPI pins.
R_{IO}	0.01 to 10kΩ	Protect micro-controller and device GPIO pins
R_{PU}	4.7kΩ	
R_{SNSx}	0.5 - 1.5kΩ	Translate the sense current into sense voltage for ADC input
C_{SNSx}	1 to 10nF	Low-pass filter for the ADC input.
Output diode	Optional for output wire inductance > 5µH	Clamp transient voltage due to output wireharness during switch turn off

Table 9-1. Recommended External Components (continued)

COMPONENT	TYPICAL VALUE	PURPOSE
R_{VDD}	1 to 10Ω	Limit the rate of rise / fall in VDD supply input- to the IC.
C_{VDD}	470 to 1000nF	VDD supply voltage stability to system ground.
C_{VBB1}, C_{VBB2}	220 – 4700nF	Prevent undervoltage during hard-short to ground fault event
C_{VBB_FILTER}	220 – 4700nF	Stabilize the input supply and filter out low frequency noise.
C_{OUTx_FILTER}	22 to 100nF	Filtering of voltage transients (for example, ESD, ISO7637-2).
C_{VOUTx1}, C_{VOUTx2}	22 to 100nF	Filtering of voltage transients

9.2 Typical Application

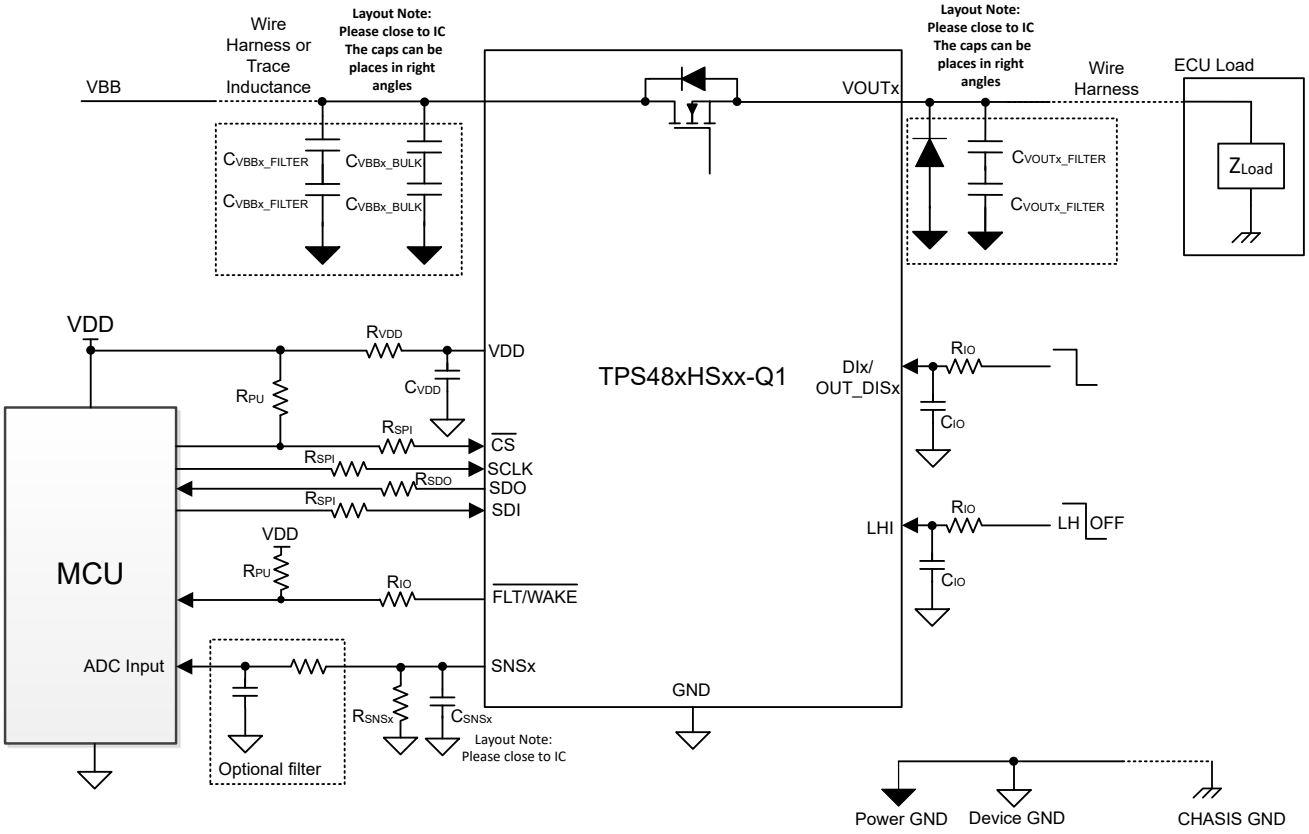


Figure 9-2. Block Diagram for Powering an ECU load with Input Capacitance

ADVANCE INFORMATION

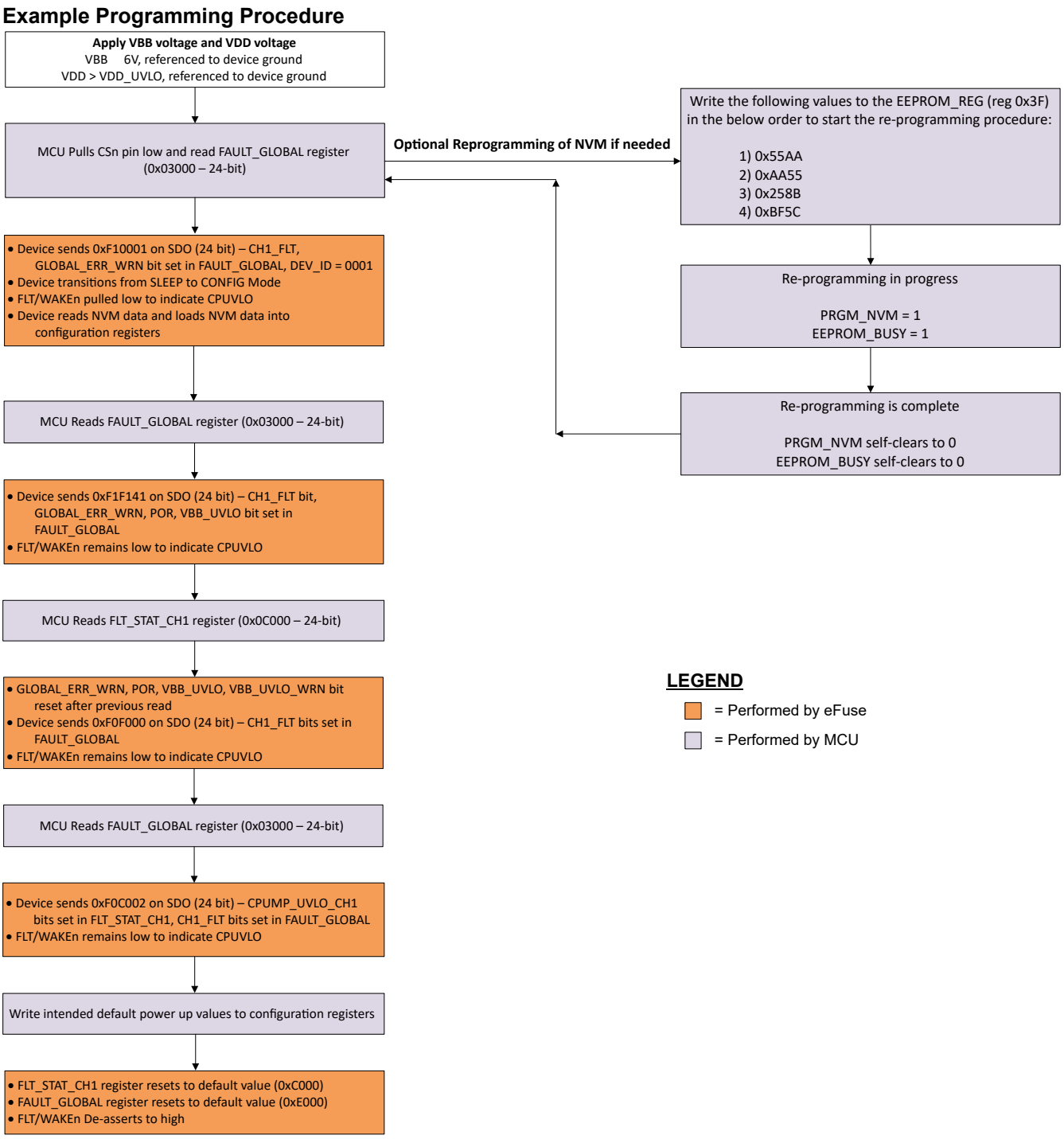


Figure 9-3. TPS481HS04-Q1 Example Programming Procedure

9.2.1 Design Requirements

For this design example, use the input parameters shown in Table 9-2.

Table 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BB}	48V
Undervoltage lockout set point, $V_{(VBB\_UVLOF)}$	24V

Table 9-2. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Load wakeup threshold, I_{LWU}	Small FET, 0.23A
Current limit, I_{CL_REG}	8.1A
Output bulk capacitor, C_{BULK}	680µA
I2t start threshold, I_{NOM}	15.5A
Overcurrent threshold, I_{OCP}	62.9A

9.2.2 Detailed Design Procedure

Table 9-3. Configuration Register Settings

BIT FIELD NAME	SETTING
CAP_CHRG_CHx	Sets capactior charging method
INRUSH_LIMIT_CHx	Set inrush current limit
INRUSH_DURATION_CHx	Sets inrush duration
LPM_EXIT_CURR_CHx	Sets load wakeup current
UV_CONFIG_CHx	Sets VBB UVLO threshold, hysteresis and masking time
I2T_CONFIG_CHx	Sets I2t start threshold, cooldown timer
I2T_TRIP_CHx	Sets I2t trip threshold
SCP_CONFIG_CHx	Sets SCP threshold, masking time
LATCH_CHx	Auto-retry or latch

9.2.3 Application Curves

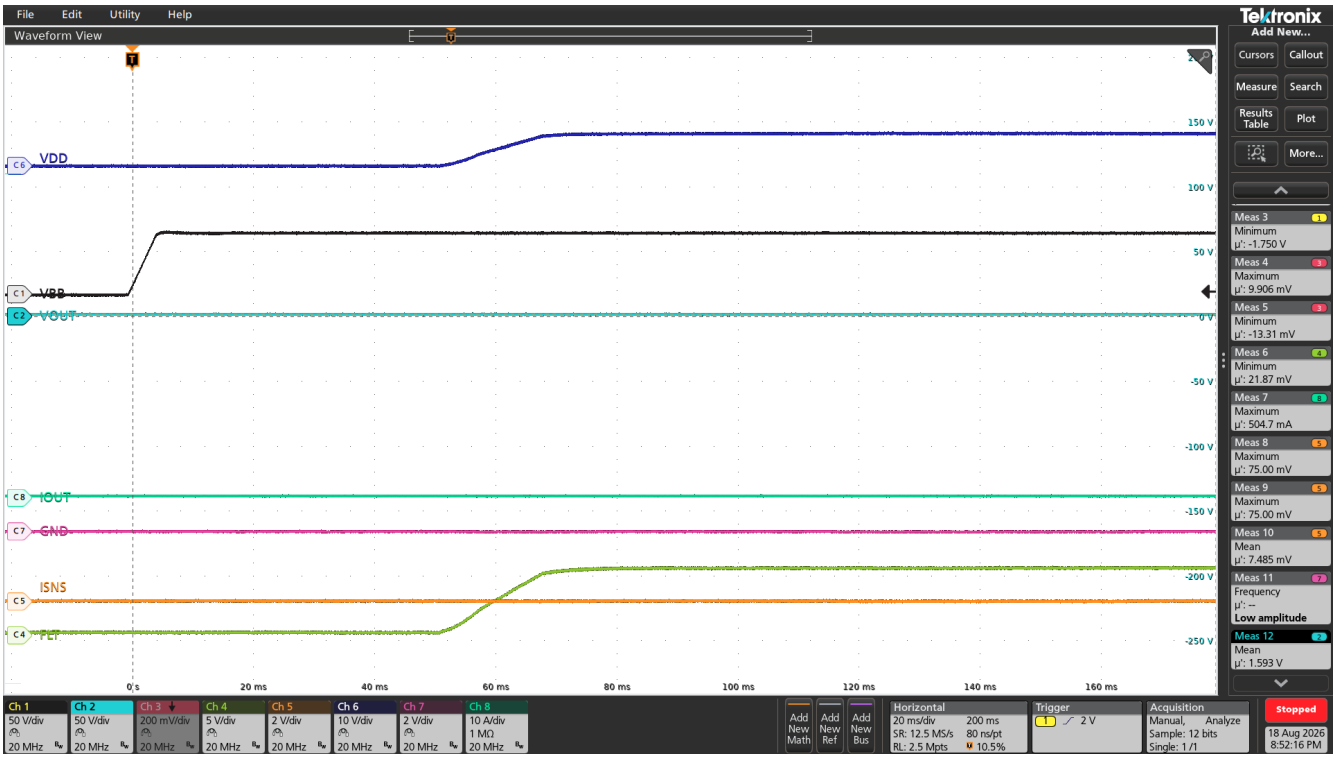


Figure 9-4. Startup Profile

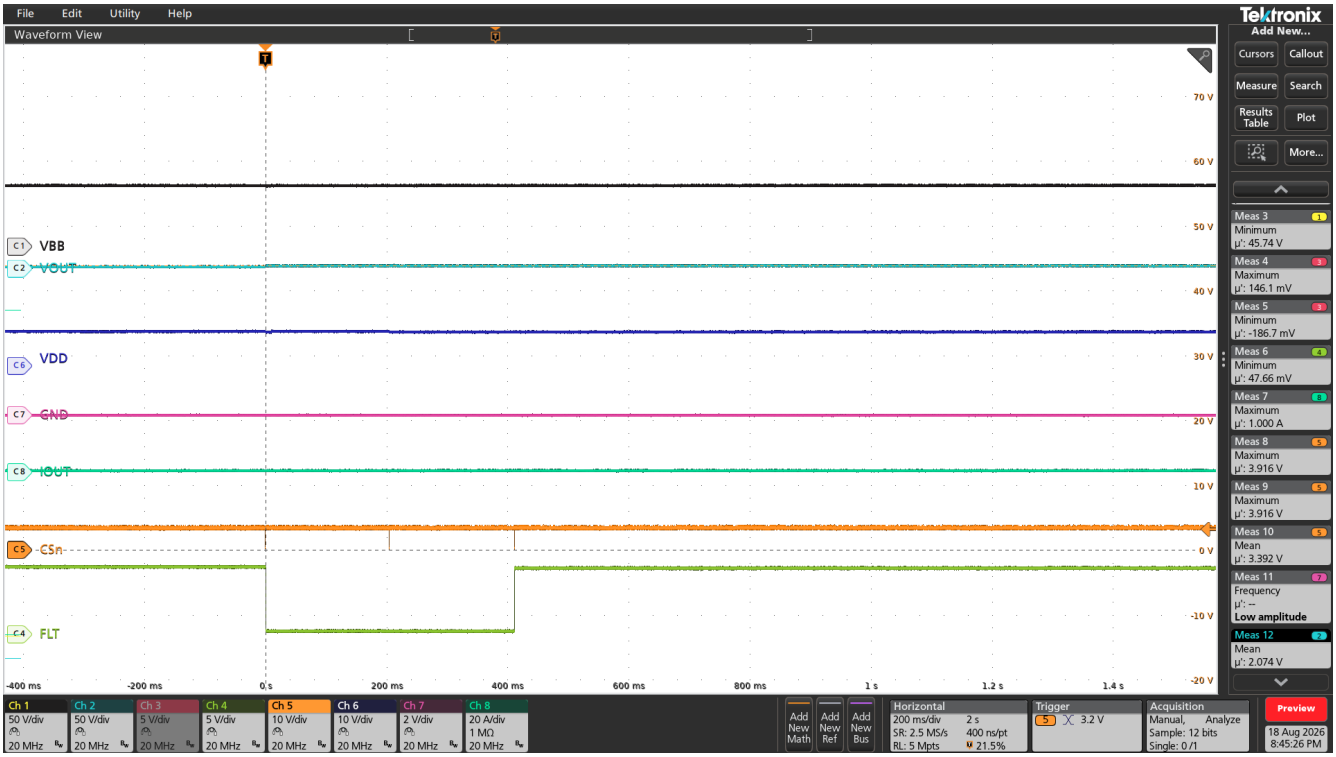


Figure 9-5. $\overline{CS}$ Pulled From High to Low For Device Transition From SLEEP to CONFIG Mode, Read FLT_STAT_CHx First and Then FAULT_GLOBAL Registers to Clear These Registers and Deassert FLT/ WAKE Pin

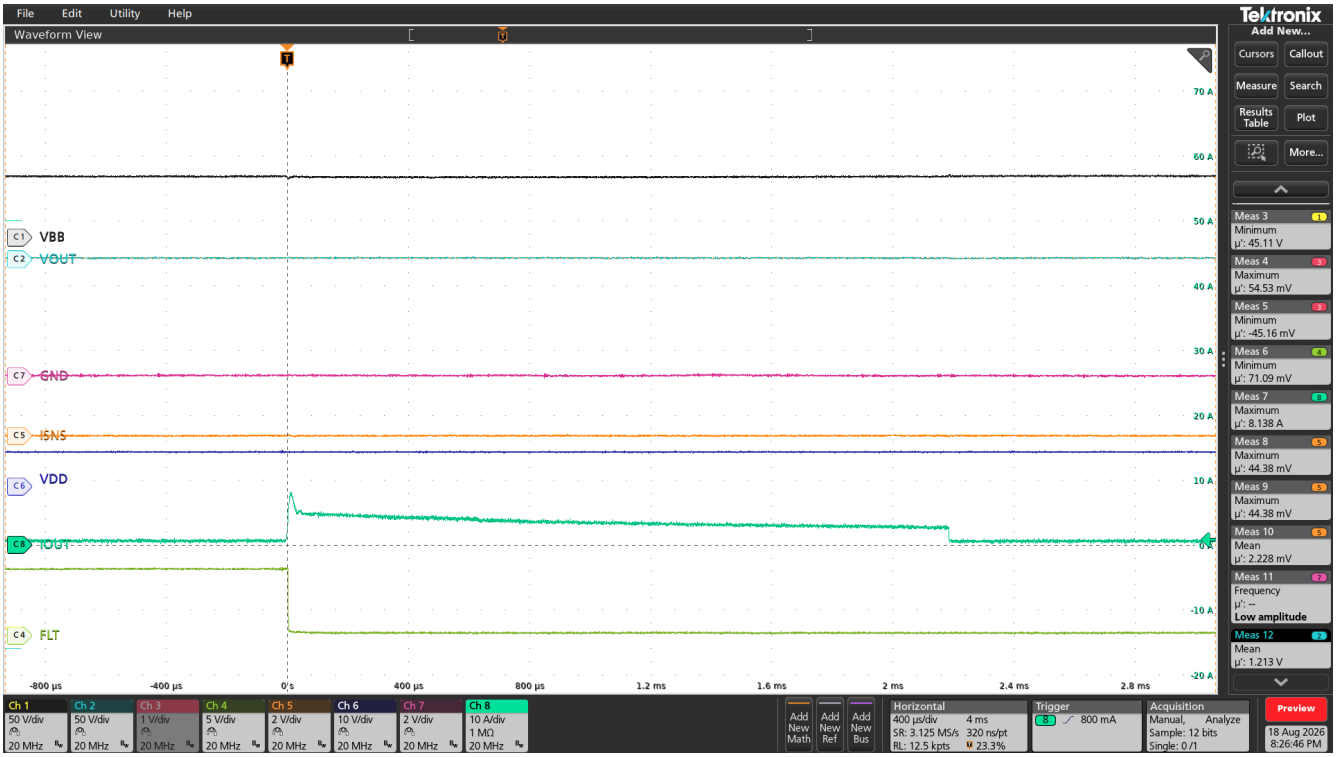


Figure 9-6. CHx_ON Bit Set From '0' to '1' With CAP_CHRG_CHx = 0x2 (Current limit regulation mode) With COUT = 680µF

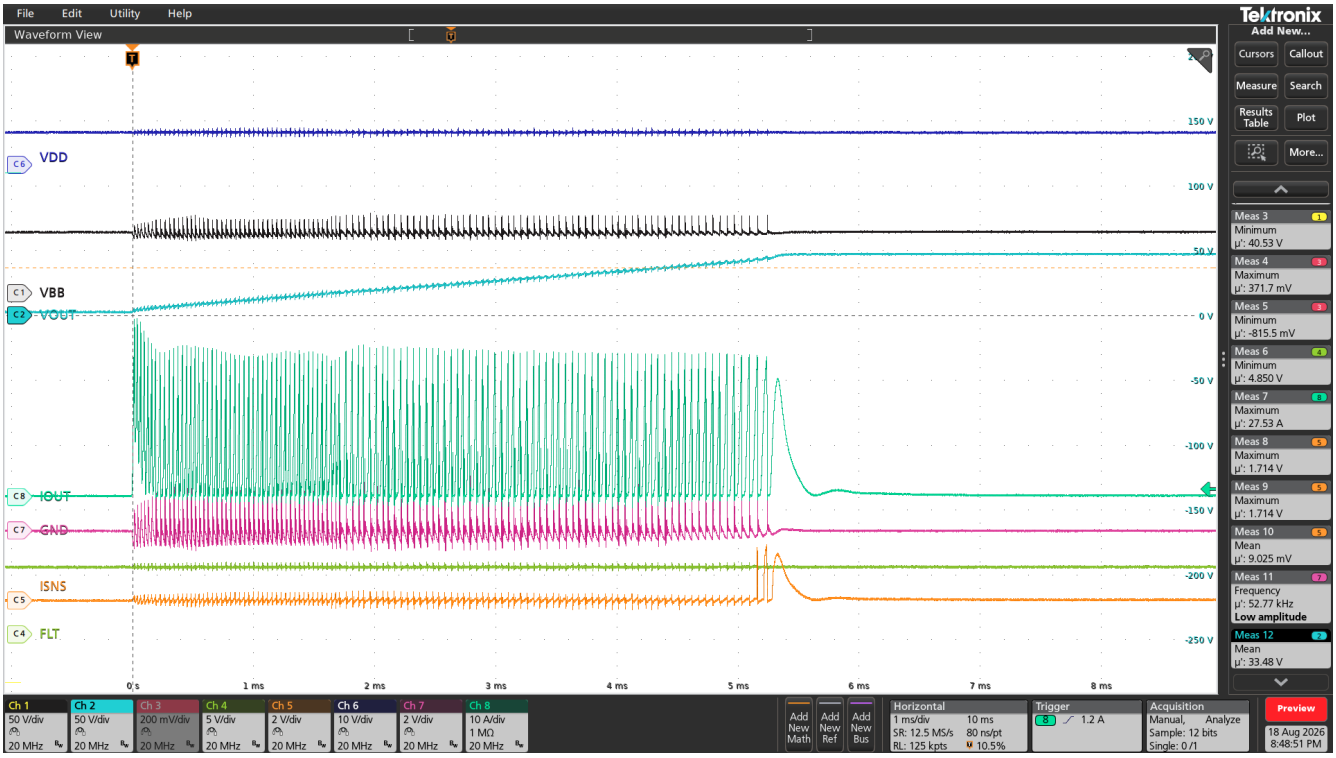


Figure 9-7. CHx_ON Bit Set From '0' to '1' With CAP_CHRG_CHx = 0x3 (PWM method) With COUT = 680µF, LIN = 0.5µH, LOUT = 0.5µH

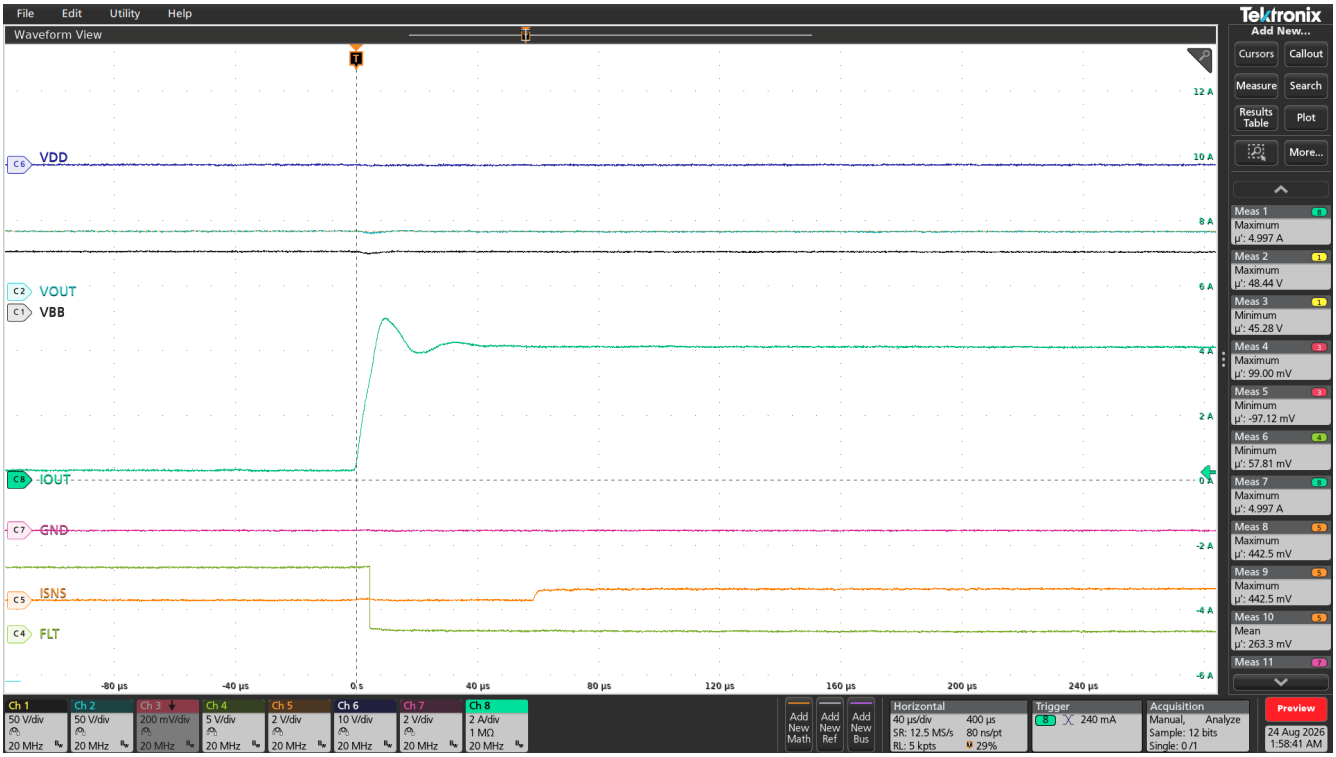


Figure 9-8. LPM to Active Mode Via Increase in Load Current

ADVANCE INFORMATION

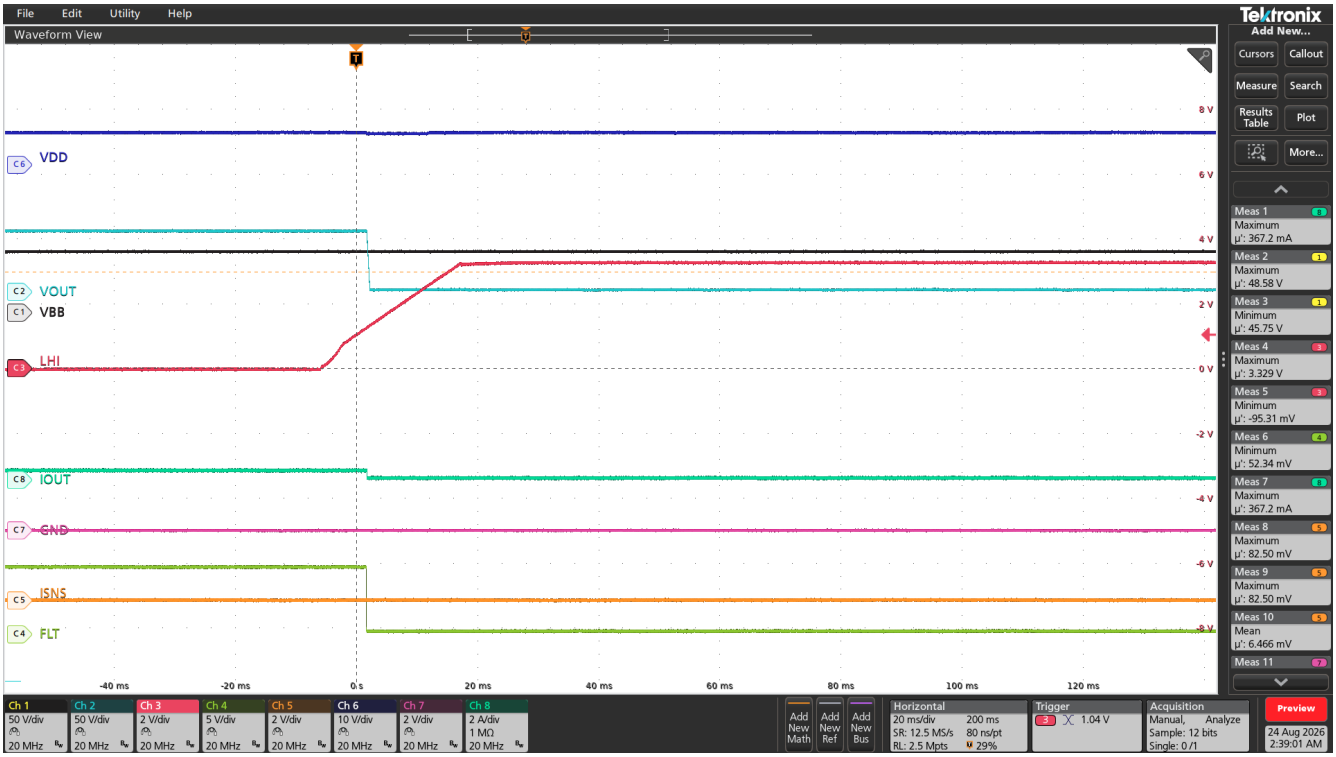


Figure 9-9. LPM to LIMPHOME Mode When LHI is Pulled From Low to High

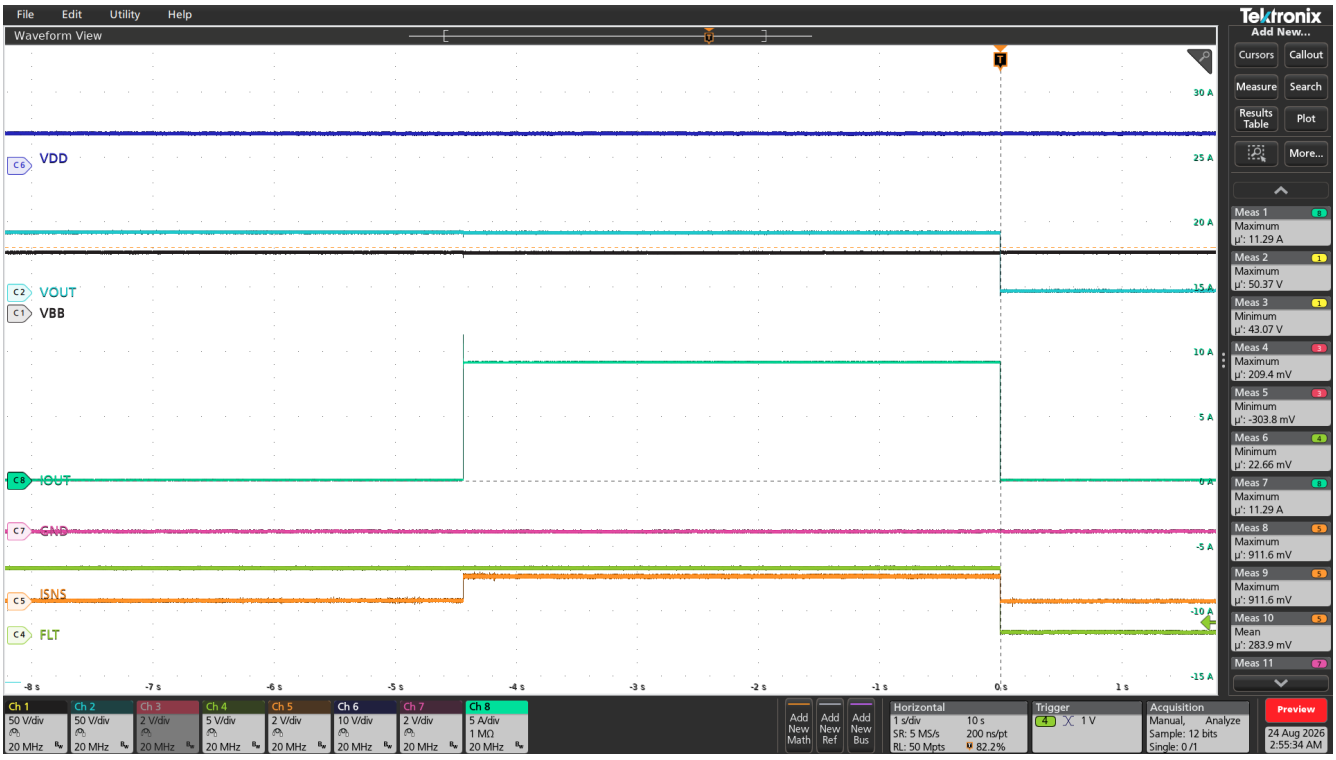


Figure 9-10. I2T Protection Behaviour in ACTIVE Mode

9.3 Power Supply Recommendations

The device is designed to operate in a 24V or 48V automotive system. The device works with two power supply inputs – a battery input and a low voltage supply input (5V or 3.3V) typically generated with a DC-DC converter (recommended to reduce quiescent current draw from the battery) or LDO external to the IC from the battery.

The nominal supply voltage range is 8V to 60V as measured at the V_{BB} pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in the *Electrical Characterisitcs* table. The device is also designed to withstand voltage transients beyond this range like load dump. When operating outside of the nominal voltage range but within the operating voltage range, the device will exhibit normal functional behavior.

9.4 Layout

9.4.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed thermal pad (connected to VBB pin) to a large broken copper pour. On the top PCB layer, the pour can extend beyond the package dimensions as shown in the example below. In addition to this, TI recommends to also have a V_{BB} plane either on one of the internal PCB layers or on the bottom layer.

Vias must connect this plane to the top V_{BB} pour. TI recommends that the IO pins that connect to the controller be routed through a via and internal or bottom PCB layer.

ADVANCE INFORMATION

9.4.2 Layout Example

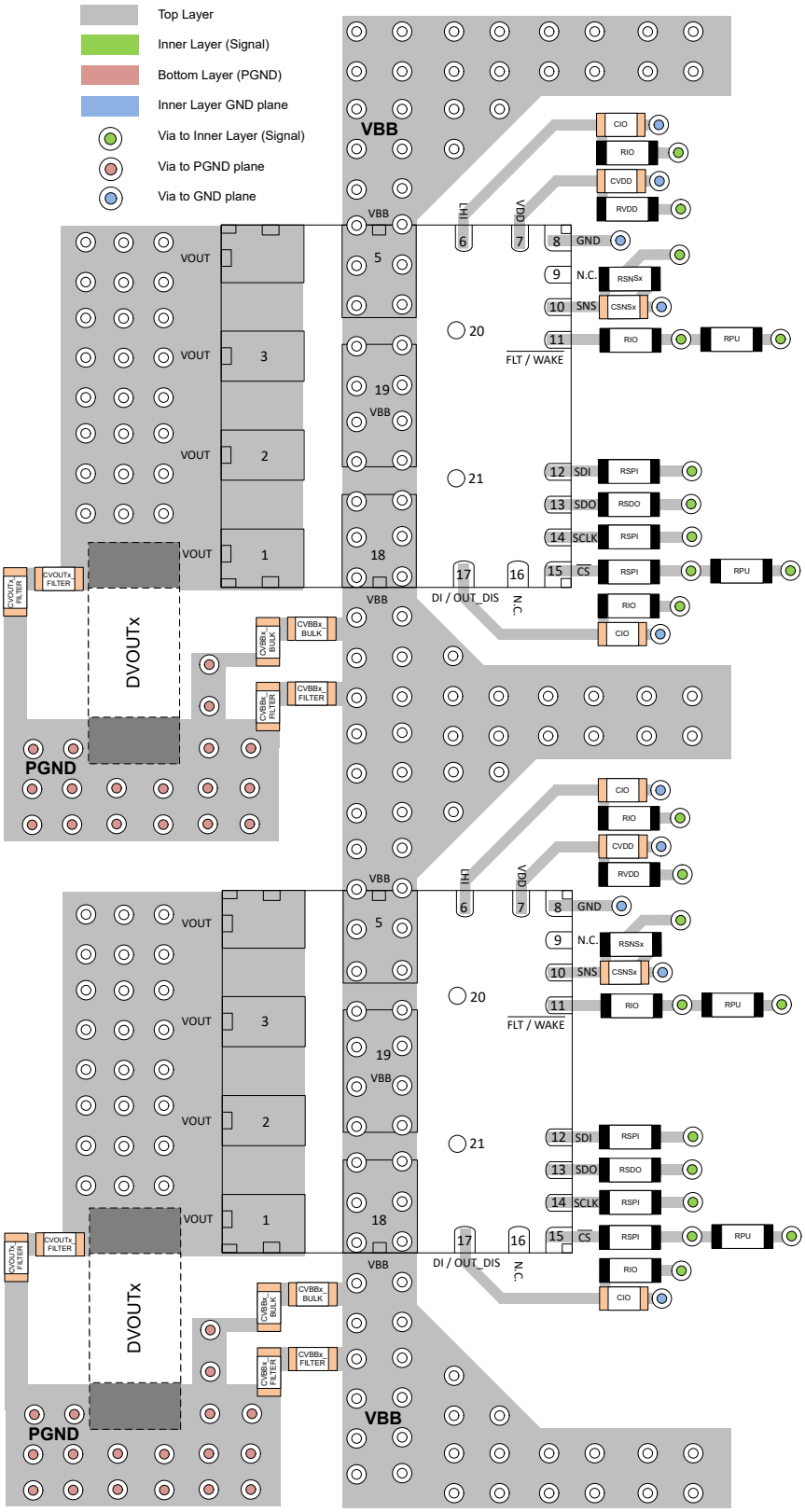


Figure 9-11. Typical PCB Layout Example of TPS481HS04-Q1

10 Device and Documentation Support

10.1 Documentation Support

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2026	*	Initial Release

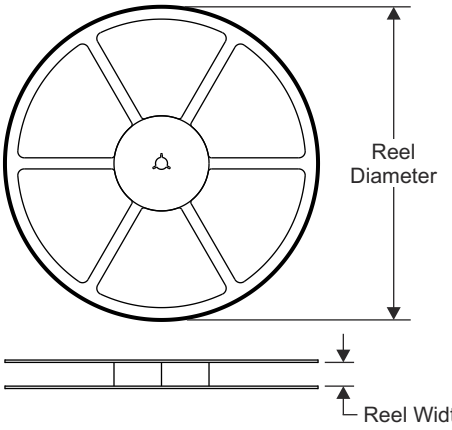
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

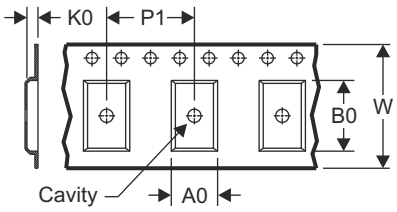
ADVANCE INFORMATION

12.1 Tape and Reel Information

REEL DIMENSIONS

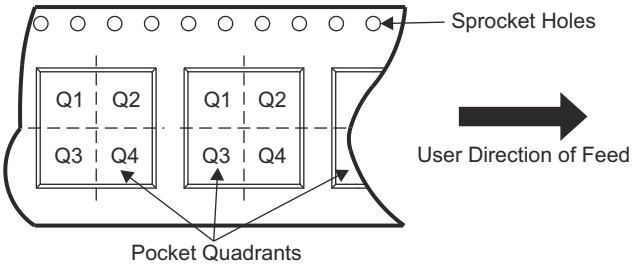


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

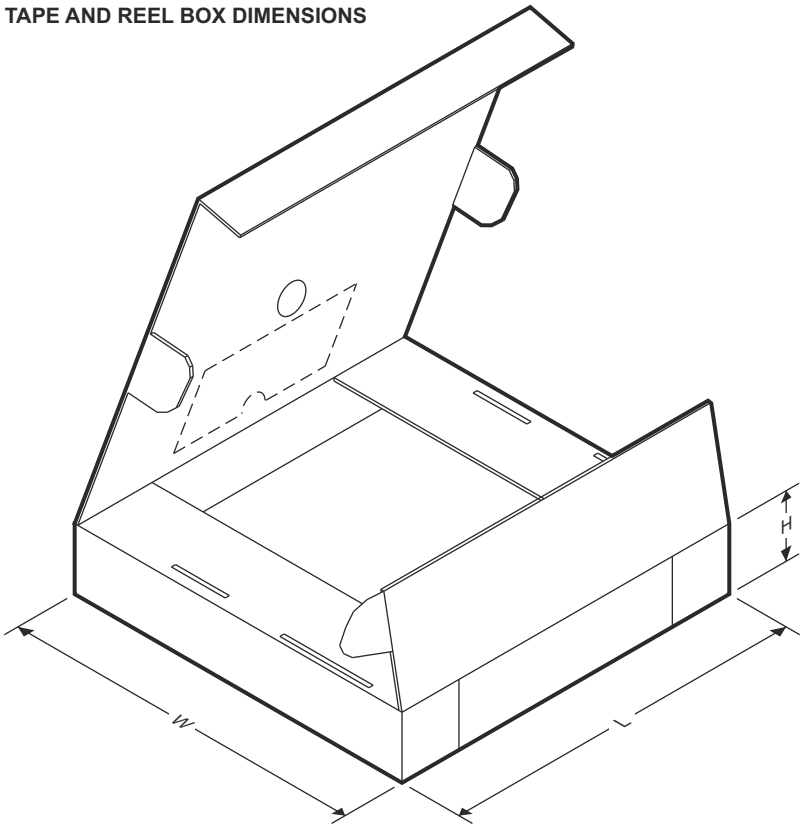
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS481HS04QRBLR Q1	QFN	RBL	21	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS481HS04QRBLRQ1	QFN	RBL	21	3000	367.0	367.0	38.0

ADVANCE INFORMATION

12.2 Mechanical Data

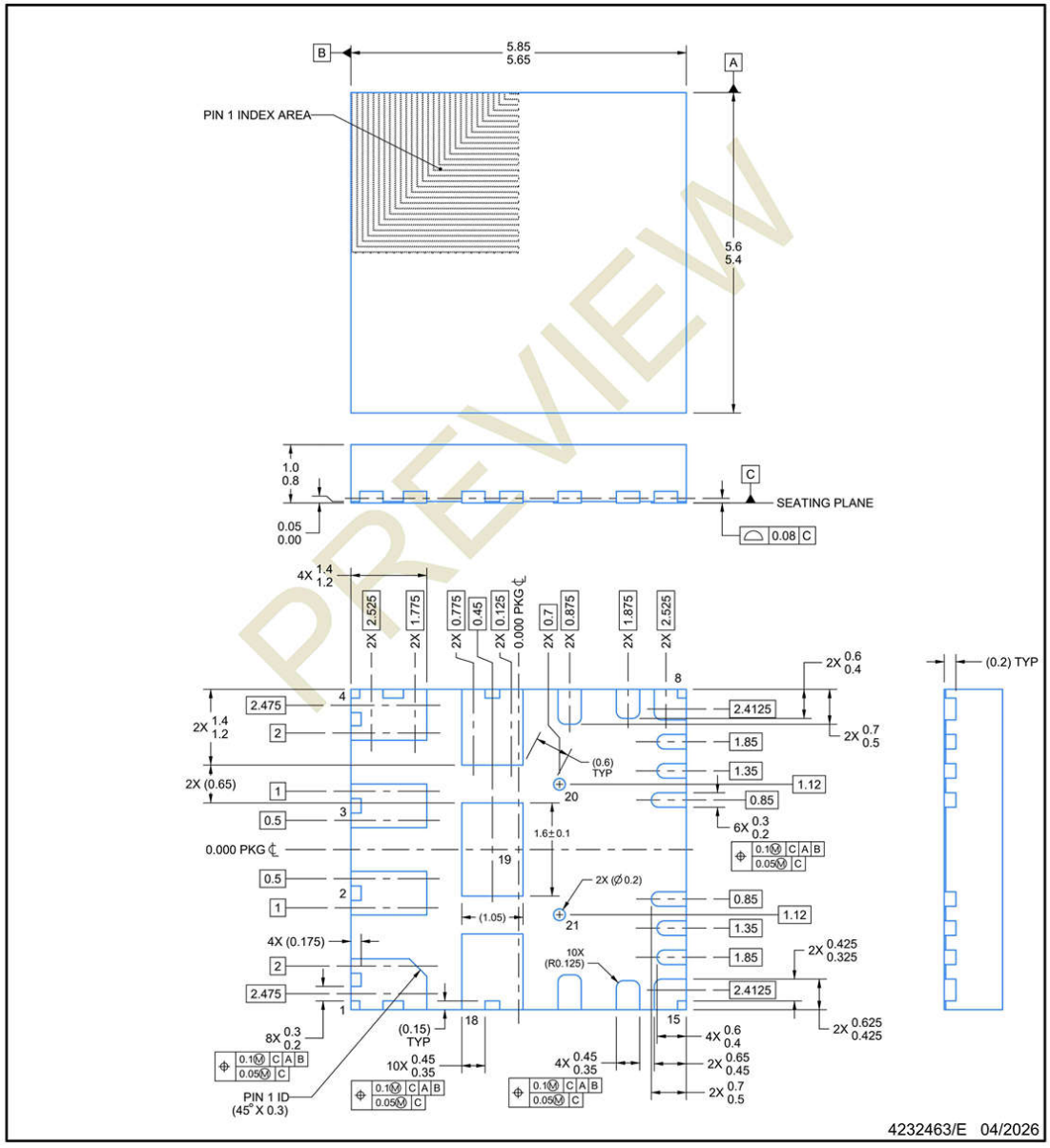
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RBL0021A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

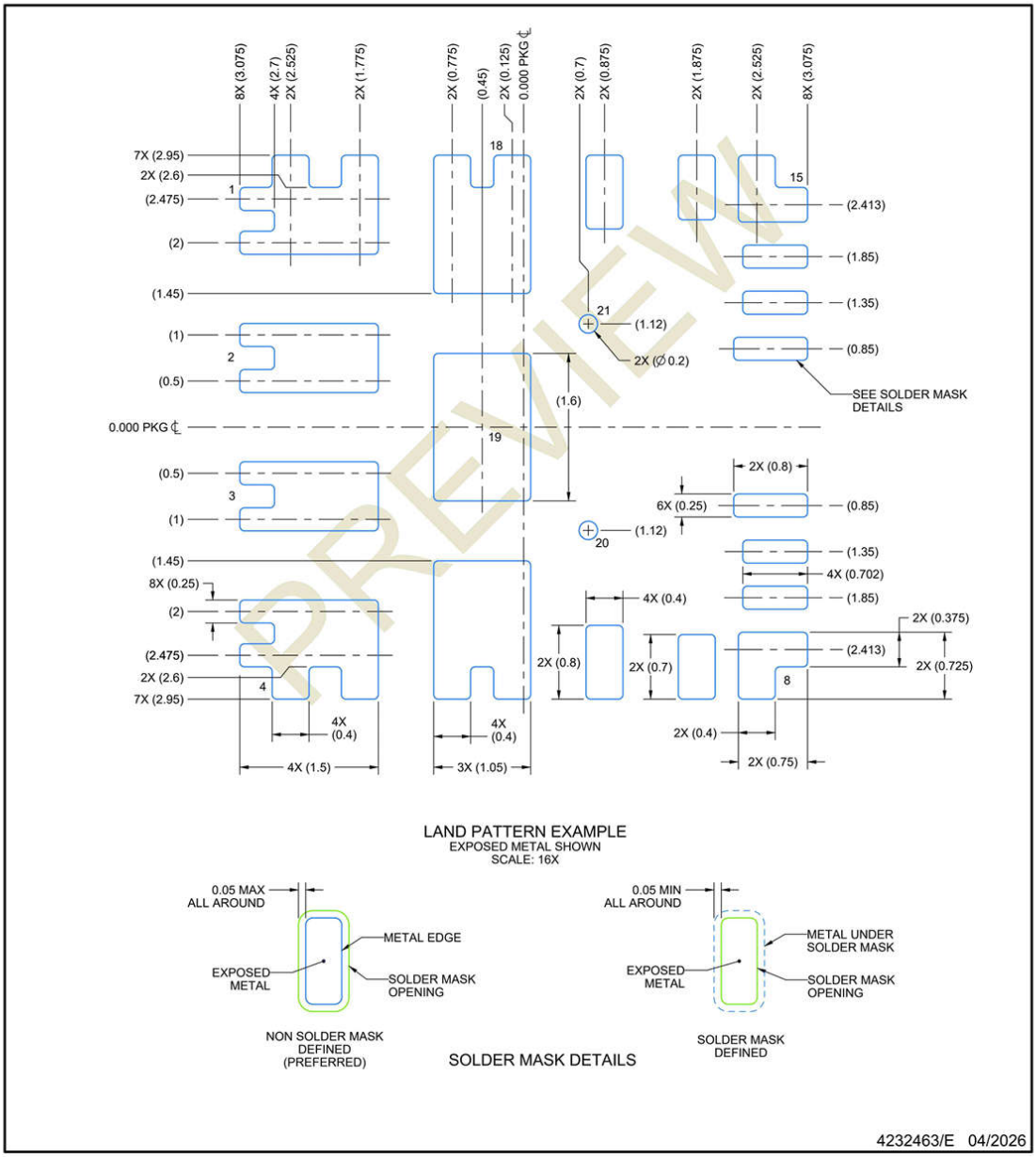
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RBL0021A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



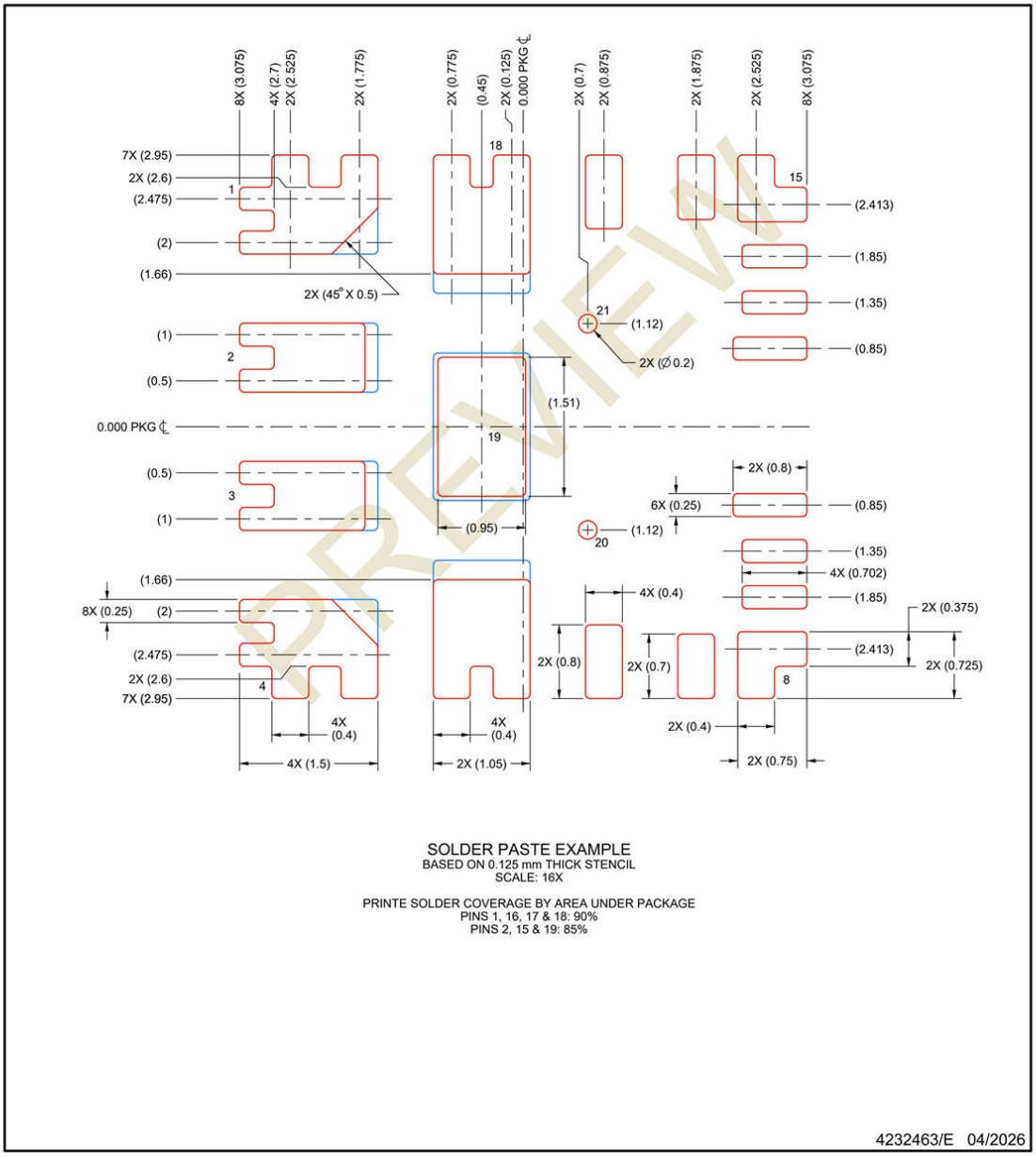
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RBL0021A — **VQFN-HR - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

PRINTE SOLDER COVERAGE BY AREA UNDER PACKAGE
PINS 1, 16, 17 & 18: 90%
PINS 2, 15 & 19: 85%

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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