TPS4H160-Q1 40V, 160mΩ Automotive Quad-Channel Smart High-Side Switch

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level H3A
  - Device CDM ESD classification level C4B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Quad-channel 160mΩ smart high-side switch with full diagnostics
  - Version A: open-drain digital output
  - Version B: current-sense analog output
- Wide operating voltage 3.4V to 40V
- Ultra-low standby current: <500nA
- High-accuracy current sense: ±15% under >25mA load
- Adjustable current limit with external resistor, ±15% under >500mA load
- Protection
  - Short-to-GND protection by current limit (internal or external)
  - Thermal shutdown with latch off option and thermal swing
  - Inductive load negative voltage clamp with optimized slew rate
  - Loss-of-GND and loss-of-battery protection
- Diagnostics
  - Overcurrent and short-to-ground detection
  - Open-load and short-to-battery detection
  - Global fault report for fast interrupt
- 28-pin thermally-enhanced PWP package

2 Applications

- ADAS modules
- Automotive display module
- Body control module

3 Description

The TPS4H160-Q1 device is fully protected quad-channel smart high-side switch with four integrated 160mΩ NMOS power FETs.

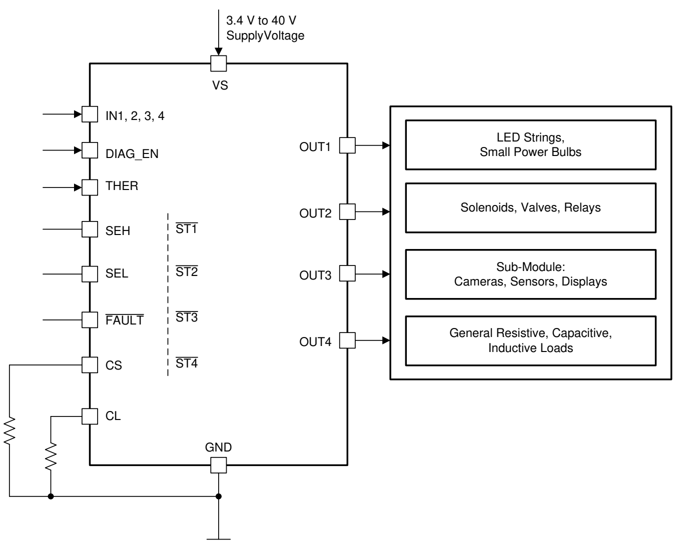
Full diagnostics and high-accuracy current sense enable intelligent control of the load.

An external adjustable current limit improves the reliability of whole system by limiting the inrush or overload current.

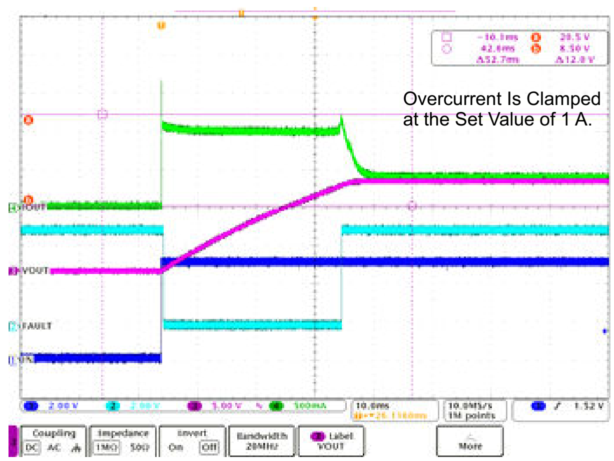
Package Information

PART NUMBER	PACKAGE(1)	CHANNELS
TPS4H160-Q1 Version A	PWP (HTSSOP, 28)	4
TPS4H160-Q1 Version B		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Schematic



Driving a Capacitive Load With Adjustable Current Limit

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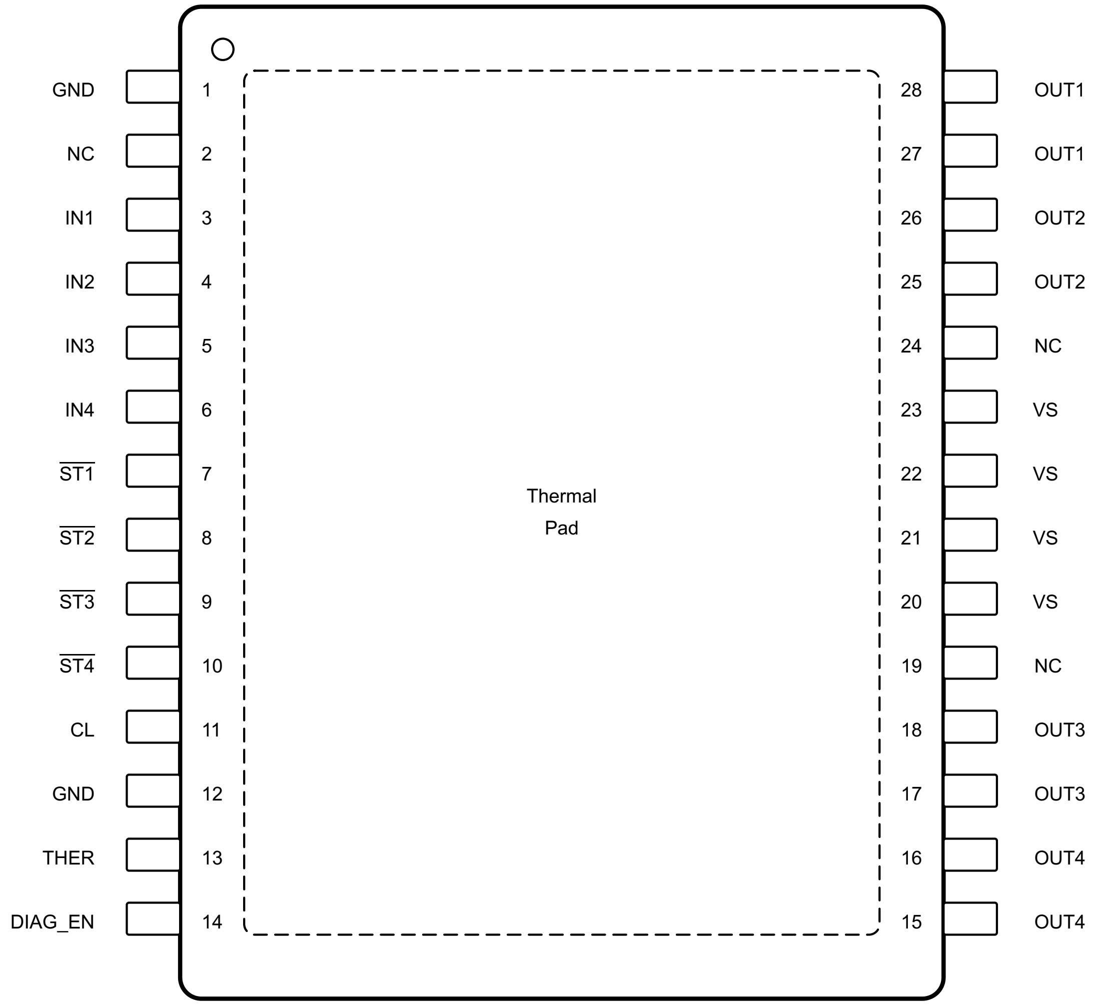
4 Device Comparison Table

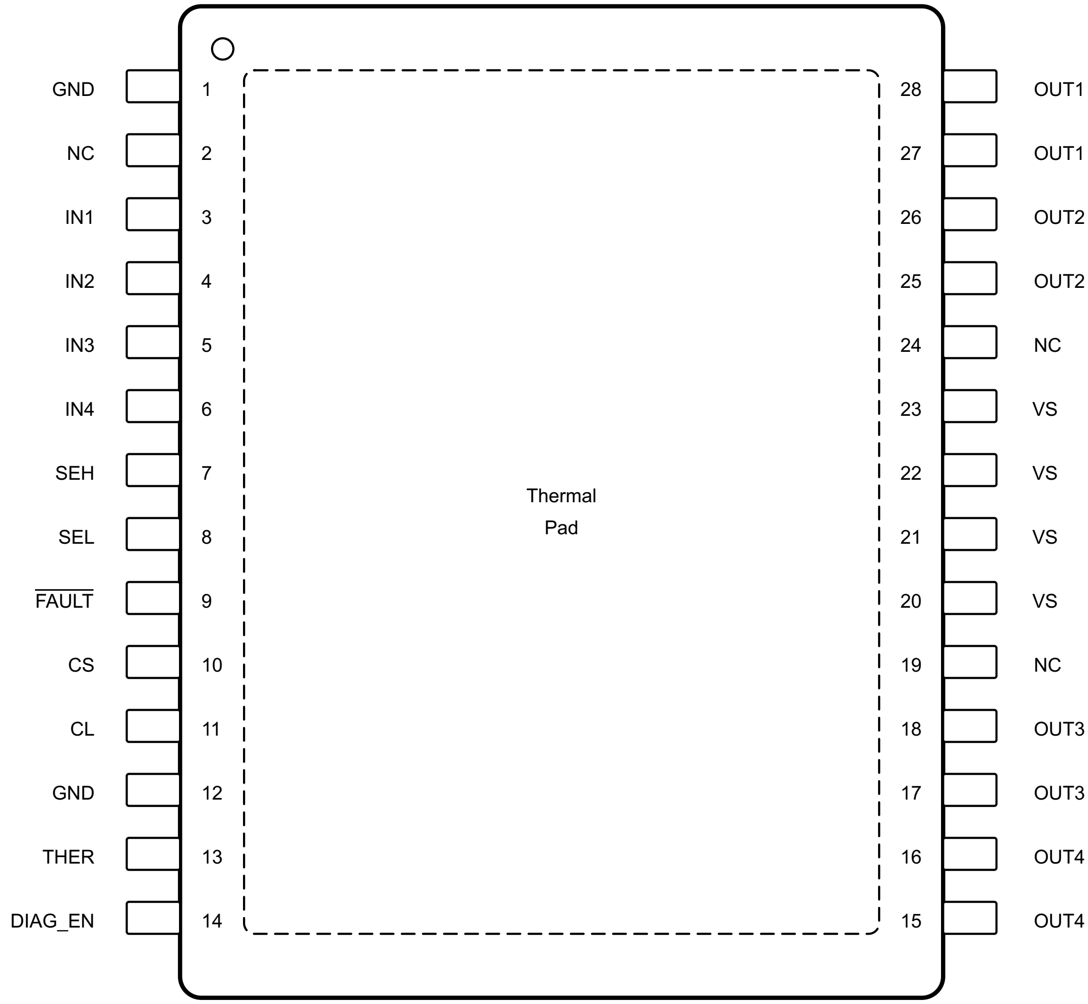
PART NO.	FAULT REPORTING MODE
TPS4H160-Q1 Version A	Open-drain digital output
TPS4H160-Q1 Version B	Current-sense analog output

5 Pin Configuration and Functions



NC – No internal connection

Figure 5-1. PWP Package, 28-Pin HTSSOP With Exposed Thermal Pad - Version A (Top View)



NC – No internal connection

Figure 5-2. PWP Package, 28-Pin HTSSOP With Exposed Thermal Pad - Version B (Top View)

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	VERSION A	VERSION B		
CL	11	11	O	Adjustable current limit. Connect to device GND if external current limit is not used.
CS	—	10	O	Current-sense output
DIAG_EN	14	14	I	Enable-disable pin for diagnostics; internal pulldown
FAULT	—	9	O	Global fault report with open-drain structure, ORed logic for quad-channel fault conditions
GND	1, 12	1, 12	—	Ground pin
IN1	3	3	I	Input control for channel 1 activation; internal pulldown
IN2	4	4	I	Input control for channel 2 activation; internal pulldown
IN3	5	5	I	Input control for channel 3 activation; internal pulldown
IN4	6	6	I	Input control for channel 4 activation; internal pulldown
NC	2, 19, 24	2, 19, 24	—	No internal connection
ST1	7	—	O	Open-drain diagnostic status output for channel 1

Table 5-1. Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	VERSION A	VERSION B		
$\overline{ST2}$	8	—	O	Open-drain diagnostic status output for channel 2
$\overline{ST3}$	9	—	O	Open-drain diagnostic status output for channel 3
$\overline{ST4}$	10	—	O	Open-drain diagnostic status output for channel 4
SEH	—	7	I	CS channel-selection high bit; internal pulldown
SEL	—	8	I	CS channel-selection low bit; internal pulldown
THER	13	13	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown
OUT1	27, 28	27, 28	O	Output of the channel 1 high side-switch, connected to the load
OUT2	25, 26	25, 26	O	Output of the channel 2 high side-switch, connected to the load
OUT3	17, 18	17, 18	O	Output of the channel 3 high side-switch, connected to the load
OUT4	15, 16	15, 16	O	Output of the channel 4 high side-switch, connected to the load
VS	20, 21, 22, 23	20, 21, 22, 23	I	Power supply
Thermal pad	—	—	—	Connect to device GND or leave floating

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) [1] [2]

		MIN	MAX	UNIT
Supply voltage	t < 400 ms		48	V
Reverse polarity voltage[3]		–36		V
Current on GND pin	t < 2 minutes	–100	250	mA
Voltage on INx, DIAG_EN, SEL, SEH, and THER pins		–0.3	7	V
Current on INx, DIAG_EN, SEL, SEH, and THER pins		–10	—	mA
Voltage on $\overline{\text{STx}}$ or $\overline{\text{FAULT}}$ pins		–0.3	7	V
Current on $\overline{\text{STx}}$ or $\overline{\text{FAULT}}$ pins		–30	10	mA
Voltage on CS pin		–2.7	7	V
Current on CS pin		—	30	mA
Voltage on CL pin		–0.3	7	V
Current on CL pin		—	6	mA
Inductive load switch-off energy dissipation, single pulse, single channel[4]		—	40	mJ
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground plane.
(3) Reverse polarity condition: t < 60 s, reverse current < $I_{R(2)}$, V_{INx} = 0 V, all channels reverse, GND pin 1-kΩ resistor in parallel with diode.
(4) Test condition: V_{VS} = 13.5 V, L = 8 mH, R = 0 Ω, T_J = 150°C. FR4 2s2p board, 2 × 70-µm Cu, 2 x 35-µm Cu. 600 mm^2 thermal pad copper area.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	All pins except VS, OUTx, GND	±4000	V
			Pins VS, OUTx, GND	±5000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±750	
			Corner pins (1, 14, 15, and 28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VS}	Supply operating voltage	4	40	V
	Voltage on INx, DIAG EN, SEL, SEH, and THER pins	0	5	V
	Voltage on $\overline{STx}$ and $\overline{FAULT}$ pins	0	5	V
	Nominal dc load current	0	2.5	A
T_A	Operating ambient temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS4H160-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	17.1	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	14.4	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.5	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	14.3	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

5 V < V_{VS} < 40 V; −40°C < T_J < 150°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING VOLTAGE						
$V_{VS(nom)}$	Nominal operating voltage		4		40	V
$V_{VS(uvr)}$	Undervoltage turnon	V_{VS} rises up	3.5	3.7	4	V
$V_{VS(uvf)}$	Undervoltage shutdown	V_{VS} falls down	3	3.2	3.4	V
$V_{(uv,hys)}$	Undervoltage shutdown, hysteresis			0.5		V
OPERATING CURRENT						
$I_{(op)}$	Nominal operating current[(1)]	V_{VS} = 13.5 V, V_{INx} = 5 V, V_{DIAG_EN} = 0 V, I_{OUTx} = 0.5 A, current limit = 2 A, all channels on			8	mA
$I_{(off)}$	Standby current	V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTx} = THER = 0 V, T_J = 25°C			0.5	µA
		V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{CS} = V_{CL} = V_{OUTx} = THER = 0 V, T_J = 125°C			5	
$I_{(off,diag)}$	Standby current with diagnostic enabled	V_{VS} = 13.5 V, V_{INx} = 0 V, V_{DIAG_EN} = 5 V, $V_{VS} – V_{OUTx}$ > $V_{(ol,off)}$, not in open-load mode			5	mA
$t_{(off,diag)}$	Standby mode deglitch time[(1)]	IN from high to low, if deglitch time > $t_{(off,deg)}$, the device enters into standby mode.	10	12.5	15	ms
$I_{lkg(out)}$	Output leakage current in off-state	V_{VS} = 13.5 V, V_{INx} = V_{DIAG_EN} = V_{OUTx} = 0			3	µA
POWER STAGE						
$r_{DS(on)}$	On-state resistance[(1)]	V_{VS} ≥ 3.5 V, T_J = 25°C		165		mΩ
		V_{VS} ≥ 3.5 V, T_J = 150°C			280	
$I_{CL(int)}$	Internal current limit	Internal current limit value, CL pin connected to GND	8		14	A
$I_{CL(TSD)}$	Current limit during thermal shutdown[(1)]	Internal current limit value under thermal shutdown		6.5		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value		70%		
$V_{DS(clamp)}$	Drain-to-source internal clamp voltage		50		70	V

6.5 Electrical Characteristics (continued)

5 V < V_{VS} < 40 V; −40°C < T_J < 150°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DIODE CHARACTERISTICS						
V_F	Drain−source diode voltage	IN = 0, I_{OUTx} = −0.15 A.	0.3	0.7	0.9	V
$I_{R(1)}$, $I_{R(2)}$	Continuous reverse current from source to drain[(1)]	t < 60 s, V_{INx} = 0 V, T_J = 25°C, single channel reversed, short-to-battery condition		2.5		A
		t < 60 s, V_{INx} = 0 V, GND pin 1-kΩ resistor in parallel with diode. T_J = 25°C. Reverse-polarity condition, all channels reversed		2		
LOGIC INPUT (INx, DIAG_EN, SEL, SEH, THER)						
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{(logic,pd)}$	Logic-pin pulldown resistor	INx, SEL, SEH, THER, V_{INx} = V_{SEL} = V_{SEH} = V_{THER} = 5 V	100	175	250	kΩ
		DIAG_EN. V_{VS} = V_{DIAG_EN} = 5 V	200	275	350	
DIAGNOSTICS						
$I_{lkg(GND\_loss)}$	Output leakage current under GND loss condition				100	µA
$V_{(ol,off)}$	Open-load detection threshold	IN = 0 V, when V_{VS} – V_{OUTx} < $t_{(ol,off)}$, duration longer than $t_{(ol,off)}$, then open load is detected, off state	1.6		2.6	V
$t_{d(ol,off)}$	Open-load detection threshold deglitch time (see Figure 6-3)	IN = 0 V, when V_{VS} – V_{OUTx} < $V_{(ol,off)}$, duration longer than $t_{(ol,off)}$, then open load is detected, off state	300	550	800	µs
$I_{(ol,off)}$	Off-state output sink current	V_{INx} = 0 V, V_{DIAG_EN} = 5 V, V_{VS} = V_{OUTx} = 13.5 V, T_J = 125°C, open load	–75			µA
$V_{OL(STx)}$	Status low-output voltage	I_{STx} = 2 mA, version A only			0.2	V
$V_{OL(FAULT)}$	Fault low-output voltage	I_{FAULT} = 2 mA, version B only			0.2	V
$t_{CL(deg)}$	Deglitch time when current limit occurs[(1)]	V_{INx} = V_{DIAG_EN} = 5 V, the deglitch time from current limit toggling to $\overline{FAULT}$, $\overline{STx}$, CS report.	80		180	µs
$T_{(SD)}$	Thermal shutdown threshold[(1)]		160	175		°C
$T_{(SD,rst)}$	Thermal shutdown status reset threshold[(1)]			155		°C
$T_{(SW)}$	Thermal swing shutdown threshold[(1)]			60		°C
$T_{(hys)}$	Hysteresis for resetting the thermal shutdown or thermal swing[(1)]			10		°C
CURRENT SENSE (Version B) AND CURRENT LIMIT						
$K_{(CS)}$	Current-sense ratio			300		
$K_{(CL)}$	Current-limit ratio			2500		
$V_{CL(th)}$	Current limit internal threshold[(1)]			0.8		V
$dK_{(CS)}$ / $K_{(CS)}$	Current-sense accuracy, (I_{CS} × $K_{(CS)}$ – I_{OUTx}) /I_{OUTx} × 100	V_{VS} = 13.5 V, I_{OUTx} ≥ 5 mA	–65%		65%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 25 mA	–15%		15%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 50 mA	–8%		8%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 100 mA	–4%		4%	
		V_{VS} = 13.5 V, I_{OUTx} ≥ 0.5 A	–3%		3%	
$dK_{(CL)}$ / $K_{(CL)}$	External current limit accuracy[(2)] (I_{OUTx} – I_{CL} × $K_{(CL)}$) × 100 / (I_{CL} × $K_{(CL)}$)	V_{VS} = 13.5 V, $I_{(limit)}$ ≥ 0.25 A	–20%		20%	
		V_{VS} = 13.5 V, 0.5 A ≤ $I_{(limit)}$ ≤ 7 A	–15%		15%	
$V_{CS(lin)}$	Current-sense voltage linear range[(1)]	V_{VS} ≥ 6.5 V	0		4	V
		5 V ≤ V_{VS} < 6.5 V	0		V_{VS} – 2.5	
$I_{OUTx(lin)}$	Output-current linear range[(1)]	V_{VS} ≥ 6.5 V, $V_{CS(lin)}$ ≤ 4 V	0		2.5	A
		5 V ≤ V_{VS} < 6.5 V, $V_{CS(lin)}$ ≤ V_{VS} – 2.5 V	0		2.5	
$V_{CS(H)}$	Current sense pin output voltage	V_{VS} ≥ 7 V, fault mode	4.5		6.5	V
		5 V ≤ V_{VS} < 7 V, fault mode	Min(V_{VS} – 2, 4.5)		6.5	V
$I_{CS(H)}$	Current-sense pin output current	V_{CS} = 4.5 V, V_{VS} = 13.5 V	15			mA

6.5 Electrical Characteristics (continued)

5 V < V_{VS} < 40 V; −40°C < T_J < 150°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{lkg(CS)}$	Current-sense leakage current in disabled mode	V_{DIAG_EN} = 0 V, T_J =125°C			0.5	µA

(1) Value specified by design, not subject to production test
(2) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting

6.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Delay time, V_{OUTx} 10% after $V_{INx}\uparrow$ (See Figure 6-1.)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, IN rising edge to 10% of V_{OUTx}	20	50	90	µs
$t_{d(off)}$	Delay time, V_{OUTx} 90% after $V_{INx}\downarrow$ (See Figure 6-1.)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, IN falling edge to 90% of V_{OUTx}	20	50	90	µs
dV/dt(on)	Turnon slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, V_{OUTx} from 10% to 90%	0.1	0.3	0.55	V/µs
dV/dt(off)	Turnoff slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A, V_{OUTx} from 90% to 10%	0.1	0.3	0.55	V/µs
$t_{d(match)}$	$t_{d(rise)} - t_{d(fall)}$ (See Figure 6-1.)	V_{VS} = 13.5 V, I_L = 0.5A. $t_{d,\ rise}$ is the IN rising edge to V_{OUTx} = 90%. $t_{d(fall)}$ is the IN falling edge to V_{OUTx} = 10%.	–50		50	µs
CURRENT-SENSE CHARACTERISTICS (See Figure 6-2.)						
$t_{CS(off1)}$	CS settling time from DIAG_EN disabled[(1)]	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUTx} = 0.5 A. current limit = 2 A. DIAG_EN falling edge to 10% of V_{CS}.			20	µs
$t_{CS(on1)}$	CS settling time from DIAG_EN enabled[(1)]	V_{VS} = 13.5 V, V_{INx} = 5 V, I_{OUTx} = 0.5 A. current limit is 2 A. DIAG_EN rising edge to 90% of V_{CS}.			20	µs
$t_{CS(off2)}$	CS settling time from IN falling edge	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A. current limit = 2 A. IN falling edge to 10% of V_{CS}	30		100	µs
$t_{CS(on2)}$	CS settling time from IN rising edge	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.5 A. current limit = 2 A. IN rising edge to 90% of V_{CS}	50		150	µs
t_{SEx}	Multi-sense transition delay from channel to channel	V_{DIAG_EN} = 5 V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	µs

(1) Value specified by design, not subject to production test

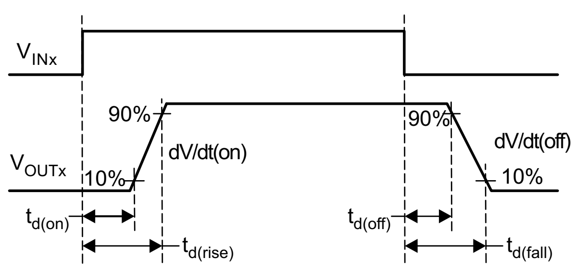


Figure 6-1. Output Delay Characteristics

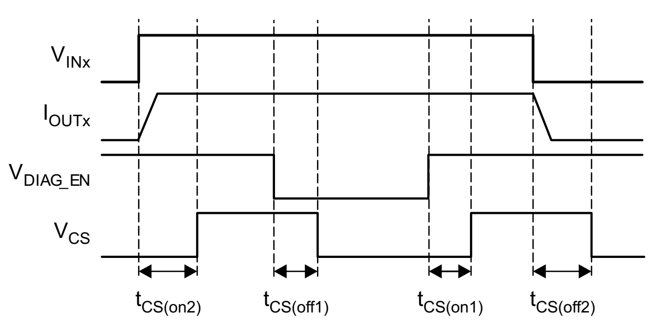


Figure 6-2. CS Delay Characteristics

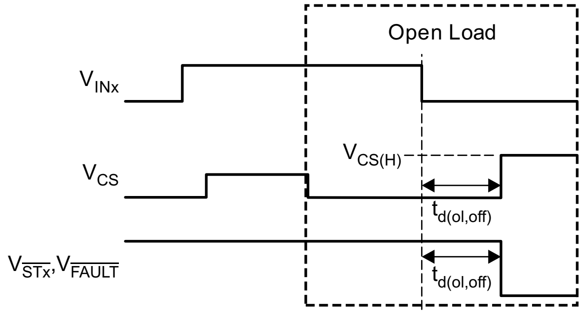


Figure 6-3. Open-Load Blanking-Time Characteristics

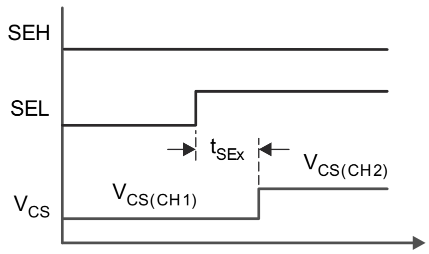


Figure 6-4. Multi-Sense Transition Delay

6.7 Typical Characteristics

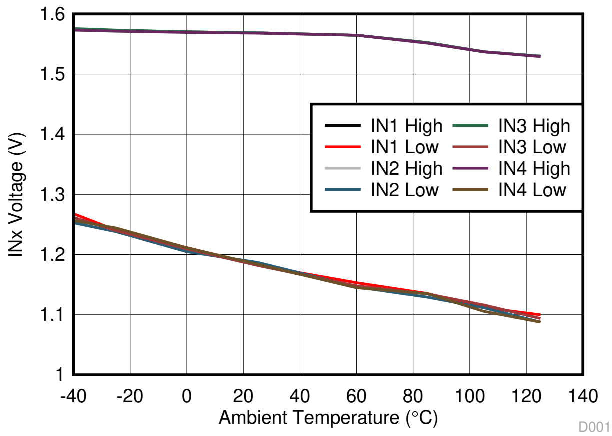


Figure 6-5. INx Voltage Threshold

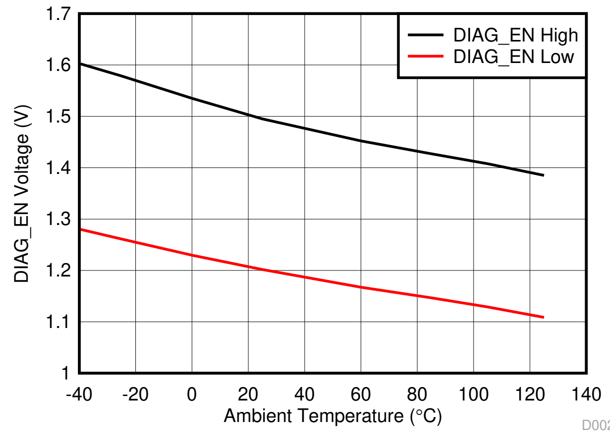


Figure 6-6. DIAG_EN Voltage Threshold

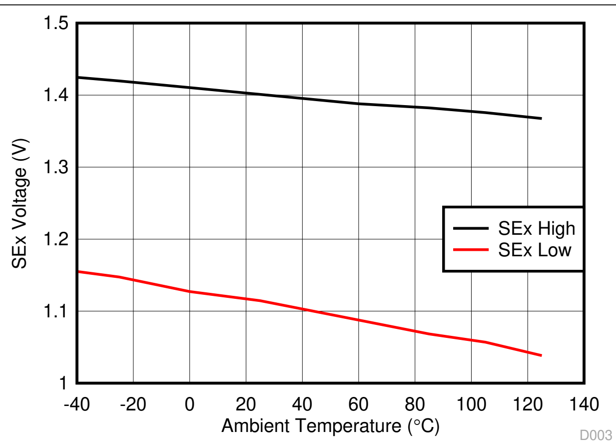


Figure 6-7. SEx Voltage Threshold

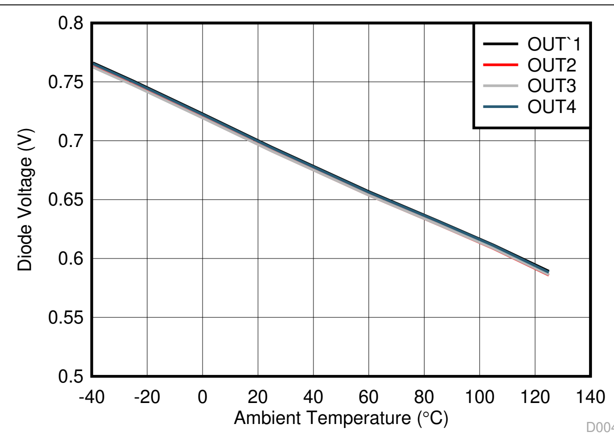


Figure 6-8. Body-Diode Forward Voltage

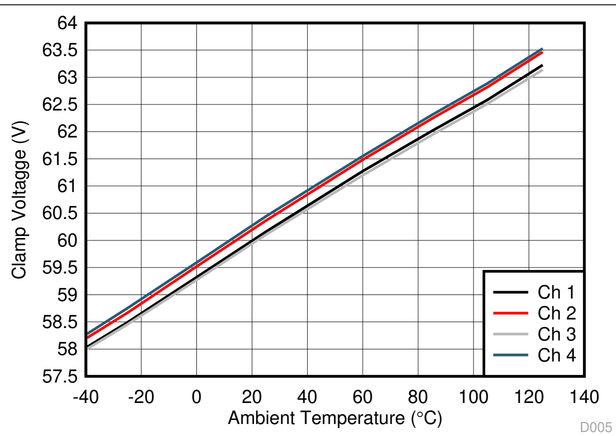


Figure 6-9. Drain-to-Source Clamp Voltage

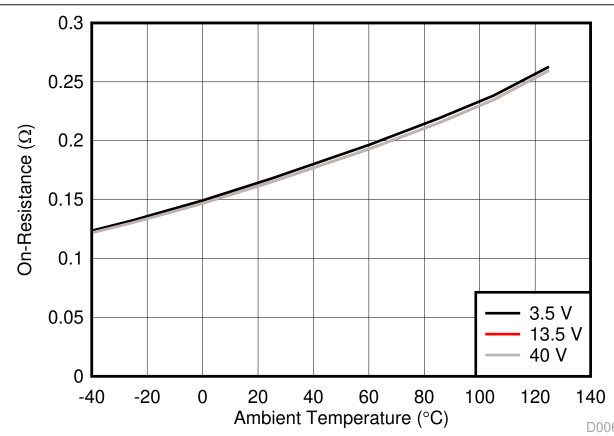


Figure 6-10. Channel-1 FET On-Resistance

6.7 Typical Characteristics (continued)

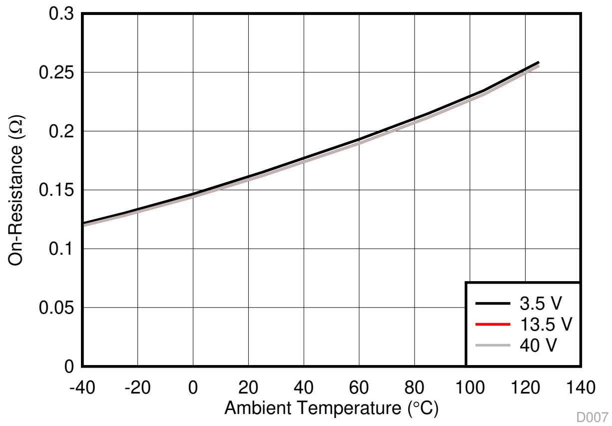


Figure 6-11. Channel-2 FET On-Resistanc

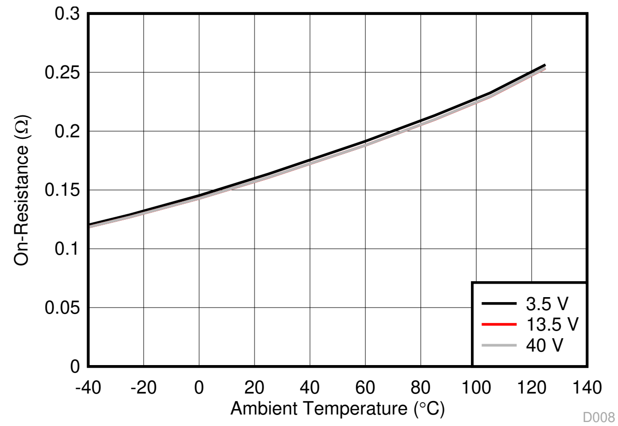


Figure 6-12. Channel-3 FET On-Resistanc

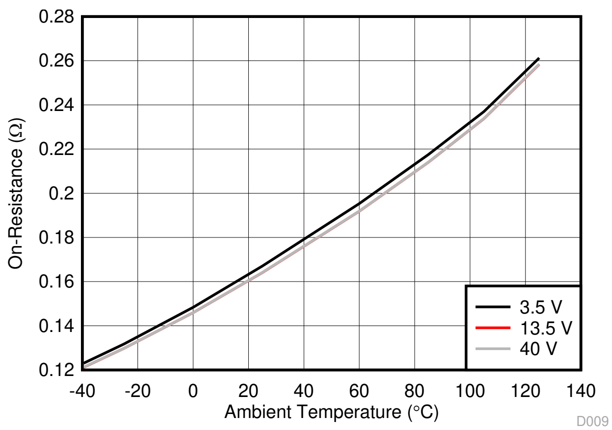


Figure 6-13. Channel-4 FET On-Resistanc

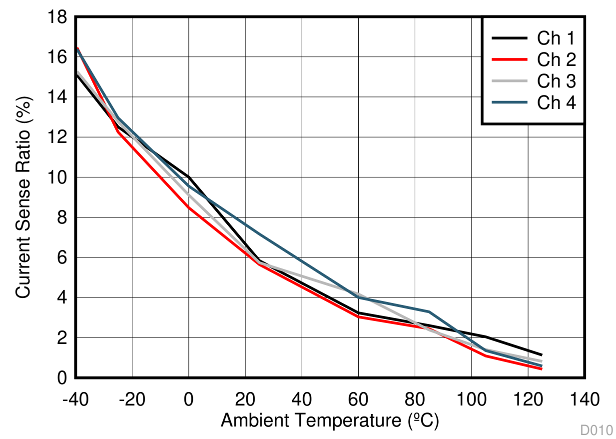


Figure 6-14. Current-Sense Ratio at 5 mA

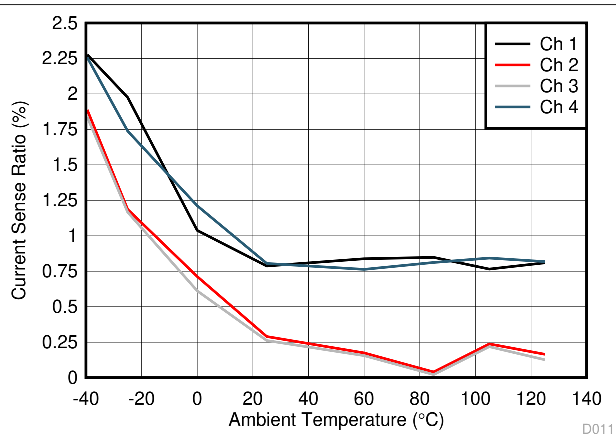


Figure 6-15. Current-Sense Ratio at 25 mA

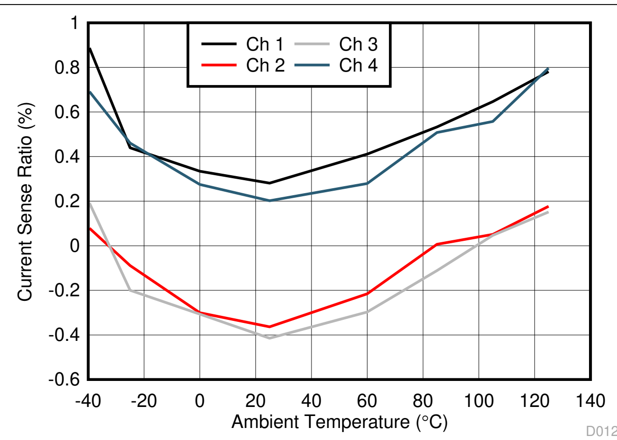


Figure 6-16. Current-Sense Ratio at 50 mA

6.7 Typical Characteristics (continued)

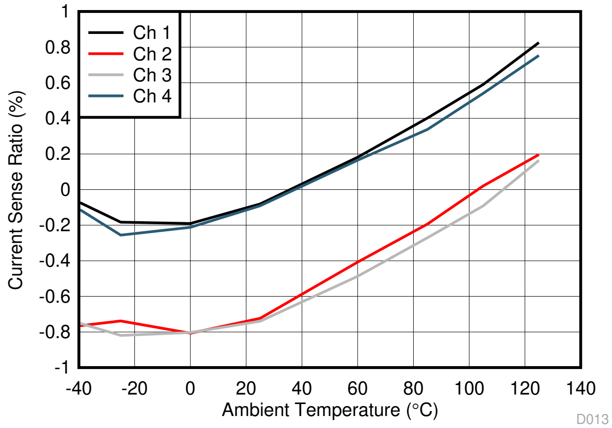


Figure 6-17. Current-Sense Ratio at 100 mA

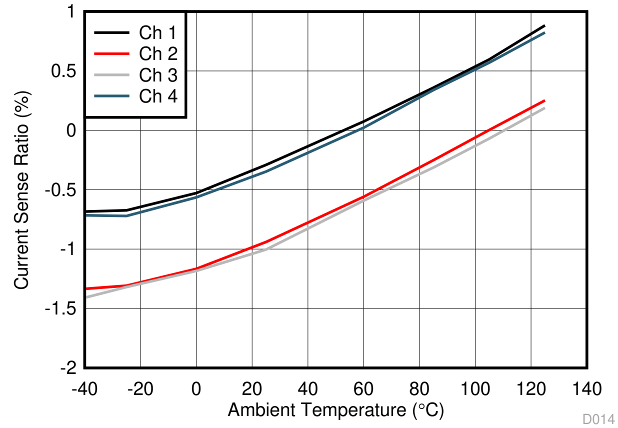


Figure 6-18. Current-Sense Ratio at 500 mA

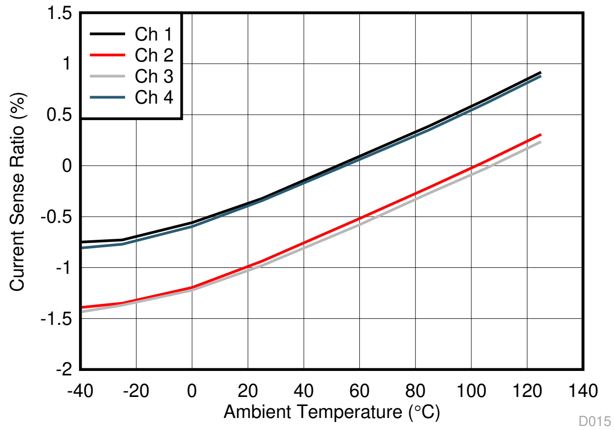


Figure 6-19. Current-Sense Ratio at 1 A

7 Detailed Description

7.1 Overview

The TPS4H160-Q1 device is a smart high-side switch, with internal charge pump and quad-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. The device has two versions with different diagnostic reporting, the open-drain digital output (version A) and the current-sense analog output (version B).

For version A, the device implements the digital fault report with an open-drain structure. When a fault occurs, the device pulls $\overline{STx}$ down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. The digital status of each channel can report individually, or globally by connecting the $\overline{STx}$ pins together.

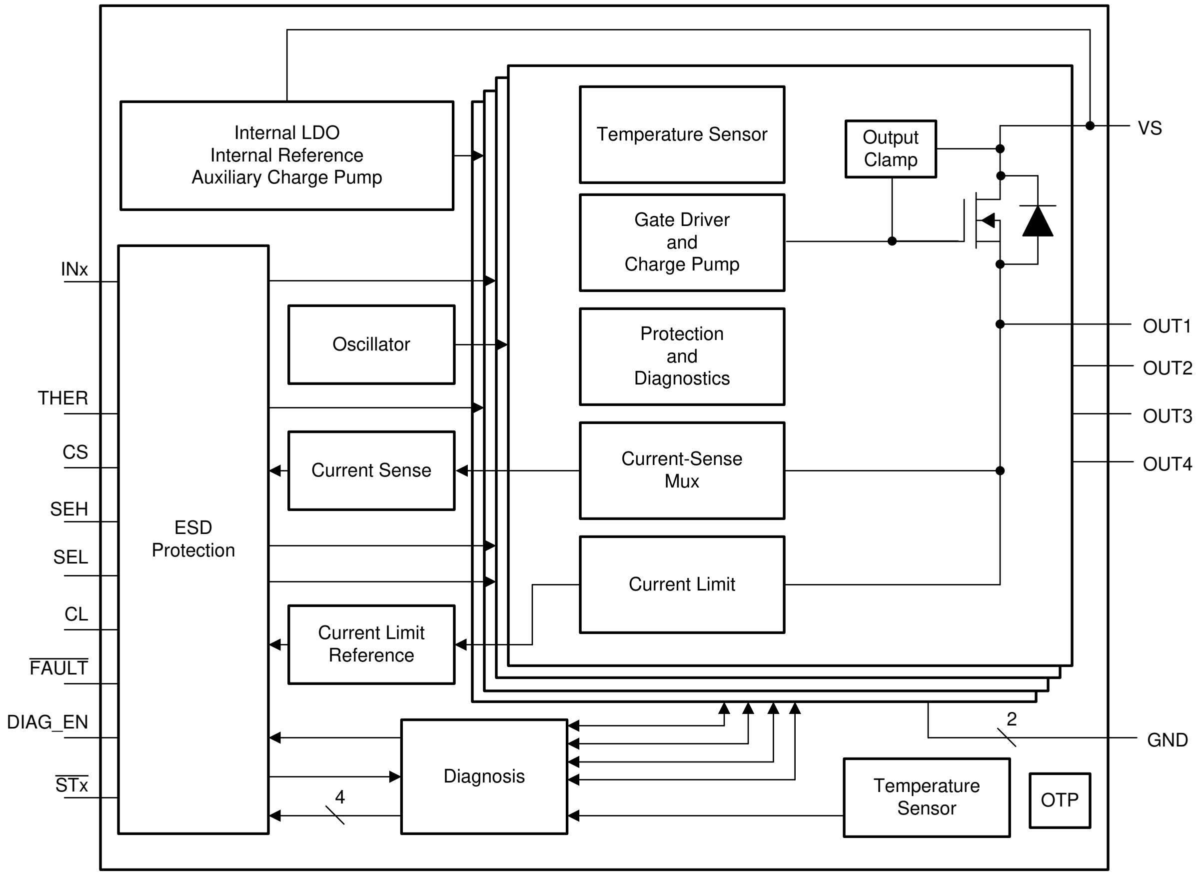
For version B, high-accuracy current sense makes the diagnostics more accurate without further calibration. One integrated current mirror can source 1 / $K_{(CS)}$ of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal. $K_{(CS)}$ is a constant value across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of $V_{CS(H)}$.

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Besides, the device also implements an internal current limit with a fixed value.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS4H160-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on their respective pins are as shown by the arrows in Figure 7-1. All voltages are measured relative to the ground plane.

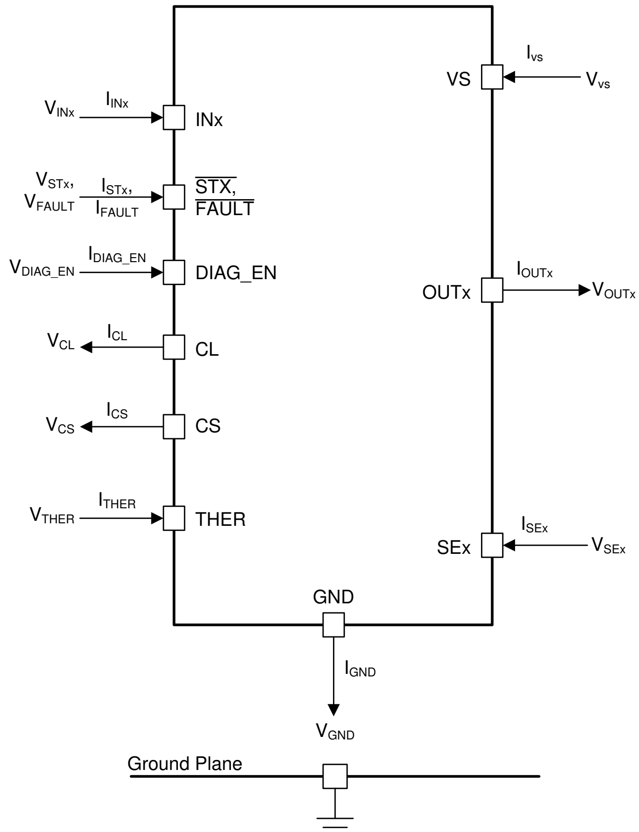


Figure 7-1. Voltage and Current Conventions

7.3.2 Accurate Current Sense

High-accuracy current sense is implemented in the version-B device. It allows a better real-time monitoring effect and more-accurate diagnostics without further calibration.

One integrated current mirror can source 1 / $K_{(CS)}$ of the load current, and the mirrored current flows into the external current sense resistor to become a voltage signal. The current mirror is shared by the four channels. $K_{(CS)}$ is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device is calibrated accurately during production, so post-calibration is not required. See Figure 7-2 for more details.

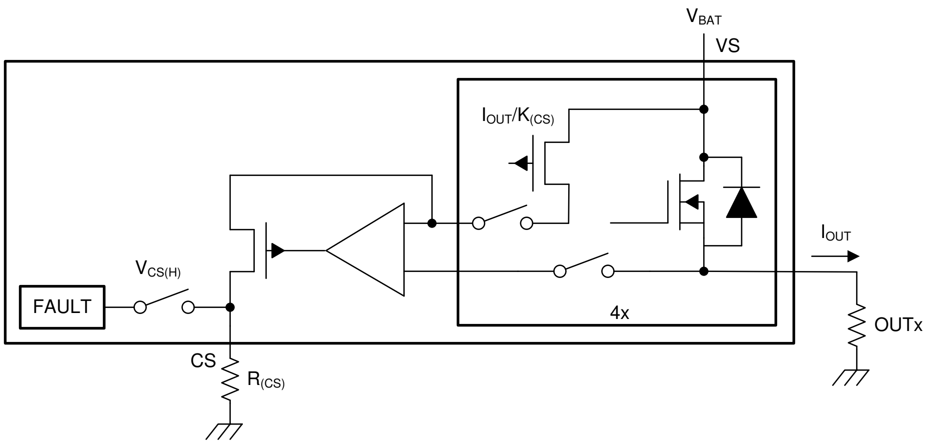


Figure 7-2. Current-Sense Block Diagram

When a fault occurs, the CS pin also works as a fault report with a pullup voltage, $V_{CS(H)}$. See Figure 7-3 for more details.

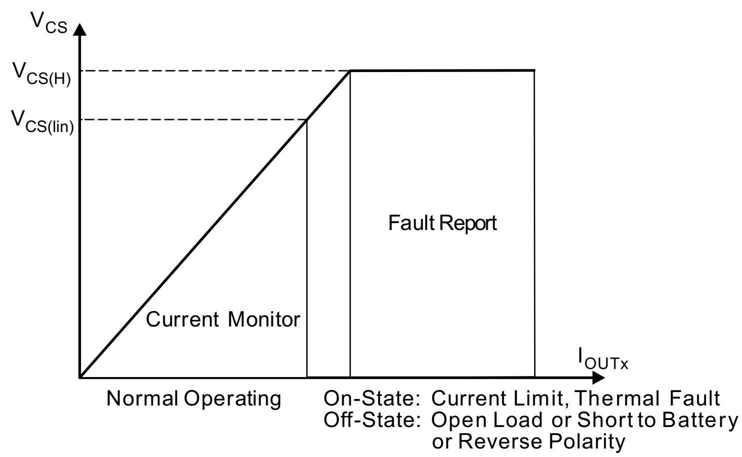


Figure 7-3. Current-Sense Output-Voltage Curve

Use Equation 1 to calculate $R_{(CS)}$.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUTx}} \tag{1}$$

Take the following points into consideration when calculating $R_{(CS)}$.

- Ensure V_{CS} is within the current-sense linear region (V_{CS}, $I_{OUTx(lin)}$) across the full range of the load current. Check $R_{(CS)}$ with Equation 2.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \leq \frac{V_{CS(lin)}}{I_{CS}} \tag{2}$$

- In fault mode, ensure I_{CS} is within the source capacity of the CS pin ($I_{CS(H)}$). Check $R_{(CS)}$ with Equation 3.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \geq \frac{V_{CS(H,min)}}{I_{CS(H,min)}} \tag{3}$$

7.3.3 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{CL(TSD)}$ to reduce the power dissipation on the power FET. See Figure 7-4 for more details.

The device has two current-limit thresholds.

- Internal current limit – The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit – An external resistor is used to set the current-limit threashold. Use the Equation 4 to calculate the $R_{(CL)}$. $V_{CL(th)}$ is the internal band-gap voltage. $K_{(CL)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

$$I_{CL} = \frac{V_{CL(th)}}{R_{(CL)}} = \frac{I_{OUT}}{K_{(CL)}}$$

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \quad (4)$$

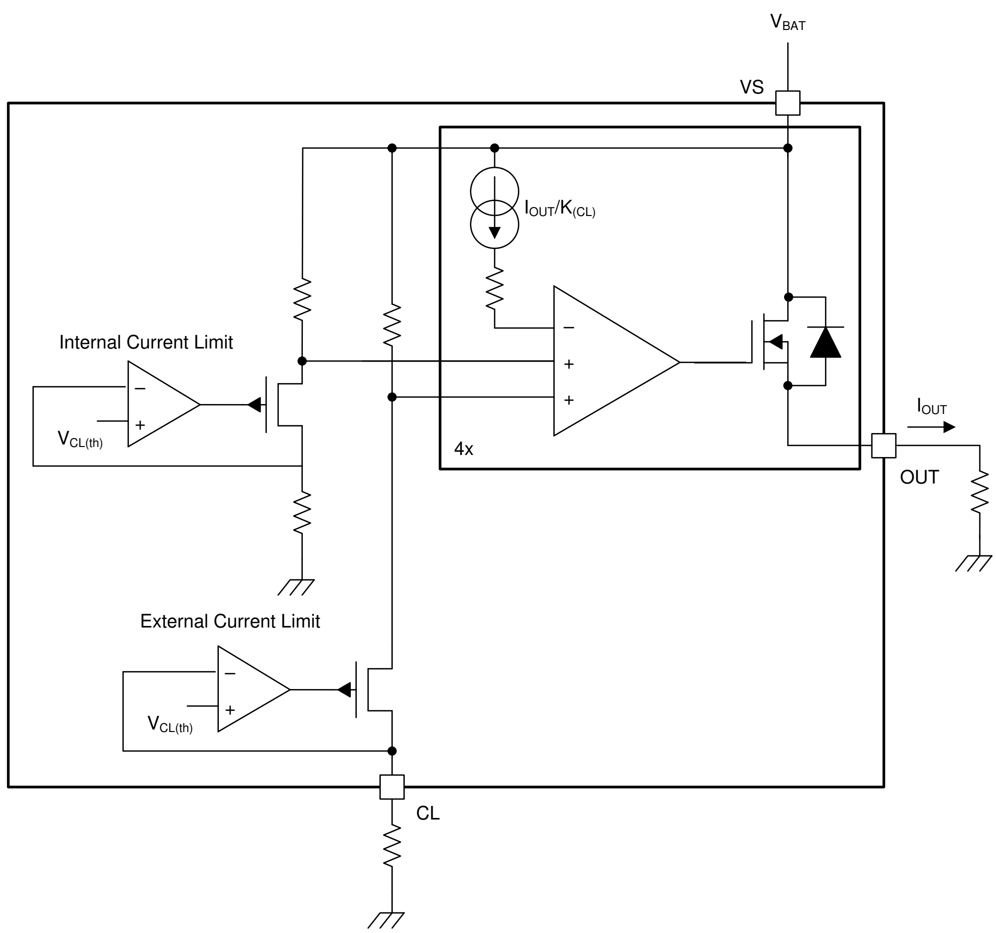


Figure 7-4. Current-Limit Block Diargam

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected with device GND.

For better protection from a hard short-to-GND condition (when the INx pins are enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the related channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 µs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

7.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \quad (5)$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \quad (6)$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

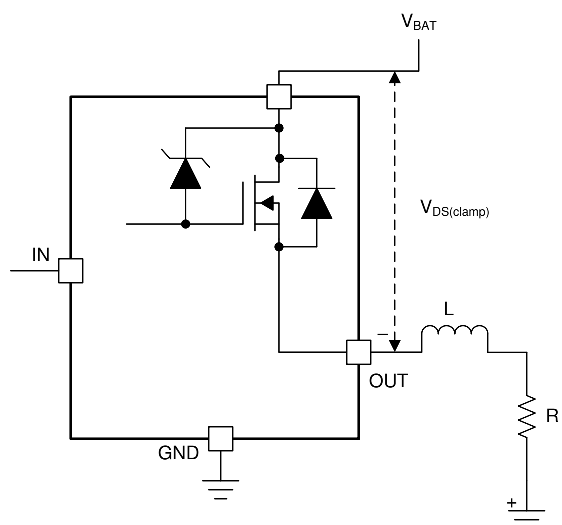


Figure 7-5. Drain-to-Source Clamping Structure

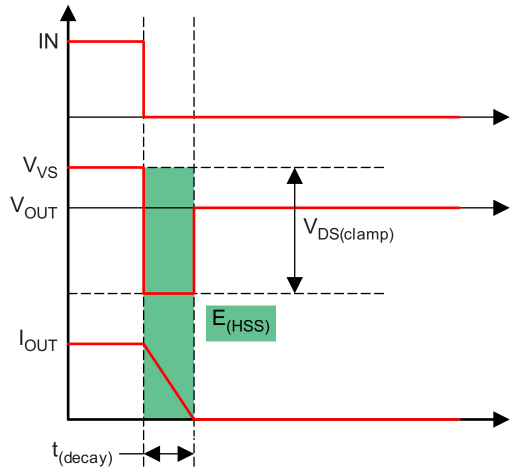


Figure 7-6. Inductive Load Switching-Off Diagram

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)\,dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (7)$$

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I^2_{OUT(max)} \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \quad (8)$$

Figure 7-7 is a waveform of the device driving an inductive load, and Figure 7-8 is waveform with an expanded time scale. Channel 1 is the IN signal, channel 2 is the supply voltage V_{VS}, channel 3 is the output voltage V_{OUT}, channel 4 is the output current I_{OUT}, and channel M is the measured power dissipation $E_{(HSS)}$.

On the waveform, the duration of V_{OUT} from V_{VS} to (V_{VS} – $V_{DS(clamp)}$) is around 120 μs. The device also optimizes the switching-off slew rate when the clamp is active. This optimization can help the system design by keeping the effects of transient power and EMI to a minimum. As shown in Figure 7-7 and Figure 7-8, the controlled slew rate is around 0.5 V/μs.

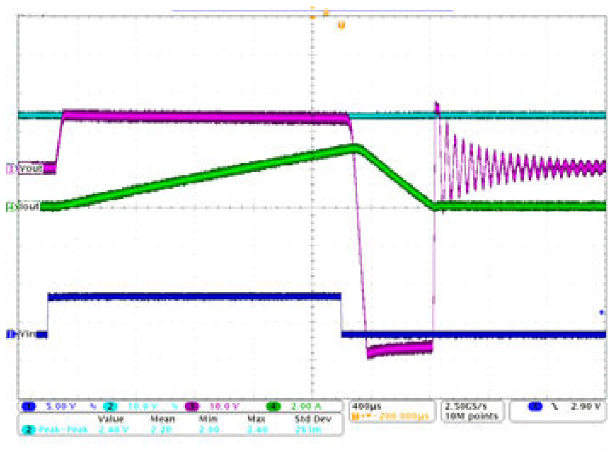


Figure 7-7. Inductive Load Switching-Off Waveform

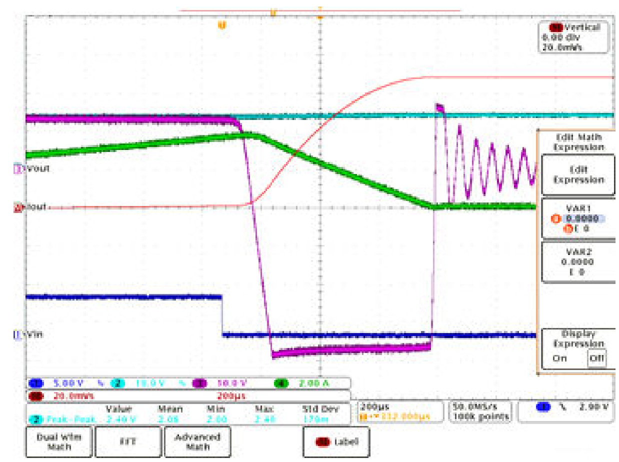


Figure 7-8. Inductive Load Switching-Off Expanded Waveform

Note that for PWM-controlled inductive loads, it is recommended to add the external freewheeling circuitry shown in Figure 7-9 to protect the device from repetitive power stressing. TVS is used to achieve the fast decay. See Figure 7-9 for more details.

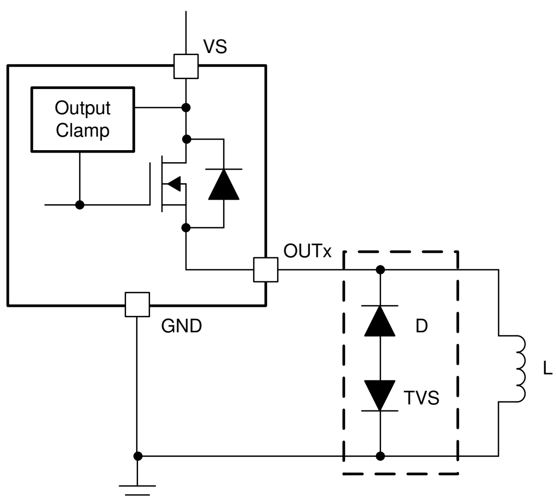


Figure 7-9. Protection With External Circuitry

7.3.5 Fault Detection and Reporting

7.3.5.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and INx low.

7.3.5.2 Multiplexing of Current Sense

For version B, SEL and SEH are two pins to multiplex the shared current-sense function among the four channels. See Table 7-1 for more details.

Table 7-1. Diagnosis Configuration Table

DIAG_EN	INx	SEH	SEL	CS ACTIVATED CHANNEL	CS, $\overline{\text{FAULT}}$, $\overline{\text{STx}}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	—	High impedance	Diagnostics disabled, full protection
	L					Diagnostics disabled, no protection
H	—	0	0	Channel 1	See Table 7-2	See Table 7-2
		0	1	Channel 2		
		1	0	Channel 3		
		1	1	Channel 4		

7.3.5.3 Fault Table

Table 7-2 applies when the DIAG_EN pin is enabled.

Table 7-2. Fault Table

CONDITIONS	INx	OUTx	THER	CRITERION	$\overline{\text{STx}}$ (VER. A)	CS (VER. B)	$\overline{\text{FAULT}}$ (VER. B)	FAULT RECOVERY
Normal	L	L	—	—	H	0	H	—
	H	H	—	—	H	In linear region	H	—
Overlaod, short to ground	H	L	—	Current limit triggered	L	$V_{CS(H)}$	L	Auto
Open load[(1)], short to battery, reverse polarity	L	H	—	$V_{VS} – V_{OUTx} < V_{(ol,off)}$	L	$V_{CS(H)}$	L	Auto
Thermal shutdown	H	—	L	T_{SD} triggered	L	$V_{CS(H)}$	L	Output auto-retry. Fault recovers when $T_J < T_{(SD,rst)}$ or when INx toggles.
			H					Output latch off. Fault recovers when INx toggles.
Thermal swing	H	—	—	T_{SW} triggered	L	$V_{CS(H)}$	L	Auto

(1) An external pullup is required for open-load detection.

7.3.5.4 $\overline{\text{STx}}$ and $\overline{\text{FAULT}}$ Reporting

For version A, four individual $\overline{\text{STx}}$ pins report the fault conditions, each pin for its respective channel. When a fault condition occurs, it pulls $\overline{\text{STx}}$ down to GND. A 3.3- or 5-V external pullup is required to match the supply level of the microcontroller. The digital status of each channel can be reported individually, or globally by connecting all the $\overline{\text{STx}}$ pins together.

For version B, a global $\overline{\text{FAULT}}$ pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the $\overline{\text{FAULT}}$ pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the microcontroller.

After the $\overline{\text{FAULT}}$ report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The CS pin also works as a fault report with an internal pullup voltage, $V_{CS(H)}$.

7.3.6 Full Diagnostics

7.3.6.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{CL(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

7.3.6.2 Open-Load Detection

7.3.6.2.1 Channel On

When a channel on, benefiting from the high-accuracy current sense in a small current range, if an open-load event occurs, it can be detected as an ultralow V_{CS} and handled by the microcontroller. Note that the detection is not reported on the $\overline{STx}$ or $\overline{FAULT}$ pins. The microcontroller must multiplex the SEL and SEH pins to detect the channel-on open-load fault proactively.

7.3.6.2.2 Channel Off

When a channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{VS} - V_{OUTx} < V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 20 kΩ.

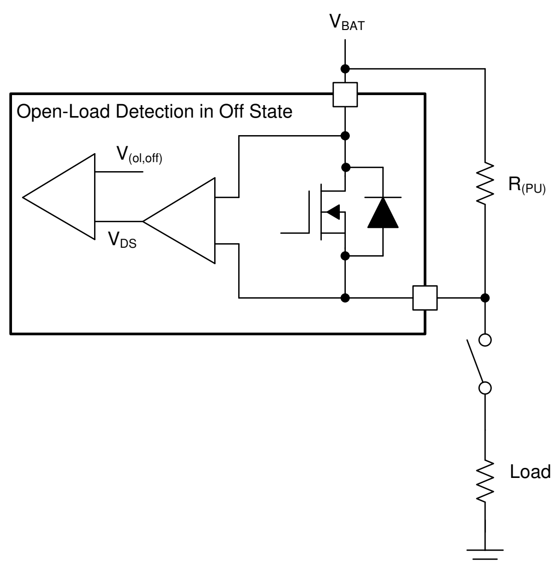


Figure 7-10. Open-Load Detection in Off-State

7.3.6.3 Short-to-Battery Detection

Short-to-battery has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Table 7-2 for more details.

In the on-state, reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state.

- If $V_{OUTx} - V_{VS} < V_{(F)}$ (body diode forward voltage), no reverse current occurs.
- If $V_{OUTx} - V_{VS} > V_{(F)}$, reverse current occurs. The current must be limited to less than $I_{R(1)}$. Setting an INx pin high can minimize the power stress on its channel. Also, for external reverse protection, see Reverse-Current Protection for more details.

7.3.6.4 Reverse Polarity Detection

Reverse polarity detection has the same detection mechanism and behavior as open-load detection both in the on-state and off-state. See Table 7-2 for more details.

In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state. The reverse current must be limited to less than $I_{R(2)}$. Set the related INx pin high to keep the power dissipation to a minimum. For external reverse-blocking circuitry, see Reverse-Current Protection for more details.

7.3.6.5 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

7.3.6.5.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thefrmal shutdown occurs, the respective output turns off. The THER pin is used to configure the behavior after the thermal shutdown occurs.

- When the THER pin is low, thermal shutdown operates in the auto-retry mode. The output automatically recovers when $T_J < T_{(SD)} – T_{(hys)}$, but the current is limited to $I_{CL(TSD)}$ to avoid repetitive thermal shutdown. The thermal shutdown fault signal is cleared when $T_J < T_{(SD,rst)}$ or after toggling the related INx pin.
- When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related INx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} – T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} – T_{(Logic)} < T_{(sw)} – T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation. As shown in Figure 7-11, multiple thermal swings are triggered before thermal shutdown occurs.

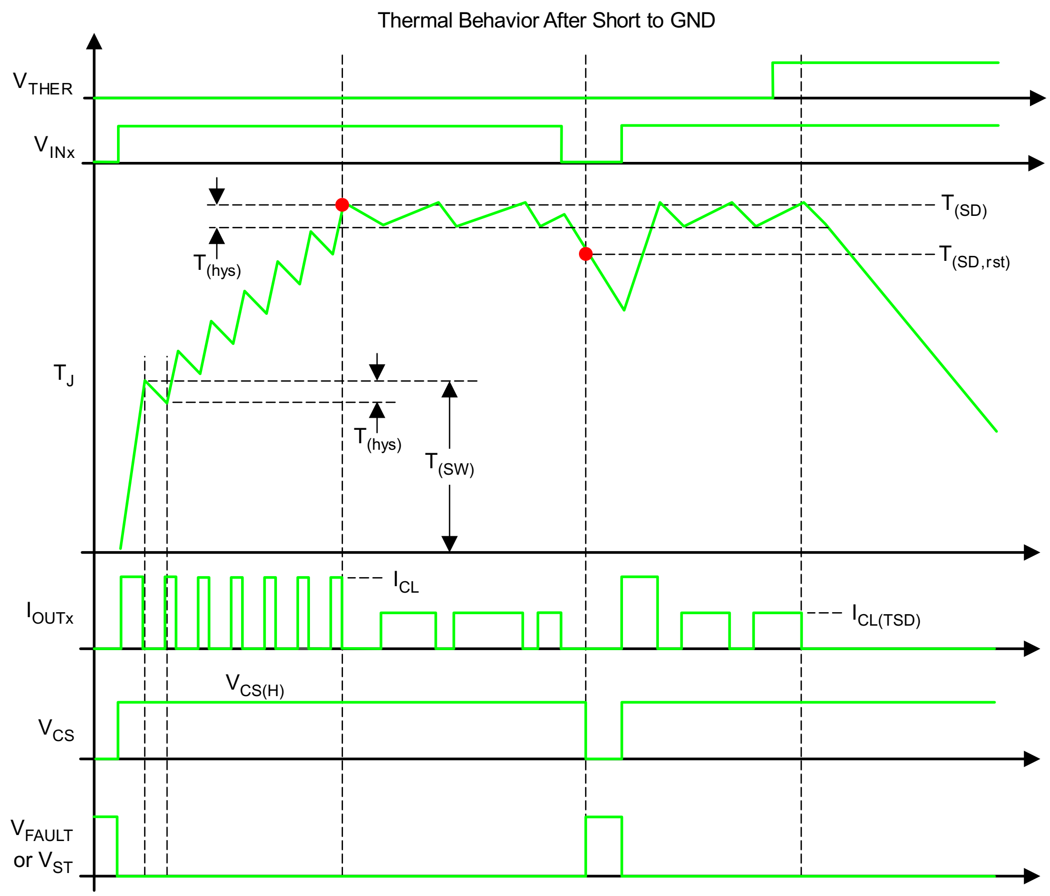


Figure 7-11. Thermal Behavior Diagram

7.3.7 Full Protections

7.3.7.1 UVLO Protection

The device monitors the supply voltage V_{VS}, to prevent unpredicted behaviors when V_{VS} is too low. When V_{VS} falls down to $V_{VS(uvf)}$, the device shuts down. When V_{VS} rises up to $V_{VS(uvr)}$, the device turns on.

7.3.7.2 Loss-of-GND Protection

When loss of GND occurs, output is shut down regardless of whether the INx pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND. If the forward voltage of the reverse current protection diode in the GND network exceeds the 0.6 V recommendation, the device may indicate a false loss of GND detection.

7.3.7.3 Protection for Loss of Power Supply

When loss of supply occurs, the output is shut down regardless of whether the INx pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the I/O pins to maintain the inductance current. To protect the system in this condition, TI recommends two types of external protections: the GND network or the external free-wheeling diode.

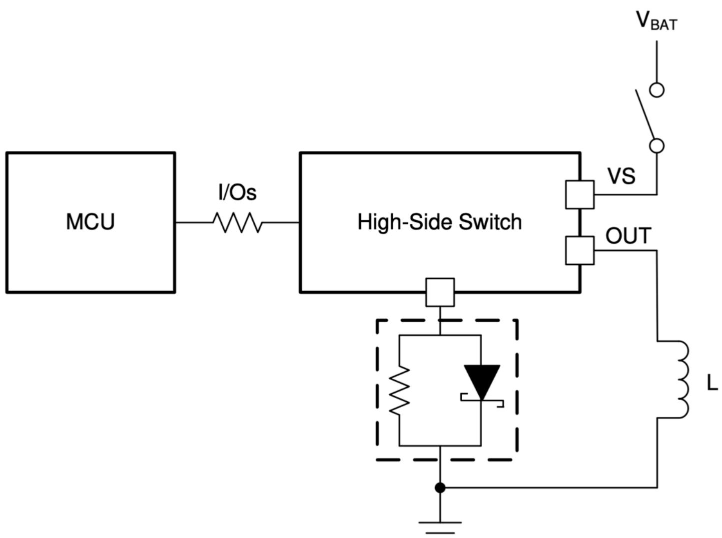


Figure 7-12. Protection for Loss of Power Supply, Method 1

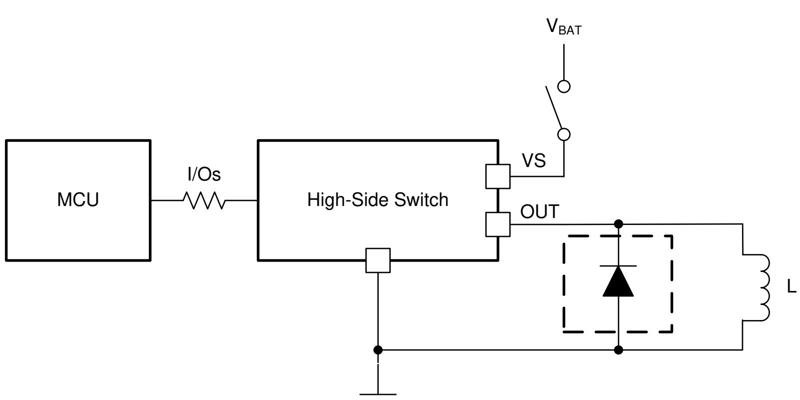


Figure 7-13. Protection for Loss of Power Supply, Method 2

7.3.7.4 Reverse-Current Protection

Reverse current occurs in two conditions: short to battery and reverse polarity.

- When a short to the battery occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current. The GND pin maximum current is specified in the Absolute Maximum Ratings.

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

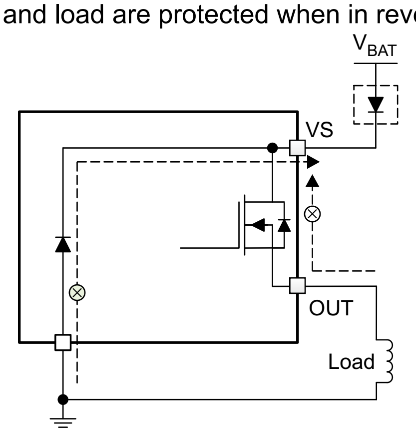


Figure 7-14. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with an >100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

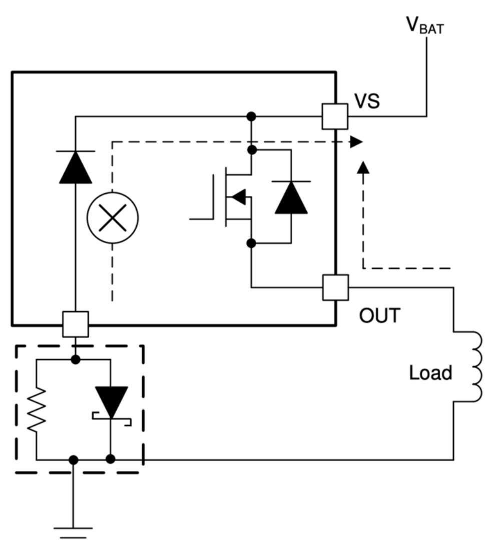


Figure 7-15. Reverse-Current External Protection, Method 2

7.3.7.5 MCU I/O Protection

In some severe conditions, such as the ISO7637-2 test or the loss of battery with inductive loads, a negative pulse occurs on the GND pin This pulse can cause damage on the connected microcontroller. TI recommends serial resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

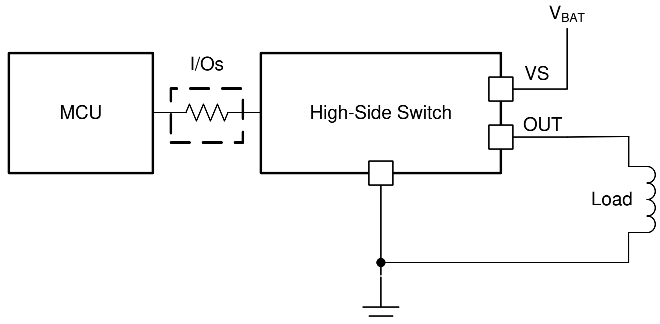


Figure 7-16. MCU I/O External Protection

7.4 Device Functional Modes

7.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics.

Note that IN must be low for $t > t_{(off,deg)}$ to enter the standby mode, where $t_{(off,deg)}$ is the standby mode deglitch time used to avoid false triggering. Figure 7-17 shows a working-mode diagram.

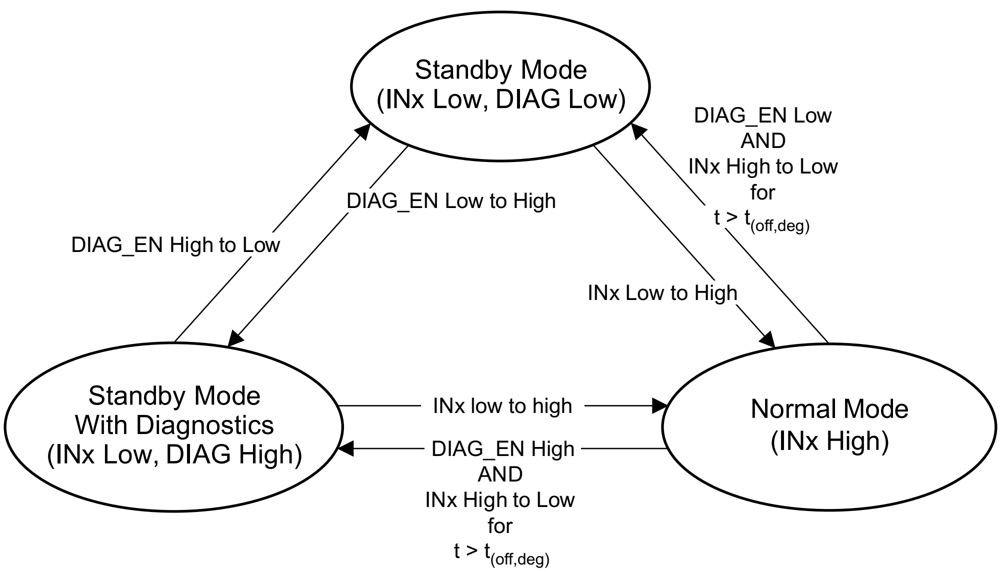


Figure 7-17. Working Modes

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS4H160-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

8.2 Typical Application

The following figure shows an example of the external circuitry connections based on the version-B device.

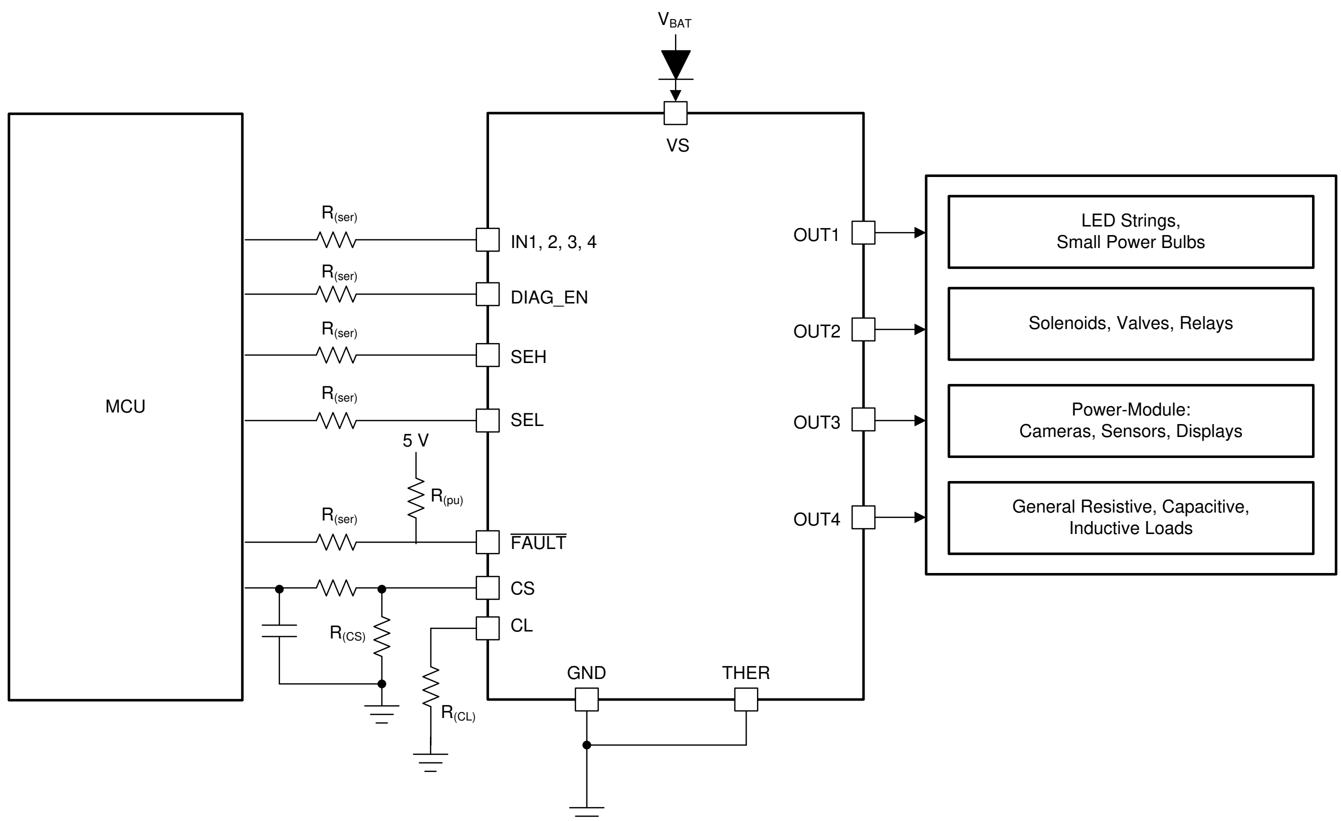


Figure 8-1. Typical Application Diagram

8.2.1 Design Requirements

- V_{VS} range from 9 V to 16 V
- Load range is from 0.1 A to 1 A for each channel
- Current sense for fault monitoring
- Expected current-limit value of 2.5 A
- Automatic recovery mode when thermal shutdown occurs
- Full diagnostics with 5-V MCU
- Reverse-voltage protection with a blocking diode in the power-supply line

8.2.2 Detailed Design Procedure

To keep the 1-A nominal current in the 0 to 4-V current-sense range, calculate the $R_{(CS)}$ resistor using Equation 9. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUT}} = \frac{4 \times 300}{1} = 1200\ \Omega \quad (9)$$

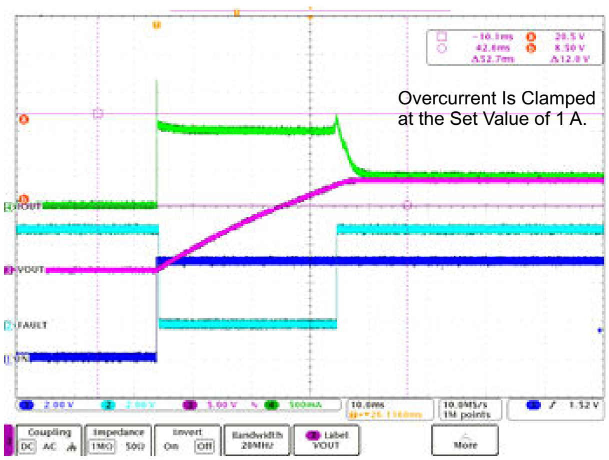
To set the adjustable current limit value at 2.5-A, calculate $R_{(CL)}$ using Equation 10.

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 2500}{2.5} = 800\ \Omega \quad (10)$$

TI recommends $R_{(ser)}$ = 10 kΩ for 5-V MCU, and $R_{(pu)}$ = 10 kΩ as the pullup resistor.

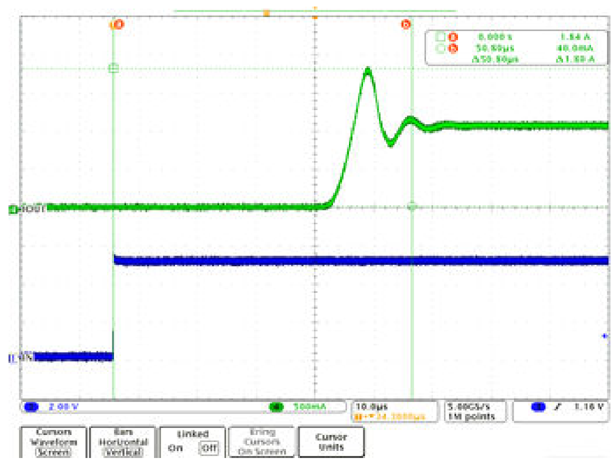
8.2.3 Application Curves

Figure 8-2 shows a test example of soft-start when driving a big capacitive load. Figure 8-3 shows an expanded waveform of the output current.



V_S = 12 V; INx = ↑; Current limit = 1 A
Load current = 0.4 A; C_L = 2.3 mF; CH1 = INx
CH2 = $\overline{FAULT}$; CH3 = output voltage; CH4 = output current

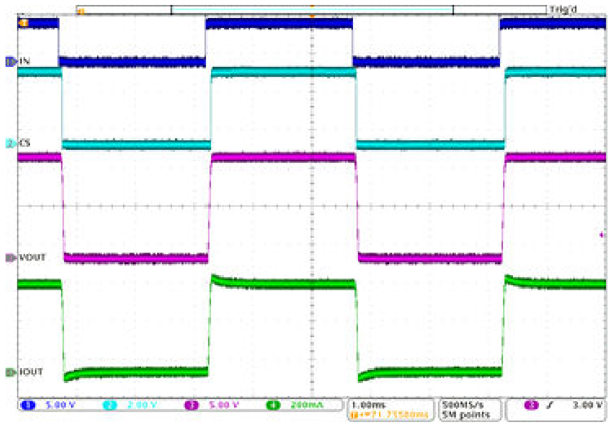
Figure 8-2. Driving a Capacitive Load With Adjustable Current Limit



V_{VS} = 12 V; INx = ↑; Current limit = 1 A
Load current = 0.4 A; C_L = 2.3 mF; CH1 = INx
CH2 = $\overline{FAULT}$; CH3 = output voltage; CH4 = output current

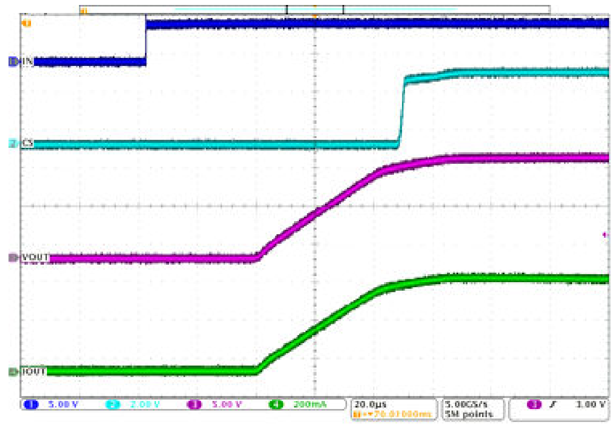
Figure 8-3. Driving a Capacitive Load, Expanded Waveform

Figure 8-4 shows a test example of PWM-mode driving. Figure 8-5 shows the expanded waveform of the rising edge. Figure 8-6 shows the expanded waveform of the falling edge.



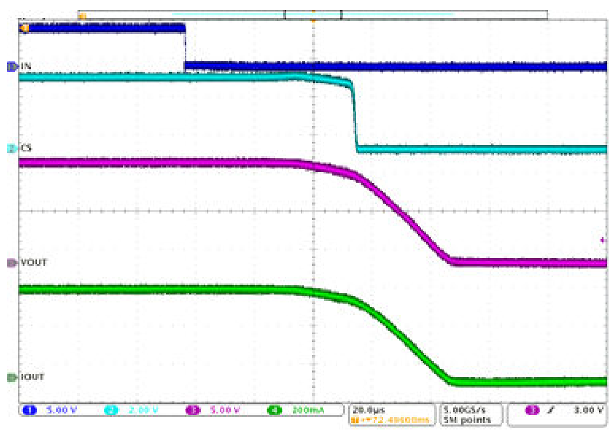
V_{VS} = 13.5 V INx = 200-Hz PWM at 50% duty cycle CH1 = INx signal
CH2 = CS voltage CH3 = output voltage CH4 = output current

Figure 8-4. PWM Signal Driving



V_{VS} = 13.5 V INx = 200-Hz PWM at 50% duty cycle CH1 = INx signal
CH2 = CS voltage CH3 = output voltage CH4 = output current

Figure 8-5. Expanded Waveform of Rising Edge



V_{VS} = 13.5 V INx = 200-Hz PWM at 50% duty cycle CH1 = INx signal
CH2 = CS voltage CH3 = output voltage CH4 = output current

Figure 8-6. Expanded Waveform of Falling Edge

8.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system or 24-V industrial system. Detailed supply voltage should be within the range specified in the *Recommended Operating Conditions*.

8.4 Layout

8.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

8.4.2 Layout Examples

8.4.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

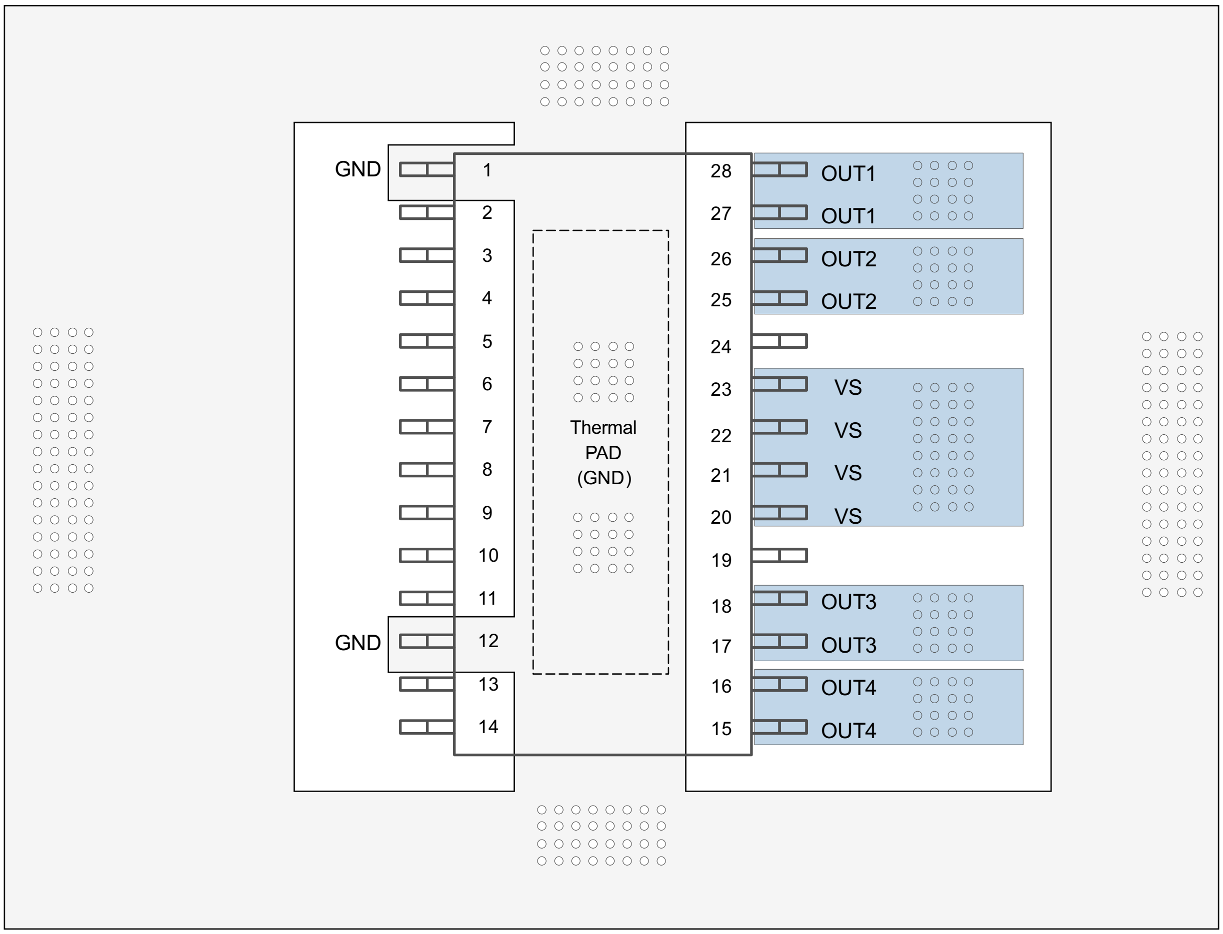


Figure 8-7. Layout Example Without a GND Network

8.4.2.2 With a GND Network

With a GND network, tie the thermal pad as one trace to the board GND copper.

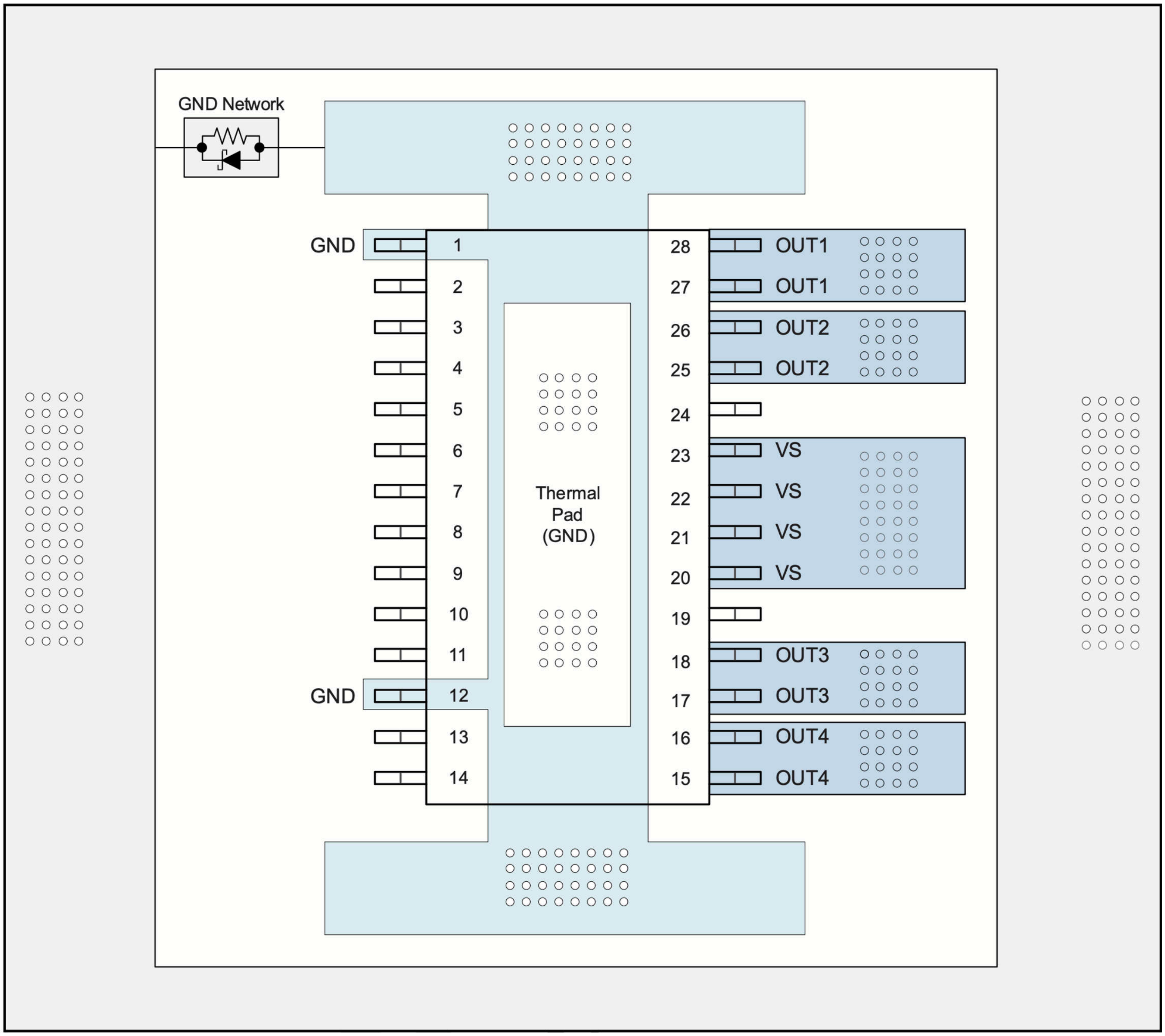


Figure 8-8. Layout Example With a GND Network

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2019) to Revision E (June 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the documents................1
- Added clarification on the reverse current protection diode in the *Loss-of-GND Protection* section................25
- Changed the standard diode to a Schottky diode in the Protection for Loss of Power Supply, Method 1 and Protection for Loss of Power Supply, Method 2 figures in the *Protection for Loss of Power Supply* section... 25
- Changed the standard diode to a Schottky diode in the Layout Example With a GND Network figure in the *With a GND Network* section...32

Changes from Revision C (March 2018) to Revision D (December 2019) **Page**

- Added Functional safety capable link to the *Features* section.. 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS4H160AQPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4H160AQ
TPS4H160AQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4H160AQ
TPS4H160BQPWPRQ1	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4H160BQ
TPS4H160BQPWPRQ1.A	Active	Production	HTSSOP (PWP) | 28	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4H160BQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

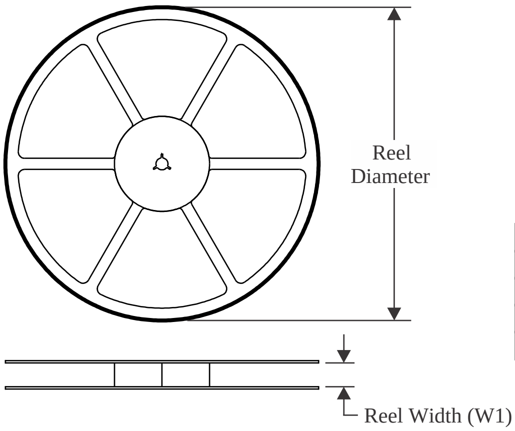
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

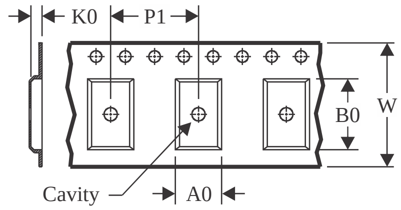
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

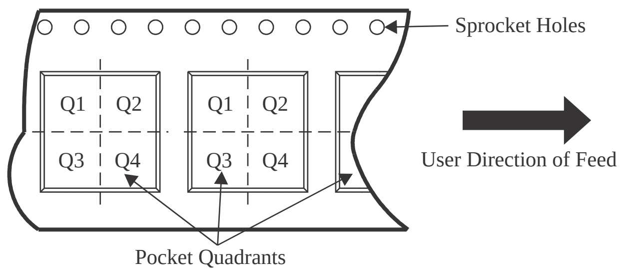


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

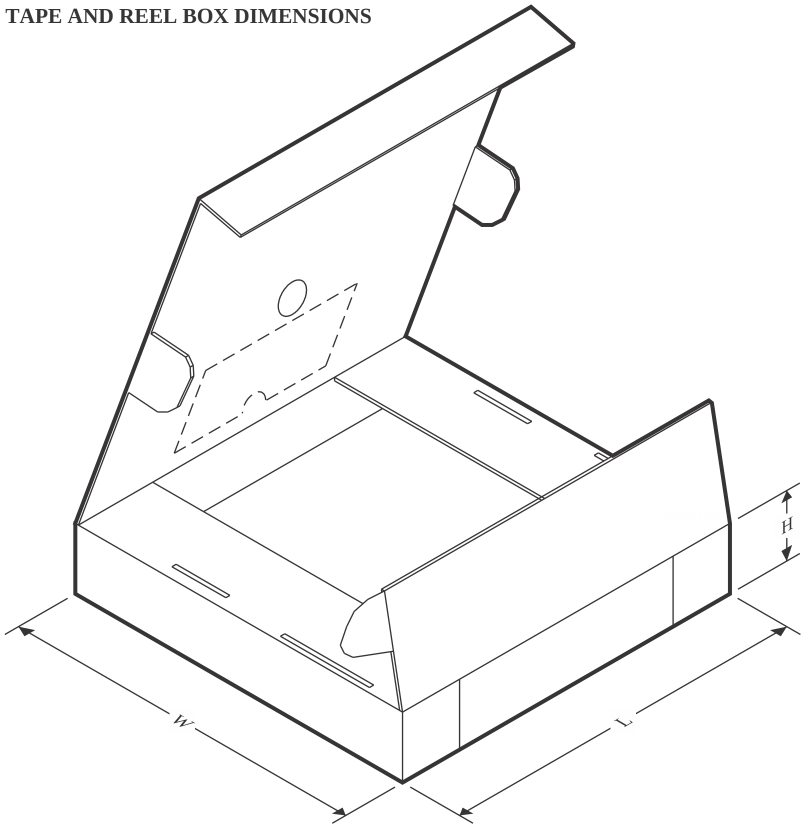
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS4H160AQPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TPS4H160BQPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

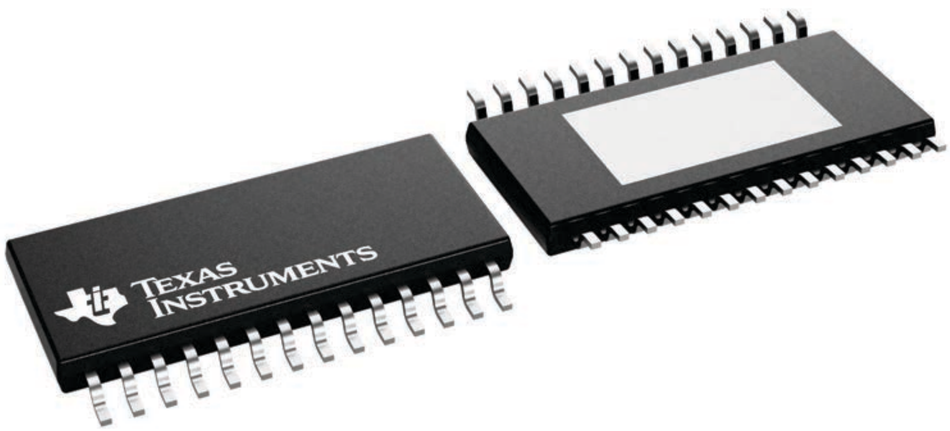
TAPE AND REEL BOX DIMENSIONS

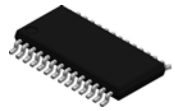


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS4H160AQPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0
TPS4H160BQPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

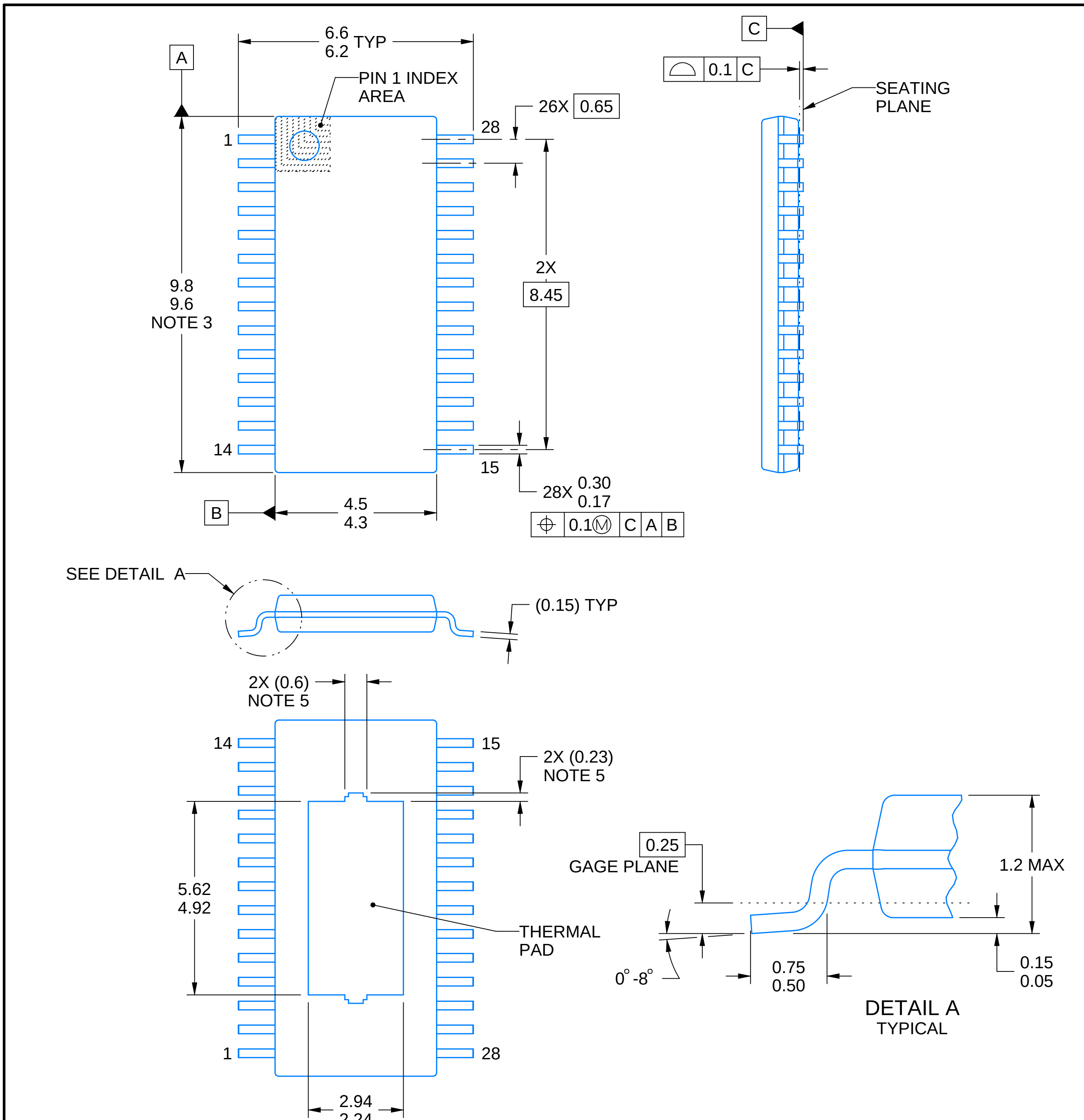




PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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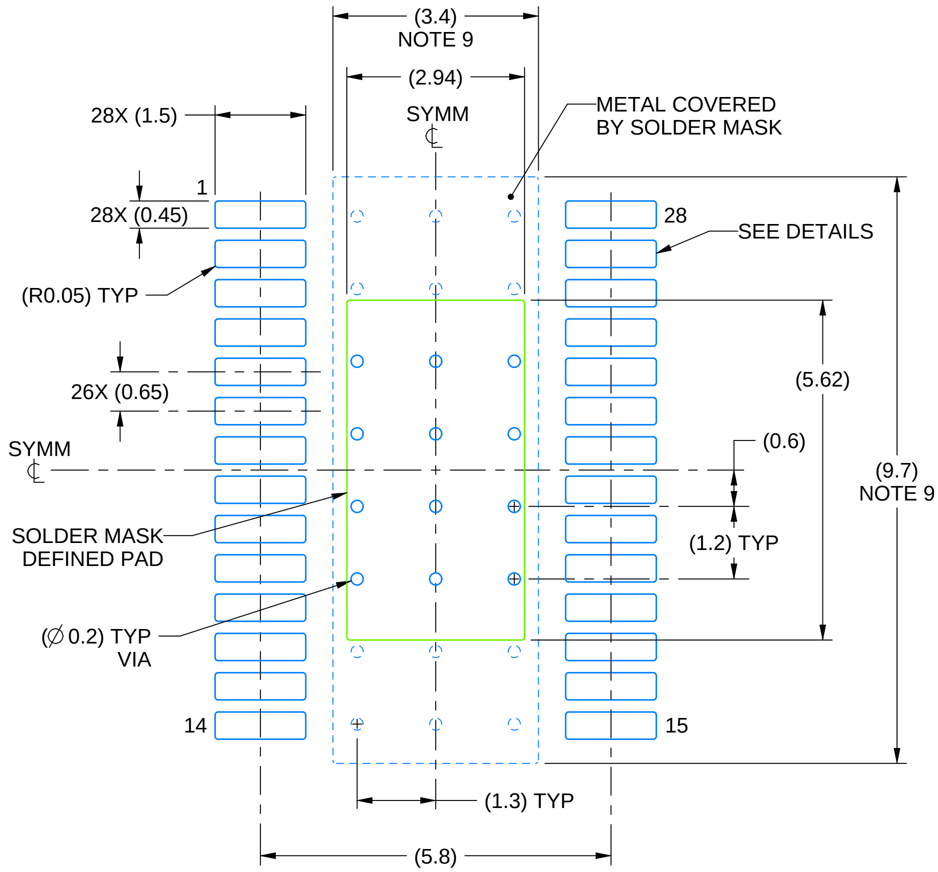
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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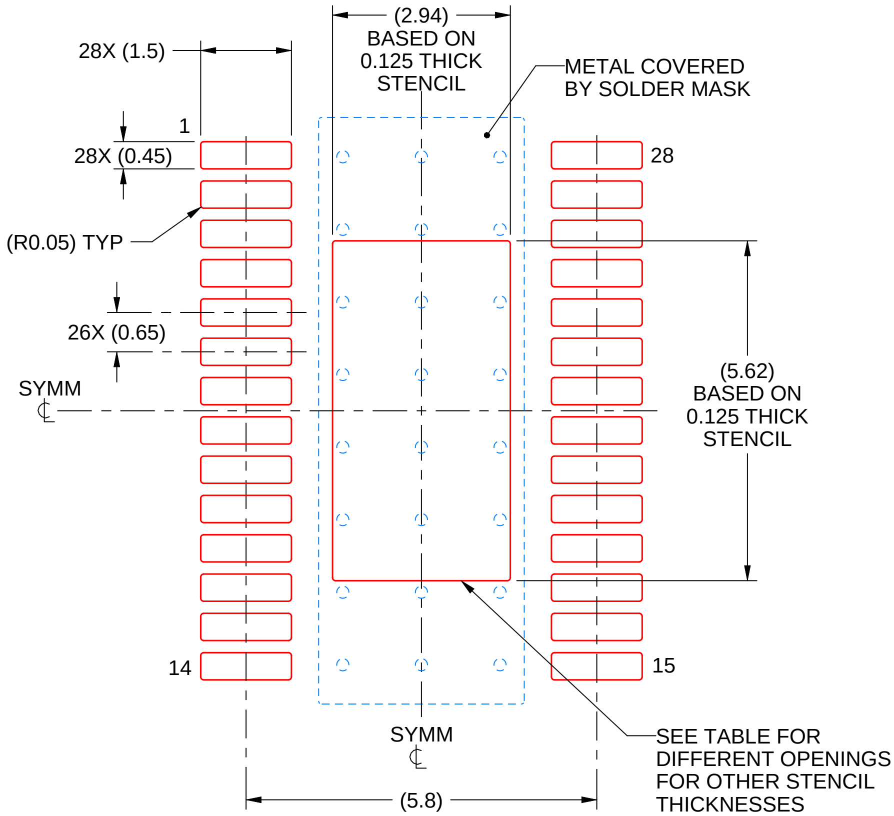
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.29 X 6.28
0.125	2.94 X 5.62 (SHOWN)
0.15	2.68 X 5.13
0.175	2.48 X 4.75

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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