TPS4HC120-Q1 120mΩ, 2A, Quad-Channel Automotive Smart High-Side Switch

1 Features

- Quad-channel 120mΩ automotive smart high-side switch with full diagnostics
  - Open-drain status output
  - Current sense analog output
- Wide operating voltage: 3V to 28V
- Low power mode (LPM) with automatic entry and exit
  - $I_{Q,LPM}$ < 20μA/ch with all 4 channels on and in LPM mode
- Ultra-low sleep current, < 1μA at 25°C
- Selectable current limit, 0.25A to 5A
- Protection
  - Overload and short-circuit protection
  - Thermal shutdown and swing with self recovery
  - Inductive load negative voltage clamp
  - Loss-of-GND, loss-of-battery, and reverse battery protection
- Diagnostics
  - Global fault report for fast interrupt
  - Overcurrent and short-to-ground detection
  - Open-load and short-to-battery detection
- Automotive qualified
  - AEC-Q100 qualified for automotive applications:
    - Temperature: –40°C to 125°C, T_A
  - Electrical transient disturbance immunity certification of ISO7637-2 and ISO16750-2
- Package: 28-pin thermally-enhanced HVSSOP

2 Applications

- ADAS modules
- Automotive display module
- Body control module

3 Description

The TPS4HC120-Q1 is an automotive quad-channel, smart high-side switch, with integrated NMOS power FET and charge pump, designed to meet the requirements of 12V automotive battery systems. The low R_{ON} (120mΩ) minimizes the device power dissipation when driving a wide range of output load current up to 2A when all four channels are enabled or 2.5A when only one channel is enabled.

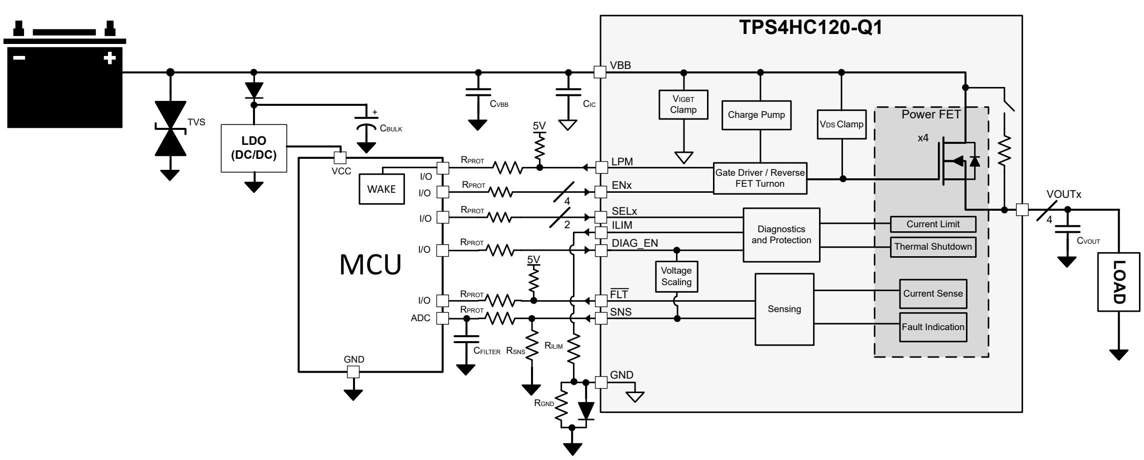
The device integrates protection features such as thermal shutdown, output clamp, and current limit. These features improve system robustness during fault events such as short circuit. The TPS4HC120-Q1 implements a selectable current limiting circuit that improves the reliability of the system by reducing inrush current when driving large capacitive loads and minimizing overload current. The device offers 10 selectable current limit settings (0.25A to 5A) based on the external resistor used on the ILIM pin. The device also provides an accurate load current sense that allows for improved load diagnostics such as overload and open-load detection, which enables better predictive maintenance.

The TPS4HC120-Q1 is available in a 28-pin, 7.1mm × 4.9mm HVSSOP leaded package with 0.5mm pin pitch minimizing the PCB footprint.

Package Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
TPS4HC120-Q1	DGQ (HVSSOP, 28)	7.1mm × 4.9mm

(1) See also Section 4.
(2) For more information, see Section 11.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic

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4 Device Comparison Table

PART NUMBER	BEHAVIOR AFTER THERMAL FAULT
TPS4HC120A-Q1	LATCH off the faulted channel after thermal fault. Toggle EN to re-enable the specific channel.
TPS4HC120B-Q1	Auto-retry after thermal fault.

5 Pin Configuration and Functions

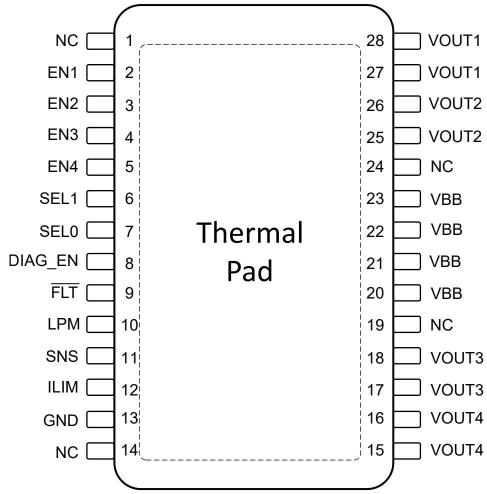


Figure 5-1. DGQ Package, 28-Pin HVVSOP (Top View)

Table 5-1. Pin Functions

See Applications Section for full list of recommended components

PIN		TYPE	DESCRIPTION
NO.	NAME		
1, 14, 19, 24	NC	N/A	No internal connection.
2	EN1	Input	Input control for channel 1 activation, internal pulldown.
3	EN2	Input	Input control for channel 2 activation, internal pulldown.
4	EN3	Input	Input control for channel 3 activation, internal pulldown.
5	EN4	Input	Input control for channel 4 activation, internal pulldown.
6	SEL1	Input	SNS channel-selection high bit; internal pulldown.
7	SEL0	Input	SNS channel-selection low bit; internal pulldown.
8	DIAG_EN	Input	Enable-disable pin for diagnostics, internal pulldown.
9	$\overline{FLT}$	Output	Open drain global fault output. Referred to $\overline{FAULT}$, $\overline{FLT}$, or fault pin. Recommended 5kΩ–10kΩ pullup resistor.
10	LPM	Output	Open drain LPM status pin. Pulled high by external supply if the device is in LPM or SLEEP state. Pulled low internally when device is in ACTIVE mode. Recommended 5kΩ–10kΩ pullup resistor.
11	SNS	Output	SNS current output.
12	ILIM	Output	Adjustable current limit. Connect a resistor to chip GND, SHORT the pin to chip GND, or leave the pin OPEN to set the current limit value.
13	GND	Power	Ground of device. Connect to resistor- diode ground network to have reverse battery protection.
15, 16	VOUT4	Power	Output of channel 4 of the high side switch, connected to load.
17, 18	VOUT3	Power	Output of channel 3 of the high side switch, connected to load.
20, 21, 22, 23	VBB	Power	Power supply
25, 26	VOUT2	Power	Output of channel 2 of the high side switch, connected to load.
27, 28	VOUT1	Power	Output of channel 1 of the high side switch, connected to load.
Thermal Pad	Pad	Power	Thermal Pad, internally shorted to ground.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
V_{BB}	Maximum continuous supply voltage		28	V
V_{LD}	Load dump voltage, ISO16750-2:2010(E)		35	V
V_{REV}	Reverse polarity voltage, maximum duration of 3 minutes and with the application circuit	–18		V
I_{EN1} ,I_{EN2}, I_{EN3}, I_{EN4}	Enable pin current	–0.5	20	mA
V_{EN1} ,V_{EN2}, V_{EN3}, V_{EN4}	Enable pin voltage	–1.5	5.5	V
I_{DIA_EN}	Diagnostic enable pin current	–0.5	20	mA
V_{DIA_EN}	Diagnostic enable pin voltage	-1.5	5.5	V
I_{SNS}	Sense pin current	–10	150	mA
V_{SNS}	Sense pin voltage	–1.5	5.5	V
I_{SELx}	SELx pin current	–0.5	20	mA
V_{SELx}	SELx pin voltage	–1.5	5.5	V
I_{FLT}	$\overline{FLT}$ pin current	-30	2.5	mA
V_{FLT}	$\overline{FLT}$ pin voltage	–0.3	5.5	V
I_{LPM}	LPM pin current	-30	2.5	mA
V_{LPM}	LPM pin voltage	–0.3	5.5	V
I_{ILIM}	ILIM pin current	-0.5	20	mA
V_{ILIM}	ILIM pin voltage	–1.5	5.5	V
I_{GND}	Reverse ground current, V_{BB} < 0V	–50		mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[(1)]	Human-body model (HBM), per AEC Q100-002 [(2)]	All pins except VBB and VOUT	±2000	V
		Human-body model (HBM), per AEC Q100-002 [(2)]	VBB and VOUT	±4000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±750	

(1) All ESD strikes are with reference from the pin mentioned to GND pin.
(2) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) [1]Digital input pins are EN1, EN2, EN3, EN4, SEH, SEL, DIAG_EN

		MIN	MAX	UNIT
V_{VBB_NOM}	Nominal supply voltage [1]	4	18	V
V_{VBB_EXT}	Extended supply voltage[2]	3	28	V
V_{VBB_SC}	Short circuit supply voltage capability		28	V
V_{DIN}	All digital input pin voltage	–1	5.5	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND pin.
(2) The device functions within the extended operating range, however some parametric values do not apply.

6.4 Thermal Information

THERMAL METRIC[1] [2]		TPS4HC120-Q1 DGQ (HVSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

6.5 Electrical Characteristics

V_{BB} = 6V to 18V, T_A = –40°C to +125°C (unless otherwise noted); Typical application is 13.5V, 1A, RILIM = Open (unless otherwise specified). Digital input pins are EN1, EN2, EN3, EN4, SEL0, SEL1, DIAG_EN.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT						
V_{UVLOR}	V_{BB} undervoltage lockout rising	Measured with respect to the GND pin of the device	3.2	3.6	4.0	V
V_{UVLOF}	V_{BB} undervoltage lockout falling	Measured with respect to the GND pin of the device	2.5	2.75	3.0	V
V_{Clamp}	VDS clamp voltage	T_J = 25°C	35		43	V
		T_J = –40°C to +150°C	34		45	
$V_{OUT,Clamp}$	VOUT clamp voltage	T_J = –40°C to +150°C	-31		-23	V
I_Q	Quiescent current all channels enabled	$V_{BB} \le 28V$, $V_{ENx} = V_{DIAG\_EN} = 5V$, $I_{OUTx} = 0A$		3.8	4.5	mA
$I_{Q,DIAG\_DIS}$	Quiescent current channel enabled diagnostic disabled	$V_{BB} \le 28V$ $V_{EN} = 5V$ $V_{DIA\_EN} = 0V$, $I_{OUTx} = 0A$		3.8	4.2	mA
I_{SB}	Current consumption in standby mode	$V_{BB} \le 18V$, $I_{SNS} = 0mA$ $V_{ENx} = 0V$, $V_{DIAG\_EN} = 5V$, $V_{OUT} = 0V$		3.8	4.5	mA
t_{STBY}	Delay time to remain in standby mode before entering sleep mode	$V_{ENx} = V_{DIAG\_EN}$ = 5V to 0V		20		ms

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_A = –40°C to +125°C (unless otherwise noted); Typical application is 13.5V, 1A, RILIM = Open (unless otherwise specified). Digital input pins are EN1, EN2, EN3, EN4, SEL0, SEL1, DIAG_EN.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SLEEP}	Sleep current (total device leakage including MOSFET channels)	V_{BB} ≤ 18V, V_{ENx} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_A = 25°C			0.5	µA
			T_A = 125°C			2	
$I_{OUT(sleep)}$	Output leakage current per channel	V_{BB} ≤ 18V, V_{ENx} = V_{DIAG_EN} = 0V, V_{OUT} = 0V	T_A = 25°C		0.01	0.2	µA
			T_A = 125°C			0.5	
IL_{NOM}	Continuous load current, per channel	All channels enabled	T_A = 85°C		2		A
		One channel enabled			3		
R_{ON} CHARACTERISTICS							
R_{ON}	On-resistance	5V < V_{BB} ≤ 28V, I_{OUT}= 1A	T_J = 25°C		120		mΩ
			T_J = 150°C			250	
		3V ≤ V_{BB} ≤ 5V, I_{OUT} =1A	T_J = 25°C			175	
			T_J = 150°C			280	
ΔR_{ON}	Percentage difference in R_{ON} between channels	5V < V_{BB} ≤ 28V, I_{OUT}= 1A	T_J = –40°C to +150°C		5		%
$R_{ON(REV)}$	On-resistance during reverse polarity	–18V ≤ V_{BB} ≤ –6V	T_J = 25°C		120		mΩ
			T_J = 150°C			250	
V_F	Body diode forward conduction voltage	V_{EN} = 0V I_{OUT} = –0.1A			0.8	1	V
CURRENT SENSE CHARACTERISTICS							
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}	I_{OUT} = 1A			1040		
I_{SNS}	Current sense current and accuracy	V_{EN} = V_{DIAG_EN} = 5V	I_{OUT} = 2A		1.9		mA
				–4		3	%
			I_{OUT} = 1.5A		1.43		mA
				–4		3	%
			I_{OUT} = 750mA		0.72		mA
				–4		4	%
			I_{OUT} = 300mA		0.29		mA
				–5		5	%
			I_{OUT} = 100mA		0.1		mA
				–12		12	%
			I_{OUT} = 75mA		0.072		mA
				–16		16	%
			I_{OUT} = 30mA		0.03		mA
				–35		35	%
			I_{OUT} = 15mA		0.014		mA
				–75		75	%
SNS CHARACTERISTICS							
V_{SNSFH}	V_{SNS} fault high-level	V_{DIAG_EN} = 5V, R_{SNS}= 1kΩ		4.5	5	5.2	V
		V_{DIAG_EN} = 3.3V, R_{SNS}= 1kΩ		3.2	3.6	3.9	
		V_{DIAG_EN} = 1.8V, R_{SNS}= 1kΩ		3.2	3.6	3.9	
I_{SNSFH}	I_{SNS} fault high-level	V_{DIAG_EN} > $V_{IH,DIAG\_EN}$		4.5		6.5	mA
V_{BB_ISNS}	V_{BB} headroom needed for full current sense and fault functionality	V_{DIAG_EN} = 3.3V	Measured with respect to GND pin of device	5			V
		V_{DIAG_EN} = 5V		6.5			

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_A = –40°C to +125°C (unless otherwise noted); Typical application is 13.5V, 1A, RILIM = Open (unless otherwise specified). Digital input pins are EN1, EN2, EN3, EN4, SEL0, SEL1, DIAG_EN.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
CURRENT LIMIT CHARACTERISTICS							
I_{CL}	I_{CL} current limit setting	R_{ILIM} > 60kΩ (ILIM = OPEN)		3.8	4.8	5.6	A
		R_{ILIM} < 1.1kΩ (ILIM = GND)		1.9	2.2	2.4	
		R_{ILIM} = 2.49kΩ			1.9		
		R_{ILIM} = 4.87kΩ			1.7		
		R_{ILIM} = 9.76kΩ			1.5		
		R_{ILIM} = 16.5kΩ		1.1	1.25	1.4	
		R_{ILIM} = 23.2kΩ			1		
		R_{ILIM} = 31.6kΩ			0.75		
		R_{ILIM} = 43.2kΩ[1]			0.5		
		R_{ILIM} = 57.6kΩ[1]		0.19	0.25	0.32	
I_{CL_LINPK}	Linear Mode peak	T_J = –40°C to +150°C, dI/dt < 0.01A/ms	I_{ILIM} = 0.25A to 2.2A			1.6 × I_{CL}	A
I_{CL_ENPS}	Peak current enabling into permanent short	T_J = –40°C to +150°C	Load = 5µH +100mΩ			2.25 × I_{CL}	A
I_{OVCR}	OVCR Peak current when short is applied while switch enabled	T_J = –40°C to +150°C	Load = 5µH +100mΩ			12	A
FAULT CHARACTERISTICS							
R_{OL}	Open-load (OL) detection internal resistor	V_{EN} = 0V, V_{DIAG_EN} = 5V		100	150	175	kΩ
t_{OL}	Open-load (OL) detection deglitch time	V_{EN} = 0V, V_{DIAG_EN} = 5V, When $V_{BB} – V_{OUT} < V_{OL}$, duration longer than t_{OL}. Openload detected.			300	500	µs
V_{OL}	Open-load (OL) detection voltage	V_{EN} = 0V, V_{DIAG_EN} = 5V				1.5	V
t_{OL1}	OL and STB indication-time from EN falling	V_{EN} = 5V to 0V, V_{DIAG_EN} = 5V I_{OUT} = 0mA, $V_{OUT} = V_{BB} – V_{OL}$				500	µs
t_{OL2}	OL and STB indication-time from DIA_EN rising	V_{EN} = 0V, V_{DIAG_EN} = 0V to 5V I_{OUT} = 0mA, $V_{OUT} = V_{BB} – V_{OL}$				600	µs
T_{ABS}	CHx Thermal shutdown threshold			162			°C
T_{HYS}	CHx Thermal shutdown hysteresis					30	°C
T_{REL}	CHx Relative thermal shutdown				80		°C
t_{FAULT_FLT}	Fault indication-time	V_{DIAG_EN} = 5V Time between fault and $\overline{FLT}$ asserting				60	µs
t_{FAULT_SNS}	Fault indication-time	V_{DIAG_EN} = 5V Time between fault and I_{SNS} settling at V_{SNSFH}				60	µs
t_{RETRY}	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown).		1	2	3	ms
LOW POWER MODE							
$I_{LPM,enter}$	Load current level for entry to LPM	t > t_{STBY}		83	110	137	mA
ILPM,exit	Load current level for exit of LPM			130	165	200	mA
$R_{DSON,LPM}$	R_{DSON} in Low Power Mode	50mA I_{LOAD}			130		mΩ

6.5 Electrical Characteristics (continued)

V_{BB} = 6V to 18V, T_A = –40°C to +125°C (unless otherwise noted); Typical application is 13.5V, 1A, RILIM = Open (unless otherwise specified). Digital input pins are EN1, EN2, EN3, EN4, SEL0, SEL1, DIAG_EN.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q,LPM}$	Quiescent current per channel in LPM with all channels enabled	I_{LOAD} = 0mA, T_A = –40°C to +125°C			20	µA
t_{LPM}	LPM transition indication-time	Device in LPM transition out time between current increase and $\overline{LPM}$ asserting			50	µs
t_{WAKE}	Recovery/exit time from LPM	Device in LPM transition out time between wake interrupt (EN, DIAG_EN pin) and LPM asserting			50	µs
$I_{PKLPM,exit}$	Current peak coming out of LPM, current setting ≤ 2.25A	Peak current for immediate shutoff in LPM, T_A = –40°C to +125°C		1.6 × I_{LIM}		
DIGITAL INPUT PIN CHARACTERISTICS						
$V_{IL, DIN}$	Input voltage low-level	No GND network			0.8	V
$V_{IH, DIN}$	Input voltage high-level	No GND network	1.5			V
$V_{IHYS, DIN}$	Input voltage hysteresis		100			mV
R_{PD_DIN}	Internal pulldown resistor for ENx, DIAG_EN		0.7	1	1.3	MΩ
	Internal pulldown resistor for SEL0, SEL1		0.7	1	1.3	
$I_{IH, DIN}$	Input current high-level for SEL0, SEL1	V_{DINx} = 5.5V			10	µA
	Input current high-level for DIAG_EN	V_{DIAG_EN} = 5.5V			30	
$I_{IH, DIN}$	Input current high-level for ENx	V_{ENx} = 5.5V			30	µA
DIGITAL OUTPUT PIN CHARACTERISTICS						
V_{LPM}	LPM low output voltage	$I_{\overline{LPM}}$ = 2mA			0.4	V
V_{FLT}	$\overline{FLT}$ low output voltage	$I_{\overline{FLT}}$ = 2mA			0.4	V

(1) If using GND network, accuracy for this current limit setting is shifted from the table value.

6.6 Timing Characteristics, SNS

V_{BB} = 6V to 18V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIAG_EN 50% of V_{DIAG_EN} to 90% of settled ISNS	V_{EN} = 5V, V_{DIAG_EN} = 0V to 5V R_{SNS} = 1kΩ, I_L = 30mA			60	µs
		V_{ENx}= 5V, V_{DIAG_EN} = 0V to 5V R_{SNS} = 1kΩ, I_L = 1A			30	
$t_{SNSION2}$	Settling time from rising edge of EN and DIAG_EN 50% of V_{DIAG_EN} V_{EN} to 90% of settled ISNS	V_{EN} = V_{DIAG_EN} = 0V to 5V VBB = 13.5V R_{SNS} = 1kΩ, R_{LOAD} = 20Ω			150	µs
$t_{SNSION3}$	Settling time from rising edge of EN with DIAG_EN HI; 50% of V_{DIAG_EN} V_{EN} to 90% of settled ISNS	V_{EN} = 0V to 5V, V_{DIAG_EN} = 5V, VBB = 13.5V, R_{SNS} = 1kΩ, R_{LOAD} = 20Ω			150	µs
$t_{SNSIOFF}$	Settling time from falling edge of DIAG_EN	V_{EN} = 5V, V_{DIAG_EN} = 5V to 0V, VBB = 13.5V, R_{SNS} = 1kΩ, R_L = 20Ω			20	µs

6.6 Timing Characteristics, SNS (continued)

V_{BB} = 6V to 18V, T_A = –40°C to 125°C (unless otherwise noted)

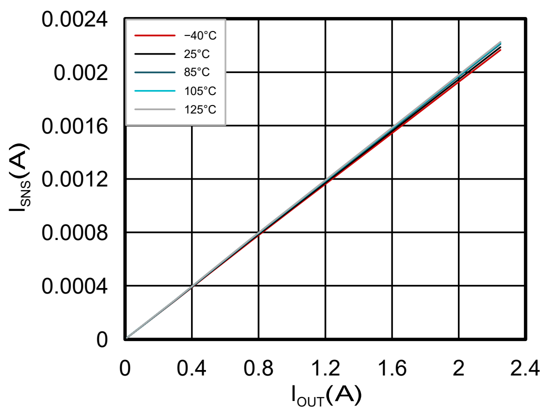
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SETTLEH}$	Settling time from rising edge of load step	V_{EN} = 5V, V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 10mA to 1A			20	µs
$t_{SETTLEL}$	Settling time from falling edge of load step	V_{EN} = 5V, V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_{OUT} = 1A to 10mA			20	µs
t_{SELx}	Multi-sense transition delay from channel to channel	V_{EN} = 5V, V_{DIAG_EN} = 5V R_{SNS} = 1kΩ, I_{OUT1} = 1A to I_{OUT2} = 0.5A			50	µs

6.7 Switching Characteristics

V_{BB} = 13.5V, T_A = –40°C to 125°C (unless otherwise noted)

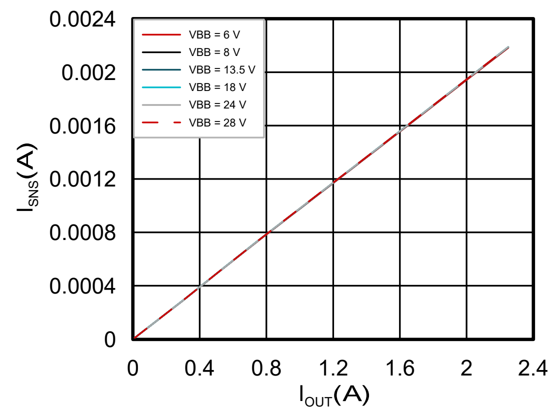
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Channel turn-on delay time (from Active)	V_{BB} = 13.5V, R_L = 1kΩ 50% of EN to 10% of VOUT		30	55	µs
	Channel turn-on delay time (from Sleep or LPM)			40	60	
t_{DF}	Channel turn-off delay time (from Active)	V_{BB} = 13.5V, R_L = 10Ω 50% of EN to 90% of VOUT		30	55	µs
	Channel turn-off delay time (from LPM)			30	85	
SR_R	VOUT rising slew rate	V_{BB} = 13.5V, 20% to 80% of V_{OUT}, R_L = 10Ω	0.1	0.3	0.55	V/µs
SR_F	VOUT falling slew rate	V_{BB} = 13.5V, 80% to 20% of V_{OUT}, R_L = 10Ω	0.1	0.3	0.5	V/µs
t_{ON}	Channel turn-on time (Standby delay to Active)	V_{BB} = 13.5V, R_L = 10Ω 50% of EN to 80% of VOUT	30	50	100	µs
t_{OFF}	Channel turn-off time (Active to Standby delay)	V_{BB} = 13.5V, R_L = 10Ω 50% of EN to 20% of VOUT	30	70	145	µs
t_{ON} - t_{OFF}	Turn-on and off matching	1ms enable pulse V_{BB} = 13.5V, R_L = 10Ω	–40		40	µs
		200-µs enable pulse, V_{BB} = 13.5V, R_L = 10Ω	–40		40	
Δ_{PWM}	PWM accuracy - average load current	200-µs enable pulse (1ms period), V_{BB} = 13.5V, R_L = 10Ω	–25		25	%
		PWM ≤ 500Hz, 50% duty cycle, V_{BB} = 13.5V, R_L = 10Ω	–12		12	
E_{ON}	Switching energy losses during turn-on	V_{BB} = 13.5V, R_L = 10Ω		0.5		mJ
E_{OFF}	Switching energy losses during turn-off	V_{BB} = 13.5V, R_L = 10Ω		0.5		mJ

6.8 Typical Characteristics



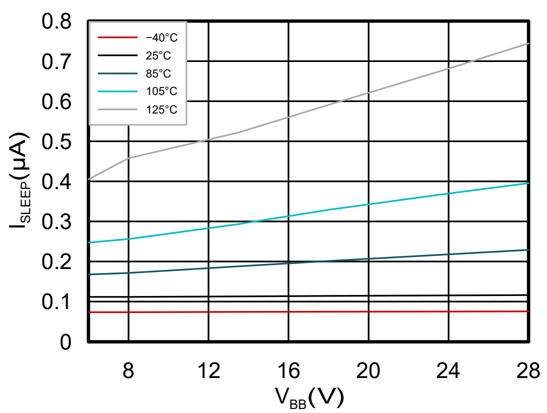
V_{BB} = 13.5V

Figure 6-1. I_{SNS} vs I_{OUT} Over Temperature



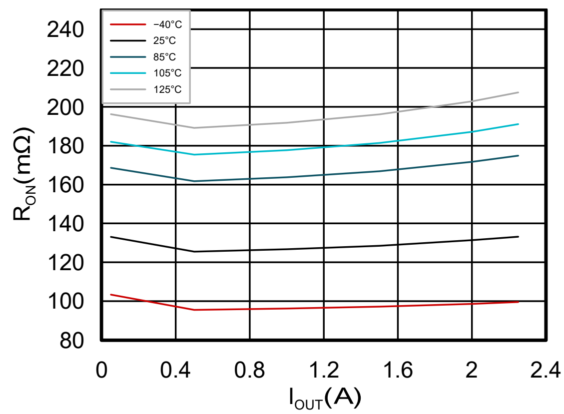
T_A = 25°C

Figure 6-2. I_{SNS} vs I_{OUT} Over V_{BB} Voltage



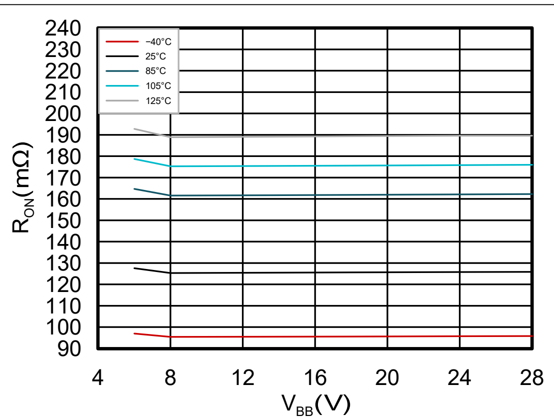
ENx = 0V DIAG_EN = 0V

Figure 6-3. I_{SLEEP} vs V_{BB} Over Temperature



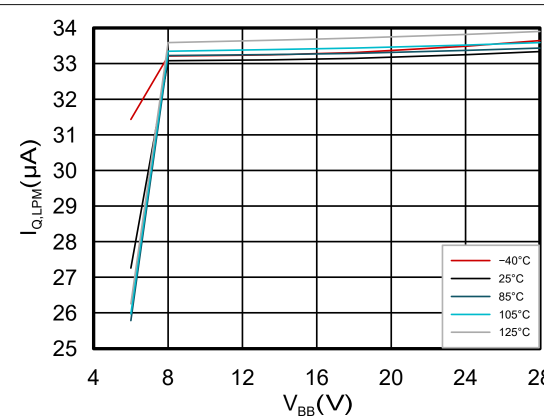
V_{BB} = 13.5V

Figure 6-4. R_{ON} vs I_{OUT} Over Temperature



I_{OUT} = 0.5A

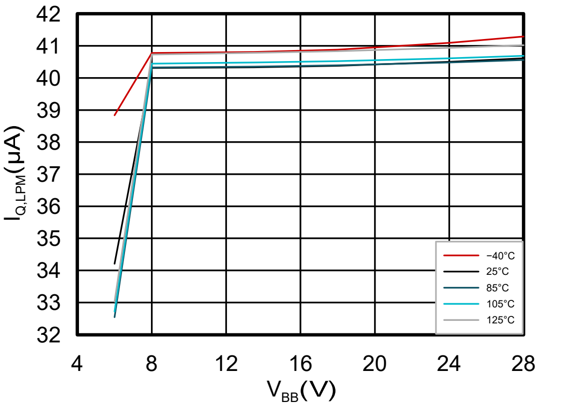
Figure 6-5. R_{ON} vs V_{BB} Over Temperature



EN1 = 5V EN2, 3, 4 = 0V DIAG_EN = 0V

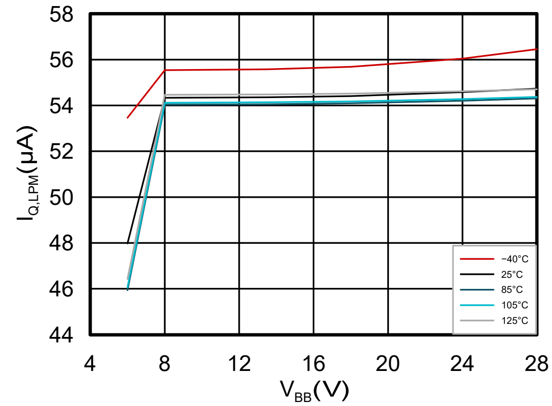
Figure 6-6. $I_{Q,LPM}$ vs V_{BB} Over Temperature When 1 Channel is Enabled

6.8 Typical Characteristics (continued)



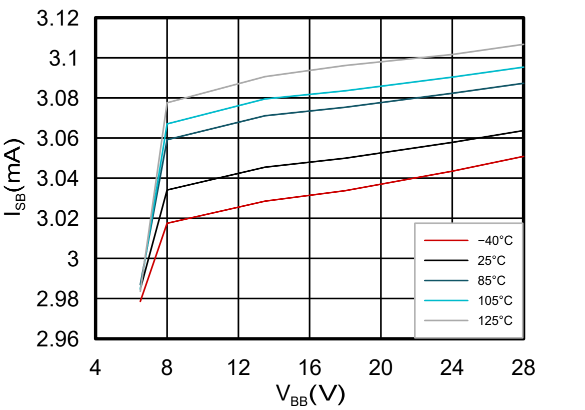
EN1, 2 = 5V EN3, 4 = 0V DIAG_EN = 0V

Figure 6-7. $I_{Q,LPM}$ vs V_{BB} Over Temperature When 2 Channels are Enabled



EN1, 2, 3, 4 = 5V DIAG_EN = 0V

Figure 6-8. $I_{Q,LPM}$ vs V_{BB} Over Temperature When 4 Channels are Enabled



DIAG_EN = 5V EN1 = 5V EN2, 3, 4 = 0V
No load condition

Figure 6-9. I_{SB} vs V_{BB} Over Temperature

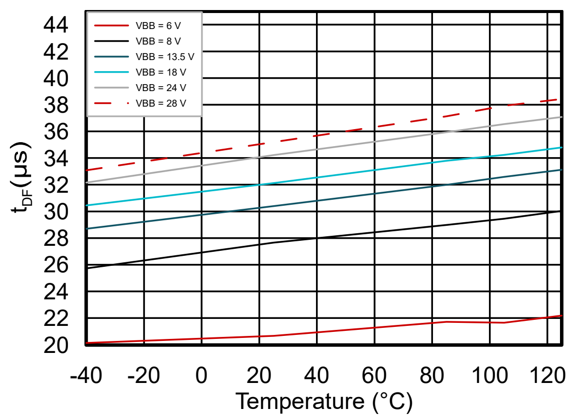


Figure 6-10. t_{DF} vs Temperature Over V_{BB} Voltage

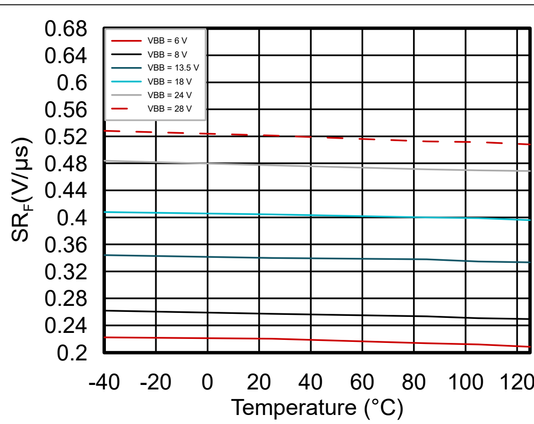


Figure 6-11. SR_F vs Temperature Over V_{BB} Voltage

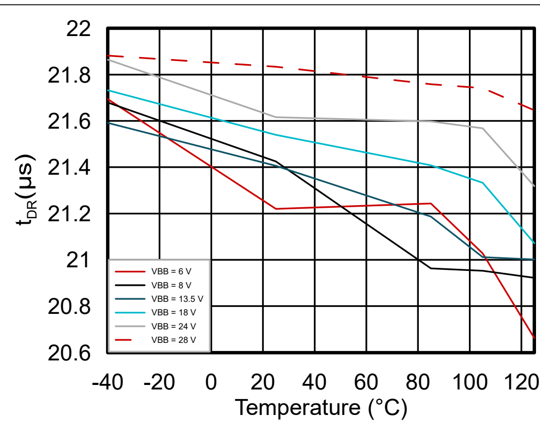


Figure 6-12. t_{DR} vs Temperature Over V_{BB} Voltage

6.8 Typical Characteristics (continued)

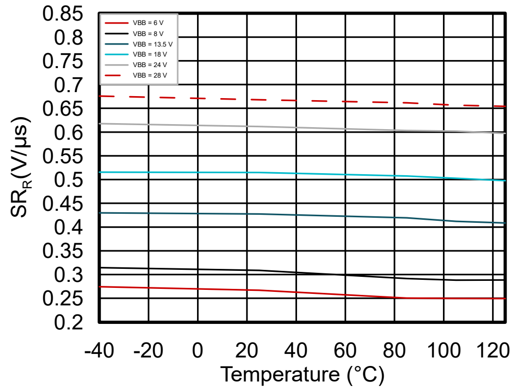
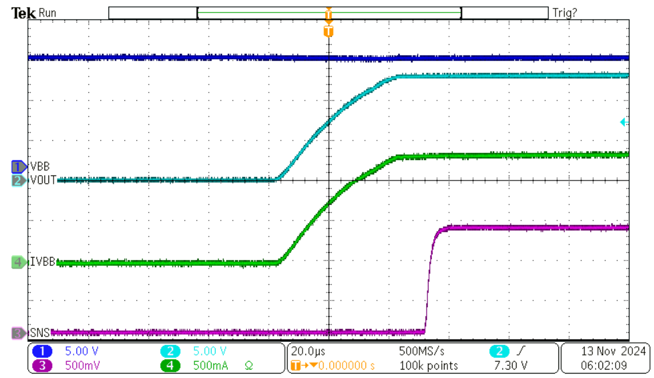
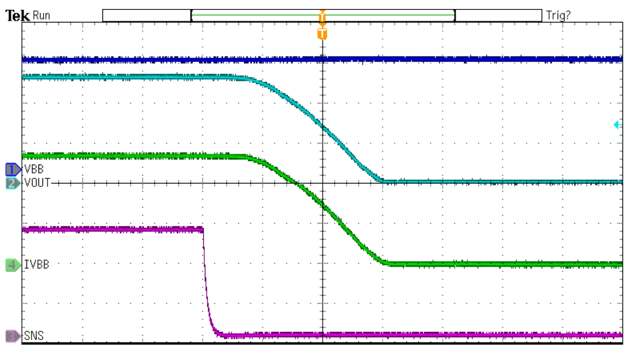


Figure 6-13. SR_R vs Temperature Over V_{BB} Voltage



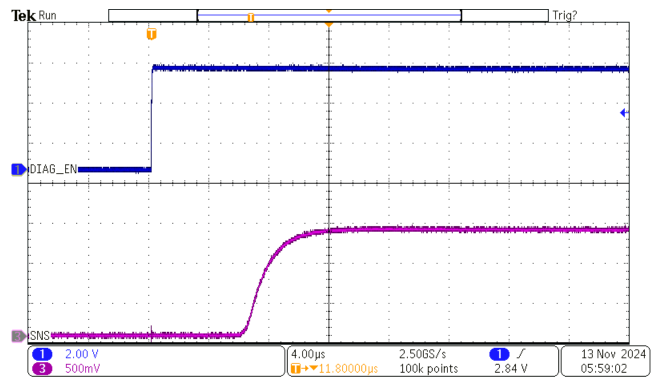
V_{BB} = 13.5V R_{SNS} = 1kΩ ILIM = OPEN
R_{OUT} = 10Ω T_A = 25°C

Figure 6-14. Switch Turn-On



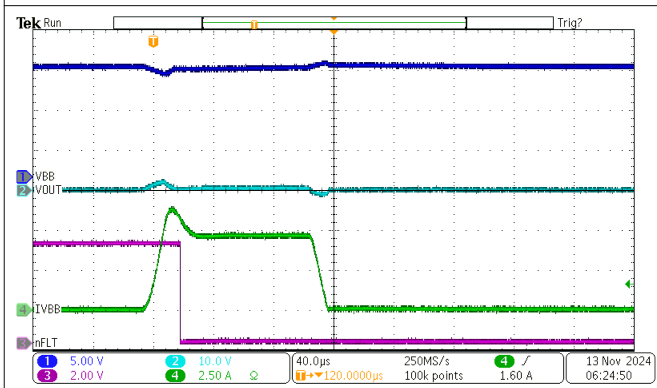
V_{BB} = 13.5V R_{SNS} = 1kΩ ILIM = OPEN
R_{OUT} = 10Ω T_A = 25°C

Figure 6-15. Switch Turn-Off



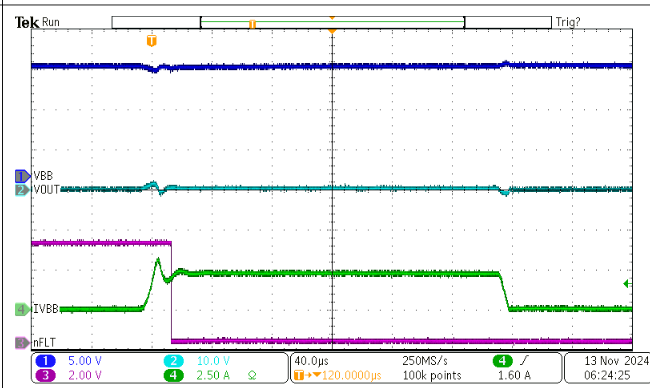
V_{BB} = 13.5V R_{SNS} = 1kΩ ILIM = OPEN
R_{OUT} = 10Ω T_A = 25°C

Figure 6-16. SNS Pin Voltage With DIAG_EN Turning ON



V_{BB} = 13.5V R_{SNS} = 1kΩ ILIM = OPEN
Z_{OUT} = 100mΩ + 5μH T_{AMB} = 25°C

Figure 6-17. Permanent Short Behavior With ILIM Open



V_{BB} = 13.5V R_{SNS} = 1kΩ ILIM = Short-to-GND
Z_{OUT} = 100mΩ + 5μH T_A = 25°C

Figure 6-18. Permanent Short Behavior With ILIM Short-to-GND

7 Detailed Description

7.1 Overview

The TPS4HC120-Q1 device is a smart high-side switch, with internal charge pump and quad-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of the whole system.

The device has logic pins to enable each of the four channels and a separate pin to enable the diagnostic output with two pins to select the channel to be output on the analog current SNS pin. The device also implements a global FLT pin for use as an interrupt to the MCU.

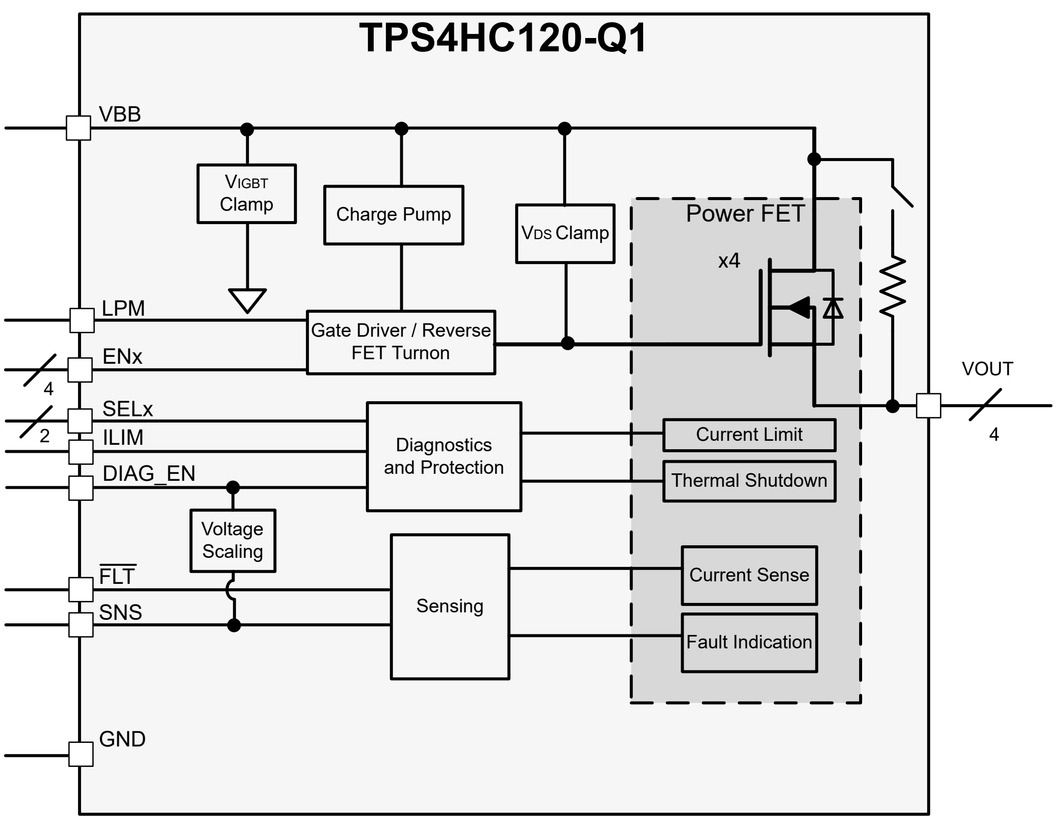
The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device also helps save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source for protection. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

When the current consumptions on all channels are small, along with other requirements described in Section 7.3.2.1, the device automatically enters low power mode. This mode has ultra-low quiescent current consumption, and is applicable for loads that are active when the vehicle is off to preserve the battery. There is a dedicated LPM pin that indicates the mode of the device, and is useful as an interrupt signal to wake up the MCU.

The TPS4HC120-Q1 device is able to drive a wide variety of resistive, inductive, and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on each pin are as shown by the arrows in Figure 7-1. All voltages are measured relative to the ground plane.

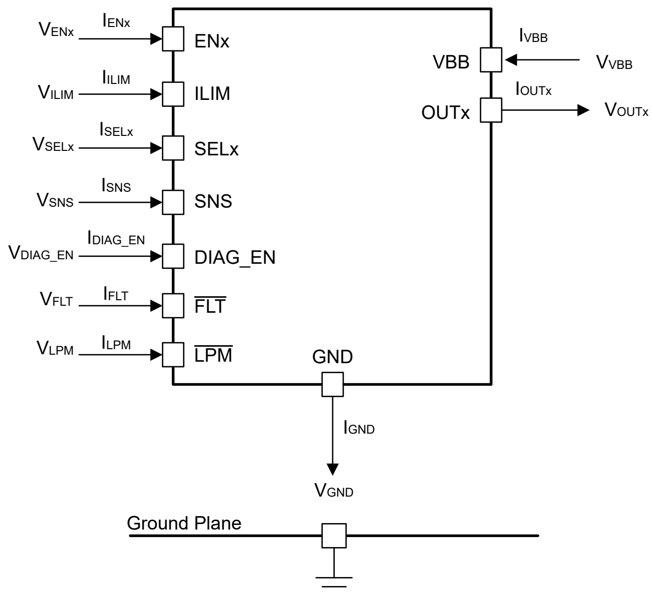


Figure 7-1. Voltage and Current Conventions

7.3.2 Low Power Mode

Low power mode (LPM) is designed to be able to still provide small amounts of current to loads without consuming much quiescent current. This type of feature is useful in power-at-all-time loads or to just generally reduce the amount of power dissipation from the supply. The quiescent current draw during this mode is defined in Section 6.5 under $I_{Q,LPM}$. The TPS4HC120-Q1 can automatically enter and exit this mode by detecting that the load current is below $I_{LPM,enter}$ on all active channels, and then exits this mode when load current increases above $I_{LPM,exit}$. This section describes the entry, exit and protections mechanisms in this mode.

7.3.2.1 Entry into LPM

When the load current going through the channel is below the $I_{LPM,enter}$ threshold on all active channels and diagnostics are turned off (DIAG_EN is low) for longer than t_{STBY}, the device automatically enters into LPM. This means that the digital core is turned off and the charge pump strength is reduced to reduce the quiescent current to $I_{Q,LPM}$.

All the requirements below need to be met for the device to enter the LPM automatically:

- T_J < 125°C
- V_{BB} ≥ 6V
- DIAG_EN is LOW
- At least one channel is ON
- All the ON channels have load currents < $I_{LPM,enter}$ per channel
- No EN pin toggling
- All the above conditions are true for time longer than t_{STBY}

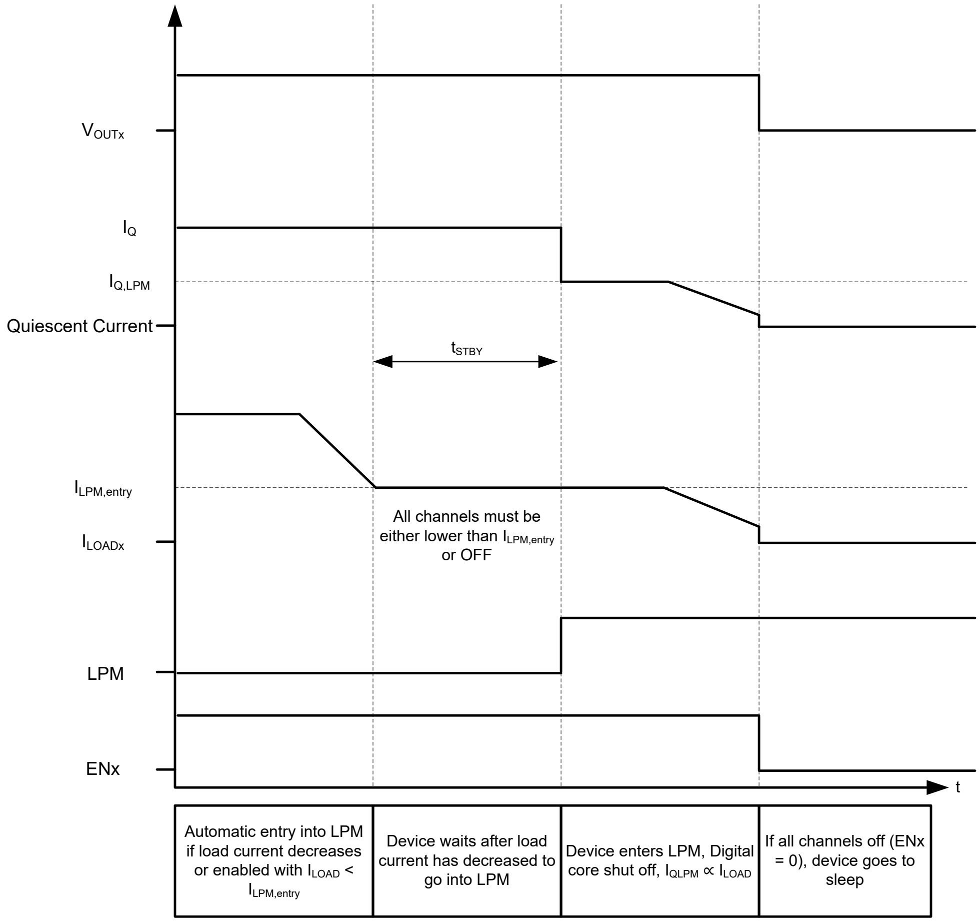


Figure 7-2. Entering LPM

7.3.2.2 During LPM

The quiescent current of the device during LPM, $I_{Q,LPM}$, is a function of how many channels are active. $I_{Q,LPM}$ is proportional to the load current, meaning that the lower the load current is during this time, then the lower the quiescent current is. Additionally, because the digital core is disabled, diagnostics such as current sensing or open load detection are not available during this mode. If diagnostics are desired, enable the DIAG_EN pin to exit LPM and return the device back to normal operation. After DIAG_EN is disabled, the device goes back into LPM after t_{STBY}. Similarly, the current limit mechanism is not active in the same manner. By definition, the minimum current limit is higher than the entry point of LPM. However, the short-circuit protection is still in place to protect the device.

The following summary lists the behavior of the device during LPM:

- I_q reduces to $I_{Q,LPM}$ per channel
- $R_{DS,ON}$ per channel increases to $R_{DSON,LPM}$
- No clamped current limit for overload conditions as the device exits the LPM first
- Short-circuit protection is in place to shut off the device if load current increases to $I_{PKLPM,exit}$ during LPM
- No thermal shutdown protection

7.3.2.3 Exiting LPM

The device exits LPM if any one of four conditions is met:

- Load current increases slowly: If the load current increases beyond $I_{LPM,exit}$ slowly, the device wakes up and pulls the LPM pin low to signal the device is no longer in low power mode. The output voltage droop is minimal.

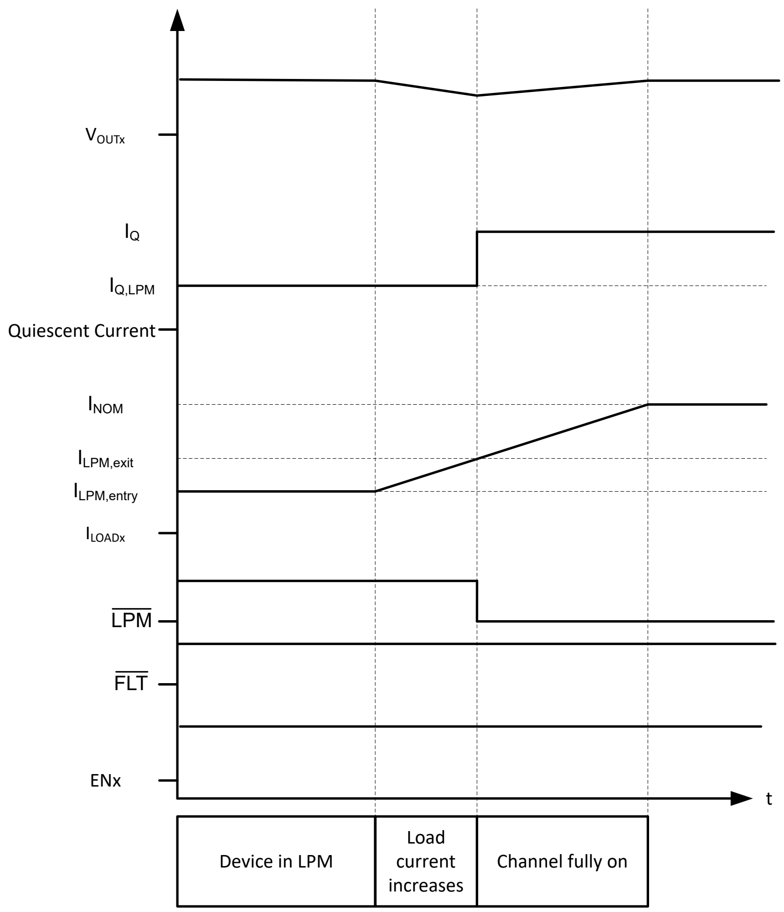


Figure 7-3. Exiting LPM With Load Current Slow Increase

- Load current increases rapidly (short-circuit): If the load current increases rapidly beyond $I_{LPM,exit}$, the device shuts down for protection and comes back on within the t_{WAKE} time in normal operation with full functionality. As the device comes back on, the LPM pin is pulled LOW to represent that the device has come out of LPM. The FLT pin also pulls low if the fault is still present.

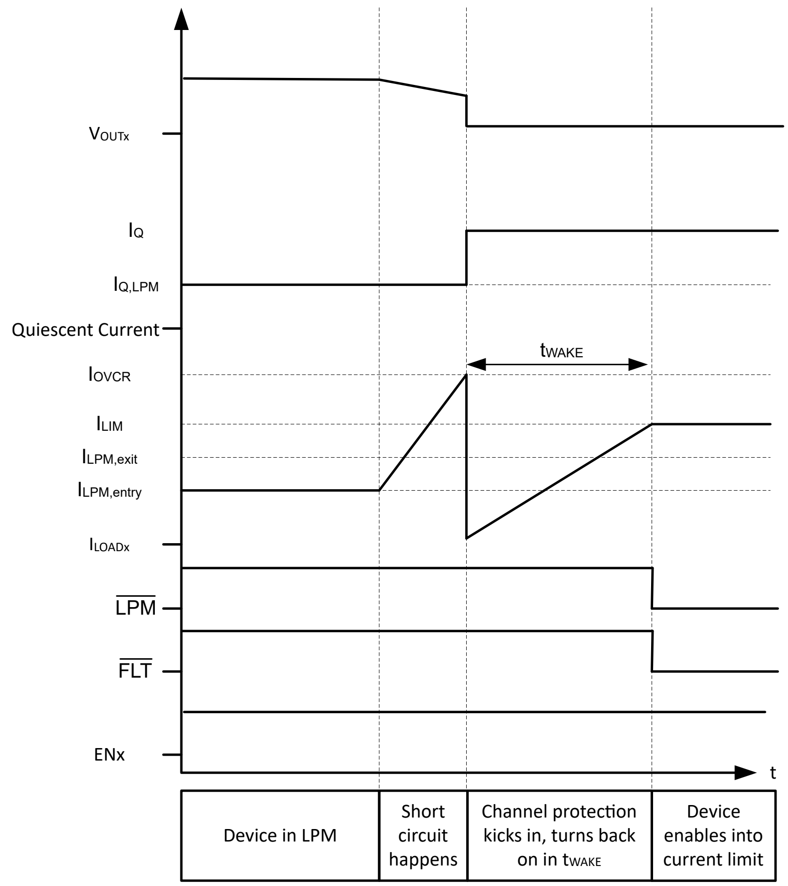


Figure 7-4. Exiting LPM With Rapid Load Current Increase (Short-Circuit)

- Any ENx is toggled (from ON to OFF or OFF to ON): If any channel is turned ON or turned OFF during LPM, the device wakes up and performs the desired action. After the device wakes up, if the LPM entry conditions are still met, the device enters LPM again after t_{STBY}.
- DIAG_EN is turned ON: if DIAG_EN goes high, the device goes into the DIAGNOSTIC mode, which fully turns on the device so that all of the functionality works as intended in the DIAGNOSTIC state. If DIAG_EN goes back low, with all LPM entry conditions are met, the device goes back into LPM after t_{STBY}.

Any time the device comes out of LPM to ACTIVE state, the LPM pin pulls LOW. If the system must wake up when the device comes out of LPM, then the LPM pin is able to be used to send a wake up signal to the MCU. Otherwise, ignore the LPM pin.

7.3.3 Accurate Current Sense

The high-accuracy current-sense function is internally implemented, which allows a better real-time monitoring effect and more-accurate diagnostics without further calibration. A current mirror is used to source 1 / K_{SNS} of the load current, flowing out to the external resistor between the SNS pin and GND, and reflected as voltage on the SNS pin.

K_{SNS} is the ratio of the output current and the sense current. The accuracy values of K_{SNS} quoted in the *Electrical Characteristics* take into consideration temperature and supply voltage. Each device is internally calibrated while in production, so post-calibration by users is not required in most cases.

The maximum voltage out on the SNS pin is clamped to V_{SNSFH}, which is the fault voltage level. To ensure that this voltage is not higher than the system can tolerate, limit the max voltage at the DIAG_EN pin to the voltage at the SNS pin. If DIAG_EN is between V_{IH} and 3.3V, the maximum output on the SNS pin is approximately 3.3V. However, if the voltage at DIAG_EN is above 3.3V, then the fault SNS voltage, V_{SNSFH}, tracks that voltage up to 5V. Tracking is done because the GPIO voltage output that is powering the diagnostics through DIAG_EN is close to the maximum acceptable ADC voltage within the same microcontroller. Therefore, choose the sense resistor value, R_{SNS}, to maximize the range of currents needed to be measured by the system. Choose the R_{SNS} value based on application need. The maximum usable R_{SNS} value is bounded by the ADC minimum acceptable voltage, $V_{ADC,min}$, for the smallest load current needed to be measured by the system, $I_{LOAD,min}$. Choose the minimum acceptable R_{SNS} value so that the V_{SNS} voltage is less than the V_{SNSFH} value, allowing for the system to correctly determine faults. This difference between the maximum readable current through the SNS pin, $I_{LOAD,max} \times R_{SNS}$, and the V_{SNSFH} is called the headroom voltage, V_{HR}. The headroom voltage is determined by the system but is important so that there is a difference between the maximum readable current and a fault condition. Therefore, the minimum R_{SNS} value has to be the V_{SNSFH} minus the V_{HR} times the sense current ratio, K_{SNS} divided by the maximum load current the system must measure, $I_{LOAD,max}$. Use the following equation to set the boundary equation.

$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \le R_{SNS} \le (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (1)$$

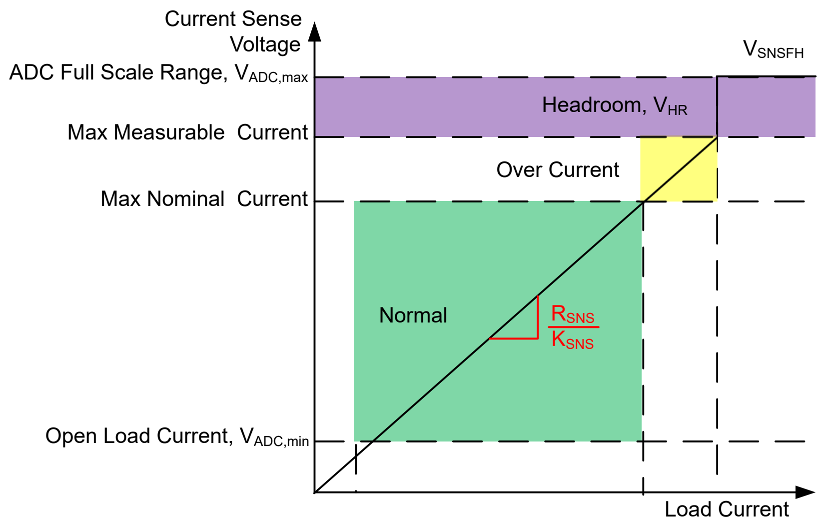


Figure 7-5. Voltage Indication on the Current-Sense Pin

The maximum current the system wants to read, $I_{LOAD,max}$, must be less than the current-limit threshold because after the current-limit threshold is tripped, the V_{SNS} value goes to V_{SNSFH}.

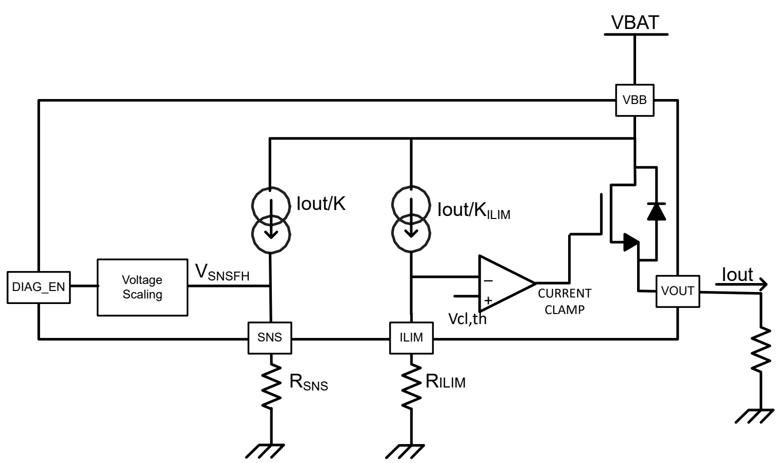


Figure 7-6. Current-Sense and Current-Limit Block Diagram

Because this scheme adapts based on the voltage coming in from the MCU, there is no need to have a Zener diode on the SNS pin to protect from high voltages.

7.3.4 Adjustable Current Limit

A high-accuracy adjustable current limit allows higher reliability, which protects the power supply and wires during short circuit or power up by being programed to an acceptable level. Also, current limiting help save system costs by reducing PCB traces, connector size, capacity of the preceding power stage and possibly reducing wire gauge.

Current limit offers protection from over-stressing to the load and integrated power FET. the current limit regulates the output current to the set value, asserts the $\overline{\text{FLT}}$ pin, and pulls up the SNS pin to V_{SNSFH} if the device is set up to output that channel on the SNS pin.

The device can be programmed to different current limit values through an external resistor on the ILIM pin. There are 10 current limit settings which are set based on resistors values in Table 7-1. Tolerance resistors ≤ 1% are recommended for the R_{ILIM} resistor.

Table 7-1. Current Limit Setting Through External Resistor

ALLOWED RESISTOR VALUE(1)	ILIM THRESHOLD
57.6kΩ	250mA
43.2kΩ	500mA
31.6kΩ	750mA
23.2kΩ	1A
16.5kΩ	1.25A
9.76kΩ	1.5A
4.87kΩ	1.75A
2.49kΩ	2A
Short to GND (< 1.1kΩ)	2.25A
Open (> 60kΩ)	5A

(1) Interpret any resistor settings that are not listed in this table as one of the adjacent levels, which are not recommended configurations.

To set a different inrush current limit and steady state current limit, the current limit resistor is able to change dynamically when the device is on. Adopt the MOSFET-based control scheme to change the current limit on the fly. However, carefully consider the components and the layout at ILIM pin to minimize the capacitance at the pin. Any capacitance ≥ 100pF at ILIM pin possibly affects the current limit functionality. Select a MOSFET with low input capacitance for the dynamic current limit.

A current limit event occurs when I_{OUTx} reaches the regulation threshold level, I_{CL}. When I_{OUT} reaches the current limit threshold, I_{CL}, the device is able to remain enabled and limit I_{OUTx} to I_{CL}. When the device remains enabled (and limits I_{OUT}), thermal shutdown potentially triggers due to the high amount of power dissipation in the FET. Figure 7-7 shows the regulation loop response when the device is enabled into a short circuit. The figure shows the scenario with the auto-retry version listed in Section 4. The LATCH version latches off after the first thermal shutdown. Be aware that the current peak is able to be at a higher value (I_{CL_ENPS}) than the regulation threshold (I_{CL}).

When an overcurrent event occurs, the current limit must respond quickly to limit the peak current seen on short circuits (both hot and enabling into a short). Limit the peak so that the supply does not droop for a given amount of supply capacitance. This peak limiting is especially important in applications where the device is powered from a DC/DC instead of car battery.

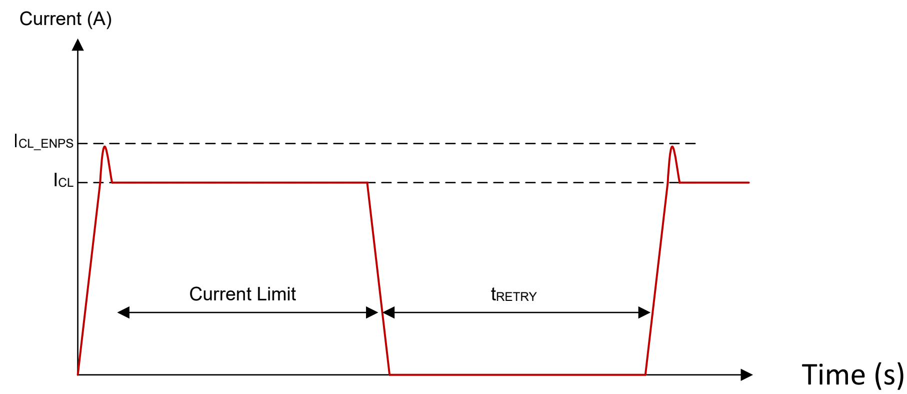


Figure 7-7. Enable Into Short Current Limit (Auto-Retry Version)

However, a higher output current (I_{CL_LINPK}) than the current limit regulation loop threshold (I_{CL}) is potentially available from the switch during an overload condition before the current limitation is applied.

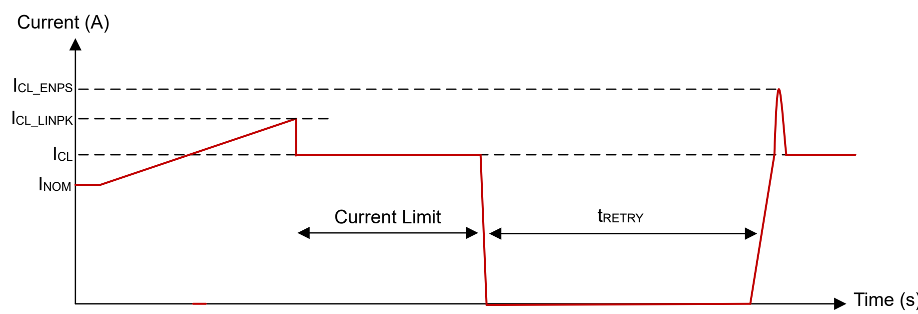


Figure 7-8. Linear Peak From Soft Short (Auto-Retry Version)

The device applies a strong pulldown to limit the current during the short circuit event while the switch is enabled. The current then drops down to zero before the current limit regulation loop engages the switch turn-on, and the behavior is similar to the enable into a short circuit case.

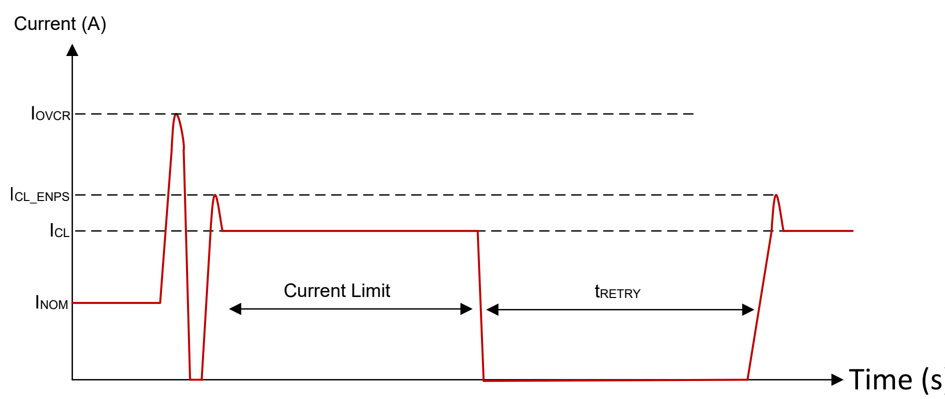


Figure 7-9. Hot Short Event (Auto-Retry Version)

7.3.5 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage can cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \tag{2}$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \tag{3}$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation.

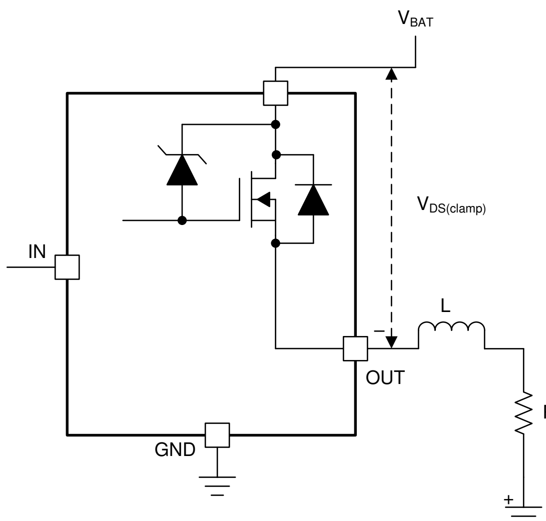


Figure 7-10. Drain-to-Source Clamping Structure

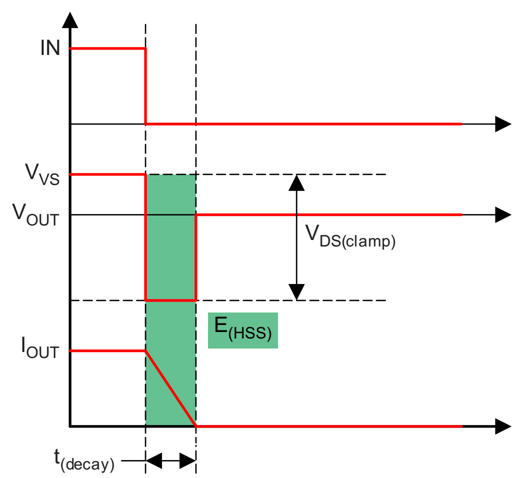


Figure 7-11. Inductive Load Switching-Off Diagram

From the high-side switch perspective, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)\,dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \tag{4}$$

When R approximately equals 0, $E_{(HSD)}$ is given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I^2_{OUT(max)} \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \tag{5}$$

The recommendation for PWM-controlled inductive loads is to add the external freewheeling circuitry shown in Figure 7-12 to protect the device from repetitive power stressing. The TVS is used to achieve the fast decay. See also Figure 7-12.

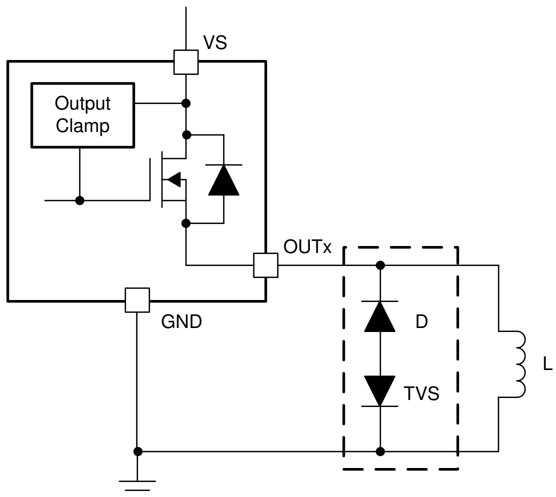


Figure 7-12. Protection With External Circuitry

7.3.6 Fault Detection and Reporting

7.3.6.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and ENx low.

7.3.6.2 Multiplexing of Current Sense

SELx pins are used to multiplex the shared current-sense function among the four channels within the same device. Pulling each pin high or low sets the corresponding channel to be output on the SNS pin if DIAG_EN is high. $\overline{\text{FLT}}$ still represents a global interrupt that goes low if a fault occurs on any channel.

If current sense information is multiplexed across different devices, do not directly tie the SNS pins together across multiple devices. When the DIAG_EN is LOW, there is an internal clamp at SNS pin that clamps the voltage to approximately 2V. One device SNS pin is able to affect the SNS readback of other devices if tied directly.

To use the SNS pin across multiple devices, connect individual SNS pin to different analog input pins of MCU; see Figure 7-13. Alternatively, use an external analog MUX to connect to a single MCU pin; see Figure 7-14.

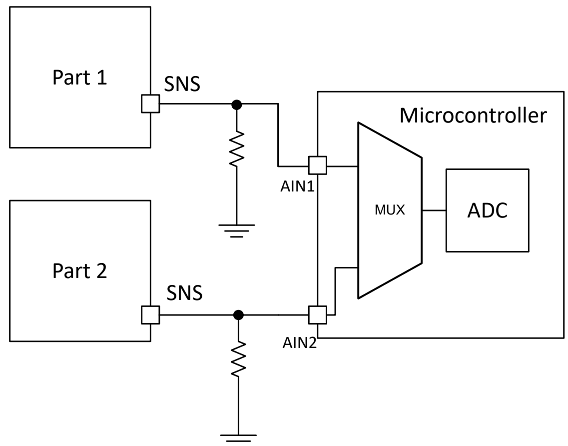


Figure 7-13. SNS Sharing Across Multiple Devices Method 1

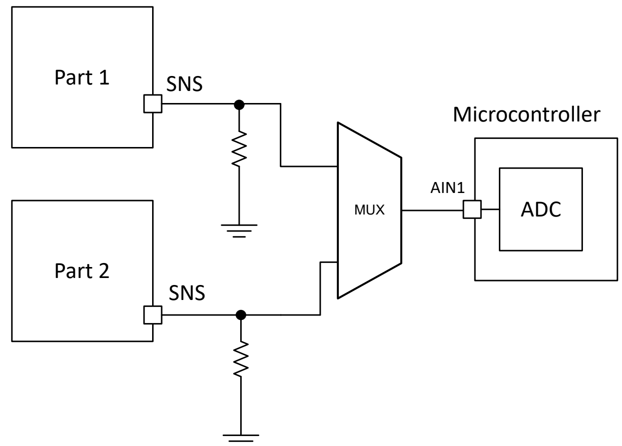


Figure 7-14. SNS Sharing Across Multiple Devices Method 2

Table 7-2. Diagnosis Configuration Table

DIAG_EN	ENx	SEL0	SEL1	SNS ACTIVATED CHANNEL	SNS	$\overline{FLT}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	—	0V. Clamp to 2V internally if external voltage is applied to the pin.	See Table 7-3	SNS disabled, $\overline{FLT}$ reporting, full protection
	L					High-Z	Diagnostics disabled, no protection
H	—	0	0	Channel 1	See Table 7-3	See Table 7-3	See Table 7-3
		0	1	Channel 2			
		1	0	Channel 3			
		1	1	Channel 4			

7.3.6.3 $\overline{\text{FAULT}}$ Reporting

The global $\overline{\text{FLT}}$ pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the $\overline{\text{FLT}}$ pin is pulled down to GND. A 3.3V or 5V external pullup is required to match the supply level of the microcontroller. The $\overline{\text{FLT}}$ pin reports faults on any channel as long as the device is not in the SLEEP or LOW POWER MODE.

After the $\overline{\text{FAULT}}$ report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The SNS pin also works as a fault report with an internal pullup voltage, V_{SNSFH} if DIAG_EN is high.

7.3.6.4 Fault Table

Table 7-3. Fault Table

CONDITIONS	ENx	OUTx	SNS (If DIAG_EN is high)	$\overline{\text{FLT}}$ (with external pullup)	BEHAVIOR	FAULT RECOVERY
Normal	L	L	0	H	Normal	—
	H	$V_{BB} - I_{LOAD} \times R_{ON}$	I_{LOAD} / K_{SNS}	H	Normal	—
Overcurrent	H	$V_{BB} - I_{LIM} \times R_{ON}$	V_{SNSFH}	L	Holds the current at the current limit until thermal shutdown or when the overcurrent event is removed.	Auto
Open load, short to battery, reverse polarity	L	H	V_{SNSFH}	L	Internal pull-up resistor is active. Fault is asserted when $V_{VS} - V_{OUTx} < V_{(ol,off)}$	Auto
	H	H	$I_{LOAD} / K_{SNS} \approx 0$	H	Normal behavior. User can make judgment based on SNS pin output.	—
Hot short	H	L	V_{SNSFH}	L	Device immediately shuts down, and re-enables into current limit.	Auto-retry into current limit until thermal shutdown. Auto-retry version repeats until the fault goes away. Latch version must toggle EN after first thermal shutdown.
Enable into permanent short	L → H	L	V_{SNSFH}	L	Device enables into current limit until thermal shutdown.	Enable into current limit until thermal shutdown. Auto-retry version repeats until the fault goes away. Latch version requires EN to be toggled after the first thermal shutdown.
Absolute thermal shutdown, Relative thermal shutdown	H	L	V_{SNSFH}	L	Shuts down when devices hits relative or absolute thermal shutdown.	For auto-retry version, output auto-retry after t_{RETRY}. Fault recovers when $T_J < T_{HYS}$ or when ENx toggles. Latch version recovers only when EN toggles.
Reverse polarity	X	X	X		X	Channel turns on to lower power dissipation. Limit current into ground pin by external ground network.

7.3.7 Full Diagnostics

7.3.7.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device clamps the current to I_{CL} until thermal shutdown. TPS4HC120A automatically recovers when the fault condition is removed.

In a hot short condition, when the short-circuit is applied when the EN is HIGH, the device shuts down immediately and auto-retries the same as enable into permanent short condition, as shown in Figure 7-9.

7.3.7.2 Open-Load Detection

7.3.7.2.1 Channel On

When a channel is ON, benefiting from the high-accuracy current sense in the small current range, an open-load event can be detected as an ultra low V_{SNS} and handled by the microcontroller. Note that the detection is not reported on the $\overline{\text{FAULT}}$ pin or the fault registers. The microcontroller must multiplex the SEL and SEH pins to output the correct channel out on the SNS pin.

7.3.7.2.2 Channel Off

In the OFF state, when DIAG_EN is high, there is an internal pull-up resistor R_{OL} that pulls up a channel to V_{BB}. The specific channel that gets pulled up is based on the selection of SEL0 and SEL1, and the other channels do not have the pull-up resistor engaged.

If there is load present at the selected channel, then the output voltage is pulled to around 0V, as the load is much stronger than the R_{OL}. In the case of an open load, the output voltage is pulled close to the supply voltage by the R_{OL}. If V_{BB} - V_{OUT} < $V_{OL,off}$ for the selected channel, the $\overline{\text{FLT}}$ pin goes low to indicate the fault to the MCU, and the SNS pin is pulled up to I_{SNSFH}.

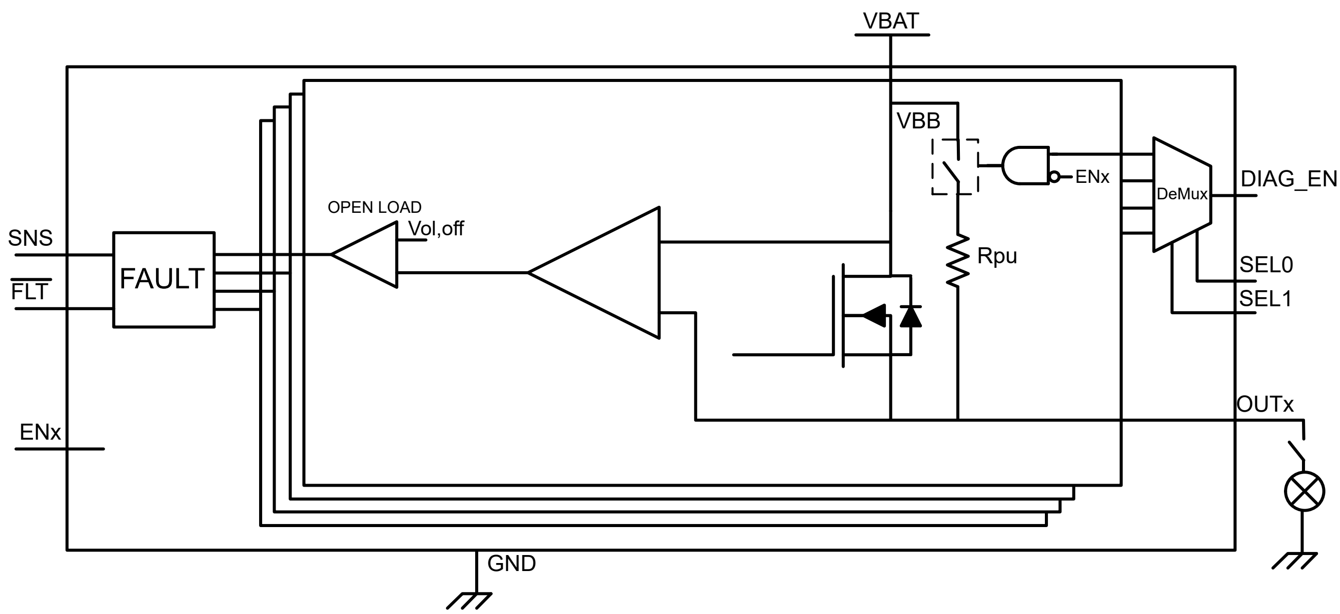


Figure 7-15. Open-Load Detection in Off-State

7.3.7.3 Short-to-Battery Detection

Short-to-battery has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Table 7-3 for more details.

7.3.7.4 Reverse-Polarity and Battery Protection

Reverse-polarity, commonly referred to as reverse battery, occurs when the ground of the device goes to the battery potential, $V_{GND} = V_{BAT}$, and the supply pin goes to ground, $V_{BB} = 0V$. In this case, if the EN2 pin has a path to the *ground* plane, then the FET turns on to lower the power dissipation through the main channel and prevent current flow through the body diode. The resistor-diode ground network (if there is no central blocking diode on the supply) is required for device protection during a reverse-battery event.

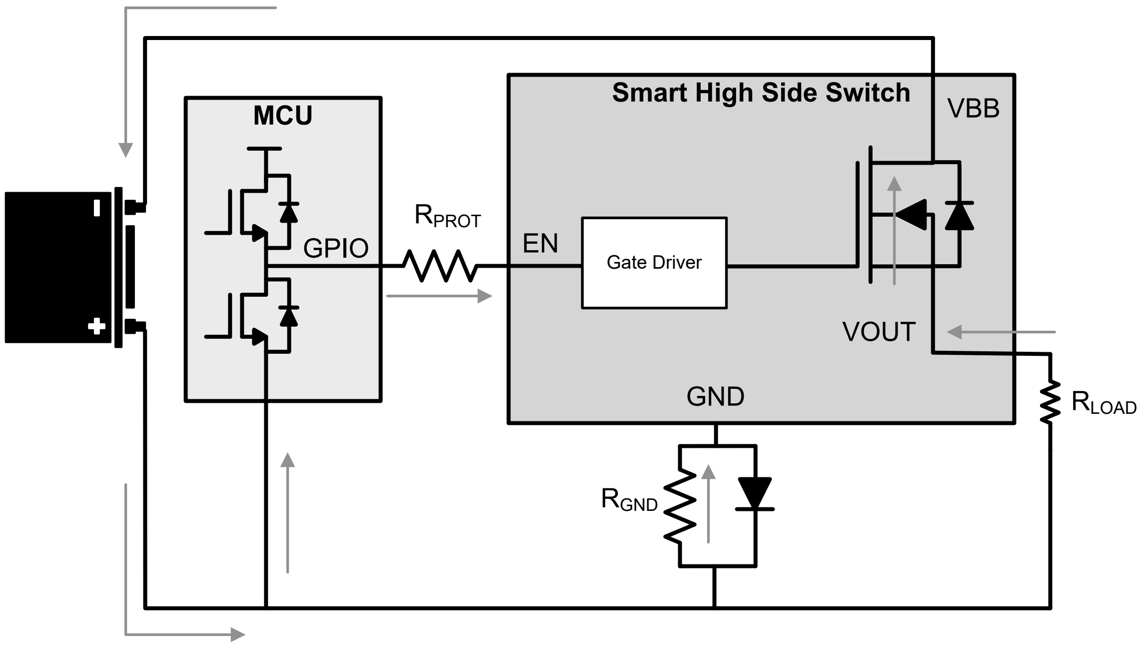


Figure 7-16. Reverse Battery Circuit

See also Section 7.3.8.4 and Table 7-3.

7.3.7.5 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (absolute thermal shutdown) and dynamic temperature protection (relative thermal shutdown). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

7.3.7.5.1 Thermal Protection Behavior

The thermal protection behavior can be split up into three categories of events that can happen. Figure 7-17 shows each of these categories.

1. **Relative thermal shutdown**: The device is enabled into an overcurrent event. The output current rises up to the I_{ILIM} level and the $\overline{FLT}$ goes low. With this large amount of current going through the junction temperature of the FET increases rapidly with respect to the controller temperature. When the power FET temperature rises T_{REL} amount above the controller junction temperature $\Delta T = T_{FET} - T_{CON} > T_{REL}$, the device shuts down. For auto-retry version, after t_{RETRY}, the part tries to restart. The latch version requires EN to be toggled to re-enable the channel. The $\overline{FLT}$ pin is asserted until the fault condition is cleared.
2. **Absolute thermal shutdown**: The device is still enabled in an overcurrent event. However, in this case the junction temperature rises up and hits an absolute reference temperature, T_{ABS}, and then shuts down. For auto-retry version, the device does not recover until both $T_J < T_{ABS} - T_{hys}$ and the t_{RETRY} timer has expired. For latch version, toggling EN is required to re-enable the channel.

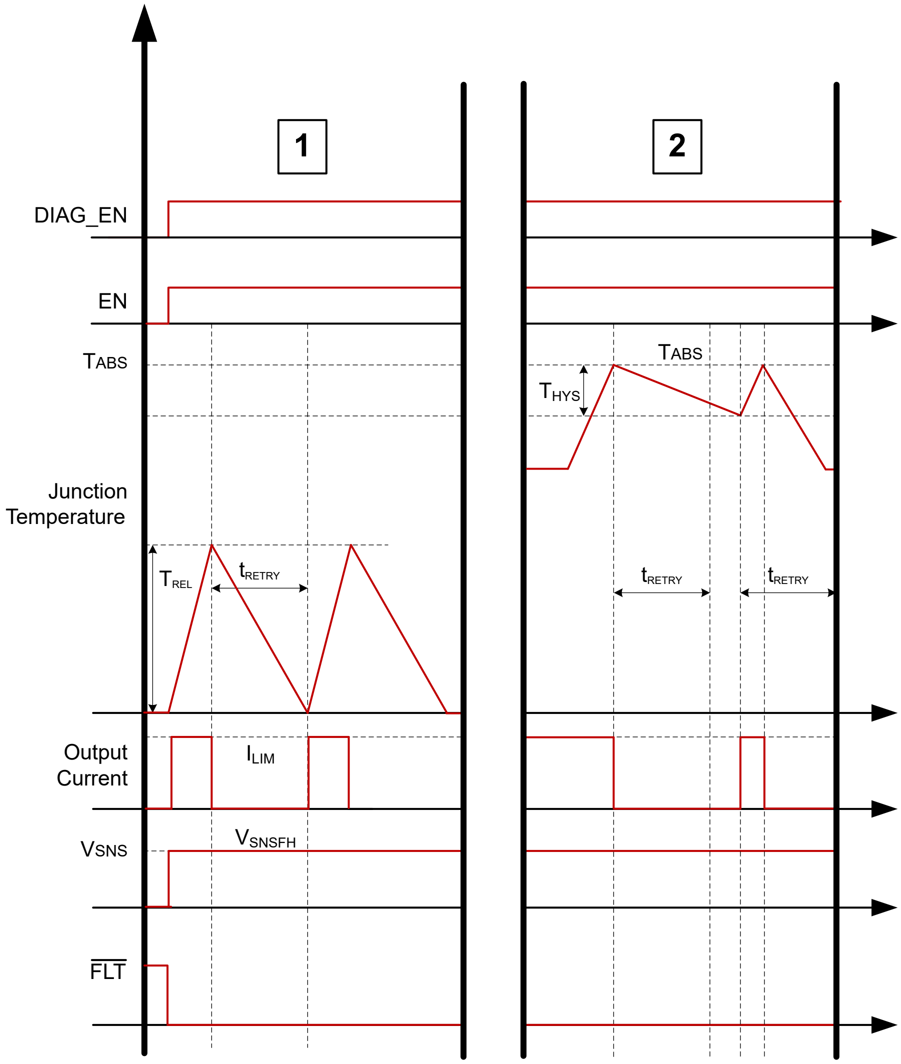


Figure 7-17. Thermal Behavior for Auto-Retry Version

7.3.8 Full Protections

7.3.8.1 UVLO Protection

The device monitors the supply voltage V_{VBB}, to prevent unpredicted behaviors when V_{VBB} is too low. When V_{VBB} falls down to V_{UVLOF}, the device shuts down. When V_{VBB} rises up to V_{UVLOR}, the device turns on.

7.3.8.2 Loss of GND Protection

When loss of GND occurs, output is turned off regardless of whether the input signal is high or low.

Case 1 (loss of device/IC GND): loss of GND protection is active when the thermal pad (Tab), IC GND, and current limit ground are one trace connected to the system ground, as shown in Figure 7-18.

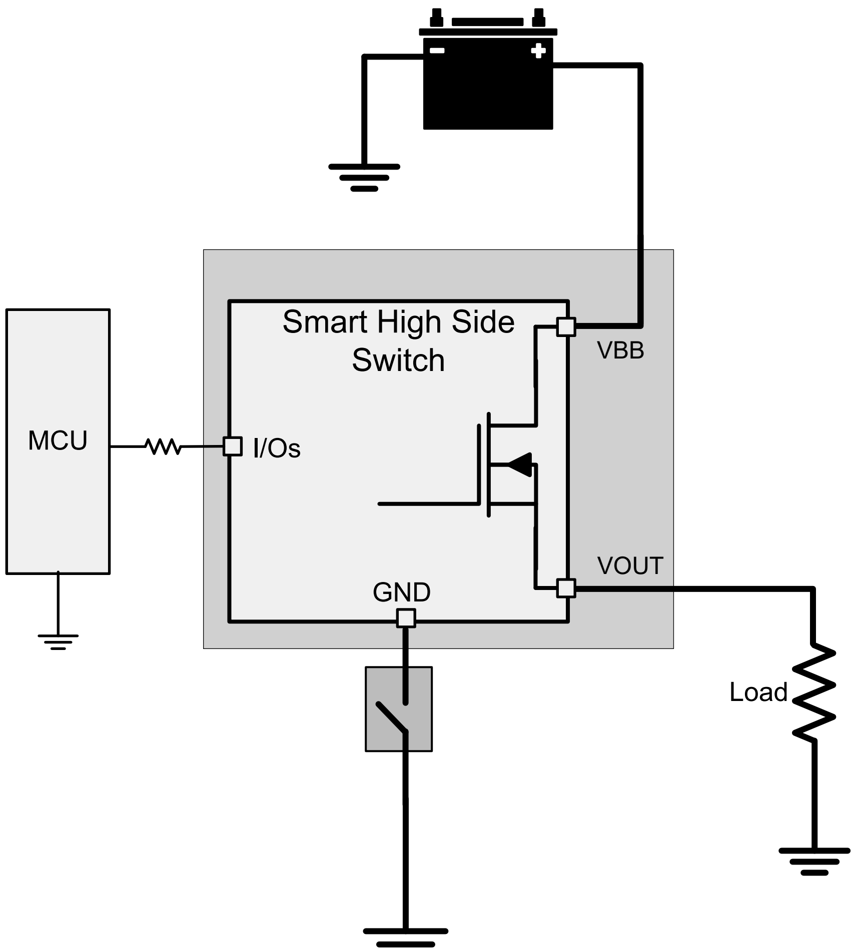


Figure 7-18. Loss of Device GND

Case 2 (loss of module GND): when the whole ECU module GND is lost, protections are also active. At this condition, the load GND remains connected.

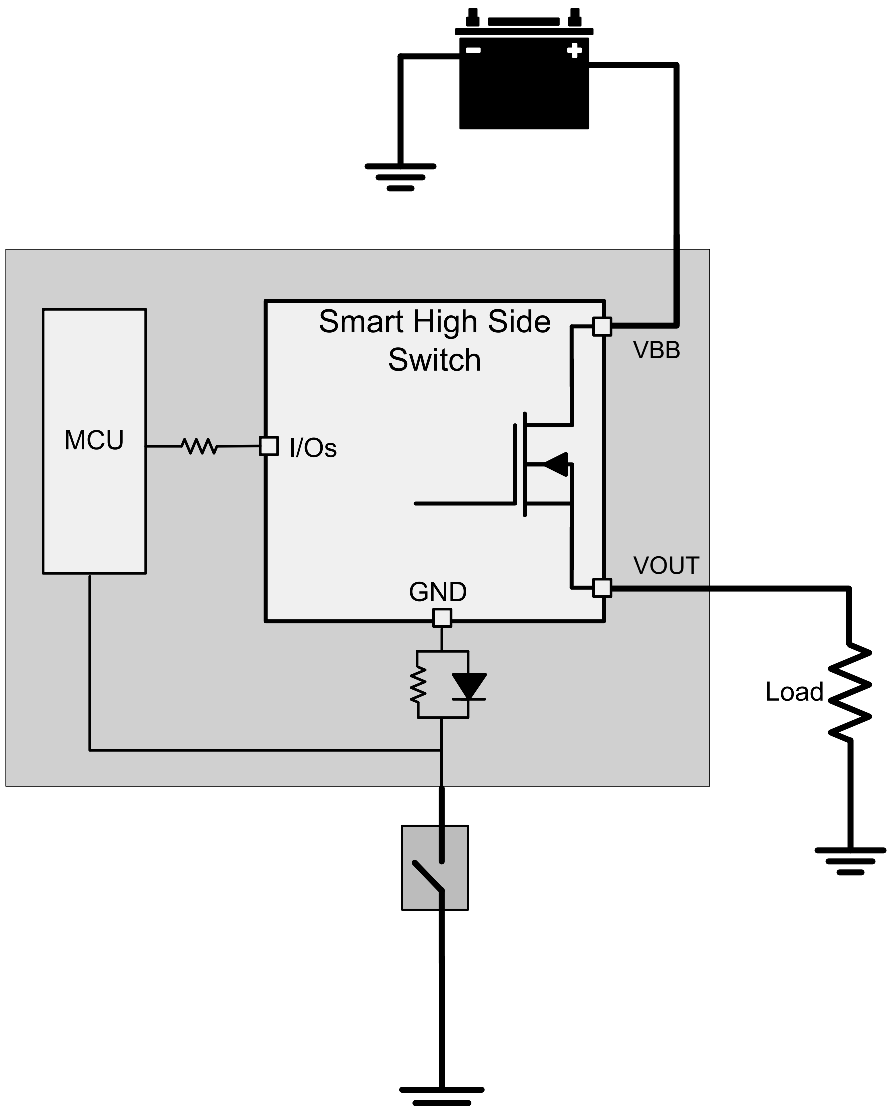


Figure 7-19. Loss of Module GND

7.3.8.3 Loss of Power Supply Protection

When loss of supply occurs, output is turned off regardless of whether the input is high or low. For a resistive or capacitive load, loss of supply protection is easy to achieve due to no more power. The worst case is a charged inductive load. In this case, the current is driven from all of the IOs to maintain the inductance output loop. TI recommends either the MCU serial resistor plus the GND network (diode and resistor in parallel) or external free-wheeling circuitry.

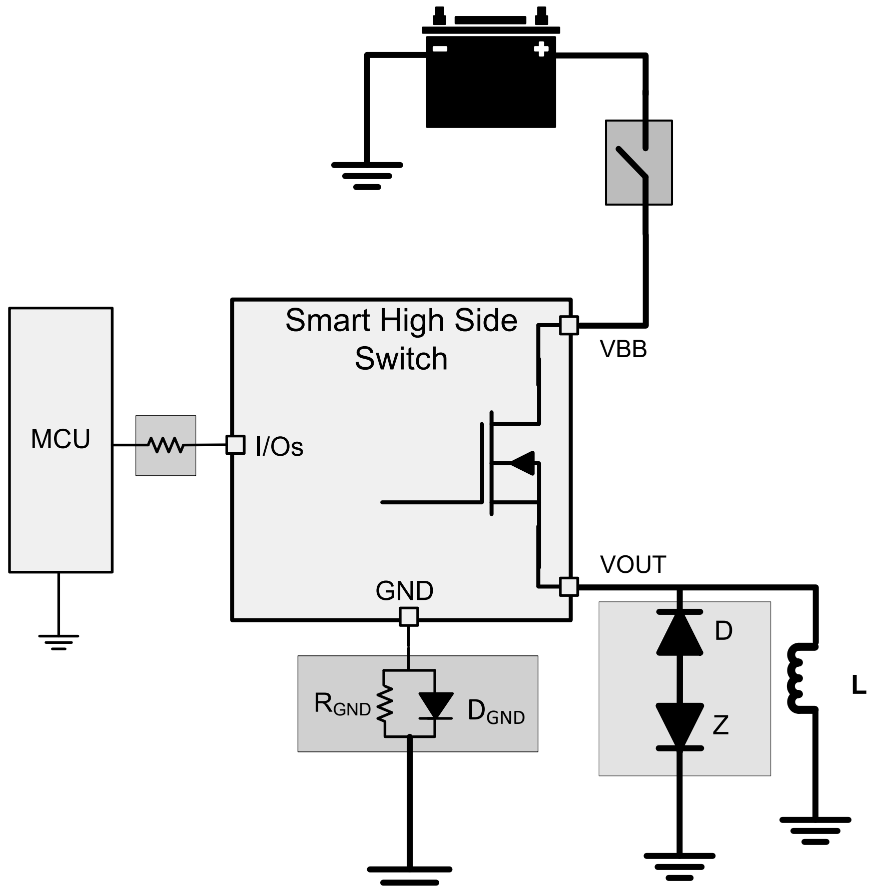


Figure 7-20. Loss of Battery

7.3.8.4 Reverse Polarity Protection

Method 1: Block diode connected with V_{BB}. Both the device and load are protected when in reverse polarity. The blocking diode does not allow any of the current to flow during reverse battery condition.

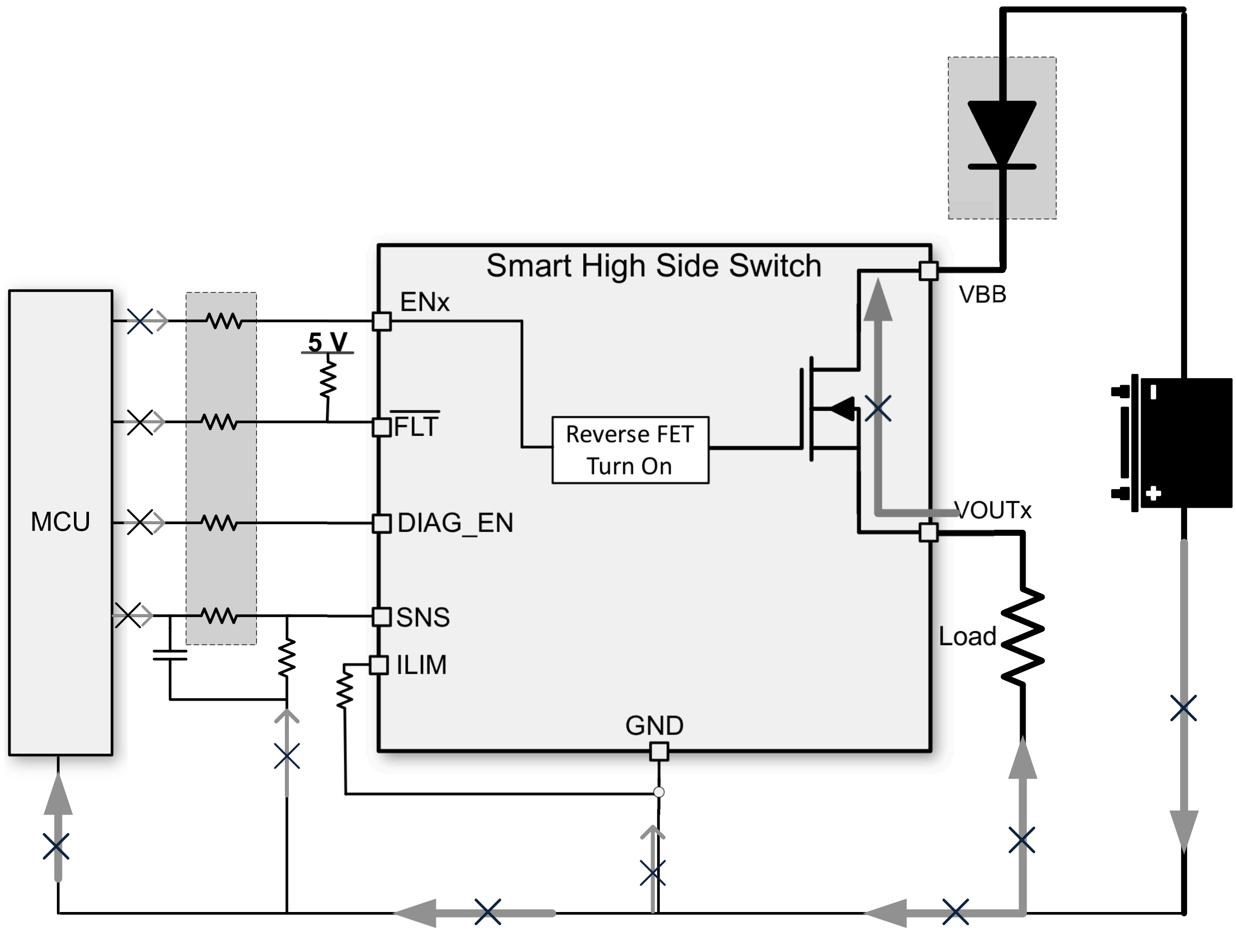


Figure 7-21. Reverse Protection With Block Diode

Method 2 (GND network protection): Only the high-side device is protected under this connection. The load reverse current is limited by the impedance of the load. When reverse polarity happens, the continuous reverse current through the power FET must not make the heat build up be greater than the absolute maximum junction temperature. Device temperature is calculated using the $R_{ON(REV)}$ value and the $R_{\theta JA}$ specification. In the reverse-battery condition, ensure that the FET comes on to lower the power dissipation. This action is achieved through the path from EN to system ground where the positive voltage is being applied. No matter what types of connection are between the device GND and the board GND, if a GND voltage shift happens, ensure the following proper connections for the normal operation:

- Connect the current limit programmable resistor to the device GND.

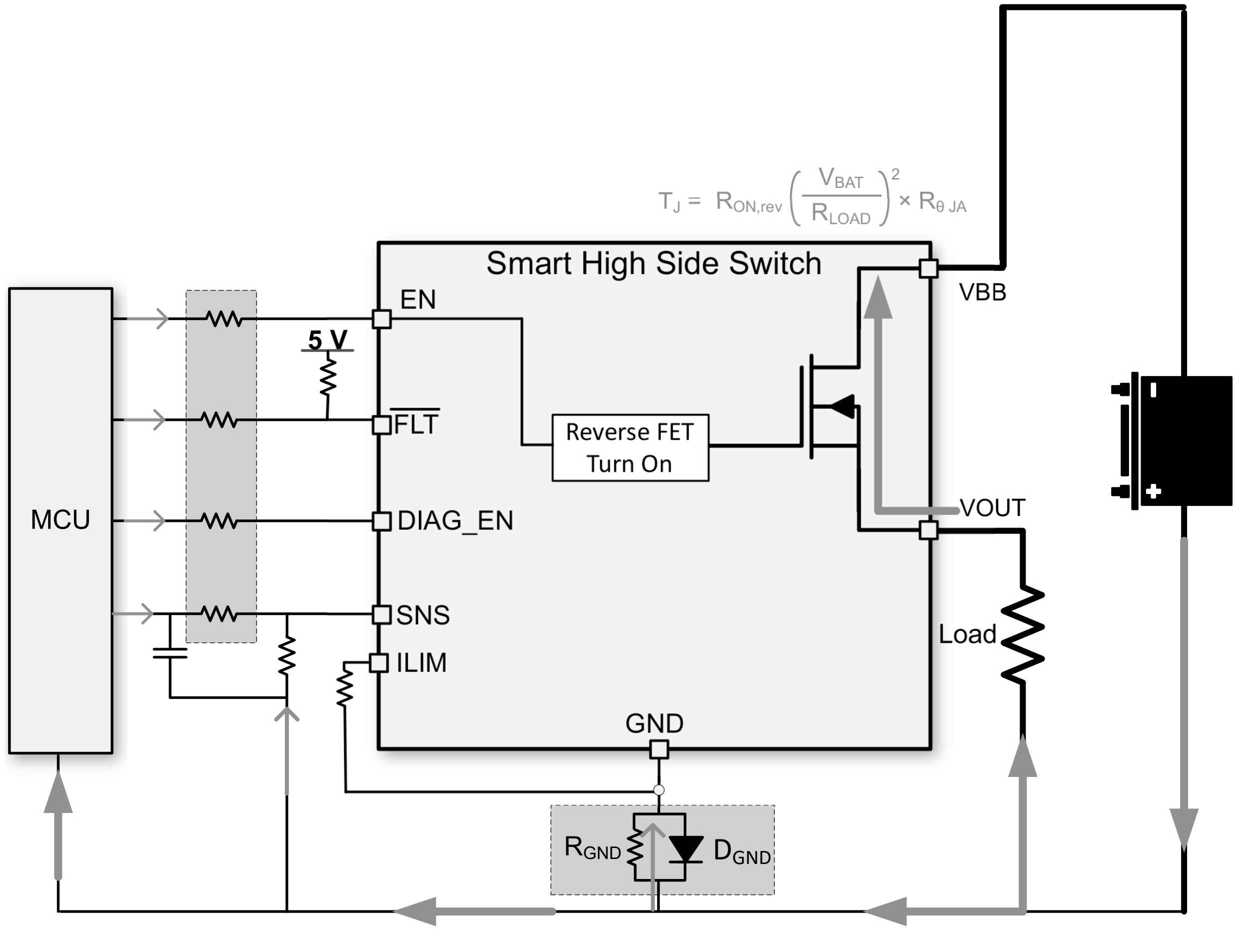


Figure 7-22. Reverse Protection With GND Network

- **Recommendation – resistor and diode in parallel:** A peak negative spike sometimes occurs when the inductive load is switching off, which can damage the HSD or the diode. Therefore, TI recommends a resistor in parallel with the diode when driving an inductive load. The recommended selection are a 1kΩ resistor in parallel with an I_F > 100mA diode. If multiple high-side switches are used, share the resistor and diode among devices.

  If multiple high-side power switches are used, share the resistor among devices.
- **Ground Resistor:** The higher resistor value contributes to a better current limit effect when the reverse battery or negative ISO pulses.

$$R_{GND} \geq \frac{(-V_{CC})}{(-I_{GND})} \tag{6}$$

  where

  – $-V_{CC}$ is the maximum reverse battery voltage (typically –16V).
  – $-I_{GND}$ is the maximum reverse current the ground pin can withstand, which is available in the *Absolute Maximum Ratings*.
- **Ground Diode:** A diode is needed to block the reverse voltage, which also brings a ground shift (≈600mV). Additionally, the diode must be ≈200V reverse voltage for the ISO 7637 pulse 1 testing so that the diode is not biased.

7.3.8.5 Protection for MCU I/Os

In many conditions, such as the negative ISO pulse, or the loss of battery with an inductive load, a negative potential on the device GND pin is able to potentially damage the MCU I/O pins (more likely, the internal circuitry connected to the pins). Therefore, serial resistors between MCU and HSS are required.

Also, for proper protection against loss of GND, TI recommends 10kΩ resistance for the R_{PROT} resistors.

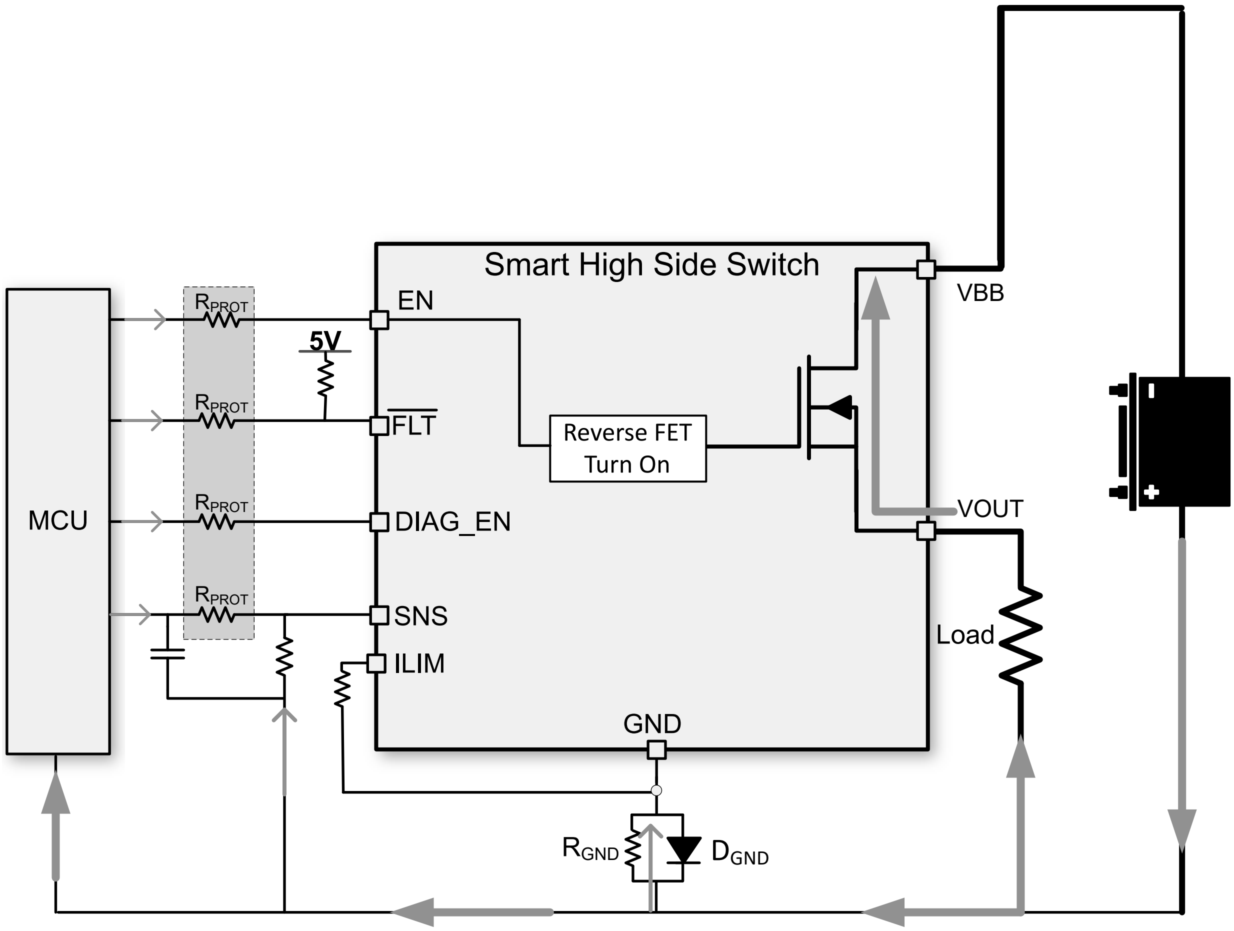


Figure 7-23. MCU I/O Protections

7.4 Device Functional Modes

7.4.1 Working Modes

This device has several states to transition into based on the ENx pins, DIAG_EN pin, and load conditions.

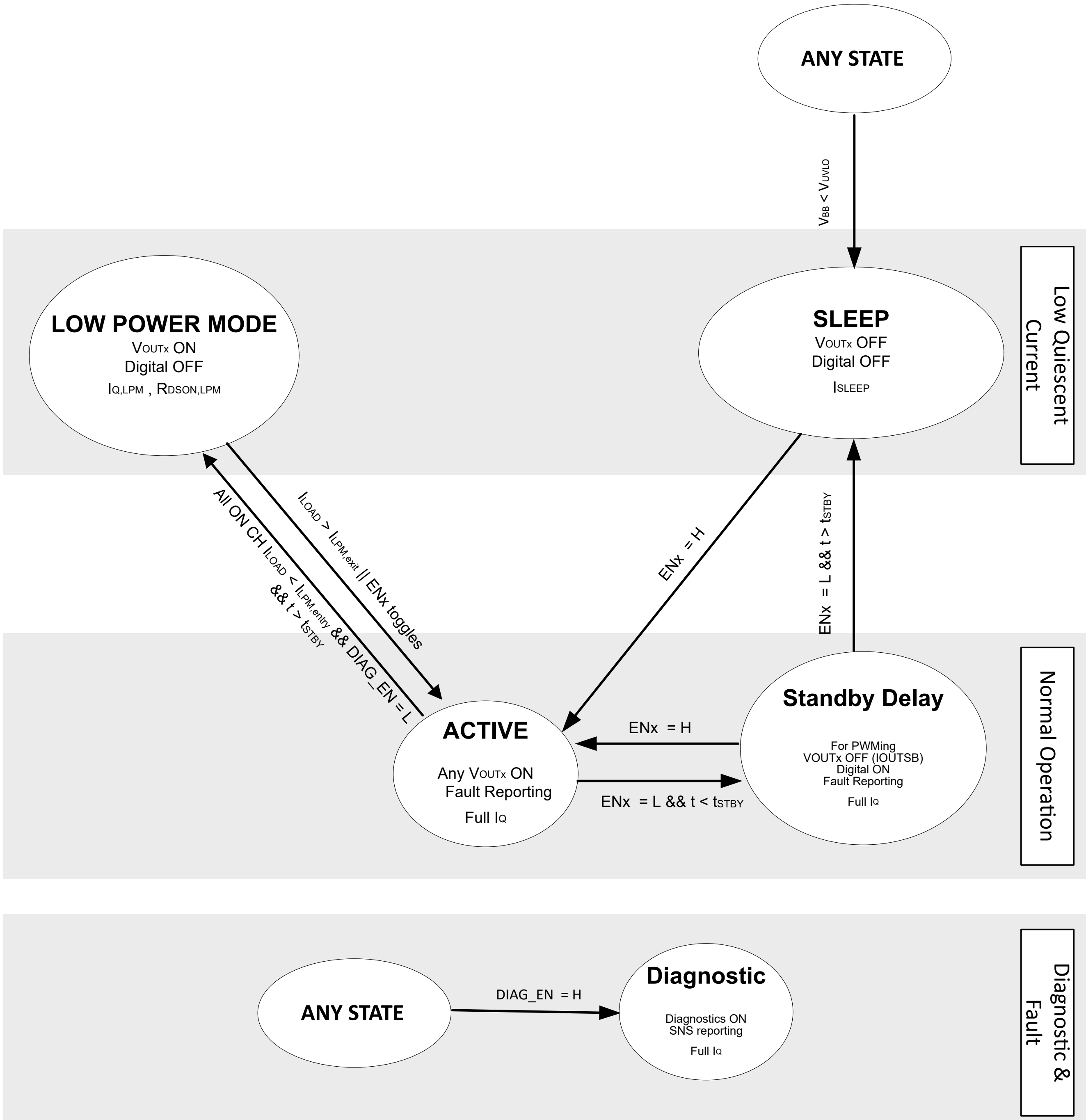


Figure 7-24. State Diagram

7.4.1.1 SLEEP

In the SLEEP state, everything inside the device is turned off and the quiescent current is the I_{SLEEP}. The device only transitions out of the SLEEP state if the ENx pins or DIAG_EN pin is pulled high. From the SLEEP state, the device is able to transfer into the ACTIVE state if any of the ENx pins are pulled high, or into the DIAGNOSTIC state if the DIAG_EN pin, without any of the ENx pins, goes high. Additionally, if the device is in any of the states and VBB drops to less than V_{UVLOF}, the device transitions into SLEEP state.

7.4.1.2 DIAGNOSTIC

The DIAGNOSTIC state is when the device is outputting diagnostics on the SNS and $\overline{FLT}$ pins. This state occurs when the device is in any previous state and the DIAG_EN pin goes high. The off-state diagnostics are comprised of open load detection in off-state and short-to-battery detection. The $\overline{FLT}$ pin asserts if there is a fault on any of the channels, but the SNS pin only outputs a fault for the channel associated to the SELx pin values. From the DIAGNOSTIC state, the device transfers into the ACTIVE state if the DIAG_EN pin goes back low and any channel is on, or into the STANDBY DELAY state if all channels are off.

7.4.1.3 ACTIVE

The ACTIVE state is when any of the channel outputs are on by the ENx pin associated. In the ACTIVE state, the current limit value is set by the external resistor on the ILIM pin. If the DIAG_EN pin is pulled high while in the ACTIVE state, the SNS pin outputs a proportional current to the load current of the channel associated to the SELx pins configuration until a fault occurs on that channel. Additionally the $\overline{FLT}$ pin reports if there is a fault occurring on any channel. The device can transition out of the ACTIVE state by turning off all of the channels while DIAG_EN is high or low, or a fault occurring. If all of the channels turn off and DIAG_EN is high, the device transitions into the DIAGNOSTIC state. If all of the channels turn off and the DIAG_EN pin is low, then the device transfers into the STANDBY DELAY state.

7.4.1.4 STANDBY DELAY

The STANDBY DELAY state is when the ENx pins are all low, the outputs are all turned off, and the DIAG_EN pin is also low, but there has not yet been t_{STBY} amount of time. This state is included so that the channel outputs are able to support PWM without all of the internal rails being cut off and put into SLEEP mode. After the device has waited t_{STBY}, the device completely shuts down and transitions into SLEEP. However, if during t_{STBY}, ENx goes high, the device transitions into ACTIVE without shutting completely down. Similarly if the DIAG_EN goes high, the device transitions into DIAGNOSTIC.

7.4.1.5 LOW POWER MODE

The LOW POWER MODE state is when the channels that are active are less than the $I_{LPM,entry}$ level for longer than t_{STBY} and the DIAG_EN is low. The device turns off all unnecessary internal blocks and reduces the quiescent current from I_Q to $I_{Q,LPM}$. The device is still protected but no diagnostics or fault reporting is possible until device comes out of this mode. See also Section 7.3.2.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS4HC120-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including the low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

8.1.1 EMC Transient Disturbances Test

As a result of the severe electrical conditions in the automotive environment, immunity capacity against electrical transient disturbances is required, especially for a high-side power switch, which is connected directly to the battery. Detailed test requirements are in accordance with the ISO 7637-2:2011 and ISO 16750-2:2010 standards.

Table 8-1. ISO 7637-2:2011(E) in 12V System

TEST ITEM (1) (2)	TEST PULSE SEVERITY LEVEL AND V_S ACCORDINGLY		PULSE DURATION (t_d)	MINIMUM NUMBER OF PULSES OR TEST TIME	BURST-CYCLE PULSE-REPETITION TIME		INPUT RESISTANCE (Ω)	FUNCTION PERFORMANCE STATUS CLASSIFICATION(3)
	LEVEL	V_S/V			MIN	MAX		
1	III	–112	2ms	500 pulses	0.5s	—	10	Status II
2a	III	55	50µs	500 pulses	0.2s	5s	2	Status II
2b	IV	10	0.2s to 2s	10 pulses	0.5s	5s	0 to 0.05	Status II
3a	IV	–220	0.1µs	1h	90ms	100ms	50	Status II
3b	IV	150	0.1µs	1h	90ms	100ms	50	Status II

(1) Tested both under input low condition and high condition.
(2) GND pin network is a 1kΩ resistor in parallel with a diode BAS21-7-F.
(3) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.

Table 8-2. ISO 16750-2:2010(E) Load Dump Test B in 12V System

TEST ITEM (1) (2) (3)	TEST PULSE SEVERITY LEVEL AND V_S ACCORDINGLY		PULSE DURATION (t_d)	MINIMUM NUMBER OF PULSES OR TEST TIME	BURST-CYCLE PULSE-REPETITION TIME	INPUT RESISTANCE (Ω)	FUNCTION PERFORMANCE STATUS CLASSIFICATION(4)
	LEVEL	V_S/V					
Test B	N/A	35	40ms to 400ms	5 pulses	60s	0.5 to 4	Status II

(1) Tested both under input low condition and high condition (DIAG_EN, ENx, and VBB are all classified as inputs).
(2) Considering the worst test condition, the device is tested without any filter capacitors on VBB and VOUTx.
(3) The GND pin network is a 1kΩ resistor in parallel with a diode BAS21-7-F.
(4) Status II: The function does not perform as designed during the test, but returns automatically to normal operation after the test.

8.2 Typical Application

Figure 8-1 shows an example of the external circuitry connections for TPS4HC120.

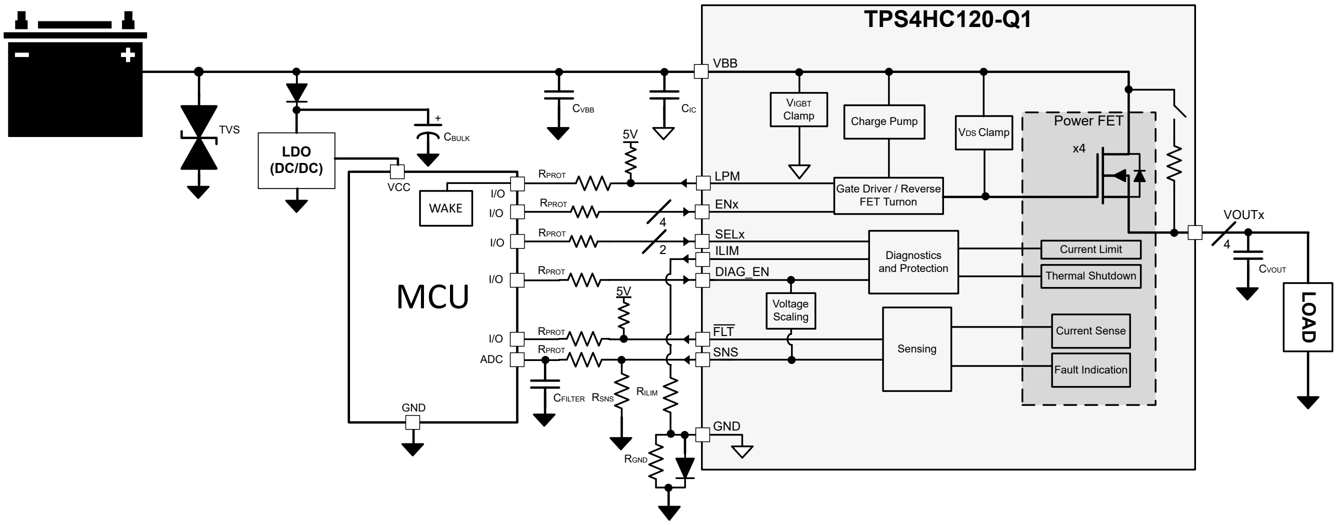


Figure 8-1. Typical Application Diagram

Table 8-3. Recommended Component Values

COMPONENT	DESCRIPTION	PURPOSE
TVS	SMBJ39CA	Filter voltage transients coming from battery (ISO7637-2)
C_{VBB}	220nF	Better EMI performance
C_{IC}	100nF	Minimal amount of capacitance on input for EMI mitigation
C_{BULK}	10µF	Help filter voltage transients on the supply rail
R_{PROT}	10kΩ	Protection resistor for microcontroller and device I/O pins
R_{LIM}	Discrete values as listed in Table 7-1	Set current limit threshold
R_{SNS}	1kΩ	Translate the sense current into sense voltage
C_{FILTER}	100nF	Coupled with RPROT on the SNS line creates a low pass filter to filter out noise going into the ADC of the MCU
C_{VOUT}	22nF	Improves EMI performance, filtering of voltage transients
R_{PULLUP}	5kΩ	Pull up resistor for open-drain pins ($\overline{FLT}$ and LPM)
R_{GND}	1kΩ	Stabilize GND potential during turn-off of inductive load
D_{GND}	BAS21 Diode	Keeps GND close to system ground during normal operation

8.2.1 Design Requirements

Table 8-4. Example Design Requirements

PARAMETER	VALUE
V_{DIAG_EN}	5V
$I_{LOAD,max}$	1A
$I_{LOAD,min}$	10mA
$V_{ADC,min}$	5mV
V_{HR}	1V

8.2.2 Detailed Design Procedure

To keep the 1A nominal current in the 0V to 4V current-sense range, calculate the $R_{(SNS)}$ resistor using Equation 7. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

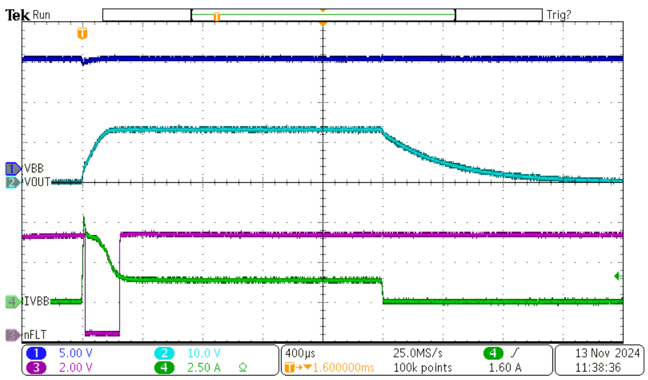
$$V_{ADC,min} \times K_{SNS} / I_{LOAD,min} \leq R_{SNS} \leq (V_{SNSFH} - V_{HR}) \times K_{SNS} / I_{LOAD,max} \quad (7)$$

The design requirement listed in Table 8-4 yields 520Ω ≤ R_{SNS} ≤ 4160Ω, and 1kΩ R_{SNS} satisfies the requirements.

To set the adjustable current limit value, use the $R_{(ILIM)}$ recommended in the Current Limit Table. In this application, to leave enough margin for the current transient and ripple, a 9.76kΩ R_{ILIM} resistor satisfies the requirements.

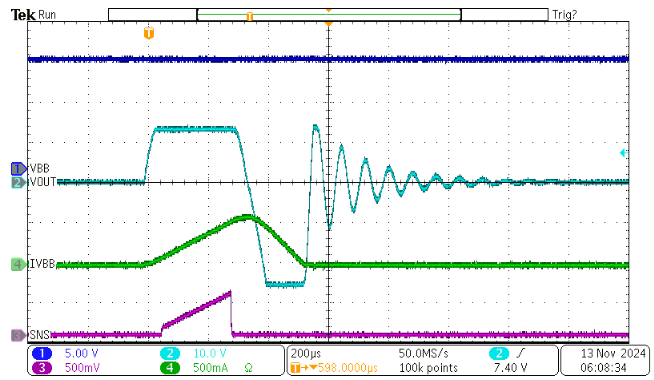
8.2.3 Application Curves

Figure 8-2 shows a test example of soft-start when driving a big capacitive load. Figure 8-3 shows the VDS clamp engaging during inductive load discharge.



V_{BB} = 13.5V R_{SNS} = 1kΩ ILIM = OPEN
Z_{OUT} = 10Ω + 47µF T_{AMB} = 25°C

Figure 8-2. Capacitive Load Driving



V_{BB} = 13.5V R_{SNS} = 1kΩ ILIM = OPEN
Z_{OUT} = 5.5mH T_{AMB} = 25°C

Figure 8-3. Inductive Load Discharge

8.3 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12V automotive system. The supply voltage must be within the range specified in the *Recommended Operating Conditions*.

Table 8-5. Voltage Operating Ranges

VBB VOLTAGE RANGE	NOTE
3V to 6V	Extended lower 12V automotive battery operation such as cold crank and start-stop. Device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy and timing parameters can deviate from specifications. Check the individual specifications in Section 6.5 to confirm the applicable voltage range.
6V to 18V	Nominal 12V automotive battery voltage range. All parametric specifications apply and the device is fully functional and protected.
18V to 24V	Extended upper 12V automotive battery operation such as double battery. Device is fully functional and protected but some parametrics such as R_{ON}, current sense accuracy, current limit accuracy, and timing parameters can deviate from specifications. Check the individual specifications in Section 6.5 to confirm the applicable voltage range.
35V	Load dump voltage. Device is operational and lets the pulse pass through without being damaged but does not protect against short circuits.

8.4 Layout

8.4.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design helps optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when no heat sinks are attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- To prevent solder voids, ensure that all thermal vias are either plated shut or plugged and capped on both sides of the board. To maintain reliability and performance, the maintain at least 85% solder coverage.

8.4.2 Layout Examples

8.4.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

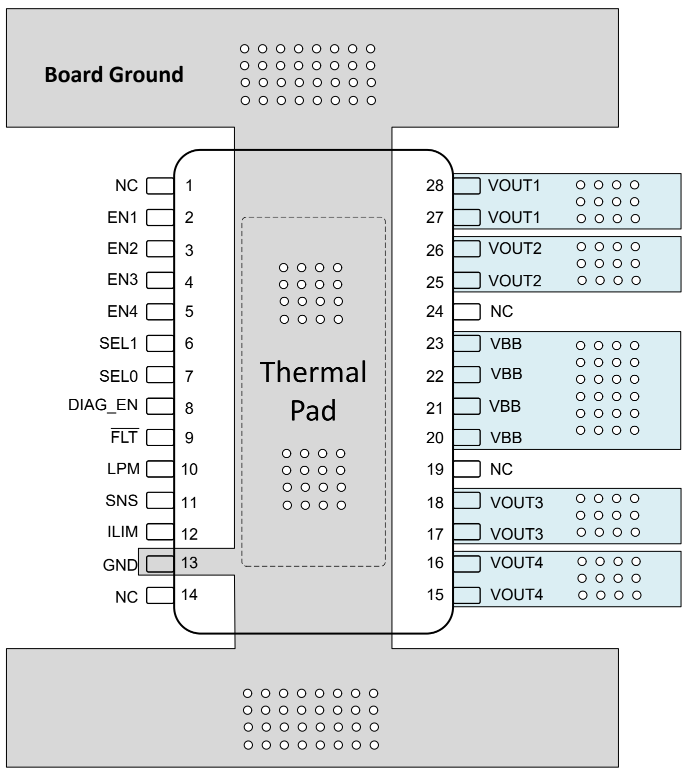


Figure 8-4. Layout Example Without a GND Network

8.4.2.2 With a GND Network

With a GND network, tie the thermal pad with a single trace through the GND network to the board GND copper. Have more IC GND coverage to get better thermal performance of the part.

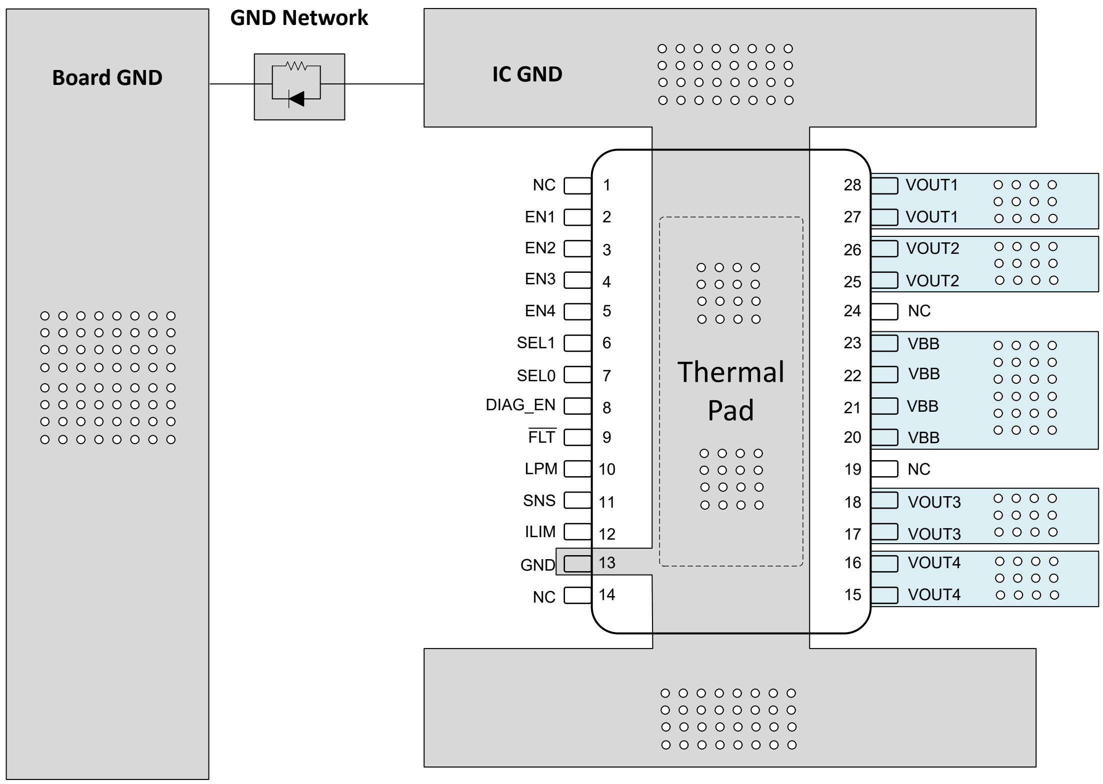


Figure 8-5. Layout Example With a GND Network

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2025) to Revision B (July 2025) — **Page**

- Changed TPS4HC120B-Q1 status from preview to production data (active)........ 1
- Updated formatting and page flow for clarity........ 1

Changes from Revision * (December 2024) to Revision A (January 2025) — **Page**

- Added *Device Comparison Table* 2
- Updated to show LPM pin added........ 14
- Added description for both auto-retry and latch versions........ 19
- FLT now reports regardless of DIAG_EN........ 22
- FLT now reports regardless of DIAG_EN........ 24
- Updated the table to add description for auto-retry and latch versions........ 24

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS4HC120AQDGQRQ1	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4HC120A
TPS4HC120AQDGQRQ1.A	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4HC120A
TPS4HC120BQDGQRQ1	Active	Production	HVSSOP (DGQ) | 28	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	4HC120B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

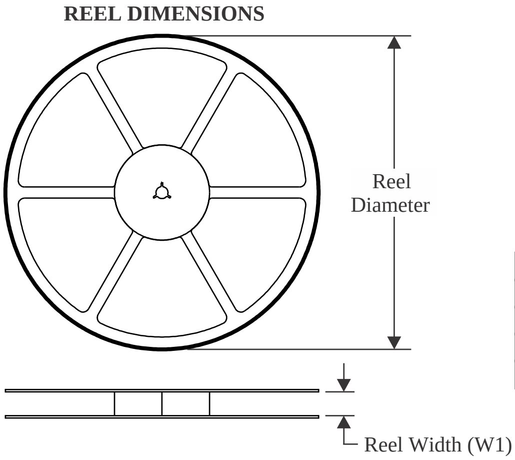
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

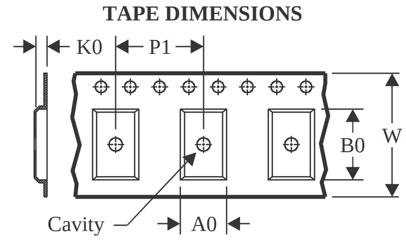
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

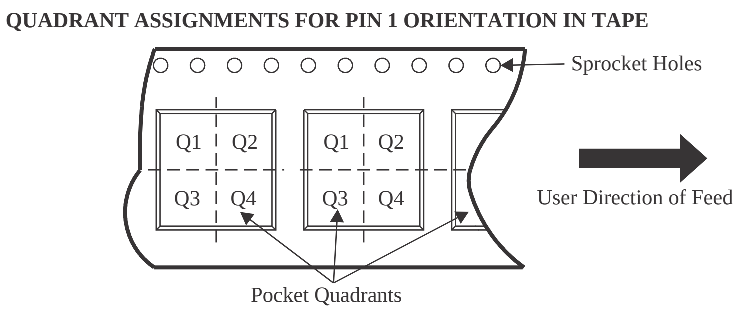
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





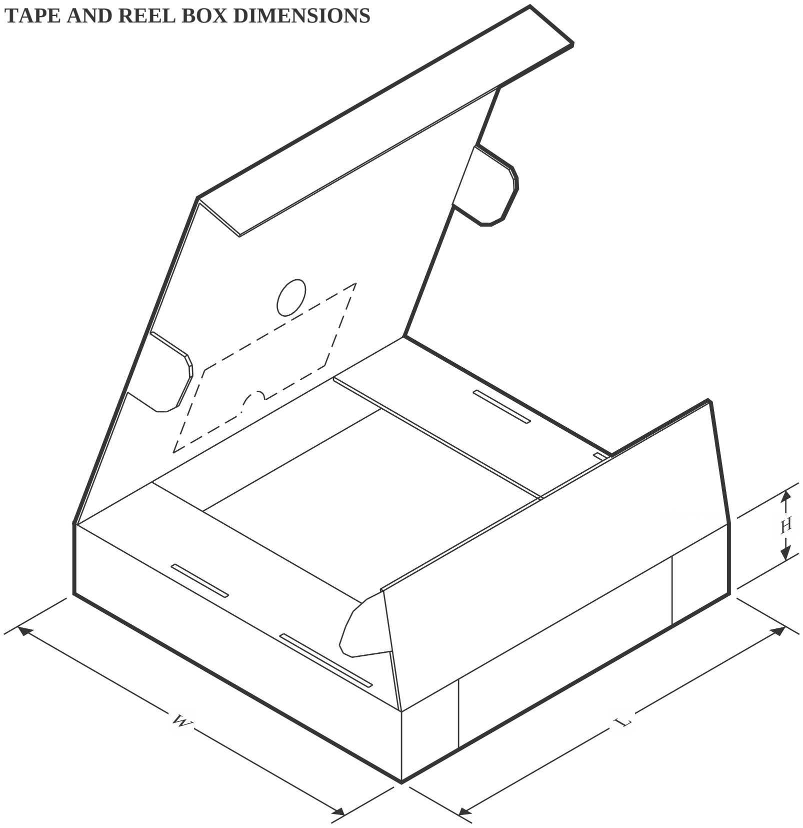
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS4HC120AQDGQRQ1	HVSSOP	DGQ	28	2500	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1
TPS4HC120BQDGQRQ1	HVSSOP	DGQ	28	2500	330.0	16.4	5.5	7.4	1.45	8.0	16.0	Q1

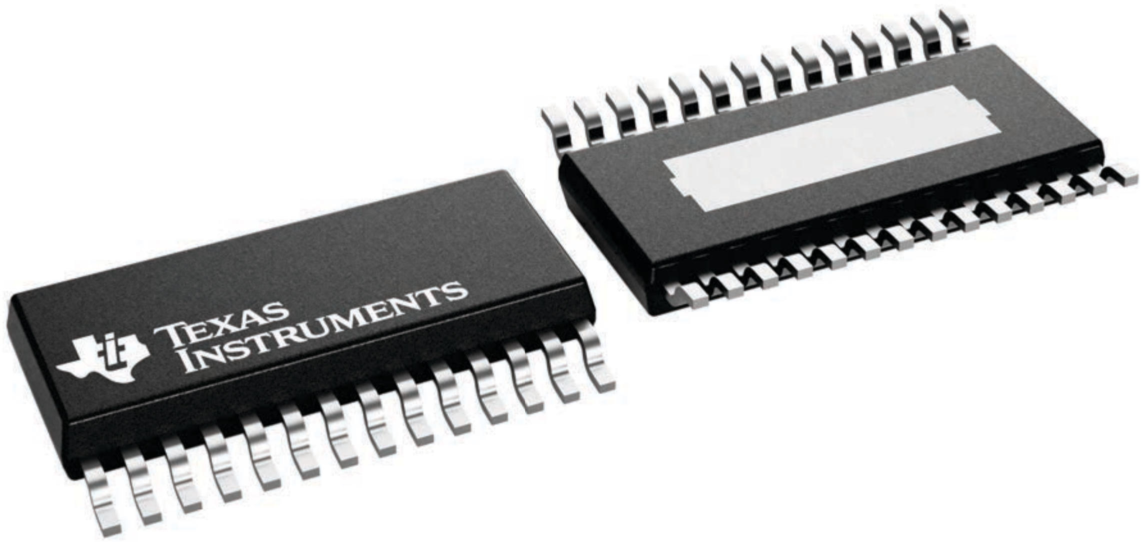
TAPE AND REEL BOX DIMENSIONS

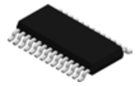


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS4HC120AQDGQRQ1	HVSSOP	DGQ	28	2500	353.0	353.0	32.0
TPS4HC120BQDGQRQ1	HVSSOP	DGQ	28	2500	353.0	353.0	32.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

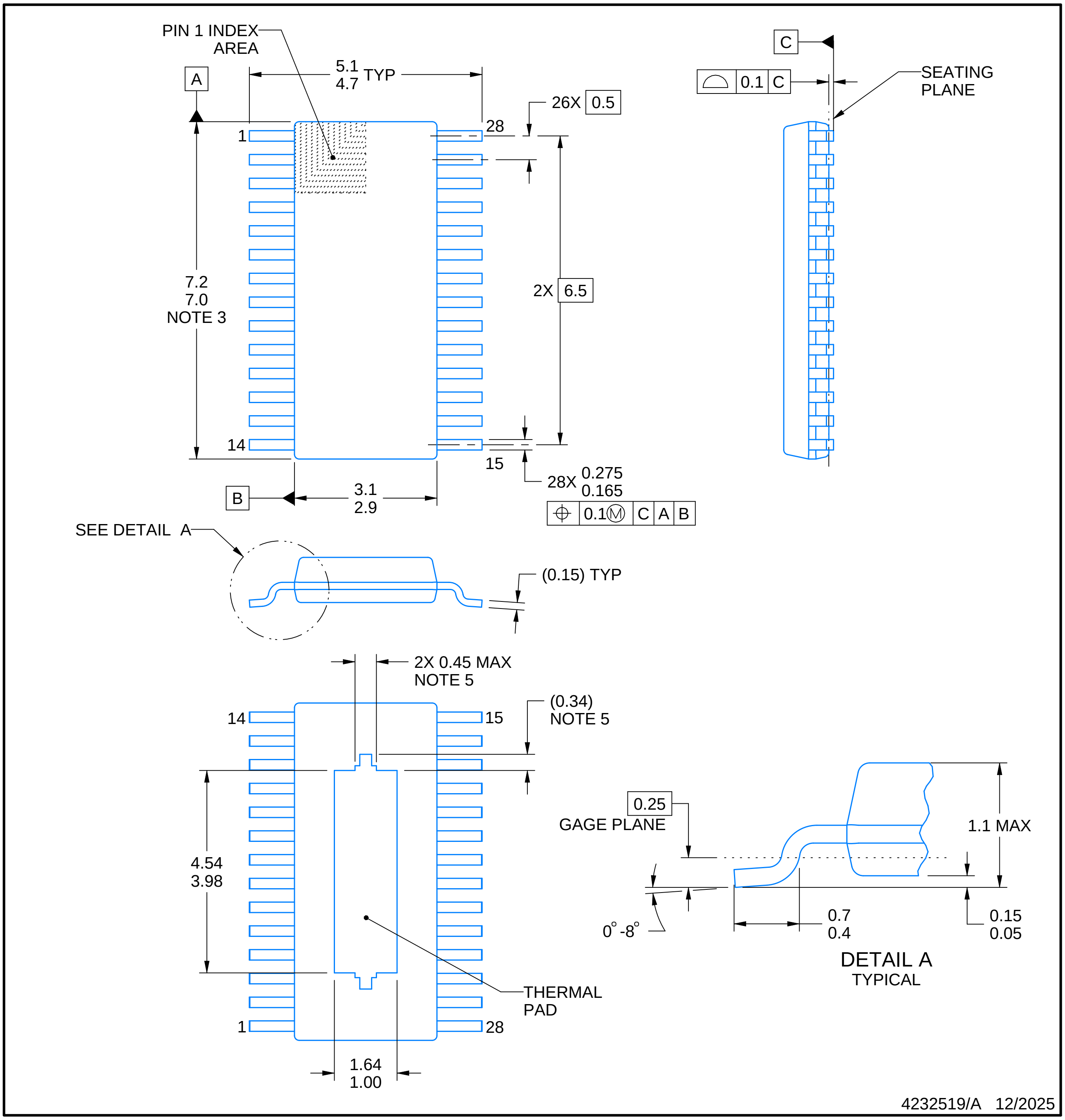




DGQ0028C

PowerPAD™ VSSOP - 1.1 mm max height

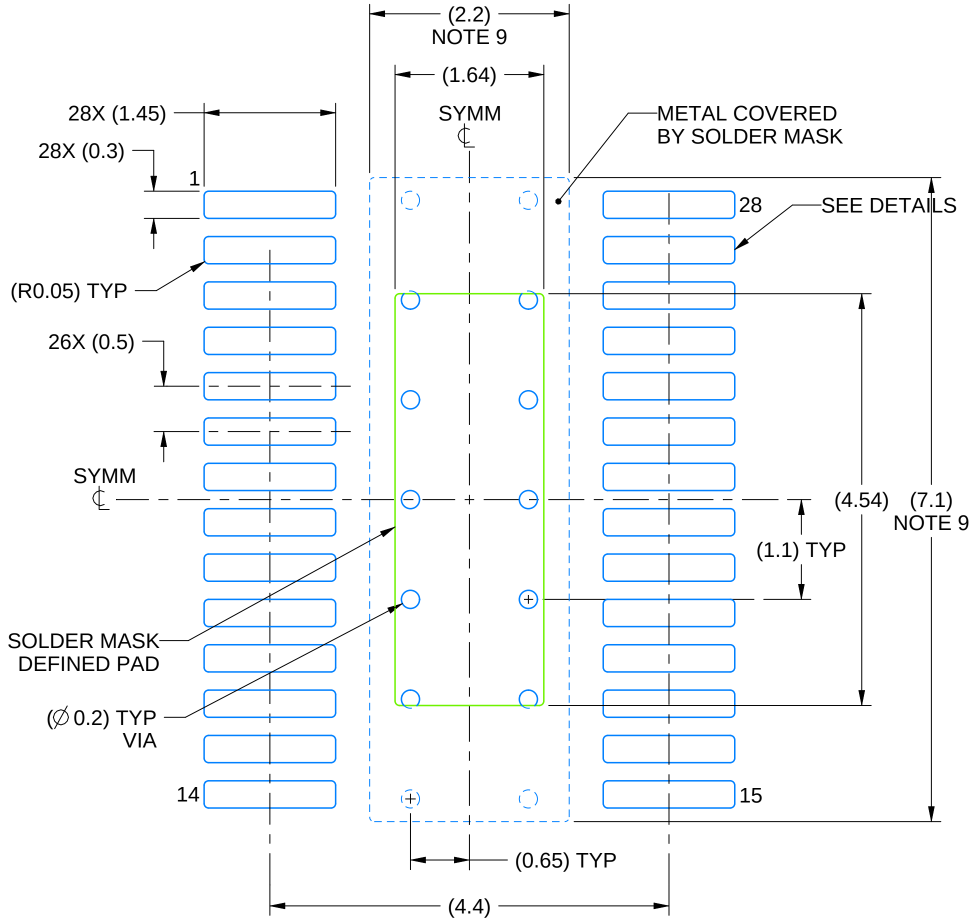
SMALL OUTLINE PACKAGE



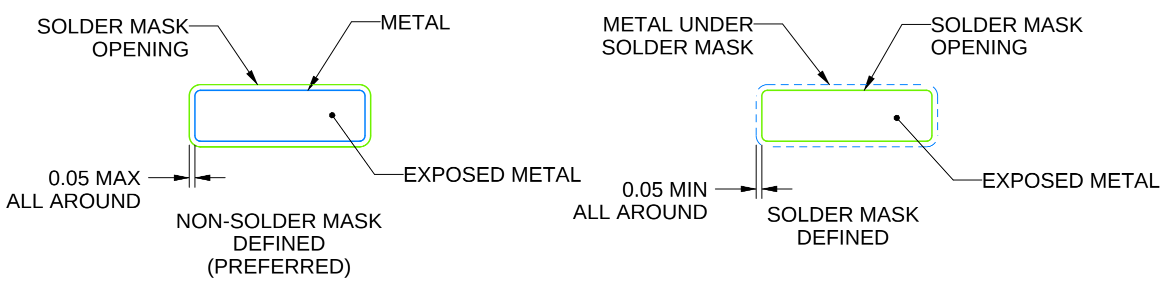
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

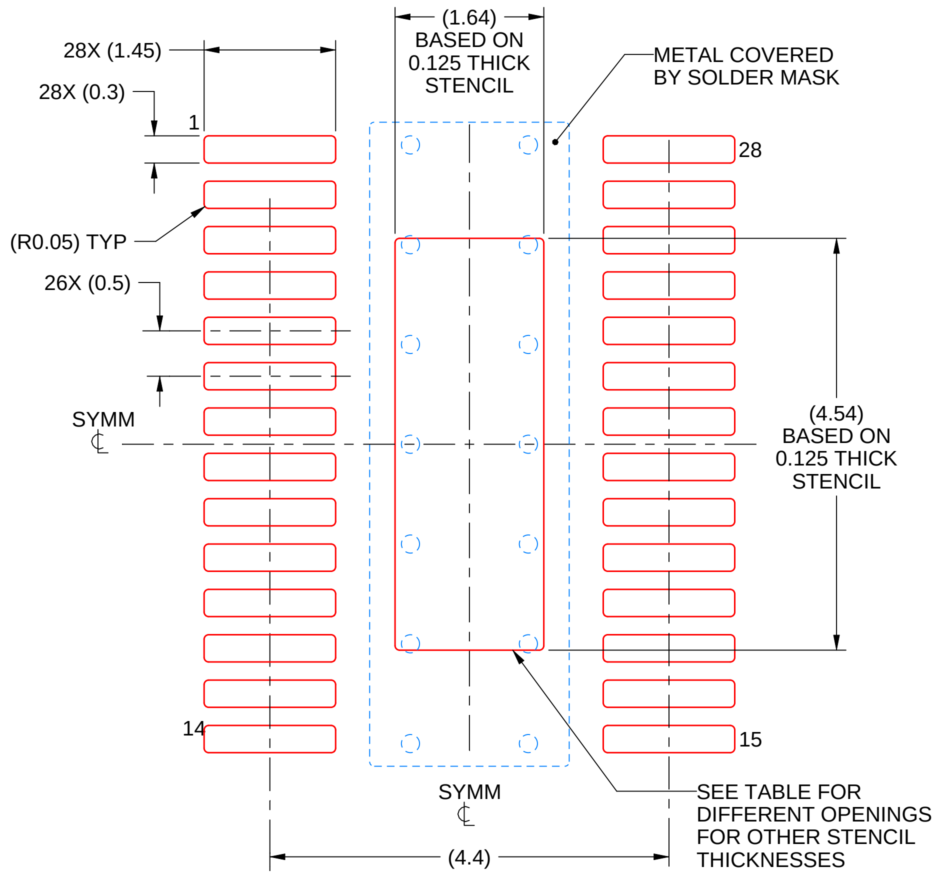


SOLDER MASK DETAILS

4232519/A 12/2025

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.83 X 5.08
0.125	1.64 X 4.54 (SHOWN)
0.15	1.50 X 4.14
0.175	1.39 X 3.84

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.