

# TPS51633 3-Phase, D-CAP+™ Step-Down Controller for VR12.6 V<sub>CPU</sub>

## 1 Features

- Intel® VR12.6 PWM Specification serial VID (SVID) compliant
- 1-, 2-, or 3-phase operation
- Full VR12.6 mobile feature set including digital current monitor, PS3 and PS4 operation
- 8-Bit DAC with 0.50-V to 2.30-V output range
- Optimized efficiency at light and heavy loads
- 8 independent levels of overshoot reduction (OSR) and undershoot reduction (USR)
- Driverless configuration for efficient high-frequency switching
- Supports discrete, Power Block, Power Stage or DrMOS MOSFET implementations
- Accurate, adjustable voltage positioning
- 300-kHz to 800-kHz frequency selections
- Patented AutoBalance Phase Balancing
- Selectable 8-level current limit
- 4.5-V to 28-V conversion voltage range
- Small, 4 × 4, 32-Pin, QFN PowerPAD™ integrated circuit package

## 2 Applications

- Adapter
- Battery
- NVDC
- 5-V or 12-V Rails

## 3 Description

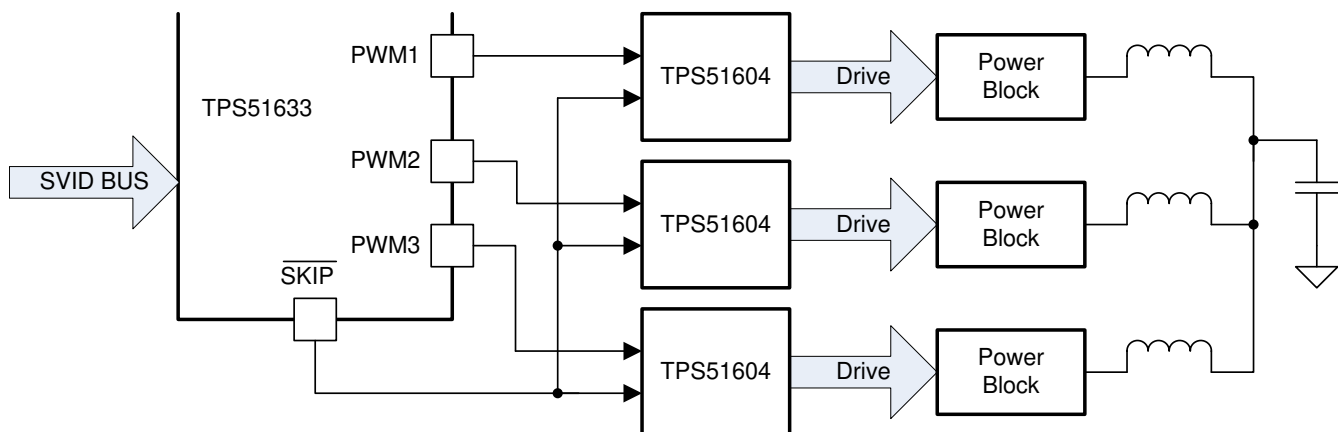
The TPS51633 device is a driverless step-down controller that is fully compliant with the SVID communications protocol, meeting the Intel VR12.6 specification. Advanced control features such as D-CAP+ architecture with overlapping pulse support undershoot reduction (USR) and overshoot reduction (OSR) provide fast transient response, lowest output capacitance and high efficiency. The TPS51633 device also supports single-phase operation in CCM or DCM for light-load efficiency. The TPS51633 device integrates the full complement of VR12.6 I/O features including VR\_READY (PGOOD), ALERT and VR\_HOT. The SVID interface address allows programming from 0 to 7.

In PS4, the quiescent power consumption of the controller is typically 0.25 mW. Adjustable control of VCPU slew rate and voltage positioning round out the VR12.6 features. Paired with the new TPS51604 FET gate driver, the solution delivers exceptionally high speed and low switching loss. The TPS51633 device works with selected TI Power Stage™ products for optimum efficiency as well as DrMOS products.

The TPS51633 device is available in space saving, thermally enhanced 32-pin QFN package that operates from –40°C to 105°C.

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE (NOM)
TPS51633	VQFN (32)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the document.



**Figure 3-1. Simplified Schematic**



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## 4 Revision History

DATE	REVISION	NOTES
June 2022	*	Initial release.

## 5 Device and Documentation Support

### 5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 5.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 5.3 Trademarks

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### 5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 5.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS51633RSMR</a>	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TPS 51633
TPS51633RSMR.A	Active	Production	VQFN (RSM)   32	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TPS 51633
<a href="#">TPS51633RSMT</a>	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TPS 51633
TPS51633RSMT.A	Active	Production	VQFN (RSM)   32	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	TPS 51633

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

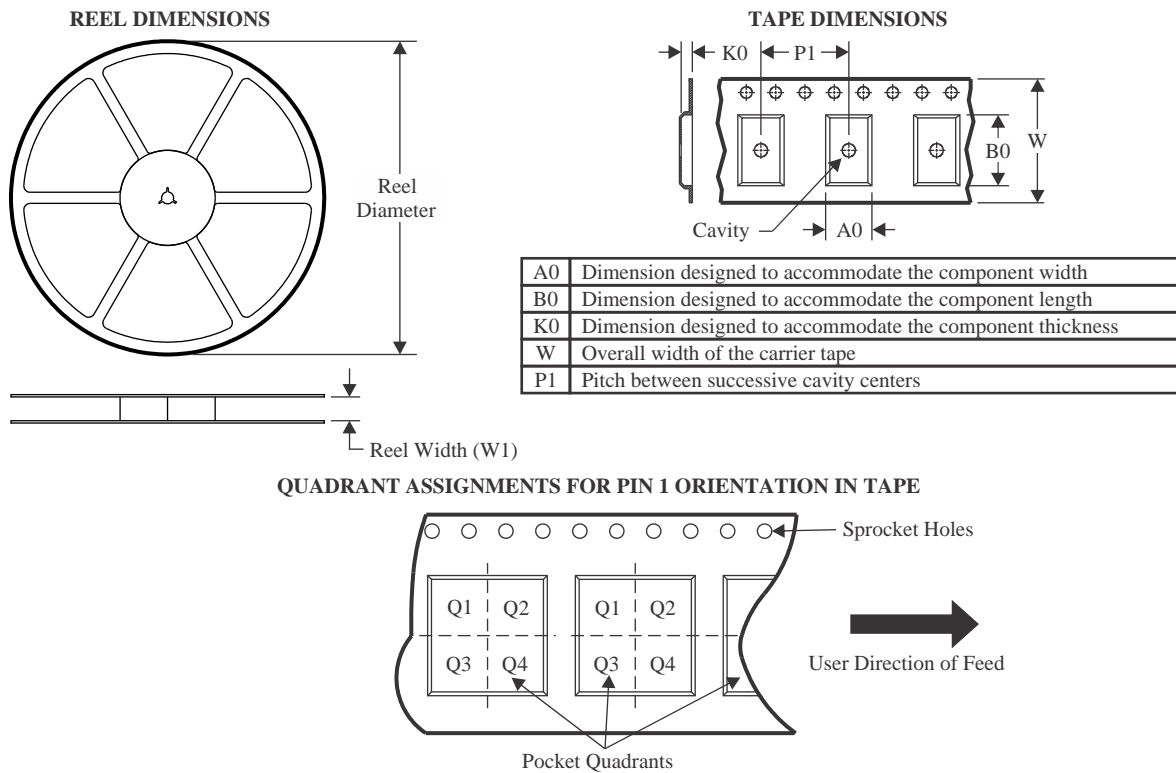
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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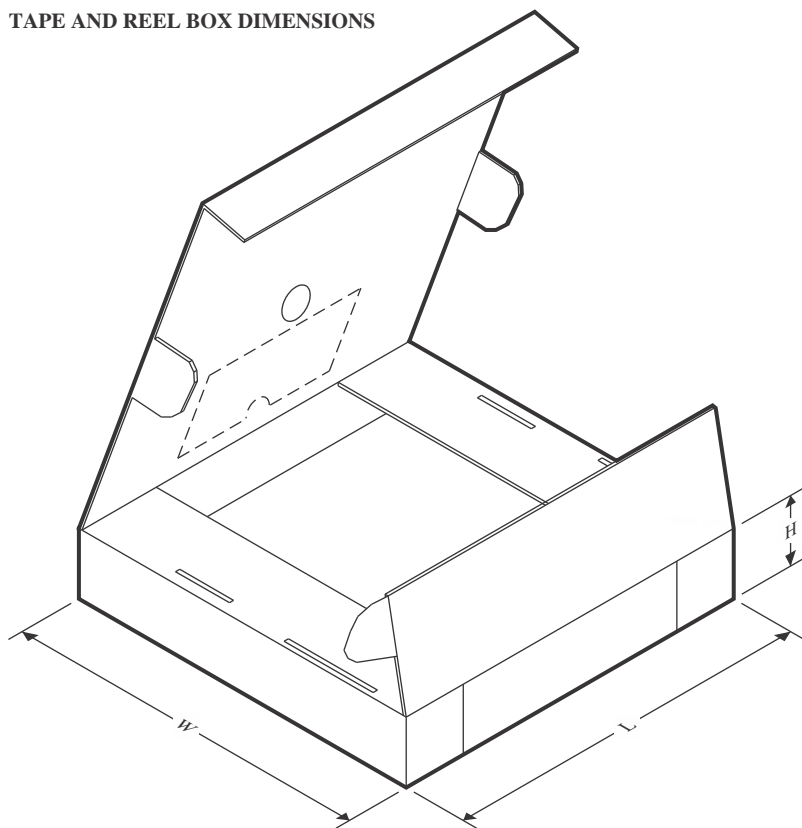
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51633RSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS51633RSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51633RSMR	VQFN	RSM	32	3000	346.0	346.0	33.0
TPS51633RSMT	VQFN	RSM	32	250	182.0	182.0	20.0

## GENERIC PACKAGE VIEW

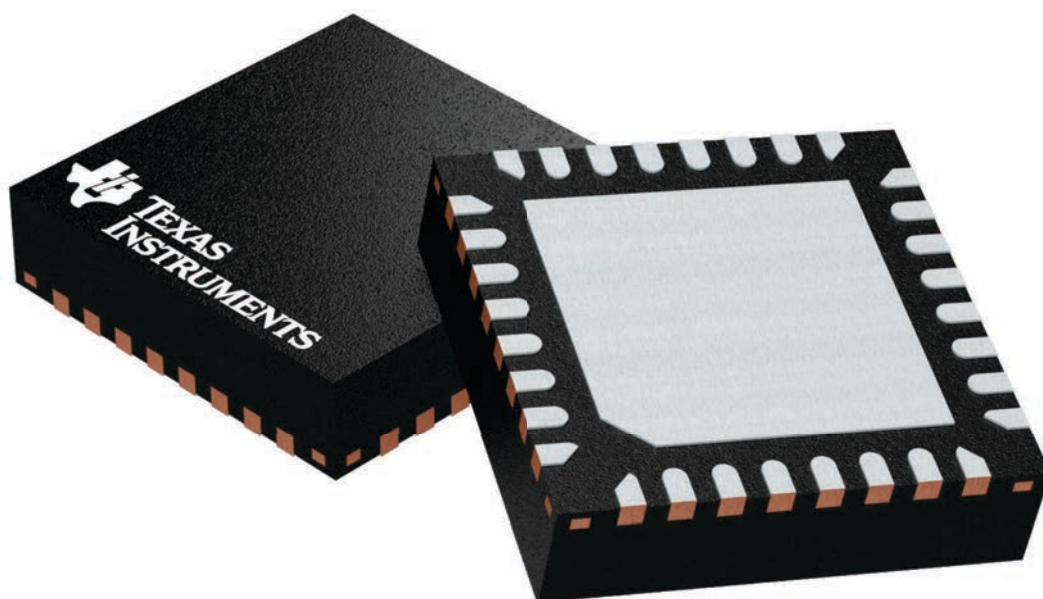
**RSM 32**

**VQFN - 1 mm max height**

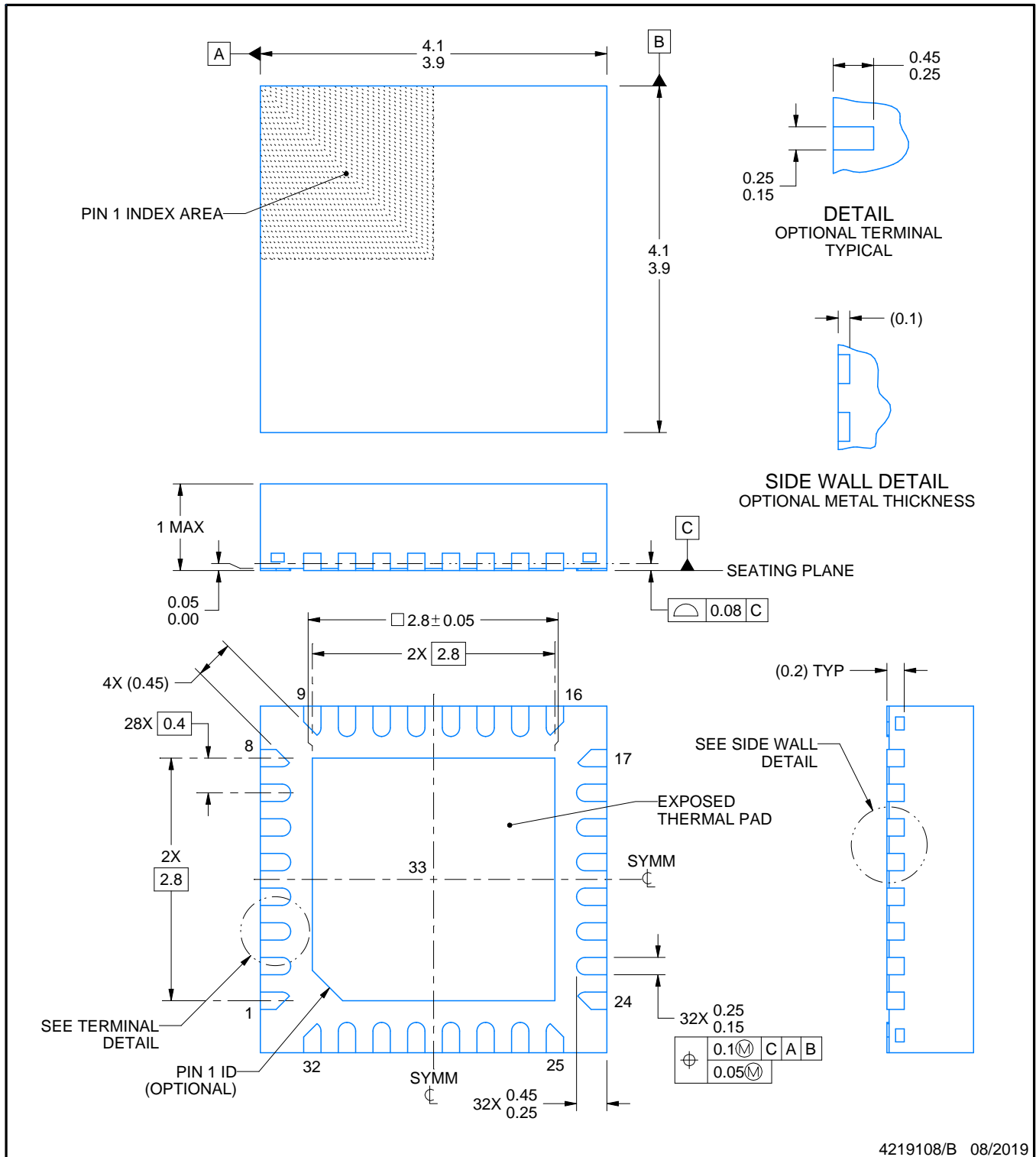
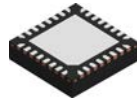
4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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## NOTES:

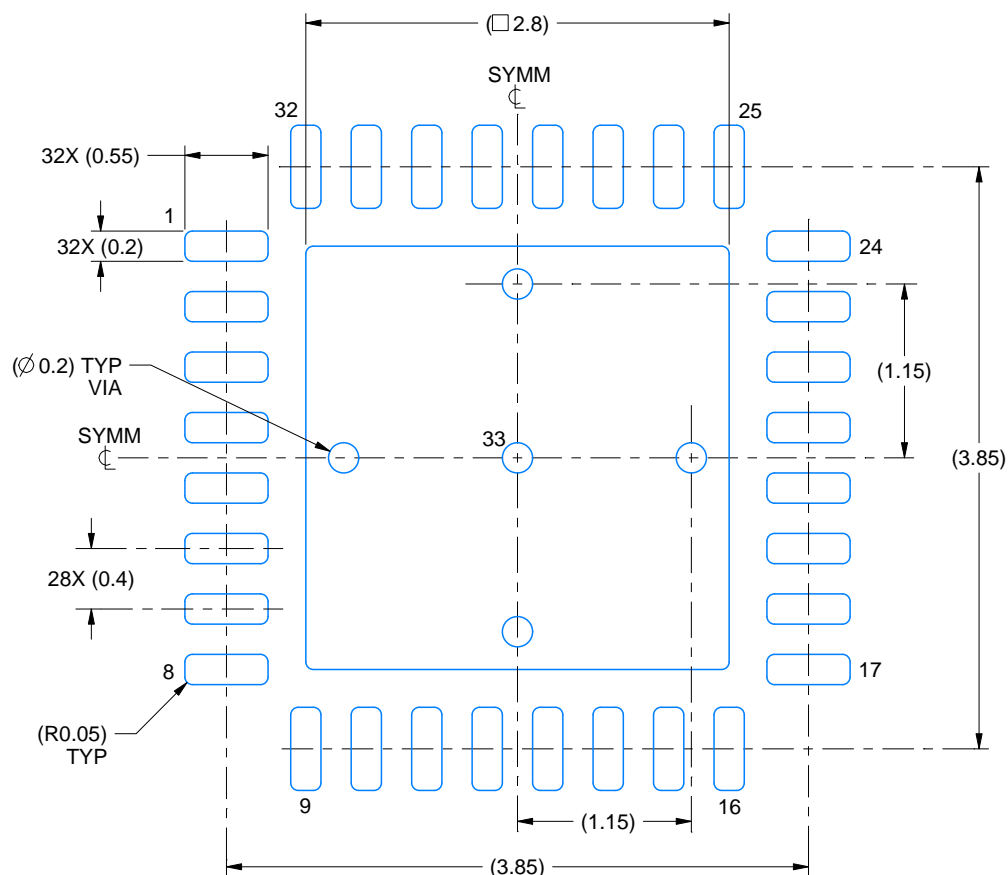
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

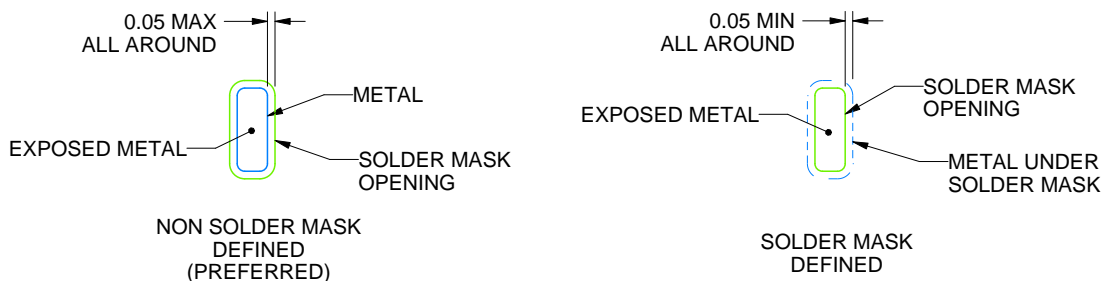
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

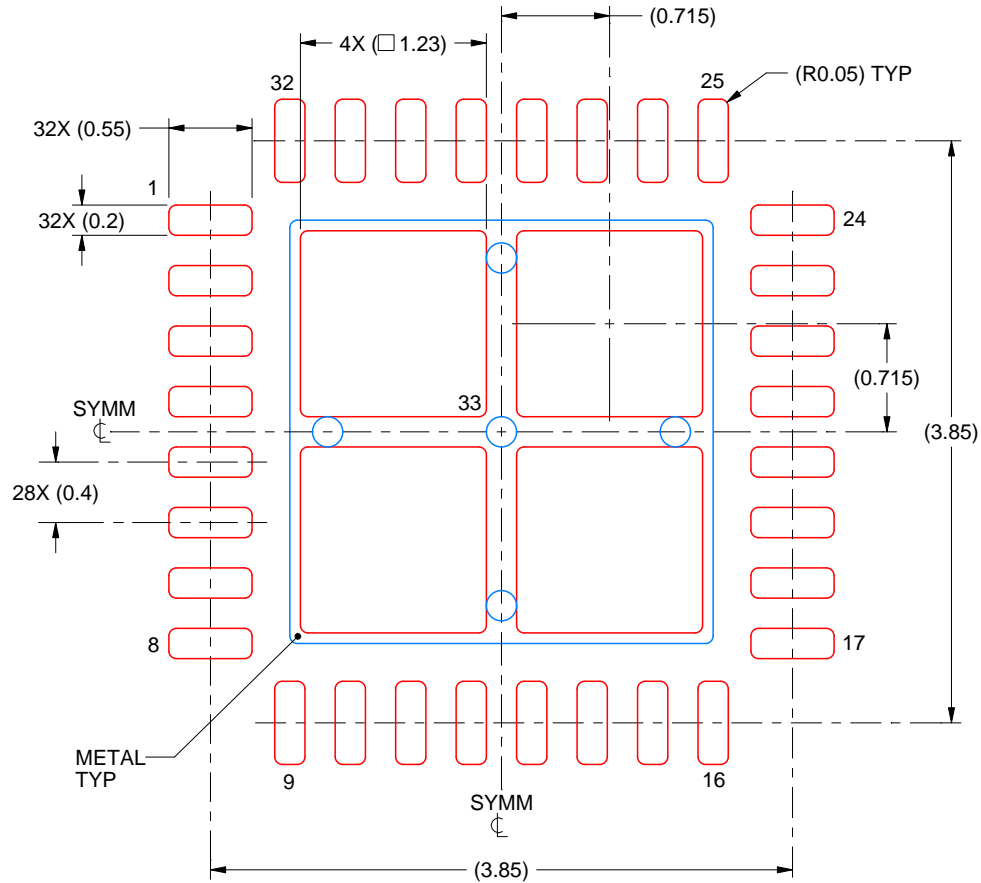
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slue271](http://www.ti.com/lit/slue271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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