



TPS54527 4.5-V to 18-V Input, 5-A Synchronous Step-Down Converter

1 Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 6 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications: 65 mΩ (High Side) and 36 mΩ (Low Side)
- High Efficiency: Less Than 10 μA at Shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Prebiased Soft Start
- 650-kHz Switching Frequency
- Cycle-by-Cycle Overcurrent Limit

2 Applications

- Wide Range of Applications for Low Voltage System
 - Digital TV Power Supply
 - High Definition Blu-ray Disc™ Players
 - Networking Home Terminal
 - Digital Set Top Box (STB)

3 Description

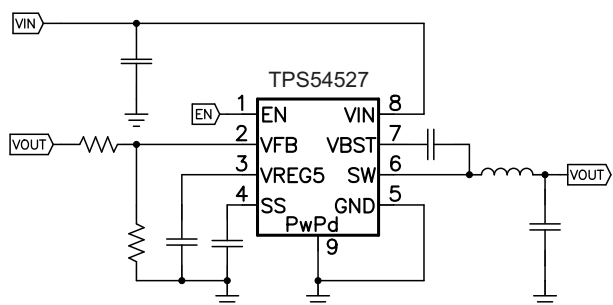
The TPS54527 is an adaptive on-time D-CAP2 mode synchronous buck converter. The TPS54527 enables system designers to complete the suite of various end equipment's power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54527 uses the D-CAP2 mode control which provides a fast transient response with no external compensation components. The TPS54527 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from a 4.5-V to 18-V input. The output voltage can be programmed from 0.76 V to 6 V. The device also features an adjustable soft-start time. The TPS54527 is available in the 8-pin DDA package, and designed to operate from –40°C to 85°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS54527	SO PowerPAD (8)	4.89 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Copyright © 2016, Texas Instruments Incorporated

Load Transient Response

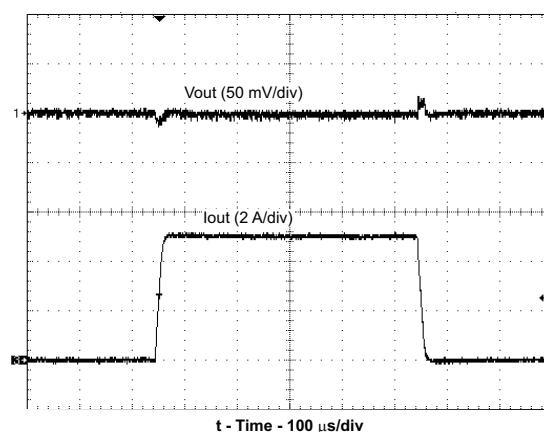


Table of Contents

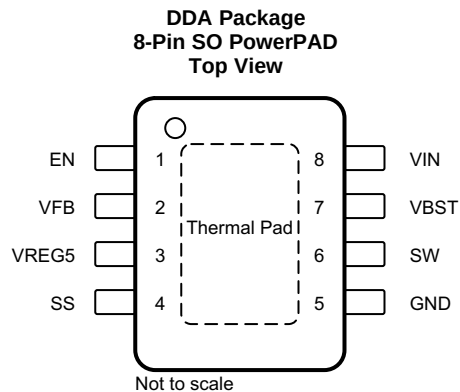
1 Features	1	7.4 Device Functional Modes.....	9
2 Applications	1	8 Application and Implementation	11
3 Description	1	8.1 Application Information.....	11
4 Revision History	2	8.2 Typical Application	11
5 Pin Configuration and Functions	3	9 Power Supply Recommendations	14
6 Specifications	3	10 Layout	14
6.1 Absolute Maximum Ratings	3	10.1 Layout Guidelines	14
6.2 ESD Ratings.....	4	10.2 Layout Example	15
6.3 Recommended Operating Conditions.....	4	10.3 Thermal Consideration.....	15
6.4 Thermal Information	4	11 Device and Documentation Support	16
6.5 Electrical Characteristics.....	5	11.1 Documentation Support	16
6.6 Timing Requirements	5	11.2 Receiving Notification of Documentation Updates	16
6.7 Typical Characteristics	6	11.3 Community Resources.....	16
7 Detailed Description	8	11.4 Trademarks	16
7.1 Overview	8	11.5 Electrostatic Discharge Caution.....	16
7.2 Functional Block Diagram	8	11.6 Glossary	16
7.3 Feature Description.....	8	12 Mechanical, Packaging, and Orderable Information	16

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2012) to Revision D	Page
- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. - Deleted Ordering Information table; see POA at the end of the data sheet.....	 1 1
Changes from Revision B (January 2012) to Revision C	Page
Changed $t_{OFF(MIN)}$ From: 310 ns To: 330 ns.....	5
Changes from Revision A (November 2011) to Revision B	Page
Changed equation 1 denominator from 2 to 6.....	8
Changes from Original (July 2011) to Revision A	Page
Changed pinout drawing to correct pins 5, 6, 7, 8 location	3

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable input control. EN is active high and must be pulled up to enable the device.
VFB	2	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	O	5.5-V power supply output. A capacitor (typically 1 μ F) must be connected to GND. VREG5 is not active when EN is low.
SS	4	I	Soft-start control. An external capacitor must be connected to GND.
GND	5	—	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	O	Switch node connection between high-side NFET and low-side NFET.
VBST	7	O	Supply input for the high-side FET gate drive circuit. Connect 0.1- μ F capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	I	Input voltage supply pin.
Thermal Pad	Back side	—	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	20	V
	VBST	–0.3	26	
	VBST (10-ns transient)	–0.3	28	
	VBST (vs SW)	–0.3	6.5	
	VFB, SS	–0.3	6.5	
	SW	–2	20	
	SW (10-ns transient)	–3	22	
Output voltage	VREG5	–0.3	6.5	V
	GND	–0.3	0.3	
Voltage from GND to thermal pad, V_{diff}		–0.2	0.2	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500
			V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage		4.5	18	V
	Input voltage	VBST	−0.1	24	V
		VBST (10 ns transient)	−0.1	27	
		VBST(vs SW)	−0.1	5.7	
		SS	−0.1	5.7	
		EN	−0.1	18	
		VFB	−0.1	5.5	
		SW	−1.8	18	
		SW (10 ns transient)	−3	21	
		GND	−0.1	0.1	
V_{OUT}	Output voltage	VREG5	−0.1	5.7	V
I_{OUT}	Output current	I_{VREG5}	0	5	mA
T_A	Operating free-air temperature		−40	85	°C
T_J	Operating junction temperature		−40	150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS54527	UNIT
		DDA (SO PowerPAD)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{VIN}	Operating non-switching supply current	V _{IN} current, T _A = 25°C, EN = 5 V, V _{FB} = 0.8 V		900	1400	μA
I _{VINSDN}	Shutdown supply current	V _{IN} current, T _A = 25°C, EN = 0 V		3.6	10	μA
LOGIC THRESHOLD						
V _{ENH}	EN high-level input voltage	EN	1.6			V
V _{ENL}	EN low-level input voltage	EN			0.6	V
VFB VOLTAGE AND DISCHARGE RESISTANCE						
V _{FBTH}	VFB threshold voltage	T _A = 25°C, V _{OUT} = 1.05 V, continuous mode	757	765	773	mV
		T _A = −40°C to 85°C , V _{OUT} = 1.05 V, continuous mode ⁽¹⁾	751	765	779	mV
I _{VFB}	VFB input current	V _{FB} = 0.8 V, T _A = 25°C		0	±0.15	μA
VREG5 OUTPUT						
V _{REG5}	VREG5 output voltage	T _A = 25°C, 6 V < V _{IN} < 18 V, 0 < I _{VREG5} < 5 mA	5.2	5.5	5.7	V
V _{LN5}	Line regulation	6 V < V _{IN} < 18 V, I _{VREG5} = 5 mA			25	mV
V _{LD5}	Load regulation	0 mA < I _{VREG5} < 5 mA			100	mV
I _{VREG5}	Output current	V _{IN} = 6 V, V _{REG5} = 4 V, T _A = 25°C		60		mA
MOSFET						
R _{DS(ON)H}	High side switch resistance	T _A = 25°C, V _{BST} – SW = 5.5 V		65		mΩ
R _{DS(ON)L}	Low side switch resistance	T _A = 25°C		36		mΩ
CURRENT LIMIT						
I _{ocl}	Current limit	L out = 1.5 μH ⁽¹⁾	5.6	6.4	7.9	A
THERMAL SHUTDOWN						
T _{SDN}	Thermal shutdown threshold	Shutdown temperature ⁽¹⁾		165		°C
		Hysteresis ⁽¹⁾		35		
SOFT START						
I _{SSC}	SS charge current	V _{SS} = 1 V	4.2	6	7.8	μA
I _{SSD}	SS discharge current	V _{SS} = 0.5 V	0.1	0.2		mA
UVLO						
UVLO	UVLO threshold	Wake up VREG5 voltage	3.45	3.75	4.05	V
		Hysteresis VREG5 voltage	0.19	0.32	0.45	

(1) Not production tested.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	ON time	$V_{IN} = 12\text{ V}$, $V_{OUT} = 1.05\text{ V}$		150		ns
$t_{OFF(MIN)}$	Minimum OFF time	$T_A = 25^\circ\text{C}$, $V_{FB} = 0.7\text{ V}$		260	330	ns

6.7 Typical Characteristics

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

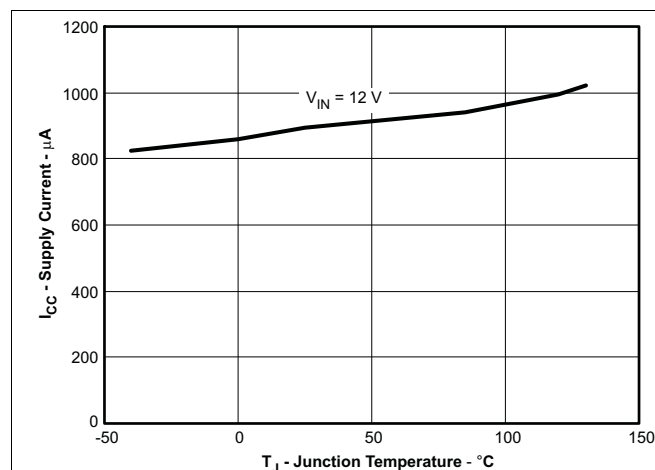


Figure 1. VIN Current vs Junction Temperature

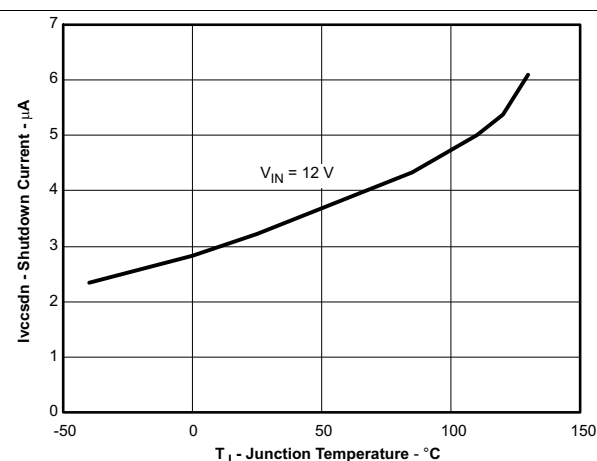


Figure 2. VIN Shutdown Current vs Junction Temperature

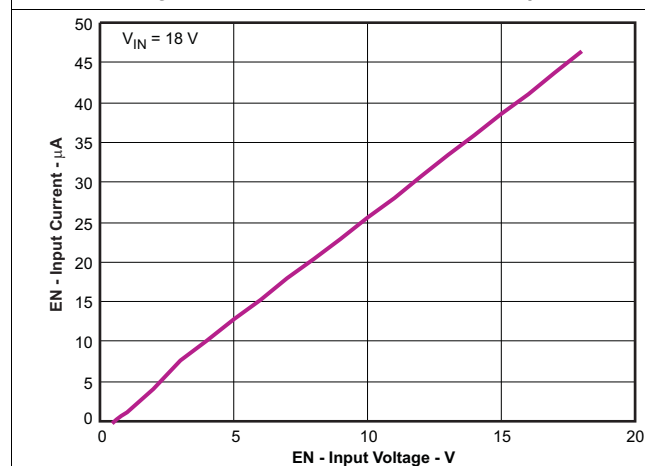


Figure 3. EN Current vs EN Voltage

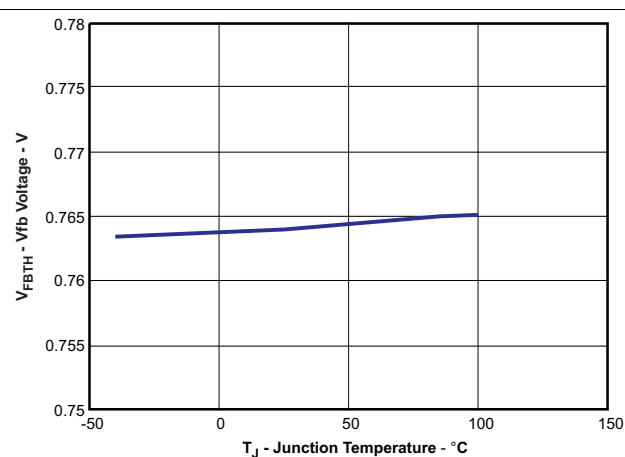


Figure 4. VFB Voltage vs Junction Temperature

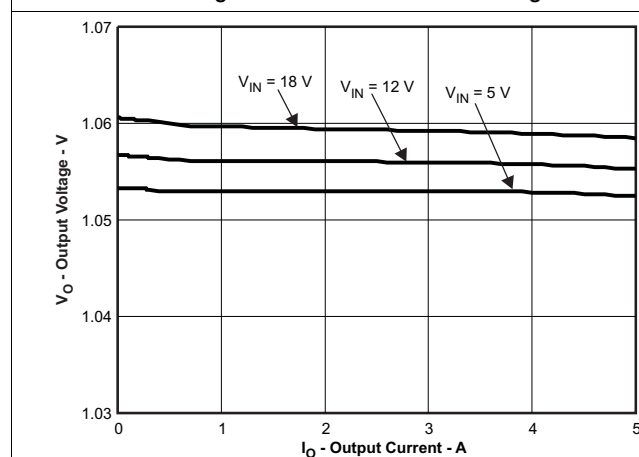


Figure 5. 1.05-V Output Voltage vs Output Current

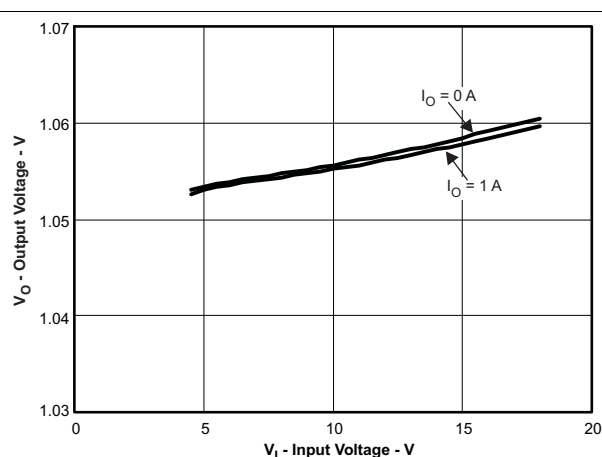


Figure 6. 1.05-V Output Voltage vs Input Voltage

Typical Characteristics (continued)

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

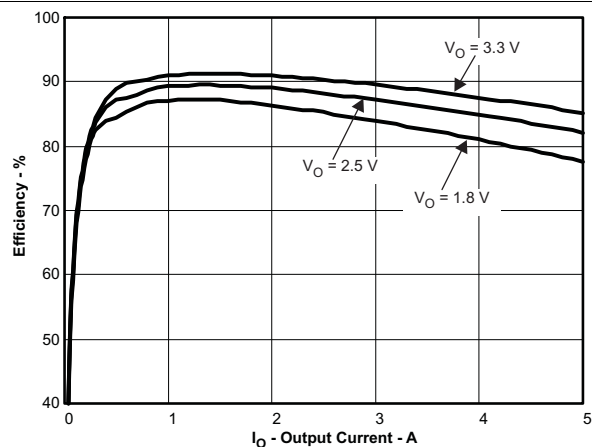


Figure 7. Efficiency vs Output Current

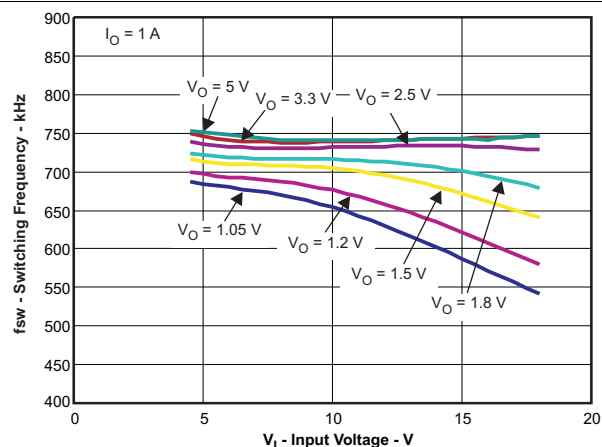


Figure 8. Switching Frequency vs Input Voltage

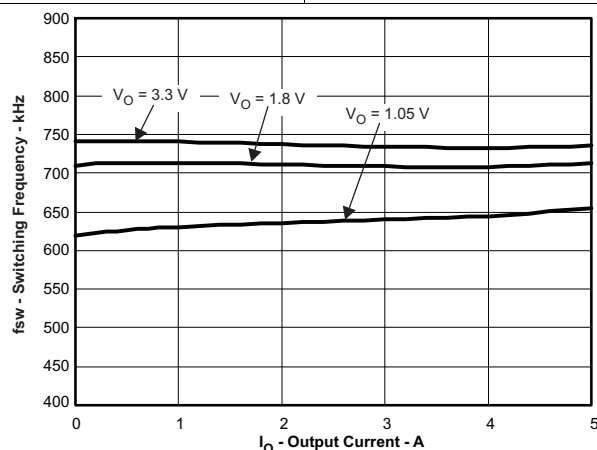


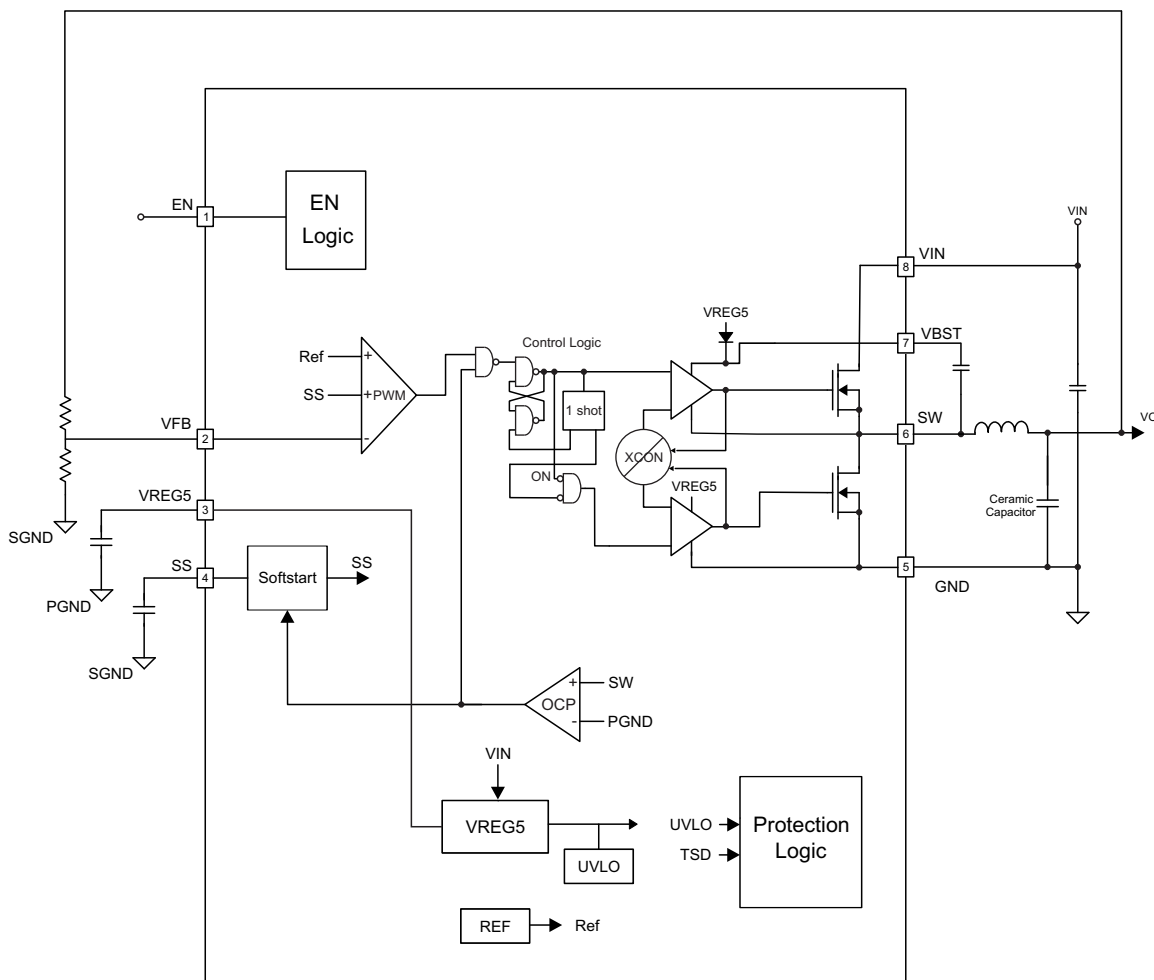
Figure 9. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS54527 is a 5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

7.3.1 Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6-μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 1. VFB voltage is 0.765 V and SS pin source current is 6-μA.

$$t_{ss}(\text{ms}) = \frac{C6(\text{nF}) \times V_{FB} \times 1.1}{I_{SS}(\mu\text{A})} = \frac{C6(\text{nF}) \times 0.765 \times 1.1}{6} \quad (1)$$

Feature Description (continued)

The TPS54527 contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage V_{FB}), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by $1 - D$, where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the output voltage (V_{OUT}) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

7.3.2 Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current (I_{OUT}). The TPS54527 constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The peak current is the average load current plus one half of the peak-to-peak inductor current. The valley current is the average load current minus one half of the peak-to-peak inductor current. Because the valley current is used to detect the overcurrent threshold, the load current is higher than the over-current threshold. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

7.3.3 UVLO Protection

Undervoltage lockout protection (UVLO) monitors the voltage of the VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54527 is shut off. This protection is non-latching.

7.3.4 Thermal Shutdown

TPS54527 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 PWM Operation

The main control loop of the TPS54527 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

Device Functional Modes (continued)

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage (V_{IN}) and the output voltage (V_{OUT}) to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

7.4.2 PWM Frequency and Adaptive On-Time Control

TPS54527 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54527 runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is V_{OUT} / V_{IN} , the frequency is constant.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54327 is designed to provide up to a 2-A output current from an input voltage source ranging from 4.5 V to 18 V. The output voltage is configurable from 0.7 V to 6 V.

8.2 Typical Application

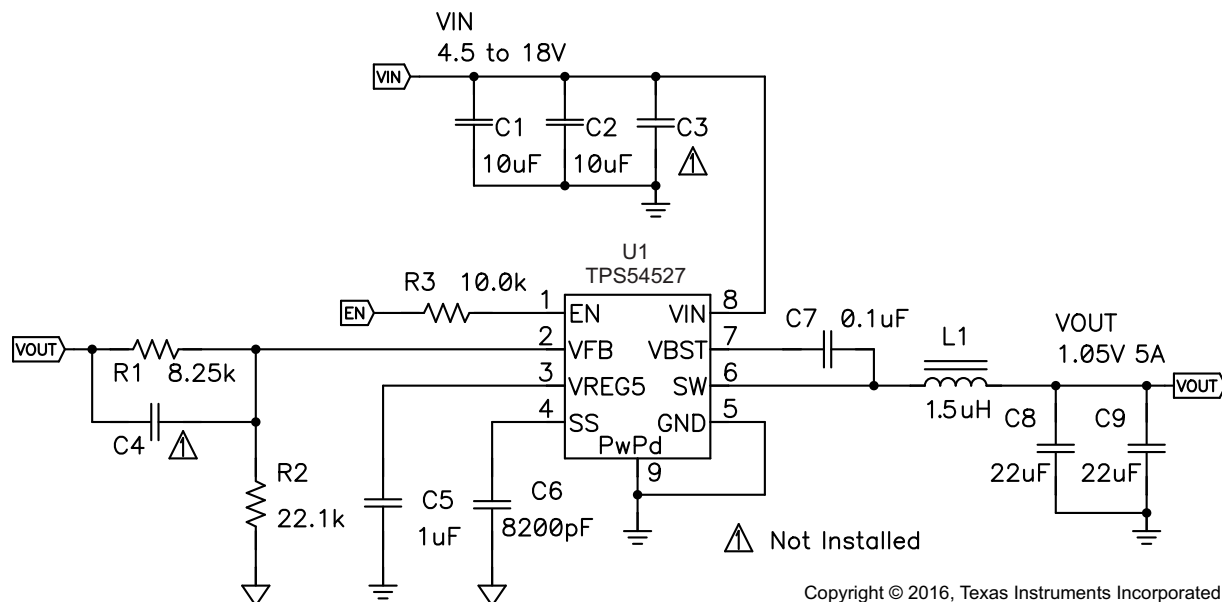


Figure 10. Shows the schematic diagram for this design example.

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage	4.5 V to 18 V
Output voltage	1.05 V
Output current	5 A
Output voltage ripple	20 mV
Input voltage ripple	100 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using a 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate V_{OUT} .

To improve efficiency at very light loads consider using larger value resistors, too high of resistance is more susceptible to noise and voltage errors from the VFB input current is more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2} \right) \quad (2)$$

8.2.2.2 Output Filter Selection

The output filter used with the TPS54527 is an LC circuit. This LC filter has a double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54527. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of [Equation 3](#) is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. TI recommends the values in [Table 2](#) to meet this requirement.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF) ⁽¹⁾	L1 (μH)	C8 + C9 (μF)
1	6.81	22.1	—	1 to 1.5	22 to 68
1.05	8.25	22.1	—	1 to 1.5	22 to 68
1.2	12.7	22.1	—	1 to 1.5	22 to 68
1.5	21.5	22.1	—	1.5	22 to 68
1.8	30.1	22.1	5 to 22	1.5	22 to 68
2.5	49.9	22.1	5 to 22	2.2	22 to 68
3.3	73.2	22.1	5 to 22	2.2	22 to 68
5	124	22.1	5 to 22	3.3	22 to 68

(1) Optional

Because the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using [Equation 4](#), [Equation 5](#), and [Equation 6](#). The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 700 kHz for f_{SW} .

Use 650 kHz for f_{SW} . Chose an inductor that is rated for the peak current of [Equation 5](#) and the RMS current of [Equation 6](#).

$$I_{IPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{Ipeak} = I_O + \frac{I_{IPP}}{2} \quad (5)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{IPP}^2} \quad (6)$$

For this design example, the calculated peak current is 5.51 A and the calculated RMS current is 5.01 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54527 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 µF to 68 µF. Use [Equation 7](#) to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.29 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS54527 requires an input decoupling capacitor and a bulk capacitor is required depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from VIN to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST and SW pins for proper operation. TI recommends using a ceramic capacitor.

8.2.2.5 VREG5 Capacitor Selection

A 1-µF ceramic capacitor must be connected between the VREG5 and GND pins for proper operation. TI recommends using a ceramic capacitor.

8.2.3 Application Curves

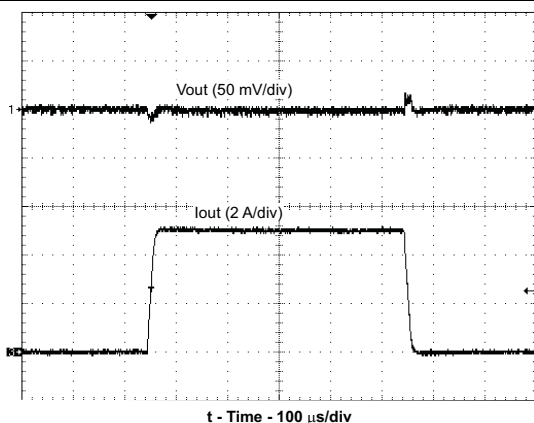


Figure 11. 1.05-V, 50-mA to 2-A Load Transient Response

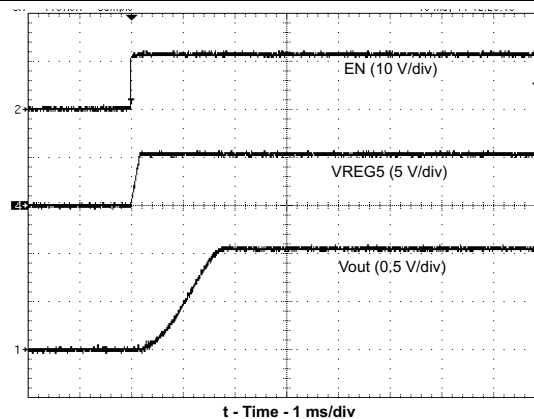
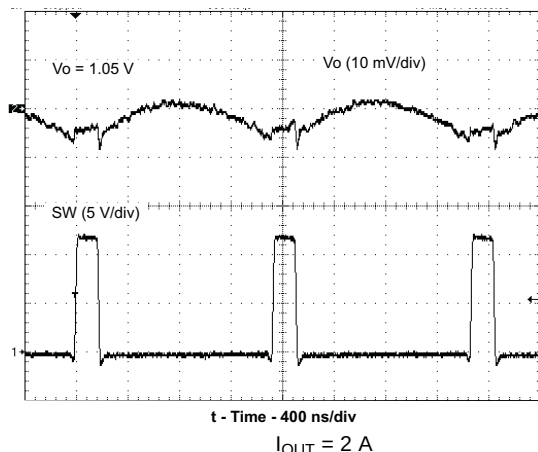
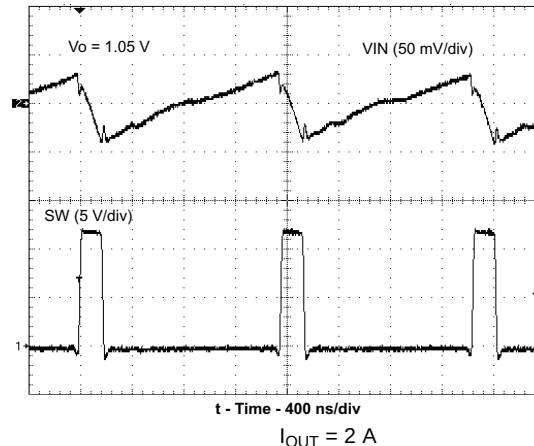


Figure 12. Start-Up Wave Form


Figure 13. Voltage Ripple at Output

Figure 14. Voltage Ripple at Input

9 Power Supply Recommendations

The input voltage range is from 4.5 V to 18 V. The input power supply and the input capacitors must be placed as close to the device as possible to minimize the impedance of the power-supply line.

10 Layout

10.1 Layout Guidelines

1. The TPS54527 can supply large load currents up to 5 A, so heat dissipation may be a concern. The top side area adjacent to the TPS54527 must be filled with ground as much as possible to dissipate heat.
2. The bottom side area directly below the IC must a dedicated ground area. It must be directly connected to the thermal pad of the device using vias as shown. The ground area must be as large as practical. Additional internal layers can be dedicated as ground planes and connected to the vias as well.
3. Keep the input switching current loop as small as possible.
4. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
5. Keep analog and non-switching components away from switching components.
6. Make a single point connection from the signal ground to power ground.
7. Do not allow switching current to flow under the device.
8. Keep the pattern lines for VIN and PGND broad.
9. Exposed pad of device must be connected to PGND with solder.
10. VREG5 capacitor must be placed near the device, and connected PGND.
11. Output capacitor must be connected to a broad pattern of the PGND.
12. Voltage feedback loop must be as short as possible, and preferably with ground shield.
13. Lower resistor of the voltage divider which is connected to the VFB pin must be tied to SGND.
14. Providing sufficient via is required for VIN, SW and PGND connection.
15. PCB pattern for VIN, SW, and PGND must be as broad as possible.
16. VIN capacitor must be placed as near as possible to the device.

10.2 Layout Example

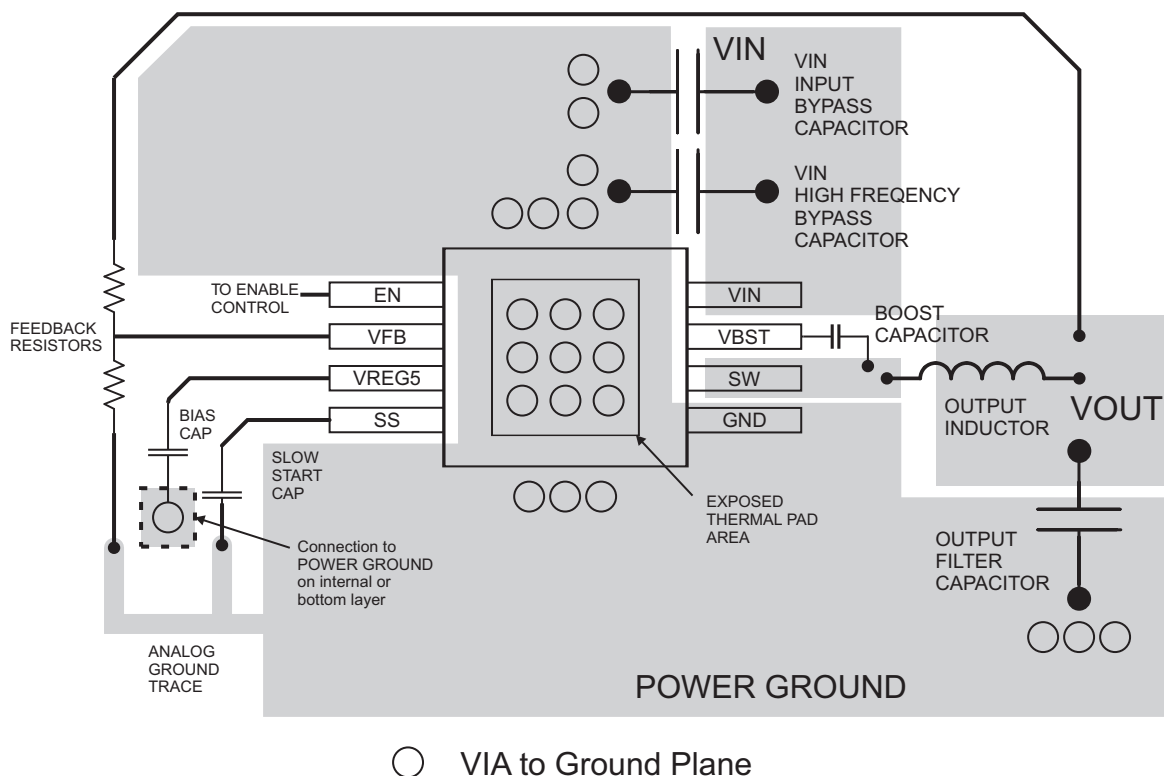


Figure 15. PCB Layout

10.3 Thermal Consideration

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heat sink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heat sink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see [PowerPAD Thermally Enhanced Package](#) and [PowerPAD Made Easy](#).

The exposed thermal pad dimensions for this package are shown in [Figure 16](#).

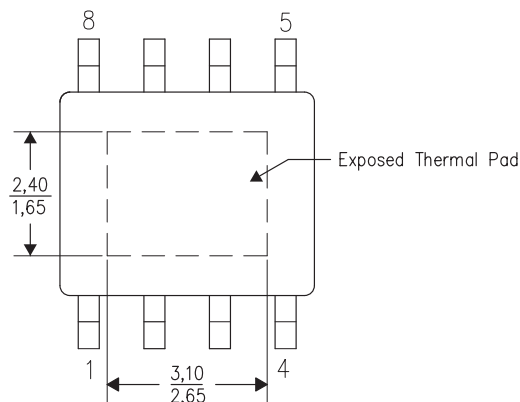


Figure 16. Thermal Pad Dimensions (Top View)

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- [PowerPAD Thermally Enhanced Package](#) (SLMA002)
- [PowerPAD Made Easy](#) (SLMA004)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

D-CAP2, E2E are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54527DDA	Active	Production	SO PowerPAD (DDA) 8	75 BULK	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 85	54527
TPS54527DDA.A	Active	Production	SO PowerPAD (DDA) 8	75 BULK	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54527
TPS54527DDA.B	Active	Production	SO PowerPAD (DDA) 8	75 BULK	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54527
TPS54527DDAR	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU SN	Level-2-260C-1 YEAR	-40 to 85	54527
TPS54527DDAR.A	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54527
TPS54527DDAR.B	Active	Production	SO PowerPAD (DDA) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	54527

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

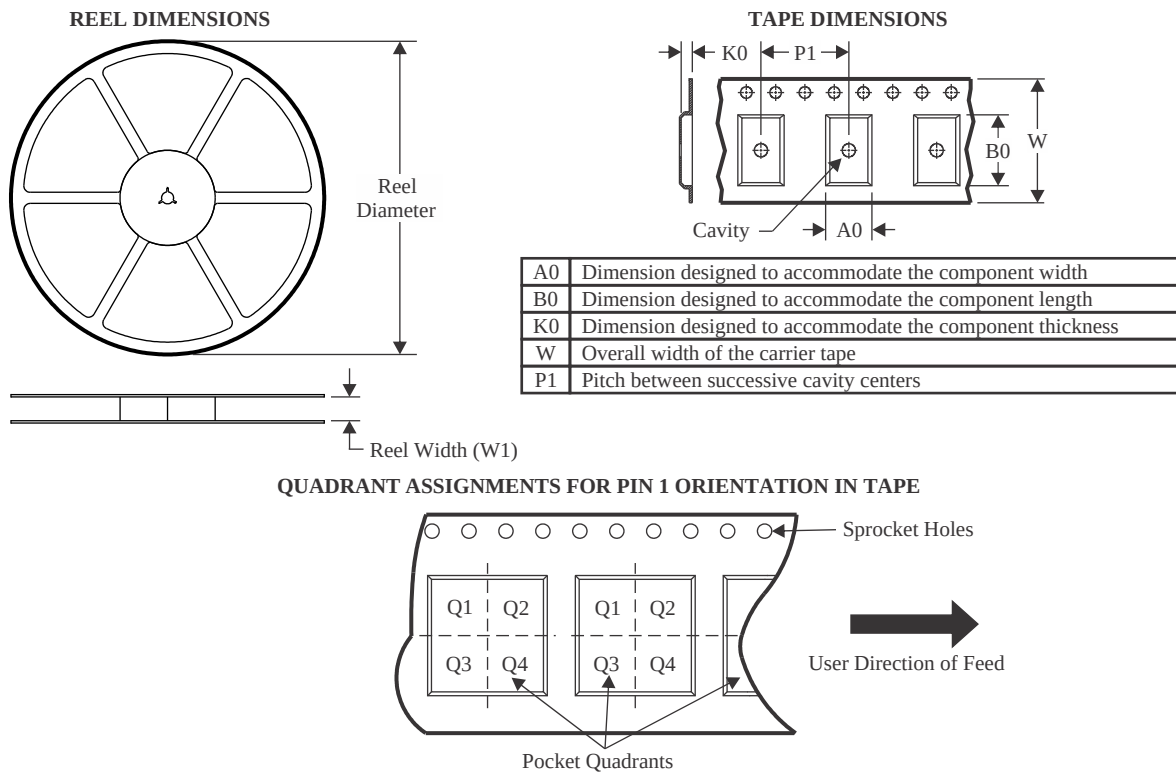
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

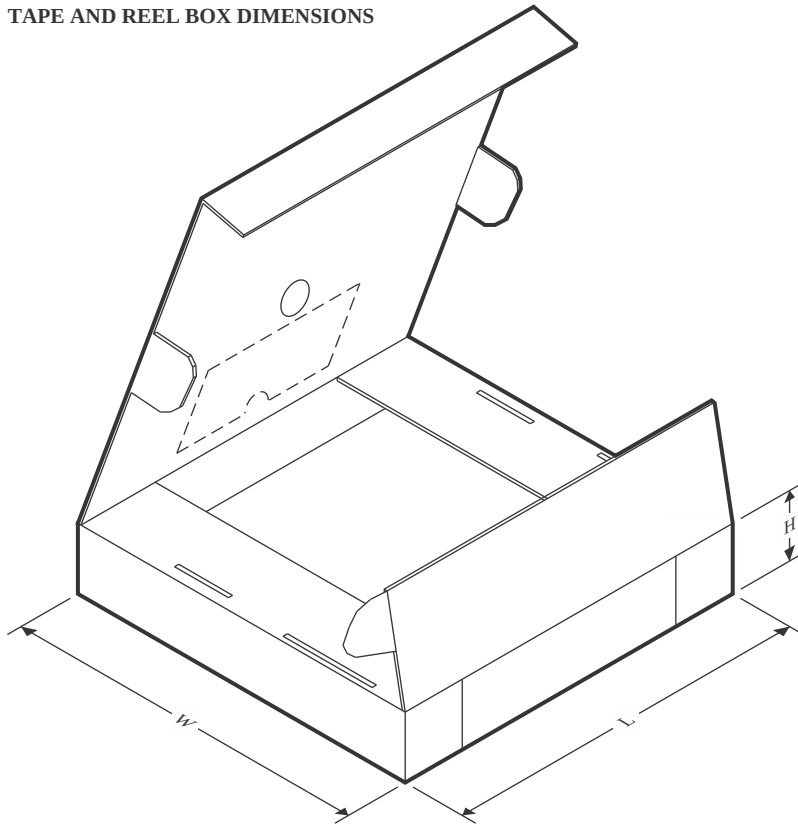
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54527DDAR	SO PowerPAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

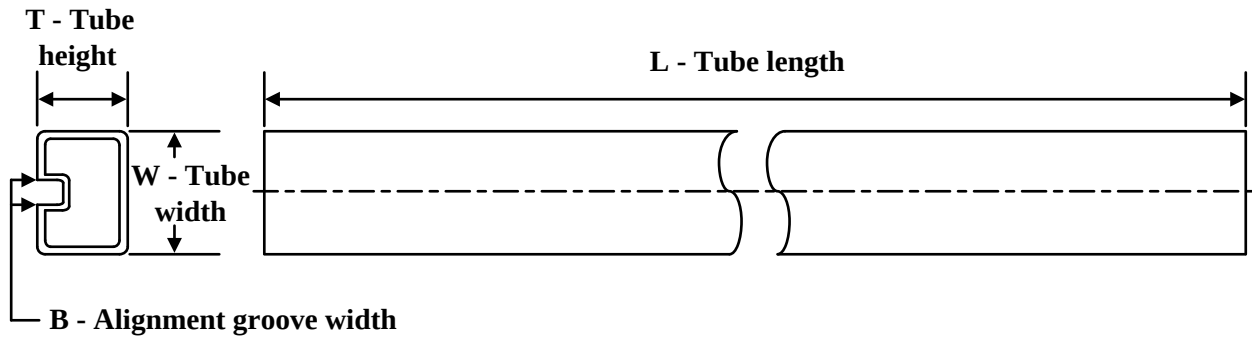
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

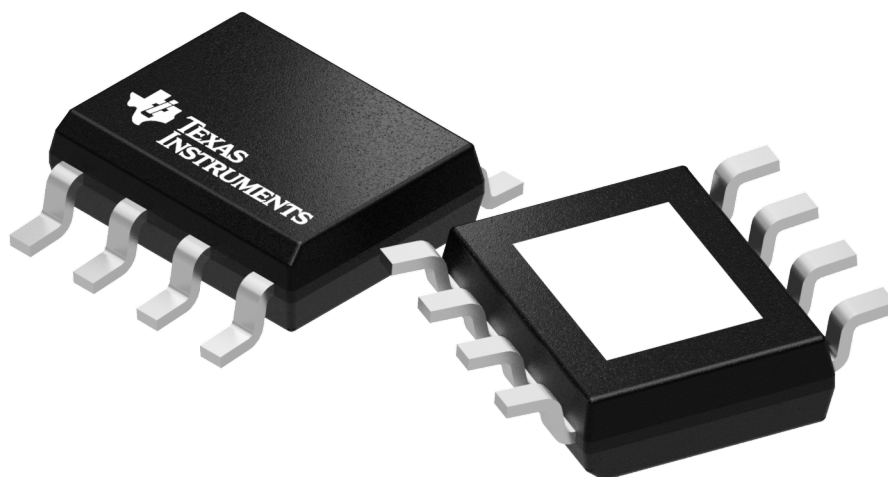
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54527DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE



*All dimensions are nominal

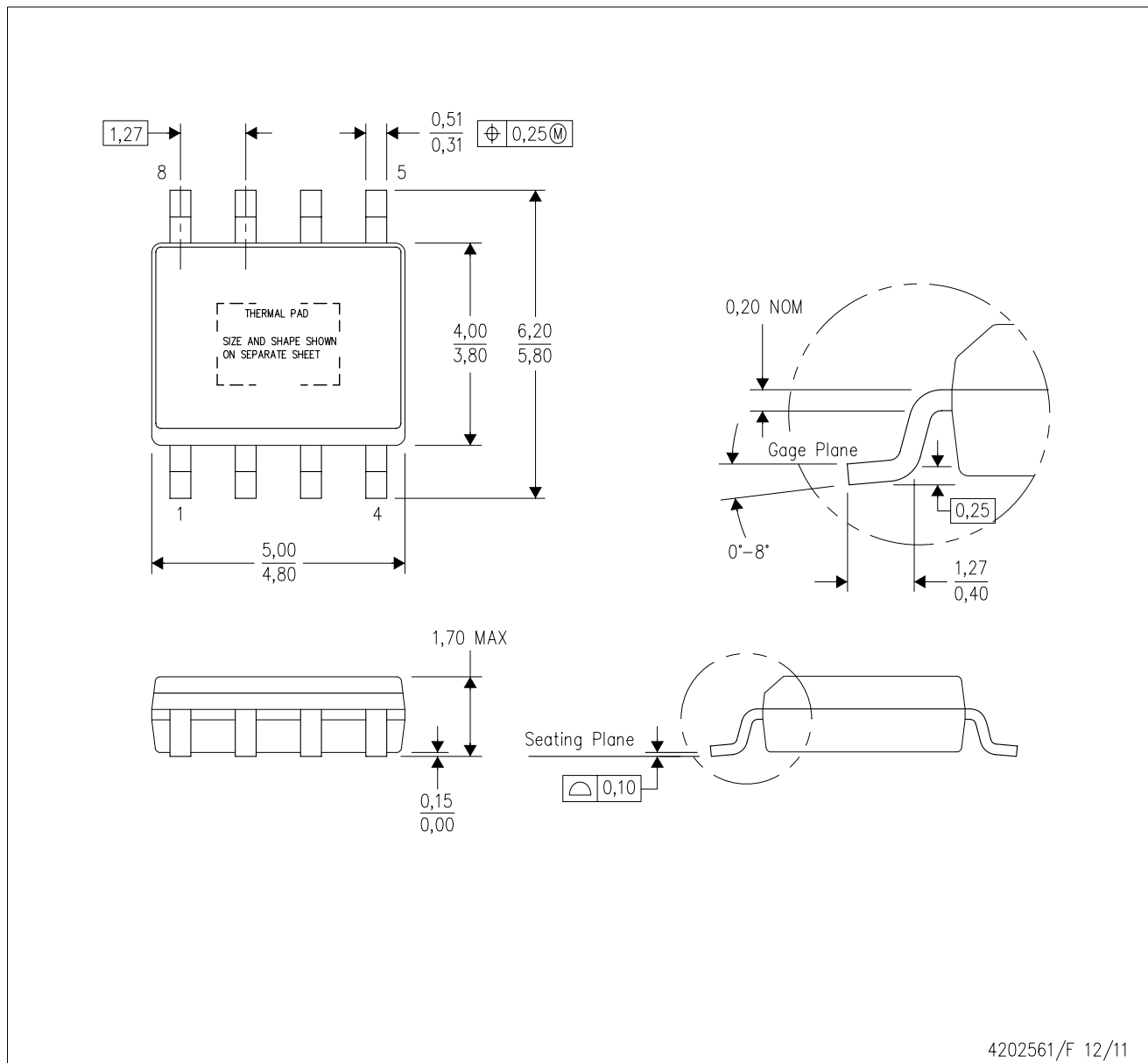
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS54527DDA	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS54527DDA.A	DDA	HSOIC	8	75	517	7.87	635	4.25
TPS54527DDA.B	DDA	HSOIC	8	75	517	7.87	635	4.25



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

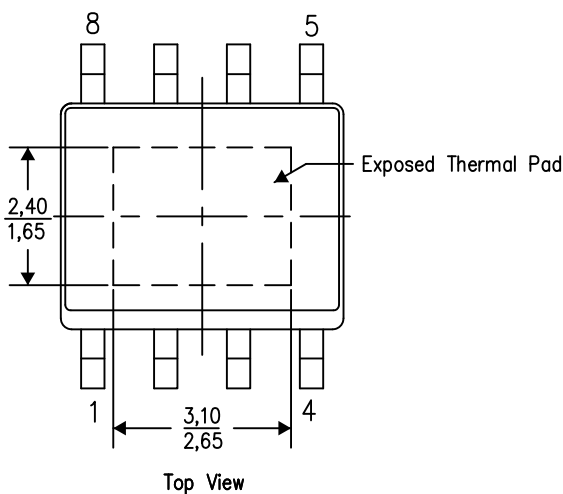
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

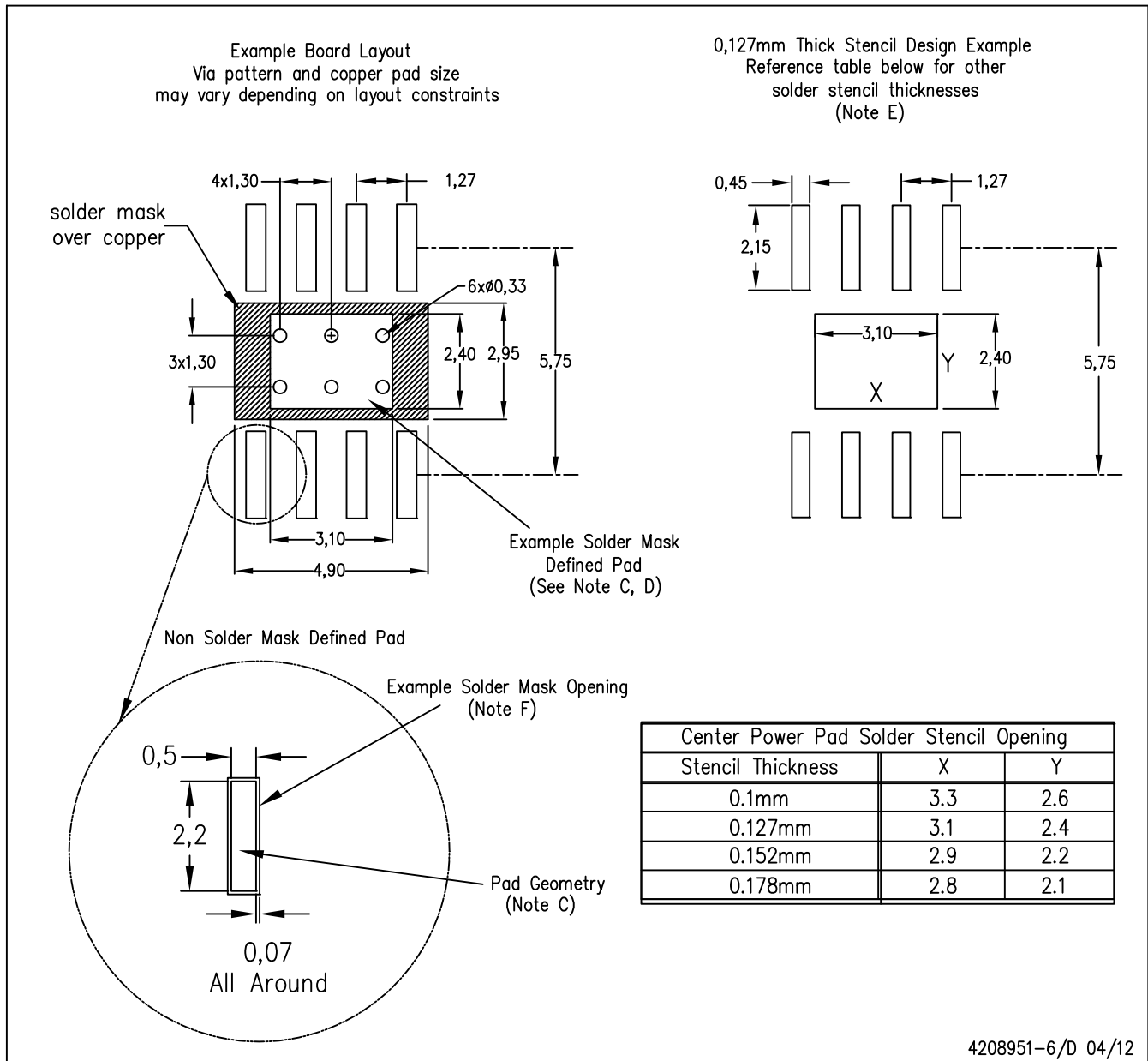
4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

PowerPAD™ SOIC - 1.7 mm max height

Technical drawing of a microelectronic package showing top, side, and detail views with dimensions and feature callouts.

Top View:

- Overall width: 6.2 TYP, 5.8
- Overall height: 5.0, 4.8, NOTE 3
- Pin 1 ID Area (hatched)
- Pin 1 location: 1
- Pin 2 location: 8
- Pin 3 location: 5
- Pin 4 location: 4
- Pin 5 location: 5
- Pin 6 location: 8
- Pin 7 location: 5
- Pin 8 location: 4
- Pin 9 location: 1
- Pin 10 location: 8
- Pin 11 location: 5
- Pin 12 location: 4
- Pin 13 location: 1
- Pin 14 location: 8
- Pin 15 location: 5
- Pin 16 location: 4
- Pin 17 location: 1
- Pin 18 location: 8
- Pin 19 location: 5
- Pin 20 location: 4
- Pin 21 location: 1
- Pin 22 location: 8
- Pin 23 location: 5
- Pin 24 location: 4
- Pin 25 location: 1
- Pin 26 location: 8
- Pin 27 location: 5
- Pin 28 location: 4
- Pin 29 location: 1
- Pin 30 location: 8
- Pin 31 location: 5
- Pin 32 location: 4
- Pin 33 location: 1
- Pin 34 location: 8
- Pin 35 location: 5
- Pin 36 location: 4
- Pin 37 location: 1
- Pin 38 location: 8
- Pin 39 location: 5
- Pin 40 location: 4
- Pin 41 location: 1
- Pin 42 location: 8
- Pin 43 location: 5
- Pin 44 location: 4
- Pin 45 location: 1
- Pin 46 location: 8
- Pin 47 location: 5
- Pin 48 location: 4
- Pin 49 location: 1
- Pin 50 location: 8
- Pin 51 location: 5
- Pin 52 location: 4
- Pin 53 location: 1
- Pin 54 location: 8
- Pin 55 location: 5
- Pin 56 location: 4
- Pin 57 location: 1
- Pin 58 location: 8
- Pin 59 location: 5
- Pin 60 location: 4
- Pin 61 location: 1
- Pin 62 location: 8
- Pin 63 location: 5
- Pin 64 location: 4
- Pin 65 location: 1
- Pin 66 location: 8
- Pin 67 location: 5
- Pin 68 location: 4
- Pin 69 location: 1
- Pin 70 location: 8
- Pin 71 location: 5
- Pin 72 location: 4
- Pin 73 location: 1
- Pin 74 location: 8
- Pin 75 location: 5
- Pin 76 location: 4
- Pin 77 location: 1
- Pin 78 location: 8
- Pin 79 location: 5
- Pin 80 location: 4
- Pin 81 location: 1
- Pin 82 location: 8
- Pin 83 location: 5
- Pin 84 location: 4
- Pin 85 location: 1
- Pin 86 location: 8
- Pin 87 location: 5
- Pin 88 location: 4
- Pin 89 location: 1
- Pin 90 location: 8
- Pin 91 location: 5
- Pin 92 location: 4
- Pin 93 location: 1
- Pin 94 location: 8
- Pin 95 location: 5
- Pin 96 location: 4
- Pin 97 location: 1
- Pin 98 location: 8
- Pin 99 location: 5
- Pin 100 location: 4
- Pin 101 location: 1
- Pin 102 location: 8
- Pin 103 location: 5
- Pin 104 location: 4
- Pin 105 location: 1
- Pin 106 location: 8
- Pin 107 location: 5
- Pin 108 location: 4
- Pin 109 location: 1
- Pin 110 location: 8
- Pin 111 location: 5
- Pin 112 location: 4
- Pin 113 location: 1
- Pin 114 location: 8
- Pin 115 location: 5
- Pin 116 location: 4
- Pin 117 location: 1
- Pin 118 location: 8
- Pin 119 location: 5
- Pin 120 location: 4
- Pin 121 location: 1
- Pin 122 location: 8
- Pin 123 location: 5
- Pin 124 location: 4
- Pin 125 location: 1
- Pin 126 location: 8
- Pin 127 location: 5
- Pin 128 location: 4
- Pin 129 location: 1
- Pin 130 location: 8
- Pin 131 location: 5
- Pin 132 location: 4
- Pin 133 location: 1
- Pin 134 location: 8
- Pin 135 location: 5
- Pin 136 location: 4
- Pin 137 location: 1
- Pin 138 location: 8
- Pin 139 location: 5
- Pin 140 location: 4
- Pin 141 location: 1
- Pin 142 location: 8
- Pin 143 location: 5
- Pin 144 location: 4
- Pin 145 location: 1
- Pin 146 location: 8
- Pin 147 location: 5
- Pin 148 location: 4
- Pin 149 location: 1
- Pin 150 location: 8
- Pin 151 location: 5
- Pin 152 location: 4
- Pin 153 location: 1
- Pin 154 location: 8
- Pin 155 location: 5
- Pin 156 location: 4
- Pin 157 location: 1
- Pin 158 location: 8
- Pin 159 location: 5
- Pin 160 location: 4
- Pin 161 location: 1
- Pin 162 location: 8
- Pin 163 location: 5
- Pin 164 location: 4
- Pin 165 location: 1
- Pin 166 location: 8
- Pin 167 location: 5
- Pin 168 location: 4
- Pin 169 location: 1
- Pin 170 location: 8
- Pin 171 location: 5
- Pin 172 location: 4
- Pin 173 location: 1
- Pin 174 location: 8
- Pin 175 location: 5
- Pin 176 location: 4
- Pin 177 location: 1
- Pin 178 location: 8
- Pin 179 location: 5
- Pin 180 location: 4
- Pin 181 location: 1
- Pin 182 location: 8
- Pin 183 location: 5
- Pin 184 location: 4
- Pin 185 location: 1
- Pin 186 location: 8
- Pin 187 location: 5
- Pin 188 location: 4
- Pin 189 location: 1
- Pin 190 location: 8
- Pin 191 location: 5
- Pin 192 location: 4
- Pin 193 location: 1
- Pin 194 location: 8
- Pin 195 location: 5
- Pin 196 location: 4
- Pin 197 location: 1
- Pin 198 location: 8
- Pin 199 location: 5
- Pin 200 location: 4
- Pin 201 location: 1
- Pin 202 location: 8
- Pin 203 location: 5
- Pin 204 location: 4
- Pin 205 location: 1
- Pin 206 location: 8
- Pin 207 location: 5
- Pin 208 location: 4
- Pin 209 location: 1
- Pin 210 location: 8
- Pin 211 location: 5
- Pin 212 location: 4
- Pin 213 location: 1
- Pin 214 location: 8
- Pin 215 location: 5
- Pin 216 location: 4
- Pin 217 location: 1
- Pin 218 location: 8
- Pin 219 location: 5
- Pin 220 location: 4
- Pin 221 location: 1
- Pin 222 location: 8
- Pin 223 location: 5
- Pin 224 location: 4
- Pin 225 location: 1
- Pin 226 location: 8
- Pin 227 location: 5
- Pin 228 location: 4
- Pin 229 location: 1
- Pin 230 location: 8
- Pin 231 location: 5
- Pin 232 location: 4
- Pin 233 location: 1
- Pin 234 location: 8
- Pin 235 location: 5
- Pin 236 location: 4
- Pin 237 location: 1
- Pin 238 location: 8
- Pin 239 location: 5
- Pin 240 location: 4
- Pin 241 location: 1
- Pin 242 location: 8
- Pin 243 location: 5
- Pin 244 location: 4
- Pin 245 location: 1
- Pin 246 location: 8
- Pin 247 location: 5
- Pin 248 location: 4
- Pin 249 location: 1
- Pin 250 location: 8
- Pin 251 location: 5
- Pin 252 location: 4
- Pin 253 location: 1
- Pin 254 location: 8
- Pin 255 location: 5
- Pin 256 location: 4
- Pin 257 location: 1
- Pin 258 location: 8
- Pin 259 location: 5
- Pin 260 location: 4
- Pin 261 location: 1
- Pin 262 location: 8
- Pin 263 location: 5
- Pin 264 location: 4
- Pin 265 location: 1
- Pin 266 location: 8
- Pin 267 location: 5
- Pin 268 location: 4
- Pin 269 location: 1
- Pin 270 location: 8
- Pin 271 location: 5
- Pin 272 location: 4</

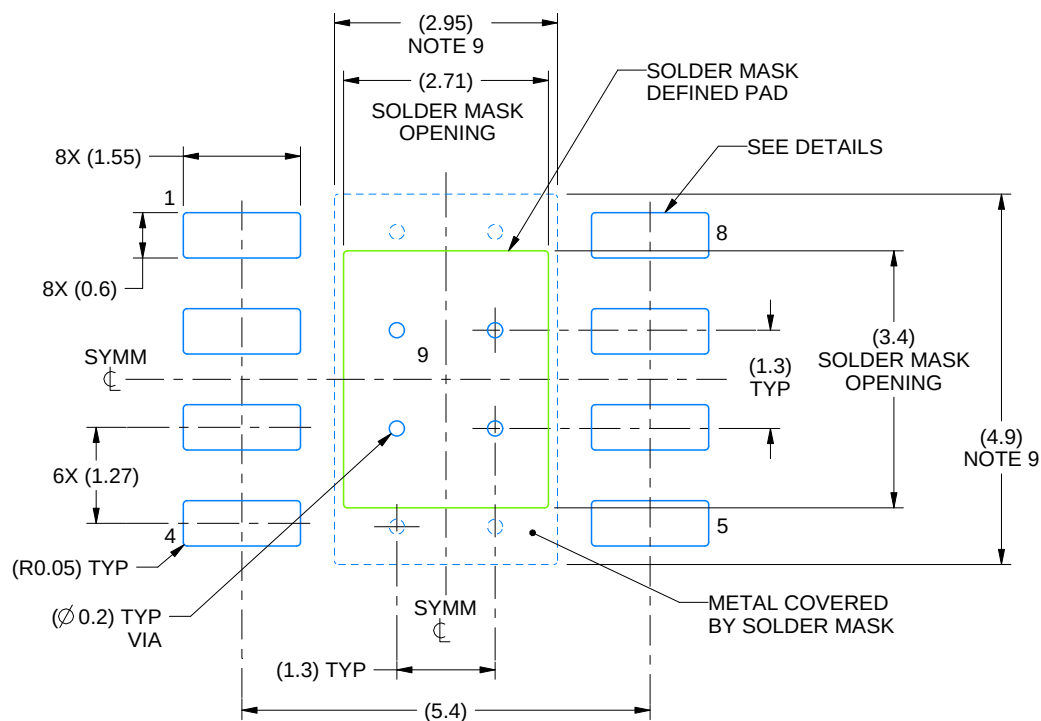
PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

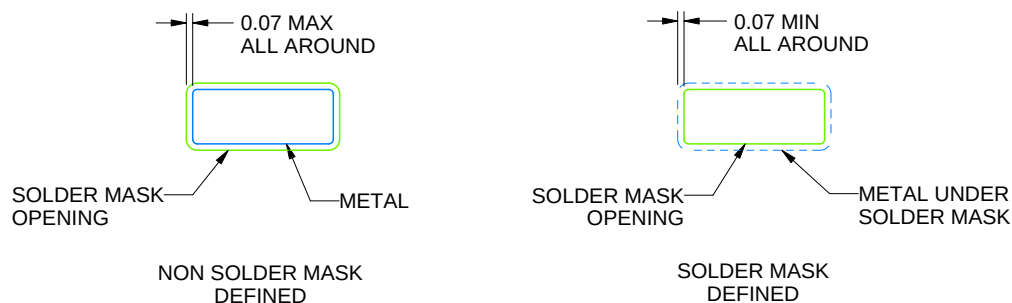
DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-8

4214849/B 09/2025

NOTES: (continued)

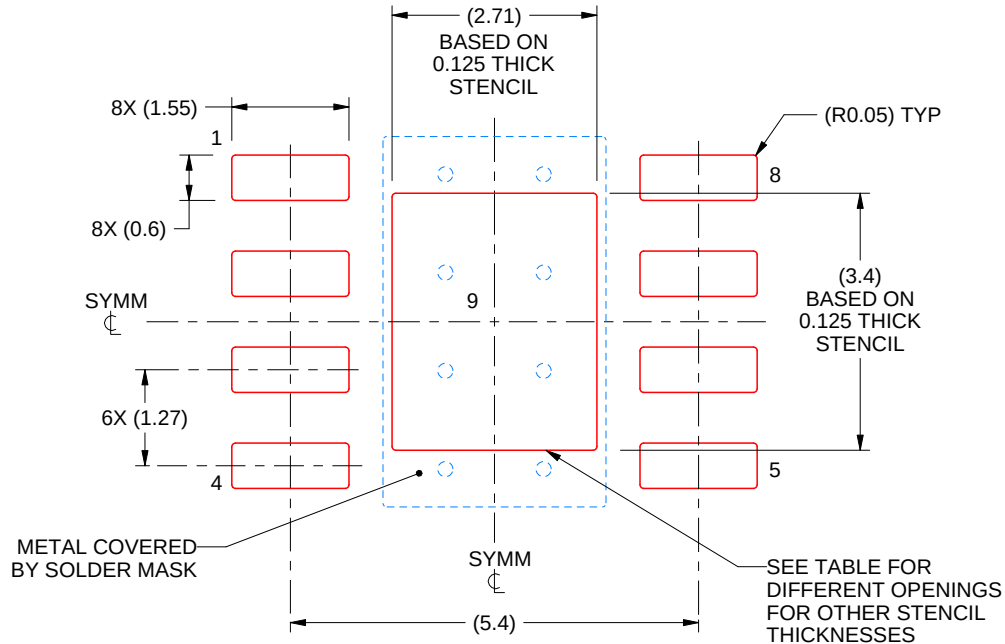
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DDA0008B

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.03 X 3.80
0.125	2.71 X 3.40 (SHOWN)
0.150	2.47 X 3.10
0.175	2.29 X 2.87

4214849/B 09/2025

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025