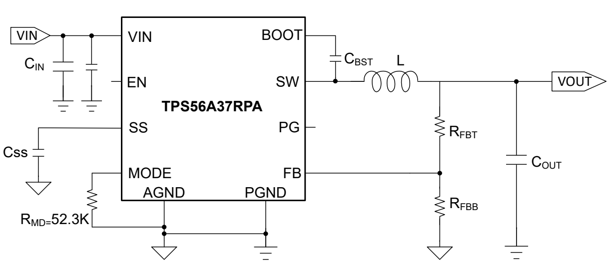
TPS56A37 4.5V to 28V Input, 10A, Synchronous Buck Converter

1 Features

- 4.5V to 28V input voltage range
- 0.6V to 13V output voltage range
- Supports 10A continuous output current
- Integrated 19.4mΩ and 8.5mΩ MOSFETs
- 0.6V ±1% reference voltage at 25°C
- 45uA low quiescent current
- D-CAP3™ control mode for fast transient response
- Eco-mode (auto-skip mode) for high light-load efficiency
- Fixed 500kHz switching frequency
- Cycle by cycle over current limit
- Adjustable soft-start time with default 1.8ms
- Built-in output discharge function
- Power-good indicator to monitor output voltage
- Supports up to 98% duty operation
- Non-latched protections for UV, OV, OT, and UVLO
- –40°C to +150°C operating junction temperature
- Small 10-pin 3.0mm × 3.0mm HotRod™ QFN package
- Pin-to-pin compatible with 6A TPS56637 and 8A TPS56837

2 Applications

- Industrial PC, EPOS, factory automation and control
- Multifunction printers, video conference system
- Monitors, TV, speakers, PC and notebooks, portable electronics
- General purposes for 12V,19V, 24V power-bus supply



Simplified Schematic

3 Description

The TPS56A37 is a high-efficiency, easy-to-use, synchronous buck converter with a wide input voltage range of 4.5V to 28V. The device supports up to 10A continuous output current at output voltages between 0.6V and 13V.

The TPS56A37 uses D-CAP3 control mode to provide fast transient response, good line and load regulation, no requirement for external compensation, and supports low equivalent series resistance (ESR) output capacitors like MLCC.

The TPS56A37 operates at Eco-mode to attain high efficiency at light load with fixed 500kHz switching frequency. The TPS56A37 has adjustable soft-start time by connecting the SS capacitor and with default 1.8ms with the SS pin floating.

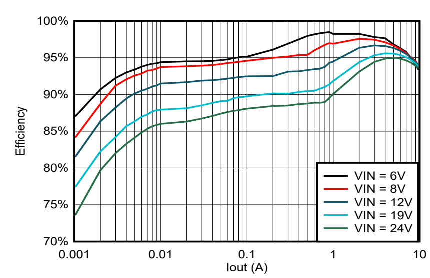
The TPS56A37 provides complete non-latched OV (overvoltage), UV (undervoltage), OC (overcurrent), OT (overtemperature), and UVLO (undervoltage lockout) protections combined with power-good indicator and output discharge function features.

The TPS56A37 is available in a 10-pin, 3.0mm × 3.0mm HotRod QFN package, and the junction temperature is specified from –40°C to 150°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS56A37	RPA (VQFN-HR, 10)	3.00mm × 3.00mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency, Vout = 5V, Fsw = 500kHz

Table of Contents

4 Pin Configuration and Functions

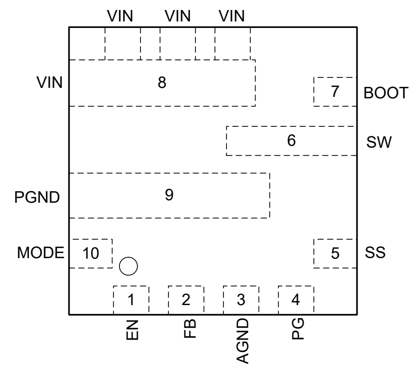


Figure 4-1. RPA Package, 10-Pin VQFN-HR (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	1	I	Enable input control. Driving EN high or leaving this pin floating enables the converter. A resistor divider between this pin, VIN and AGND can be used to implement an external UVLO.
FB	2	I	Output feedback. Connect FB to the output voltage with a feedback resistor divider.
AGND	3	G	Ground of internal analog circuitry. Connect AGND to PGND plane at a single point.
PG	4	O	Open drain power-good indicator, this pin is asserted low if output voltage is out of PG threshold due to overvoltage, undervoltage, thermal shutdown, EN shutdown, or during soft start.
SS	5	O	Soft-start time selection pin. Connecting an external capacitor to AGND to set the soft-start time and if no external capacitor is connected, the soft-start time is 1.8ms by default.
SW	6	O	Switching node terminal. Connect the output inductor to this pin with wide and short tracks.
BOOT	7	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect a 0.1µF bootstrap capacitor between BOOT and SW.
VIN	8	P	Input voltage supply pin. Drain terminal of high-side MOSFET. Connect the input decoupling capacitors between VIN and PGND.
PGND	9	G	Power GND terminal. Source terminal of low-side MOSFET.
MODE	10	I	Connect this pin with a 52.3K resistor to AGND.

(1) I = Input, P = Power, G = Ground, O = Output.

5 Specifications

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	32	V
	BOOT	–0.3	SW + 6	V
	BOOT-SW	–0.3	6	V
	EN, FB, MODE	–0.3	6	V
	PGND, AGND	–0.3	0.3	V
Output voltage	SW	–2	32	V
	SW (<10ns transient)	–5	35	V
	PG, SS	–0.3	6	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).[1]

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	4.5		28	V
	BOOT	–0.1		SW + 5.5	
	BOOT-SW	–0.1		5.5	V
	EN, FB, SS, MODE	–0.1		5.5	V
	PGND, AGND	–0.1		0.1	V
Output voltage	SW	–1		28	V
	PG	–0.1		5.5	V
Operating junction temperature, T_J		–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS56A37 QFN HotRod 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC)[2]	68.1	°C/W
Eff $R_{\theta JA}$	Effective junction-to-ambient thermal resistance (4-layer TI EVM)	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) This junction-to-ambient thermal resistance (JEDEC) is based on JEDEC standard EVM without GND thermal vias.

5.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 24V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5V to 28V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current, Operating [1]	T_J = 25°C, V_{EN} = 5V, V_{FB} = 0.65V, non-switching		45		µA
I_{SHDNN}	Shutdown supply current	T_J = 25°C, V_{EN} = 0V		3		µA
UVLO						
UVLO	V_{IN} undervoltage lockout	Wake up V_{IN} voltage	4.0	4.2	4.4	V
		Shutdown V_{IN} voltage	3.5	3.65	3.8	V
		Hysteresis V_{IN} voltage		550		mV
ENABLE(EN PIN)						
I_{EN_PULLUP}	EN pullup current	V_{EN} = 1.1V		1		µA
I_{EN_HYS}	Hysteresis current	V_{EN} = 1.3V		3		µA
V_{EN_ON}	Enable threshold	EN rising		1.18	1.26	V
V_{EN_OFF}		EN falling	1	1.07		V
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage	V_{OUT} = 5V, continuous mode operation, T_J = 25°C	0.594	0.6	0.606	V
		V_{OUT} = 5V, continuous mode operation, T_J = –40°C to 150°C	0.591	0.6	0.609	V
MOSFET						
R_{dson_HS}	High-side MOSFET on-resistance	T_J = 25°C, V_{BST} – V_{SW} = 5V		19.4		mΩ
R_{dson_LS}	Low-side MOSFET on-resistance	T_J = 25°C		8.5		mΩ
CURRENT LIMIT						
I_{LS_OCL}	Low-side MOSFET valley current limit		10	12	13.8	A
I_{HS_OCL}	High-side MOSFET peak current limit		12.75	15	17.25	A

5.5 Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that do not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 24V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5V to 28V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{NOCL}	Low-side MOSFET negative current limit		2.5			A
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	V_{IN} = 24V, V_{OUT} = 5V, continuous mode operation		500		kHz
$t_{ON(MIN)}$	Minimum on time(2)			50		ns
$t_{OFF(MIN)}$	Minimum off time(2)	T_J = 25°C		150		ns
SOFT START						
t_{SS}	Internal soft-start time			1.8		ms
I_{SS}	Soft-start charging current			6		uA
POWER GOOD						
V_{PGTH}	PG lower threshold - falling	% of V_{FB}		85%		
	PG lower threshold - rising	% of V_{FB}		90%		
	PG upper threshold - falling	% of V_{FB}		110%		
	PG upper threshold - rising	% of V_{FB}		115%		
I_{PGSINK}	PG sink current	V_{FB} = 0.5V, V_{PG} = 0.4V	10			mA
t_{PG_DLY}	PG delay	PG from low-to-high		64		us
		PG from high-to-low		32		us
V_{OVP}	Output OVP threshold	OVP detect		125%		
t_{OVP_DEG}	OVP propagation deglitch	T_J = 25°C		32		us
V_{UVP}	Output UVP threshold	Hiccup detect		65%		
t_{UVP_WAIT}	UV protection hiccup wait time			256		us
t_{UVP_HICCUP}	UV protection hiccup time before recovery			10.5 × t_{SS}		s
THERMAL SHUTDOWN						
Thermal shutdown threshold(3)		Temperature Rising	150	165		°C
		Hysteresis		30		°C
SW DISCHARGE RESISTANCE						
V_{OUT} discharge resistance		V_{EN} = 0, V_{SW} = 0.5V, T_J = 25°C		200		Ω

(1) Not representative of the total input current of the system when in regulation. Specified by design and characterization test.
(2) Not production tested. Specified by design.
(3) Not production tested. Specified by design and engineering sample correlation.

5.6 Typical Characteristics

V_{IN} = 24V (unless otherwise noted).

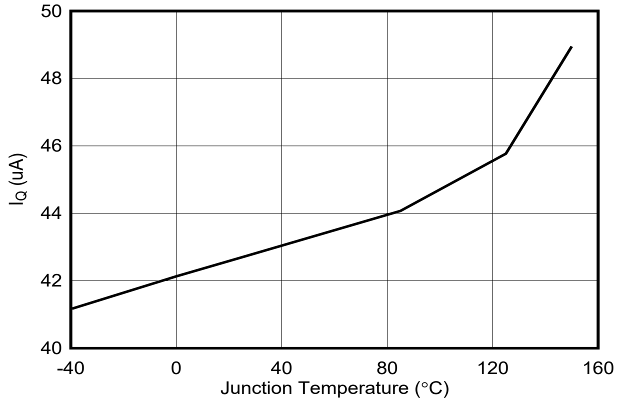


Figure 5-1. Quiescent Current vs Temperature

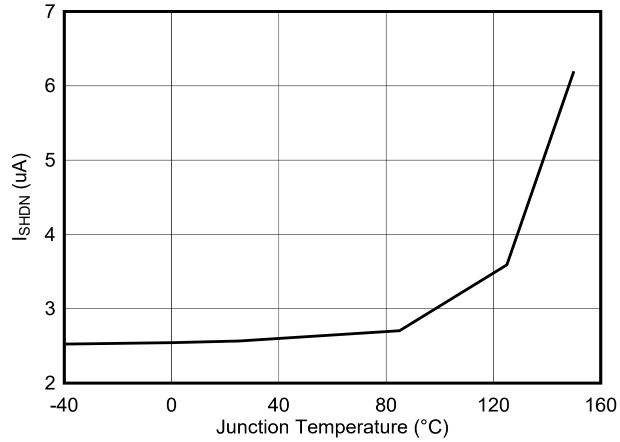


Figure 5-2. Shutdown Current vs Temperature

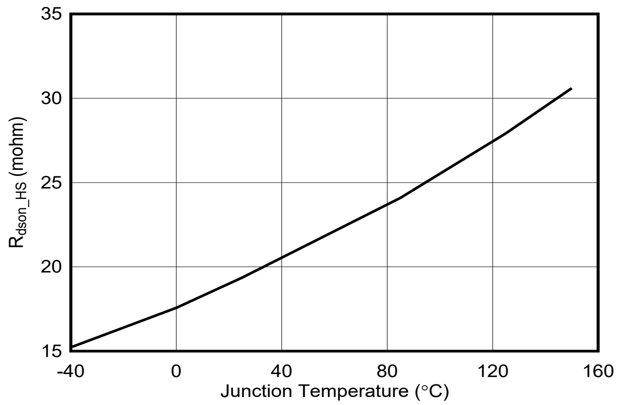


Figure 5-3. High-Side R_{DS}(on) vs Temperature

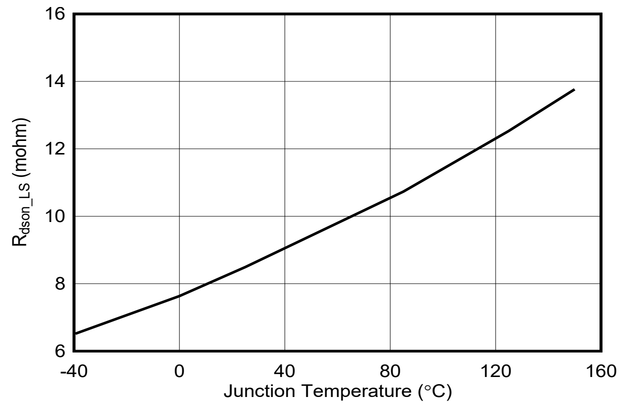


Figure 5-4. Low-Side R_{DS}(on) vs Temperature

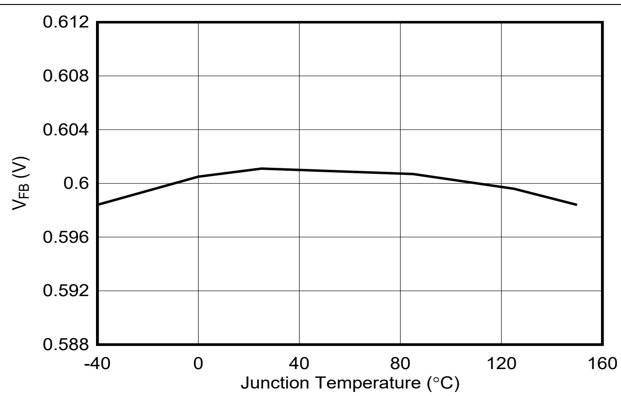


Figure 5-5. Feedback Voltage vs Temperature

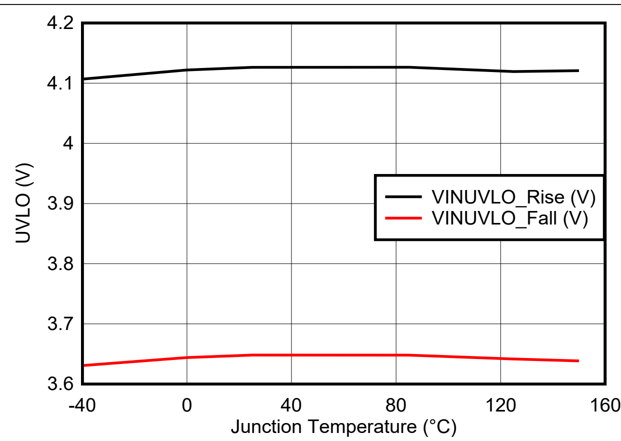


Figure 5-6. VIN UVLO vs Temperature

5.6 Typical Characteristics (continued)

V_{IN} = 24V (unless otherwise noted).

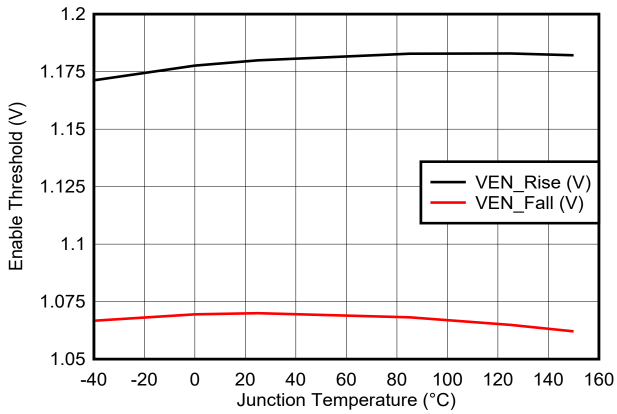


Figure 5-7. EN Threshold vs Temperature

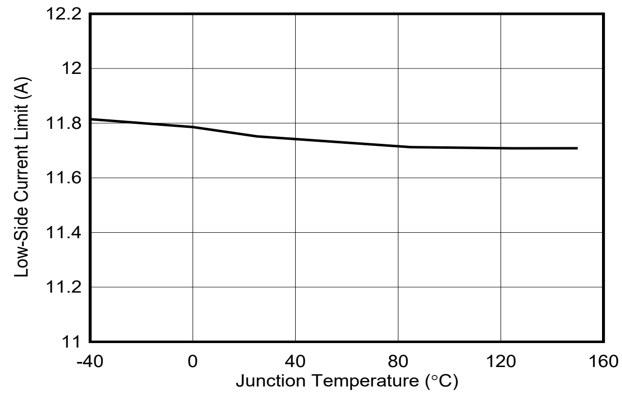


Figure 5-8. Low-Side Valley Current Limit vs Temperature

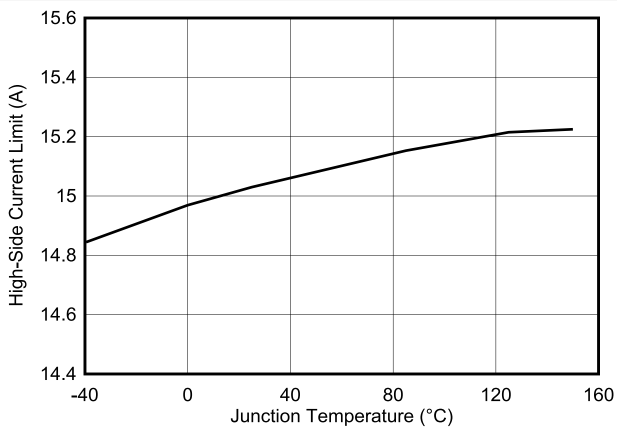


Figure 5-9. High-side Peak Current Limit vs Temperature

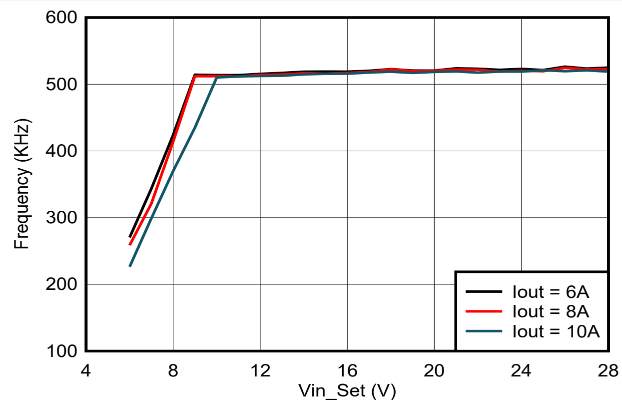


Figure 5-10. Switching Frequency vs Input Voltage, Vout = 5V, Fsw = 500kHz

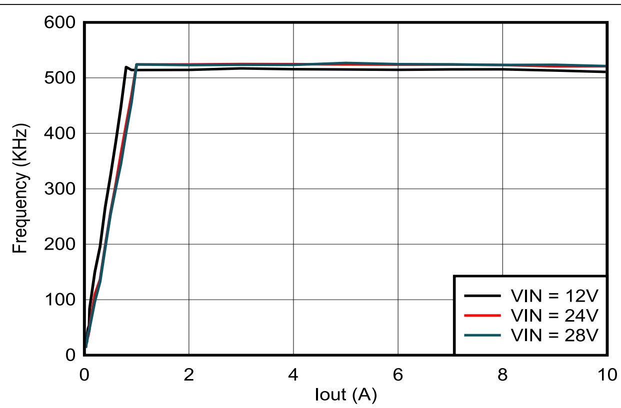


Figure 5-11. Switching Frequency vs Output Current, Vout = 5V, Fsw = 500kHz

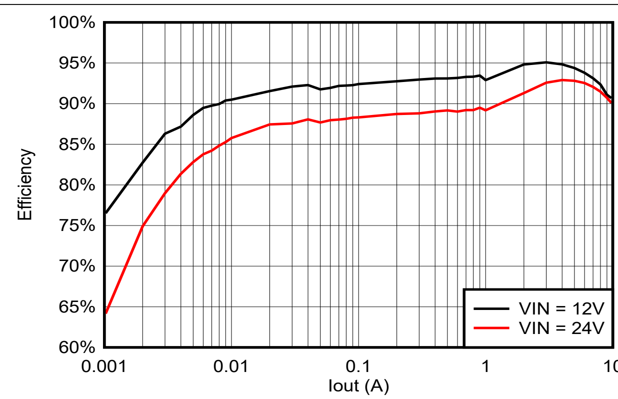


Figure 5-12. Efficiency, Vout = 3.3V, Fsw = 500kHz

5.6 Typical Characteristics (continued)

V_{IN} = 24V (unless otherwise noted).

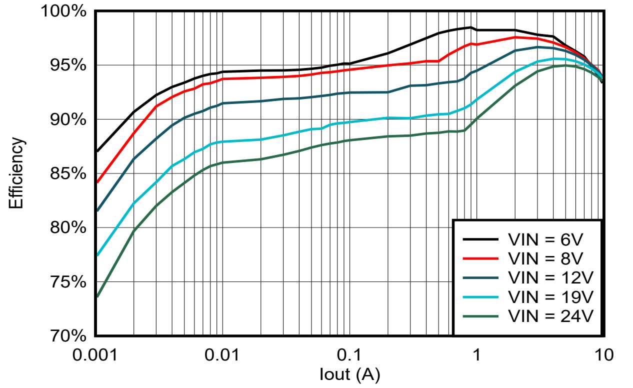


Figure 5-13. Efficiency, Vout = 5V, Fsw = 500kHz

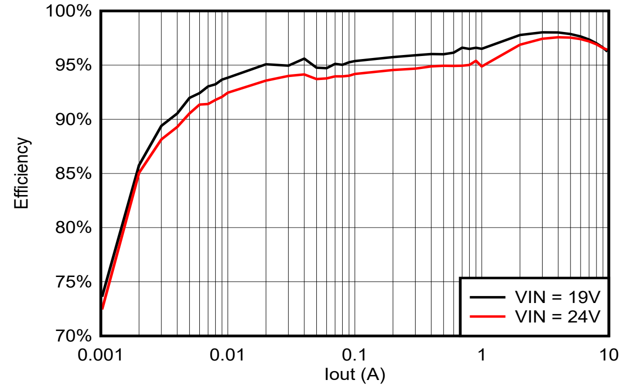


Figure 5-14. Efficiency, Vout = 12V, Fsw = 500kHz

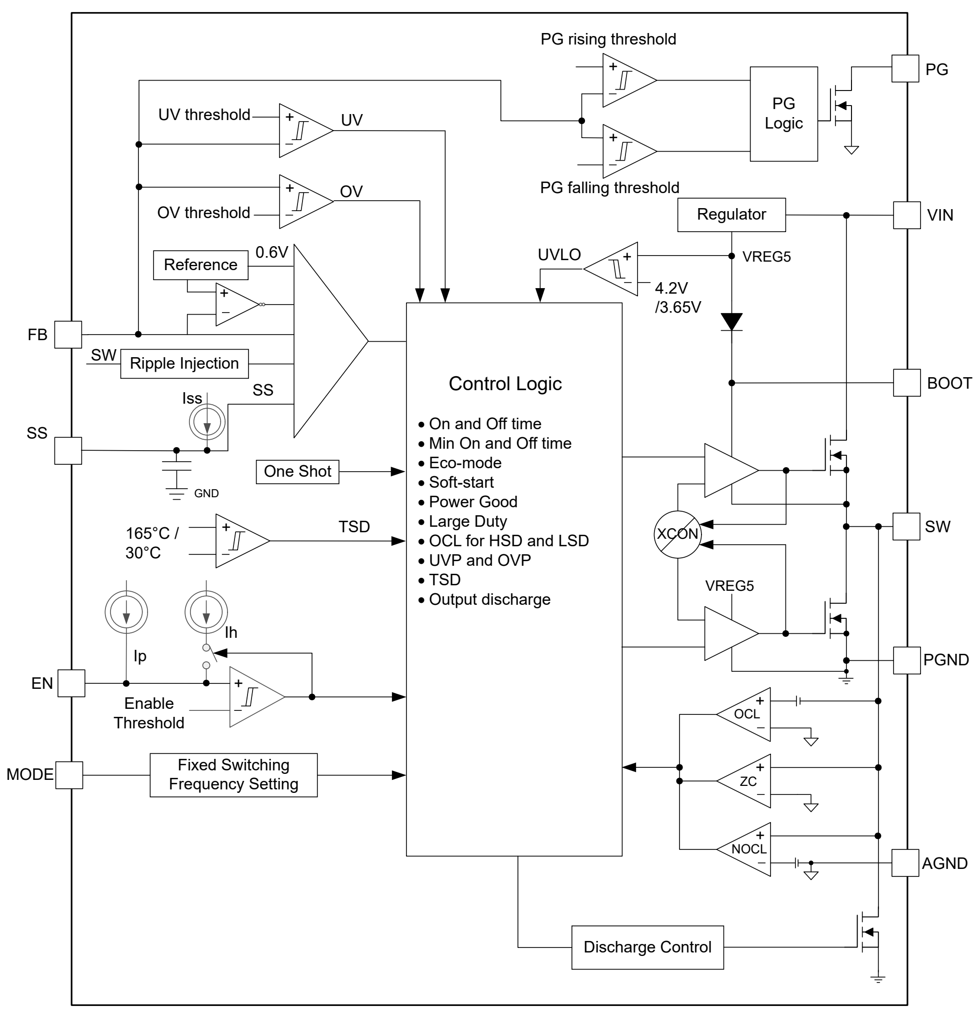
6 Detailed Description

6.1 Overview

The TPS56A37 is an 10A synchronous buck converter operating from 4.5V to 28V input voltage (Vin). The device output voltage ranges from 0.6V to 13V (Vout) and supports 10A continuous output current with fixed 500kHz switching frequency. The proprietary D-CAP3 control mode enables low external component count, ease of design, optimization of the power design for power, size and efficiency. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition. Eco-mode allows the TPS56A37 to maintain high efficiency at light load. The TPS56A37 is able to adapt both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The EN pin has an internal pullup current that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. Soft-start time can be set by connecting a capacitor to the SS pin. Leaving the SS pin floating is set to default 1.8ms soft-start time. The TPS56A37 has the PG pin to indicate output status and has a built-in discharge function by using an integrated MOSFET with 200Ω $R_{DS(on)}$. The device is protected from output short, undervoltage, overvoltage, and overtemperature conditions.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS56A37 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for quasi-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The D-CAP3 control mode is stable even with virtually no ripple at the output. The TPS56A37 also includes an error amplifier that makes the output voltage very accurate. No external current sense network or loop compensation is required for D-CAP3 control mode topology.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the output voltage V_{OUT}, and is inversely proportional to the converter input voltage V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. When the feedback voltage falls below the reference voltage, the one-shot timer is reset and the high-side MOSFET is turned on again. An internal ripple generation circuit is added to reference voltage for emulating the output ripple, and this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC).

6.3.2 Power Up Sequence

Figure 6-1 shows the typical start-up sequence of the device after the enable signal triggers the EN turn-on threshold. After the voltage of internal VCC crosses the UVLO rising threshold, the MODE setting is read. After this process, the MODE is latched and does not change until VIN or EN toggles to restart-up this device. Then after a delay, the internal soft-start function begins to ramp up and Vout ramps up smoothly. When Vout is up to the reference voltage, PGOOD turns to high after a delay.

The MODE pin of TPS56A37 is the internal fixed switching frequency setting pin which TI recommends to connect a 1% 52.3k resistor to AGND.

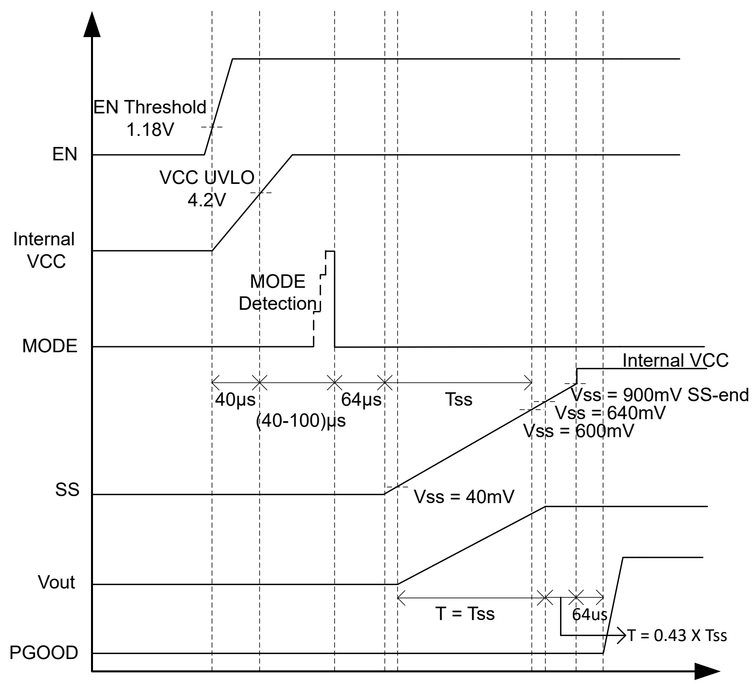


Figure 6-1. Power-Up Sequence

6.3.3 Eco-mode Control Scheme

TPS56A37 is set to Eco-mode control scheme to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in the continuous conduction mode so that longer time is needed to discharge the output capacitor with smaller load current to the level of the reference voltage. This process makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Equation 1 calculates the transition point to the light load operation $I_{OUT(LL)}$ current.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times Fsw} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{1}$$

6.3.4 Soft Start and Prebiased Soft Start

The TPS56A37 has an adjustable soft-start time that can be set by connecting a capacitor between SS and AGND. Leaving the SS pin floating is set to default internal soft start time 1.8ms. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. The device tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time (T_{SS}) is shown in Equation 2.

$$T_{ss} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \tag{2}$$

If the external capacitor (C_{SS}) has pre-stored voltage at start-up, the device initially discharge the external capacitor voltage to lower voltage then charge again to prevent inrush start-up.

If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme makes sure that the converters ramp up smoothly into regulation point.

6.3.5 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the standby operation.

The EN pin has an internal pullup current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, open-drain or open-collector output logic can be used to interface with the pin.

The TPS56A37 implements internal undervoltage lockout (UVLO) circuitry on the V_{IN} pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 500mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 6-2. When using the external UVLO function, TI recommends setting the hysteresis at a value greater than 500mV.

The EN pin has a small pullup current, I_p, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because the pullup current increases by I_h when the EN pin crosses the enable threshold. Use Equation 3 and Equation 4 to calculate the values of R1 and R2 for a specified UVLO threshold. After R1, R2 settle down, the V_{EN} voltage can be calculated by Equation 5, which must be lower than 5.5V with maximum V_{EN}.

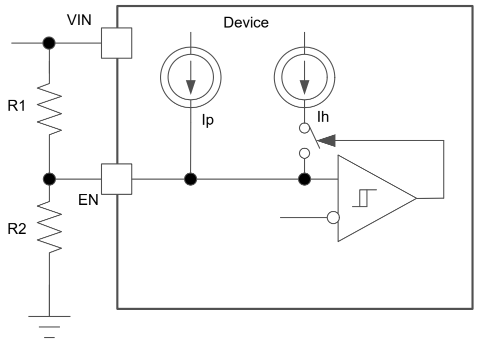


Figure 6-2. Adjustable VIN Undervoltage Lockout

$$R_1 = \frac{V_{START} \times \frac{V_{ENfalling}}{V_{ENrising}} - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \tag{3}$$

$$R_2 = \frac{R_1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_1 \times \left(I_p + I_h\right)} \tag{4}$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 \times R_2 \times \left(I_p + I_h\right)}{R_1 + R_2} \tag{5}$$

Where

- I_p = 1μA
- I_h = 3μA
- $V_{ENfalling}$ = 1.07V
- $V_{ENrising}$ = 1.18V

6.3.6 Output Overcurrent Limit and Undervoltage Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle low-side MOSFET valley current detection and high-side MOSFET peak current detection. The switching current is monitored by measuring the MOSFET drain to source voltage. This voltage is proportional to the switching current. To improve accuracy, the voltage sensing is temperature compensated.

There are some important considerations for this type of overcurrent limit. When the load current is higher than the I_{LS_OCL} added by one half of the peak-to-peak inductor ripple current, or higher than I_{HS_OCL} subtracted by one half of the peak-to-peak inductor ripple current, the OCP is triggered and the current is being limited. Output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 65% of the target voltage, the UVP comparator detects the fall and shuts down the device after a deglitch wait time of 256us and then re-start after the hiccup time of 10.5 cycles of soft-start time. When the overcurrent condition is removed, the output recovers.

6.3.7 Overvoltage Protection

The TPS56A37 has the overvoltage protection feature. When the output voltage becomes higher than 125% of the target voltage, the OVP is triggered. The output discharges after a deglitch time of 32us and both the high-side MOSFET driver and the low-side MOSFET driver turn off. When the overvoltage condition is removed, the output voltage recovers.

6.3.8 UVLO Protection

Undervoltage Lockout protection(UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. This protection is non-latched.

6.3.9 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 165°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and the discharge path is turned on. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 30°C is implemented on the thermal shutdown temperature.

6.3.10 Output Voltage Discharge

The TPS56A37 has a built in discharge function by using an integrated MOSFET with 200Ω $R_{DS(on)}$, which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET. The discharge path turns on when the device is turned off due to UV, OV, OT, and EN shutdown conditions.

6.3.11 Power Good

The TPS56A37 has a built in power-good (PG) function to indicate whether the output voltage has reached the appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 5.5V). TI recommends a pullup resistor of 100kΩ to pull up to 5V voltage. It can sink 10mA of current and maintain the specified logic low level. After the FB pin voltage is between 90% and 110% of the internal reference voltage (V_{REF}) and after a deglitch time of 64µs, the PG turns to high impedance status. The PG pin is pulled low after a deglitch time of 32µs when FB pin voltage is lower than 85% of the internal reference voltage or greater than 115% of the internal reference voltage, or in events of EN shutdown, UVLO conditions, and thermal shutdown. V_{IN} must remain present for the PG pin to stay low as shown in Table 6-1.

Table 6-1. Power-Good Pin Logic Table

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	90% × V_{REF} =< V_{FB} <= 110% × V_{REF}	√	
	V_{FB} < 85% × V_{REF} or V_{FB} > 115% × V_{REF}		√
Shutdown (EN=Low)			√
UVLO	2V < V_{IN} < V_{UVLO}		√
Thermal shutdown	T_J > T_{SD}		√
Power supply removal	V_{IN} < 2V	√	

6.3.12 Large Duty Operation

The TPS56A37 can support large duty operations by smoothly dropping down the switching frequency. The switching frequency is allowed to smoothly drop when duty cycle is higher than 62% to make T_{ON} extended to implement the large duty operation and also improve the performance of the load transient. The TPS56A37 can support up to 98% duty cycle operation.

6.4 Device Functional Modes

6.4.1 Standby Operation

The TPS56A37 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 3µA (typical) when in standby condition.

6.4.2 Light Load Operation

TPS56A37 is set to Eco-mode control scheme. The device enters pulse skip mode after the valley of the inductor ripple current crosses zero. The Eco-mode control scheme maintains higher efficiency at light load with a lower switching frequency.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The schematic of Figure 7-1 shows a typical application for TPS56A37. This design converts an input voltage range of 5.5V to 28V down to 5V with a maximum output current of 10A.

7.2 Typical Application

The application schematic in Figure 7-1 shows the TPS58637 5.5V to 28V input, 5V output converter design meeting the requirements for 10A output. This circuit is available as the evaluation module (EVM). The following sections provide the design procedure.

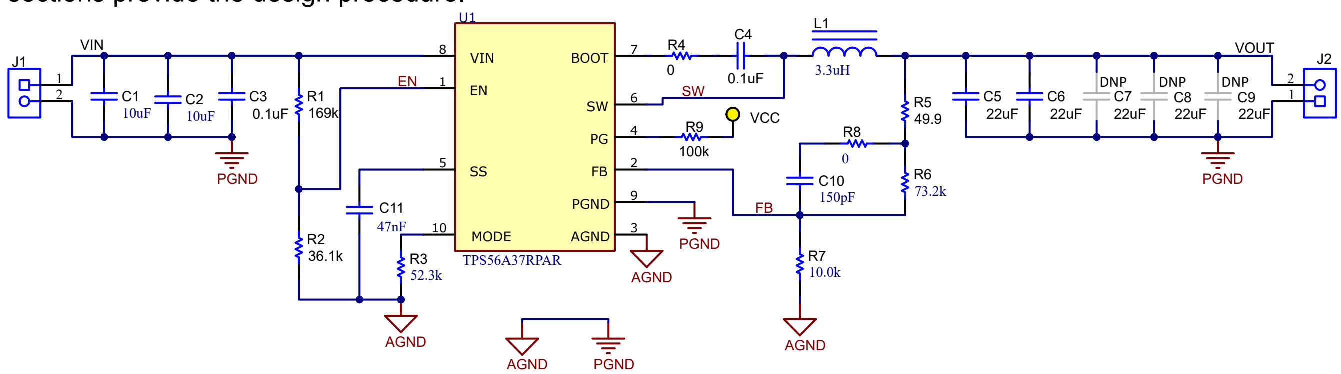


Figure 7-1. TPS56A37 5V, 10A Reference Design

7.2.1 Design Requirements

Table 7-1 shows the design parameters for this application.

Table 7-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	24V nominal, 5.5V to 28V
Output voltage	5V
Transient response, 10A load step	ΔV_{OUT} = ±5%
Output ripple voltage	< 50mV at CCM
Output current rating	10A
Operating frequency	500kHz

7.2.2 Detailed Design Procedure

7.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 6 to calculate VOUT R5 is optional and can be used to measure the control loop frequency response.

To improve efficiency at very light loads, consider using larger value resistors. If the resistance is too high, the device is more susceptible to noise and voltage errors from the VFB input current is more noticeable. Please note that TI does not recommend dynamically adjusting output voltage.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R6}{R7}\right) \tag{6}$$

7.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{7}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. D-CAP3 control mode introduces a high frequency zero that reduces the gain roll off to –20dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 7 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, use the values recommended in Table 7-2.

Table 7-2. Recommended Component Values

Switching Frequency (kHz)	Output Voltage[1] (V)	R6[2] (kΩ)	R7 (kΩ)	L1 (µH)	C_{OUT} [3]			C10 [4](pF)
					Minimum	Typical	Maximum	
500	1.05	7.5	10	1	22uF × 1	22uF × 3	22uF × 10	
	1.8	20	10	1.5	22uF × 1	22uF × 3	22uF × 10	
	3.3	45.3	10	2.2	22uF × 1	22uF × 3	22uF × 10	100-200 (150 typical)
	5	73.2	10	3.3	22uF × 1	22uF × 2	22uF × 10	100-200 (150 typical)
	9	140	10	4.7	22uF × 1	22uF × 2	22uF × 10	50-150 (100 typical)
	12	383	20	5.6	22uF × 1	22uF × 2	22uF × 10	30-100 (30 typical)

(1) Please use the recommended L1 and C_{OUT} combination of the higher and closest output rail for unlisted output rails.
(2) R6 = 0Ω for V_{OUT} = 0.6V.
(3) C_{OUT} in this data sheet is using Murata GRM32ER71E226KE15L 25VDC capacitor. Recommend to use the same effective output capacitance. The effective capacitance is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. A careful study of bias and temperature variation of any capacitor bank must be made to make sure that the minimum value of effective capacitance is provided. Refer to the

information of DC bias and temperature characteristics from manufacturers of ceramic capacitors. Higher than Cout_max capacitance is allowed by careful tuning the feedforward compensation.

(4) R8 and C10 can be used to improve the load transient response or improve the loop-phase margin. The *Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor* application report is helpful when experimenting with a feed-forward capacitor.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 8, Equation 9, and Equation 10. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 500kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 9 and the RMS current of Equation 10.

$$Il_{p-p} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_{OUT} \times Fsw} \tag{8}$$

$$Il_{PEAK} = I_O + \frac{Il_{p-p}}{2} \tag{9}$$

$$I_{LO(RMS)} = \sqrt{I_O{}^2 + \frac{1}{12} \times Il_{p-p}{}^2} \tag{10}$$

For this design example, the calculated peak current is 11.25A and the calculated RMS current is 10.03A. The inductor used is Wurth 744325330 with saturation current 15A and rating current 9.7A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS56A37 is intended for use with ceramic or other low ESR capacitors. Use Equation 11 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times Fsw} \tag{11}$$

For this design, two MuRata GRM32ER71E226KE15L 22µF output capacitors are used so that the effective capacitance is 35µF at DC biased voltage of 5V. The calculated RMS current is 0.69A and each output capacitor is rated for 5A.

7.2.2.3 Input Capacitor Selection

The TPS56A37 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10µF for the decoupling capacitor. TI recommends an additional 0.1µF capacitor (C3) from VIN to PGND pin to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage. The input voltage ripple can be calculated using Equation 12.

$$\Delta V_{IN} = \frac{I_{OUTMAX} \times 0.25}{C_{IN} \times Fsw} \tag{12}$$

The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 13:

$$I_{CIN(RMS)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(MIN)}} \times \frac{V_{IN(MIN)} - V_{OUT}}{V_{IN(MIN)}}} \tag{13}$$

7.2.2.4 Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor (C4) must be connected between the BOOT to SW pin for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10V or higher voltage rating.

7.2.3 Application Curves

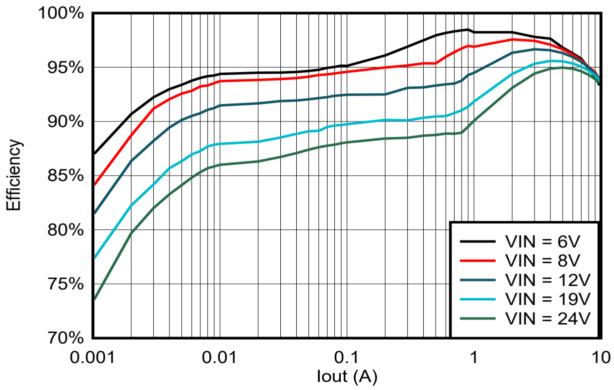


Figure 7-2. Efficiency

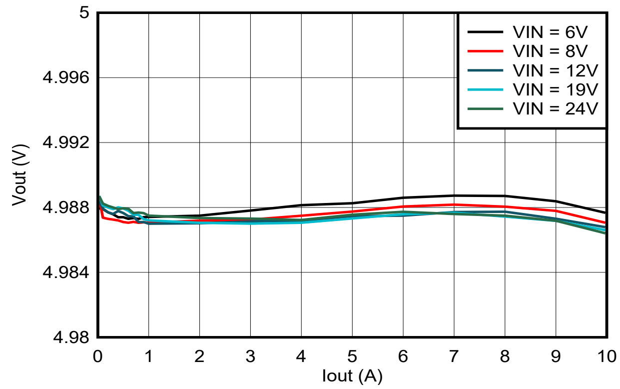


Figure 7-3. Load Regulation

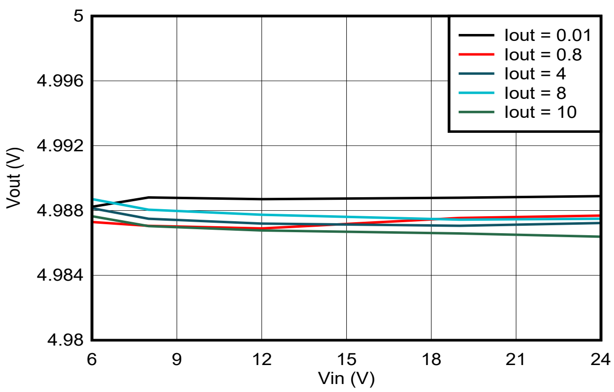
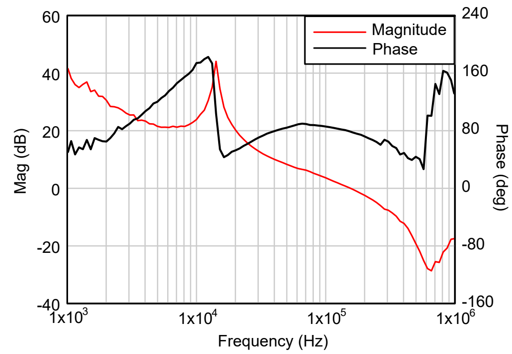


Figure 7-4. Line Regulation



V_{IN} = 24V V_{OUT} = 5V I_{OUT} = 5A Fsw = 500kHz

Figure 7-5. Bode Plot

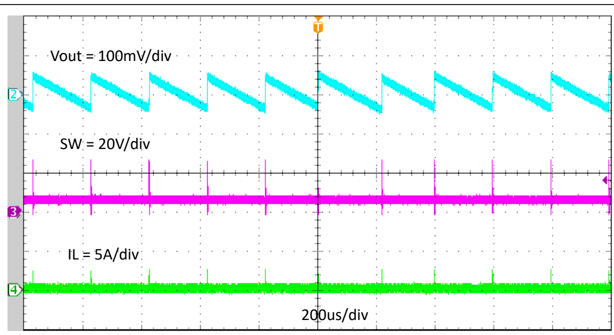


Figure 7-6. Steady State Waveforms, I_{OUT} = 0.01A

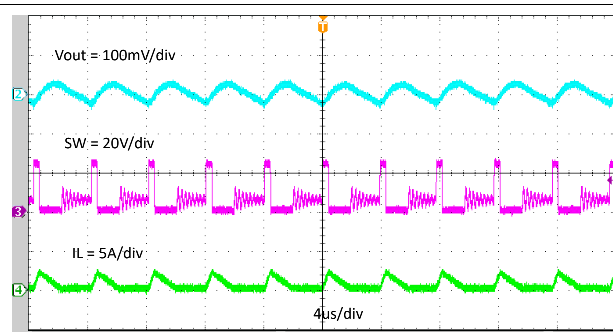


Figure 7-7. Steady State Waveforms, I_{OUT} = 0.5A

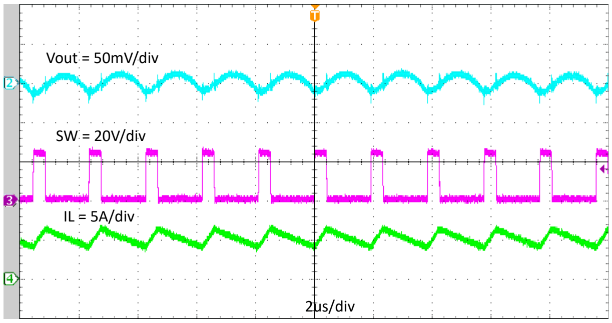


Figure 7-8. Steady State Waveforms, I_{OUT} = 5A

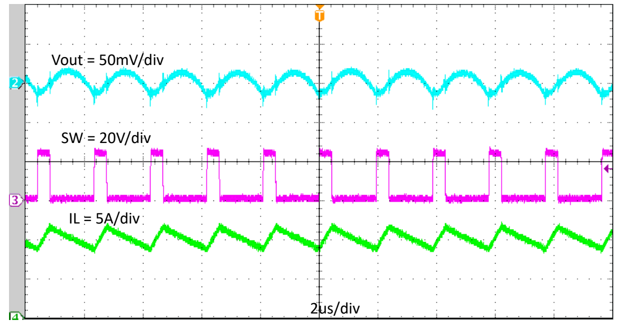


Figure 7-9. Steady State Waveforms, I_{OUT} = 10A

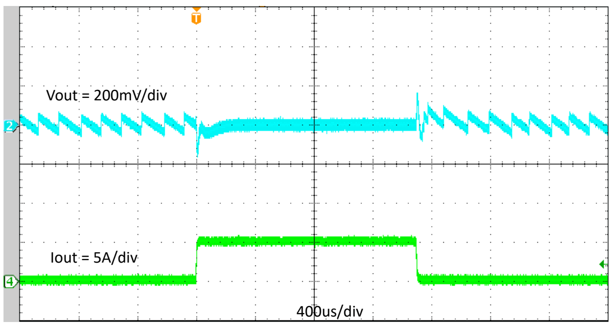


Figure 7-10. Transient Response 0A to 5A

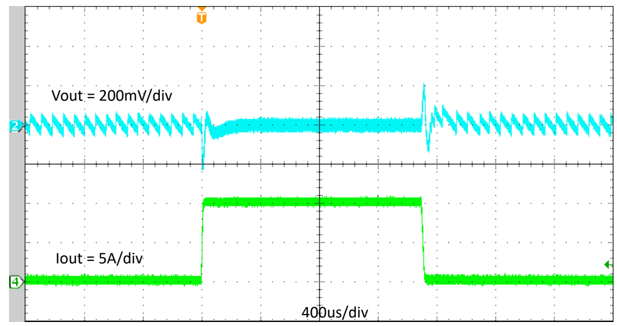


Figure 7-11. Transient Response 0A to 10A

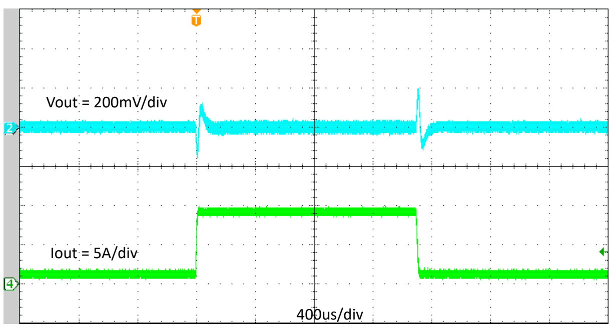


Figure 7-12. Transient Response 1A to 9A

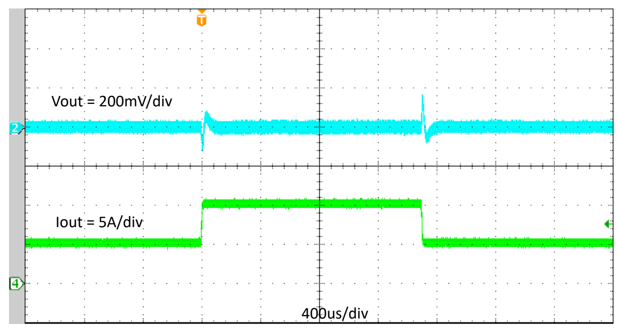


Figure 7-13. Transient Response 5A to 10A

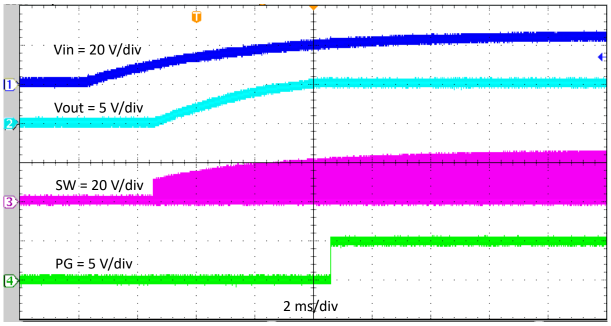


Figure 7-14. Start-Up Relative to V_{IN}

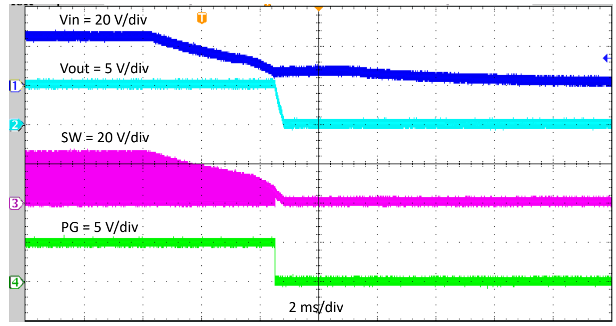


Figure 7-15. Shutdown Relative to V_{IN}

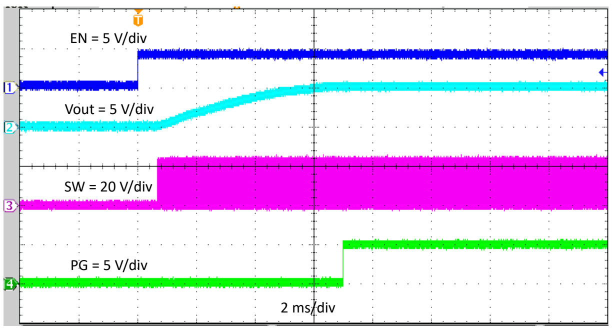


Figure 7-16. Enable Relative to EN

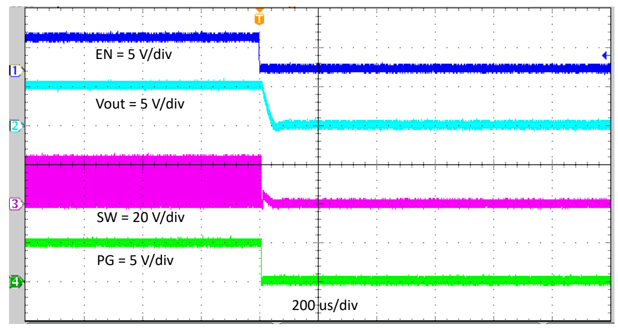


Figure 7-17. Disable Relative to EN

7.3 Power Supply Recommendations

The TPS56A37 is designed to operate from input supply voltage in the range of 4.5V to 28V. Buck converters require the input voltage to be higher than the output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56A37 circuit, TI recommends some additional input bulk capacitance.

7.4 Layout

7.4.1 Layout Guidelines

1. Use a four-layer PCB with maximum ground plane partitioning possible for good thermal performance. A 76mm × 76mm, four-layer PCB with 2-1-1-2oz copper is used as example.
2. Make VIN and PGND traces as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
3. Put at least two vias for PGND pad for better thermal performance.
4. Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
5. Provide sufficient vias for the input capacitor and output capacitor.
6. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
7. Do not allow switching current to flow under the device.
8. Keep the SS trace as far as possible to SW trace to minimize coupling during soft start.
9. Connect a separate VOUT path to the upper feedback resistor.
10. Keep the voltage feedback loop away from the high-voltage switching trace, and preferably has ground shield.
11. Make the trace of the VFB node as small as possible to avoid noise coupling. Also keep feedback resistors and the feedforward capacitor near the IC.
12. Make the PGND trace between the output capacitor and the PGND pin as wide as possible to minimize the trace impedance.
13. Inner layer 1 is PGND and AGND with the single point net tie.
14. Inner layer 2 is PGND for better heat dissipation.

7.4.2 Layout Example

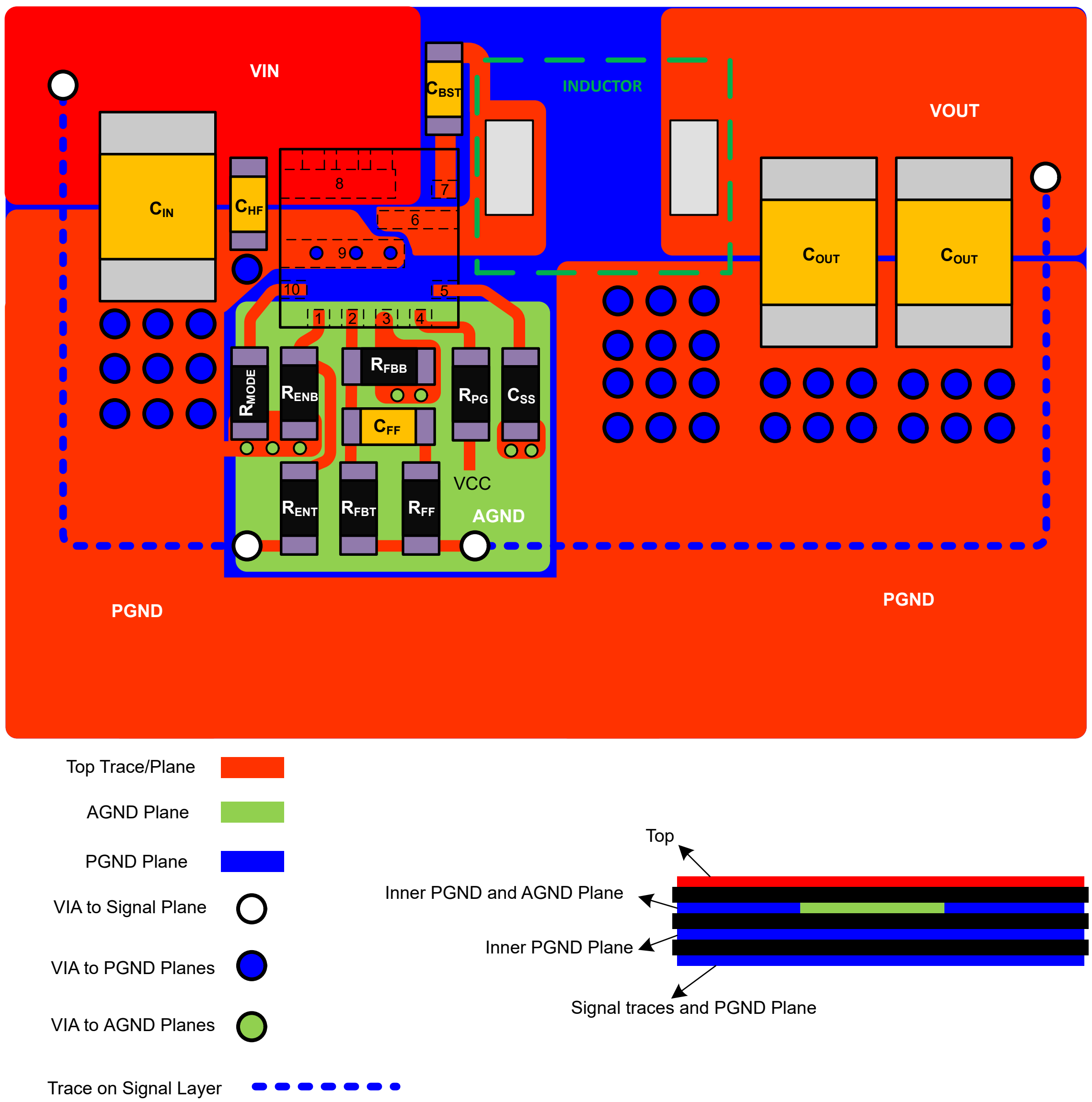


Figure 7-18. TPS56A37 layout

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor* application report

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
January 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS56A37RPAR	Active	Production	VQFN-HR (RPA) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	T56A37
TPS56A37RPAR.A	Active	Production	VQFN-HR (RPA) | 10	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 150	T56A37

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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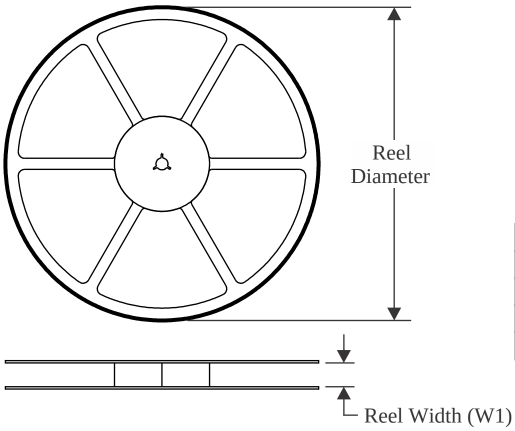
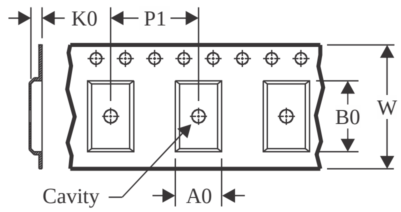
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

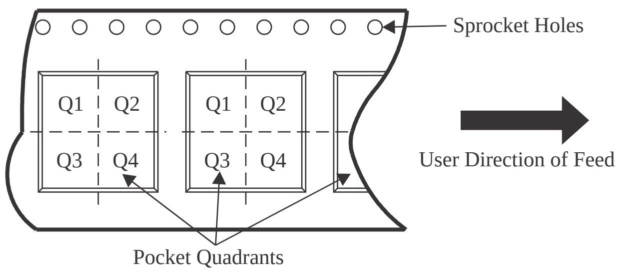


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

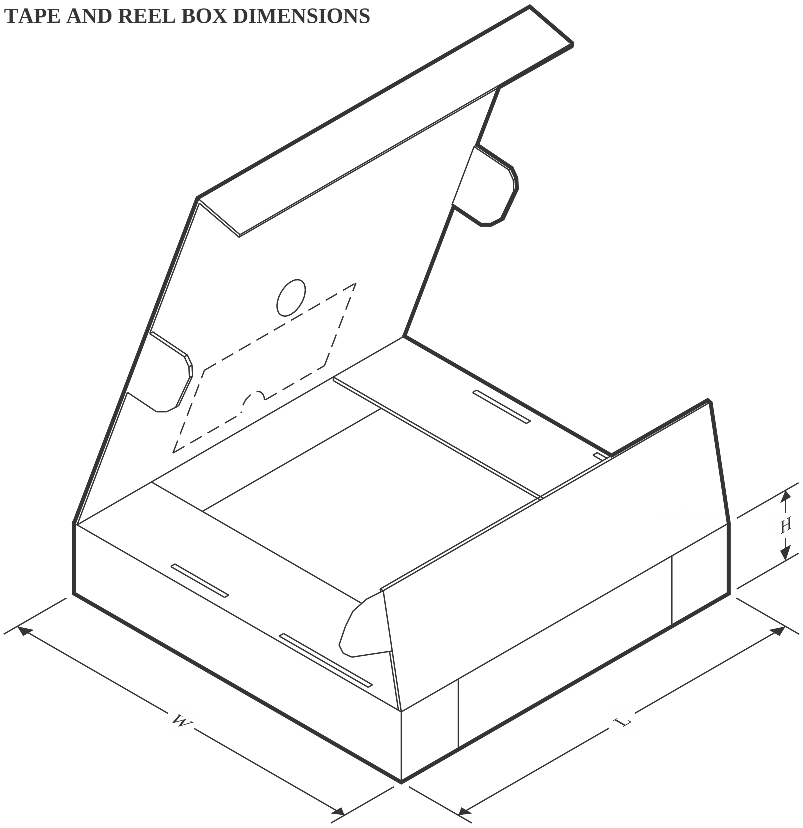
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

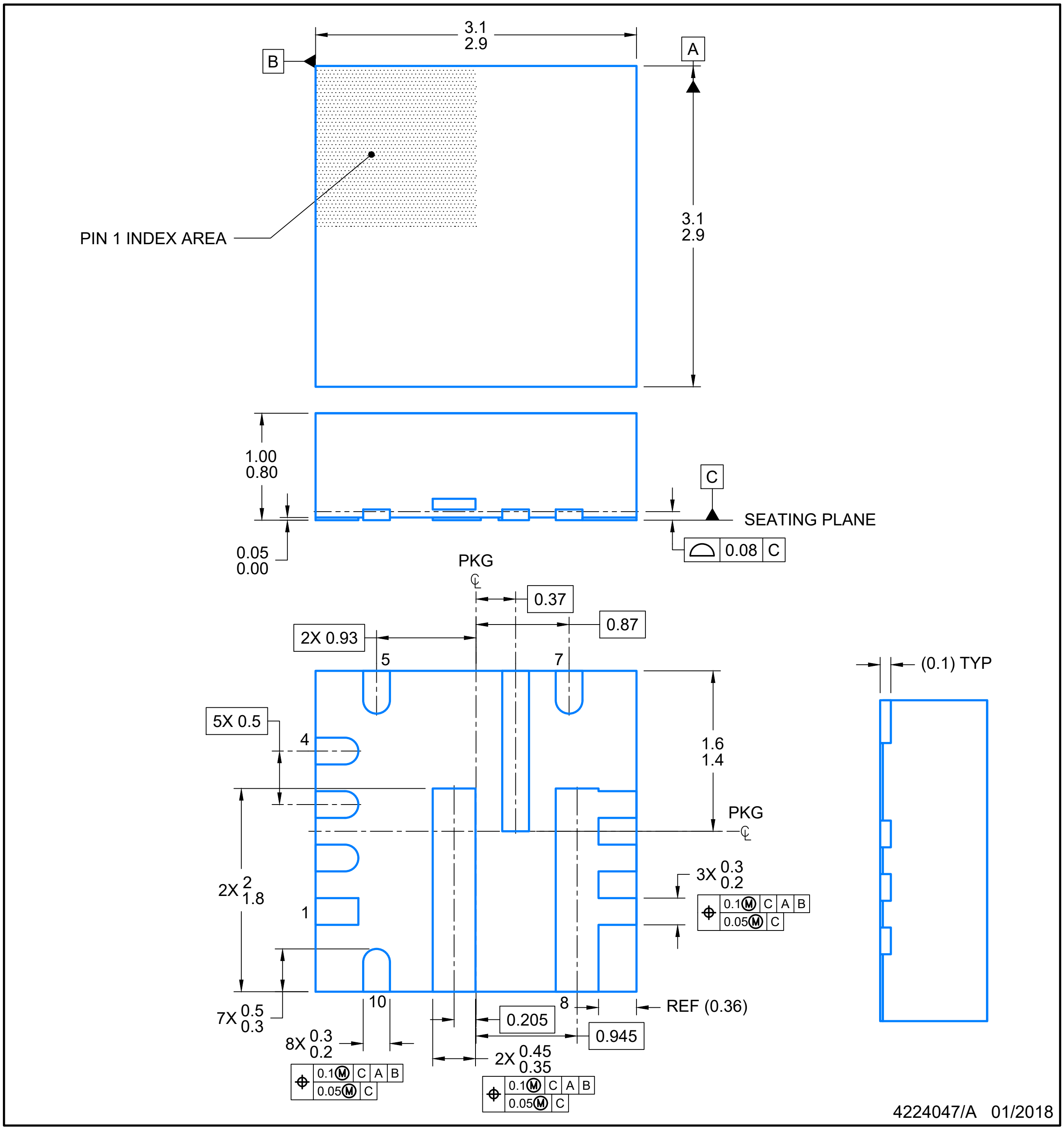
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56A37RPAR	VQFN-HR	RPA	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



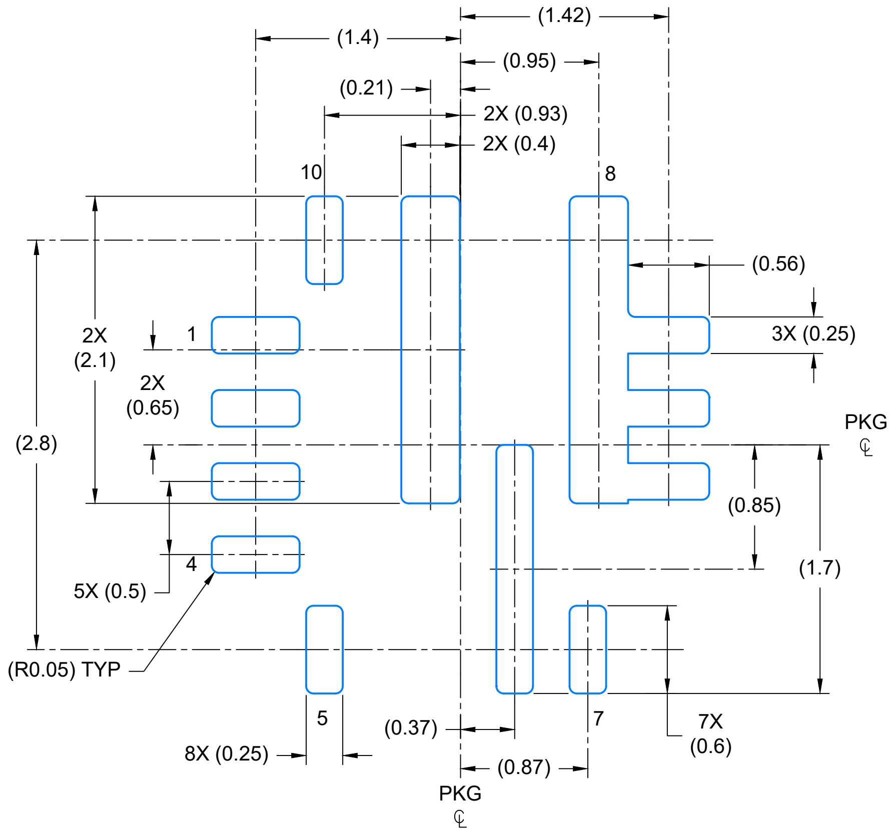
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56A37RPAR	VQFN-HR	RPA	10	3000	360.0	360.0	36.0

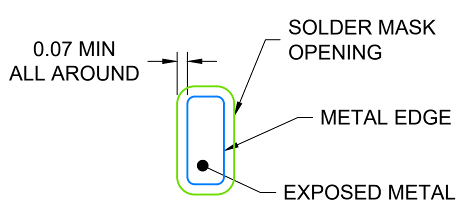


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

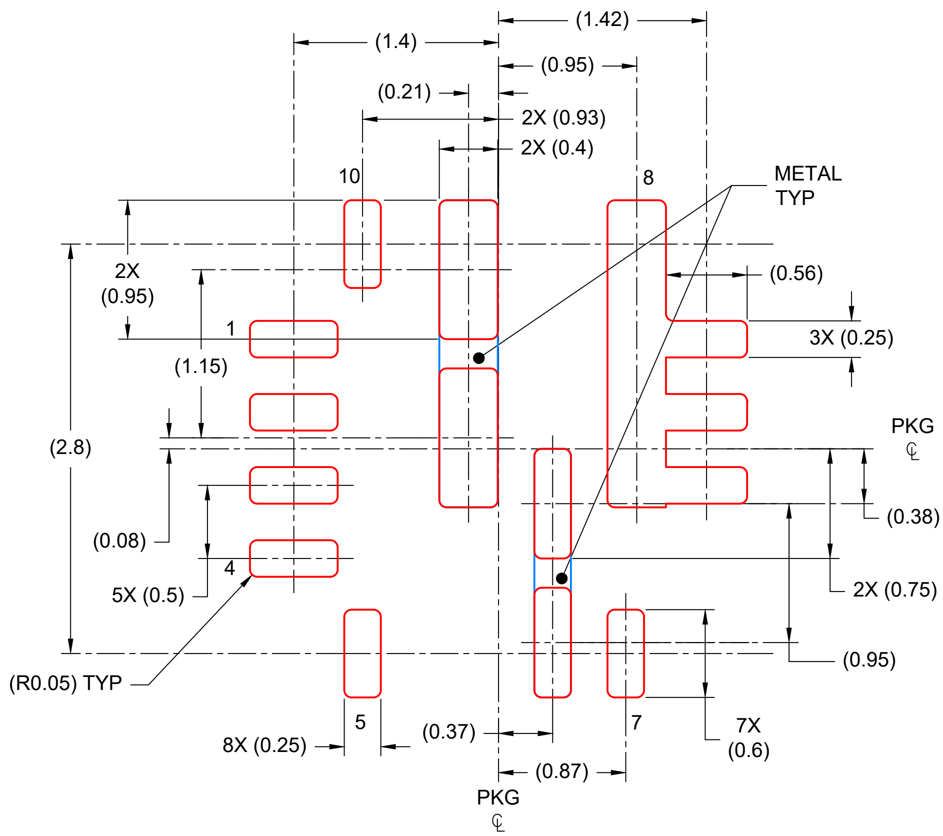


NON SOLDER MASK
DEFINED

4224047/A 01/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
PADS 6 and 9: 89% PRINTED COVERAGE BY
AREA
SCALE: 20X

4224047/A 01/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.