TPS6104x Low-Power, DC-DC Boost Converters in SOT-23 and WSON Packages

1 Features

- 1.8V to 6V input voltage range
- Adjustable output voltage range up to 28V
- 400mA (TPS61040) and 250mA (TPS61041) internal switch current
- Up to 1MHz switching frequency
- 28µA typical no-load quiescent current
- 1µA typical shutdown current
- Internal soft start
- Available in SOT23-5, TSOT23-5, and 2mm × 2mm × 0.8mm WSON packages

2 Applications

- LCD bias supply
- White-LED supply for LCD backlights
- Digital still camera
- PDAs, organizers, and handheld PCs
- Cellular phones
- Internet audio players
- Standard 3.3V or 5V to 12V conversion

3 Description

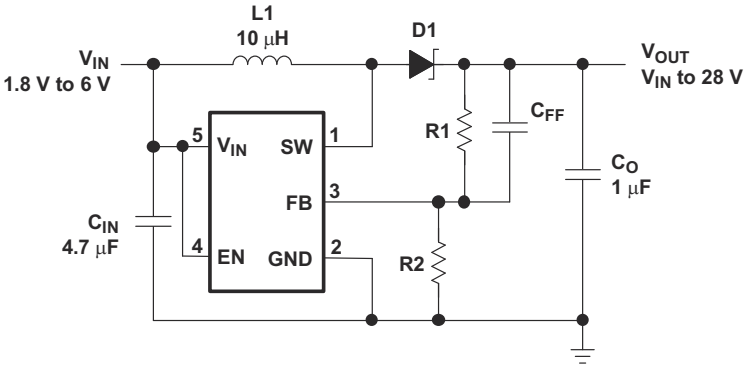
The TPS6104x is a high-frequency boost converter dedicated for small to medium LCD bias supply and white LED backlight supplies. The device is designed to generate output voltages up to 28V from a dual-cell NiMH/NiCd or a single-cell Li-Ion battery. The part can also be used to generate standard 3.3V or 5V to 12V power conversions.

The TPS6104x operates with a switching frequency up to 1MHz. This frequency allows the use of small external components using ceramic as well as tantalum output capacitors. Together with the thin WSON package, the TPS6104x gives a very small overall design size. The TPS61040 device has an internal 400mA switch current limit, while the TPS61041 device has a 250mA switch current limit, offering lower output voltage ripple and allows the use of a smaller form factor inductor for lower power applications. The low quiescent current (typically 28µA) together with an optimized control scheme, allows device operation at very high efficiencies over the entire load current range.

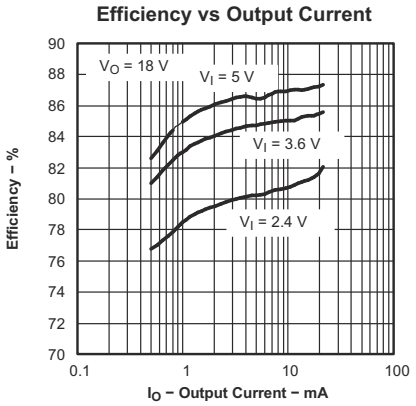
Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS61040	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DDC (SOT-23-THN, 5)	2.9mm × 2.8mm
	DRV (WSON, 6)	2mm × 2mm
TPS61041	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DRV (WSON, 6)	2mm × 2mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Schematic



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Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Pin Configuration and Functions....3
5 Specifications....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....4
5.4 Thermal Information....4
5.5 Electrical Characteristics....5
5.6 Typical Characteristics....6
6 Detailed Description....9
6.1 Overview....9
6.2 Functional Block Diagram....9
6.3 Feature Description....9
6.4 Device Functional Modes....10
7 Application and Implementation....11
7.1 Application Information....11
7.2 Typical Application....11
7.3 System Examples....16
7.4 Power Supply Recommendations....18
7.5 Layout....18
8 Device and Documentation Support....20
8.1 Device Support....20
8.2 Receiving Notification of Documentation Updates....20
8.3 Support Resources....20
8.4 Trademarks....20
8.5 Electrostatic Discharge Caution....20
8.6 Glossary....20
9 Revision History....20
10 Mechanical, Packaging, and Orderable Information....21

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4 Pin Configuration and Functions

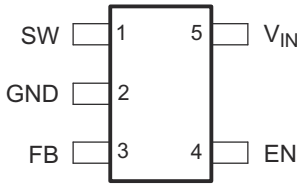


Figure 4-1. DDC Package, DBV Package SOT 5 Pins Top View

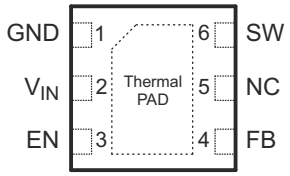


Figure 4-2. DRV Package WSON 6 Pins Transparent Top View

Table 4-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	DDC, DBV NO.	DRV NO.		
EN	4	3	I	This is the enable pin of the device. Pulling this pin to ground forces the device into shutdown mode reducing the supply current to less than 1µA. This pin must not be left floating and needs to be terminated.
FB	3	4	I	This is the feedback pin of the device. Connect this pin to the external voltage divider to program the desired output voltage.
GND	2	1	—	Ground
NC	—	5	—	No connection
SW	1	6	I	Connect the inductor and the Schottky diode to this pin. This is the switch pin and is connected to the drain of the internal power MOSFET.
V_{IN}	5	2	I	Supply voltage pin
	—	ThermalPAD	—	Solder to ground plane for heat sink

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltages on pin V_{IN} (2)	–0.3	7	V
Voltages on pins EN, FB (2)	–0.3	V_{IN} + 0.3	V
Switch voltage on pin SW (2)	–0.3	30	V
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22C101(2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500V HBM is possible with the necessary precautions. Pins listed as ±XXX V must actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250V CDM is possible with the necessary precautions. Pins listed as ±YYY V must actually have higher performance.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	1.8		6	V
V_{OUT}	Output voltage range			28	V
L	Inductor(1)	2.2	10		µH
f	Switching frequency(1)			1	MHz
C_{IN}	Input capacitor (1)		4.7		µF
C_{OUT}	Output capacitor (1)	1			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See application section for further information.

5.4 Thermal Information

THERMAL METRIC(1)		TPS61040			TPS61041		UNIT
		DBV	DDC	DRV	DBV	DRV	
		5 PINS	5 PINS	6 PINS	5 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.2	214.7	83.0	205.2	83.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	118.3	38.5	57.1	118.3	57.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.8	35.4	52.9	34.8	52.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.2	0.4	2.4	12.2	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.9	34.8	53.4	33.9	53.4	°C/W

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THERMAL METRIC(1)		TPS61040			TPS61041		UNIT
		DBV	DDC	DRV	DBV	DRV	
		5 PINS	5 PINS	6 PINS	5 PINS	6 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	26.9	—	26.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

V_{IN} = 2.4V, EN = V_{IN}, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		1.8		6	V
I_Q	Operating quiescent current	I_{OUT} = 0mA, not switching, V_{FB} = 1.3V		28	50	µA
I_{SD}	Shutdown current	EN = GND		0.1	1	µA
V_{UVLO}	Undervoltage lockout threshold			1.5	1.7	V
ENABLE						
V_{IH}	EN high level input voltage		1.3			V
V_{IL}	EN low level input voltage				0.4	V
I_I	EN input leakage current	EN = GND or V_{IN}		0.1	1	µA
POWER SWITCH AND CURRENT LIMIT						
Vsw	Maximum switch voltage				30	V
t_{off}	Minimum off time		250	400	550	ns
t_{on}	Maximum on time		4	6	7.5	µs
$R_{DS(on)}$	MOSFET on-resistance	V_{IN} = 2.4V; I_{SW} = 200mA; TPS61040		600	1000	mΩ
$R_{DS(on)}$	MOSFET on-resistance	V_{IN} = 2.4V; I_{SW} = 200mA; TPS61041		750	1250	mΩ
	MOSFET leakage current	V_{SW} = 28V		1	10	µA
I_{LIM}	MOSFET current limit	TPS61040	350	400	450	mA
I_{LIM}	MOSFET current limit	TPS61041	215	250	285	mA
OUTPUT						
V_{OUT}	Adjustable output voltage range		V_{IN}		28	V
V_{ref}	Internal voltage reference			1.233		V
I_{FB}	Feedback input bias current	V_{FB} = 1.3V			1	µA
V_{FB}	Feedback trip point voltage	1.8V ≤ V_{IN} ≤ 6V	1.208	1.233	1.258	V
	Line regulation (1)	1.8V ≤ V_{IN} ≤ 6V; V_{OUT} = 18V; I_{load} = 10mA; C_{FF} = not connected		0.05		%/V
	Load regulation(1)	V_{IN} = 2.4V; V_{OUT} = 18V; 0mA ≤ I_{OUT} ≤ 30mA		0.15		%/mA

(1) The line and load regulation depend on the external component selection. See the application section for further information.

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5.6 Typical Characteristics

Table 5-1. Table of Graphs

			FIGURE
η	Efficiency	vs Load current	Figure 5-1, Figure 5-2, Figure 5-3
		vs Input voltage	Figure 5-4
I_Q	Quiescent current	vs Input voltage and temperature	Figure 5-5
V_{FB}	Feedback voltage	vs Temperature	Figure 5-6
I_{SW}	Switch current limit	vs Temperature	Figure 5-7
I_{CL}	Switch current limit	vs Supply voltage, TPS61041	Figure 5-8
		vs Supply voltage, TPS61040	Figure 5-9
$R_{DS(on)}$	$R_{DS(on)}$	vs Temperature	Figure 5-10
		vs Supply voltage	Figure 5-11
	Line transient response		Figure 7-2
	Load transient response		Figure 7-3
	Start-up behavior		Figure 7-4

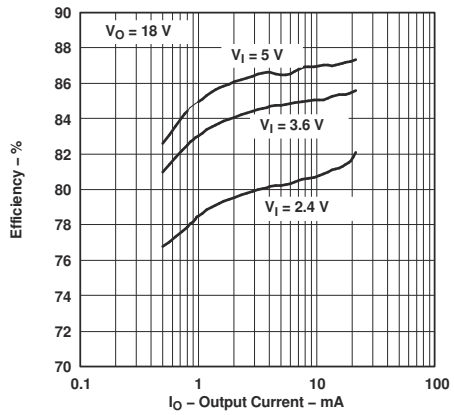


Figure 5-1. Efficiency vs Output Current

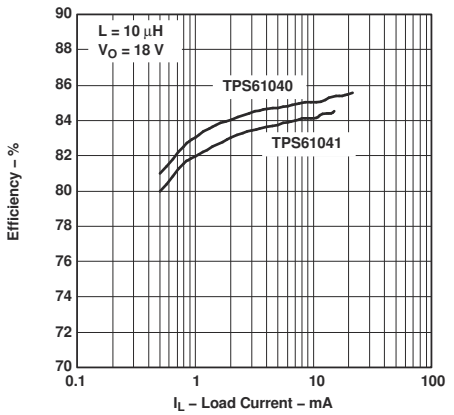


Figure 5-2. Efficiency vs Load Current

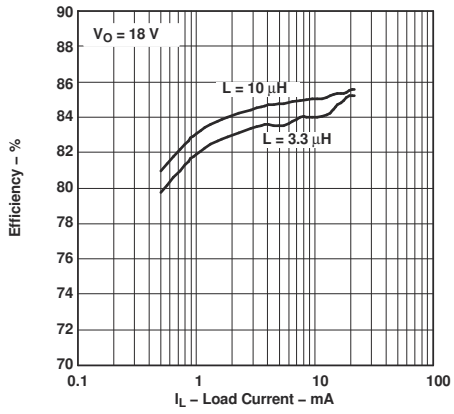


Figure 5-3. Efficiency vs Load Current

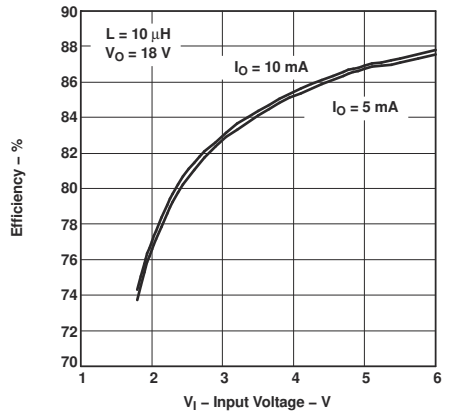


Figure 5-4. Efficiency vs Input Voltage

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5.6 Typical Characteristics (continued)

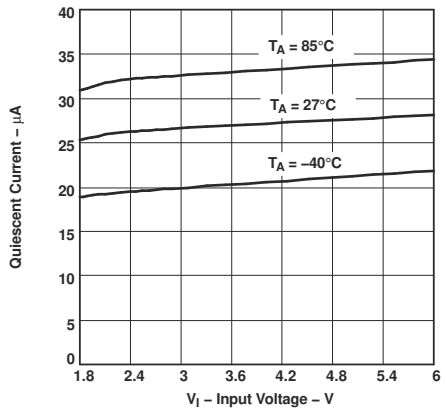


Figure 5-5. TPS61040 Quiescent Current vs Input Voltage

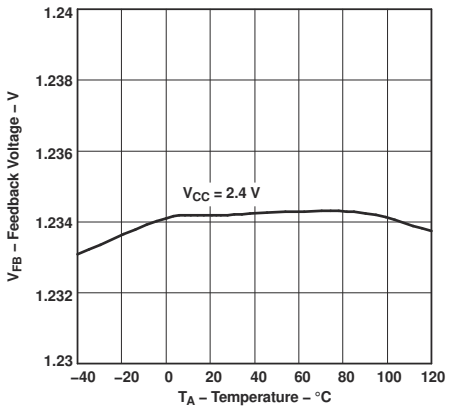


Figure 5-6. Feedback Voltage vs Free-Air Temperature

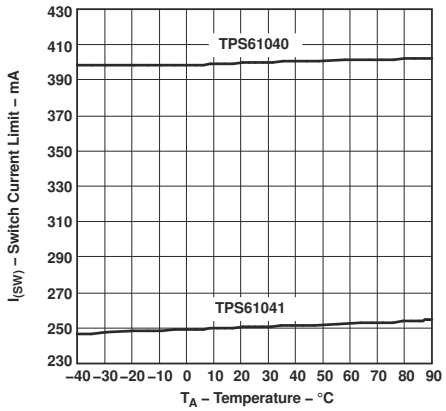


Figure 5-7. TPS6104x Switch Current Limit vs Free-Air Temperature

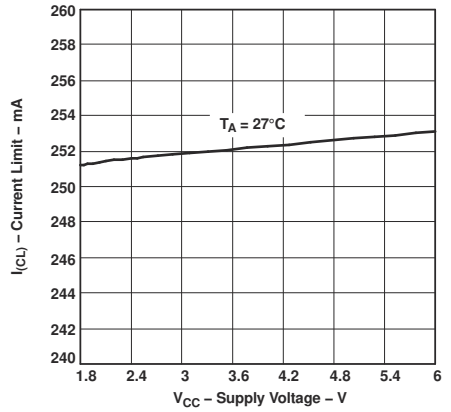


Figure 5-8. TPS61041 Current Limit vs Supply Voltage

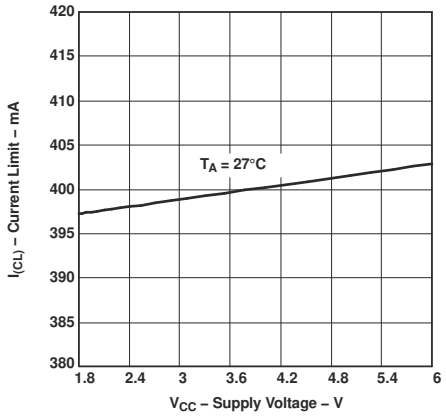


Figure 5-9. TPS61040 Current Limit vs Supply Voltage

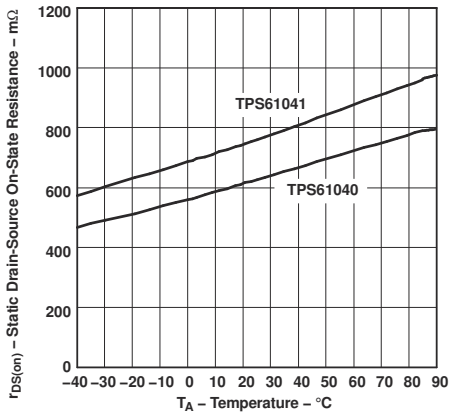


Figure 5-10. TPS6104x Static Drain-Source On-State Resistance vs Free-Air Temperature

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5.6 Typical Characteristics (continued)

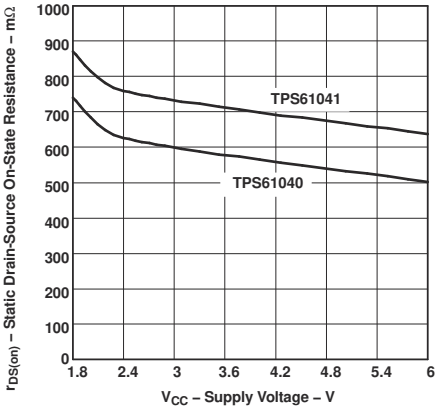


Figure 5-11. TPS6104x Static Drain-Source On-State Resistance vs Supply Voltage

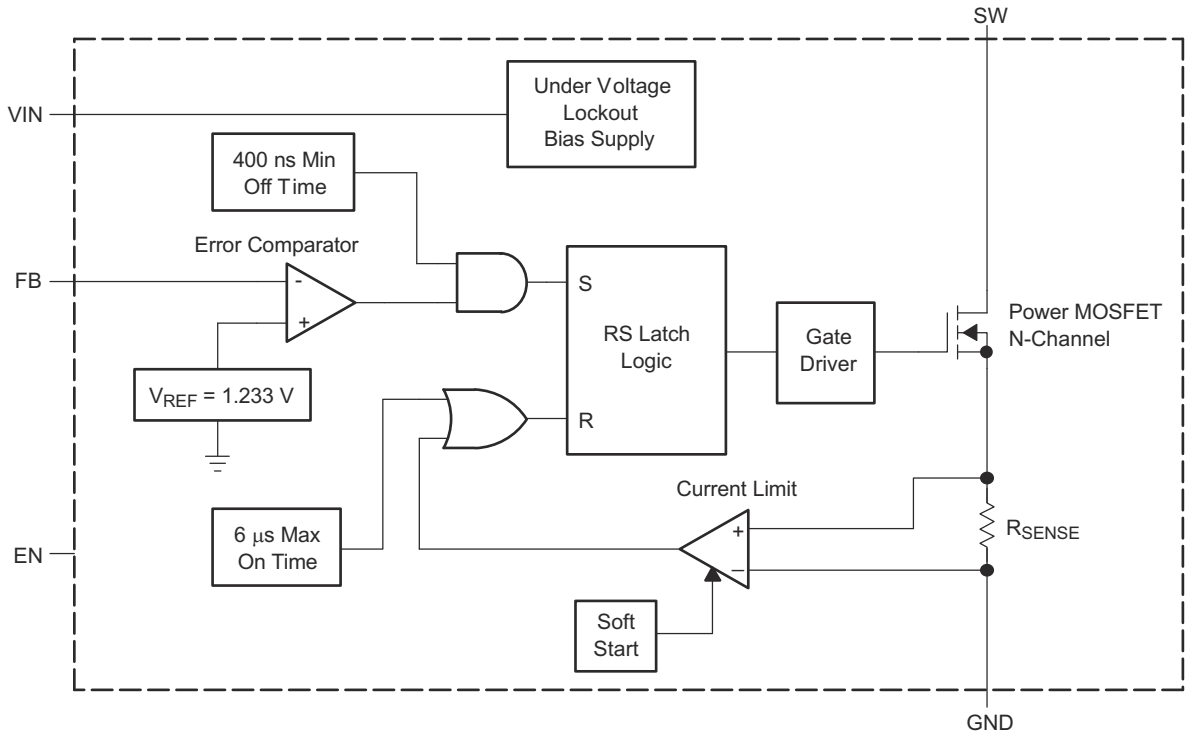
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6 Detailed Description

6.1 Overview

The TPS6104x is a high-frequency boost converter dedicated for small to medium LCD bias supply and white LED backlight supplies. The device is designed to generate output voltages up to 28V from a dual-cell NiMH/ NiCd or a single cell device Li-Ion battery.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Peak Current Control

The internal switch turns on until the inductor current reaches the typical dc current limit (I_{LIM}) of 400mA (TPS61040) or 250mA (TPS61041). Due to the internal propagation delay of typical 100ns, the actual current exceeds the dc current limit threshold by a small amount. The typical peak current limit can be calculated:

$$I_{peak(typ)} = I_{LIM} + \frac{V_{IN}}{L} \times 100\ ns$$

$$I_{peak(typ)} = 400\ mA + \frac{V_{IN}}{L} \times 100\ ns \text{ for the TPS61040-Q1}$$

$$I_{peak(typ)} = 250\ mA + \frac{V_{IN}}{L} \times 100\ ns \text{ for the TPS61041-Q1} \quad (1)$$

The higher the input voltage and the lower the inductor value, the greater the peak.

By selecting the TPS6104x, tailoring the design to the specific application current limit requirements is possible. A lower current limit supports applications requiring lower output power and allows the use of an inductor with a lower current rating and a smaller form factor. A lower current limit typically has a lower output voltage ripple as well.

6.3.2 Soft Start

All inductive step-up converters exhibit high inrush current during start-up if no special precaution is made. This can cause voltage drops at the input rail during start up and must result in an unwanted or early system shut down.

The TPS6104x limits this inrush current by increasing the current limit in two steps starting from $\frac{I_{LIM}}{4}$ for 256 cycles to $\frac{I_{LIM}}{2}$ for the next 256 cycles, and then full current limit (see Figure 7-4).

6.3.3 Enable

Pulling the enable (EN) to ground shuts down the device reducing the shutdown current to 1µA (typical). Because there is a conductive path from the input to the output through the inductor and Schottky diode, the output voltage is equal to the input voltage during shutdown. The enable pin needs to be terminated and must not be left floating. Using a small external transistor disconnects the input from the output during shutdown as shown in Figure 7-6.

6.3.4 Undervoltage Lockout

An undervoltage lockout prevents misoperation of the device at input voltages below typical 1.5V. When the input voltage is below the undervoltage threshold, the main switch is turned off.

6.3.5 Thermal Shutdown

An internal thermal shutdown is implemented and turns off the internal MOSFETs when the typical junction temperature of 168°C is exceeded. The thermal shutdown has a hysteresis of typically 25°C. This data is based on statistical means and is not tested during the regular mass production of the IC.

6.4 Device Functional Modes

6.4.1 Operation

The TPS6104x operates with an input voltage range of 1.8V to 6V and can generate output voltages up to 28V. The device operates in a pulse-frequency-modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range, and with a switching frequency up to 1MHz, the device enables the use of very small external components.

The converter monitors the output voltage, and as soon as the feedback voltage falls below the reference voltage of typically 1.233V, the internal switch turns on and the current ramps up. The switch turns off as soon as the inductor current reaches the internally set peak current of typically 400mA (TPS61040) or 250mA (TPS61041). See *Peak Current Control* for more information. The second criteria that turns off the switch is the maximum on-time of 6µs (typical). This is just to limit the maximum on-time of the converter to cover for extreme conditions. As the switch is turned off the external Schottky diode is forward biased delivering the current to the output. The switch remains off for a minimum of 400ns (typical), or until the feedback voltage drops below the reference voltage again. Using this PFM peak current control scheme the converter operates in discontinuous conduction mode (DCM) where the switching frequency depends on the output current, which results in very high efficiency over the entire load current range. This regulation scheme is inherently stable, allowing a wider selection range for the inductor and output capacitor.

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7 Application and Implementation

Note

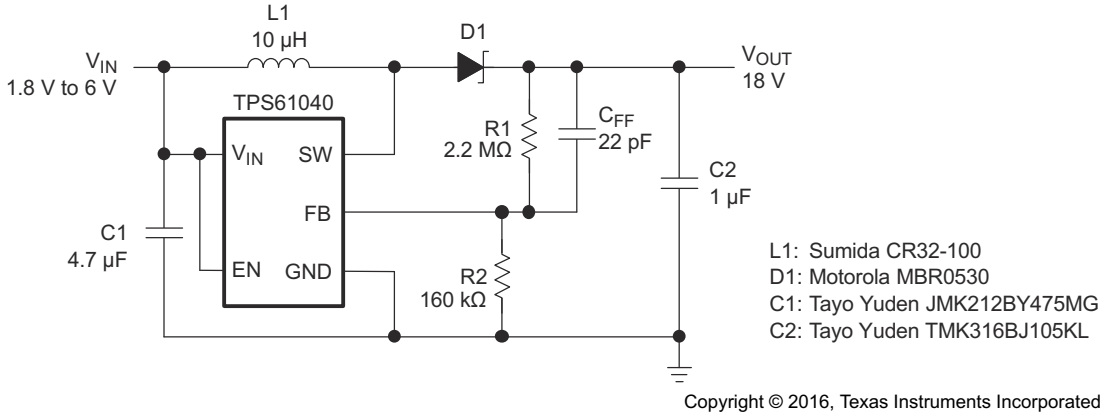
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS6104x is designed for output voltages up to 28V with an input voltage range of 1.8V to 6V and a switch peak current limit of 400mA (250mA for the TPS61041). The device operates in a pulse-frequency-modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range, and with a switching frequency up to 1MHz, the device enables the use of very small external components. The following section provides a step-by-step design approach for configuring the TPS61040 as a voltage regulating boost converter for LCD bias power supply, as shown in Figure 7-1.

7.2 Typical Application

The following section provides a step-by-step design approach for configuring the TPS611040 as a voltage regulating boost converter for LCD bias supply, as shown in Figure 7-1.



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Figure 7-1. LCD Bias Supply

7.2.1 Design Requirements

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage	1.8V to 6V
Output Voltage	18V
Output Current	10mA

7.2.2 Detailed Design Procedure

7.2.2.1 Inductor Selection, Maximum Load Current

Because the PFM peak current control scheme is inherently stable, the inductor value does not affect the stability of the regulator. The selection of the inductor together with the nominal load current, input and output voltage of the application determines the switching frequency of the converter. Depending on the application, inductor values from 2.2 µH to 47µH are recommended. The maximum inductor value is determined by the maximum on time of the switch, typically 6 µs. The peak current limit of 400mA/250mA (typically) must be reached within this 6-µs period for proper operation.

The inductor value determines the maximum switching frequency of the converter. Therefore, select the inductor value that ensures the maximum switching frequency at the converter maximum load current is not exceeded. The maximum switching frequency is calculated by the following formula:

$$f_{S(max)} = \frac{V_{IN(min)} \times (V_{OUT} - V_{IN})}{I_P \times L \times V_{OUT}} \quad (2)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- $V_{IN(min)}$ = The highest switching frequency occurs at the minimum input voltage

If the selected inductor value does not exceed the maximum switching frequency of the converter, the next step is to calculate the switching frequency at the nominal load current using the following formula:

$$f_S(I_{load}) = \frac{2 \times I_{load} \times (V_{OUT} - V_{IN} + V_d)}{I_P^2 \times L} \quad (3)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- I_{load} = Nominal load current
- Vd = Rectifier diode forward voltage (typically 0.3V)

A smaller inductor value gives a higher converter switching frequency, but lowers the efficiency.

The inductor value has less effect on the maximum available load current and is only of secondary order. The best way to calculate the maximum available load current under certain operating conditions is to estimate the expected converter efficiency at the maximum load current. This number can be taken out of the efficiency graphs shown in Figure 5-1 through Figure 5-4. The maximum load current can then be estimated as follows:

$$I_{load(max)} = \eta \frac{I_P^2 \times L \times f_{S(max)}}{2 \times (V_{OUT} - V_{IN})} \quad (4)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- fS_{max} = Maximum switching frequency as calculated previously
- η = Expected converter efficiency. Typically 70% to 85%

The maximum load current of the converter is the current at the operation point where the converter starts to enter the continuous conduction mode. Usually the converter must always operate in discontinuous conduction mode.

Last, the selected inductor must have a saturation current that meets the maximum peak current of the converter (as calculated in *Peak Current Control*). Use the maximum value for I_{LIM} for this calculation.

Another important inductor parameter is the dc resistance. The lower the dc resistance, the higher the efficiency of the converter. See Table 7-2 and the typical applications for the inductor selection.

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Table 7-2. Recommended Inductor for Typical LCD Bias Supply (see Figure 10-1)

DEVICE	INDUCTOR VALUE	COMPONENT SUPPLIER(1)	COMMENTS
TPS61040	10µH	Sumida CR32-100	High efficiency
	10µH	Sumida CDRH3D16-100	High efficiency
	10µH	Murata LQH4C100K04	High efficiency
	4.7µH	Sumida CDRH3D16-4R7	Small design size
	4.7µH	Murata LQH3C4R7M24	Small design size
TPS61041	10µH	Murata LQH3C100K24	High efficiency Small design size

(1) See *Third-Party Products* disclaimer

7.2.2.2 Setting the Output Voltage

The output voltage is calculated as:

$$V_{OUT} = 1.233\ V \times \left(1 + \frac{R1}{R2}\right) \quad (5)$$

For battery-powered applications, a high-impedance voltage divider must be used with a typical value for R2 of ≤200kΩ and a maximum value for R1 of 2.2MΩ. Smaller values might be used to reduce the noise sensitivity of the feedback pin.

A feedforward capacitor across the upper feedback resistor R1 is required to provide sufficient overdrive for the error comparator. Without a feedforward capacitor, or one whose value is too small, the TPS6104x shows *double pulses* or a pulse burst instead of single pulses at the switch node (SW), causing higher output voltage ripple. If this higher output voltage ripple is acceptable, the feedforward capacitor can be left out.

The lower the switching frequency of the converter, the larger the feedforward capacitor value required. A good starting point is to use a 10pF feedforward capacitor. As a first estimation, the required value for the feedforward capacitor at the operation point can also be calculated using the following formula:

$$C_{FF} = \frac{1}{2 \times \pi \times \frac{fS}{20} \times R1} \quad (6)$$

where

- R1 = Upper resistor of voltage divider
- fS = Switching frequency of the converter at the nominal load current (See *Inductor Selection, Maximum Load Current* for calculating the switching frequency)
- C_{FF} = Choose a value that comes closest to the result of the calculation

The larger the feedforward capacitor the worse the line regulation of the device. Therefore, when concern for line regulation is paramount, the selected feedforward capacitor must be as small as possible. See the following section for more information about line and load regulation.

7.2.2.3 Line and Load Regulation

The line regulation of the TPS6104x depends on the voltage ripple on the feedback pin. Typically, a 50mV peak-to-peak voltage ripple on the feedback pin FB gives good results.

Some applications require a very tight line regulation and can only allow a small change in output voltage over a certain input voltage range. If no feedforward capacitor C_{FF} is used across the upper resistor of the voltage feedback divider, the device has the best line regulation. Without the feedforward capacitor the output voltage ripple is higher because the TPS6104x shows output voltage bursts instead of single pulses on the switch pin (SW), increasing the output voltage ripple. Increasing the output capacitor value reduces the output voltage ripple.

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If a larger output capacitor value is not an option, a feed-forward capacitor C_{FF} can be used as described in the previous section. The use of a feedforward capacitor increases the amount of voltage ripple present on the feedback pin (FB). The greater the voltage ripple on the feedback pin (≥50mV), the worse the line regulation. There are two ways to improve the line regulation further:

1. Use a smaller inductor value to increase the switching frequency, which lowers the output voltage ripple, as well as the voltage ripple on the feedback pin.
2. Add a small capacitor from the feedback pin (FB) to ground to reduce the voltage ripple on the feedback pin down to 50mV again. As a starting point, the same capacitor value as selected for the feedforward capacitor C_{FF} can be used.

7.2.2.4 Output Capacitor Selection

For best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value but tantalum capacitors can be used as well, depending on the application.

Assuming the converter does not show double pulses or pulse bursts on the switch node (SW), the output voltage ripple can be calculated as:

$$\Delta V_{out} = \frac{I_{out}}{C_{out}} \times \left(\frac{1}{fS(Iout)} - \frac{I_P \times L}{Vout + Vd - Vin} \right) + I_P \times ESR \quad (7)$$

where

- I_P = Peak current as described in *Peak Current Control*
- L = Selected inductor value
- I_{out} = Nominal load current
- fS (I_{out}) = Switching frequency at the nominal load current as calculated previously
- Vd = Rectifier diode forward voltage (typically 0.3V)
- C_{out} = Selected output capacitor
- ESR = Output capacitor ESR value

See Table 7-3 and the *Typical Application* for choosing the output capacitor.

Table 7-3. Recommended Input and Output Capacitors

DEVICE	CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER(1)	COMMENTS
TPS6104x	4.7µF/X5R/0805	6.3V	Tayo Yuden JMK212BY475MG	C_{IN}/C_{OUT}
	10µF/X5R/0805	6.3V	Tayo Yuden JMK212BJ106MG	C_{IN}/C_{OUT}
	1µF/X7R/1206	25V	Tayo Yuden TMK316BJ105KL	C_{OUT}
	1µF/X5R/1206	35V	Tayo Yuden GMK316BJ105KL	C_{OUT}
	4.7µF/X5R/1210	25V	Tayo Yuden TMK325BJ475MG	C_{OUT}

(1) See *Third-Party Products* disclaimer.

7.2.2.5 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 4.7µF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering this value can be increased. See Table 7-3 and typical applications for input capacitor recommendations.

7.2.2.6 Diode Selection

To achieve high efficiency a Schottky diode must be used. The current rating of the diode must meet the peak current rating of the converter as it is calculated in *Peak Current Control*. Use the maximum value for I_{LIM} for this calculation. See Table 7-4 and the typical applications for the selection of the Schottky diode.

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Table 7-4. Recommended Schottky Diode for Typical LCD Bias Supply (see Figure 10-1)

DEVICE	REVERSE VOLTAGE	COMPONENT SUPPLIER(1)	COMMENTS
TPS6104x	30V	ON Semiconductor MBR0530	
	20V	ON Semiconductor MBR0520	
	20V	ON Semiconductor MBRM120L	High efficiency
	30V	Toshiba CRS02	

(1) See *Third-Party Products* disclaimer.

7.2.3 Application Curves

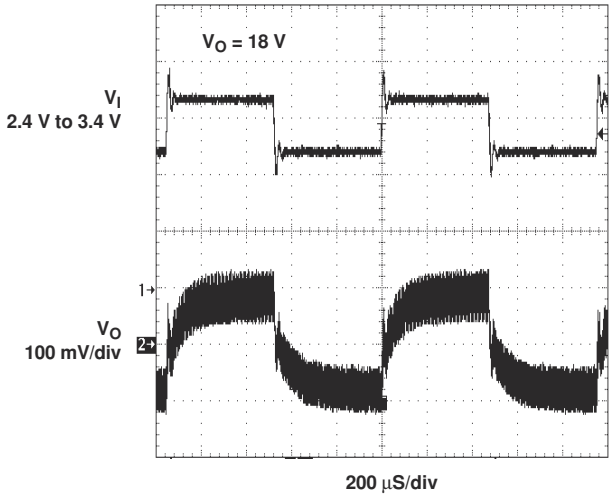


Figure 7-2. Line Transient Response

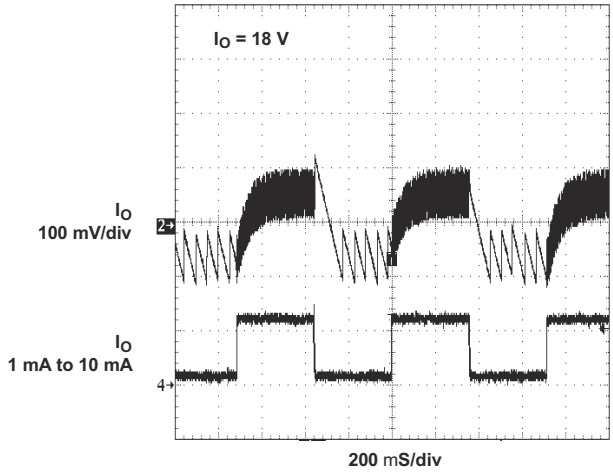


Figure 7-3. Load Transient Response

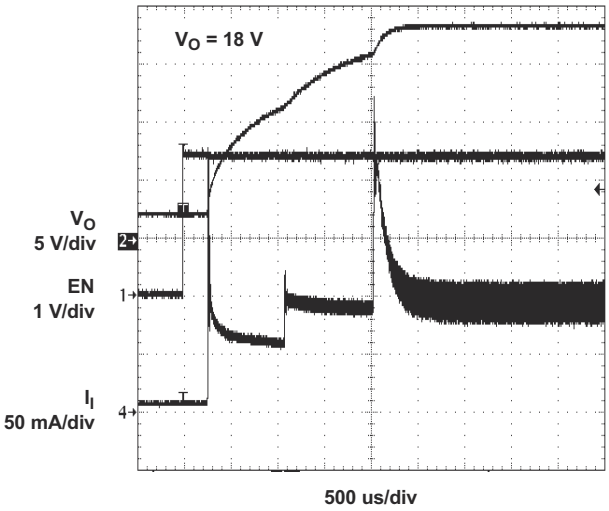
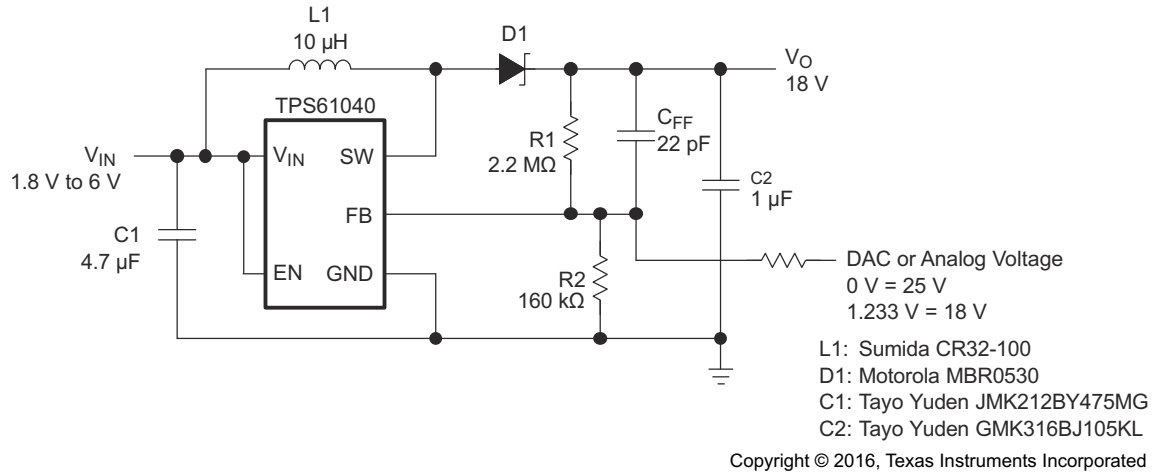


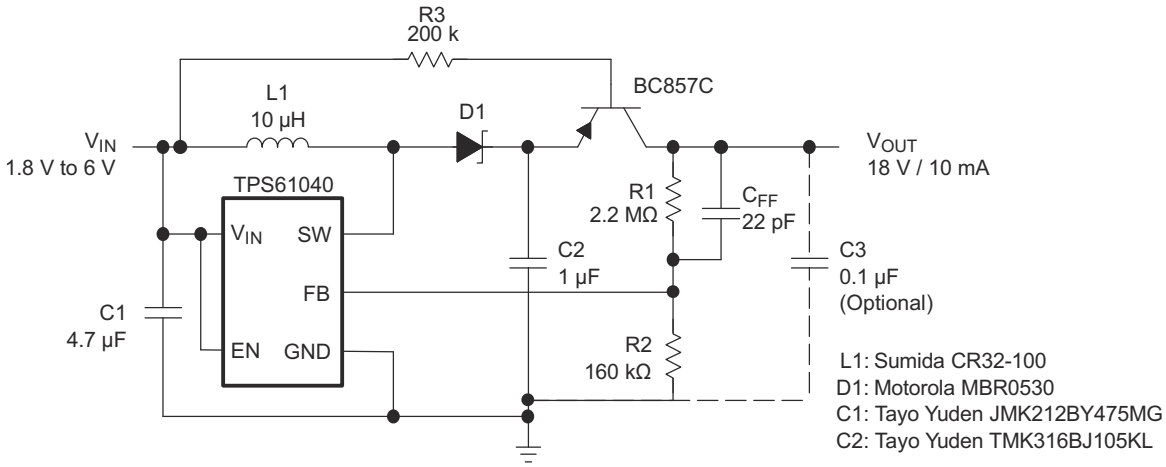
Figure 7-4. Start-Up Behavior

7.3 System Examples



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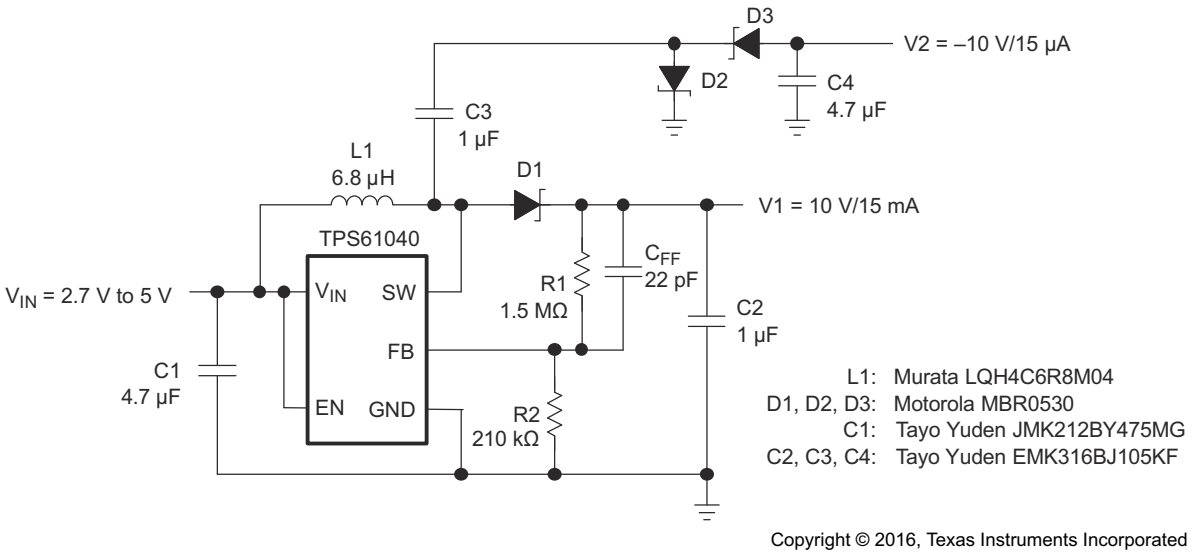
Figure 7-5. LCD Bias Supply With Adjustable Output Voltage



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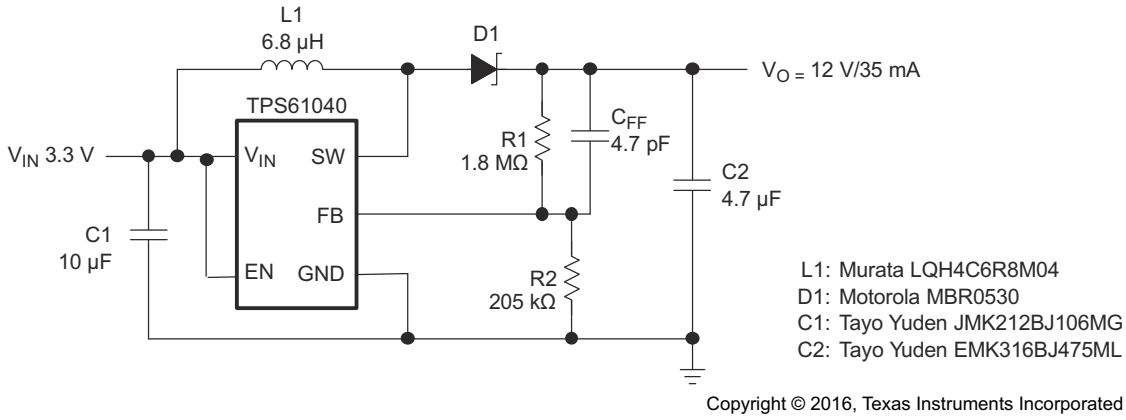
Figure 7-6. LCD Bias Supply With Load Disconnect

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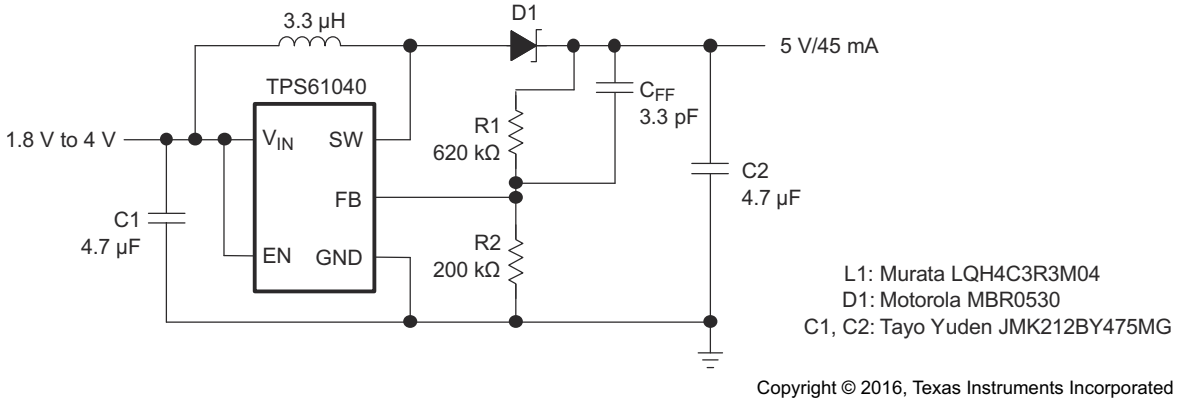
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Figure 7-7. Positive and Negative Output LCD Bias Supply



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Figure 7-8. Standard 3.3V to 12V Supply



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Figure 7-9. Dual Battery Cell to 5V/50mA Conversion Efficiency Approximately Equals 84% at V_{IN} = 2.4V to Vo = 5V/45mA

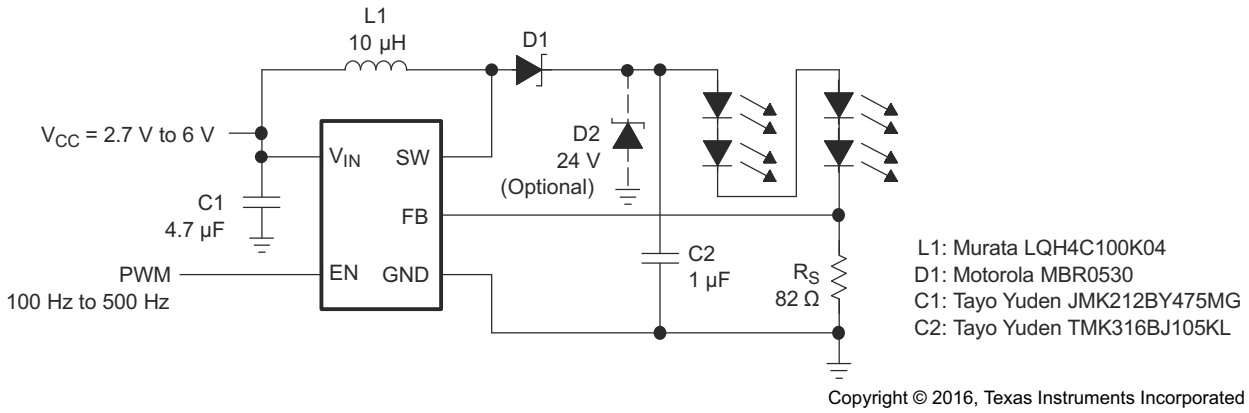
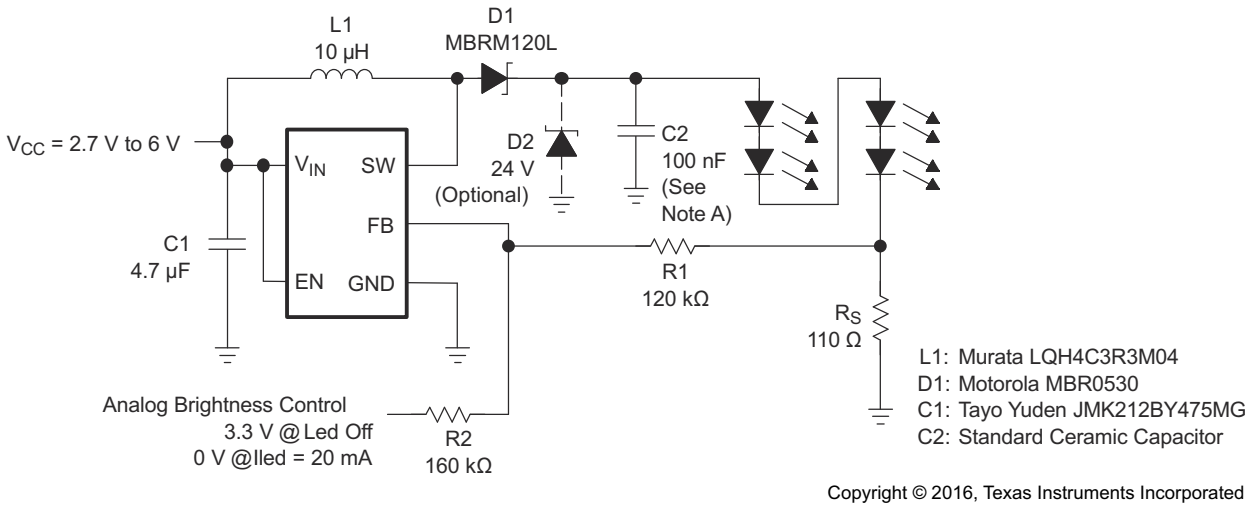


Figure 7-10. White LED Supply With Adjustable Brightness Control Using a PWM Signal on the Enable Pin, Efficiency Approximately Equals 86% at V_{IN} = 3V, I_{LED} = 15mA



A. A smaller output capacitor value for C2 causes a larger LED ripple.

Figure 7-11. White LED Supply With Adjustable Brightness Control Using an Analog Signal on the Feedback Pin

7.4 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8V and 6V. The output current of the input power supply must be rated according to the supply voltage, output voltage and output current of TPS6104x.

7.5 Layout

7.5.1 Layout Guidelines

Typical for all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

The input capacitor must be placed as close as possible to the input pin for good input voltage filtering. The inductor and diode must be placed as close as possible to the switch pin to minimize the noise coupling into other circuits. Because the feedback pin and network is a high-impedance circuit, the feedback network must be routed away from the inductor. The feedback pin and feedback network must be shielded with a ground plane or trace to minimize noise coupling into this circuit.

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Wide traces must be used for connections in bold as shown in Figure 7-12. A star ground connection or ground plane minimizes ground shifts and noise.

7.5.2 Layout Example

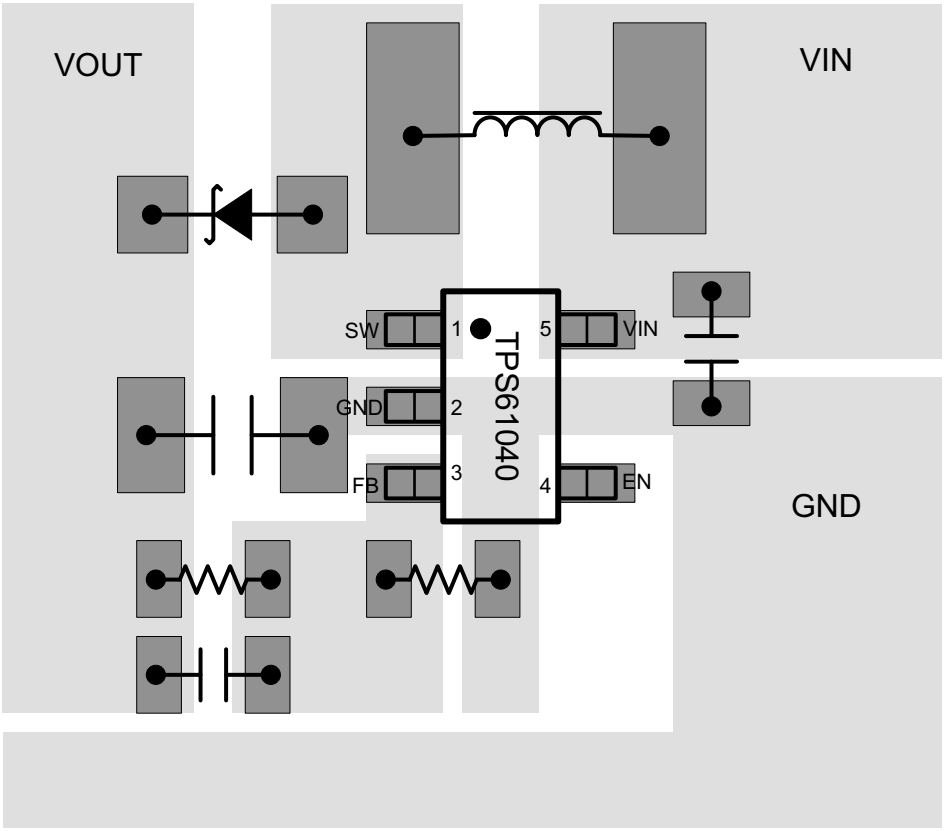


Figure 7-12. Layout Diagram

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

Changes from Revision K (July 2022) to Revision L (August 2026)	Page
• Changed switch voltage on pin SW MIN value from 30 to –0.3	4

Changes from Revision J (December 2019) to Revision K (July 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision I (December 2016) to Revision J (December 2019)	Page
• Changed DRV package pinout image to show thermal pad outline and transparent top view	3

Changes from Revision H (October 2015) to Revision I (December 2016)	Page
• Changed C_{IN} from: 4.7mF To: 4.7µF and C_O From: 1mF To: 1µF in the *Typical Application Schematic*	1

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Changes from Revision G (December 2014) to Revision H (October 2015)	Page
• Added 500µs/div label to X-axis of Figure 7-4.	15

Changes from Revision F (December 2010) to Revision G (December 2014)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61040DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PHOI
TPS61040DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PHOI
TPS61040DDCR	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXK
TPS61040DDCR.B	Active	Production	SOT-23-THIN (DDC) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXK
TPS61040DDCT	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXK
TPS61040DDCT.B	Active	Production	SOT-23-THIN (DDC) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	QXK
TPS61040DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CCL
TPS61040DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CCL
TPS61040DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCL
TPS61040DRVRG4.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CCL
TPS61040DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CCL
TPS61040DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CCL
TPS61040DRVTG4	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CCL
TPS61041DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PHPI
TPS61041DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHPI
TPS61041DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	CAW
TPS61041DRVR.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	CAW
TPS61041DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CAW
TPS61041DRVRG4.B	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CAW
TPS61041DRVT	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	CAW
TPS61041DRVT.B	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	CAW
TPS61041DRVTG4	Active	Production	WSON (DRV) | 6	250 | SMALL T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	CAW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

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OTHER QUALIFIED VERSIONS OF TPS61040, TPS61041 :

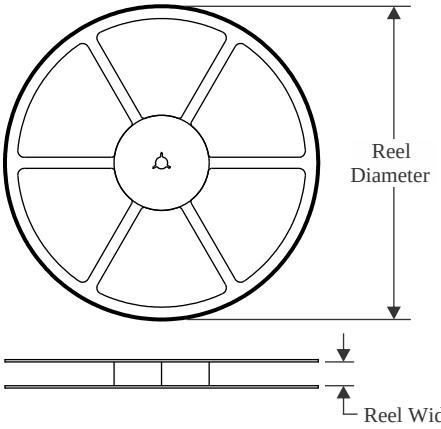
- Automotive : TPS61040-Q1, TPS61041-Q1

NOTE: Qualified Version Definitions:

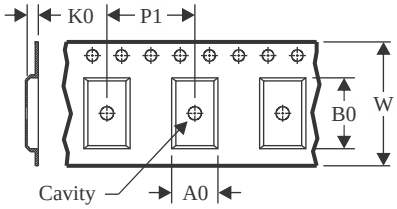
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

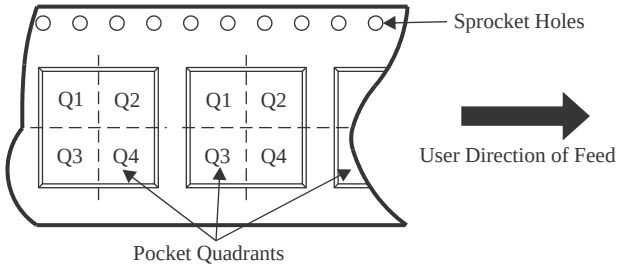


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

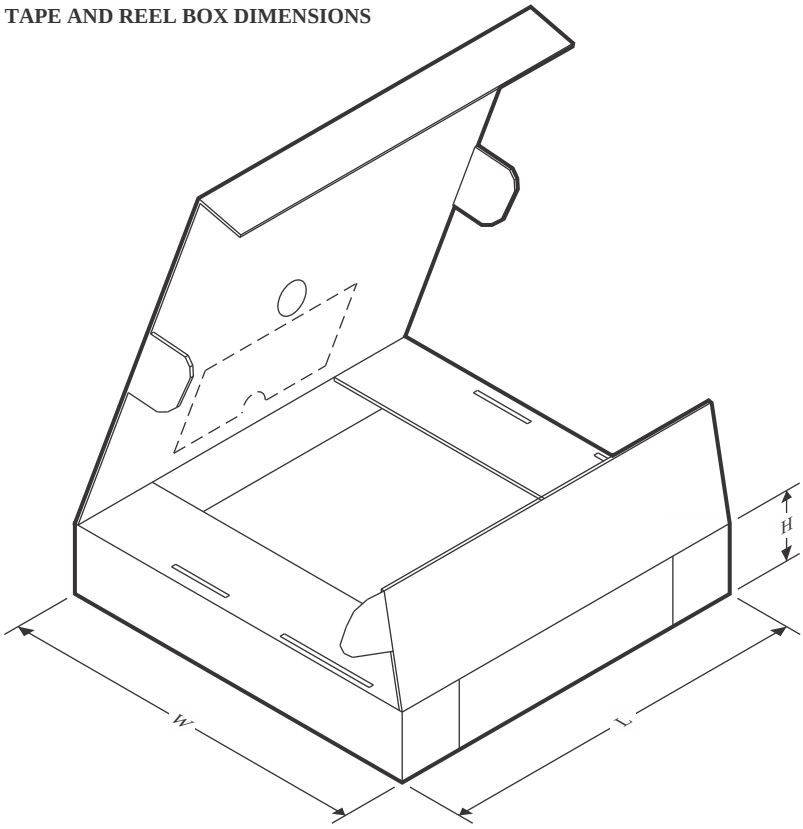
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61040DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS61040DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS61040DDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS61040DDCT	SOT-23-THIN	DDC	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS61040DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61040DRVRG4	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61040DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61041DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS61041DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61041DRVRG4	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61041DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS61041DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

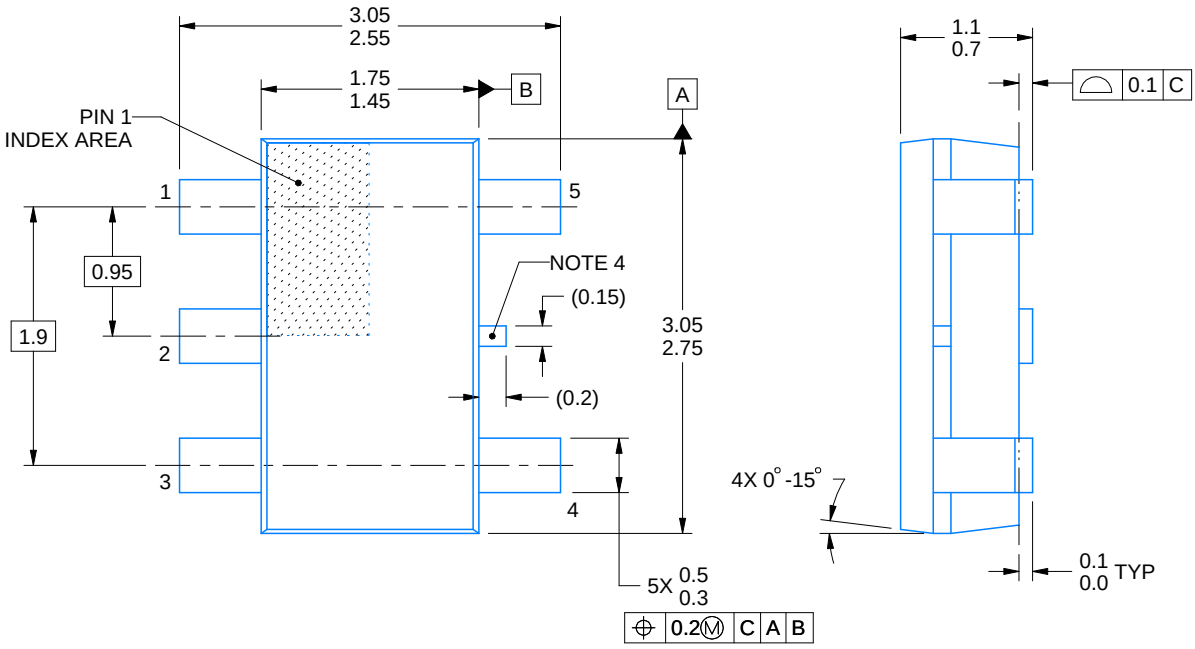
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61040DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS61040DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS61040DDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
TPS61040DDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
TPS61040DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS61040DRVRG4	WSON	DRV	6	3000	205.0	200.0	33.0
TPS61040DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS61041DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS61041DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS61041DRVRG4	WSON	DRV	6	3000	205.0	200.0	33.0
TPS61041DRVT	WSON	DRV	6	250	205.0	200.0	33.0
TPS61041DRVT	WSON	DRV	6	250	203.0	203.0	35.0

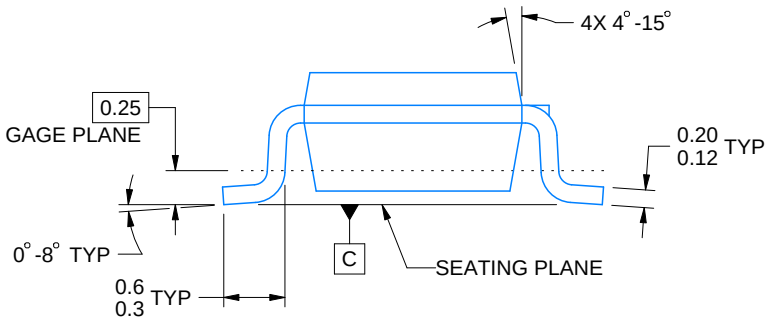
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

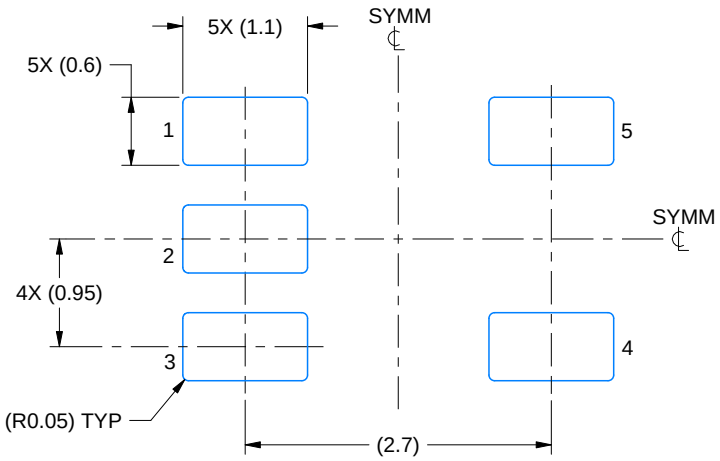




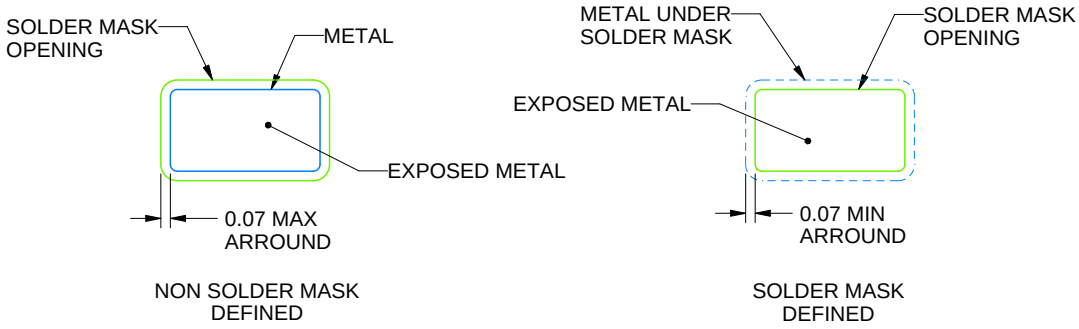
4220752/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

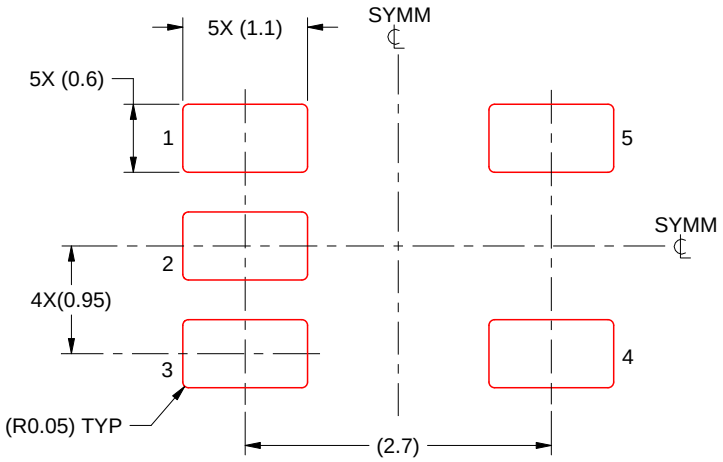


SOLDERMASK DETAILS

4220752/C 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4220752/C 08/2024

NOTES: (continued)

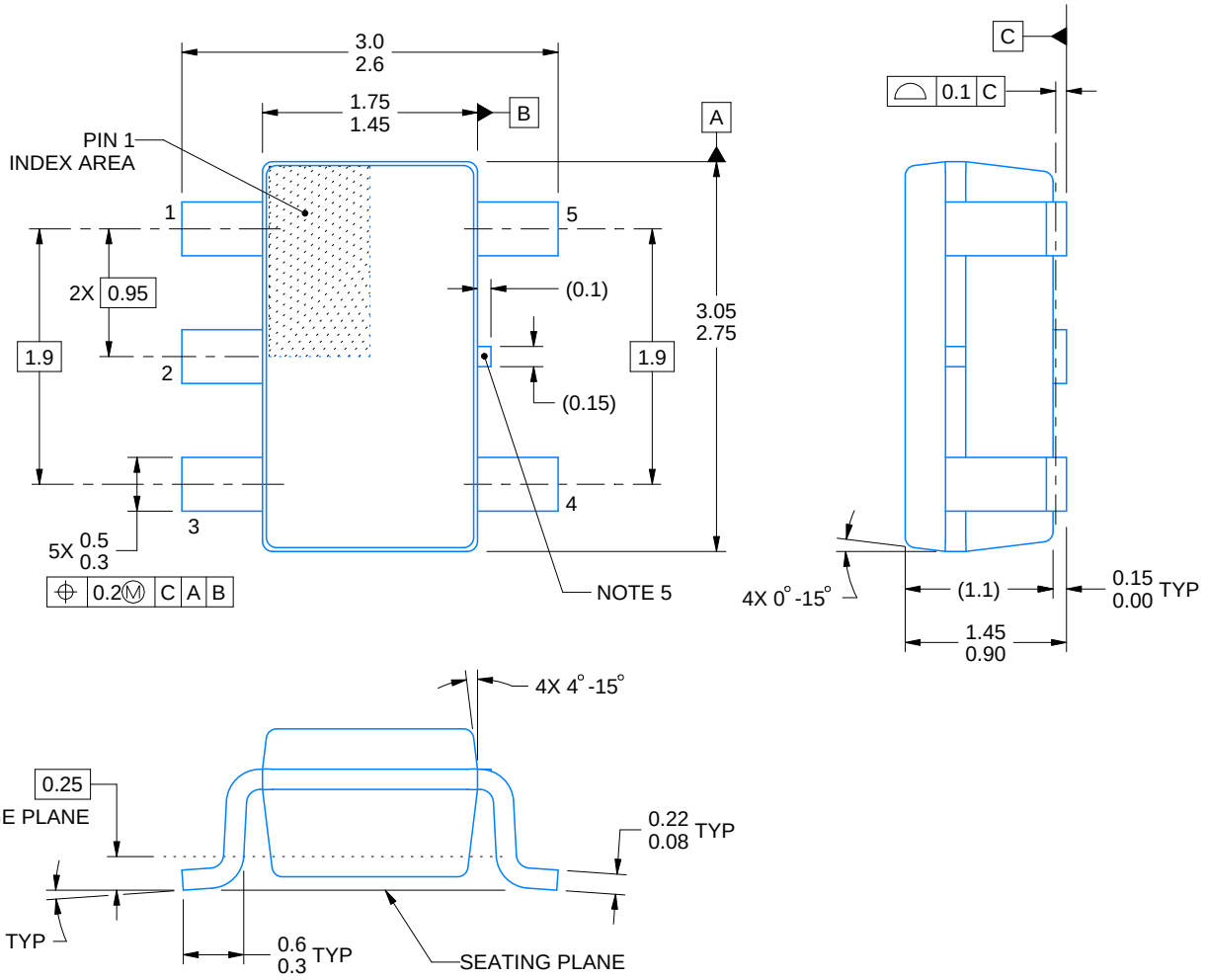
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

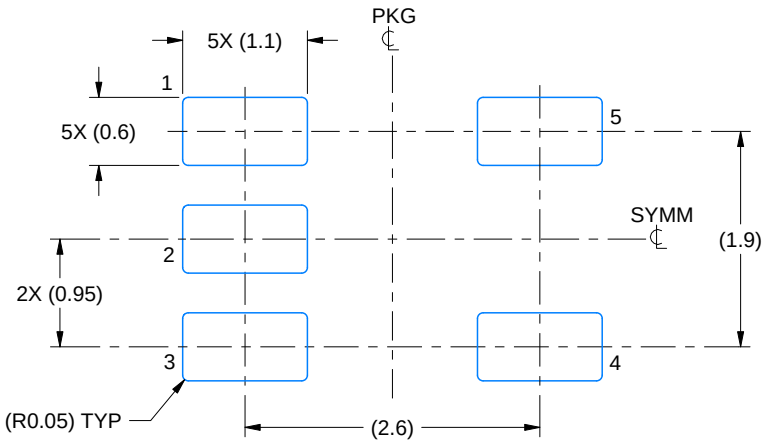
SMALL OUTLINE TRANSISTOR



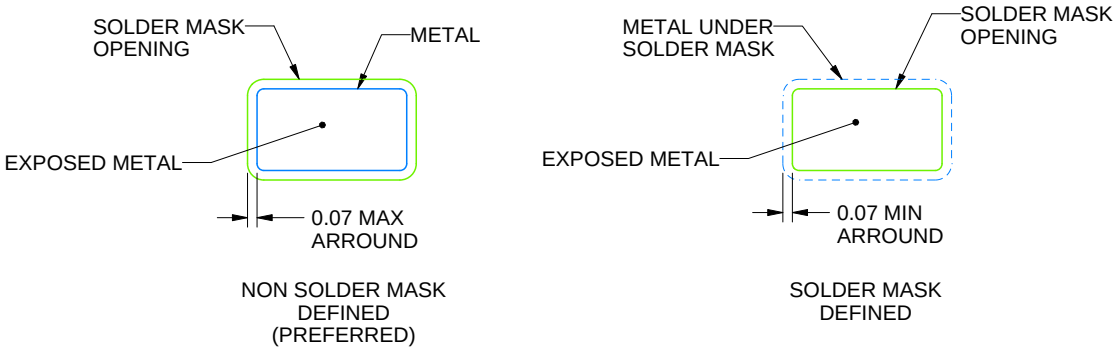
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

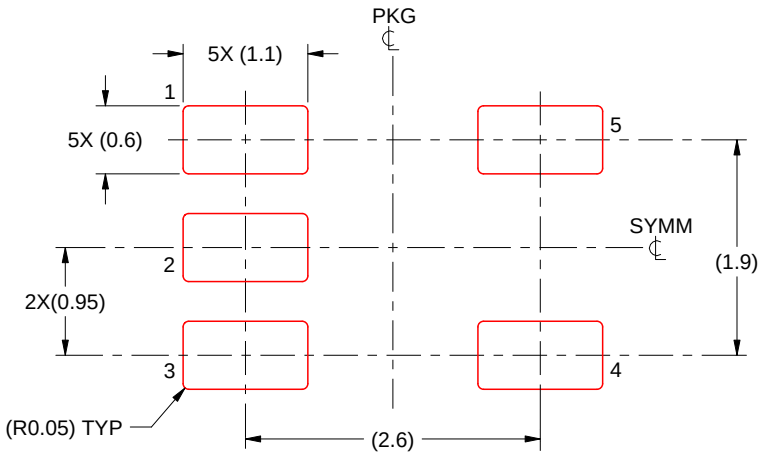


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

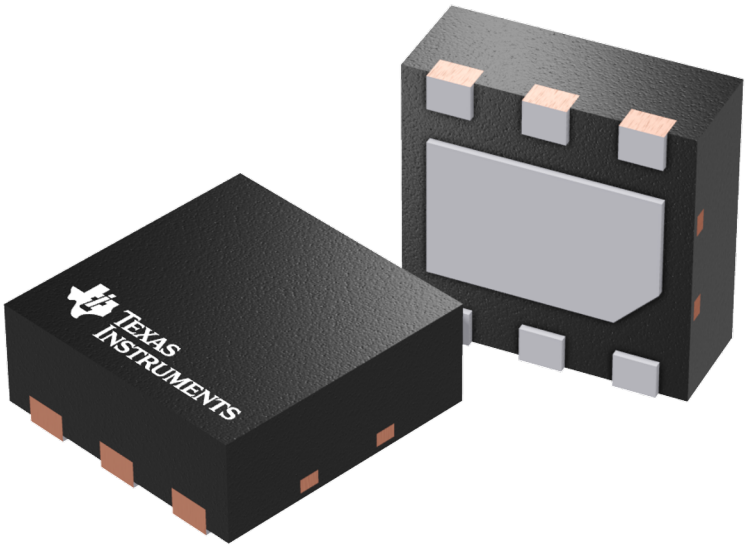
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



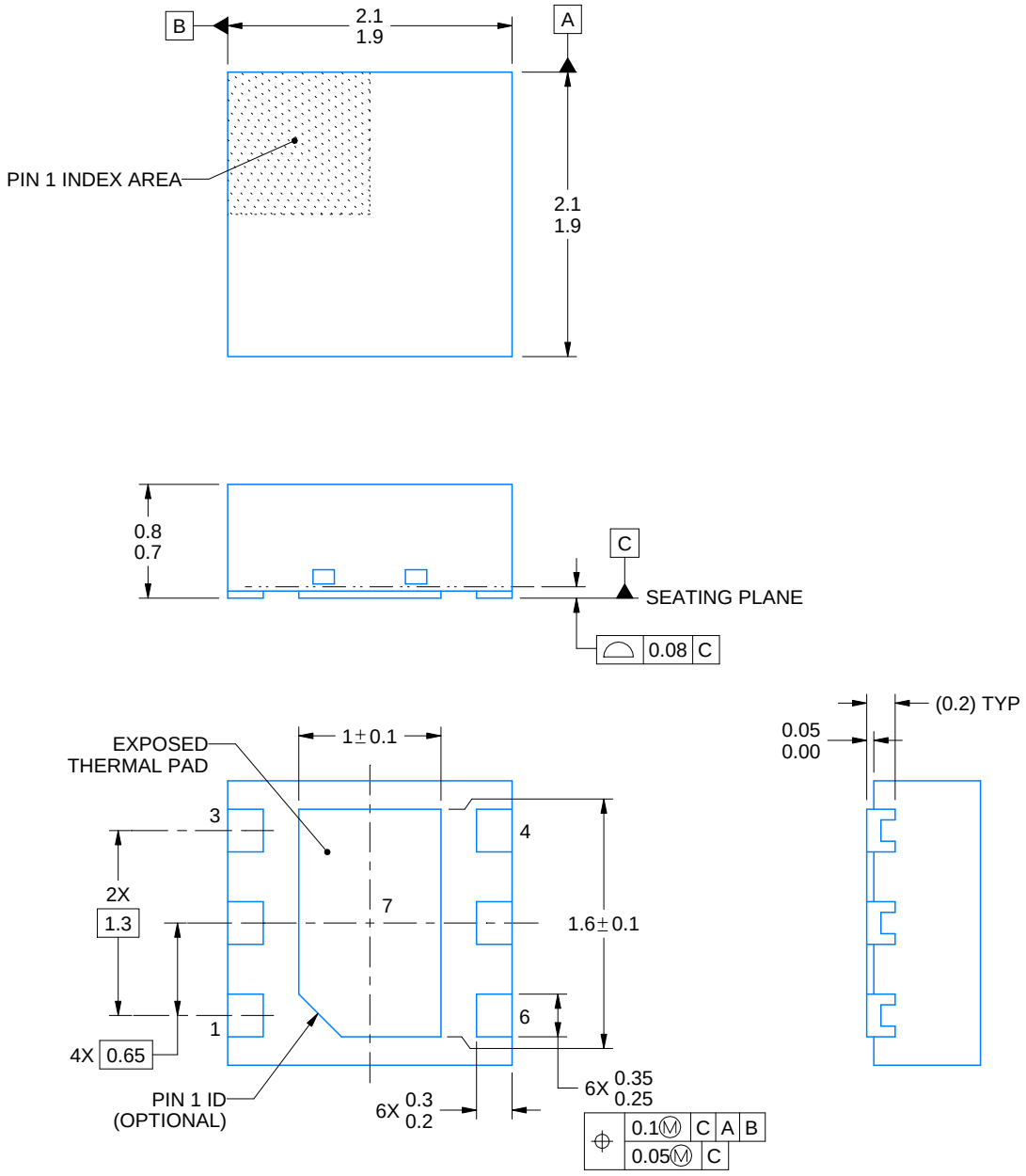
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

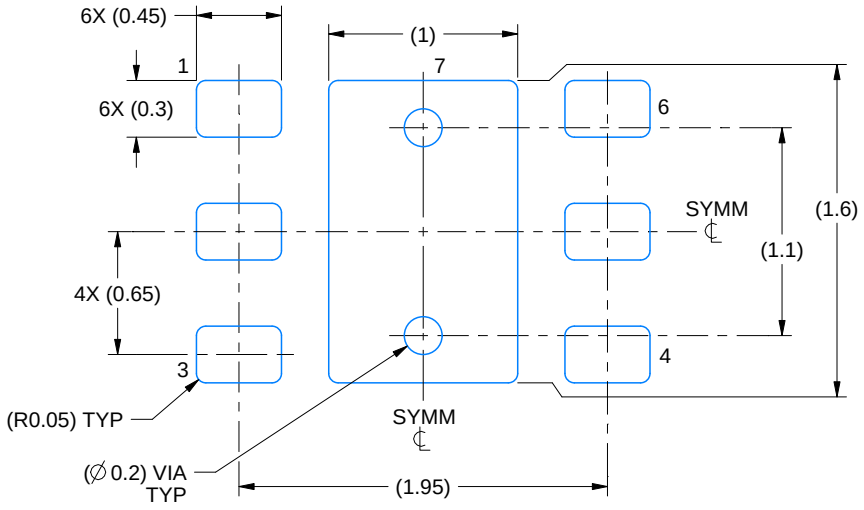
PLASTIC SMALL OUTLINE - NO LEAD



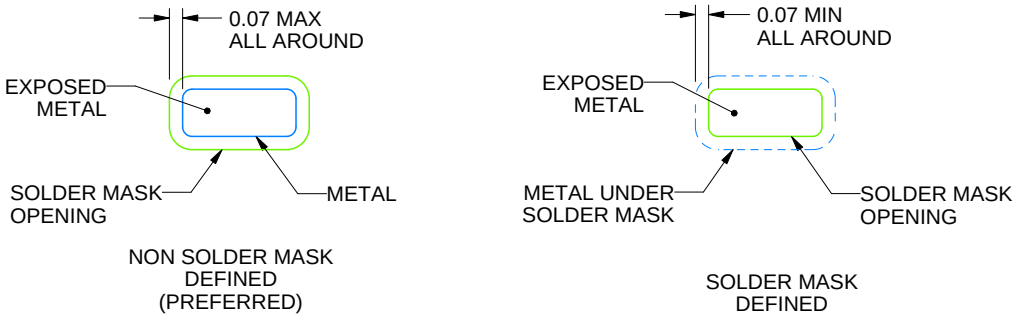
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

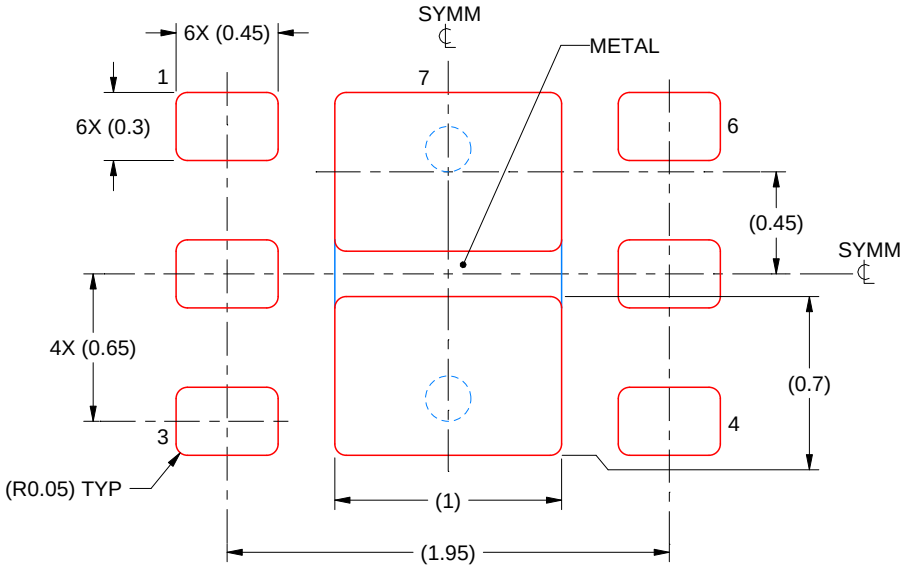


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



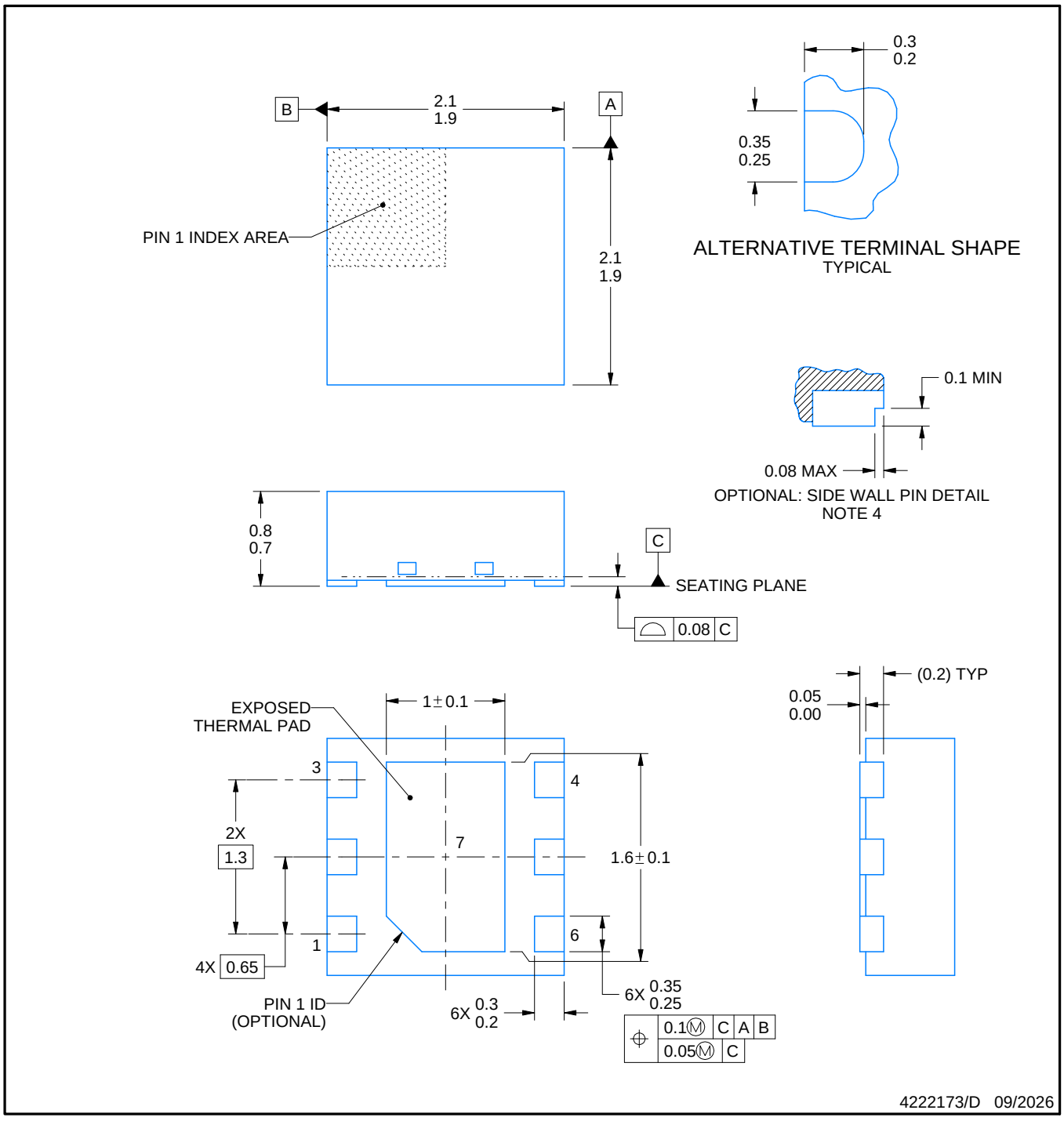
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

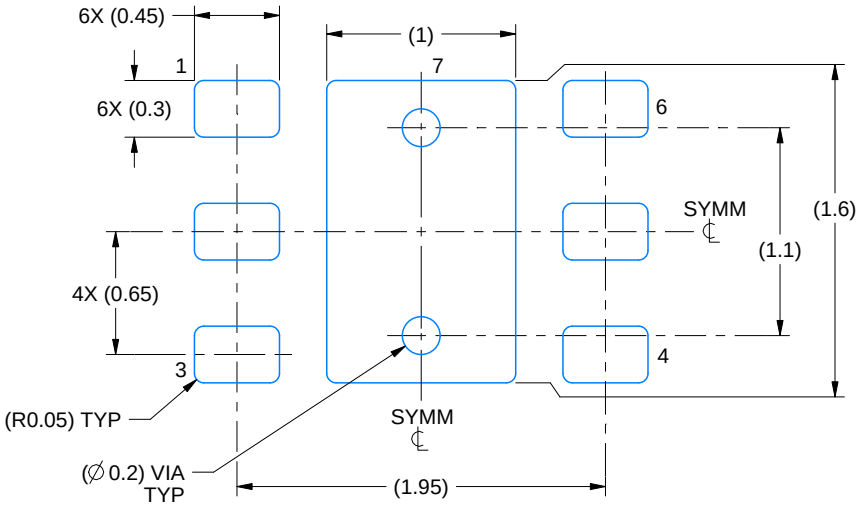
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

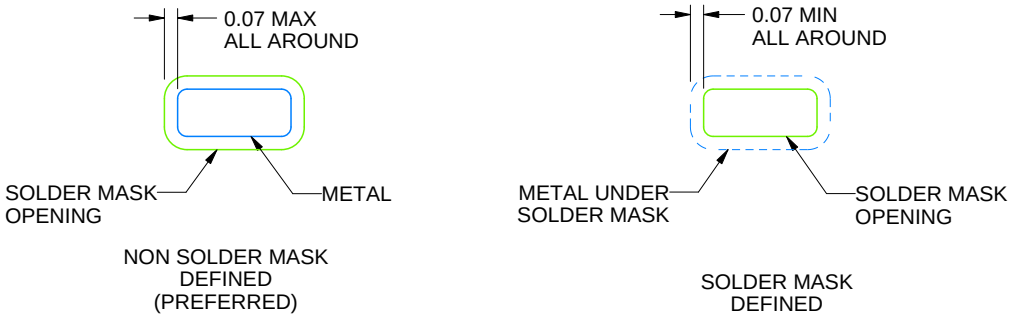


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X

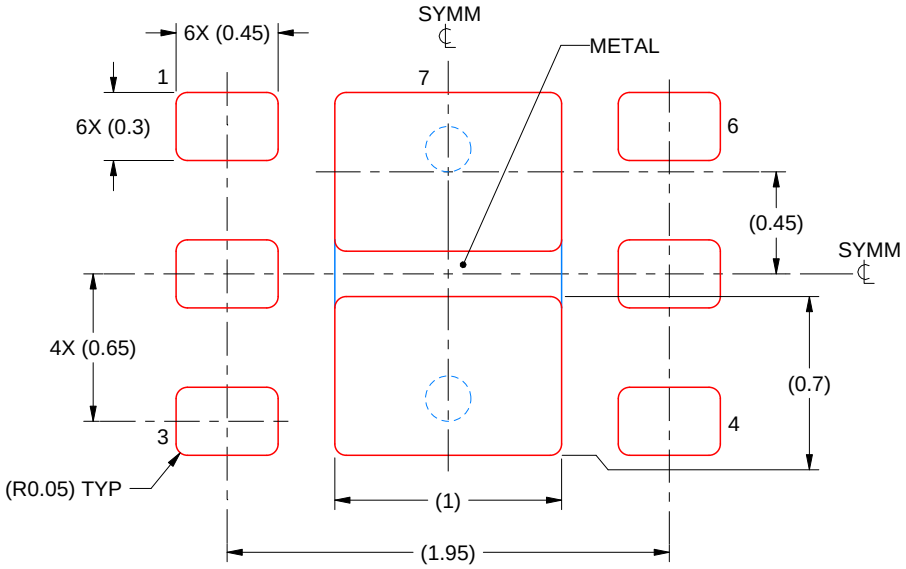


SOLDER MASK DETAILS

4222173/D 09/2026

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/D 09/2026

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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