TEXAS INSTRUMENTS
TPS61089, TPS610891
SLVSD38C – NOVEMBER 2015 – REVISED AUGUST 2021

TPS61089x 12.6-V, 7-A Fully-Integrated Synchronous Boost Converters in 2.0-mm x 2.5-mm VQFN Package

1 Features

- Input voltage range: 2.7 V to 12 V
- Output voltage range: 4.5 V to 12.6 V
- Up to 90% efficiency at V_{IN} = 3.3 V, V_{OUT} = 9 V, and I_{OUT} = 2 A
- Resistor-programmable peak current limit up to 10 A for high pulse current
- Adjustable switching frequency: 200 kHz to 2.2 MHz
- 4-ms built-in soft start time
- PFM operation mode at light load (TPS61089)
- Forced PWM operation mode at light load (TPS610891)
- Internal output overvoltage protection at 13.2 V
- Cycle-by-cycle overcurrent protection
- Thermal shutdown
- 2.00-mm × 2.50-mm VQFN HotRod™ package
- Create a custom design using the TPS61089x with the WEBENCH® Power Designer

2 Applications

- Bluetooth™ speaker
- Quick charge power bank
- Portable POS terminal

3 Description

The TPS61089x represents the TPS61089 and the TPS610891. The TPS61089x is a fully-integrated synchronous boost converter with a 19-mΩ main power switch and a 27-mΩ rectifier switch. The device provides a high-efficiency and small-size power solution for portable equipment. The TPS61089x features a wide input voltage range from 2.7 V to 12 V to support applications powered with single-cell or two-cell Lithium ion/polymer batteries. The TPS61089x has 7-A continuous switch current capability and provides output voltage up to 12.6 V.

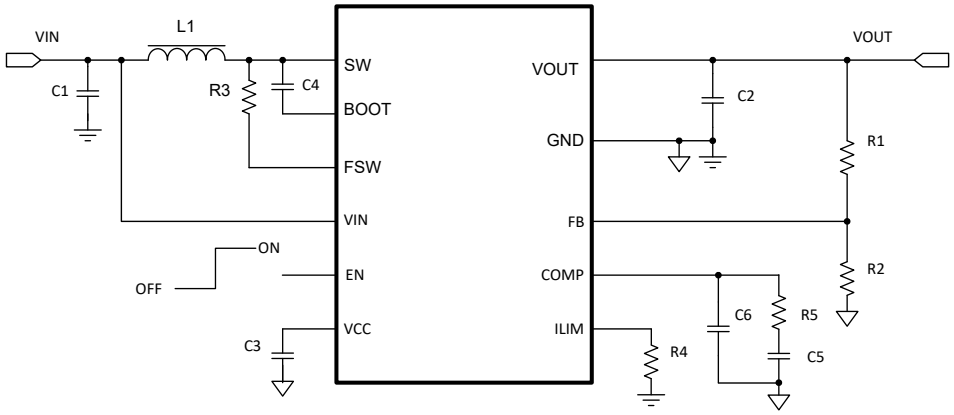
The TPS61089x uses adaptive constant off-time peak current control topology to regulate the output voltage. In moderate to heavy load condition, the TPS61089x works in the pulse width modulation (PWM) mode. In light load condition, the TPS61089 works in the pulse frequency modulation (PFM) mode to improve the efficiency, while the TPS610891 still works in the PWM mode to avoid application problems caused by low switching frequency. The switching frequency in PWM mode is adjustable from 200 kHz to 2.2 MHz. The TPS61089x also implements a built-in 4-ms soft start function and an adjustable peak switch current limit function. In addition, the device provides 13.2-V output overvoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.

The TPS61089x is available in an extremely compact size of a 2.0-mm × 2.5-mm 11-pin VQFN package.

Device Information Table

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS61089x	VQFN (11)	2.00 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Typical Application Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2016) to Revision C (August 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document.	1
• Corrected grammar and numeric format throughout document	1
• Added WEBENCH links	1

Changes from Revision A (April 2016) to Revision B (July 2016)	Page
• Changed x axis in	7
• Changed x axis in	7

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5 Device Comparison Table

PART NUMBER	OPERATION MODE AT LIGHT LOAD
TPS61089RNR	PFM
TPS610891RNR(1)	Forced PWM

(1) Product Preview. Contact TI factory for more information.

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6 Pin Configuration and Functions

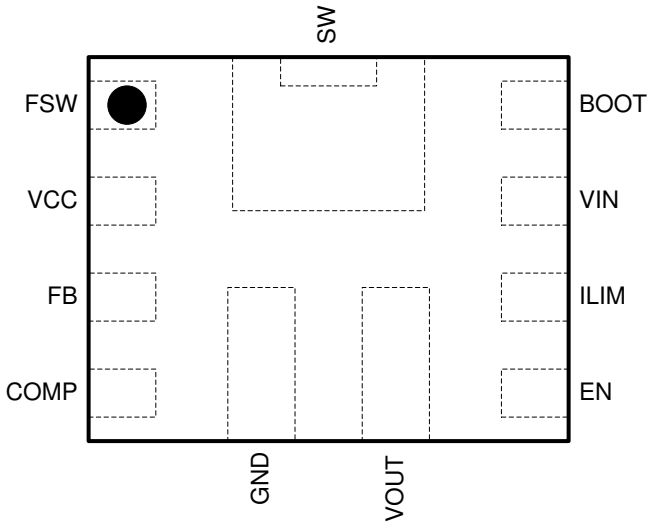


Figure 6-1. 11-Pin VQFN With Thermal Pad RNR Package (Top View)

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
FSW	1	I	The switching frequency is programmed by a resister between this pin and the SW pin.
VCC	2	O	Output of the internal regulator. A ceramic capacitor of more than 1.0 µF is required between this pin and ground.
FB	3	I	Output voltage feedback
COMP	4	O	Output of the internal error amplifier. The loop compensation network should be connected between this pin and the GND pin.
GND	5	PWR	Ground
VOUT	6	PWR	Boost converter output
EN	7	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode.
ILIM	8	O	Adjustable switching peak current limit. An external resister should be connected between this pin and the GND pin.
VIN	9	I	IC power supply input
BOOT	10	O	Power supply for high-side MOSFET gate driver. A capacitor must be connected between this pin and the SW pin
SW	11	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage at terminals(2)	BOOT	–0.3	SW + 7	V
	VIN, SW, FSW, VOUT	–0.3	14.5	
	EN, VCC, COMP	–0.3	7	
	ILIM, FB	–0.3	3.6	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		12	V
V_{OUT}	Output voltage range	4.5		12.6	V
L	Inductance, effective value	0.47	2.2	10	µH
C_{IN}	Input capacitance, effective value	10			µF
C_O	Output capacitance, effective value	10	47	1000	µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61089x RNR (VQFN) 11 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W
$R_{\theta JA(EVM)}$ (2)	Junction-to-ambient thermal resistance on EVM	39.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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(2) The EVM board is a 4-layer PCB of 76-mm x 52-mm size. The copper thickness of top layer and bottom layer is 2 oz. The copper thickness of inner layers is 1 oz.

7.5 Electrical Characteristics

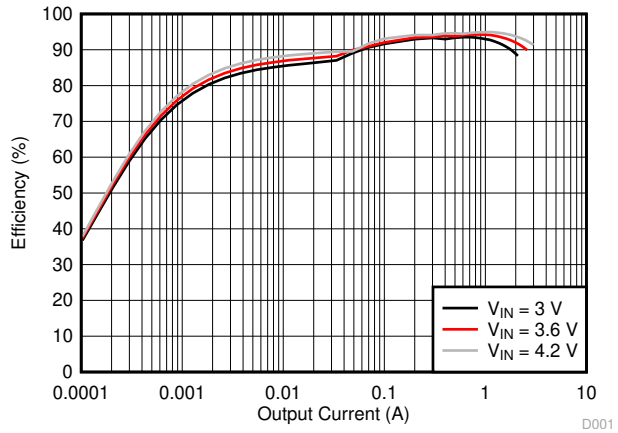
V_{IN} = 2.7 V to 5.5 V, V_{OUT} = 9 V, T_J = –40°C to 125°C. Typical values are at T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		12	V
V_{IN_UVLO}	Input voltage undervoltage lockout (UVLO) threshold	V_{IN} rising			2.7	V
		V_{IN} falling		2.4	2.5	V
V_{IN_HYS}	VIN UVLO hysteresis			200		mV
V_{CC}	VCC regulation voltage	I_{CC} = 2 mA, V_{IN} = 8 V		5.8		V
V_{CC_UVLO}	VCC UVLO threshold	V_{CC} falling		2.1		V
I_Q	Quiescent current into VIN pin	IC enabled, No load, V_{IN} = 2.7 V to 5.5 V, V_{FB} = 1.3 V, V_{OUT} = 12 V, $T_J \le 85°C$		1	3	µA
	Quiescent current into VOUT pin	IC enabled, No load, V_{IN} = 2.7 V to 5.5 V, V_{FB} = 1.3 V, V_{OUT} = 12 V, $T_J \le 85°C$		100	180	µA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} = 2.7 V to 5.5 V, $T_J \le 85°C$		1	3	µA
OUTPUT						
V_{OUT}	Output voltage range		4.5		12.6	V
V_{REF}	Reference voltage at FB pin	PWM mode	1.188	1.212	1.236	V
		PFM mode		1.224		V
I_{FB_LKG}	Leakage current into FB pin	V_{FB} = 1.2 V			100	nA
V_{OVP}	Output overvoltage protection threshold	V_{OUT} rising	12.7	13.2	13.6	V
V_{OVP_HYS}	Output overvoltage protection hysteresis	V_{OUT} falling below V_{OVP}		0.25		V
t_{SS}	Soft startup time	C_{OUT}(effective) = 47 µF, I_{OUT} = 0 A	2	4	6	ms
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	$V_{FB} = V_{REF}$ + 200 mV, V_{COMP} = 1.9 V		20		µA
I_{SOURCE}	COMP pin source current	$V_{FB} = V_{REF}$ – 200 mV, V_{COMP} = 1.9 V		20		µA
V_{CCLP_H}	High clamp voltage at the COMP pin	V_{FB} = 1 V, R_{ILIM} = 127 kΩ		2.3		V
V_{CCLP_L}	Low clamp voltage at the COMP pin	V_{FB} = 1.4 V, R_{ILIM} = 127 kΩ		1.4		V
G_{EA}	Error amplifier transconductance	V_{COMP} = 1.9 V		190		µS
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	V_{CC} = 6 V		27	44	mΩ
	Low-side MOSFET on-resistance	V_{CC} = 6 V		19	31	mΩ
SWITCHING FREQUENCY						
f_{SW}	Switching frequency	R_{FSW} = 301 kΩ		500		kHz
		R_{FSW} = 46.4 kΩ		2000		kHz
t_{ON_min}	Minimum on time	V_{CC} = 6 V		90	180	ns
CURRENT LIMIT						
I_{LIM}	Peak switch current limit, TPS61089	R_{ILIM} = 127 kΩ	7.3	8.1	8.9	A
		R_{ILIM} = 100 kΩ	9.0	10	11	A
V_{ILIM}	Internal reference voltage at ILIM pin			1.212		V
EN LOGIC INPUT						
V_{EN_H}	EN Logic high threshold				1.2	V
V_{EN_L}	EN Logic Low threshold		0.4			V
R_{EN}	EN pulldown resistor			800		kΩ
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

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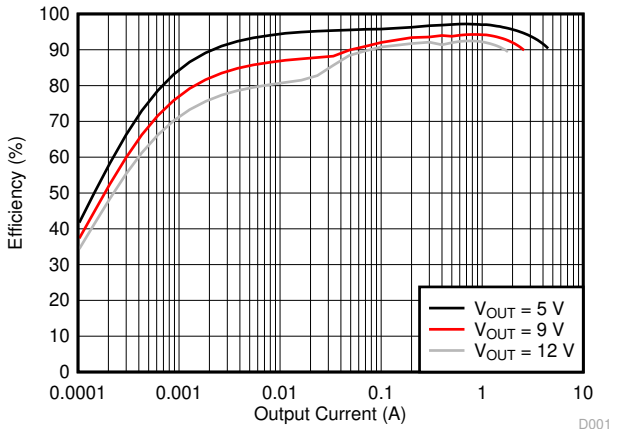
7.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 9 V, T_J = 25°C, unless otherwise noted



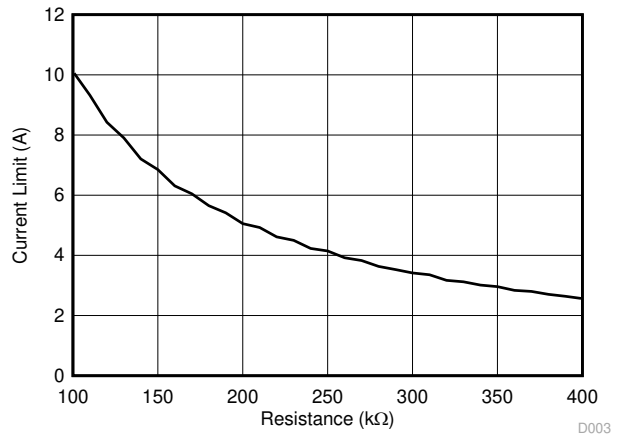
TPS61089 V_{OUT} = 9 V

Figure 7-1. Load Efficiency with Different Input Voltage



TPS61089 V_{IN} = 3.6 V

Figure 7-2. Load Efficiency with Different Output Voltage



TPS61089

Figure 7-3. Switching Peak Current Limit Setting

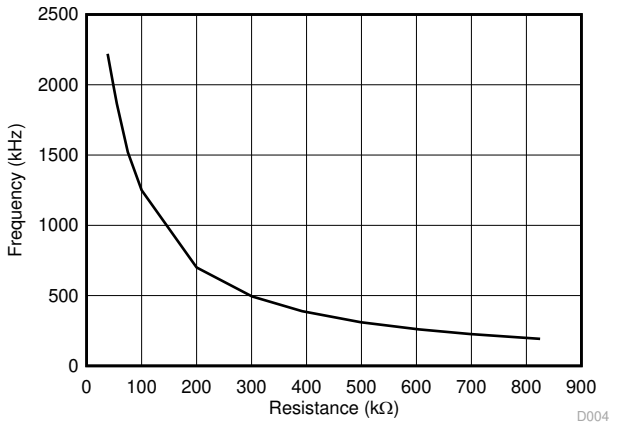


Figure 7-4. Switching Frequency Setting

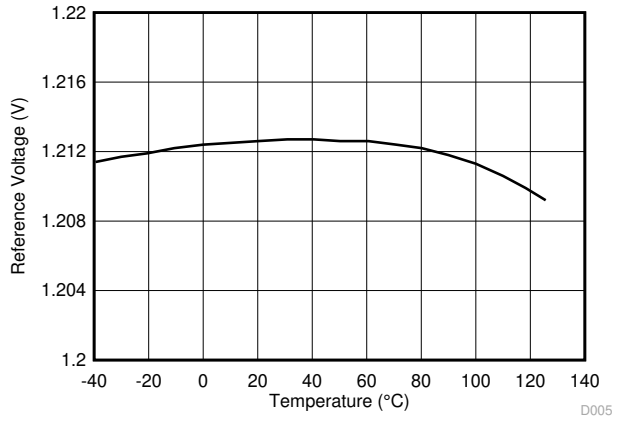


Figure 7-5. Reference Voltage vs Temperature

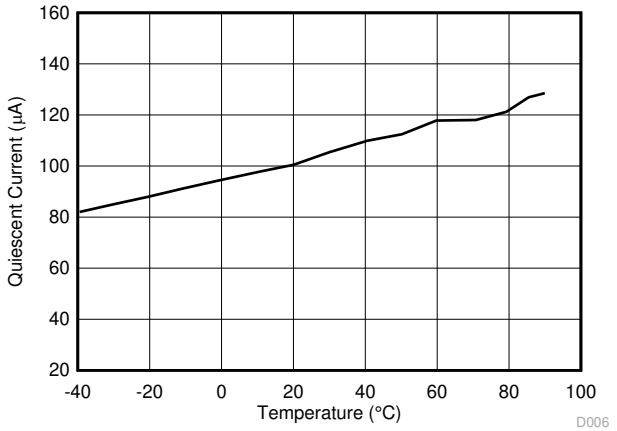


Figure 7-6. Quiescent Current vs Temperature

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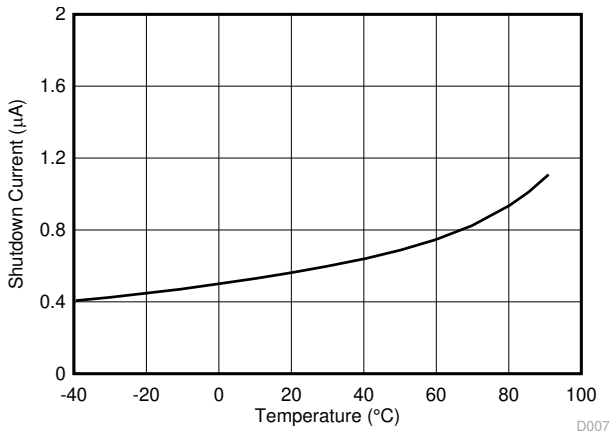


Figure 7-7. Shutdown Current vs Temperature

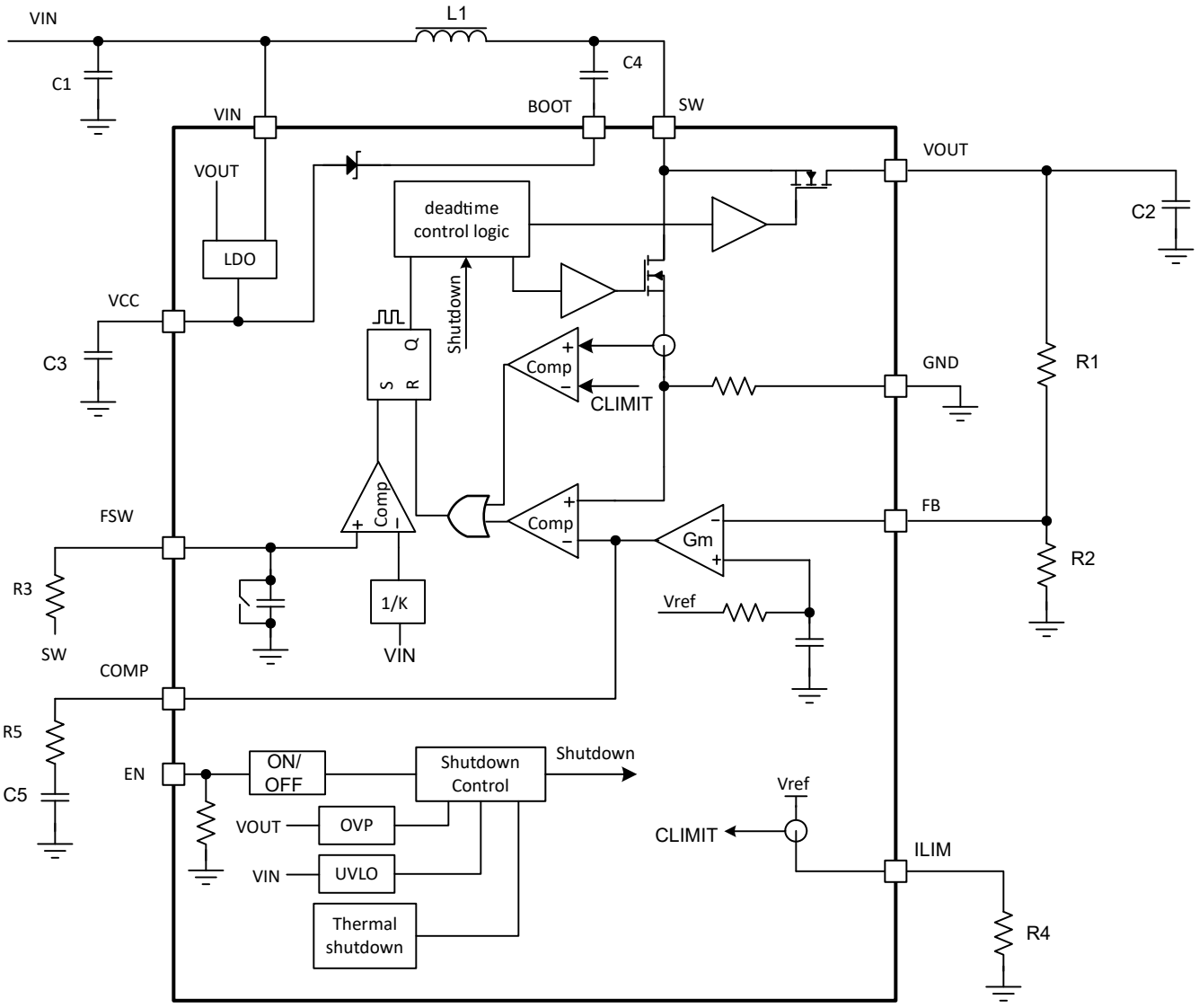
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8 Detailed Description

8.1 Overview

The TPS61089x is a synchronous boost converter, integrating a 19-mΩ main power switch and a 27-mΩ rectifier switch with adjustable switch current up to 10 A. It is capable to output continuous power more than 18 W from input of a single cell Lithium-ion battery or two-cell Lithium-ion batteries in series. The TPS61089x operates at a quasi-constant frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load current, the TPS61089 operates in PFM mode and the TPS610891 operates in forced PWM (FPWM) mode. The PFM mode brings high efficiency over the entire load range, and the FPWM mode can avoid the acoustic noise and switching frequency interference at light load. The converter uses the constant off-time peak current mode control scheme, which provides excellent line and load transient response with minimal output capacitance. The external loop compensation brings flexibility to use different inductors and output capacitors. The TPS61089x supports adjustable switching frequency ranging from 200 kHz to 2.2 MHz. The device implements cycle-by-cycle current limit to protect the device from overload conditions during boost switching. The current limit is set by an external resistor.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 2.5 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 2.7 V. This function is implemented to prevent the device from malfunctioning when the input voltage is between 2.5 V and 2.7 V.

8.3.2 Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 2.7 V and the EN pin is pulled above the high threshold, the TPS61089x is enabled. When the EN pin is pulled below the low threshold, the TPS61089x goes into shutdown mode. The device stops switching in shutdown mode and consumes less than 3-µA current. Because of the body diode of the high-side rectifier FET, the input voltage goes through the body diode and appears at the VOUT pin at shutdown mode.

8.3.3 Soft Start

The TPS61089x implements the soft start function to reduce the inrush current during start-up. The TPS61089x begins soft start when the EN pin is pulled to logic high voltage. The soft start time is typically 4 ms.

8.3.4 Adjustable Switching Frequency

The TPS61089x features a wide adjustable switching frequency ranging from 200 kHz to 2.2 MHz. The switching frequency is set by a resistor connected between the FSW pin and the SW pin of the TPS61089x. Do not leave the FSW pin open. Use Equation 1 to calculate the resistor value required for a desired frequency.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \times \frac{V_{OUT}}{V_{IN}} \right)}{C_{FREQ}} \quad (1)$$

where

- R_{FREQ} is the resistance connected between the FSW pin and the SW pin
- C_{FREQ} = 24 pF
- f_{SW} is the desired switching frequency
- t_{DELAY} = 86 ns
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

8.3.5 Adjustable Peak Current Limit

To avoid an accidental large peak current, an internal cycle-by-cycle current limit is adopted. The low-side switch turns off immediately as long as the peak switch current touches the limit. The peak inductor current can be set by selecting the correct external resistor value correlating with the required current limit. Use Equation 2 to calculate the correct resistor value for the TPS61089.

$$I_{LIM} = \frac{1030000}{R_{ILIM}} \quad (2)$$

where

- R_{ILIM} is the resistance connected between the ILIM pin and ground
- I_{LIM} is the switch peak current limit

For a typical current limit of 8 A, the resistor value is 127 kΩ for the TPS61089.

8.3.6 Overvoltage Protection

If the output voltage at the VOUT pin is detected above the overvoltage protection threshold of 13.2 V (typical value), the TPS61089x stops switching immediately until the voltage at the VOUT pin drops the hysteresis

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voltage lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

8.3.7 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown happens at the junction temperature of 150°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 130°C, then the device starts switching again.

8.4 Device Functional Modes

8.4.1 Operation

The TPS61089x synchronous boost converter operates at a quasi-constant frequency pulse width modulation (PWM) in moderate to heavy load condition. Based on the V_{IN} to V_{OUT} ratio, a circuit predicts the required off-time of the switching cycle. At the beginning of each switching cycle, the low-side N-MOSFET switch, shown in *Section 8.2*, is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips, and turns off the low-side N-MOSFET switch and the inductor current goes through the body diode of the high-side N-MOSFET in a dead-time duration. After the dead-time duration, the high-side N-MOSFET switch is turned on. Since the output voltage is higher than the input voltage, the inductor current decreases. The high-side switch is not turned off until the fixed off-time is reached. After a short dead-time duration, the low-side switch is turned on again and the switching cycle is repeated.

In light load condition, the TPS61089 implements PFM mode for applications requiring high efficiency at light load. And the TPS610891 implements forced PWM mode for applications requiring fixed switching frequency to avoid unexpected switching noise interference.

8.4.1.1 Forced PWM Mode

In forced PWM mode, the TPS610891 keeps the switching frequency unchanged in light load condition. When the load current decreases, the output of the internal error amplifier decreases as well to keep the inductor peak current down, delivering less power from input to output. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. The high-side N-MOSFET is not turned off even if the current through the MOSFET is zero. Thus, the inductor current changes its direction after it runs to zero. The power flow is from output side to input side. The efficiency will be low in this mode. But with the fixed switching frequency, there is no audible noise and other problems which might be caused by low switching frequency in light load condition.

8.4.1.2 PFM Mode

The TPS61089 improves the efficiency at light load with PFM mode. When the converter operates in light load condition, the output of the internal error amplifier decreases to make the inductor peak current down, delivering less power to the load. When the output current further reduces, the current through the inductor will decrease to zero during the off-time. Once the current through the high-side N-MOSFET is zero, the high-side MOSFET is turned off until the beginning of the next switching cycle. When the output of the error amplifier continuously goes down and reaches a threshold with respect to the peak current of I_{LIM} / 10, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the TPS61089 delivers, the output voltage increases above the nominal setting output voltage. The TPS61089 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 1.0% higher than the nominal setting voltage. With the PFM operation mode, the TPS61089 keeps the efficiency above 70% even when the load current decreases to 1 mA. At light load, the output voltage ripple is much smaller due to low peak inductor current. Refer to Figure 8-1.

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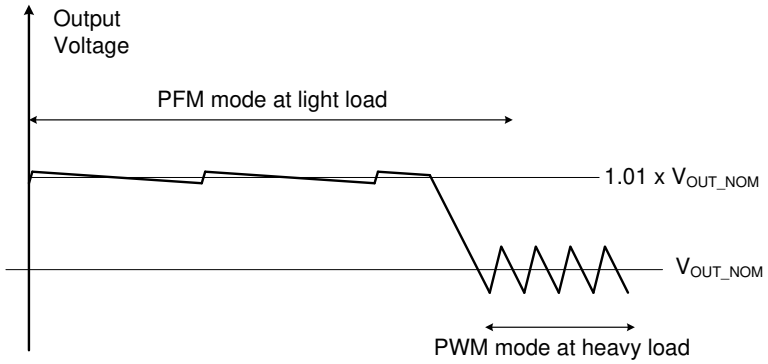


Figure 8-1. Output Voltage in PWM Mode and PFM Mode

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS61089x is designed for outputting voltage up to 12.6 V with 7-A continuous switch current capability to deliver more than 18-W power. The TPS61089x operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate to heavy load condition. In light load condition, the TPS61089 operates in PFM mode and the TPS610891 operates in forced PWM mode. The PFM mode brings high efficiency over entire load range, while PWM mode can avoid the acoustic noise as the switching frequency is fixed. In PWM mode, the TPS61089x converter uses the adaptive constant off-time peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The TPS61089x can work with a different inductor and output capacitor combination by external loop compensation. It also supports adjustable switching frequency ranging from 200 kHz to 2.2 MHz.

9.2 Typical Application

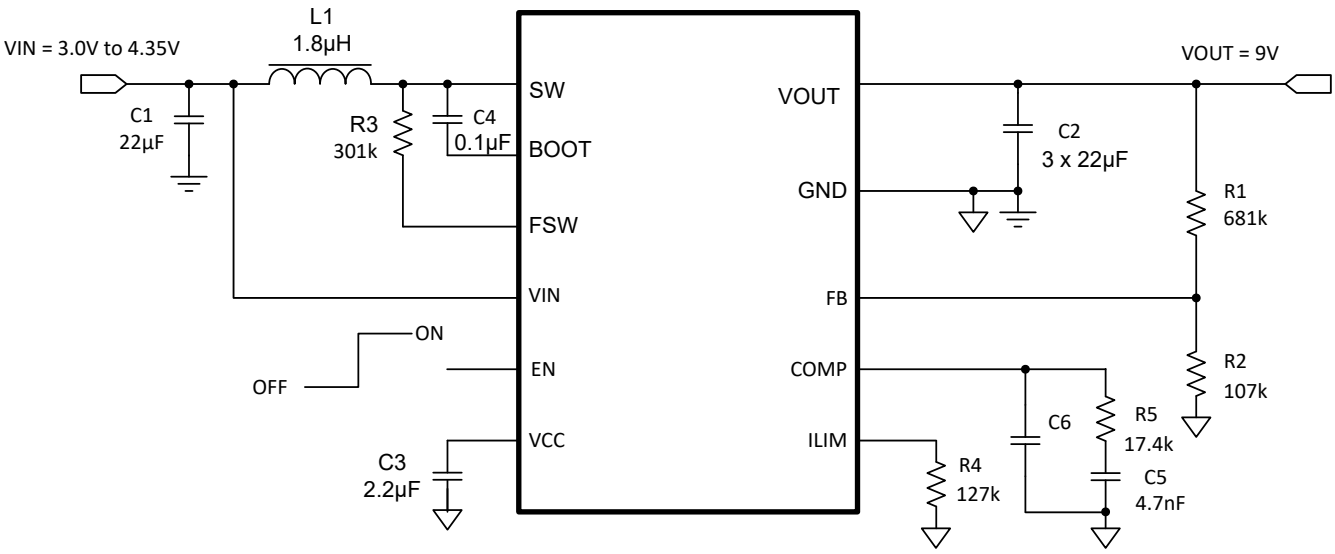


Figure 9-1. TPS61089x Single Cell Li-ion Battery to 9-V/2-A Output Converter

9.2.1 Design Requirements

Table 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	3.0 to 4.35 V
Output voltage	9 V
Output voltage ripple	100 mV peak to peak
Output current rating	2 A
Operating frequency	500 kHz
Operation mode at light load	PFM

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9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61089x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting Switching Frequency

The switching frequency is set by a resistor connected between the FSW pin and the SW pin of the TPS61089x. The resistor value required for a desired frequency can be calculated using Equation 3.

$$R_{FREQ} = \frac{4 \times \left(\frac{1}{f_{SW}} - t_{DELAY} \times \frac{V_{OUT}}{V_{IN}} \right)}{C_{FREQ}} \quad (3)$$

where

- R_{FREQ} is the resistance connected between the FSW pin and the SW pin
- C_{FREQ} = 24 pF
- f_{SW} is the desired switching frequency
- t_{DELAY} = 86 ns
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

9.2.2.3 Setting Peak Current Limit

The peak input current is set by selecting the correct external resistor value correlating to the required current limit. Use Equation 4 to calculate the correct resistor value:

$$I_{LIM} = \frac{1030000}{R_{ILIM}} \quad (4)$$

where

- R_{ILIM} is the resistance connected between the ILIM pin and ground
- I_{LIM} is the switching peak current limit

For a typical current limit of 8 A, the resistor value is 127 kΩ. Considering the device variation and the tolerance over temperature, the minimum current limit at the worst case can be 0.8 A lower than the value calculated by Equation 4. The minimum current limit must be higher than the required peak switch current at the lowest input voltage and the highest output power to make sure the TPS61089x does not hit the current limit and still can regulate the output voltage in these conditions.

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9.2.2.4 Setting Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in *TPS61089x Single Cell Li-ion Battery to 9-V/2-A Output Converter*). Typically, a minimum current of 10 µA flowing through the feedback divider gives good accuracy and noise covering. A resistor of less than 120 kΩ is typically selected for low-side resistor R2.

When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Thus, the value of R1 is calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (5)$$

9.2.2.5 Inductor Selection

Because the selection of the inductor affects the steady state operation of the power supply, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The TPS61089x is designed to work with inductor values between 0.47 µH and 10 µH. A 0.47-µH inductor is typically available in a smaller or lower-profile package, while a 10-µH inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a 10-µH inductor can maximize the controller's output current capability.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 6 to Equation 7 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductor value with –30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 6.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

where

- V_{OUT} is the output voltage of the boost regulator
- I_{OUT} is the output current of the boost regulator
- V_{IN} is the input voltage of the boost regulator
- η is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple as in Equation 7.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \quad (7)$$

where

- I_{PP} is the inductor peak-to-peak ripple
- L is the inductor value
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

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Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with Equation 8.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \quad (8)$$

Set the current limit of the TPS61089x higher than the peak current I_{Lpeak}. Then select the inductor with saturation current higher than the setting current limit.

Boost converter efficiency is dependent on the resistance of its current path, the switching loss associated with the switching MOSFETs, and the core loss of the inductor. The TPS61089x has optimized the internal switch resistance. However, the overall efficiency is affected significantly by the DC resistance (DCR) of the inductor, equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, TI would recommend an inductor with lower DCR and ESR. However, there is a tradeoff among the inductance of the inductor, DCR and ESR resistance, and its footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors. Table 9-2 lists recommended inductors for the TPS61089x. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the Sumida inductor CDMC8D28NP-1R8MC is selected for its small size and low DCR.

Table 9-2. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT / HEAT RATING CURRENT (A)	SIZE MAX (L × W × H mm)	VENDOR
CDMC8D28NP-1R8MC	1.8	12.6	9.4 / 9.3	9.5 x 8.7 x 3.0	Sumida
744311150	1.5	7.2	14.0 / 11.0	7.3 x 7.2 x 4.0	Wurth-Elektronik
744311220	2.2	12.5	13.0 / 9.0	7.3 × 7.2 × 4.0	Wurth-Elektronik
PIMB103T-2R2MS	2.2	9.0	16 / 13	11.2 × 10.3 × 3.0	Cyntec
PIMB065T-2R2MS	2.2	12.5	12 / 10.5	7.4 × 6.8 × 5.0	Cyntec

9.2.2.6 Input Capacitor Selection

For good input voltage filtering, TI recommends low-ESR ceramic capacitors. The VIN pin is the power supply for the TPS61089x. A 0.1-µF ceramic bypass capacitor is recommended as close as possible to the VIN pin of the TPS61089x. The VCC pin is the output of the internal LDO. A ceramic capacitor of more than 1.0 µF is required at the VCC pin to get a stable operation of the LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100 mV. Generally, 10-µF input capacitance is sufficient for most applications.

Note

DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. The differences between the rated capacitor value and the effective capacitance result from package size and voltage rating in combination with material. A 10-V rated 0805 capacitor with 10 µF can have an effective capacitance of less 5 µF at an output voltage of 5 V.

9.2.2.7 Output Capacitor Selection

For small output voltage ripple, TI recommends a low-ESR output capacitor like a ceramic capacitor. Typically, three 22-µF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Take care when evaluating a capacitor’s derating under DC bias. The bias

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can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the following equations to calculate the minimum required effective capacitance C_O:

$$V_{ripple_dis} = \frac{(V_{OUT} - V_{IN_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_O} \quad (9)$$

$$V_{ripple_ESR} = I_{Lpeak} \times R_{ESR} \quad (10)$$

where

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter's switching frequency.
- R_{ESR} is the ESR of the output capacitors.

9.2.2.8 Loop Stability

The TPS61089x requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network comprised of resistor R5, ceramic capacitors C5 and C6 is connected to the COMP pin.

The power stage small signal loop response of constant off time (COT) with peak current control can be modeled by Equation 11.

$$G_{PS}(S) = \frac{R_O \times (1 - D)}{2 \times R_{sense}} \times \frac{\left(1 + \frac{S}{2 \times \pi \times f_{ESRZ}}\right)\left(1 - \frac{S}{2 \times \pi \times f_{RHPZ}}\right)}{1 + \frac{S}{2 \times \pi \times f_P}} \quad (11)$$

where

- D is the switching duty cycle
- R_O is the output load resistance
- R_{sense} is the equivalent internal current sense resistor, which is 0.08 Ω
- f_P is the pole's frequency
- f_{ESRZ} is the zero's frequency
- f_{RHPZ} is the right-half-plane-zero's frequency

The D, f_P, f_{ESRZ}, and f_{RHPZ} can be calculated by following equations:

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (12)$$

where

- η is the power conversion efficiency

$$f_P = \frac{2}{2\pi \times R_O \times C_O} \quad (13)$$

where

- C_O is effective capacitance of the output capacitor

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$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (14)$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor

$$f_{RHPZ} = \frac{R_O \times (1 - D)^2}{2\pi \times L} \quad (15)$$

The COMP pin is the output of the internal transconductance amplifier. Equation 16 shows the small signal transfer function of compensation network.

$$Gc(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{S}{2 \times \pi \times f_{COMZ}}\right)}{\left(1 + \frac{S}{2 \times \pi \times f_{COMP1}}\right)\left(1 + \frac{S}{2 \times \pi \times f_{COMP2}}\right)} \quad (16)$$

where

- G_{EA} is the amplifier's transconductance
- R_{EA} is the amplifier's output resistance
- V_{REF} is the refernce voltage at the FB pin
- V_{OUT} is the output voltage
- f_{COMP1}, f_{COMP2} are the poles' frequency of the compensation network
- f_{COMZ} is the zero's frequency of the compensation network

The next step is to choose the loop crossover frequency, f_C. The higher in frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

At the crossover frequency, the loop gain is 1. Thus the value of R5 can be calculated by Equation 17, then set the values of C5 and C6 (in TPS61089x Single Cell Li-ion Battery to 9-V/2-A Output Converter) by Equation 18 and Equation 19.

$$R5 = \frac{2\pi \times V_{OUT} \times R_{sense} \times f_C \times C_O}{(1 - D) \times V_{REF} \times G_{EA}} \quad (17)$$

where

- f_C is the selected crossover frequency

The value of C5 can be set by Equation 18.

$$C5 = \frac{R_O \times C_O}{2R5} \quad (18)$$

The value of C6 can be set by Equation 19.

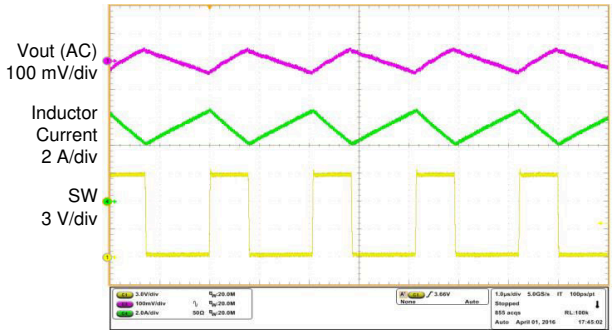
$$C6 = \frac{R_{ESR} \times C_O}{R5} \quad (19)$$

If the calculated value of C6 is less than 10 pF, it can be left open.

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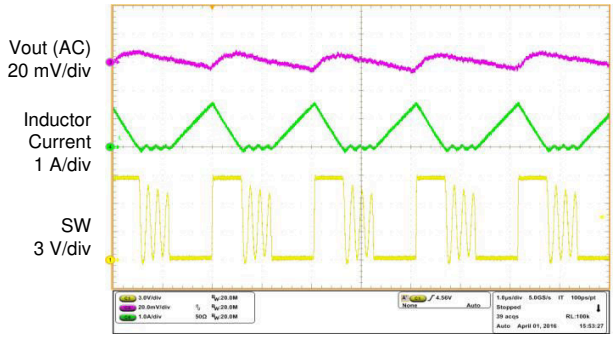
Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output votlage ringing during the line and load transient.

9.2.3 Application Curves



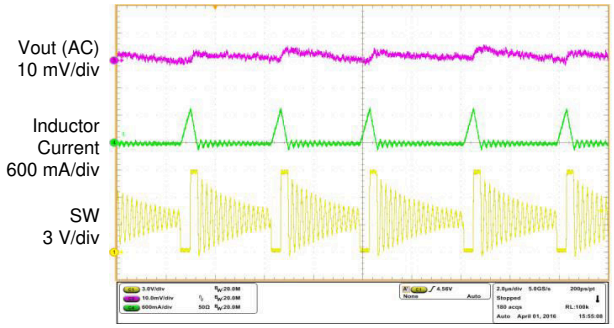
V_{IN} = 3.6 V V_{OUT} = 9 V I_{OUT} = 2 A

Figure 9-2. Switching Waveforms in CCM



V_{IN} = 3.6 V V_{OUT} = 9 V I_{OUT} = 200 mA

Figure 9-3. Switching Waveforms in DCM



V_{IN} = 3.6 V V_{OUT} = 9 V I_{OUT} = 20 mA

Figure 9-4. Switching Waveforms in PFM Mode

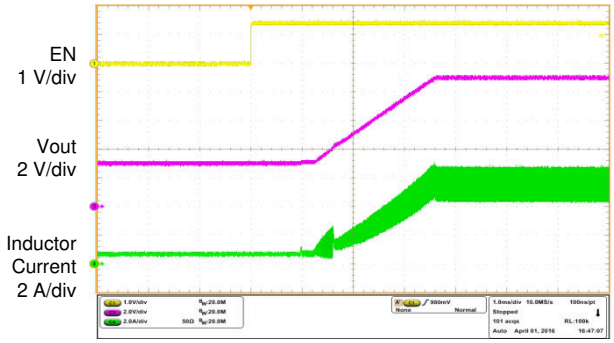


Figure 9-5. Start-up Waveforms

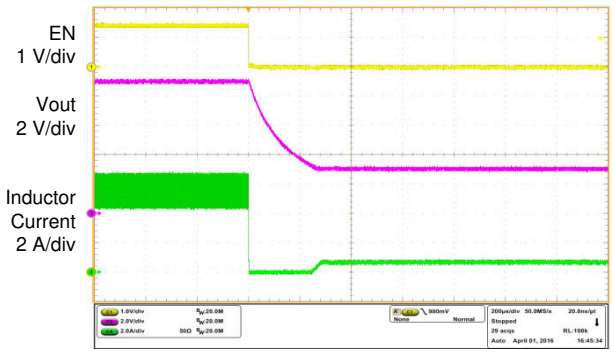
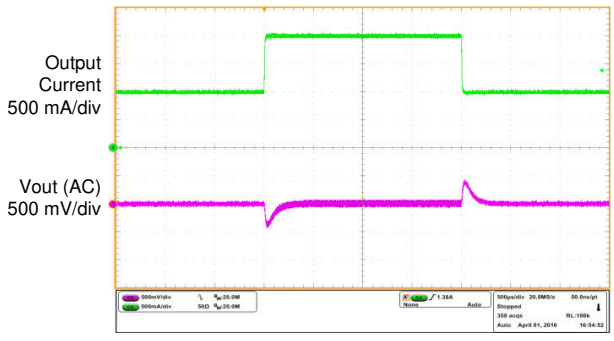


Figure 9-6. Shutdown Waveforms



V_{IN} = 3.6 V V_{OUT} = 9V I_{OUT} = 1 A to 2 A

Figure 9-7. Load Transient

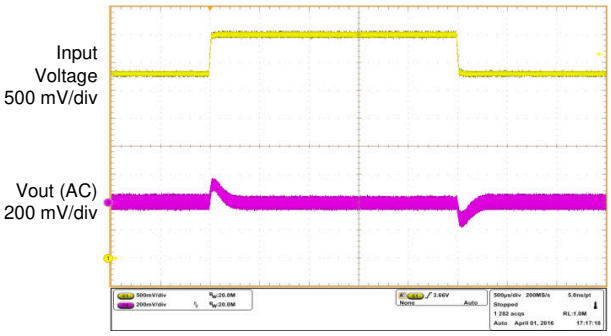


Figure 9-8. Line Transient

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10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.7 V to 12 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 µF.

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11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switching rise time and fall time are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs to be close to the VIN pin and GND pin to reduce the input supply current ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin.

11.2 Layout Example

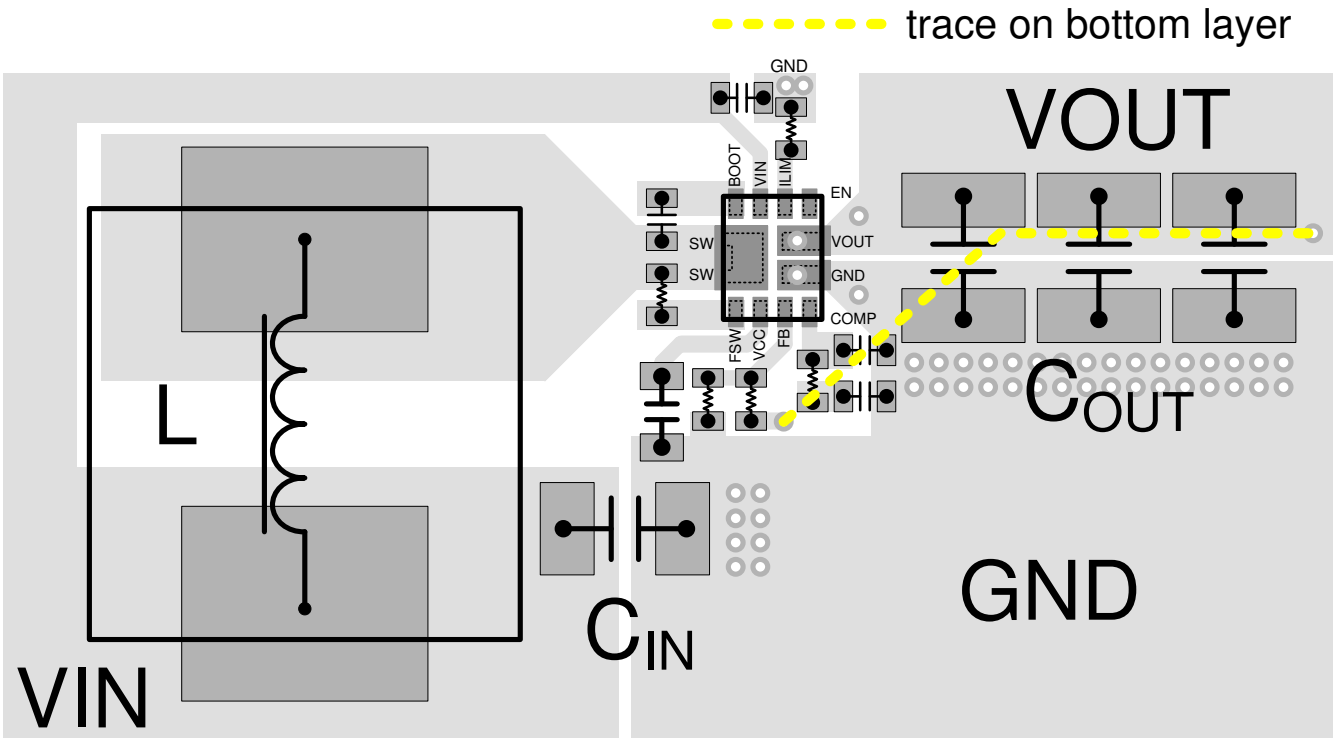


Figure 11-1. Layout Example

11.2.1 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 20.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{20}$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the *Thermal Information* table

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The TPS61089x comes in a thermally-enhanced VQFN package. The pads underneath the package improve the thermal capabilities of the package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and pad connection. Using thick PCB copper and soldering the SW pin, VOUT pin, and GND pin to large copper plate enhances the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

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12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61089x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Receiving Notification of Documentation Updates

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12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61089RNRR	Active	Production	VQFN-HR (RNR) | 11	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	ZGOI
TPS61089RNRR.A	Active	Production	VQFN-HR (RNR) | 11	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ZGOI
TPS61089RNRT	Active	Production	VQFN-HR (RNR) | 11	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	ZGOI
TPS61089RNRT.A	Active	Production	VQFN-HR (RNR) | 11	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	ZGOI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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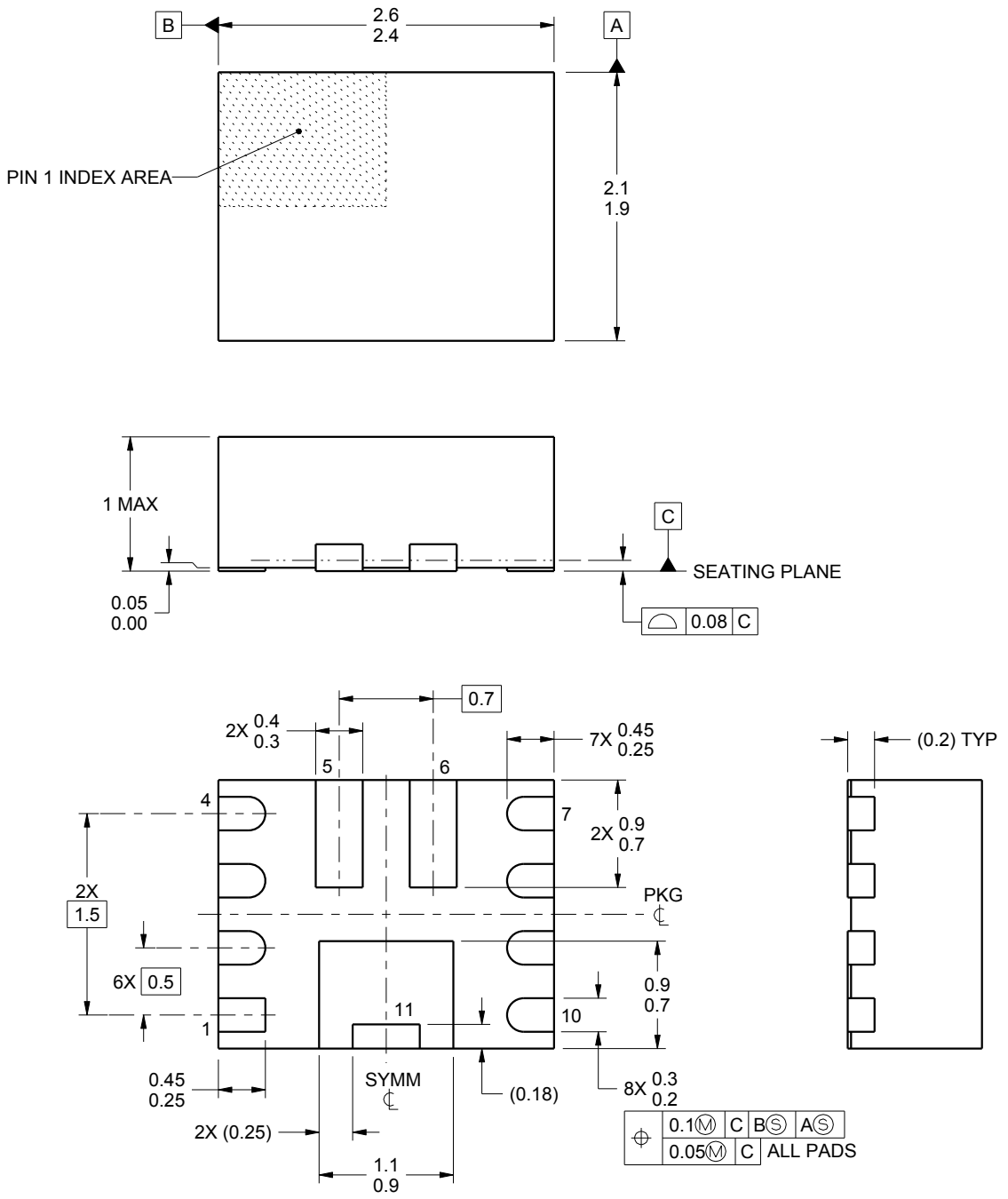
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RNR0011A

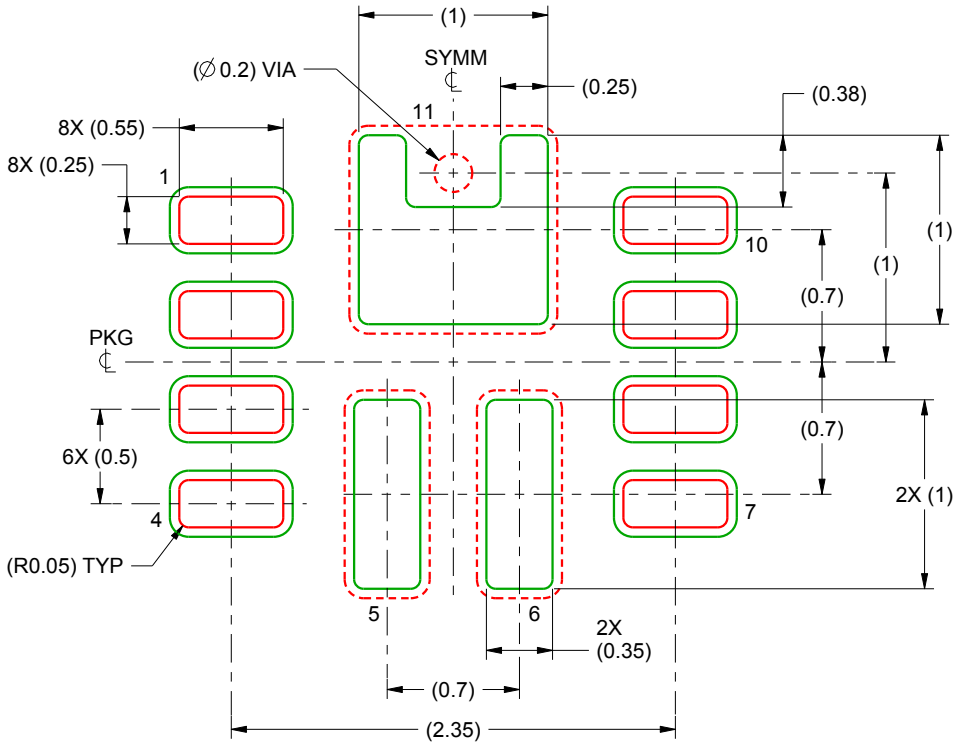
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

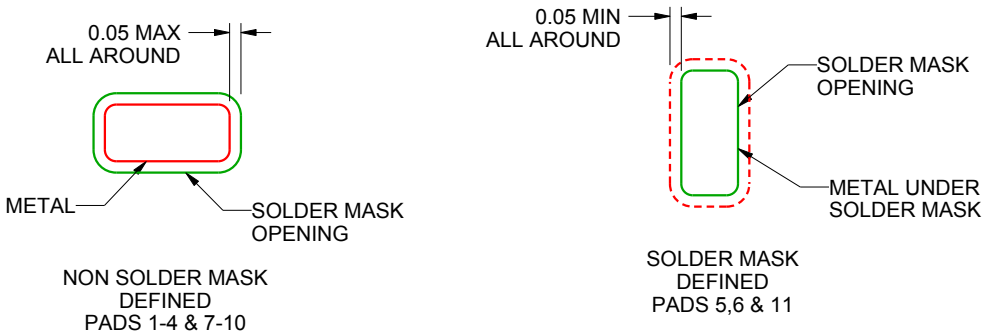


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X

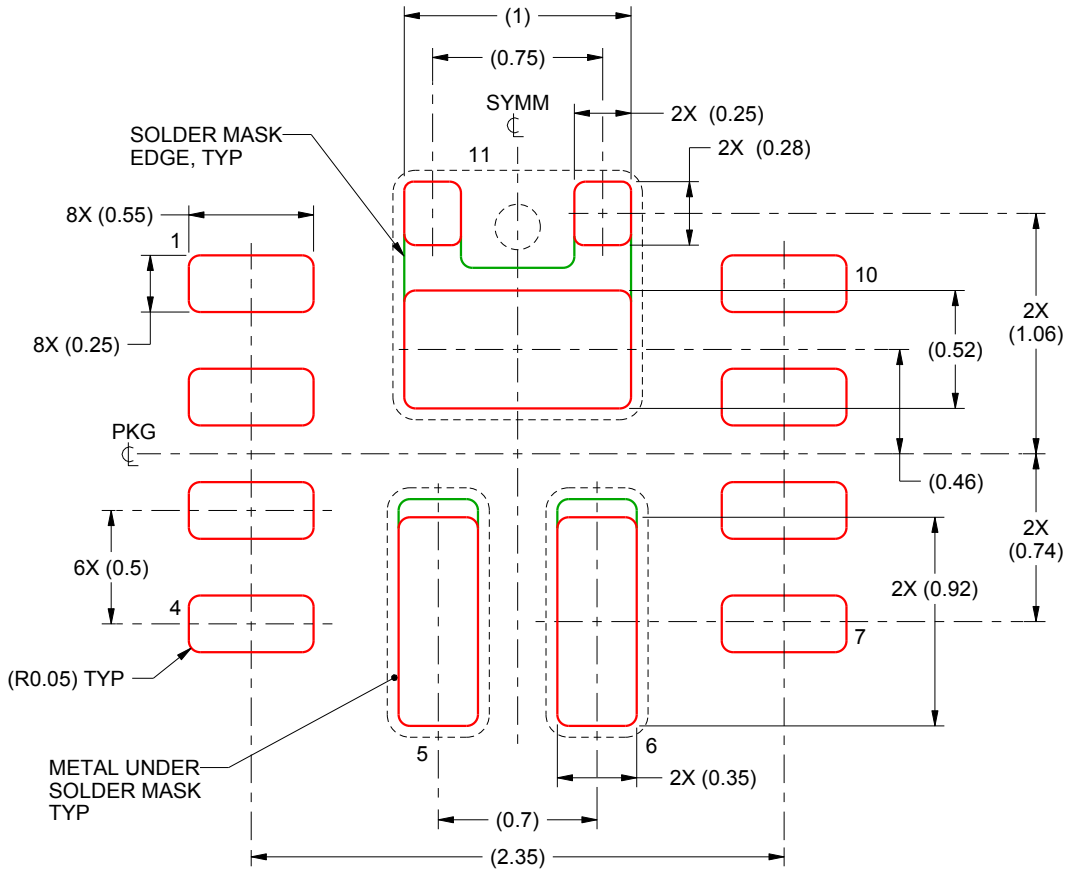


SOLDER MASK DETAILS

4222143/A 08/2015

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 5 & 6: 90% - PAD 11: 79%
SCALE:30X

4222143/A 08/2015

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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