TPS61391 85-V_{OUT} Boost Converter with Current Mirror Integrated

1 Features

- Input voltage range: 2.5 V to 5.5 V
- Output voltage range: up to 85 V
- $R_{(DS)on}$ of switching FET: 0.9 Ω
- Switch current limit: 1000 mA
- High optical power protection with 0.5-µs response time
- Switching frequency: 700 kHz
- Quiescent current: 110 µA from VIN, 340 µA from VOUT, 140 µA from AVCC
- Soft-start time: 4.8 ms
- Package: 3 mm × 3 mm × 0.75 mm QFN

2 Applications

- APD bias
- Optical line terminal
- High-voltage sensor supply

3 Description

The TPS61391 is a 700-kHz pulse-width modulating (PWM) step-up converter with an 85-V switch FET with an input ranging from 2.5 V to 5.5 V. The switching peak current is up to 1000 mA. The TPS61391 includes accurate current mirror with two gain options selectable (1 : 5 or 4 : 5).

The TPS61391 also provides high optical-power protection with an additional FET in series with the APD power path with the typical response time of 0.5 µs . It can recover automatically once the high optical releasing.

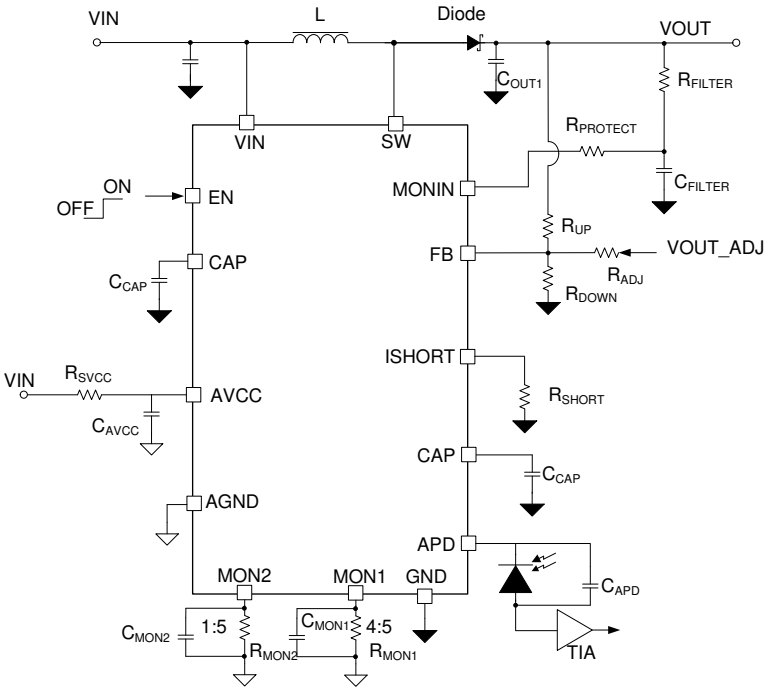
The TPS61391 is available in 3 mm × 3 mm QFN package with exposed pad underneath.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61391	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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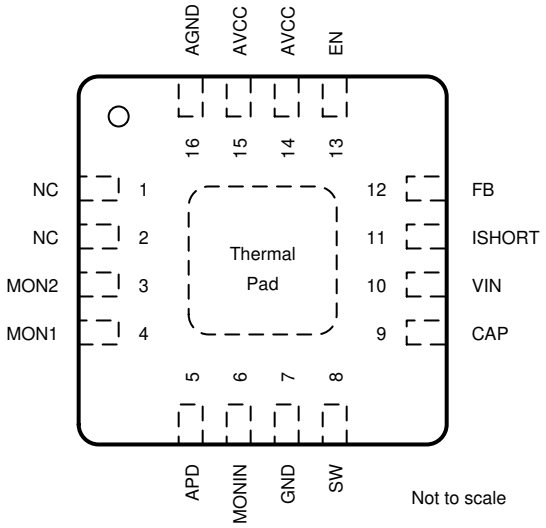
4 Revision History

DATE	REVISION	NOTES
Nov. 2019	*	Initial release.

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
NC	1,2	N/A	No internal connection
MON2	3	O	Current mirror output pin of 1 : 5 ratio (Mirror current: APD current)
MON1	4	O	Current mirror output pin of 4 : 5 ratio (Mirror current: APD current)
APD	5	O	Power supply for the APD, connect this pin with the cathode of APD
MONIN	6	I	Current mirror input pin
GND	7	–	Power Ground
SW	8	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET
CAP	9	O	Connecting a capacitor externally to lower the noise for current mirror.
VIN	10	I	IC power supply input
ISHORT	11	O	Programming the current limit for high optical power protection by a resistor between this pin and GND.
FB	12	I	Feedback voltage
EN	13	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode
AVCC	14,15	I	Power supply for the current monitor circuitry
AGND	16	–	Analog ground for the current monitor circuitry
Exposed Thermal Pad			Connect with GND, TI recommends connecting to Power GND on PCB

6 Specifications

6.1 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
V_{OUT}	Output voltage	20		85	V
T_J	Junction temperature	–40		125	°C
L	Effective Inductance		4.7		µH
C_{IN}	Effective Input Capacitance		1		µF
C_{OUT}	Effective Output Capacitance		0.1		µF

6.2 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	SW, APD, MONIN,CAP	–0.3	85	V
	Other pins	–0.3	6	V
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±1500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

THERMAL METRIC(1)		TPS61391 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Y_{JB}	Junction-to-board characterization parameter	27.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended free-air temperature range, V_{IN} = 3.3 V, AV_{CC} = 3.3 V, V_{MONIN} = 20 V to 85 V, T_J = - 40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

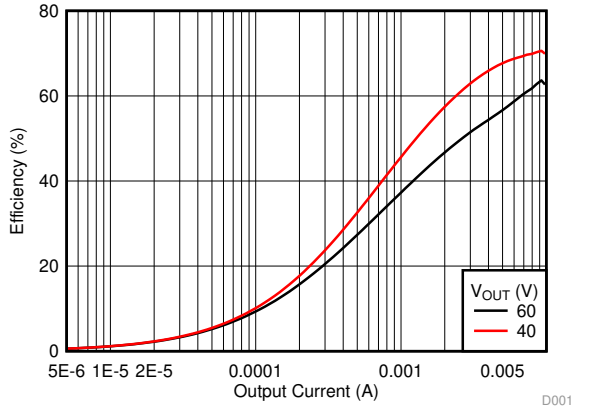
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.5		5.5	V

Electrical Characteristics (continued)

Over recommended free-air temperature range, V_{IN} = 3.3 V, AV_{CC} = 3.3 V, V_{MONIN} = 20 V to 85 V, T_J = - 40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

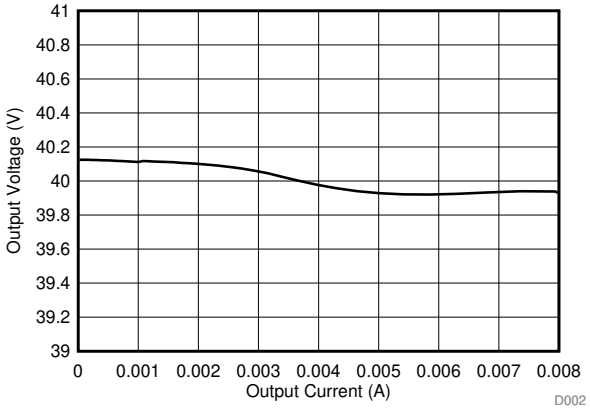
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVLO}	Under voltage lock out	V_{IN} falling		2.4	2.5	V
	Under voltage lock out hysteresis	V_{UVLO} rising - V_{UVLO} falling		200		mV
I_{Q_IN}	Quiescent current into VIN pin	V_{IN} = 3.3 V, V_{FB} =V_{REF} + 0.1 V, No switching, -40 °C ≤ T_J ≤ 85 °C		110	140	uA
I_{Q_OUT}	Quiescent current into VOUT pin	V_{IN} = 3.3 V, V_{FB} =V_{REF} + 0.1 V,No switching, -40 °C ≤ T_J ≤ 85 °C		340	430	uA
I_{Q_VCC}	Quiescent current into AVCC pin	AVCC = 3.3 V -40 °C ≤ T_J ≤ 85 °C		140	180	uA
I_{SD}	Shutdown current into VIN pin	2.5 V ≤ VIN ≤ 5.5 V, EN = 0, -40 °C ≤ T_J ≤ 85 °C			1	uA
	Shutdown current into VOUT pin	EN = 0, -40 °C ≤ T_J ≤ 85 °C			1	uA
	Shutdown current into AVCC pin	AVCC = 3.3 V, EN = 0, -40 °C ≤ T_J ≤ 85 °C			1	uA
OUTPUT						
V_{OUT}	Output voltage range				85	V
V_{REF}	Feedback regulation reference voltage	V_{IN} = 2.5 V to 5.5 V, T_J = 25 °C	1.188	1.2	1.212	V
		V_{IN} = 2.5 V to 5.5 V, -40 °C ≤ T_J ≤ 125 °C	1.182	1.2	1.218	V
I_{FB}	Feedback input leakage current			1	25	nA
POWER SWITCH						
$R_{DS(on)}$	Low-side FET on resistance	3 V ≤ V_{IN} ≤ 5.5 V		900	1300	mΩ
SWITCHING CHARACTERISTIC						
f_{SW}	Switching frequency	V_{IN} = 3.3 V, V_{OUT} = 60 V	600	700	800	kHz
CURRENT MIRROR						
k_{MON1}	4:5 Current mirror gain	I_{APD} = 5 µA to 200 µA	0.76	0.8	0.84	
k_{MON2}	1:5 Current mirror gain	I_{APD} = 100 µA to 2 mA	0.19	0.2	0.21	
V_{MON}	MON1 / MON2 Threshold		380	400	420	mV
V_{APD_DRP}	Current mirror voltage drop	I_{APD} = 1 mA	2.2	2.5	2.8	V
		I_{APD} = 5 µA		2.45		V
I_{BIAS}	Current mirror bias current		15	20	25	µA
CURRENT LIMIT						
I_{LIM_SW}	Peak switching current limit	V_{IN} = 3.3 V, V_{OUT} = 60 V	800	1000	1200	mA
I_{SHORT}	High optical power current limit	R_{ISHORT} = 25 kΩ	3.7	4	4.3	mA
		R_{ISHORT} = 50 kΩ	1.8	2	2.2	mA
CONTROL (EN)						
V_{EN_H}	EN Logic high threshold				1.2	V
V_{EN_L}	EN Logic low threshold		0.4			V
R_{EN}	EN pull down resistor			800		kΩ
TIMING						
t_{SS}	Soft start time	Ref voltage 0 to 1.2V		4.8		ms
t_{DELAY}	Delay time for high optical power protection	I_{APD} = 5 mA, I_{SHORT} = 3 mA		0.5		µs
THERMAL PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

6.6 Typical Characteristics



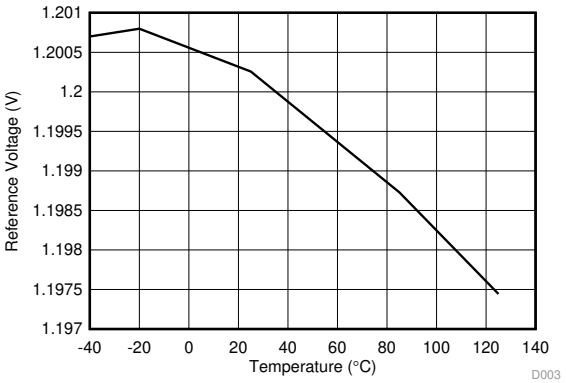
V_{IN} = 3.3 V L = 4. 7 µH C_{OUT} = 0.1 µF
Output current (boost) = 0 to 8 mA

Figure 1. Efficiency vs. Output Current



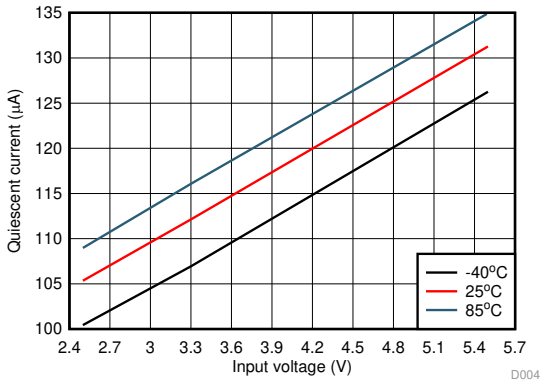
V_{IN} = 3.3 V L = 4. 7 µH C_{OUT} = 0.1 µF
Output current (boost) = 0 to 8 mA

Figure 2. Load regulation



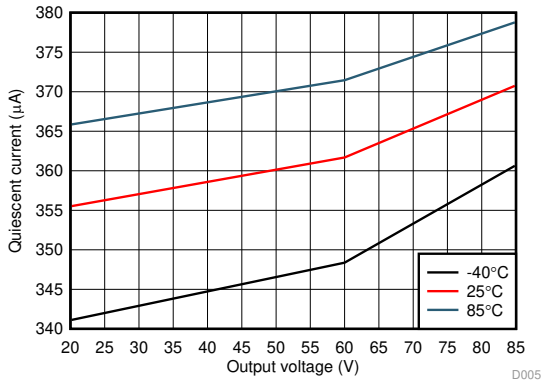
V_{IN} = 3.3 V V_{OUT} = 60 V C_{OUT} = 0.1 µF

Figure 3. Reference voltage



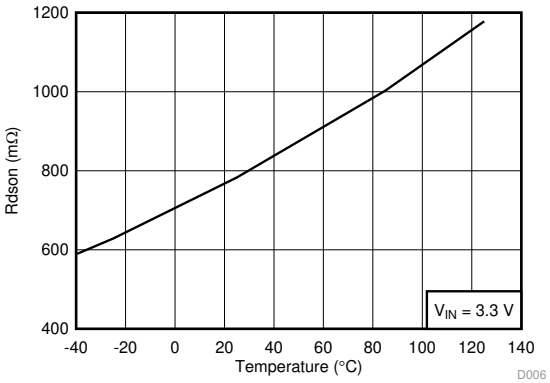
V_{OUT} = 60 V

Figure 4. Quiescent current vs. Input voltage



V_{IN} = 3.3 V

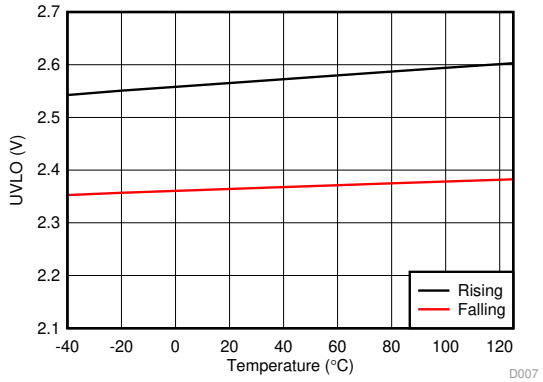
Figure 5. Quiescent current vs. Output voltage



V_{IN} = 3.3 V V_{OUT} = 60 V

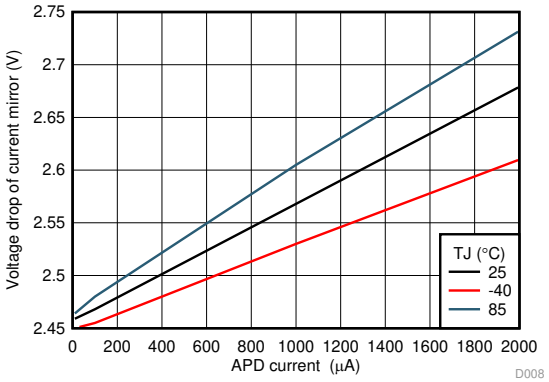
Figure 6. Rdson vs. Temperature

Typical Characteristics (continued)



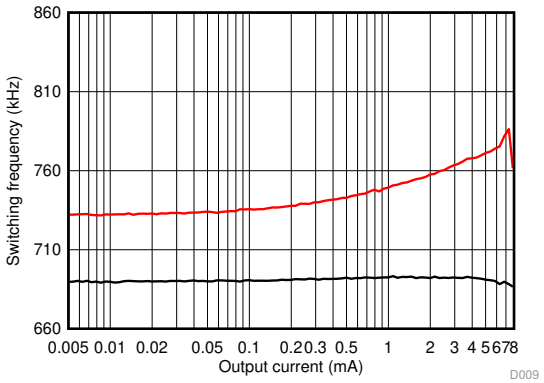
V_{OUT} = 60 V

Figure 7. Vin UVLO



V_{IN} = 3.3 V V_{OUT} = 60 V

Figure 8. Voltage drop of current mirror vs. current



V_{IN} = 3.3 V V_{OUT} = 60 V

Figure 9. Switching frequency vs. Output current

7 Detailed Description

7.1 Overview

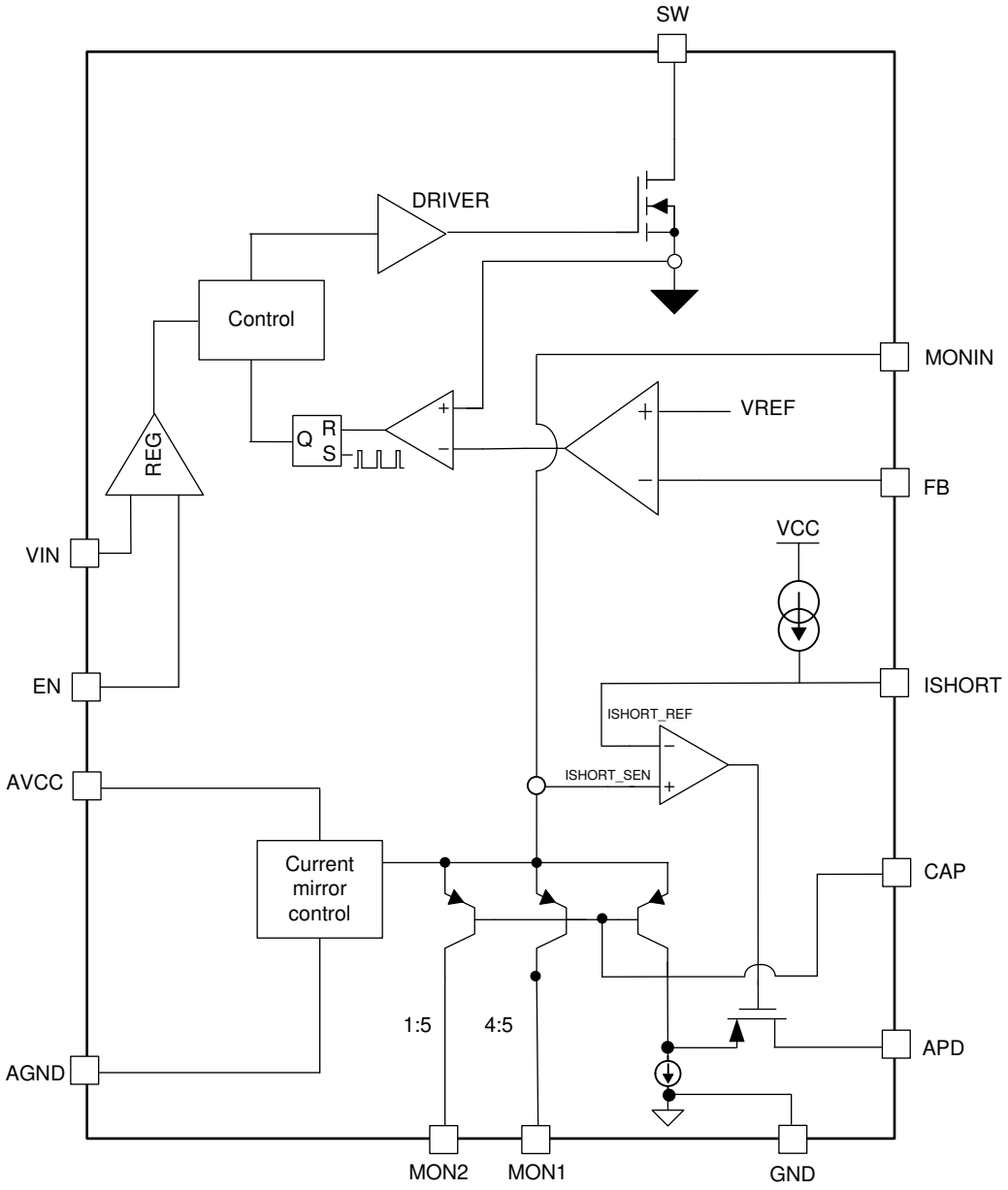
The TPS61391 is a fully integrated boost converter with an 85-V FET to convert a low input voltage to a higher voltage for biasing the APD. The TPS61391 supports an input voltage ranging from 2.5 V to 5.5 V. The device operates at a 700 kHz pulse-width modulation (PWM) crossing the whole load range.

There are two ratio options for the current proportional to APD current: the MON1 (4 : 5) and MON2 (1 : 5). By connecting a resistor from the mirror output (MON1 or MON2) to GND, the current flowing through the APD is converted into the voltage crossing the resistor from MON1 / MON2 to GND.

Additionally, a high power optical protection is integrated by clamping the pre-set current limit (program by the I_{SHORT} resistor). The response time of the high optical power is typically 0.5 µs. The device could recovery automatically when the high optical power is removed.

The device comes in a 3-mm × 3-mm QFN package with the operating junction temperature covering from –40°C to 125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 2.5 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 200 mV.

Feature Description (continued)

7.3.2 Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 2.5 V and the EN pin is pulled above the high threshold (1.2 V min.), the TPS61391 is enabled. When the EN pin is pulled below the low threshold (0.4 maximum), the device goes into shutdown mode.

7.3.3 Current Mirror

There are two current mirror options for TPS61391: the gain of 4: 5 (MON1) and 1: 5 (MON2). The maximum voltage of MON1 and MON2 is 2.5 V.

7.3.4 High Optical Power Protection

There is an additional FET in series of power path connecting with the APD. When the current flowing through the APD exceeds the short protection threshold (set by connecting the resistor from I_{SHORT} to GND), the on resistance of the FET becomes larger to clamp the current within the protection threshold by lowering the APD bias voltage. It takes typically 0.5 µs for the FET to respond in case of high optical power occuring.

When the high optical power condition releases, the TPS61391 recovers automatically back to the normal operation mode.

7.4 Device Functional Mode

7.4.1 PFM Operation

The TPS61391 integrates a power save mode with pulse frequency modulation (PFM) at the light load. When a light load condition occurs, the COMP pin voltage naturally decreases and reduces the peak current. When the COMP pin voltage further goes down with the load lowered and reaches the pre-set low threshold, the output of the error amplifier is clamped at this threshold and does not go down any more. If the load is further lowered, the device skips the switching cycles and reduces the switching losses and improves efficiency at the light load condition by reducing the average switching frequency.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61391 is a step-up DC/DC converter with current monitor circuitry integrated. The following design procedure can be used to select component values for the TPS61391. This section presents a simplified discussion of the design process.

8.2 Typical Application

This application is designed for 2.5-V to 5.5-V input, and 60-V output user case

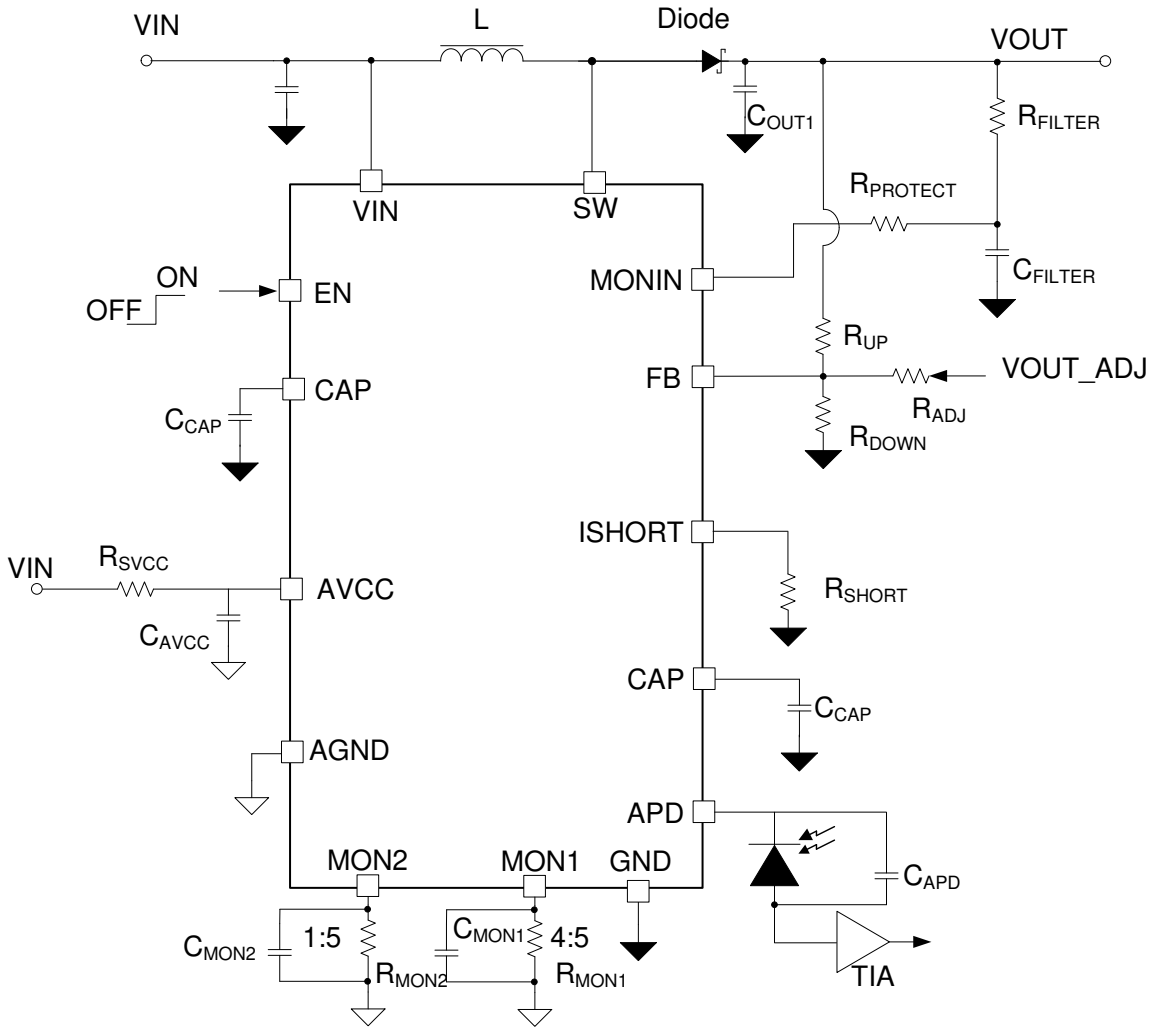


Figure 10. TPS61391 Typical Application

8.2.1 Design Requirement

For this design example, use Table 1 as the design parameters.

Typical Application (continued)

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	2.5 V to 5.5 V
Output voltage	60 V
Operating frequency	700 kHz
APD Current	0 to 2 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Rectifier Diode

A Schottky diode is the preferred type for the rectifier diode due to its low forward voltage drop and small reverse recovery charge. Low reverse leakage current is important parameter when selecting the Schottky diode. The diode must be rated to handle the maximum output voltage plus the switching node ringing. Also, it must be able to handle the average output current.

8.2.2.2 Selecting the Inductor

It is suggested that the TPS61391 device works in the DCM operation; otherwise the output voltage would not be delivered for low input voltage to high output voltage.

With the device working in DCM operation, the maximum inductor could be calculated by equation Equation 1 and Equation 2:

$$L_{MAX} = \frac{V_{IN} \times D}{f_{SW} \times I_{LIM}} \quad (1)$$

where

- V_{IN} is input voltage
- D is duty cycle
- f_{SW} is switching frequency
- I_{LIM} is current limit

For instance, if V_{IN} = 3.3 V, V_{OUT} = 60 V, f_{SW} = 600 kHz, I_{LIM} = 0.8 A, the L_{MAX} = 6.5 µH

However, there is minimum inductance is determined by the power delivered to the output side at given input condition.

$$L_{MIN} = 2 \times \frac{V_{OUT} \times I_{OUT}}{eff \times f_{SW} \times I_{LIM}^2} \quad (2)$$

where

- V_{OUT} is output voltage
- I_{OUT} is output current
- eff is the efficiency
- f_{SW} is switching frequency
- I_{LIM} is current limit

For instance, if I_{OUT} = 8 mA, V_{OUT} = 60 V, f_{SW} = 600 kHz, I_{LIM} = 0.8 A, eff = 0.6, the L_{MIN} = 4.2 µH

With the calculation aforementioned, the operating inductor is recommended between the L_{MIN} and L_{MAX}.

The 4.7 µH inductance is optimum value for using the TPS61391 in application.

8.2.2.3 Selecting Output Capacitor

Use low ESR capacitors at the output to minimize output voltage ripple. Use only X5R and X7R types, which retain their capacitance over wider voltage and temperature ranges than other types. Typically use a 0.1-µF to 1-µF capacitor for output voltage. Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate its capacitance at its rated voltage. Therefore, consider enough margins on the voltage rating to ensure adequate capacitance at the required output voltage.

8.2.2.4 Selecting Filter Resistor and Capacitor

TI recommends an additional R-C filter be added for low ripple applications. The filter parameters is characterized based on the ripple requirement. Typically, use a 100-Ω and 0.1-µF filter to reduce the switching output ripple.

8.2.2.5 Setting the Output Voltage

The output voltage of the TPS61391 is externally adjustable using a resistor divider network. The relationship between the output voltage and the resistor divider is given by Equation 3.

$$V_{OUT} = V_{FB} \times (1 + \frac{R_{UP}}{R_{DOWN}}) \quad (3)$$

where

- V_{OUT} is the output voltage
- R_{UP} the top divider resistor
- R_{DOWN} is the bottom divider resistor

Choose R_{DOWN} to be approximately 10 kΩ. Slightly increasing or decreasing R_{DOWN} can result in closer output voltage matching when using standard value resistors. In this design, R_{DOWN} = 10 kΩ and R_{UP} = 487 kΩ, resulting in an output voltage of 60 V.

8.2.2.6 Selecting Capacitor for CAP pin

TI recommends placing a ceramic capacitor from CAP pin to GND to lower the noise for the APD current mirror. A ceramic capacitor between 10 nF and 100 nF is recommended from CAP pin to GND.

8.2.2.7 Selecting Capacitor for AVCC pin

The control circuitry is powered by AVCC. A ceramic capacitor must be placed close to AVCC, with a typical capacitor value of 2.2 µF.

8.2.2.8 Selecting Capacitor for APD pin

A ceramic capacitor is required to make the APD current mirror more accurately against the noise coupling. The recommended values are from 100 pF to 470 pF.

8.2.2.9 Selecting the Resistors of MON1 or MON2

The TPS61391 provides two currents proportional to APD current on the MON pins, 4 : 5 and 1 : 5. The voltage of the resistors connecting to the MON pins convert the APD current to voltage.

8.2.2.10 Selecting the Capacitors of MON1 or MON2

The capacitors are added to the MON1 or MON2 pins to decouple the noise of APD transient current.

8.2.2.11 Selecting the Short Current Limit

The output current short-protection threshold of the TPS61391 can be programmed by an external resistor using Equation 4.

$$I_{SHORT} = \frac{100}{R_{SHORT}} \quad (4)$$

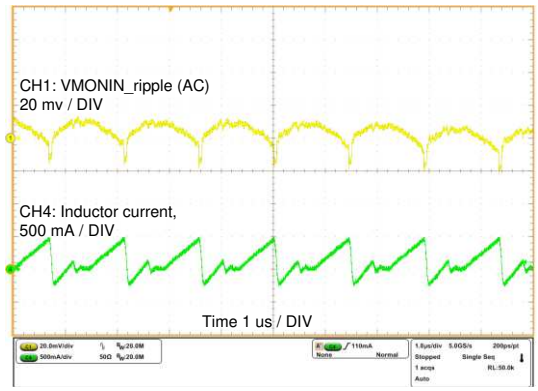
where

- I_{SHORT} (mA) is the short protection threshold
- R_{SHORT}(kΩ) is the resistor connecting from ISHORT pin to GND

For instance, if R_{SHORT} = 25 kΩ, the I_{SHORT} = 4 mA.

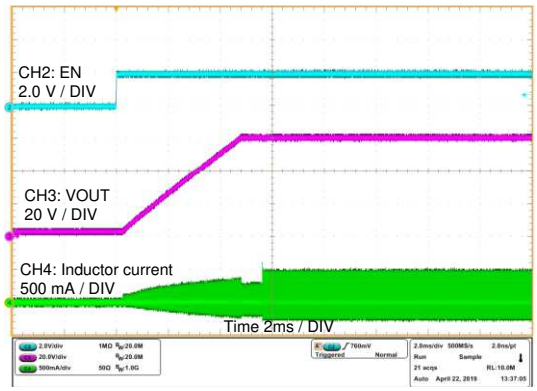
8.2.3 Application Curves

Typical condition V_{IN} = 3.3 V, V_{OUT} = 60 V, R_{SHORT} = 5 kΩ, $R_{MON1/2}$ = 3.01 kΩ and $C_{MON1/2}$ = 10 pF.
Application waveforms are measured with the inductor 4.7 µH and the output capacitance 0.1 µF at room temperature.



V_{IN} = 3.3 V V_{OUT} = 60 V APD current = 1 mA

Figure 11. Output voltage ripple with 100 Ω / 0.1 µF filter



V_{IN} = 3.3 V V_{OUT} = 60 V APD current = 1mA

Figure 12. Startup

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

The basic PCB board layout requires a separation of sensitive signal and power paths. If the layout is not carefully done, the regulator could suffer from the instability or noise problems. Use the following checklist to get good performance for a well-designed board:

- Minimize the high current path including the switch FET, rectifier FET, and the output capacitor. This loop contains high di / dt switching currents (nano seconds per ampere) and easy to transduce the high frequency noise;
- Place the noise sensitive network like current mirror output (MON1, MON2) being far away from the SW trace;
- Split the ground for the power GND, signal GND. Use a separate ground trace to connect the current monitor and boost circuitry. Connect this ground trace to the main power ground at a single point to minimize circulating currents.

10.2 Layout Example

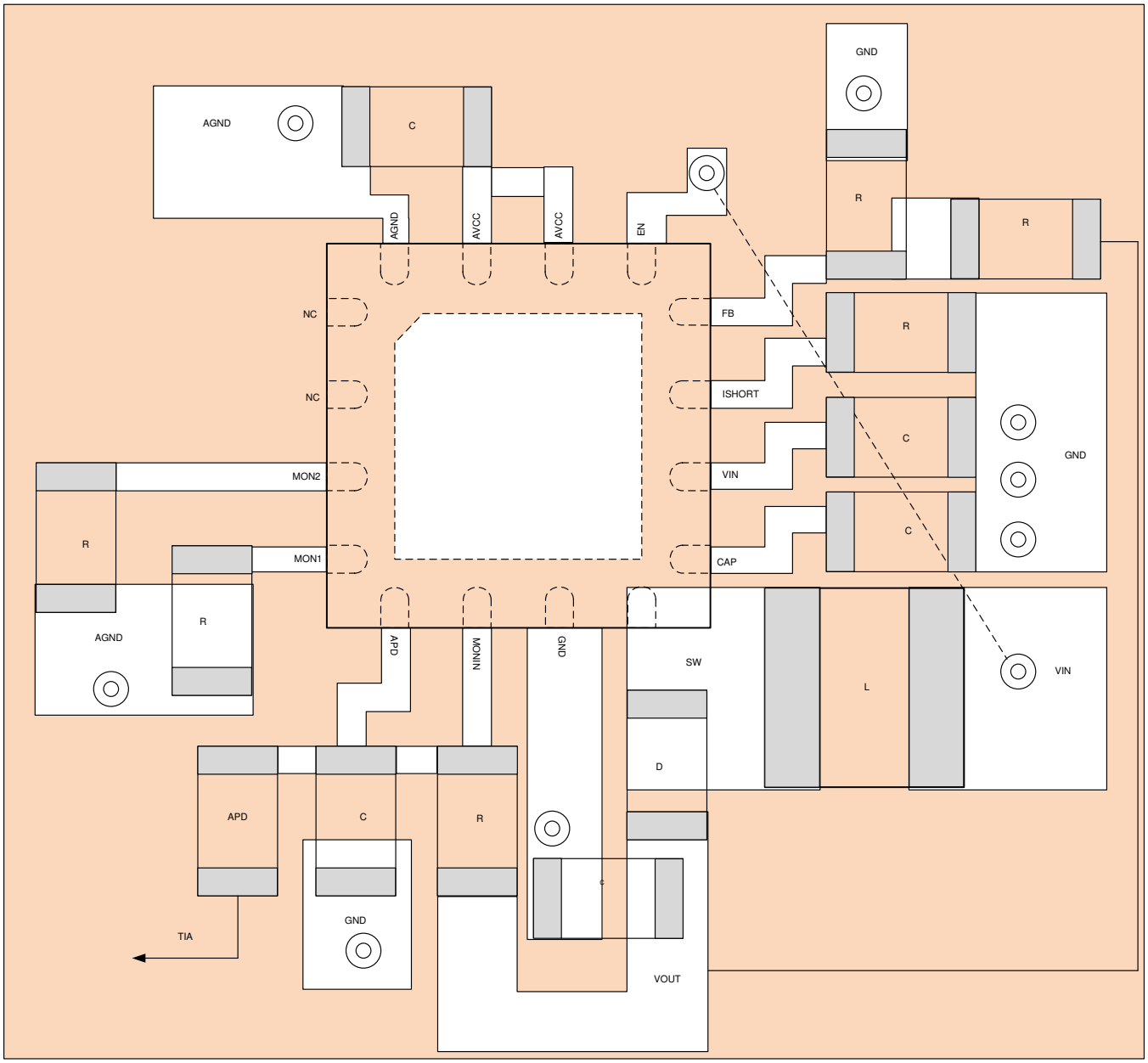


Figure 13. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- TPS61391EVM-058 Evaluation Module User's Guide, SLVUBS9

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

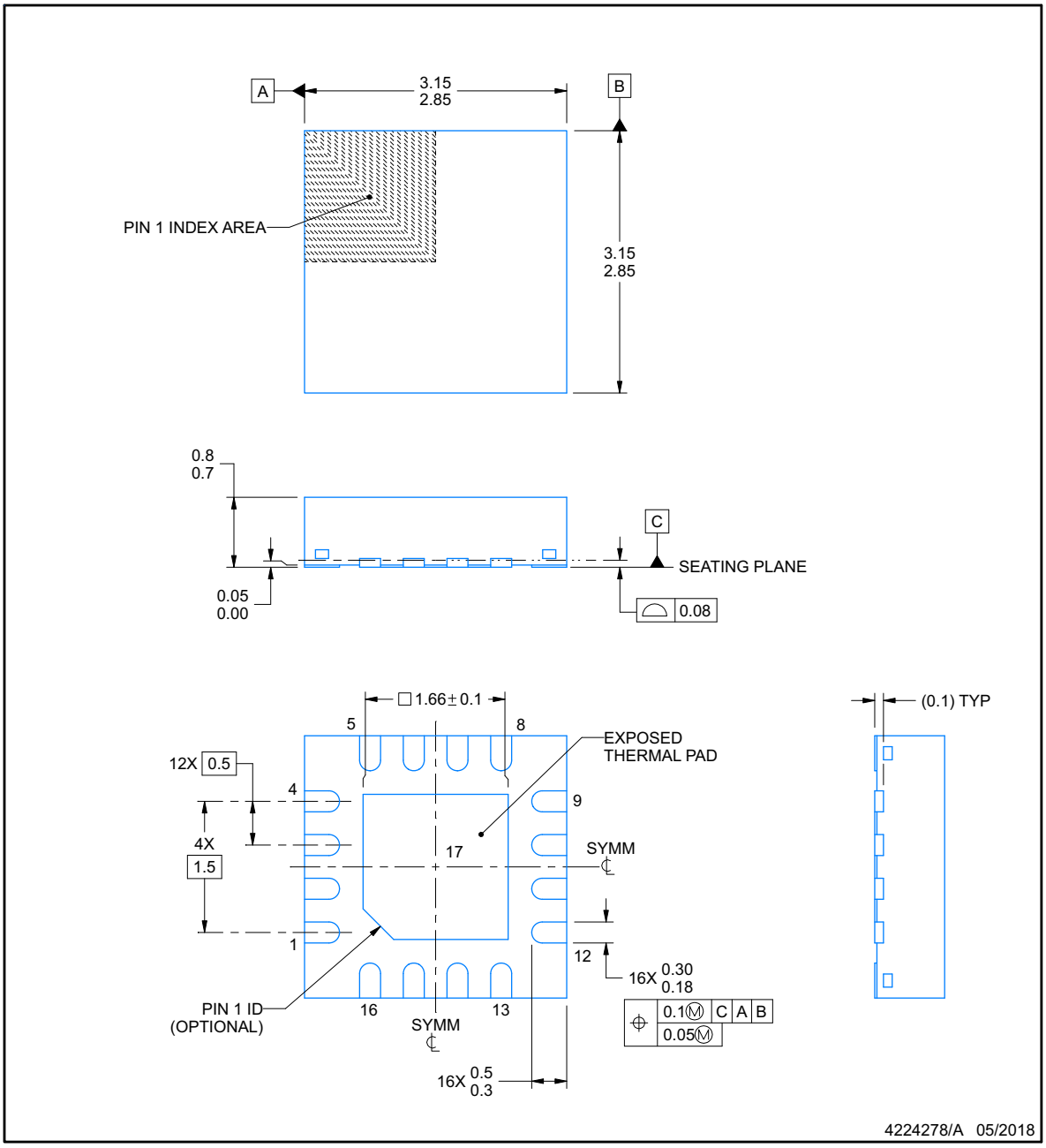
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

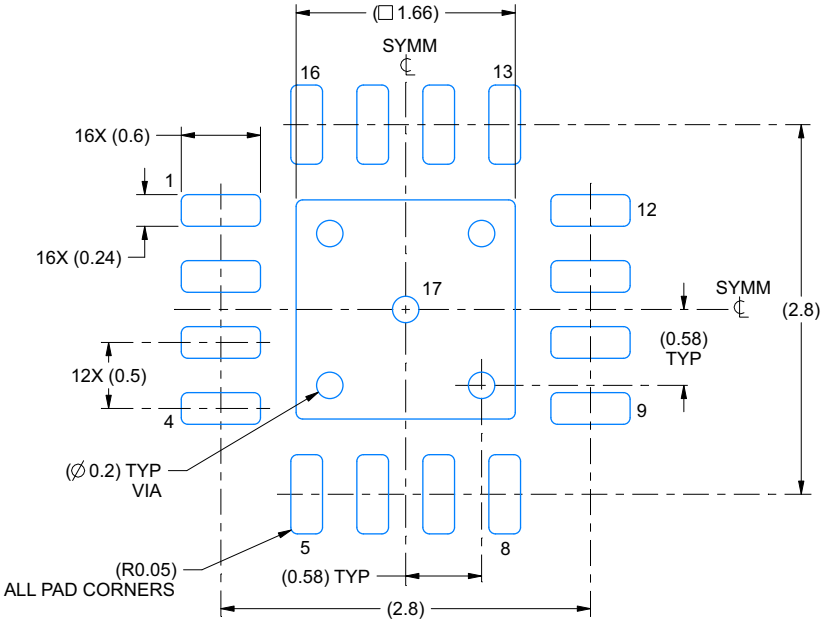
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

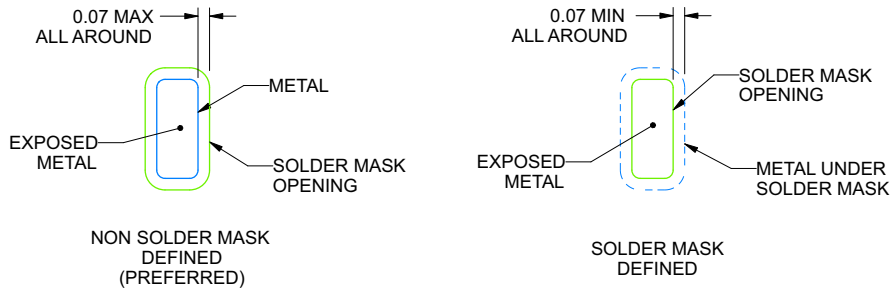
RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224278/A 05/2018

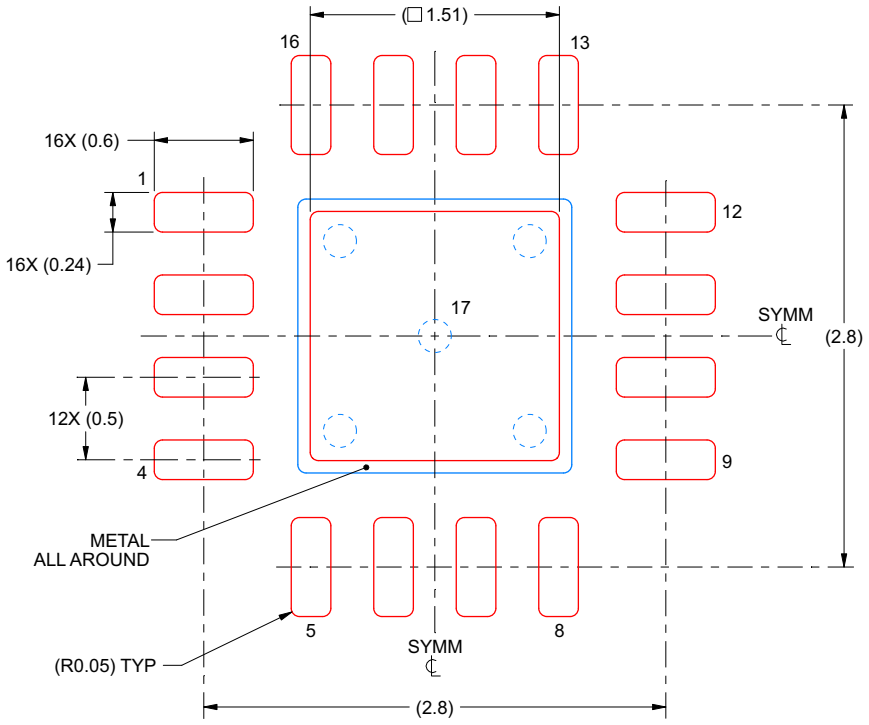
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016J — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224278/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61391RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	22GH
TPS61391RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	22GH
TPS61391RTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	22GH
TPS61391RTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	22GH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

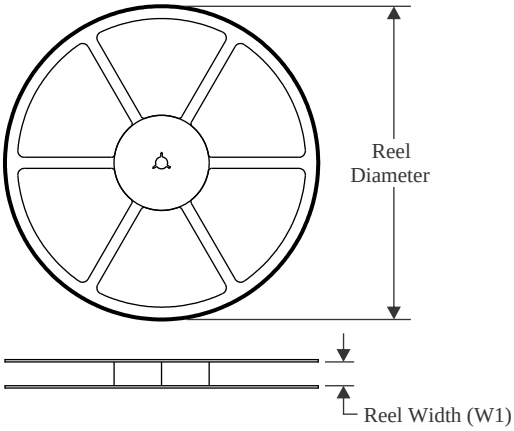
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

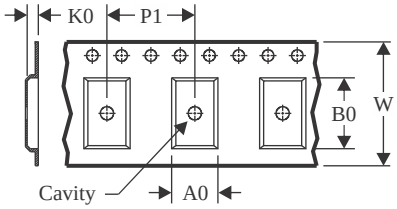
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

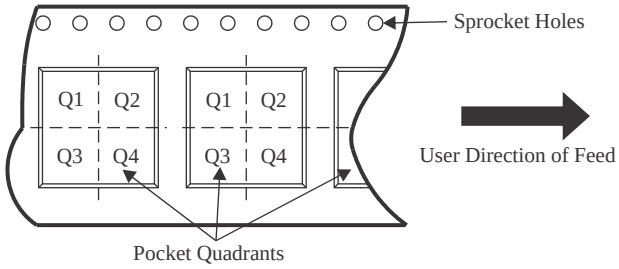


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

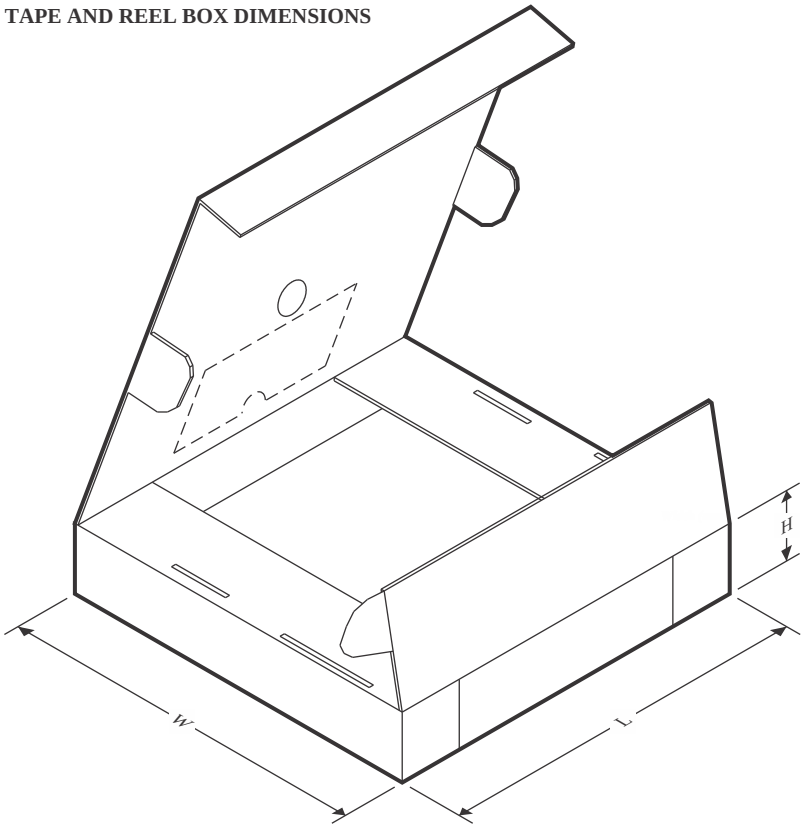
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61391RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61391RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61391RTER	WQFN	RTE	16	3000	360.0	360.0	36.0
TPS61391RTET	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

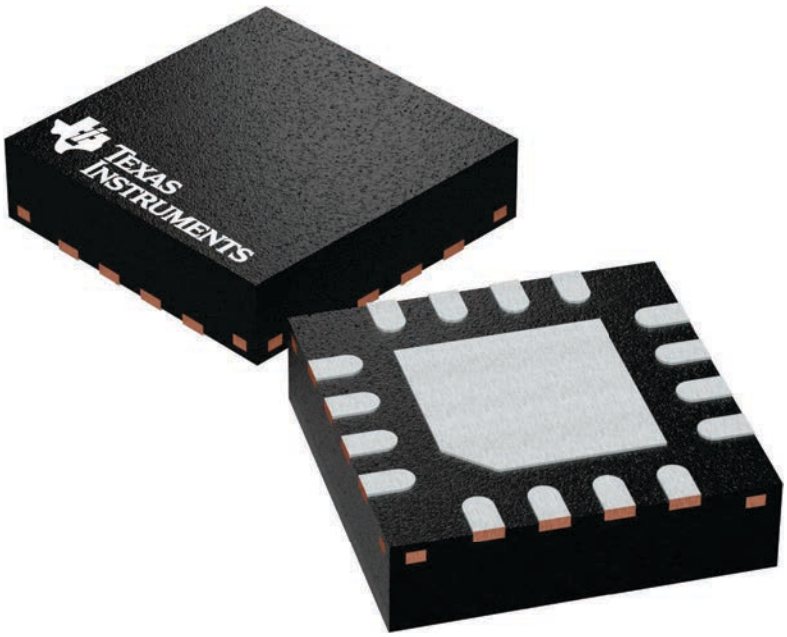
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

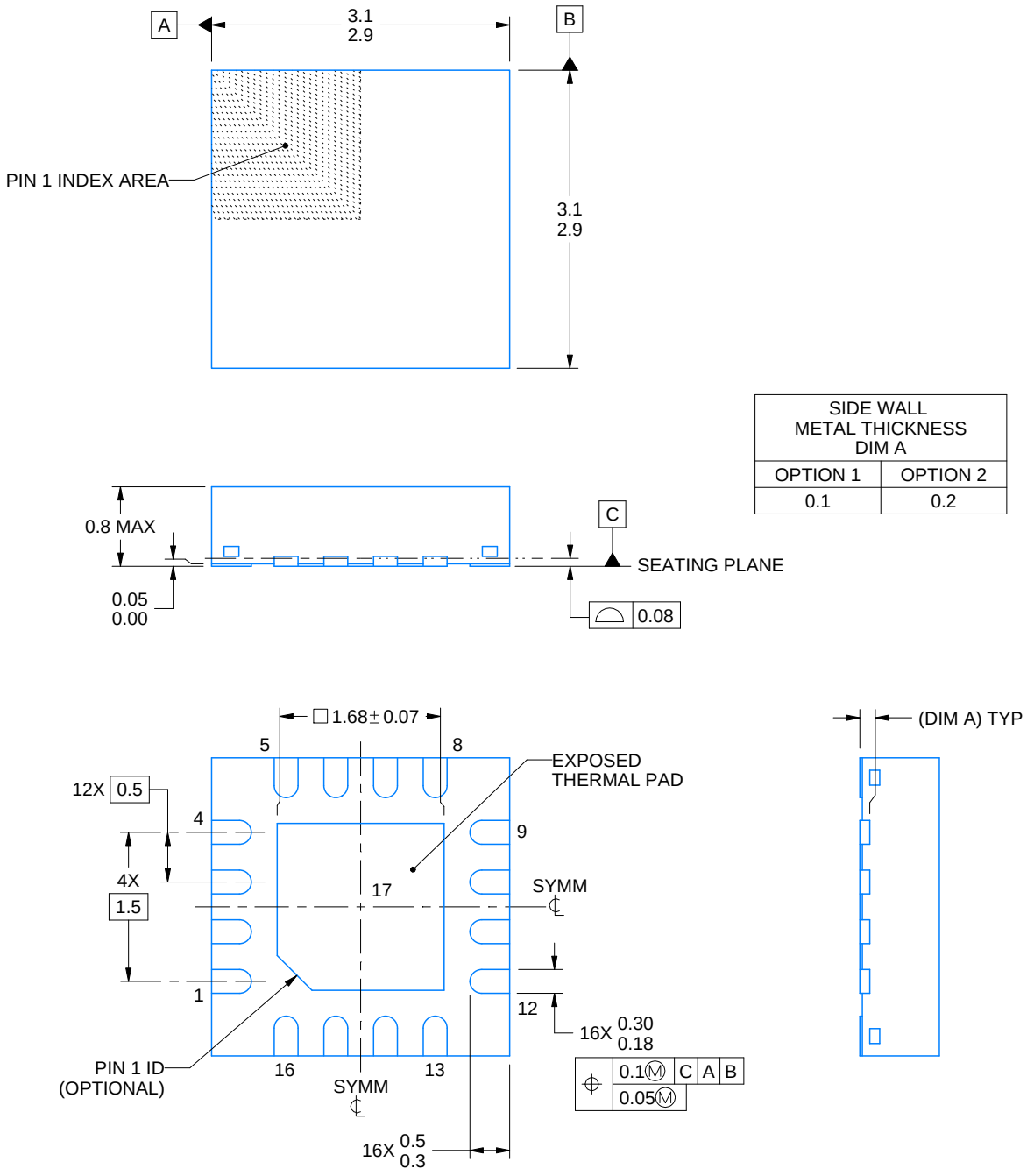


RTE0016C

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
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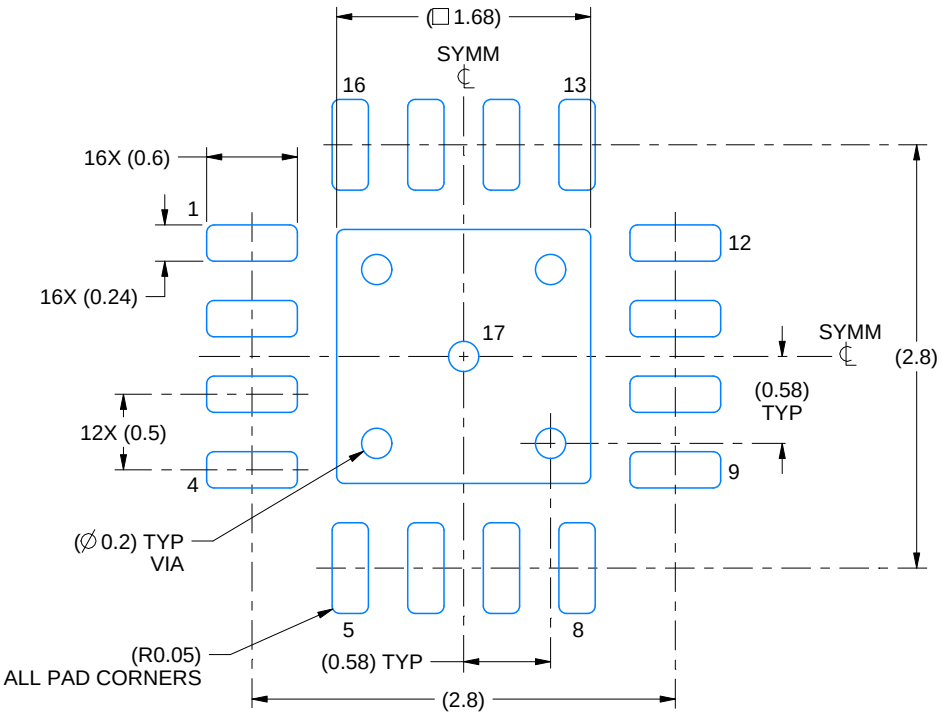
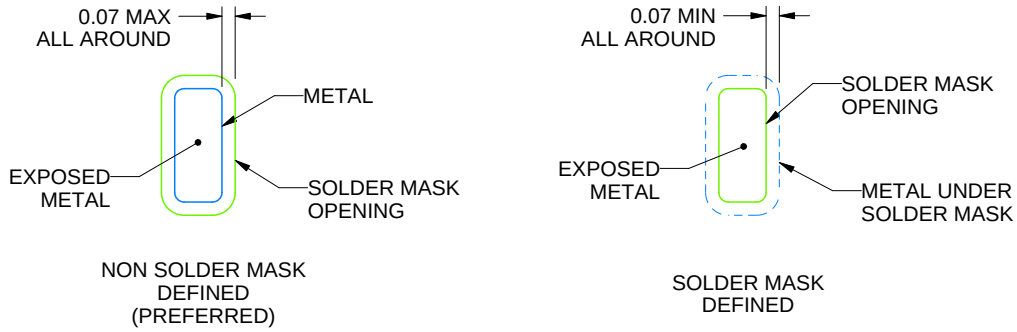


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

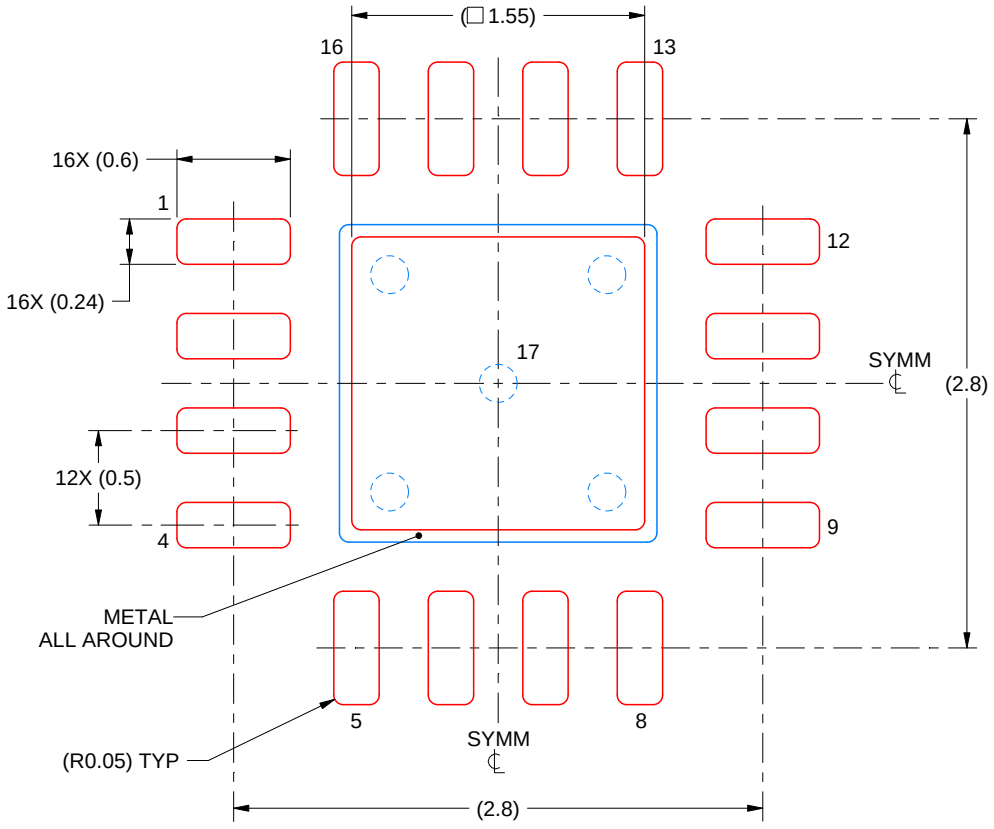


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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