TPS6215xA-Q1 3-V to 17-V 1 A Step-Down Converter with DCS-Control™

1 Features

- DCS-Control™ topology
- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade: –40°C to 125°C operating junction temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Input voltage range: 3 V to 17 V
- Adjustable output voltage from 0.9 Vto 6 V
- Pin-Selectable output voltage (nominal, +5%)
- Programmable soft start and tracking
- Seamless power save mode transition
- Quiescent current of 17 µA (typ.)
- Selectable operating frequency
- Power good output
- 100% duty cycle mode
- Short circuit protection
- Over temperature protection
- Pin-to-pin compatible with TPS62130A-Q1
- Available in a 3-mm × 3-mm, VQFN-16 package
- Create a custom design using the TPS62150A-Q1 with the WEBENCH® Power Designer

2 Applications

- ADAS camera
- Car access and security systems
- Automotive lighting
- Infotainment, CAN-, USB- power supply

3 Description

The TPS62150A-Q1 device is an easy-to-use synchronous step-down DC-DC converter optimized for applications with high power density. A high switching frequency of typically 2.5 MHz allows the use of small inductors and provides fast transient response as well as high output-voltage accuracy through the use of the DCS-Control™ topology.

With a wide operating input-voltage range of 3 to 17 V, the device is ideally suited for systems powered from intermediate bus power rails. The device supports up to 1A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

The output-voltage startup ramp is controlled by the soft-start pin, which allows operation as either a standalone power supply or in tracking configurations. Power sequencing is also possible by configuring the enable and open-drain power-good pins.

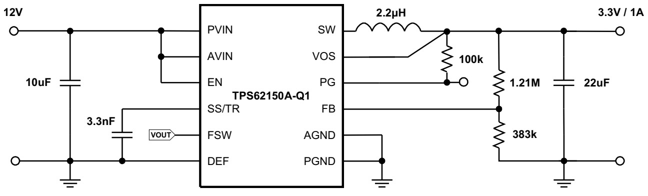
In power save mode, the device shows quiescent current of about 17 µA from V_{IN}. Power save mode which is entered automatically and seamlessly if the load is small, maintains high efficiency over the entire load range. In shutdown mode, the device is turned off and shutdown current consumption is less than 2 µA. The device is packaged in a 16-pin VQFN package measuring 3 × 3 mm (RGT).

Device Information(1)

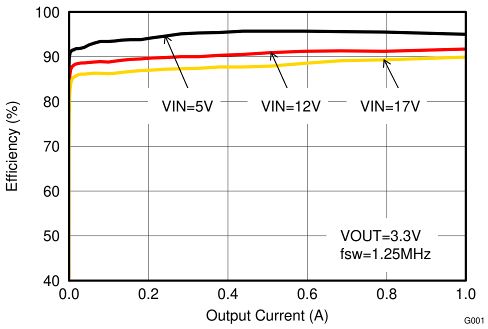
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62150A-Q1	VQFN (16)	3.00 x 3.00 mm
TPS62152A-Q1		
TPS62153A-Q1		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



Efficiency versus Output Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2019) to Revision D	Page
• Added functional safety bullet in the *Features*	1

Changes from Revision B (July 2017) to Revision C	Page
• Added initial release of the TPS62152A-Q1.	1

Changes from Revision A (November 201 6) to Revision B	Page
• Added WEBENCH® links throughout document	1
• Changed "LOG" pin to "FSW" pin on the *Pin Configuration and Functions* and added FSW description throughout the document.	3
• Added SW (AC) spec to the *Absolute Maximum Ratings* table	4
• Added *Power Good Pin Logic Table* and Frequency Selection (FSW) section regarding pin control.	12

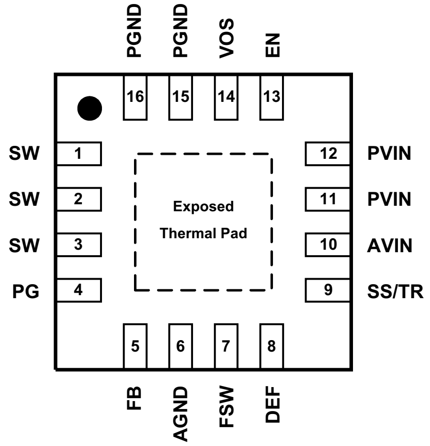
Changes from Original (May 2014) to Revision A	Page
• Added *Pin to Pin Compatible* to Features list	1
• Moved T_{stg} spec from *Handling Ratings* table to *Absolute Maximum Ratings* table	4
• Changed *Thermal Information*	4
• Added body diodes to *Functional Block Diagrams*	8
• Changed text in *Input Capacitor* section for clarity	15
• Added more Switching Frequency graphs to *Application Curves* section	20
• Changed resistor value at the LED from 0.1 Ω to 0.3 Ω in *Figure 40*	24
• Deleted decoupling capacitor from figures in the *Various Output Voltages* section	25
• Added *Receiving Notification of Documentation Updates* and *Support Resources* sections.	29

5 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE	PACKAGE MARKING
TPS62150A-Q1	Adjustable	PA8IQ
TPS62152A-Q1	3.3 V	152Q1
TPS62153A-Q1	5 V	PA8JQ

6 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN[1]		I/O	DESCRIPTION
NAME	NO.		
SW	1,2,3	O	Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.
PG	4	O	Output power good (High = VOUT ready, Low = VOUT below nominal regulation) ; open drain (requires pullup resistor)
FB	5	I	Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance.
AGND	6		Analog Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
FSW	7	I	Switching Frequency Select (Low = 2.5 MHz, High = 1.25 MHz for typical operation)[2]
DEF	8	I	Output Voltage Scaling (Low = nominal, High = nominal + 5%)[2]
SS/TR	9	I	Soft-Start / Tracking Pin. An external capacitor connected to this pin sets the internal voltage reference rise time. It can be used for tracking and sequencing.
AVIN	10	I	Supply voltage for control circuitry. Connect to same source as PVIN.
PVIN	11,12	I	Supply voltage for power stage. Connect to same source as AVIN.
EN	13	I	Enable input (High = enabled, Low = disabled)[2]
VOS	14	I	Output voltage sense pin and connection for the control loop circuitry
PGND	15,16		Power Ground. Must be connected directly to the Exposed Thermal Pad and common ground plane.
Exposed Thermal Pad			Must be connected to AGND (pin 6), PGND (pin 15, 16), and common ground plane[3]. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

(1) For more information about connecting pins, see *Detailed Description* and *Application and Implementation* sections.
(2) An internal pulldown resistor keeps logic level low, if pin is floating.
(3) See Figure 50.

7 Specifications

7.1 Absolute Maximum Ratings

See (1)		MIN	MAX	UNIT
Pin voltage (2)	AVIN, PVIN	–0.3	20	V
	EN, SS/TR, SW (DC)	–0.3	V_{IN}+0.3	
	SW (AC), less than 10ns (3)	–2	24.5	
	DEF, FSW, FB, PG, VOS	–0.3	7	V
Power Good sink current	PG		10	mA
Temperature	Operating junction temperature range, T_J	–40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) While switching.

7.2 Handling Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (2)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±500	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
Supply Voltage, V_{IN} (at AVIN and PVIN)	3		17	V
Output Voltage Range, V_{OUT} (TPS62150A-Q1)	0.9		6	V
Operating junction temperature, T_J	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TPS6215xA-Q1	UNIT
		RGT	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over junction temperature range (T_J = -40°C to +125°C), typical values at V_{IN} = 12 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		3		17	V
I_Q	Operating quiescent current	EN = High, I_{OUT} = 0 mA, device not switching		17	30	µA
I_{SD}	Shutdown current(1)	EN = Low		1.5	25	µA
V_{UVLO}	Undervoltage lockout threshold	Falling Input Voltage (PWM mode operation)	2.6	2.7	2.8	V
		Hysteresis		200		mV
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hysteresis			20		
CONTROL (EN, DEF, FSW, SS/TR, PG)						
V_H	High level input threshold voltage (EN, DEF, FSW)		0.9			V
V_L	Low level input threshold voltage (EN, DEF, FSW)				0.3	V
I_{LKG}	Input leakage current (EN, DEF, FSW)	EN = V_{IN} or GND; DEF = V_{OUT} or GND; FSW = GND		0.01	1	µA
V_{TH_PG}	Power good threshold voltage	Rising (%V_{OUT})	92%	95%	98%	
		Falling (%V_{OUT})	87%	90%	94%	
V_{OL_PG}	Power good output low	I_{PG} = –2 mA		0.07	0.3	V
I_{LKG_PG}	Input leakage current (PG)	V_{PG} = 1.8 V		1	400	nA
$I_{SS/TR}$	SS/TR pin source current		2.3	2.5	2.7	µA
POWER SWITCH						
$R_{DS(ON)}$	High-side MOSFET ON-resistance	V_{IN} ≥ 6 V		90	170	mΩ
		V_{IN} = 3 V		120		
	Low-side MOSFET ON-resistance	V_{IN} ≥ 6 V		40	70	mΩ
		V_{IN} = 3 V		50		
I_{LIMF}	High-side MOSFET forward current limit	V_{IN} = 12 V, T_A = 25°C	1.4	1.7	2.2	A
OUTPUT						
VREF	Internal reference voltage			0.8		V
I_{LKG_FB}	Input leakage current (FB)	V_{FB} = 0.8 V		1	100	nA
V_{OUT}	Output voltage range (TPS62150A-Q1)	V_{IN} ≥ V_{OUT}	0.9		6.0	V
	DEF (Output voltage programming)	DEF = 0 (GND)		VOUT		
		DEF = 1 (V_{OUT})		VOUT+5%		
	Output voltage accuracy(2)	PWM mode operation, V_{IN} ≥ V_{OUT} +1 V	–1.8%		1.8%	
		Power Save Mode operation, C_{OUT} = 22 µF	–2.3%		2.8%	
	Load regulation	V_{IN} = 12 V, V_{OUT} = 3.3 V, PWM mode operation		0.05		%/A
	Line regulation	3 V ≤ V_{IN} ≤ 17 V, V_{OUT} = 3.3 V, I_{OUT} = 1 A, PWM mode operation		0.02		%/V

(1) Current into AVIN+PVIN pin.
(2) This is the regulation accuracy of the voltage at the FB pin (adjustable version) and of the output voltage (fixed version).

7.6 Typical Characteristics

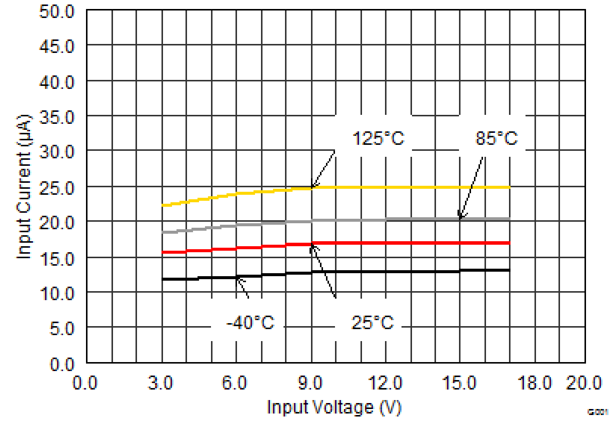


Figure 1. Quiescent Current

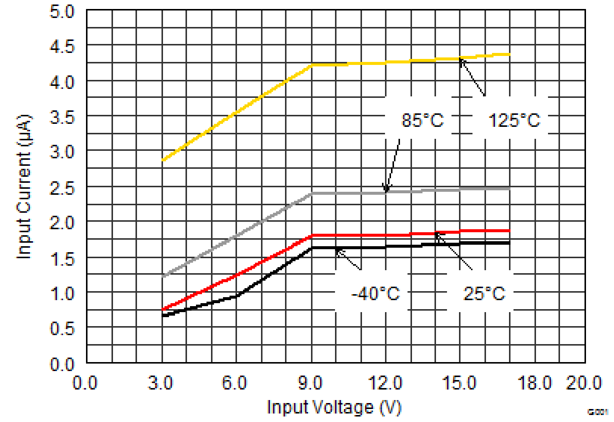


Figure 2. Shutdown Current

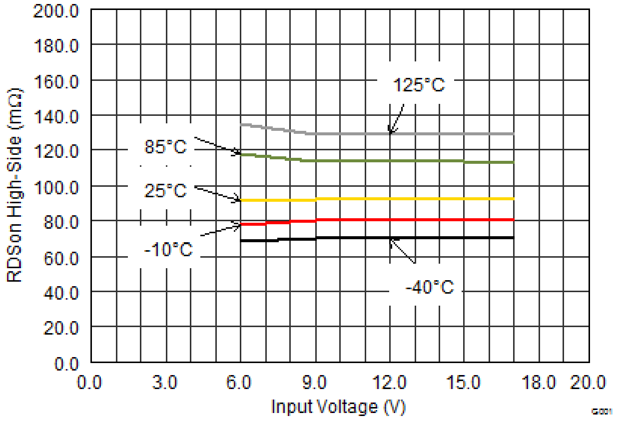


Figure 3. High-side Switch Resistance

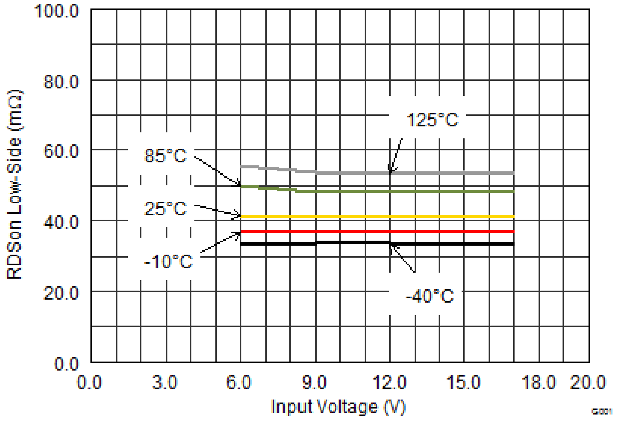


Figure 4. Low-Side Switch Resistance

8 Parameter Measurement Information

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17-V, 1-A Step-Down Converter, VQFN	TPS62150AQRGT, Texas Instruments
L1	2.2 µH, 0.165 x 0.165 in	XFL4020-222MEB, Coilcraft
C1	10 µF, 25 V, Ceramic, 1210	Standard
C3	22 µF, 6.3 V, Ceramic, 0805	Standard
C5	3300 pF, 25 V, Ceramic, 0603	
R1	Depending on Vout	
R2	Depending on Vout	
R3	100 kΩ, Chip, 0603, 1/16W, 1%	Standard

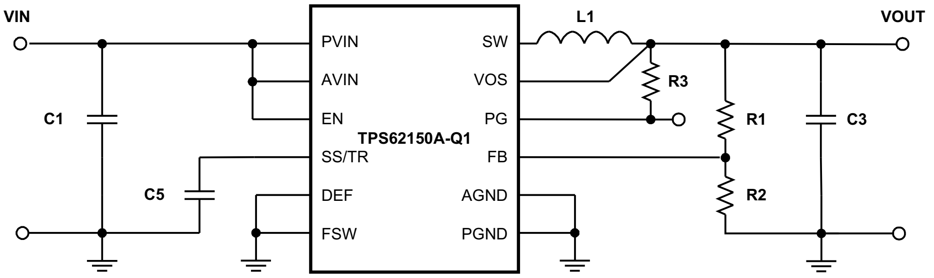


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Figure 5. Measurement Setup (High Switching Frequency)

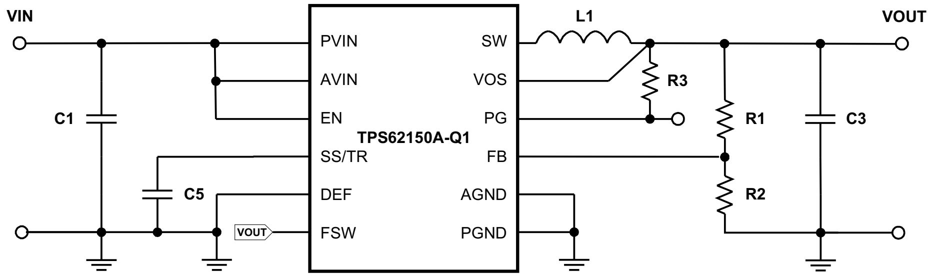

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Figure 6. Measurement Setup (Low Switching Frequency)

9 Detailed Description

9.1 Overview

The TPS6215xA-Q1 synchronous switched mode power converters are based on DCS-Control™ (**D**irect **C**ontrol with **S**eamless Transition into Power Save Mode), an advanced regulation topology that combines the advantages of hysteretic, voltage mode, and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5 MHz or 1.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Modek, the switching frequency decreases linearly with the load current. Since DCS-Control supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without affecting the output voltage.

9.2 Functional Block Diagram

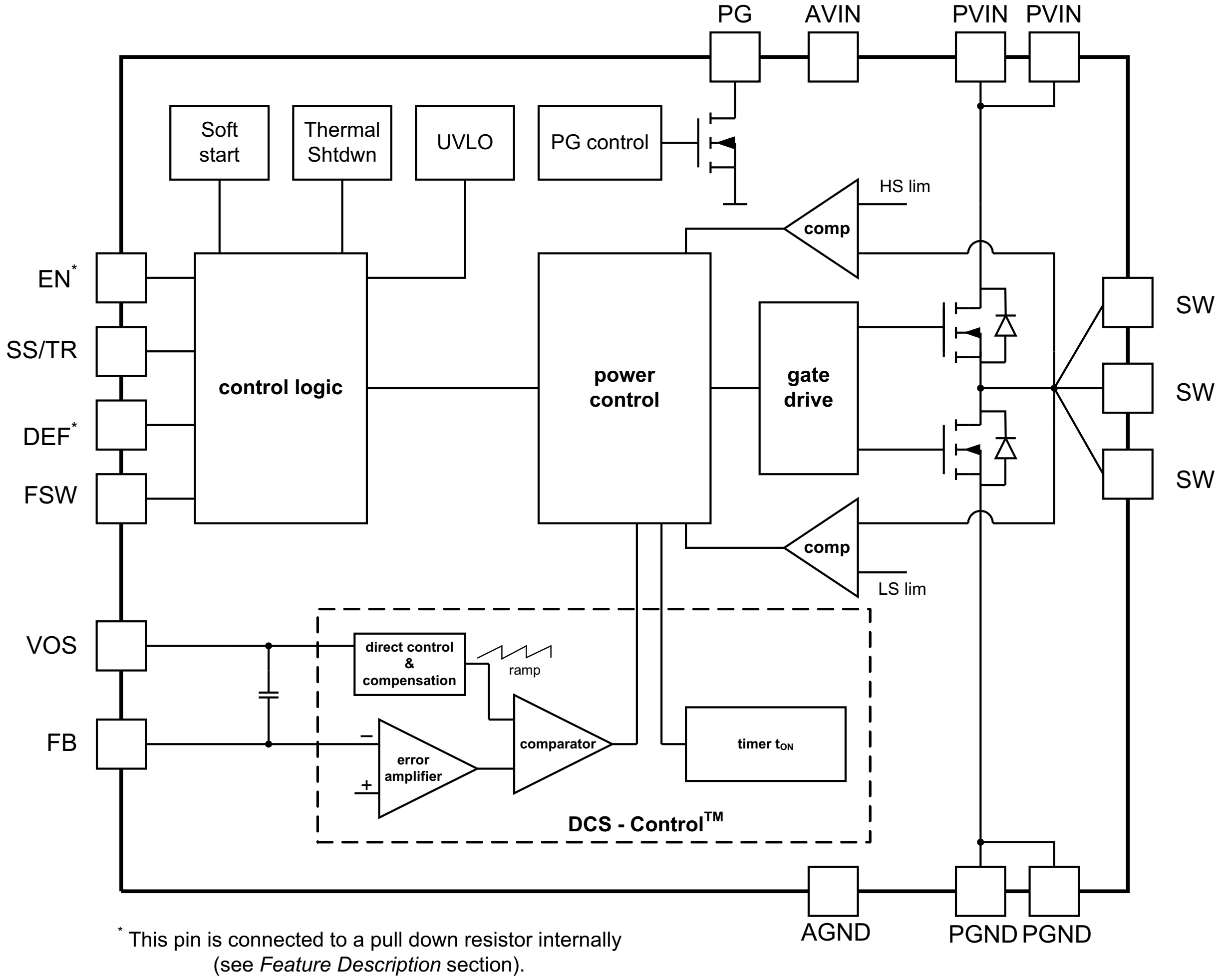

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Figure 7. TPS62150A-Q1 (Adjustable Output Voltage)

Functional Block Diagram (continued)

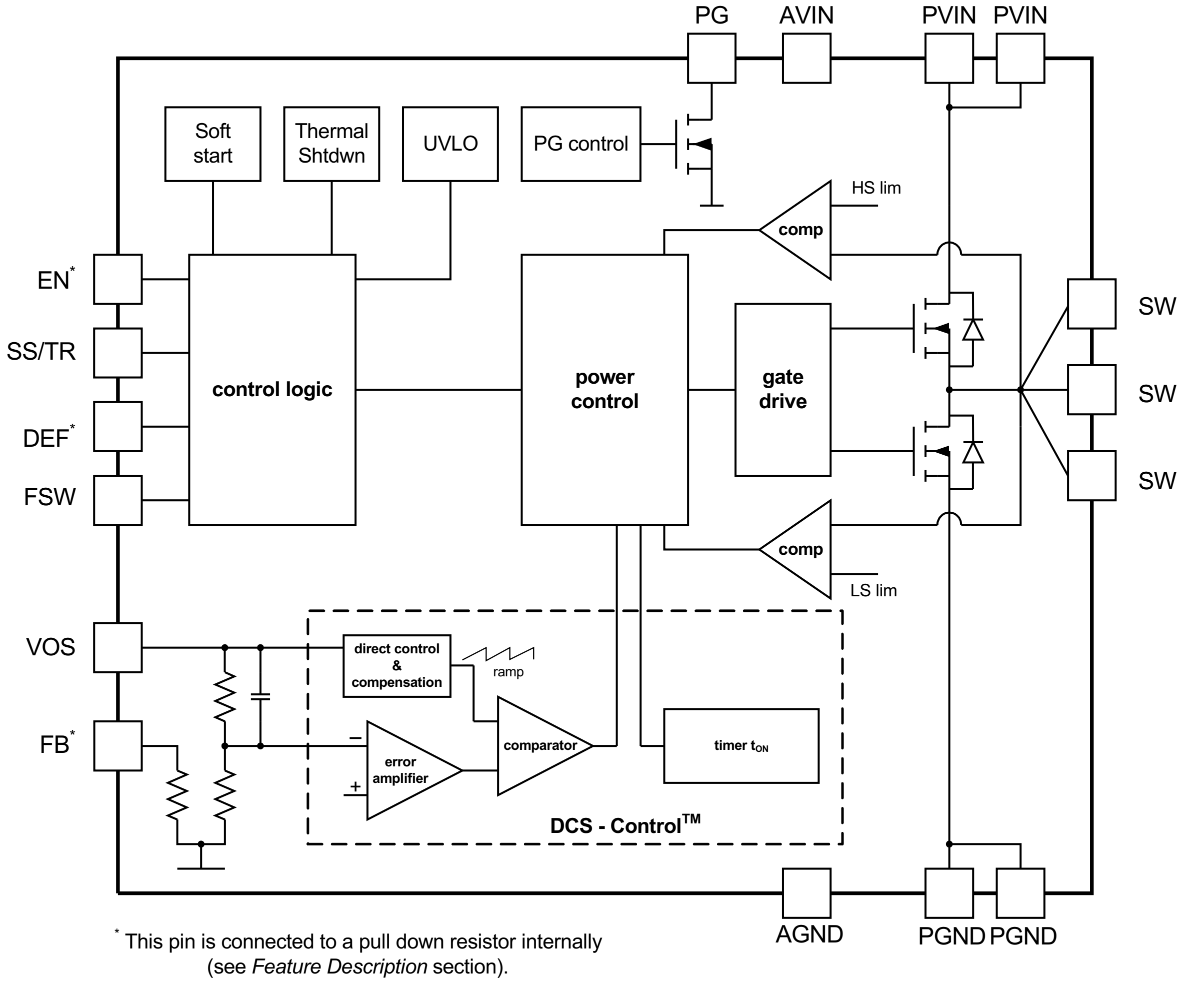

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Figure 8. TPS62153A-Q1 (5-V Fixed Output Voltage)

9.3 Feature Description

9.3.1 Pulse Width Modulation (PWM) Operation

The TPS6215xA-Q1 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz or 1.25 MHz, selectable with the FSW pin. The frequency variation in PWM is controlled and depends on V_{IN}, V_{OUT}, and the inductance. The device operates in PWM mode as long the output current is higher than half the ripple current of the inductor. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). PSM operation occurs if the output current becomes smaller than half the ripple current of the inductor.

9.3.2 Power Save Mode Operation

The built-in Power Save Mode of the TPS6215xA-Q1 is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode, the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode happens within the entire regulation scheme and is seamless in both directions.

Feature Description (continued)

TPS6215xA-Q1 includes a fixed on-time circuitry. This on-time, in steady-state operation with FSW = Low, can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 400ns \tag{1}$$

For very small output voltages, an absolute minimum on-time of about 80 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Also, the off-time can reach its minimum value at high duty cycles. The output voltage remains regulated in such case. Using t_{ON}, the typical peak inductor current in Power Save Mode can be approximated by:

$$I_{LPSM(peak)} = \frac{(V_{IN} - V_{OUT})}{L} \cdot t_{ON} \tag{2}$$

When V_{IN} decreases to typically 15% above VOUT, the TPS6215xA-Q1 does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

9.3.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D = Vout / Vin and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences (for example, for longest operation time of battery-powered applications). In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT}\left(R_{DS(on)} + R_L\right)$$

where

- I_{OUT} is the output current
- $R_{DS(on)}$ is the $R_{DS(on)}$ of the high-side FET
- R_L is the DC resistance of the inductor used (3)

9.3.4 Enable / Shutdown (EN)

When Enable (EN) is set High, the device starts operation. Shutdown is forced if EN is pulled low with a shutdown current of typically 1.5 µA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. The EN signal must be set externally to High or Low. The typical threshold values are 0.65 V (rising) and 0.45 V (falling). An internal pulldown resistor of about 400 kΩ is connected and keeps EN logic low, if Low is set initially and then the pin gets floating. It is disconnected if the pin is set High.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

9.3.5 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up, avoiding excessive inrush current and ensuring a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50 µs and VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin. See Figure 38 and Figure 39 for typical start-up operation.

Using a very small capacitor (or leaving SS/TR pin un-connected) provides the fastest start-up behavior. The TPS6215xA-Q1 can start into a pre-biased output. During monotonic pre-biased start-up, both of the power MOSFETs are not allowed to turn on until the internal ramp of the device sets an output voltage above the pre-bias voltage. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

Feature Description (continued)

A voltage supplied to SS/TR can be used for tracking a master voltage. The output voltage follows this voltage in both directions up and down (see the *Application and Implementation* section).

9.3.6 Current Limit And Short Circuit Protection

The TPS6215xA-Q1 is protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET turns off. Avoiding shoot through current, the low-side FET switches on to allow the inductor current to decrease. The high-side FET turns on again, only if the current in the low-side FET has decreased below the low-side current limit threshold.

The output current of the device is limited by the current limit (see the Electrical Characteristics). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD}$$

where

- I_{LIMF} is the static current limit, specified in the
- L is the inductor value
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- t_{PD} is the internal propagation delay (4)

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns \tag{5}$$

9.3.7 Power Good (PG)

The TPS6215xA-Q1 has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. TPS6215xA-Q1 features PG = Low when the device is turned off due to EN, UVLO, or thermal shutdown and can be used to actively discharge Vout (see Figure 42). VIN must remain present for the PG pin to stay Low. If unused, the PG pin can be left floating.

Table 2. Power Good Pin Logic Table

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable (EN = High)	$V_{FB} \geq V_{TH\_PG}$	√	
	$V_{FB} \leq V_{TH\_PG}$		√
Shutdown (EN = Low)			√
UVLO	$0.7\text{ V} < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\text{ V}$	√	

9.3.8 Pin-Selectable Output Voltage (DEF)

The output voltage of the TPS6215xA-Q1 can be increased by 5% above the nominal voltage by setting the DEF pin to High (1). When DEF is Low, the device regulates to the nominal output voltage. Increasing the nominal voltage allows adapting the power supply voltage to the variations of the application hardware. More detailed information on voltage margining using TPS6215xA-Q1 can be found in the *Voltage Margining Using the TPS62130 Application Report*. A pulldown resistor of about 400 kΩ is internally connected to the pin to ensure a proper logic level if the pin is high impedance or floating after initially set to Low. The resistor is disconnected if the pin is set High.

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(1) Maximum allowed voltage is 7V. Therefore it's recommended to connect it to VOUT, not VIN.

9.3.9 Frequency Selection (FSW)

To get high power density with very small solution size, a high switching frequency allows the use of small external components for the output filter. However, switching losses increase with the switching frequency. If efficiency is the key parameter, more than solution size, the switching frequency can be set to half (1.25 MHz typ.) by pulling FSW to High. Running with lower frequency, a higher efficiency, but also a higher output voltage ripple, is achieved. Pull FSW to Low for high frequency operation (2.5 MHz typ.). To get low ripple and full output current at the lower switching frequency, it is recommended to use an inductor of at least 2.2 µH. The switching frequency can be changed during operation, if needed. A pulldown resistor of about 400 kΩ is internally connected to the pin, acting the same way as at the DEF Pin (see *Pin-Selectable Output Voltage (DEF)*).

9.3.10 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents misoperation of the device by switching off both the power FETs. The undervoltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

9.3.11 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ.), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes Low. When T_J decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shutdown temperature.

9.4 Device Functional Modes

9.4.1 Operation above T_J = 125°C

The operating junction temperature of the device is specified up to 125°C. In power supply circuits, the self-heating effect causes that the junction temperature, T_J, is even higher than the ambient temperature T_A. Depending on T_A and the load current, the maximum operating T_J can be exceeded. However, the electrical characteristics are specified up to a T_J of 125°C only. The device operates as long as thermal shutdown threshold is not triggered.

9.4.2 Operation with V_{IN} < 3 V

The device is functional for supply voltages below 3 V and above the UVLO threshold. Parameters can differ from specified values. The minimum V_{IN} value of 3 V is not violated by UVLO threshold and hysteresis variations.

9.4.3 Operation with separate EN Control

The EN pin can be connected to V_{IN} or be controlled separately. While the EN control voltage level can be lower than the actual V_{IN} value, it must not exceed V_{IN} to avoid damage of the device. This can happen at low V_{IN}, during start-up, or power sequencing.

10 Application and Implementation

10.1 Application Information

TPS62150xA-Q1 are synchronous switch mode step-down converters, able to convert a 3-V to 17-V input voltage into a lower, 0.9-V to 6-V, output voltage, providing up to 1-A load current. The following section gives guidance on choosing external components to complete the power supply design. *Application Curves* are included for the typical application.

10.2 Typical Application

10.2.1 TPS62150A-Q1 Point-Of-Load Step Down Converter

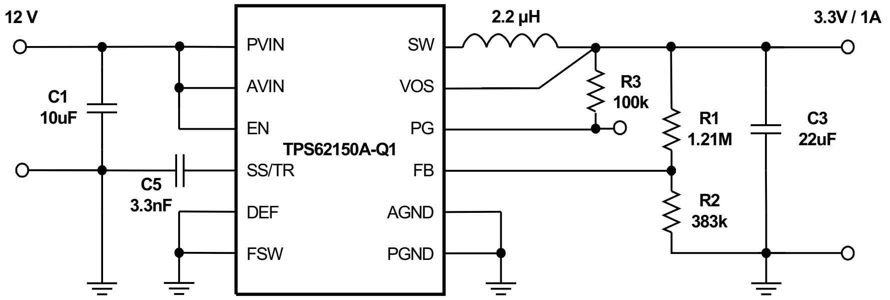

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Figure 9. Typical Schematic for 3.3-V Step-Down Converter

10.2.1.1 Design Requirements

The step-down converter design can be adapted to different output voltage and load current needs by choosing external components appropriate. The following design procedure is adequate for whole VIN, VOUT, and load current range of TPS62150A-Q1. Using Table 3, the design procedure needs minimum effort.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62150A-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.1.2.2 Programming The Output Voltage

The TPS6215xA-Q1 can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from Equation 6 (see Figure 5). It is recommended to choose resistor values which allow a current of at least 2 µA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

Typical Application (continued)

$$R_1 = R_2\left(\frac{V_{OUT}}{0.8V} - 1\right) \tag{6}$$

In case the FB pin gets opened, the device clamps the output voltage at the VOS pin internally to approximately 7.4 V.

10.2.1.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device. The TPS6215xA-Q1 is optimized to work within a range of external components. The inductance and capacitance of the LC output filter must be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability*). Table 3 can be used to simplify the output filter component selection.

Table 3. Recommended LC Output Filter Combinations(1)

	4.7 µF	10 µF	22 µF	47 µF	100 µF	200 µF	400 µF
0.47 µH							
1 µH			√	√	√	√	
2.2 µH		√	√(2)	√	√	√	
3.3 µH		√	√	√	√		
4.7 µH							

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.

The TPS6215xA-Q1 can be run with an inductor as low as 1 µH. FSW must be set Low in this case. However, for applications running with the low frequency setting (FSW = High) or with low input voltages, 2.2 µH is recommended.

More detailed information on further LC combinations can be found in the *Optimizing the TPS62130/40/50/60 Output Filter Application Report*.

10.2.1.2.4 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 7 and Equation 8 calculate the maximum inductor current under static load conditions.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{7}$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left(\frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}}\right)$$

where

- I_L(max) is the maximum inductor current
- ΔI_L is the peak-to-peak inductor ripple current
- L(min) is the minimum effective inductor value
- f_{SW} is the actual PWM switching frequency (8)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and solution size as well. The following inductors have been used with the TPS6215xA-Q1 and are recommended for use:

Table 4. List of Inductors[1]

TYPE	INDUCTANCE [µH]	CURRENT [A][2]	DIMENSIONS [LxBxH] mm	MANUFACTURER
XFL4020-102ME_	1.0 µH, ±20%	4.7	4 x 4 x 2.1	Coilcraft
XFL4020-152ME_	1.5 µH, ±20%	4.2	4 x 4 x 2.1	Coilcraft
XFL4020-222ME_	2.2 µH, ±20%	3.8	4 x 4 x 2.1	Coilcraft
IHLP1212BZ-11	1.0 µH, ±20%	4.5	3 x 3.6 x 2	Vishay
IHLP1212BZ-11	2.2 µH, ±20%	3.0	3 x 3.6 x 2	Vishay
SRP4020-3R3M	3.3µH, ±20%	3.3	4.8 x 4 x 2	Bourns
VLC5045T-3R3N	3.3µH, ±30%	4.0	5 x 5 x 4.5	TDK

(1) See *Third-Party Products Disclaimer*.
(2) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2}\Delta I_L \tag{9}$$

Using Equation 8, this current level can be adjusted by changing the inductor value.

10.2.1.2.5 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS6215xA-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use an X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see the *Optimizing the TPS62130/40/50/60 Output Filter Application Report*).

NOTE

In power save mode, the output voltage ripple depends on the output capacitance, its ESR, and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

10.2.1.2.6 Input Capacitor

For most applications, 10 µF is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage during transient events and also decouples the converter from the supply. A low ESR, multilayer ceramic capacitor is recommended for best filtering and must be placed between PVIN and PGND as close as possible to those pins. An RC, low-pass filter from PVIN to AVIN can be used, but is not required.

10.2.1.2.7 Soft-start Capacitor

A capacitance connected between the SS/TR pin and AGND allows a user programmable start-up slope of the output voltage. A constant current source supports 2.5 µA to charge the external capacitance. The capacitor required for a given soft-start ramp time for the output voltage is given by:

$$C_{SS} = t_{SS} \cdot \frac{2.5\mu A}{1.25V} \quad [F] \tag{10}$$

where

- C_{SS} is the capacitance (F) required at the SS/TR pin
- t_{SS} is the desired soft-start ramp time (s)

NOTE

DC Bias effect: High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore, the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

10.2.1.2.8 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage. If the tracking voltage is between 50 mV and 1.2 V, the FB pin tracks the SS/TR pin voltage as described in Equation 11 and shown in Figure 10.

$$V_{FB} \approx 0.64 \cdot V_{SS/TR} \tag{11}$$

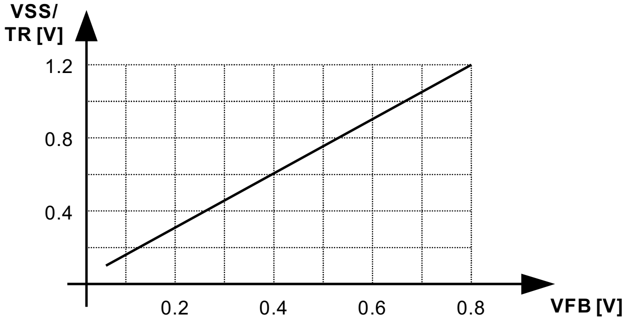

Figure 10. Voltage Tracking Relationship

Once the SS/TR pin voltage reaches about 1.2 V, the internal voltage is clamped to the internal feedback voltage and device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage, the device does not sink current from the output. So, the resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN} + 0.3 V.

If the input voltage drops into undervoltage lockout or even down to zero, the output voltage goes to zero, independent of the tracking voltage. Figure 11 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function.

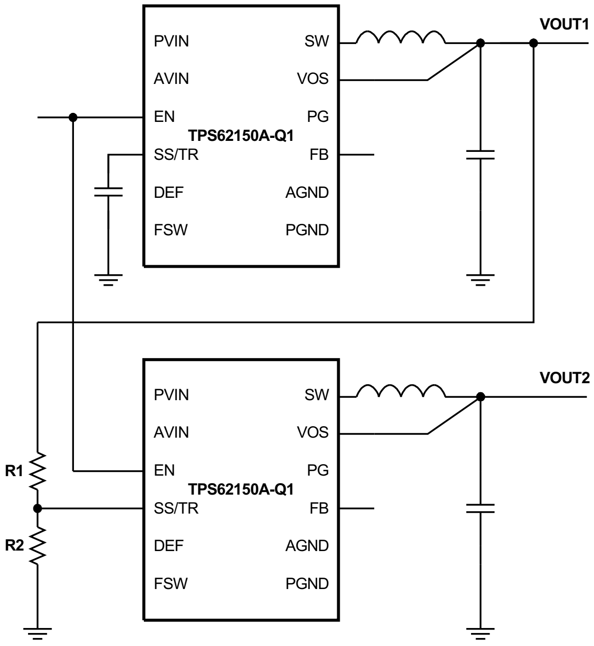

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Figure 11. Sequence for Ratiometric and Simultaneous Start-up

The resistive divider of R1 and R2 can be used to change the ramp rate of VOUT2 faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT1 to the EN pin of VOUT2. Ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. Equation 10 calculates the soft-start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in the *Sequencing and Tracking With the TPS621-Family and TPS821-Family Application Report*.

NOTE

If the voltage at the FB pin is below its typical value of 0.8 V, the output voltage accuracy can have a wider tolerance than specified.

10.2.1.2.9 Output Filter and Loop Stability

The devices of the TPS6215xA-Q1 family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 12:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 3 and are recommended for use. Different values can work, but care has to be taken on the loop stability which is affected. More information including a detailed LC stability matrix can be found in the *Optimizing the TPS62130/40/50/60 Output Filter Application Report*.

The TPS6215xA-Q1 includes an internal 25-pF feedforward capacitor connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 13 and Equation 14:

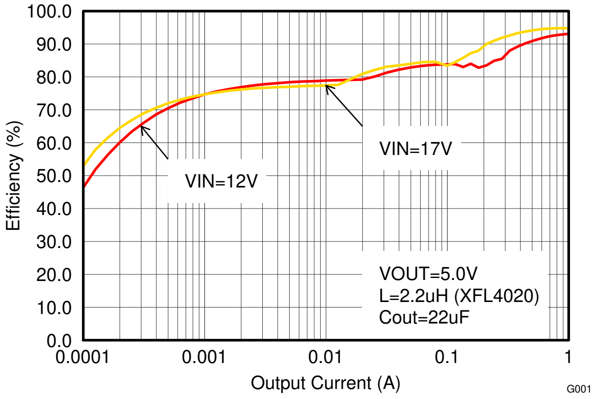
$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25\,pF} \tag{13}$$

$$f_{pole} = \frac{1}{2\pi \cdot 25\,pF} \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \tag{14}$$

Though the TPS6215xA-Q1 is stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in the *Optimizing Transient Response of Internally Compensated DC-DC Converters Application Report* and *Feedforward Capacitor to Improve Stability and Bandwidth of TPS621/821-Family Application Report*.

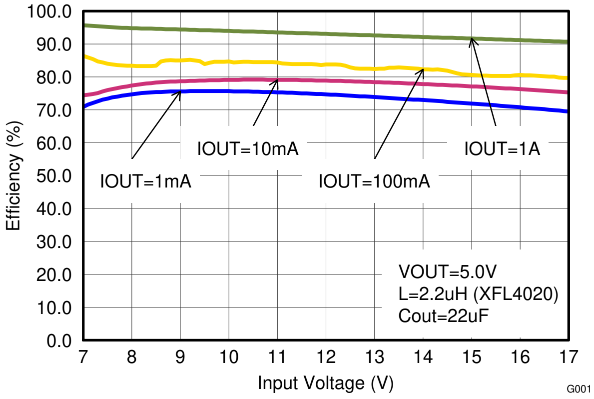
10.2.2 Application Curves

At V_{IN} = 12 V, V_{OUT} = 3.3 V, and T_A = 25°C, FSW = Low, (unless otherwise noted)



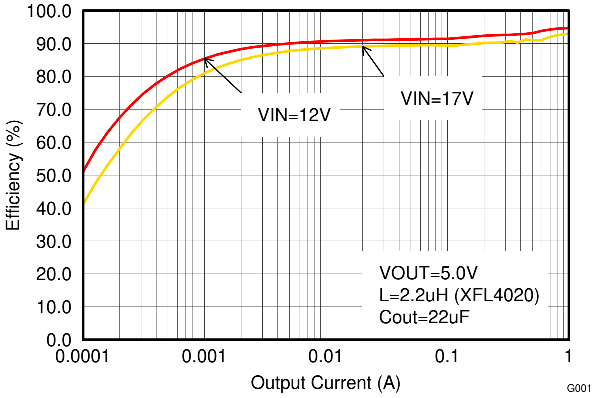
FSW = Low

Figure 12. Efficiency versus Output Current



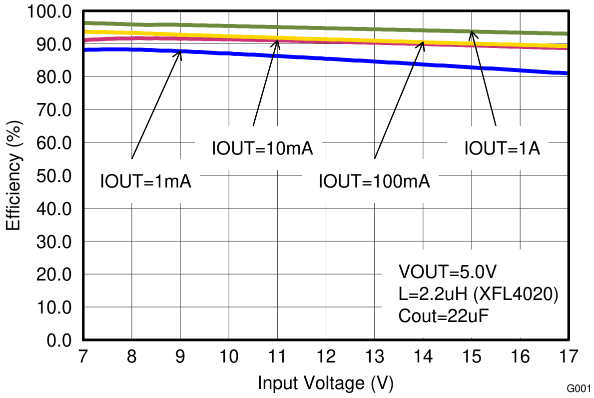
FSW = Low

Figure 13. Efficiency versus Input Voltage



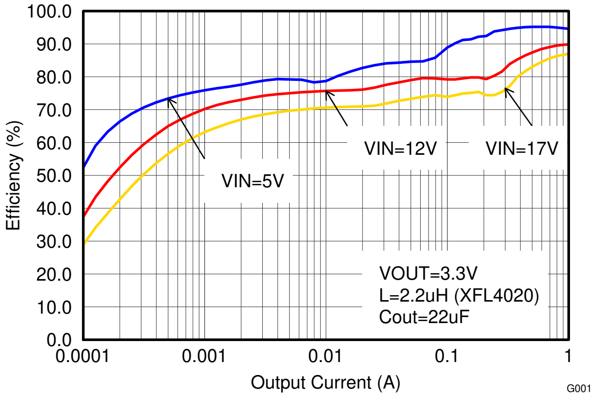
FSW = High

Figure 14. Efficiency versus Output Current



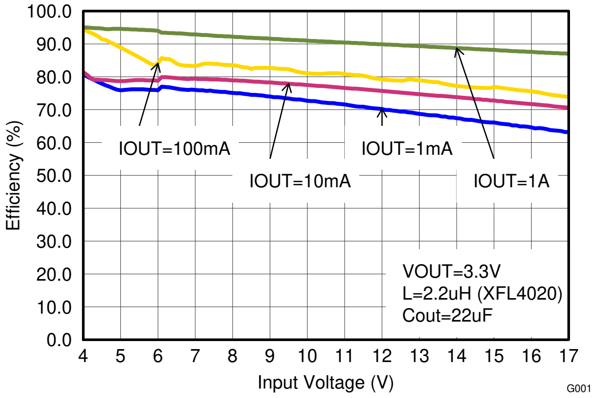
FSW = High

Figure 15. Efficiency versus Input Voltage



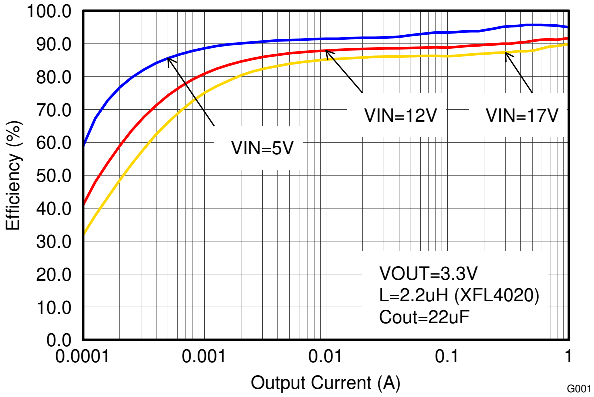
FSW = Low

Figure 16. Efficiency versus Output Current



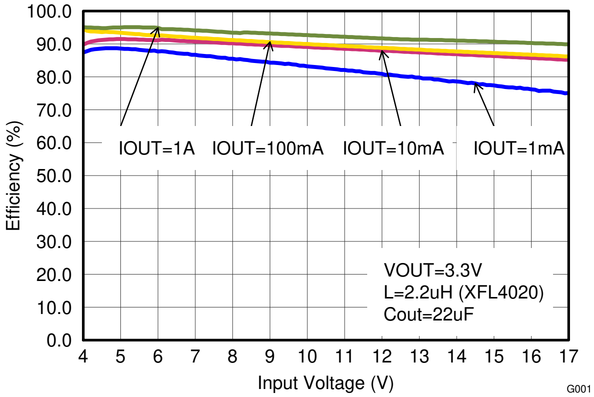
FSW = Low

Figure 17. Efficiency versus Input Voltage



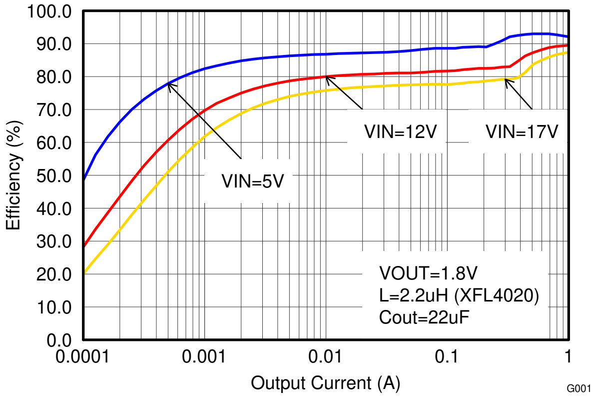
FSW = High

Figure 18. Efficiency versus Output Current



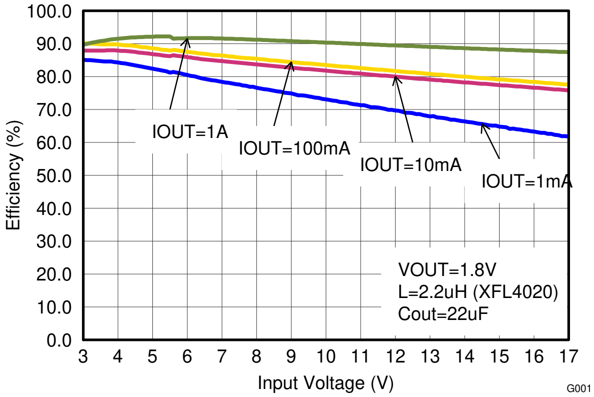
FSW = High

Figure 19. Efficiency versus Input Voltage



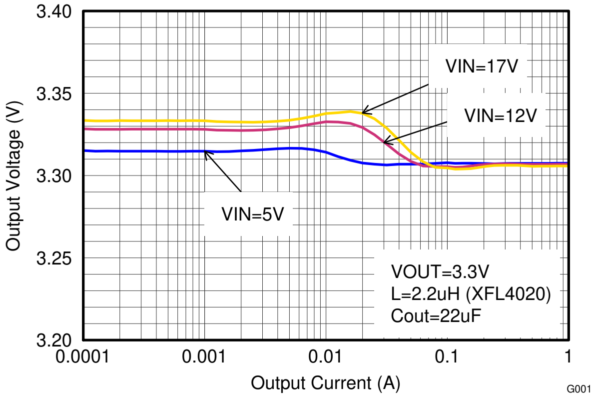
FSW = High

Figure 20. Efficiency versus Output Current



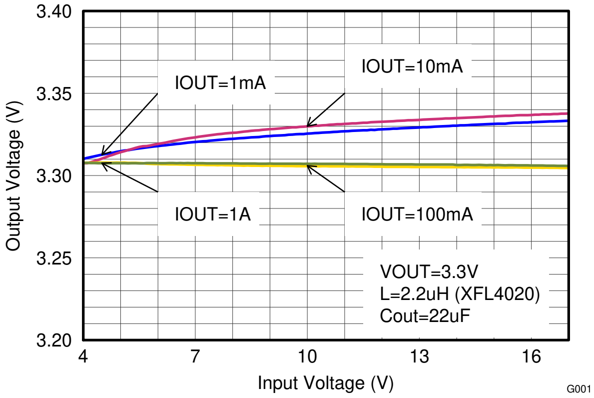
FSW = High

Figure 21. Efficiency versus Input Voltage



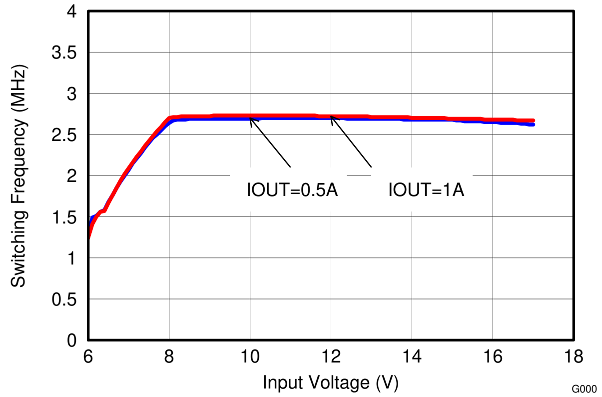
V_{OUT} = 3.3 V   L = 2.2 µH (XFL4020) C_{OUT} = 22 µF

Figure 22. Output Voltage Accuracy (Load Regulation)



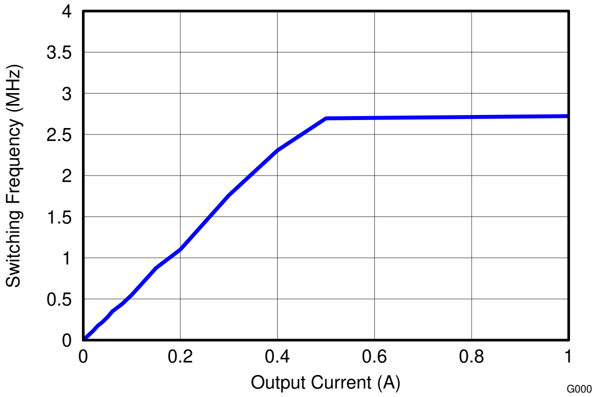
V_{OUT} = 3.3 V   L = 2.2 µH (XFL4020) C_{OUT} = 22 µF

Figure 23. Output Voltage Accuracy (Line Regulation)



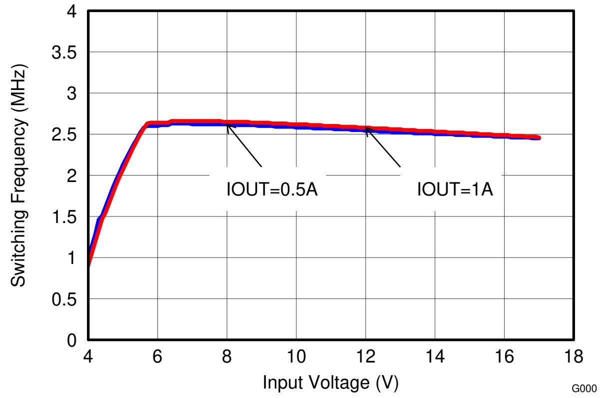
FSW = Low V_{OUT} = 5 V

Figure 24. Switching Frequency versus Input Voltage



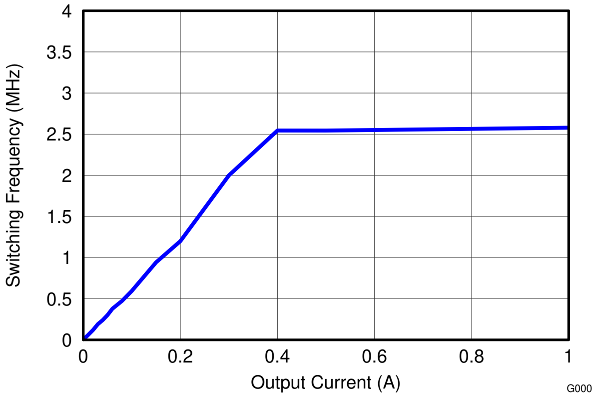
FSW = Low V_{OUT} = 5 V

Figure 25. Switching Frequency versus Output Current



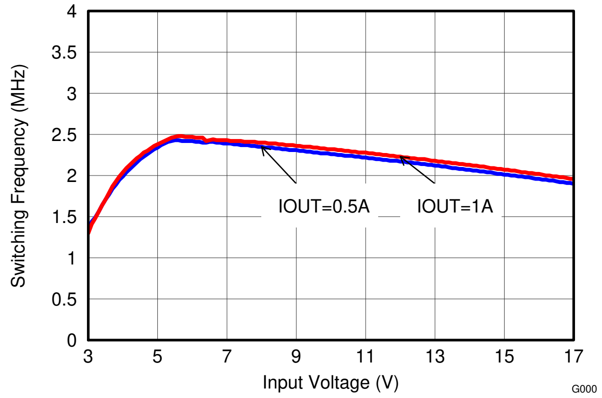
FSW = Low V_{OUT} = 3.3 V

Figure 26. Switching Frequency versus Input Voltage



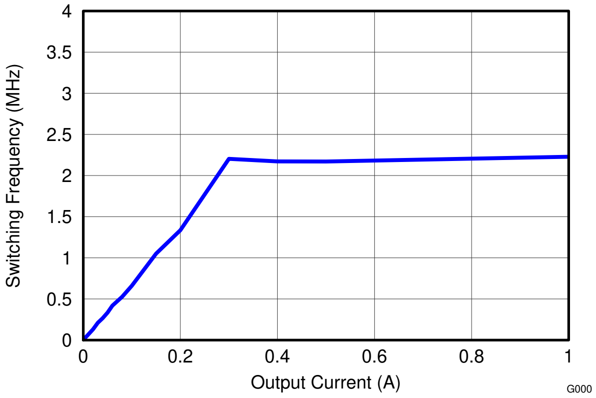
FSW = Low V_{OUT} = 3.3 V

Figure 27. Switching Frequency versus Output Current



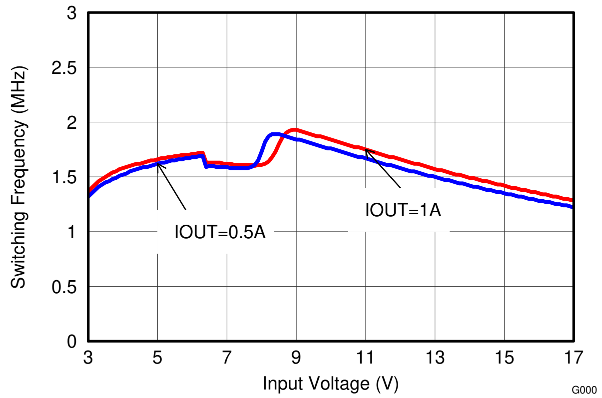
FSW = Low V_{OUT} = 1.8 V

Figure 28. Switching Frequency versus Input Voltage



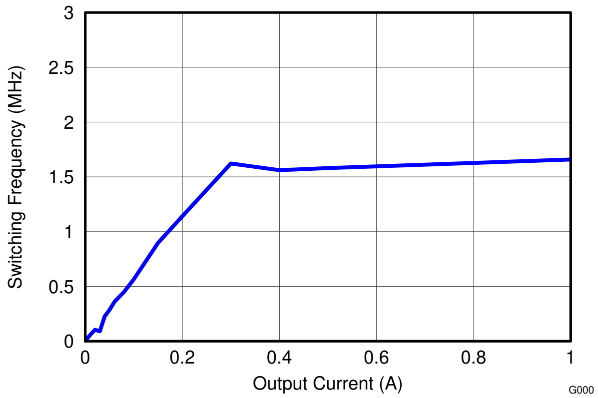
FSW = Low V_{OUT} = 1.8 V

Figure 29. Switching Frequency versus Output Current



FSW = Low V_{OUT} = 1 V

Figure 30. Switching Frequency versus Input Voltage



FSW = Low V_{OUT} = 1 V

Figure 31. Switching Frequency versus Output Current

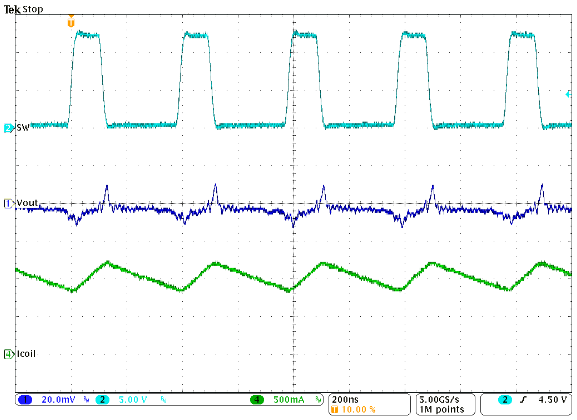


Figure 32. Typical Operation in PWM Mode (I_{OUT} = 1 A)

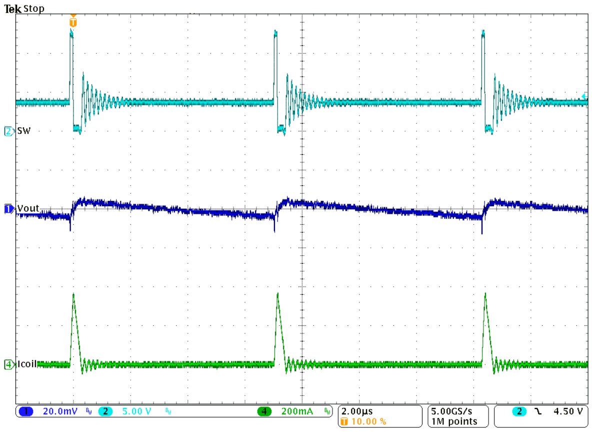


Figure 33. Typical Operation in Power Save Mode (I_{OUT} = 10 mA)

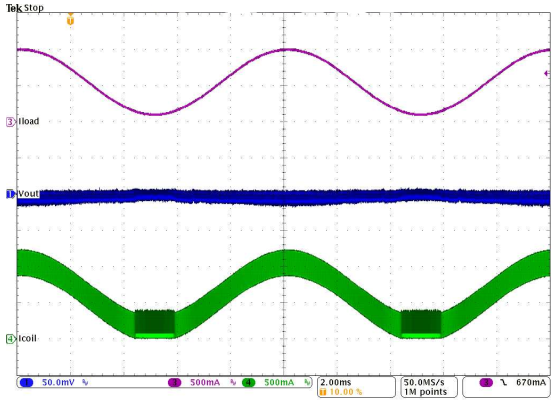


Figure 34. PWM-PSM-Transition

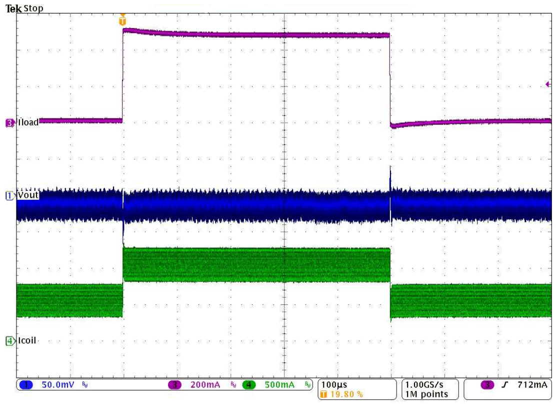


Figure 35. Load Transient Response (0.5 to 1 to 0.5 A)

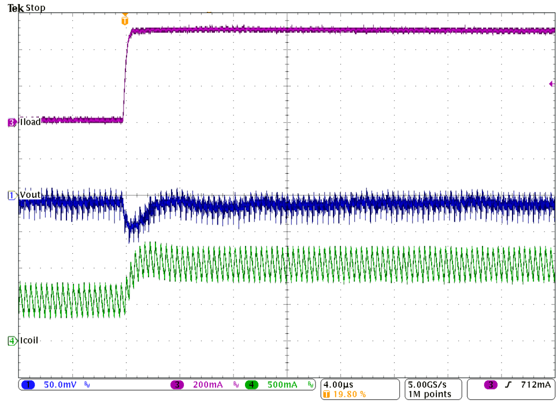


Figure 36. Load Transient Response of Figure 35, Rising Edge

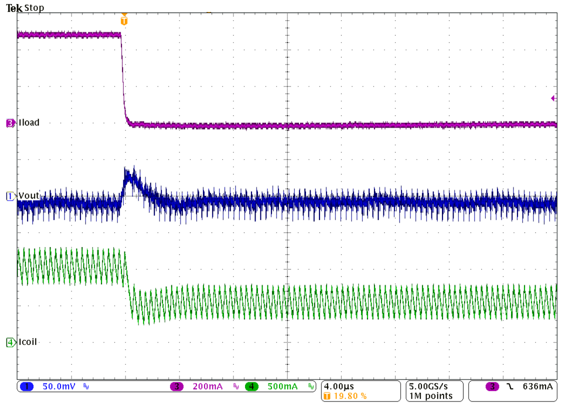


Figure 37. Load Transient Response of Figure 35, Falling Edge

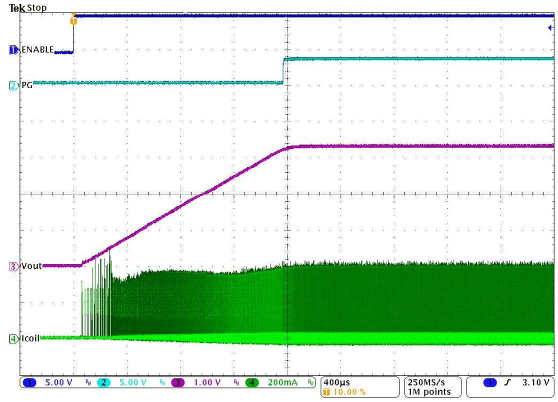


Figure 38. Start-up Into 100 mA

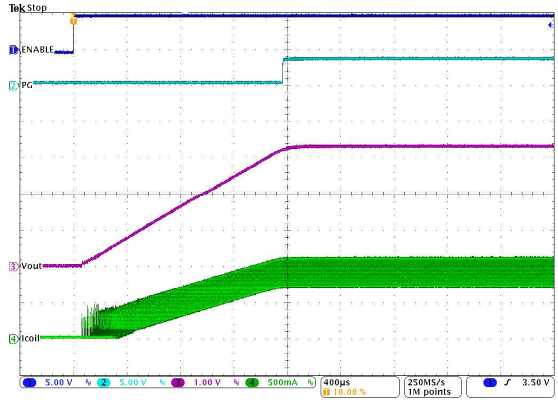


Figure 39. Start-up Into 1 A

10.2.3 System Examples

10.2.3.1 Regulated Power LED Supply

The TPS62150A-Q1 can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low, avoiding excessive power loss. Since this pin provides 2.5 µA, the feedback pin voltage can be adjusted by an external resistor per Equation 15. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62150A-Q1. Figure 40 shows an application circuit, tested with analog dimming:

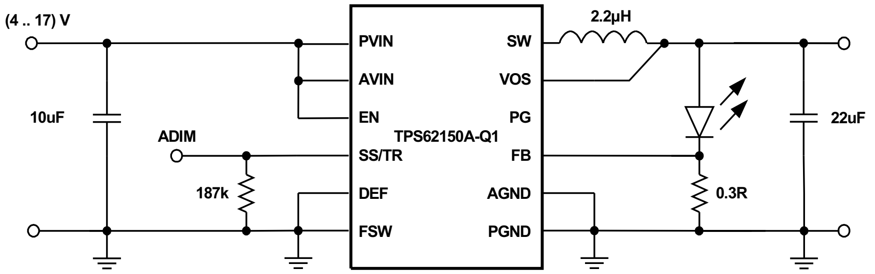


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Figure 40. Single Power LED Supply

The resistor at SS/TR sets the FB voltage to a level of about 300 mV and is calculated from Equation 15.

$$V_{FB} = 0.64 \cdot 2.5\mu A \cdot R_{SS/TR} \tag{15}$$

The device now supplies a constant current, set by the resistor at the FB pin, by regulating the output voltage accordingly. The minimum input voltage has to be rated according to the forward voltage needed by the LED used. More information is available in the *Step-Down LED Driver With Dimming With the TPS621-Family and TPS821-Family Application Report*.

10.2.3.2 Inverting Power Supply

The TPS62150A-Q1 can be used as inverting power supply by rearranging external circuitry as shown in Figure 41.

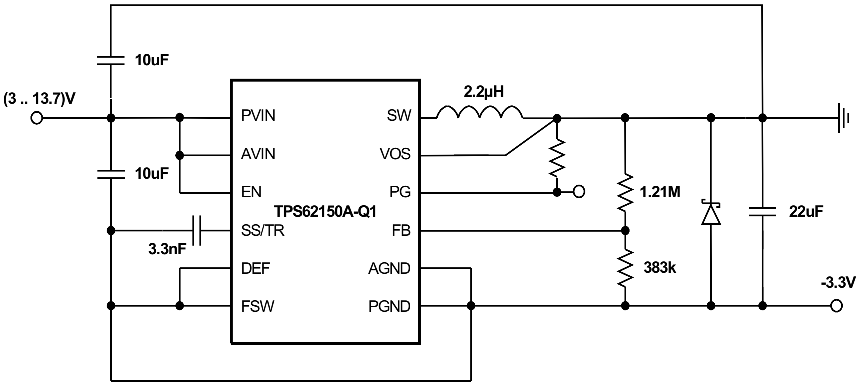

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Figure 41. –3.3-V Inverting Power Supply

As the former GND node now represents a voltage level below system ground, the voltage difference between V_{IN} and V_{OUT} has to be limited for operation to the maximum supply voltage of 17 V (see Equation 16).

$$V_{IN} + |V_{OUT}| \le V_{IN\,max} \tag{16}$$

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a Right Half Plane Zero additionally. The loop stability has to be adapted and an output capacitance of at least 22 µF is recommended. A detailed design example is given in *Using the TPS621x in an Inverting Buck-Boos Topology Application Report*.

10.2.3.3 Active Output Discharge

The TPS6215xA-Q1 pulls the PG pin Low when the device is shut down by EN, UVLO, or thermal shutdown. Connecting PG to Vout through a resistor can be used to discharge Vout in those cases (see Figure 42).

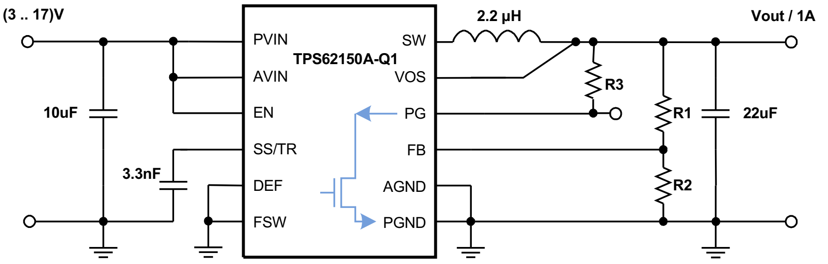

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Figure 42. Output Discharge Using PG Pin

The discharge rate can be adjusted by R3, which is also used to pull up the PG pin in normal operation. For reliability, keep the maximum current into the PG pin less than 10 mA.

10.2.3.4 Various Output Voltages

The TPS62150A-Q1 can be set for different output voltages between 0.9 V and 6 V. Some examples are shown below.

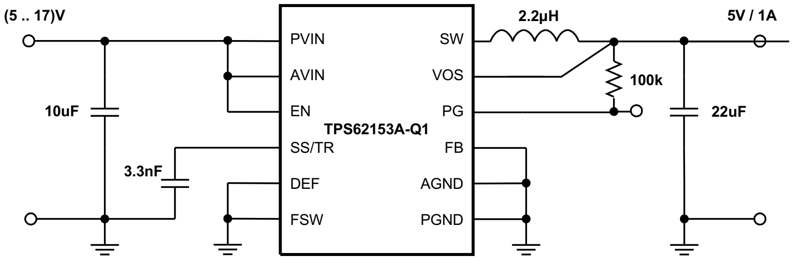

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Figure 43. 5-V Power Supply Using TPS62153A-Q1 Fixed V_{OUT} Version

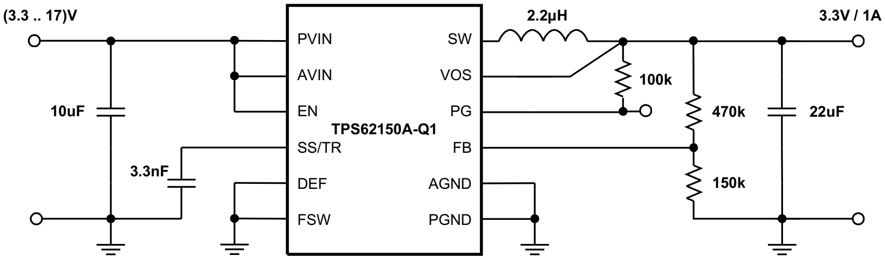

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Figure 44. 3.3-V/1-A Power Supply

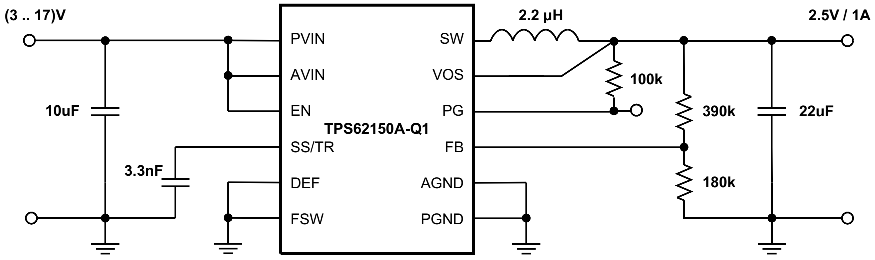

Figure 45. 2.5-V/1-A Power Supply

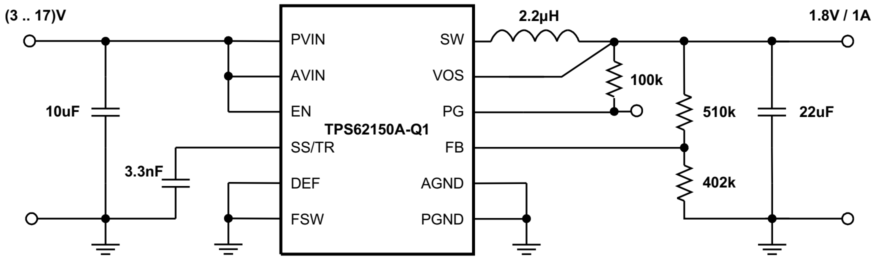

Figure 46. 1.8-V/1-A Power Supply

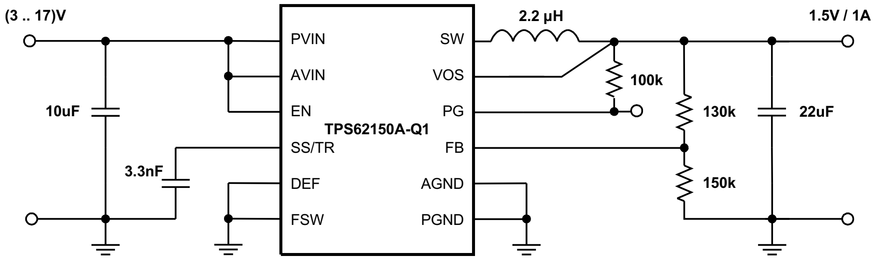

Figure 47. 1.5-V/1-A Power Supply

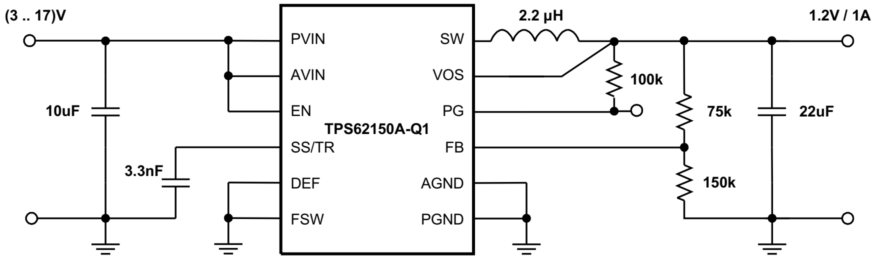

Figure 48. 1.2-V/1-A Power Supply

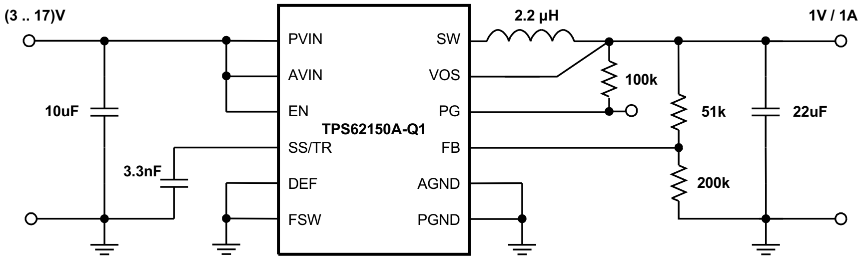

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Figure 49. 1-V/1-A Power Supply

11 Power Supply Recommendations

The TPS6215xA-Q1 devices are designed to operate from a 3-V to 17-V input voltage supply. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminal or supply peak current limitations, additional bulk capacitance can be required. In case there is ringing that is caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum type capacitor may be needed for damping.

12 Layout

12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS6215xA-Q1 demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity. The layout also influences the thermal performance of the solution by its power dissipation capabilities.

See Figure 50 for the recommended layout of the TPS62150A-Q1, which is designed for common external ground connections. Therefore, both AGND and PGND pins are directly connected to the Exposed Thermal Pad. On the PCB, the direct common ground connection of AGND and PGND to the Exposed Thermal Pad and the system ground (ground plane) is mandatory. Also connect the VOS pin in the shortest way to the VOUT potential at the output capacitor.

Provide low inductive and resistive paths for loops with high di/dt. Therefore, paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt, so the input and output capacitance is placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces are avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example, SW). Since they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin and on AVIN as well as the FB resistors, R1 and R2, must be kept close to the IC and connect directly to those pins and the AGND pin.

The Exposed Thermal Pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation.

The recommended layout is implemented on the EVM and shown in the *TPS62130EVM-505, TPS62140EVM-505, and TPS62150EVM-505 Evaluation Modules User's Guide*. Additionally, the EVM Gerber data are available for download here.

12.2 Layout Example

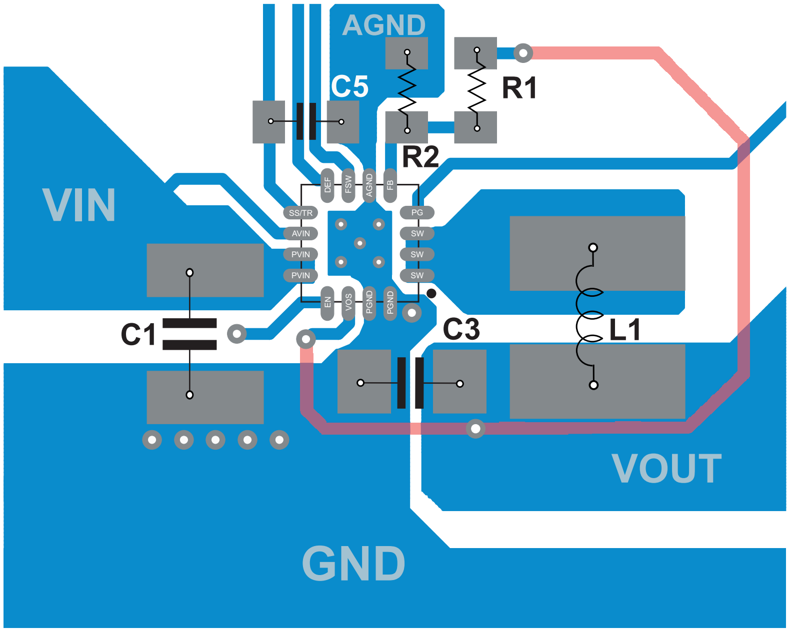

Figure 50. Layout Example with TPS62150A-Q1

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 5. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62150A-Q1	Click here	Click here	Click here	Click here	Click here
TPS62152A-Q1	Click here	Click here	Click here	Click here	Click here
TPS62153A-Q1	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.5 Trademarks

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13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

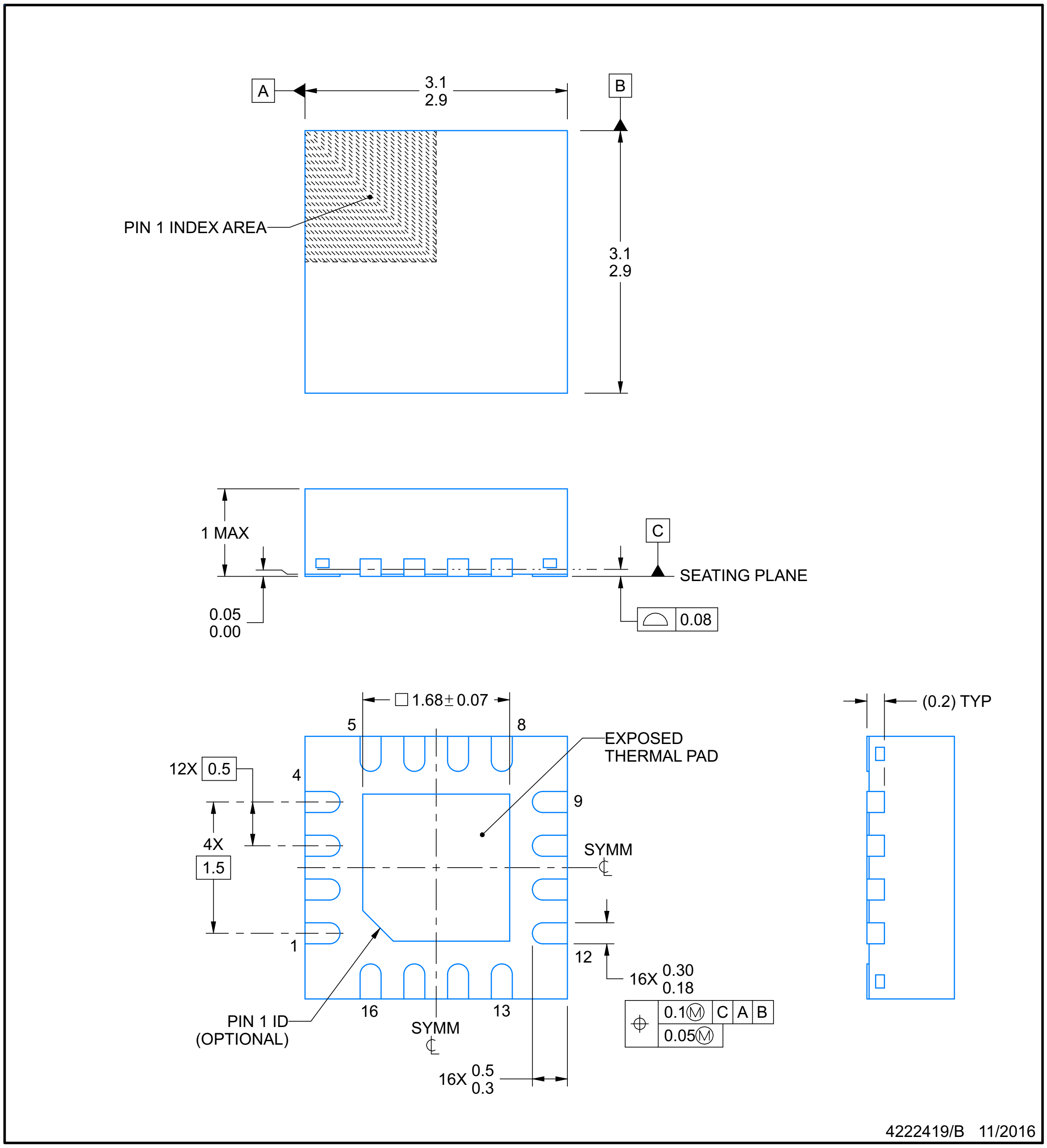
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



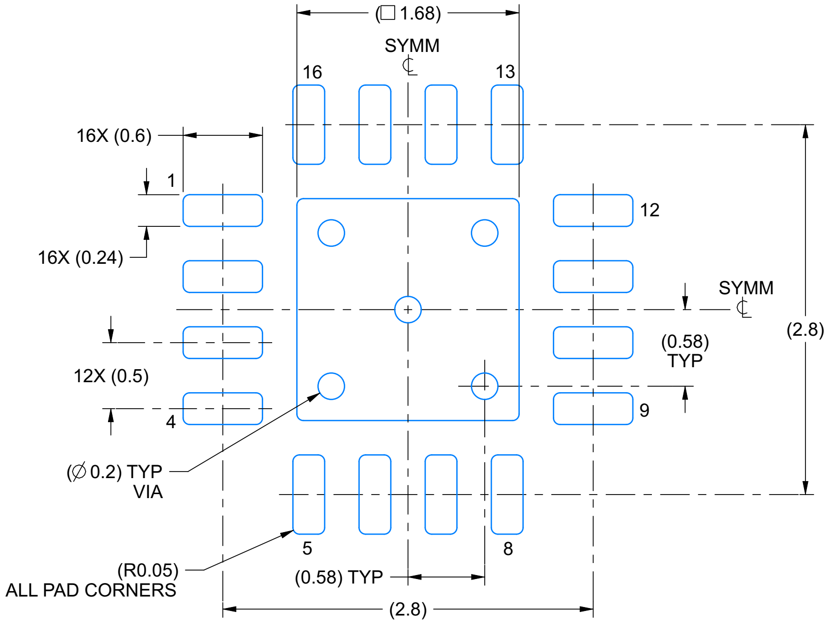
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

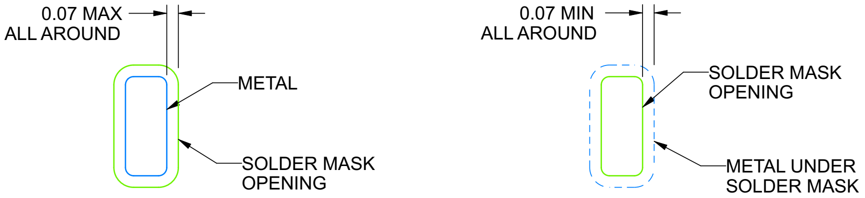
EXAMPLE BOARD LAYOUT

RGT0016C **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222419/B 11/2016

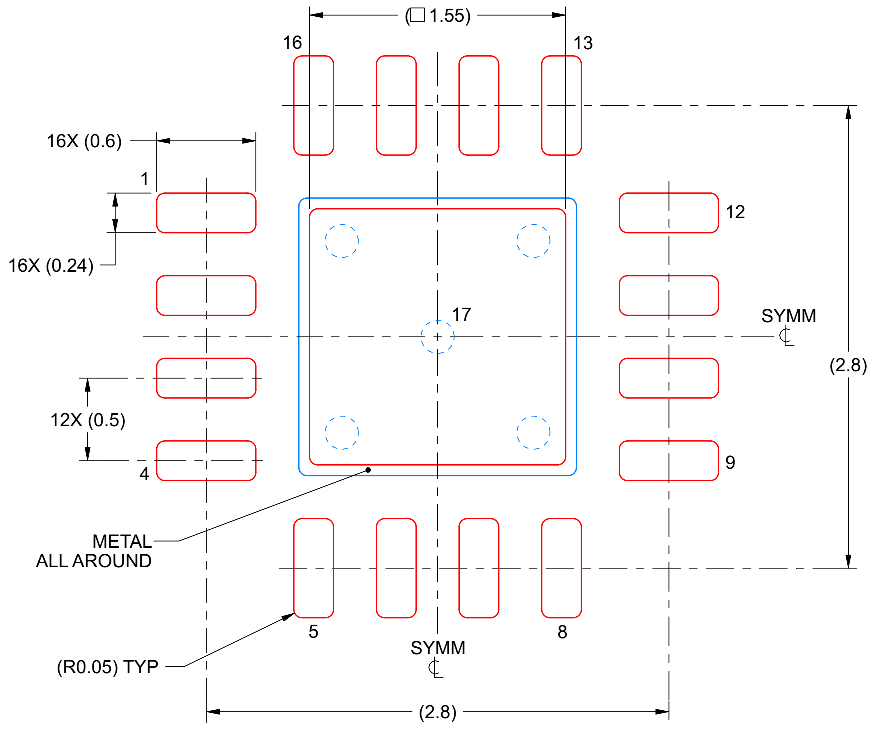
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/B 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS62150AQRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8IQ
TPS62150AQRGTRQ1.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8IQ
TPS62150AQRGTRQ1.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8IQ
TPS62150AQRGTTQ1	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8IQ
TPS62150AQRGTTQ1.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8IQ
TPS62150AQRGTTQ1.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8IQ
TPS62152AQRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	152Q1
TPS62152AQRGTRQ1.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	152Q1
TPS62152AQRGTRQ1.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	152Q1
TPS62153AQRGTRQ1	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8JQ
TPS62153AQRGTRQ1.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8JQ
TPS62153AQRGTRQ1.B	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8JQ
TPS62153AQRGTTQ1	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8JQ
TPS62153AQRGTTQ1.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8JQ
TPS62153AQRGTTQ1.B	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PA8JQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS62150A-Q1 :

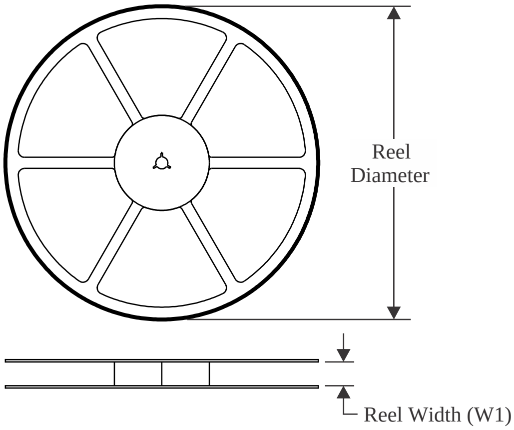
- Catalog : TPS62150A

NOTE: Qualified Version Definitions:

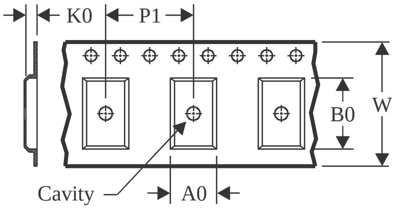
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

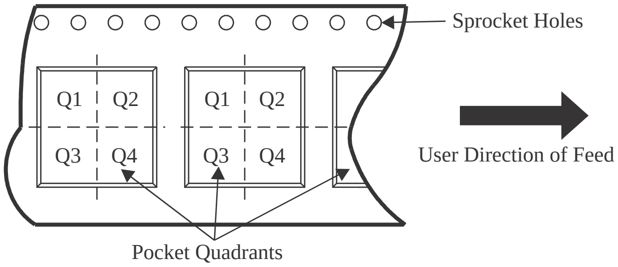


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

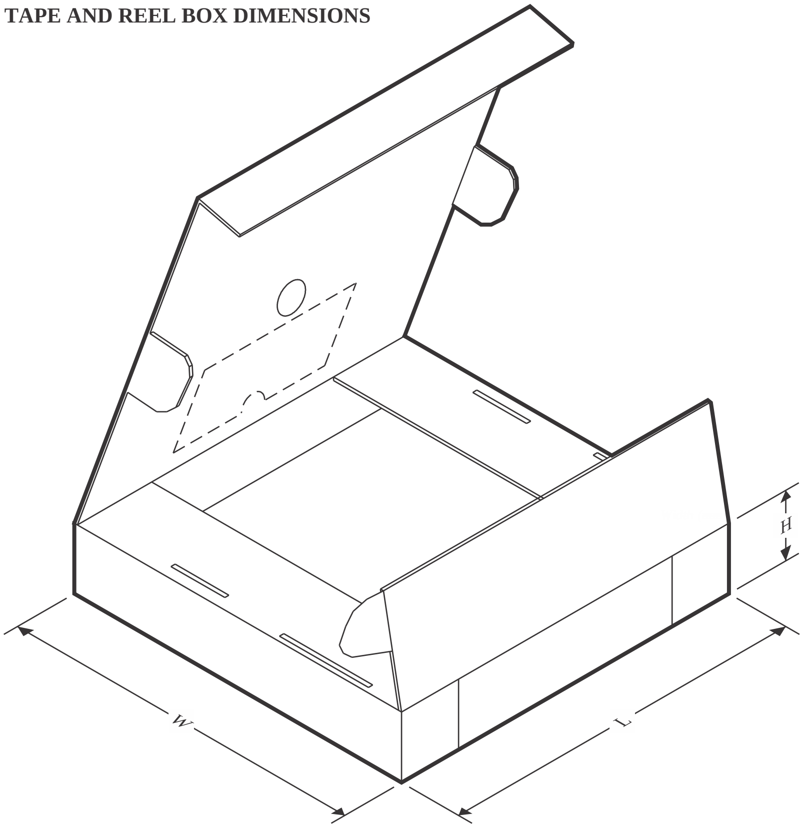
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62150AQRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62150AQRGTTQ1	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62152AQRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62153AQRGTRQ1	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62153AQRGTTQ1	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

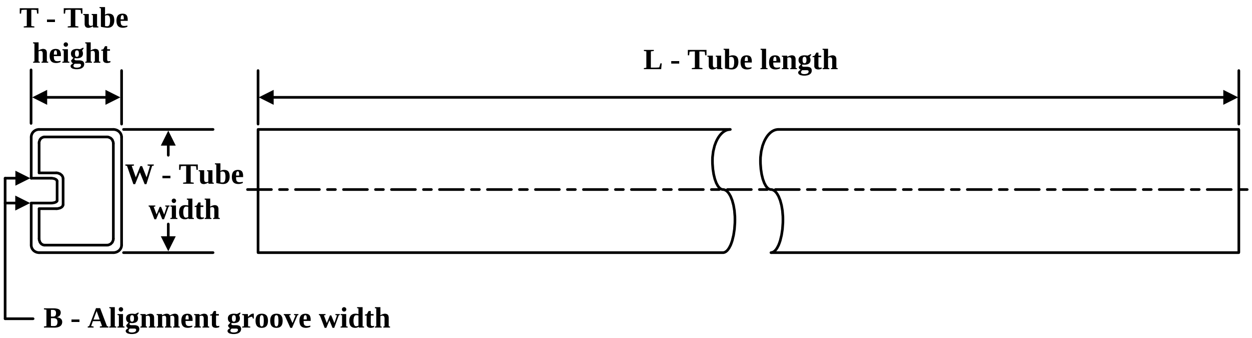
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62150AQRGTRQ1	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62150AQRGTTQ1	VQFN	RGT	16	250	552.0	185.0	36.0
TPS62152AQRGTRQ1	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62153AQRGTRQ1	VQFN	RGT	16	3000	552.0	346.0	36.0
TPS62153AQRGTTQ1	VQFN	RGT	16	250	552.0	185.0	36.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS62150AQRGTRQ1	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62150AQRGTRQ1.A	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62150AQRGTRQ1.B	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62150AQRGTTQ1	RGT	VQFN	16	250	381	4.83	2286	0
TPS62150AQRGTTQ1.A	RGT	VQFN	16	250	381	4.83	2286	0
TPS62150AQRGTTQ1.B	RGT	VQFN	16	250	381	4.83	2286	0
TPS62153AQRGTRQ1	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62153AQRGTRQ1.A	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62153AQRGTRQ1.B	RGT	VQFN	16	3000	381	4.83	2286	0
TPS62153AQRGTTQ1	RGT	VQFN	16	250	381	4.83	2286	0
TPS62153AQRGTTQ1.A	RGT	VQFN	16	250	381	4.83	2286	0
TPS62153AQRGTTQ1.B	RGT	VQFN	16	250	381	4.83	2286	0

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