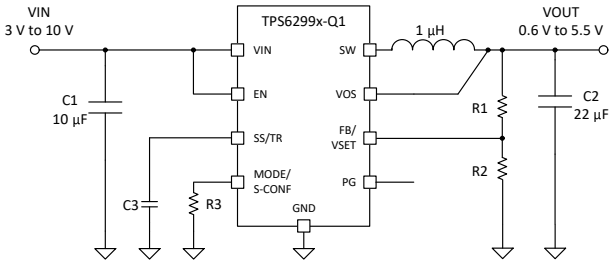
# TPS62992-Q1 3-V to 10-V, 2-A, Automotive Low $I_Q$ Buck Converter with +165°C $T_J$

## 1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, $T_A$
  - Level 2 device HBM ESD classification
  - Level C4B CDM ESD classification
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Extended $T_J$ range: up to 165°C
- High efficiency DCS-Control topology
  - $R_{DS(ON)}$: 62-mΩ high side, 22-mΩ low side
  - Seamless PWM/PFM transition
  - Internal compensation
- 4-µA low $I_Q$ (typical)
- Up to 2-A continuous output current
- ±1.5% output voltage accuracy across temp
- Configurable output voltage options:
  - 0.6-V to 5.5-V $V_{FB}$ external divider
  - $V_{SET}$ internal divider
    - 16 options between 0.4 V and 5.5 V
- Flexibility through the MODE/S-CONF pin
  - 2.5-MHz or 1.0-MHz switching frequency
  - Forced PWM or Auto PFM (power save mode) with dynamic mode change option
  - Output discharge on and off
- No external bootstrap capacitor required
- Overcurrent and overtemperature protection
- 100% duty cycle mode
- Precise enable input
- Adjustable soft start and tracking
- Power-good output
- Optimized pinout for single-layer routing
- Wettable 2.2-mm × 2.0-mm VQFN package with 0.5-mm pitch
- Create a custom design with the TPS62992-Q1 using the WEBENCH® Power Designer




**Simplified Schematic**

## 2 Applications

- ADAS
- Body electronics and lighting
- Infotainment and cluster
- Hybrid, electric, and powertrain systems

## 3 Description

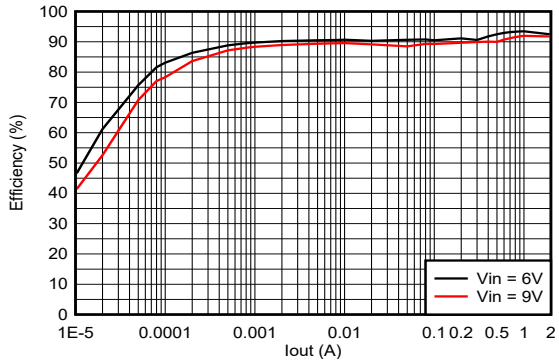
The TPS62992-Q1 is a highly efficient, small, and flexible synchronous step-down DC-DC converter that is easy to use. A selectable switching frequency of 2.5 MHz or 1.0 MHz allows the use of small inductors and provides fast transient response. The device supports high $V_{OUT}$ accuracy of ± 1.5% across the entire operasting temperature range and enhanced load transient performance with the DCS-Control topology. The wide 3-V to 10-V input voltage range supports a variety of nominal inputs, like 9-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

The TPS62992-Q1 can automatically enter power save mode (if auto PFM or PWM is selected) at light loads to maintain high efficiency. Additionally, to provide high efficiency at very small loads, the device has a low typical quiescent current of 4 µA. AEE, if enabled, provides high efficiency across $V_{IN}$, $V_{OUT}$, and load current. The device includes a MODE/Smart-CONF input to set the internal and external divider, switching frequency, output voltage discharge, and automatic power save mode or forced PWM operation.

**Package Information**

| Part Number | Package(1) | Body Size (NOM) |
|---|---|---|
| TPS62992-Q1 | RYT (VQFN, 9) | 2.20 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Efficiency Versus Output Current (3.3 $V_O$ at 2.5 MHz, 1 µH, Auto PFM or PWM)**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Revision History**....2
**5 Device Comparison Table**....3
**6 Pin Configuration and Functions**....4
**7 Specifications**....5
7.1 Absolute Maximum Ratings....5
7.2 ESD Ratings....5
7.3 Recommended Operating Conditions....5
7.4 Thermal Information....5
7.5 Electrical Characteristics....6
7.6 Typical Characteristics....8
**8 Detailed Description**....12
8.1 Overview....12
8.2 Functional Block Diagram....12
8.3 Feature Description....13
8.4 Device Functional Modes....21
**9 Application and Implementation**....23
9.1 Application Information....23
9.2 Typical Application with Adjustable Output Voltage....23
9.3 Typical Application with Selectable $V_{OUT}$ using VSET....34
9.4 System Examples....42
9.5 Power Supply Recommendations....46
9.6 Layout....46
**10 Device and Documentation Support**....48
10.1 Device Support....48
10.2 Documentation Support....48
10.3 Receiving Notification of Documentation Updates....48
10.4 Support Resources....48
10.5 Trademarks....48
10.6 Electrostatic Discharge Caution....49
10.7 Glossary....49
**11 Mechanical, Packaging, and Orderable Information**....49

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (October 2022) to Revision A (March 2023) | Page |
|---|---|
| • Corrected Figure 9-9 | 28 |
| • Corrected Figure 9-58 | 37 |


Copyright © 2023 Texas Instruments Incorporated

## 5 Device Comparison Table

| Device Number | Output Current | Input Voltage | Operating Temperature Range | Switching Frequency | PWM Mode | $V_O$ Adjust |
|---|---|---|---|---|---|---|
| TPS62993-Q1 | 0 A – 3 A | 3 V – 10 V | –40°C to 165°C | Selectable 1-MHz or 2.5-MHz options | Selectable auto PFM/PWM or forced PWM | Externally programmable or 16 internal options |
| TPS62992-Q1 | 0 A – 2 A | | | | | |
| TPS62903-Q1 | 0 A – 3 A | 3 V – 18 V | –40°C to 165°C | Selectable 1-MHz or 2.5-MHz options | Selectable auto PFM/PWM or forced PWM | Externally programmable or 16 internal options |
| TPS62902-Q1 | 0 A – 2 A | | | | | |
| TPS62901-Q1 | 0 A – 1 A | | | | | |
| TPS62903 | 0 A – 0.3 A | 3 V – 18 V | –40°C to 125°C | Selectable 1-MHz or 2.5-MHz options | Selectable auto PFM/PWM or forced PWM | Externally programmable or 16 internal options |
| TPS62902 | 0 A – 2 A | | | | | |
| TPS62901 | 0 A – 1 A | | | | | |
| TPS62903E | 0 A – 3 A | | –55°C to 165°C | | | |

Copyright © 2023 Texas Instruments Incorporated

# 6 Pin Configuration and Functions

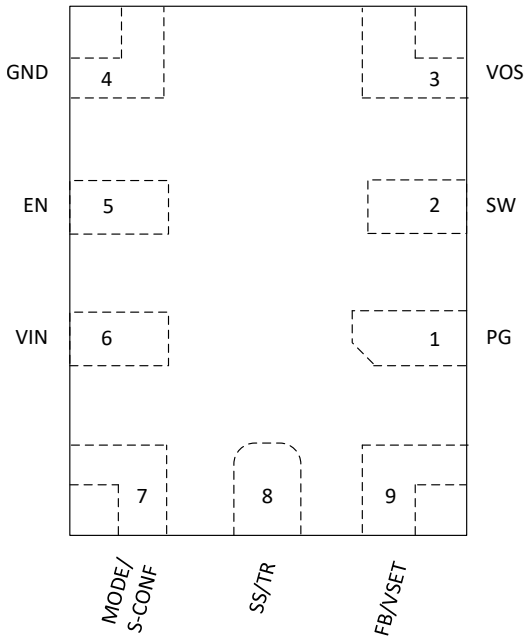



**Figure 6-1. 9-Pin RYT VQFN Package (Top View, Device Pins Face Down)**

**Table 6-1. Pin Functions**

| Pin | | Type[1] | Description |
|---|---|---|---|
| Name | Number | | |
| PG | 1 | O | Open-drain power-good output. High = $V_{OUT}$ is ready. Low = $V_{OUT}$ is below nominal regulation. This pin requires a pullup resistor. |
| SW | 2 | — | Switch pin of the converter and is connected to the internal power switches. Connect the inductor between SW and the output capacitor. |
| VOS | 3 | I | Output voltage sense pin. Connect directly to the positive pin of the output capacitor. |
| GND | 4 | — | Ground pin. This pin must be connected directly to the common ground plane. |
| EN | 5 | I | Enable input pin. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected. |
| VIN | 6 | I | Power supply input pin. Ensure the input capacitor is connected as close as possible between the VIN and GND pins. |
| MODE/ S-CONF | 7 | I | Device mode selection (auto PFM/PWM or forced PWM operation) and SmartConfig pin. Connect high, low, or to a resistor to configure the device according to Table 8-1. Do not leave this pin unconnected. |
| SS/TR | 8 | I | Soft start and tracking pin. An external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing. The pin can be left floating for the fastest ramp-up time. |
| FB/VSET | 9 | I | Depends on device configuration (see Section 8.3.1.)<br>• FB: Voltage feedback input. Connect a resistive output voltage divider to this pin.<br>• VSET: Output voltage setting pin. Connect a resistor to GND to choose the output voltage according to Table 8-2. |

(1) O = output, I = input


Copyright © 2023 Texas Instruments Incorporated

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage((2)) | VIN, EN, PG, MODE/S-CONF | –0.3 | 12 | V |
| Voltage(2) | SW ((3)) | –0.3 | $V_{IN}$ + 0.3 | V |
| Voltage((2)) | SW (AC, less than 10ns)((3)) | –3.0 | 17 | V |
| Voltage(2) | FB/VSET, SS/TR, VOS | –0.3 | 6 | V |
| $T_J$ | Junction temperature | –55 | 165 | °C |
| $T_{stg}$ | Storage temperature | –65 | 165 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC-Q100-002 HBM ESD Classification Level 2, all pins((1)) | | ±2000 | V |
| $V_{(ESD)}$ | Electrostatic discharge | Charged device model (CDM), per AEC-Q100-011 CDM ESD Classification level C4B. | All pins | ±500 | V |
| | | | Corner pins (3, 4, 7, and 9) | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_I$ | Input voltage range | 3.0 | | 10 | V |
| $V_O$ | Output voltage range | 0.4 | | 5.5 | V |
| $C_I$ | Effective input capacitance | 3 | 10 | | µF |
| $C_O$ | Effective output capacitance (2.5MHz selection)(1) | 10 | 22 | 100 (1) | µF |
| $C_O$ | Effective output capacitance (1MHz selection)(1) | 10 | 22 | 100 (1) | µF |
| L | Output inductance(2) | 1 | 2.2 | 4.7(3) | µH |
| $I_{OUT}$ | Output current | 0 | | 2 | A |
| $I_{SINK_PG}$ | Sink current at PG-Pin | | | 1 | mA |
| $T_J$ | Junction temperature (4) | -40 | | 165 | °C |

(1) This is for capacitors directly at the output of the device. More capacitance is allowed if there is a series resistance associated to the capacitor.
(2) Nominal inductance value.
(3) Larger values of inductance may be used to reduce the ripple current, but they may have a negative impact on efficiency and the overvall transient responce.
(4) Operating lifetime is derated at junction temperatures greater than 165°C.

## 7.4 Thermal Information

| THERMAL METRIC((1)) | | VQFN (RYT) | | UNIT |
|---|---|---|---|---|
| | | JEDEC PCB | TPS6299xEVM-xxx | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 97.2 | 73.5 | °C/W |

Copyright © 2023 Texas Instruments Incorporated

## 7.4 Thermal Information (continued)

| THERMAL METRIC[(1)] | | VQFN (RYT) | | UNIT |
|---|---|---|---|---|
| | | JEDEC PCB | TPS6299xEVM-xxx | |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 74.4 | N/A | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 25 | N/A | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 2.7 | 4.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 24.7 | 28 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 7.5 Electrical Characteristics

$V_I$ = 3 V to 10 V, $T_J$ = -40C °C to +165°C, Typical values at $V_I$ = 6V and $T_A$ = 25 °C unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| $I_Q$ | Operating Quiescent Current (Power Save Mode) | Iout = 0 mA device not switching | | 4 | | µA |
| $I_{Q;PWM}$ | Operating Quiescent Current (PWM Mode) | VIN= 6V, VOUT=1.2V; Iout = 0 mA, device switching | | 8 | | mA |
| $I_{SD}$ | Shutdown current into VIN pin | EN = 0 V, | | 0.27 | 3.5 | µA |
| $V_{UVLO}$ | Under Voltage Lock-Out | $V_{IN}$ rising, | 2.85 | 2.925 | 3.0 | V |
| | Under Voltage Lock-Out | $V_{IN}$ falling | 2.71 | 2.79 | 2.87 | V |
| $V_{UVLO}$ | Under Voltage Lock-Out Hysteresis | | | 130 | | mV |
| **CONTROL & INTERFACE** | | | | | | |
| $I_{LKG}$ | EN Input leakage current | EN = 5V | | 10 | 310 | nA |
| $V_{IH;MODE}$ | High-Level Input Voltage at MODE/S-CONF Pin | | 1.0 | | | V |
| $V_{IL;MODE}$ | Low-Level Input Voltage at MODE/S-CONF Pin | | | | 0.15 | V |
| $T_{SD}$ | Thermal Shutdown Threshold | $T_J$ rising | 168 | 175 | 185 | °C |
| | Thermal Shutdown Hysteresis | $T_J$ falling | | 12.5 | | |
| $V_{IH}$ | High-level input voltage at EN-Pin | | 0.97 | 1.0 | 1.03 | V |
| $V_{IL}$ | Low-level input voltage at EN-Pin | | 0.820 | 0.850 | 0.880 | V |
| $V_{PG}$ | Power good fthreshold | $V_{FB}$ rising, referenced to $V_{FB}$ nominal | 93% | 96% | 99% | |
| | | $V_{FB}$ falling, referenced to $V_{FB}$ nominal | 88% | 92% | 96% | |
| $V_{PG_HYS}$ | Power good threshold hysteresis | | 1.5% | 3.5% | 6% | |
| $V_{PG,OL}$ | Low-level output voltage at PG pin | $I_{SINK}$ = 1 mA | | | 0.4 | V |
| $I_{PG,LKG}$ | Input leakage current into PG pin | $V_{PG}$ = 5 V, | | 25 | 550 | nA |
| $t_{PG,DLY}$ | Power good delay time | $V_{FB}$ rising and falling | | 32 | | µs |
| $C_{SET}$ | Maximum Capacitance connected to VSET pin | | | | 30 | pF |
| **POWER SWITCHES** | | | | | | |
| $I_{LKG;SW}$ | Leakage current into SW-Pin | EN = 0V, $V_{SW}$ = $V_{OS}$ = 5.5V, $T_J$ up to 150°C | | 2 | 7 | µA |
| $R_{DS;ON}$ | High-side FET on resistance | $V_{IN}$ > 4 V, $I_{SW}$ = 500 mA | | 62 | 111 | mΩ |
| | Low-side FET on resistance | $V_{IN}$ > 4 V, $I_{SW}$ = 500 mA | | 22 | 41 | |
| $I_{LIM}$ | High-side FET current limit | | 2.7 | 3.1 | 3.7 | A |
| $I_{LIM}$ | Low-side FET current limit | | 2.5 | 3 | 3.5 | A |
| $I_{LIM;SINK}$ | Low-side FET sink current limit | | 1.3 | 1.7 | 2.5 | A |


Copyright © 2023 Texas Instruments Incorporated

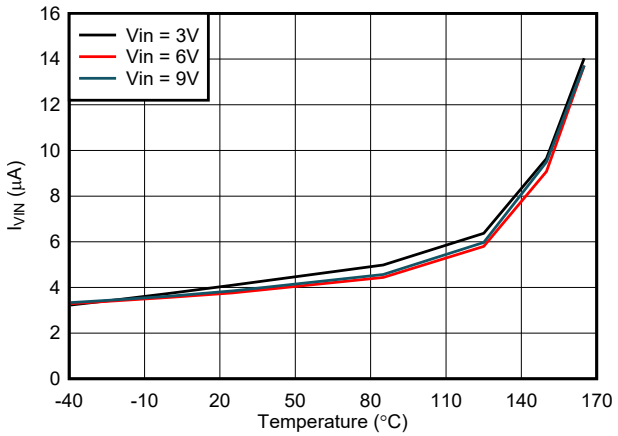
## 7.5 Electrical Characteristics (continued)

$V_I$ = 3 V to 10 V, $T_J$ = -40C °C to +165°C, Typical values at $V_I$ = 6V and $T_A$ = 25 °C unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{SW}$ | Switching frequency | 2.5-MHz selection | | 2.5 | | MHz |
| $T_{ON(MIN)}$ | Minimum On-time | | | 30 | | ns |
| $f_{SW}$ | Switching frequency | 1.0-MHz selection | | 1.0 | | MHz |
| **OUTPUT** | | | | | | |
| $V_O$ | Output Voltage Regulation | VSET Configuration selected, $T_J$ = 25°C | –1% | | +1% | |
| $V_O$ | Output Voltage Regulation | VSET Configuration selected | –1.5% | | +1.5% | |
| $V_{FB}$ | Feedback Regulation Voltage | Adjustable Configuration selected | | 0.6 | | V |
| $V_{FB}$ | Feedback Voltage Regulation | FB-Option selected. $T_J$ = 25 °C. | –0.6% | | +0.6% | |
| $V_{FB}$ | Feedback Voltage Regulation | FB-Option selected | –1.25% | | +1.25% | |
| $I_{FB}$ | Input leakage current into FB pin | Adjustable configuration, VFB = 0.6 V | | 1 | 70 | nA |
| $T_{delay}$ | Start-up delay time | $I_O$ = 0 mA, time from EN=HIGH until start switching, Adjustable Configuration selected | | 600 | 1400 | µs |
| | Start-up delay time | $I_O$ = 0 mA, time from EN=HIGH until start switching, VSET Configuration selected. The typical value is based on the first option of VSET configuration. | | 650 | 1850 | µs |
| $T_{SS}$ | Soft-Start time | $I_O$ = 0 mA after $T_{delay}$, from 1st switching pulse until target $V_O$ , Css=Open | | 150 | | µs |
| $I_{SS}$ | SS/TR source current | | 2.25 | 2.5 | 2.75 | µA |
| $V_{FB}/V_{SS/TR}$ | Tracking Gain, Adjustable Configuration | | | 0.75 | | |
| $V_{FB}/V_{SS/TR}$ | Tracking Gain tolerance | | | ±8 | | mV |
| $R_{DISCH}$ | Active Discharge Resistance | Discharge = ON - Option Selected, EN = LOW | | 7.5 | 30 | Ω |

Copyright © 2023 Texas Instruments Incorporated

## 7.6 Typical Characteristics




Measured with the device not switching

**Figure 7-1. Quiescent Current vs Temperature**

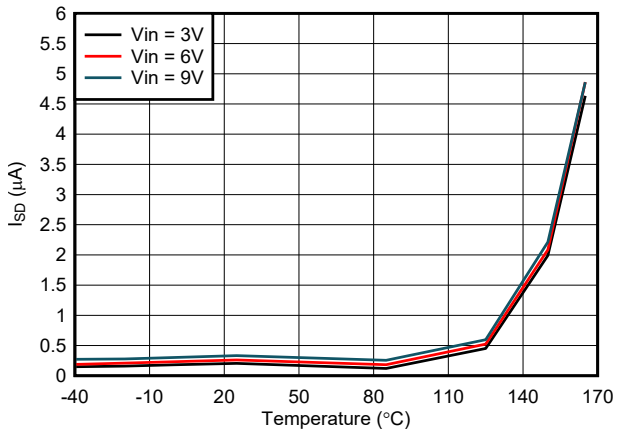



**Figure 7-2. Shutdown Current vs Temperature**

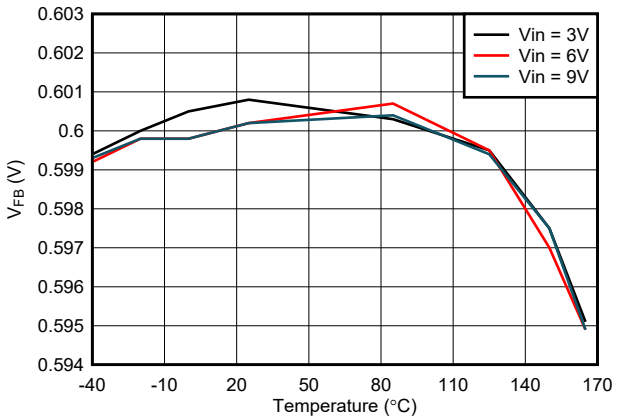



**Figure 7-3. Feedback Voltage Accuracy - External Feedback Selected**

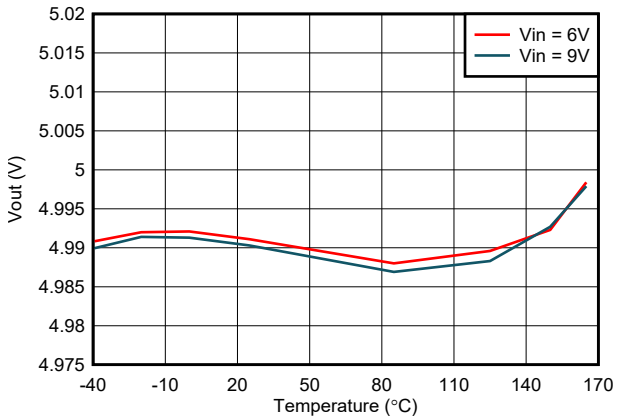
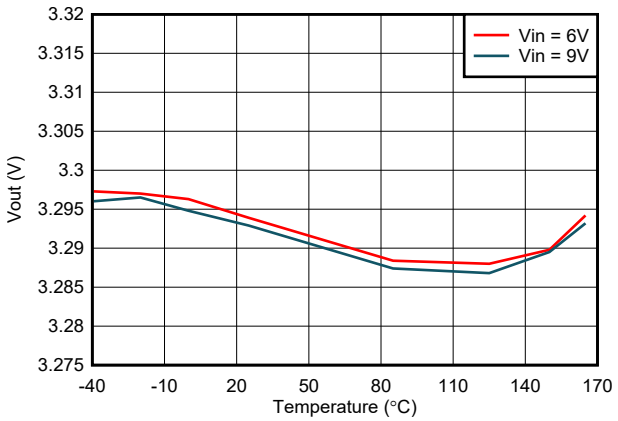
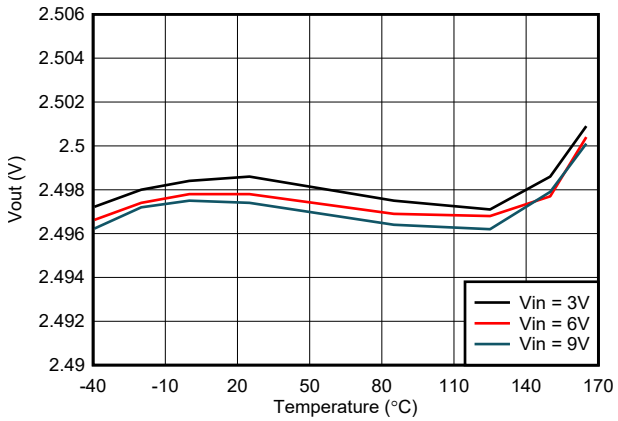



**Figure 7-4. Output Voltage Accuracy - VSET Selected**




$V_{OUT}$ = 3.3 V

**Figure 7-5. Output Voltage Accuracy - VSET Selected**

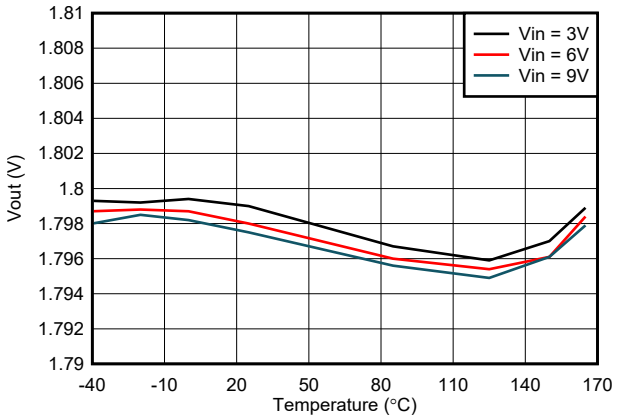



$V_{OUT}$ = 2.5 V

**Figure 7-6. Output Voltage Accuracy - VSET Selected**

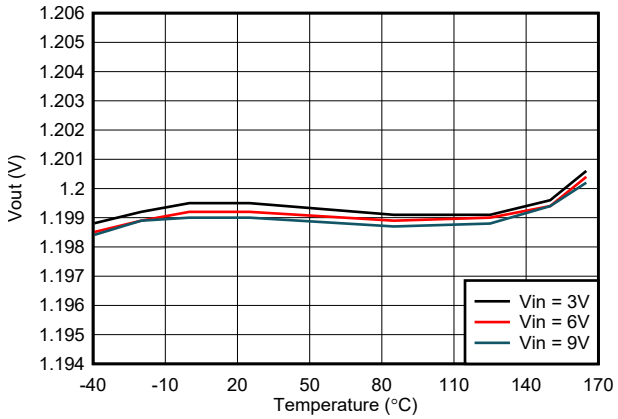

Copyright © 2023 Texas Instruments Incorporated

## 7.6 Typical Characteristics (continued)



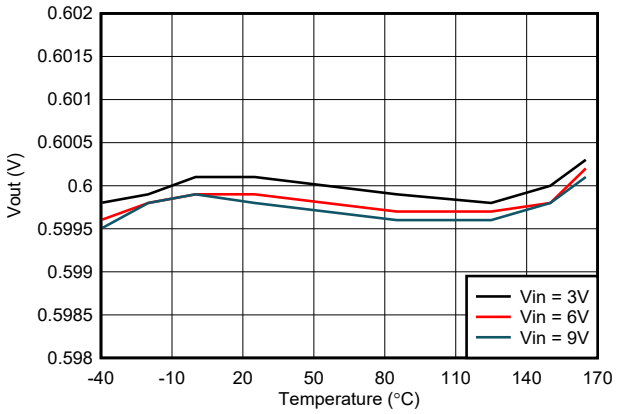

$V_{OUT}$ = 1.8 V

**Figure 7-7. Output Voltage Accuracy - VSET Selected**




$V_{OUT}$ = 1.2 V

**Figure 7-8. Output Voltage Accuracy - VSET Selected**




$V_{OUT}$ = 0.6 V

**Figure 7-9. Output Voltage Accuracy - VSET Selected**

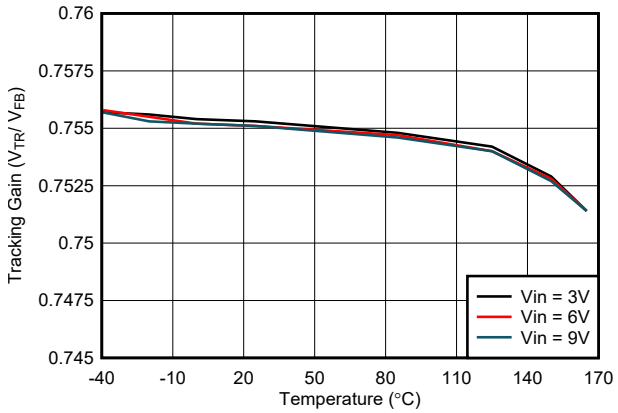
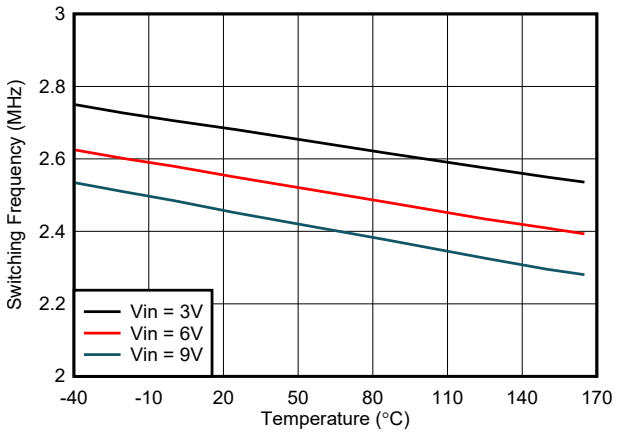
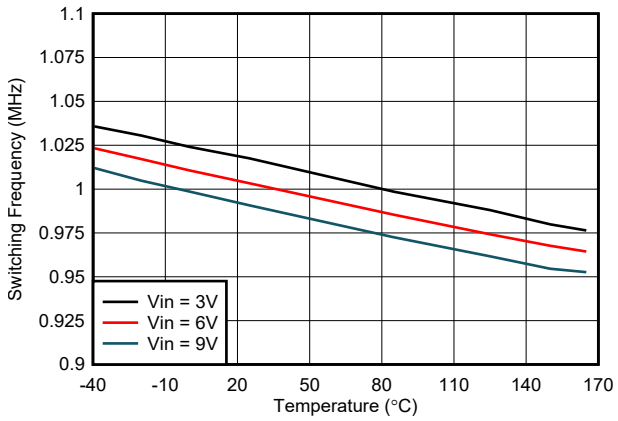



**Figure 7-10. Tracking Voltage Gain vs Temperature**




$V_{OUT}$ = 1.2 V $F_{SW}$ = 2.5 MHz FPWM $I_{OUT}$ = 0 A

**Figure 7-11. Switching Frequency vs Temperature**




$V_{OUT}$ = 1.2 V $F_{SW}$ = 1.0 MHz FPWM $I_{OUT}$ = 0 A

**Figure 7-12. Switching Frequency vs Temperature**

Copyright © 2023 Texas Instruments Incorporated

## 7.6 Typical Characteristics (continued)

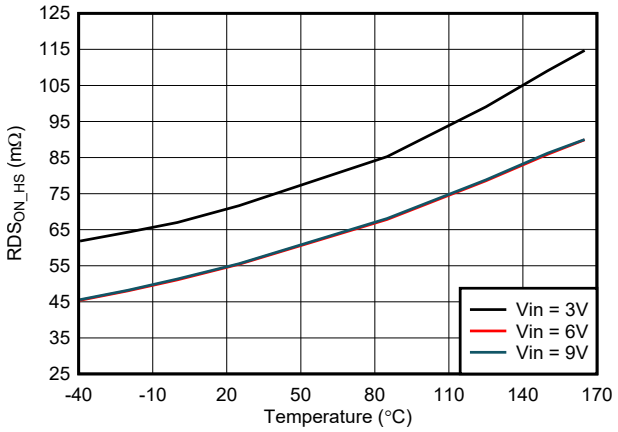



**Figure 7-13. High Side $RDS_{ON}$ vs Temperature**

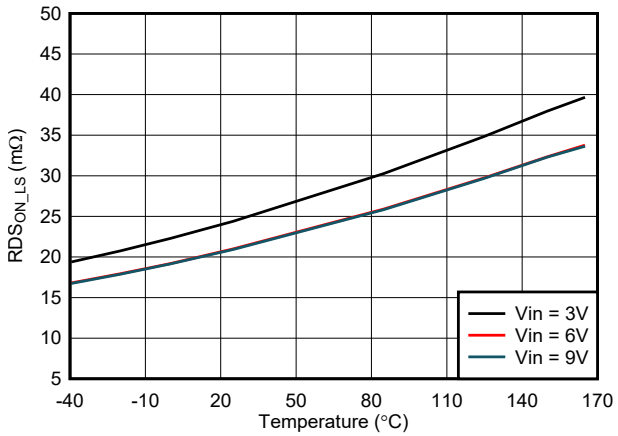



**Figure 7-14. Low Side $RDS_{ON}$ vs Temperature**

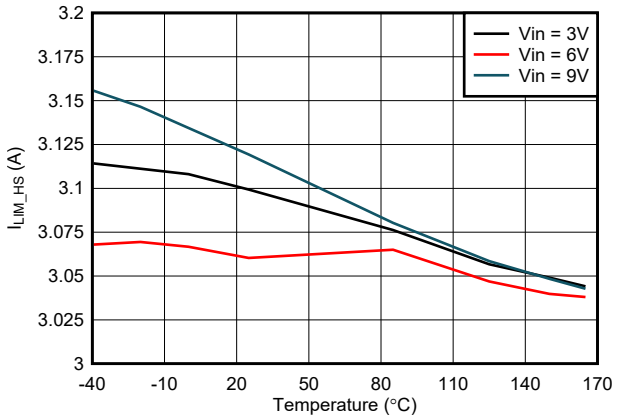



**Figure 7-15. High Side $I_{LIM}$ vs Temperature**

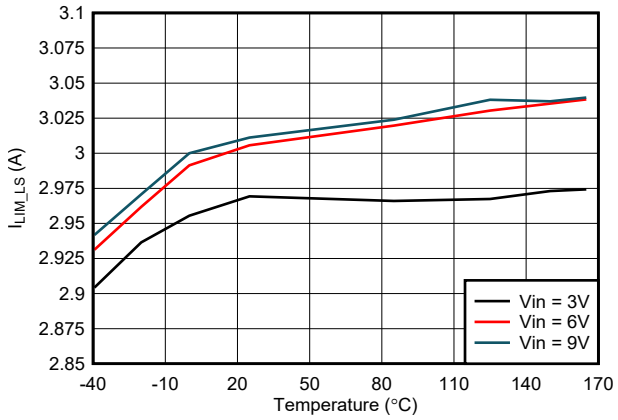



**Figure 7-16. Low Side $I_{LIM}$ vs Temperature**

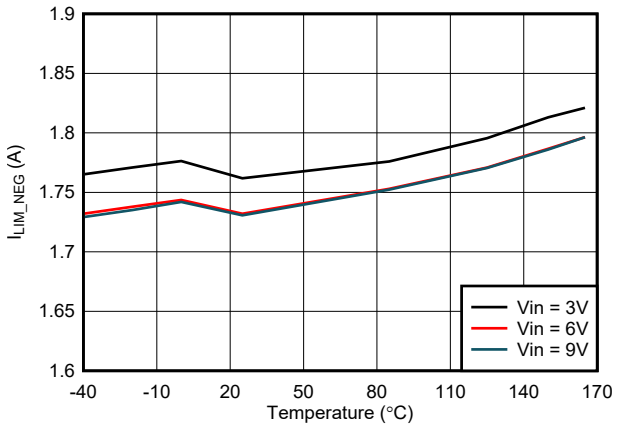



**Figure 7-17. Negative $I_{LIM}$ vs Temperature**

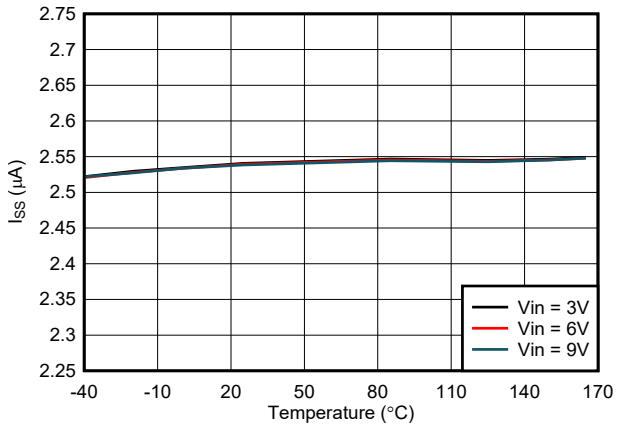



**Figure 7-18. Soft Start Current vs Temperature**


Copyright © 2023 Texas Instruments Incorporated

## 7.6 Typical Characteristics (continued)

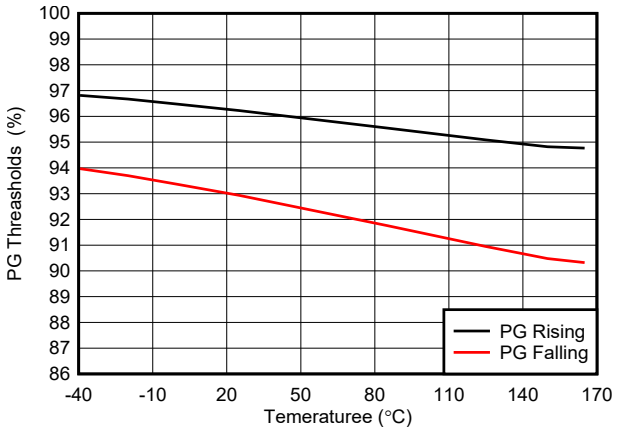



**Figure 7-19. Power Good Thresholds vs Temperature**

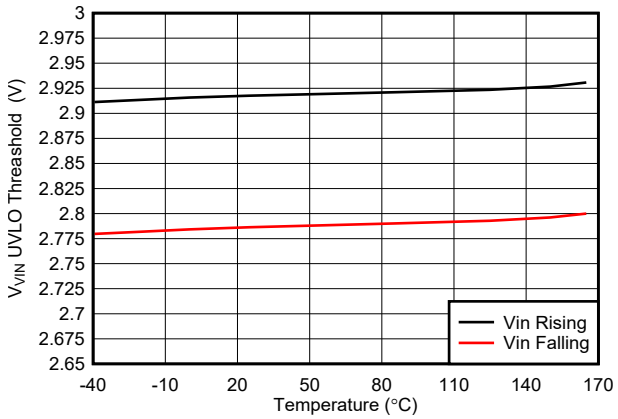



**Figure 7-20. $V_{VIN}$ UVLO Thresholds vs Temperature**

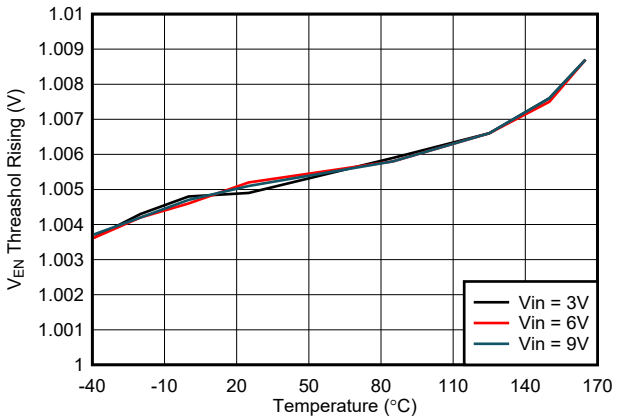



**Figure 7-21. Percise EN Threshold vs Temperature**

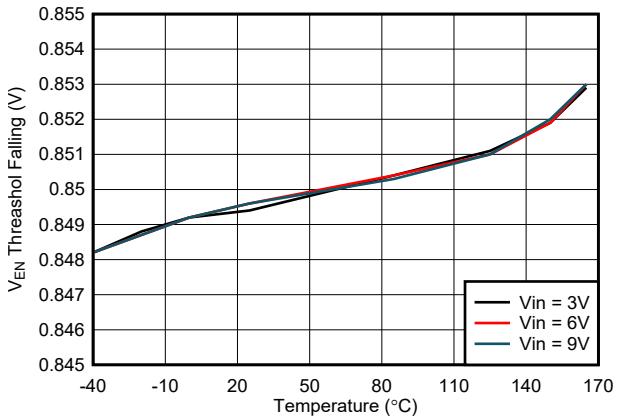


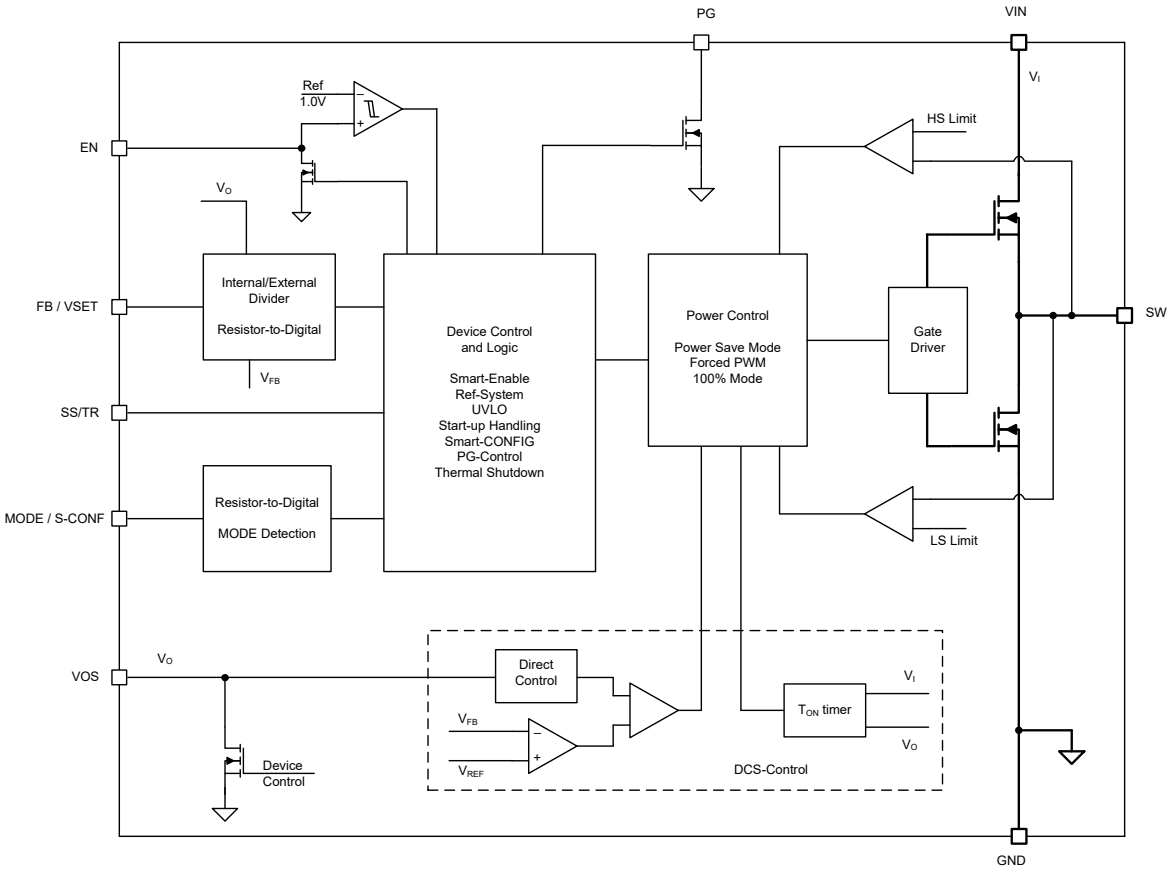

**Figure 7-22. Percise EN Threshold vs Temperature**

# 8 Detailed Description

## 8.1 Overview

The TPS62992-Q1 synchronous switched mode power converters are based on DCS-Control (Direct Control with Seamless Transition into power save mode). DCS-Control is an advanced regulation topology that combines the advantages of hysteretic, voltage mode, and current mode control. This control loop takes information about output voltage changes and feeds the information directly to a fast comparator stage. DCS-Control sets the switching frequency, which is constant for steady-state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

## 8.2 Functional Block Diagram





Copyright © 2023 Texas Instruments Incorporated

## 8.3 Feature Description

### 8.3.1 Mode Selection and Device Configuration MODE/S-CONF

With MODE/S-CONF (SmartConfig), this device features an input with two functions. This pin can be used to customize the device behavior in two ways:

- Select the device mode (Forced PWM or Auto PFM /PWM with AEE operation) with a HIGH-level or LOW-level.
- Select the device configuration (switching frequency, internal or external feedback, output discharge, and auto PFM/PWM mode) by connecting a single resistor to the MODE/S-CONF pin.

The TPS62992-Q1 interprets this pin during the start-up sequence after the internal OTP readout and before the device starts switching in soft start (see Figure 8-1). If the device reads a HIGH-level or LOW-level, the dynamic mode change is active and auto PFM/PWM or FPWM mode can be changed during operation. If the TPS62992-Q1 reads a resistor value, the device is configured according to the resistance value in Table 8-1 and there is no further interpretation during operation and device mode or other configurations can only be changed by power cycling or disabling the device.

**Note**

The MODE/S-CONF pin must not be left floating. Connect the pin high, low, or to a resistor to configure the device according to Table 8-1.

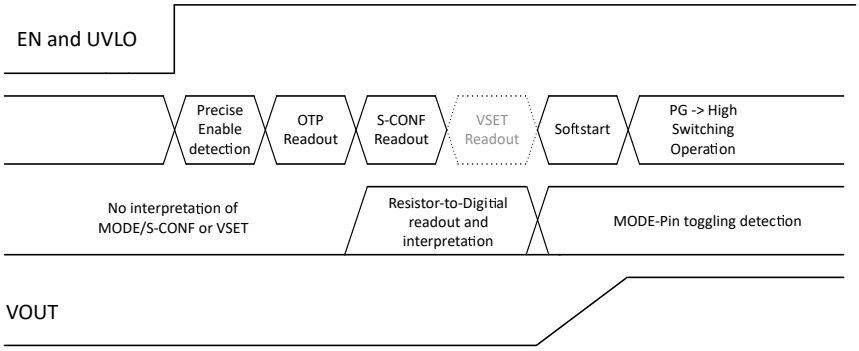



**Figure 8-1. Interpretation of S-CONF and VSET Flow**

Copyright © 2023 Texas Instruments Incorporated

**Table 8-1. SmartConfig Setting Table**

| # | Level Or Resistor Value [Ω] (1) | FB/VSET Pin | $F_{SW}$ (MHz) | Output Discharge | Mode (Auto Or Forced PWM) | Dynamic Mode Change |
|---|---|---|---|---|---|---|
| | **Setting Options by Level** | | | | | |
| 1 | GND | External FB | 2.5(2) | yes | Auto PFM/PWM with AEE | Active |
| 2 | HIGH (> $V_{IH_MODE}$) | External FB | 2.5 | yes | Forced PWM | |
| | **Setting Options by Resistor** | | | | | |
| 3 | 7.15 k | External FB | 2.5(2) | no | Auto PFM/PWM with AEE | Not active |
| 4 | 8.87 k | External FB | 2.5 | no | Forced PWM | |
| 5 | 11.0 k | External FB | 1 | yes | Auto PFM/PWM | |
| 6 | 13.7 k | External FB | 1 | yes | Forced PWM | |
| 7 | 16.9 k | External FB | 1 | no | Auto PFM/PWM | |
| 8 | 21.0 k | External FB | 1 | no | Forced PWM | |
| 9 | 26.1 k | VSET | 2.5(2) | yes | Auto PFM/PWM with AEE | |
| 10 | 32.4 k | VSET | 2.5 | yes | Forced PWM | |
| 11 | 40.2 k | VSET | 2.5(2) | no | Auto PFM/PWM with AEE | |
| 12 | 49.9 k | VSET | 2.5 | no | Forced PWM | |
| 13 | 61.9 k | VSET | 1 | yes | Auto PFM/PWM | |
| 14 | 76.8 k | VSET | 1 | yes | Forced PWM | |
| 15 | 95.3 k | VSET | 1 | no | Auto PFM/PWM | |
| 16 | 118 k | VSET | 1 | no | Forced PWM | |

(1) E96 resistor series, 1% accuracy, temperature coefficient better or equal than ±200 ppm/°C
(2) $F_{SW}$ varies based on $V_{IN}$ and $V_{OUT}$. See Section 8.4.3 for more details.

### 8.3.2 Adjustable $V_O$ Operation (External Voltage Divider)

The TPS62992-Q1 can be programmed by the MODE/S-CONF pin to operating in a classical configuration where the FB/VSET pin is used as the feedback pin, sensing $V_O$ through an external resistive divider. The TPS62992-Q1 can also be programmed to 1 of 16 different fixed output voltages (see Section 8.3.3).

If the device is configured to operate in the classical adjustable $V_O$ operation, the FB/VSET pin is used as the feedback pin and must sense $V_O$ through an external divider network. Figure 8-2 shows the typical schematic for this configuration.

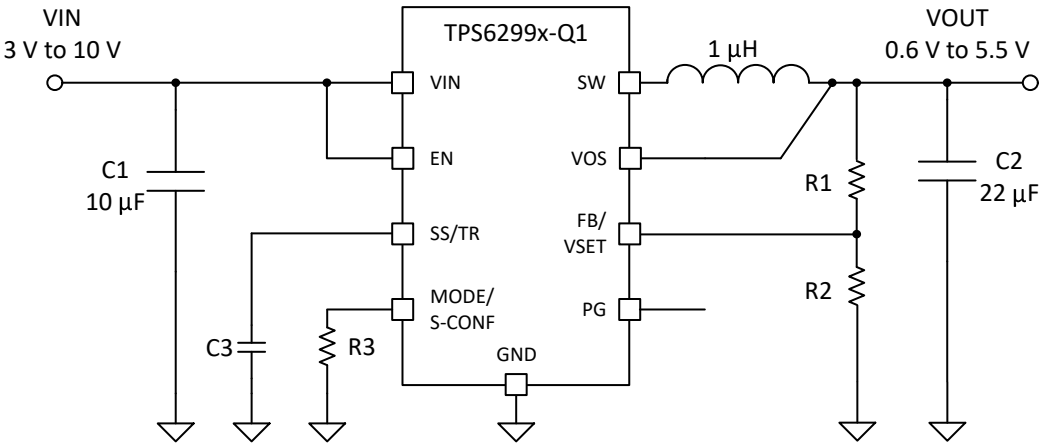



**Figure 8-2. Adjustable $V_O$ Operation Schematic**


Copyright © 2023 Texas Instruments Incorporated

### 8.3.3 Selectable $V_O$ Operation (VSET and Internal Voltage Divider)

If the device is configured to VSET operation, $V_O$ is sensed only through the VOS pin by an internal resistor divider. The target $V_O$ is programmed by an external resistor ($R_{VSET}$) connected between the VSET pin and GND. Figure 8-3 shows the typical schematic for this configuration.

**CAUTION**

The MODE/S-CONF pin must not be configured for external feedback operation (see Table 8-1) if only $R_{VSET}$ (R2 as shown in Figure 8-3) is populated. This causes the output voltage to become unregulated and can damage to the device or surrounding circuitry.

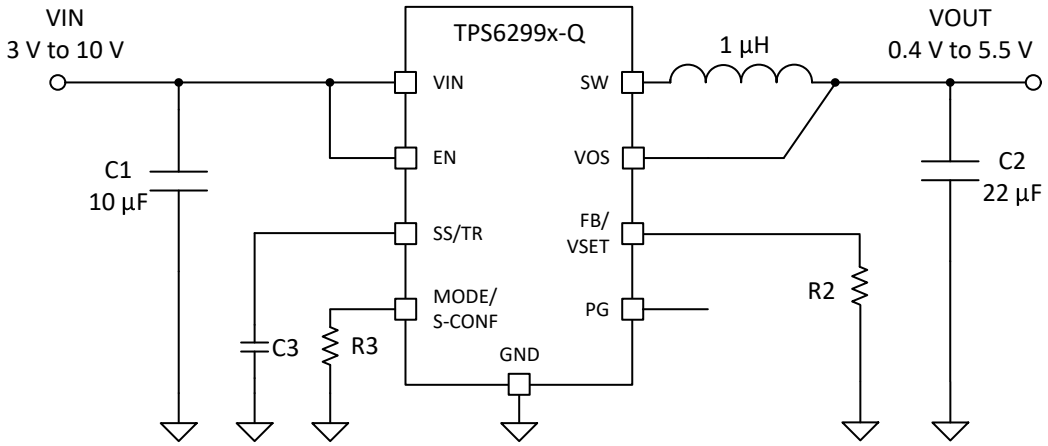



**Figure 8-3. Selectable $V_O$ Operation Schematic**

**Table 8-2. VSET Selection Table**

| # | Level Or Resistor Value [Ω] (1) | Target $V_O$ [V] |
|---|---|---|
| 1 | GND | 1.2 |
| 2 | 4.64 k | 0.4 |
| 3 | 5.76 k | 0.6 |
| 4 | 7.15 k | 0.8 |
| 5 | 8.87 k | 1.0 |
| 6 | 11.0 k | 1.1 |
| 7 | 13.7 k | 1.3 |
| 8 | 16.9 k | 1.35 |
| 9 | 21.0 k | 1.8 |
| 10 | 26.1 k | 1.9 |
| 11 | 40.2 k | 2.5 |
| 12 | 61.9 k | 3.8 |
| 13 | 76.8 k | 5.0 |
| 14 | 95.3 k | 1.25 |
| 15 | 118.0 k | 5.5 |
| 16 | 249.00 k or larger/Open | 3.3 |

(1) E96 resistor series, 1% accuracy, temperature coefficient better or equal than ±200 ppm/°C

### 8.3.4 Soft Start and Tracking (SS/TR)

With the SS/TR pin, the user can adjust the soft-start behavior or track an external voltage source (see Section 8.3.4.1 for operation details).

Copyright © 2023 Texas Instruments Incorporated

The internal soft-start circuitry controls the output voltage slope during start-up. This avoids excessive inrush current and makes sure there is a controlled output voltage rise time. The soft-start circuitry also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after the start-up delay, while the internal reference, and hence $V_O$, rises with a slope controlled by the 2.5µA (typical) $I_{SS}$ current source and an external capacitor connected to the SS/TR pin and the 2.5µA (typical) $I_{SS}$ current source.

**Note**

Shorting or pulling the SS/TR pin LOW externally prevents the device from switching as this sets the internal reference voltage to 0 V.

**Note**

Leaving the SS/TR pin unconnected provides the fastest start-up response, but this can result in some output voltage overshoot depending on the Vout value, load current, and external component sizes. Adding or increasing the soft-start capacitor ($C_{SS}$) minimizes or removes the voltage overshoot.

If the device is set to shut down (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin down to make sure there is a proper low level. Returning from those states causes a new start-up sequence as set by the SS/TR connection.

#### *8.3.4.1 Tracking Function*

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage with the typical gain and offset as specified in the *Electrical Characteristics*.

**Note**

In forced PWM (FPWM) mode the output voltage increases and decreases with any changes in the tracking voltage, but in auto PFM (power save) mode, the output voltage only decreases based on the load current.

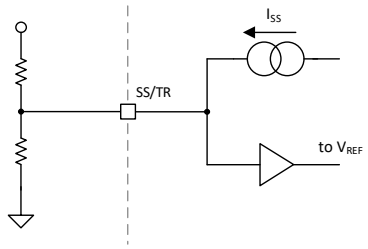



**Figure 8-4. Tracking Operation Simplified Schematic**

$$V_{FB} = 0.75 \times V_{SS/TR} \quad (1)$$

When the SS/TR pin voltage is above 0.8 V, the internal voltage is clamped and the device goes to normal regulation. This action works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing the SS/TR pin voltage in PFM mode, the device does not sink current from the output. The resulting decrease of the output voltage can therefore be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin, which is 6 V. The SS/TR pin is internally connected with a resistor to GND when EN = 0.

If the input voltage drops below undervoltage lockout, the output voltage goes to zero, independent of the tracking voltage. Figure 8-5 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function. See Section 9.4.3 in the systems examples.


Copyright © 2023 Texas Instruments Incorporated

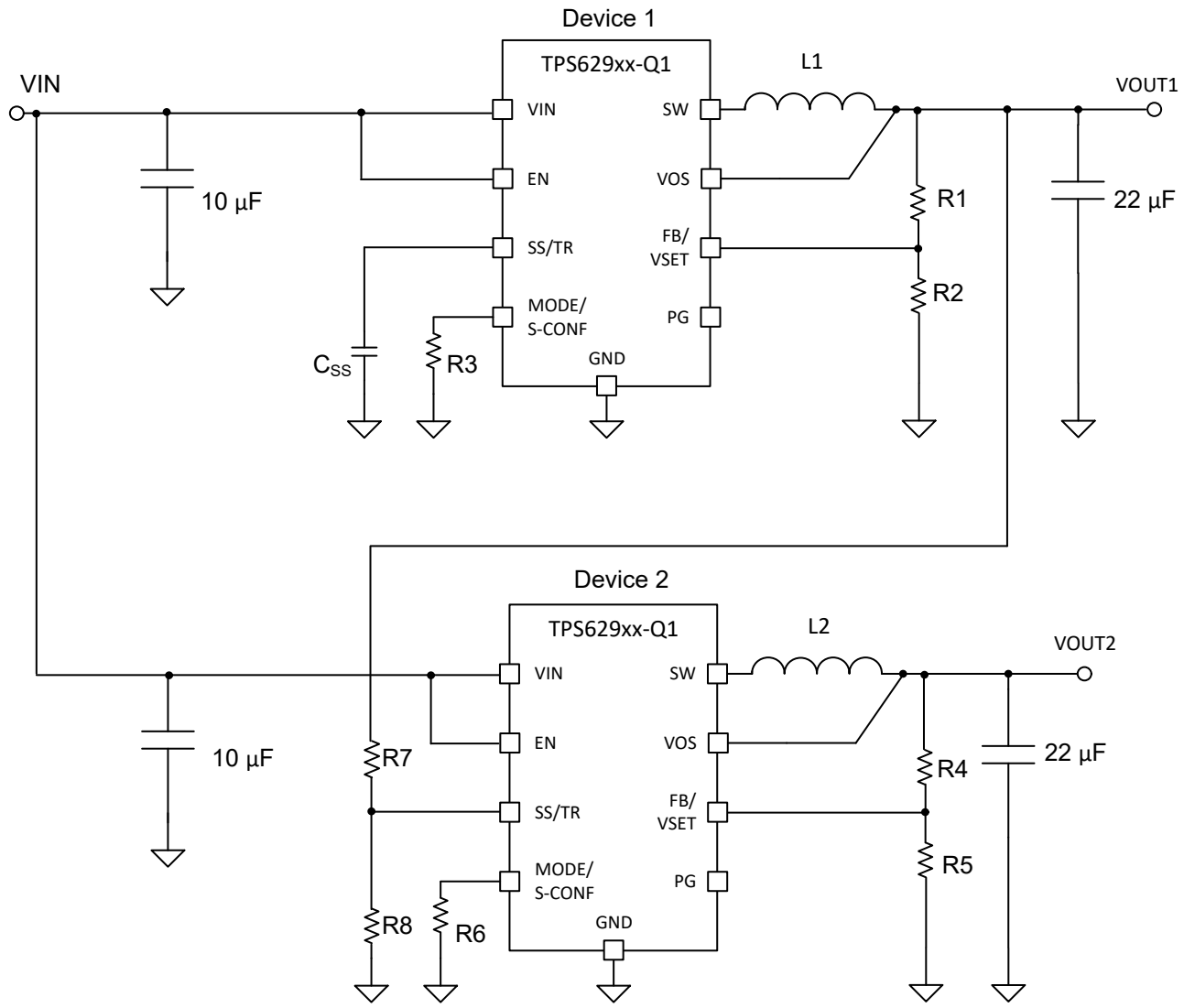



**Figure 8-5. Schematic for Ratiometric and Simultaneous Start-Up**

The resistive divider of R7 and R8 can be used to change the ramp rate of VOUT2 to be faster, slower, or the same as VOUT1.

A sequential start-up is achieved by connecting the PG pin of VOUT of device 1 to the EN pin of device 2. PG requires a pullup resistor. Ratiometric start-up sequence happens if both supplies are sharing the same soft-start capacitor. Equation 18 gives the soft-start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in the *Sequencing and Tracking With the TPS621-Family and TPS821-Family* application report.

**Note**

If the voltage at the FB pin is below its typical value of 0.6 V, the output voltage accuracy can have a wider tolerance than specified. The current of 2.5 µA out of the SS/TR pin also has an influence on the tracking function, especially for high resistive external voltage dividers on the SS/TR pin.

### 8.3.5 Smart Enable with Precise Threshold

The voltage applied at the enable pin of the TPS62992-Q1 is compared to a fixed threshold rising voltage. This allows the user to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

Copyright © 2023 Texas Instruments Incorporated

The precise enable input allows the user to program the undervoltage lockout by adding a resistor divider to the input of the EN pin.

The enable input threshold for a falling edge is lower than the rising edge threshold. The TPS62992-Q1 starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off.

An internal resistor pulls the EN pin to GND when the device is disabled and avoids the pin to be floating (after the device is enabled, the pulldown is removed). This prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to a low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

### 8.3.6 Power Good (PG)

The TPS62992-Q1 has a built-in power-good (PG) feature to indicate whether the output voltage has reached its target and the device is ready. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to the recommended input voltage level. PG is low when the device is turned off due to EN, UVLO (undervoltage lockout), or thermal shutdown. $V_{IN}$ must remain present for the PG pin to stay low.

If the power-good output is not used, TI recommends to tie to GND or leave it open.

**Table 8-3. Power Good Indicator Functional Table**

| Logic Signals | | | | PG Status |
|---|---|---|---|---|
| $V_{IN}$ | EN Pin | Thermal Shutdown | $V_{OUT}$ | |
| $V_{IN}$ > UVLO | HIGH | No | $V_{OUT}$ on target | High Impedance |
| | | | $V_{OUT}$ < target | LOW |
| | | Yes | × | LOW |
| | LOW | × | × | LOW |
| 1.8 V< $V_{IN}$ < UVLO | × | × | × | LOW |
| $V_{IN}$ < 1.8 V | × | × | × | Undefined |

**Note**

For prebiased $V_{OUT}$ conditions (during start-up) of 60% or more of the programmed output voltage, a minimum 250-µs external soft start ($C_{SS}$ > 0.75 nF) is required. If the 250-µs soft start minimum is not ensured and $V_{OUT}$ is prebiased above 60% of the programmed output voltage during start-up, PG can be seen asserted "early" before $V_{OUT}$ reaches the PG rising threshold, a glitch on PG can be observed, or both.

### 8.3.7 Output Discharge Function

The purpose of the discharge function is to make sure there is a defined down-ramp of the output voltage when the device is being disabled, and to also keep the output voltage close to 0 V when the device is off. This can be especially useful for applications with a system wide EN function that removes the output load in conjunction with disabling the power supply.

The output discharge feature is only active after the TPS62992-Q1 has been enabled at least once since the supply voltage was applied ($V_{VIN}$ > UVLO). The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V.


Copyright © 2023 Texas Instruments Incorporated

### 8.3.8 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

### 8.3.9 Current Limit and Short-Circuit Protection

The TPS62992-Q1 is protected against overload and short-circuit events. If the inductor current exceeds the high-side FET current limit ($I_{LIMH}$), the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current. The high-side FET turns on again only if the current in the low-side FET has decreased below the low-side FET current limit threshold AND the internal $I_{LIM}$ recovery delay has expired.

**Note**

While the internal recovery delay generally keeps the switching frequency within the normal operating range of the device , the switching frequency is not tightly controlled during overload events.

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is given as Equation 2:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{pd} \quad (2)$$

where

- $I_{LIMH}$ is the static high-side FET current limit as specified in the *Electrical Characteristics*.
- L is the effective inductance at the peak current.
- $V_L$ is the voltage across the inductor ($V_{IN}$–$V_{OUT}$).
- $t_{PD}$ is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductance is used. The dynamic high-side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{VIN} - V_{VOUT}}{L} \times 50ns \quad (3)$$

The TPS62992-Q1 also includes a low-side negative current limit ($I_{LIM:SINK}$) to protect against excessive negative currents that can occur in forced PMW mode under heavy to light load transient conditions. If the negative current in the low-side switch exceeds the $I_{LIM:SINK}$ threshold, the low-side switch is disabled. Both the low-side and high-side switches remain off until an internal timer re-enables the high-side switch based on the selected PWM switching frequency.

**CAUTION**

If Forced PWM (FPWM) mode is being used, TI recommends that the inductor be sized such that the inductor ripple current, $\Delta I_L$ (see Equation 9), does not exceed 2.6 A to avoid the potential for continuous operation of the negative current limit with no output load ($I_O$ = 0 A).

### 8.3.10 High Temperature Specifications

The TPS62992-Q1 is capable of high operating junction temperatures up to 165°C. The AEC-Q100 Grade-1 maximum ambient temperature requirement ($T_{A_max}$ = 125°C) combined with power dissipation on integrated chips often results in device operating temperatures well above 125 °C. Additionally, although Grade 1 with extended temperature does not exist as a standard by itself, the 165°C maximum operating junction temperature allows for the TPS62992-Q1 to be used in applications with ambient temperatures upwards of 150°C that require less device power dissipation.

Copyright © 2023 Texas Instruments Incorporated

**Note**

For more information on the different thermal metrics for semiconductor integrated circuits (ICs) including the relationship between the operating junction ($T_J$) and ambient ($T_A$) temperatures of a device, refer to the *Semiconductor and IC Package Thermal Metrics* application report.

The TPS62992-Q1 is designed to sustain these high temperatures while maintaining performance and reliability, which is accomplished by compliant electrical specifications up to $T_J$ = 165°C. In addition, extra reliability testing has been performed that exceeds the AEC-Q100 Grade 1 requirements.

### 8.3.11 Thermal Shutdown

The junction temperature, $T_J$, of the device is monitored by an internal temperature sensor. If $T_J$ rises and exceeds the thermal shutdown threshold, $T_{SD}$, the device shuts down. Both the high-side and low-side power FETs are turned off and PG goes low. When $T_J$ decreases below the hysteresis, the converter resumes normal operation, beginning with soft start. In PSM during a PFM skip pause (when both high-side and low-side FETs are off, the thermal shutdown feature is not active. A shutdown or restart is only triggered during a switching cycle. See Section 8.4.2.


Copyright © 2023 Texas Instruments Incorporated

## 8.4 Device Functional Modes

### 8.4.1 Forced Pulse Width Modulation (FPWM) Operation

The TPS62992-Q1 has two operating modes: Forced PWM (FPWM) mode discussed in this section and auto PFM and PWM as discussed in Section 8.4.2.

With the MODE/S-CONF pin configured for FPWM mode, the TPS62992-Q1 operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of either 2.5 MHz or 1.0 MHz. The frequency variation in PWM is controlled and depends on $V_{IN}$, $V_{OUT}$, and the inductance. The on time in forced PWM mode is given by Equation 4:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \tag{4}$$

For very small output voltages, a minimum on time of approximately 30 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high.

### 8.4.2 Power Save Mode Operation (Auto PFM and PWM)

When the MODE/S-CONF pin is configured for power save mode (auto PFM and PWM). The device operates in PWM mode as long the output current is higher than half of the ripple current of the inductor, and seamlessly transitions to PSM operation as the load decreases. In power save mode, the device operates in PFM mode by reducing the switching frequency linearly with the load current to maintain high efficiency under light load operation. The device remains in power save mode as long as the inductor current remains discontinuous, and the transition out of PSM also occurs seamlessly when the load current increases above the DCM boundary.

In addition to operating in PFM under light load, when the 2.5 MHz $F_{SW}$ option is selected, the TPS62992-Q1 further adjusts the on time (TON), depending on the input voltage and the output voltage to maintain highest efficiency using the AEE function as described in Section 8.4.3 .

In power save mode, the TON time can be estimated using Equation 4 for 1 MHz and Equation 8 for 2.5 MHz.

For higher input voltages and small output voltages, an absolute minimum on time of approximately 30 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Using TON, the typical peak inductor current in power save mode is approximated by Equation 5:

$$ILPSM_{peak} = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \tag{5}$$

The output voltage ripple in power save mode is given by Equation 6:

$$\Delta V = \frac{L \times V_{IN}^2}{200 \times C} + \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right) \tag{6}$$

where

- L is the effective inductance.
- C is the output effective capacitance.

**Note**

When $V_{IN}$ decreases to typically 15% above $V_{OUT}$, the TPS62992-Q1 does not enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

### 8.4.3 AEE (Automatic Efficiency Enhancement)

When the MODE/S-CONF pin is configured for auto PFM/PWM with AEE mode, the TPS62992-Q1 provides the highest efficiency over the entire input voltage and output voltage range by automatically adjusting the switching frequency of the converter (see Equation 7). To keep the efficiency high over the entire duty cycle range, the switching frequency is adjusted while maintaining the ripple current amplitudes. This feature compensates for the very small duty cycles of high $V_{IN}$ to low $V_{OUT}$ conversions, which can limit the control range in other topologies.

Copyright © 2023 Texas Instruments Incorporated

$$F_{SW}\left(MHz\right) = 10 \times V_{OUT} \times \frac{V_{IN} - V_{OUT}}{{V_{IN}}^2} \quad (7)$$

Traditionally, the efficiency of a switched mode converter decreases if $V_{OUT}$ decreases, $V_{IN}$ increases, or both. By decreasing the switching losses at lower $V_{OUT}$ values or higher $V_{IN}$ values, the AEE feature provides an efficiency enhancement across various duty cycles, especially for the lower $V_{OUT}$ values, where fixed frequency converters suffer from a significant efficiency drop.

To accomplish this, the AEE function in the TPS62992-Q1 adjusts the on time (TON) depending on the input voltage and the output voltage, and the on time in steady-state operation can be estimated as using Equation 8:

$$T_{ON}\left(ns\right) = 100 \times \frac{V_{IN}}{V_{IN} - V_{OUT}} \quad (8)$$

By using the same TON configuration (see Equation 9) across the entire load range in AEE mode, the inductor ripple current in AEE mode becomes effectively independent of the output voltage and can be approximated by Equation 9:

$$\Delta I_L\left(mA\right) = T_{ON} \times \frac{V_{IN} - V_{OUT}}{L} = 0.1 \times \frac{V_{IN}\,(V)}{L\,(\mu H)} \quad (9)$$

The TPS62992-Q1 operates in AEE mode as long as the output current is higher than half the ripple current of the inductor. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous mode (DCM), which happens when the output current becomes smaller than half the inductor ripple current.

### 8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter operating in PWM mode is given as D = $V_{OUT}$ / $V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage and the off time gets smaller. When the minimum off time of typically 80 ns is reached, the TPS62992-Q1 scales down its switching frequency while it approaches 100% mode. In 100% mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point, allowing the conversion of small input to output voltage differences (for example, getting longest operation time of battery-powered applications). In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$V_{IN\,(MIN)} = V_{OUT} + I_{OUT} \times \left(R_{DS(ON)} + R_L\right) \quad (10)$$

where

- IOUT is the output current.
- $R_{DS(on)}$ is the on-state resistance of the high-side FET.
- $R_L$ is the DC resistance of the inductor used.

### 8.4.5 Starting into a Prebiased Load

The TPS62992-Q1 is capable of starting into a prebiased output. The device only starts switching when the internal soft-start ramp is equal or higher than the feedback voltage. If the voltage at the feedback pin is biased to a higher voltage than the nominal value, the TPS62992-Q1 does not start switching unless the voltage at the feedback pin drops to the target. See the note in Section 8.3.6 regarding the soft-start requirement during prebiased conditions.


Copyright © 2023 Texas Instruments Incorporated

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The TPS62992-Q1 devices are highly efficient, small, and highly flexible synchronous step-down DC/DC converters that are easy to use. A wide input voltage range of 3 V to 10 V supports a wide variety of inputs like 9-V supply rails, single-cell or multi-cell Li-Ion, and 5-V or 3.3-V rails.

## 9.2 Typical Application with Adjustable Output Voltage

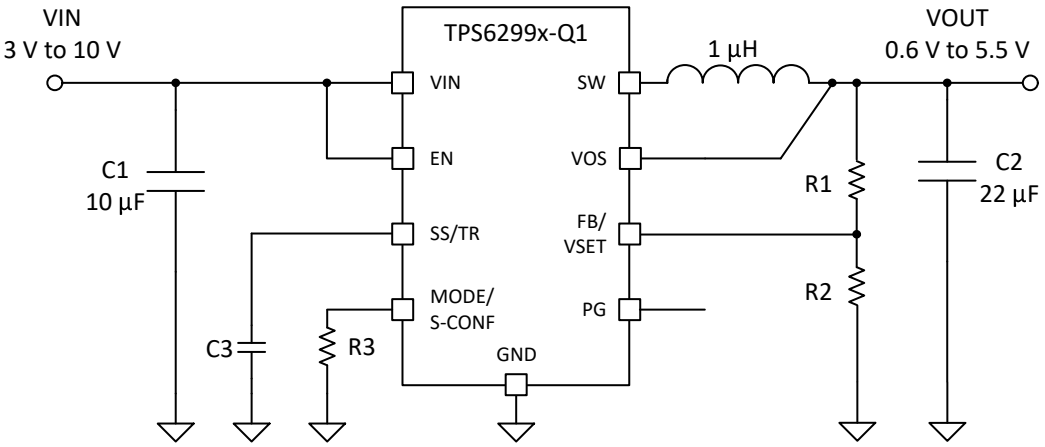



**Figure 9-1. Typical Application Circuit**

### 9.2.1 Design Requirements

**Table 9-1. List of Components**

| Reference | Description | Manufacturer |
|---|---|---|
| IC | 10 V, 2-A step-down converter | TPS62992-Q1 series; Texas Instruments |
| L | 1-µH inductor | XGL4020-102; Coilcraft |
| CIN | 10 µF, 25 V, Ceramic, X8R | CGA6P1X8R1E106K250AE, TDK |
| COUT | 22 µF, 16 V, Ceramic, X8L | CGA6P1X8L1C226M250AC, TDK |
| CSS | Depends on soft-start time; see Section 9.2.2.3.3.3. | AEC-Q200 qualified, 16 V, Ceramic, X8R |
| R1 | Depending on $V_{OUT}$; see Section 9.2.2.2. | AEC-Q200 qualified, Standard 1% metal film |
| R2 | Depending on $V_{OUT}$; see Section 9.2.2.2. | AEC-Q200 qualified, Standard 1% metal film |
| R3 | Depending on device setting, see Section 8.3.1. | AEC-Q200 qualified, Standard 1% metal film |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TPS62992-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.

Copyright © 2023 Texas Instruments Incorporated

3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 9.2.2.2 Programming the Output Voltage

When the MODE/S_CONF pin is configured for external feedback, the output voltage of the TPS62992-Q1 is fully adjustable. It can be programmed for output voltages from 0.6 V to 5.5 V using a resistor divider from $V_{OUT}$ to GND. The voltage at the FB pin is regulated to 600 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 11. TI recommends to choose resistor values that allow a current of at least 2 µA, meaning the value of R2 must not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2 \times \left(\frac{VOUT}{VFB} - 1\right) \tag{11}$$

With typical VFB = 0.6 V:

**Table 9-2. Setting the Output Voltage**

| Nominal Output Voltage | R1 | R2 | Exact Output Voltage |
|---|---|---|---|
| 0.75 V | 24.9 kΩ | 100 kΩ | 0.749 V |
| 1.2 V | 100 kΩ | 100 kΩ | 1.2 V |
| 1.5 V | 150 kΩ | 100 kΩ | 1.5 V |
| 1.8 V | 200 kΩ | 100 kΩ | 1.8 V |
| 2.0 V | 49.9 kΩ | 21.5 kΩ | 1.992 V |
| 2.5 V | 100 kΩ | 31.6 kΩ | 2.498 V |
| 3.0 V | 100 kΩ | 24.9 kΩ | 3.009 V |
| 3.3 V | 113 kΩ | 24.9 kΩ | 3.322 V |
| 5.0V | 182 kΩ | 24.9 kΩ | 4.985 V |

#### 9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the control loop of the device. The TPS62992-Q1 is optimized to work within a range of external components.

##### 9.2.2.3.1 Output Filter and Loop Stability

The TPS62992-Q1 is designed to be stable with a range of L-C filter combinations. The LC output filters inductance and capacitance have to be considered together, creating a double pole responsible for the corner frequency of the converter using Equation 12.

$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C}} \tag{12}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 9-3 and are recommended for use with the effective capacitance considered to vary by +20% and –50%. Different values can work, but care has to be taken on the loop stability, which is affected. More information including a detailed LC stability matrix can be found in the *Optimizing the TPS62130/40/50/60 Output Filter* application report.


Copyright © 2023 Texas Instruments Incorporated

**Table 9-3. Recommended LC Output Filter Combinations**

| | 4.7 µF | 10 µF | 22 µF | 47 µF | 100 µF | 200 µF |
|---|---|---|---|---|---|---|
| 1 µH | | √ | √(1) | √ | √ | √(3) |
| 1.5 µH | | √ | √ | √ | √(3) | |
| 2.2 µH | | √ | √(2) | √ | √(3) | |
| 3.3 µH | √ | √ | √ | √ | | |

(1) This LC combination is the standard value and recommended for most applications with 2.5-MHz switching frequency.
(2) This LC combination is the standard value and recommended for most applications with 1-MHz switching frequency.
(3) Output capacitance must have a ESR of ≥ 10 mΩ for stable operation, see Section 9.4.2.

The TPS62992-Q1 includes an internal 3-pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per Equation 13 and Equation 14:

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 3pF} \quad (13)$$

$$f_{pole} = \frac{1}{2\pi \times 3pF} \times \left(\frac{1}{R_1} \times \frac{1}{R_2}\right) \quad (14)$$

Although the TPS62992-Q1 devices are stable without the pole and zero being in a particular location, an external feedforward capacitor can be added to adjust their locations to the specific needs of the application can provide better performance in power save mode, improved transient response, or both. A more detailed discussion on the optimization for stability versus transient response can be found in the *Optimizing Transient Response of Internally Compensated DC-DC Converters* and *Feedforward Capacitor to Improve Stability and Bandwidth of TPS621/821-Family* application reports.

#### 9.2.2.3.2 Inductor Selection

The TPS62992-Q1 is designed for a nominal 1-µH inductor. Larger values can be used to achieve a lower inductor current ripple, but they can have a negative impact on efficiency and transient response. Smaller values than 1 µH cause a larger inductor current ripple, which causes larger negative inductor current in forced PWM mode at low or no output current. Therefore, TI does not recommend them at large voltages across the inductor as it is the case for high input voltages and low output voltages. Low-output current in forced PWM mode causes a larger negative inductor current peak, which can exceed the negative current limit. At low or no output current and small inductor values, the output voltage cannot be regulated any more. More detailed information on further LC combinations can be found in the *Optimizing the TPS62130/40/50/60 Output Filter* application report.

The inductor selection is affected by several factors like inductor ripple current, output ripple voltage, PWM-to-PFM transition point, and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 15 calculates the maximum inductor current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{\Delta I_{L(MAX)}}{2} \quad (15)$$

$$\Delta I_{L(MAX)} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN(MAX)}}}{L_{(MIN)} \times f_{SW}} \quad (16)$$

where

- $I_{L(max)}$ is the maximum inductor current.
- $\Delta I_{L(max)}$ is the maximum peak-to-peak inductor ripple current.
- $L_{(min)}$ is the minimum effective inductor value.
- $f_{sw}$ is the actual PWM switching frequency.
- $V_{OUT}$ is the output voltage.
- $V_{IN(max)}$ is the maximum expected output voltage.

Copyright © 2023 Texas Instruments Incorporated

Calculating the maximum inductor current using the actual operating conditions gives the needed minimum saturation current of the inductor. TI recommends to add a margin of about 20%. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS62992-Q1 and are recommended for use:

**Table 9-4. List of Inductors**

| Type | Inductance [µH] | Current [A](1) | Dimensions [L × B × H] mm | Manufacturer |
|---|---|---|---|---|
| XGL4020-102ME | 1.0 µH, ±20% | 8.8 | 4.0 × 4.0 × 2.1 | Coilcraft |
| XGL4020-222ME | 2.2 µH, ±20% | 6.2 | 4.0 × 4.0 × 2.1 | Coilcraft |

(1) $I_{SAT}$ at 30% drop

The inductor value also determines the load current at which power save mode is entered:

$$I_{Load(PSM)} = \frac{1}{2} \times \Delta I_L \quad (17)$$

#### 9.2.2.3.3 Capacitor Selection

##### *9.2.2.3.3.1 Output Capacitor*

The recommended value for the output capacitor is 22 µF. The architecture of the TPS62992-Q1 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends the use of X7R or X8R dielectric capacitors. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see the *Optimizing the TPS62130/40/50/60 Output Filter* application report).

In power save mode, the output voltage ripple depends on the following:

- Output capacitance
- ESR
- ESL
- Peak inductor current

Using ceramic capacitors provides small ESR, ESL, and low ripple. The output capacitor must be as close as possible to the device.

For large output voltages, the DC bias effect of ceramic capacitors is large and the effective capacitance has to be observed.

##### *9.2.2.3.3.2 Input Capacitor*

For most applications, 10 µF nominal is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. TI recommends a low-ESR multilayer ceramic capacitor (MLCC) for best filtering and must be placed between VIN and GND as close as possible to those pins.

**Table 9-5. List of Capacitors**

| Type (1) | Nominal Capacitance [µF] | Voltage Rating [V] | Size | Manufacturer |
|---|---|---|---|---|
| CGA6P1X8R1E106K250AE | 10 | 25 | 1210 | TDK |
| CGA6P1X8L1C226M250AC | 22 | 16 | 1210 | TDK |

(1) Lower of $I_{RMS}$ at 40°C rise or $I_{SAT}$ at 30% drop

##### *9.2.2.3.3.3 Soft-Start Capacitor*

A capacitor connected between SS/TR pin and GND allows a user-programmable start-up slope of the output voltage.


Copyright © 2023 Texas Instruments Incorporated

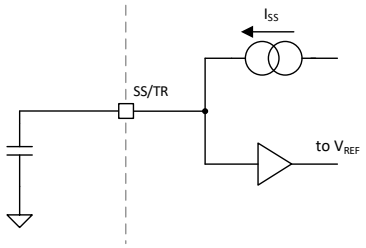



**Figure 9-2. Soft-Start Operation Simplified Schematic**

An internal constant current source is provided to charge the external capacitance. The capacitor required for a given soft-start ramp time is given by:

$$C_{SS} = T_{SS} \times \frac{I_{SS}}{V_{REF}} \quad (18)$$

where

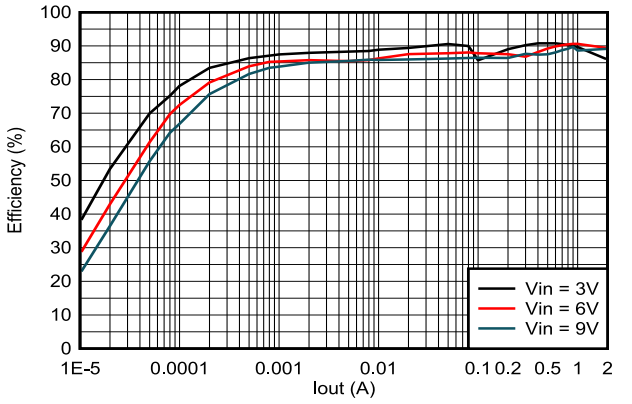
- $C_{SS}$ is the capacitance required at the SS/TR pin.
- $T_{SS}$ is the desired soft-start ramp time.
- $I_{SS}$ is the SS/TR source current, see the *Electrical Characteristics*.
- $V_{REF}$ is the feedback regulation voltage divided by tracking gain ($V_{FB}$ / 0.75); see the *Electrical Characteristics*.

The fastest achievable typical ramp time is 150 µs, even if the external $C_{ss}$ capacitance is lower than 680 pF or the pin is open.

Copyright © 2023 Texas Instruments Incorporated

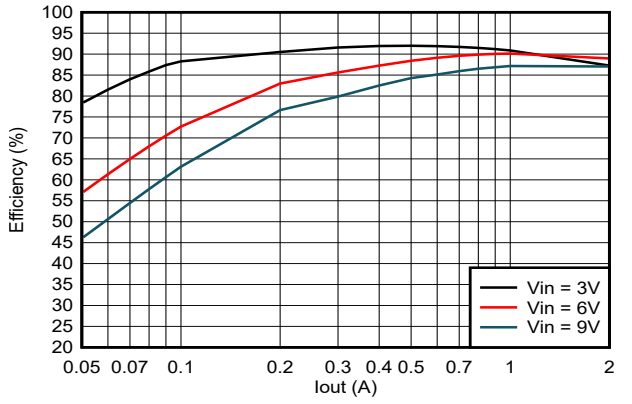
### 9.2.3 Application Curves

#### *9.2.3.1 Application Curves Vout = 1.8 V*



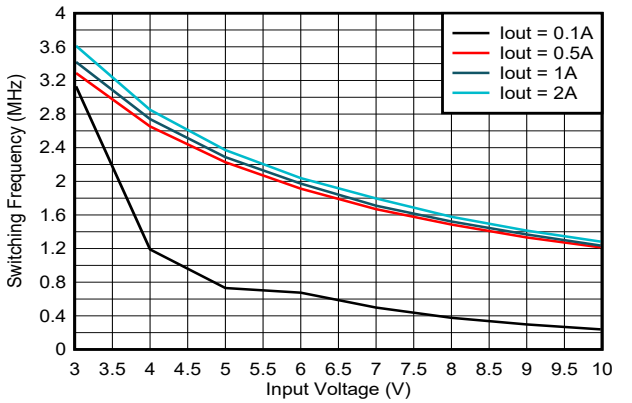

$V_{OUT}$ = 1.8 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-3. Efficiency vs Output Current**



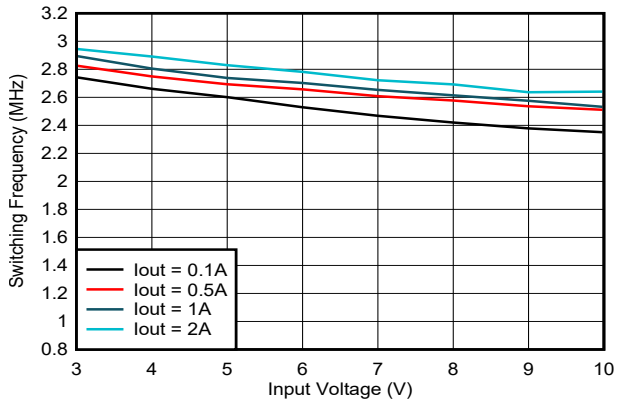

$V_{OUT}$ = 1.8 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-4. Efficiency vs Output Current**



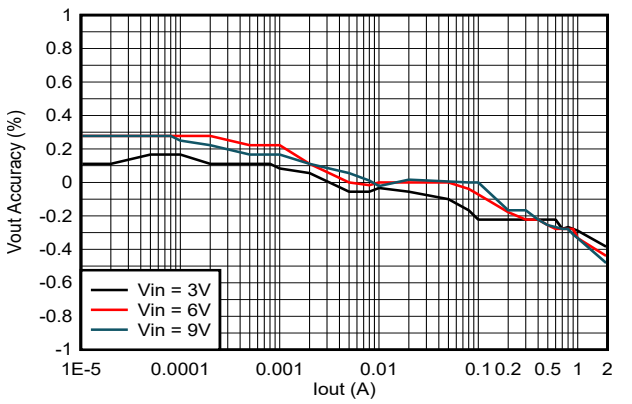

$V_{OUT}$ = 1.8 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-5. Switching Frequency vs Input Voltage**



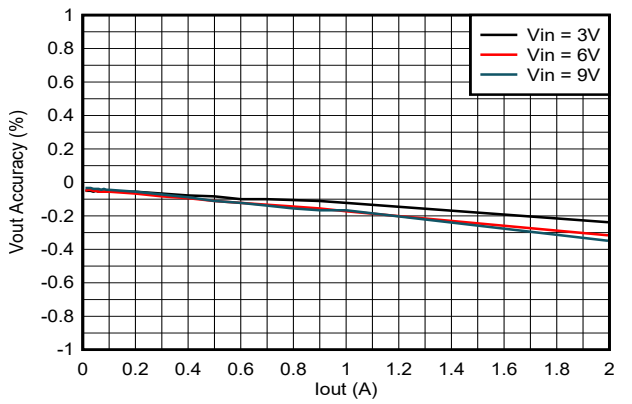

$V_{OUT}$ = 1.8 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-6. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 1.8 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

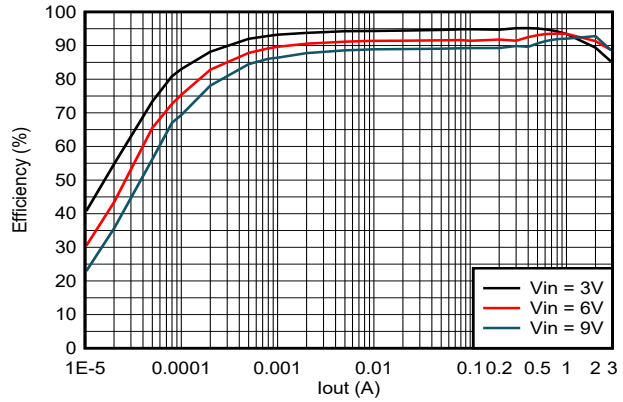
**Figure 9-7. Output Voltage vs Output Current**




$V_{OUT}$ = 1.8 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

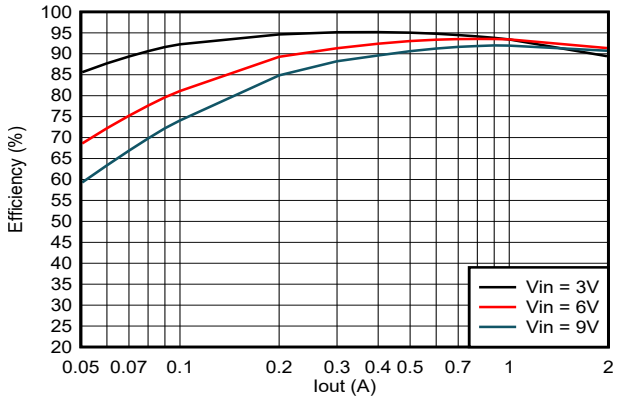
**Figure 9-8. Output Voltage vs Output Current**


Copyright © 2023 Texas Instruments Incorporated



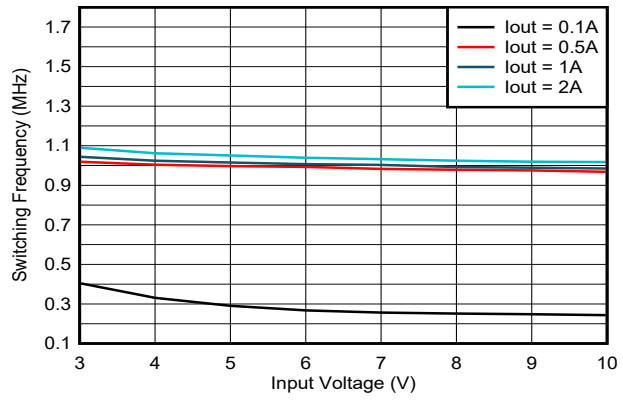

$V_{OUT}$ = 1.8 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-9. Efficiency vs Output Current**



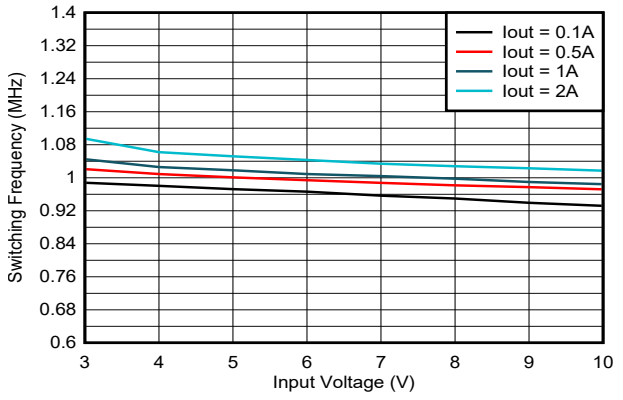

$V_{OUT}$ = 1.8 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-10. Efficiency vs Output Current**



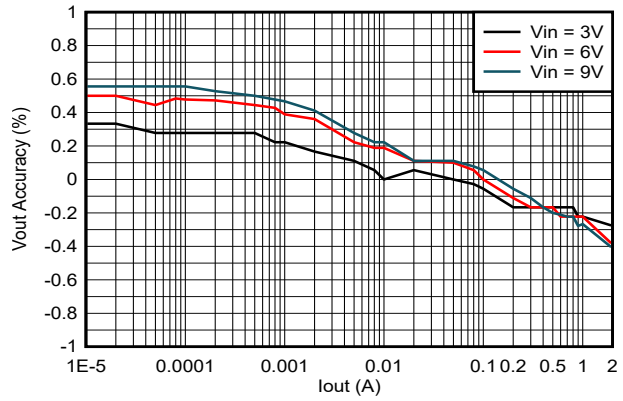

$V_{OUT}$ = 1.8 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-11. Switching Frequency vs Input Voltage**



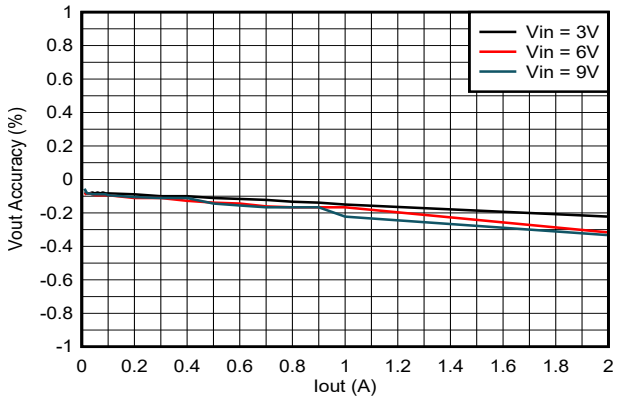

$V_{OUT}$ = 1.8 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-12. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 1.8 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

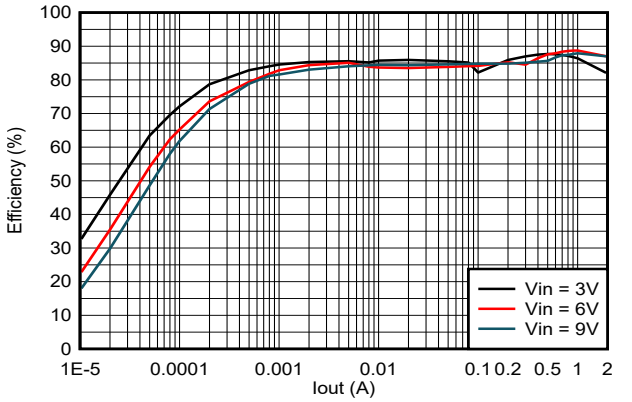
**Figure 9-13. Output Voltage vs Output Current**




$V_{OUT}$ = 1.8 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

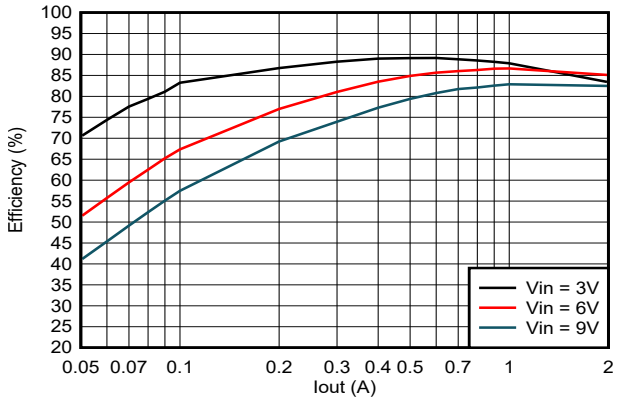
**Figure 9-14. Output Voltage vs Output Current**

### 9.2.3.2 Application Curves Vout = 1.2 V



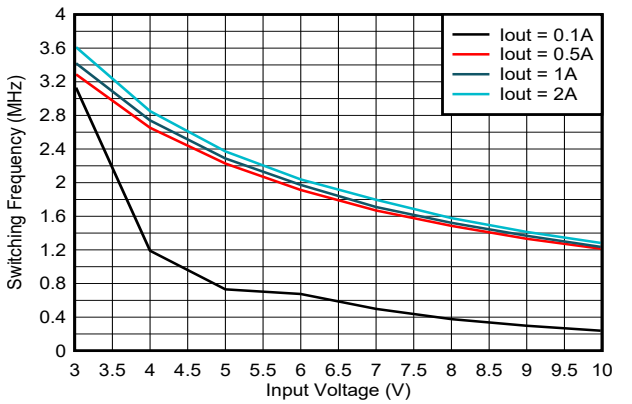

$V_{OUT}$ = 1.2 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-15. Efficiency vs Output Current**



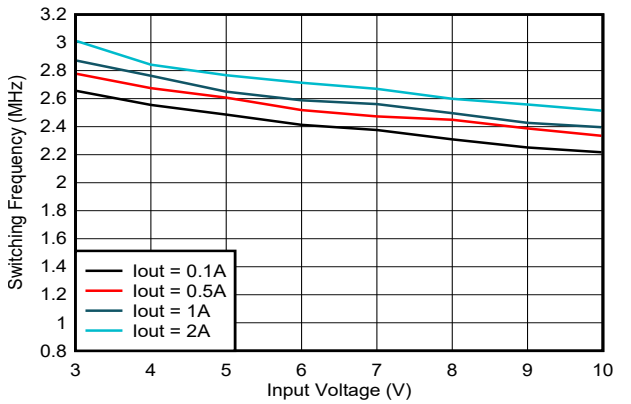

$V_{OUT}$ = 1.2 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-16. Efficiency vs Output Current**



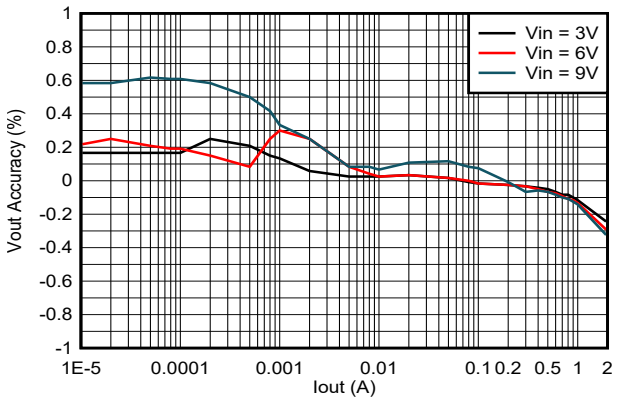

$V_{OUT}$ = 1.2 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-17. Switching Frequency vs Input Voltage**



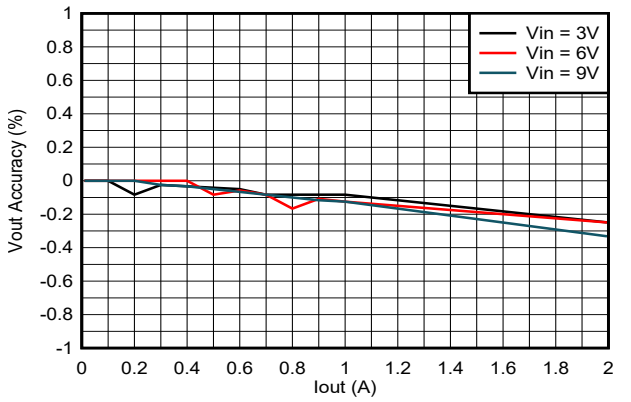

$V_{OUT}$ = 1.2 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-18. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 1.2 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

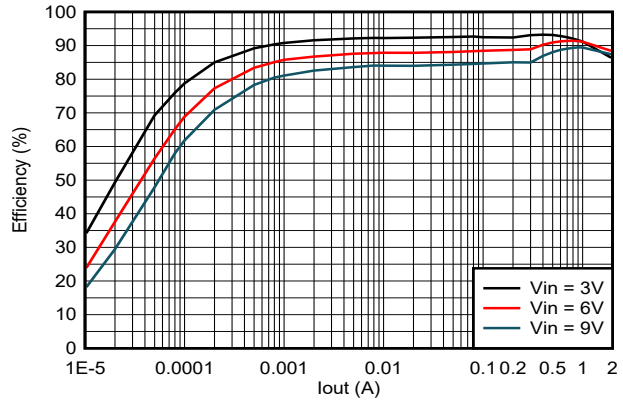
**Figure 9-19. Output Voltage vs Output Current**




$V_{OUT}$ = 1.2 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

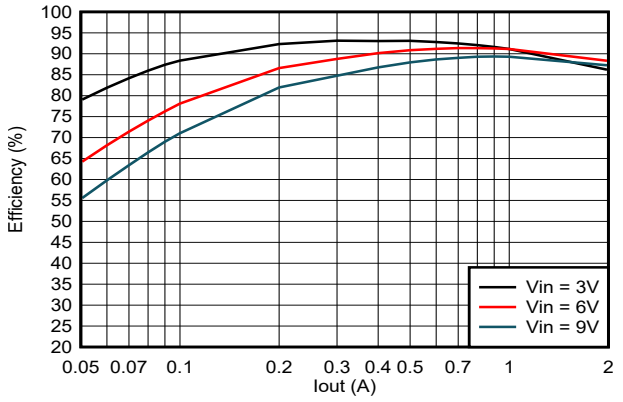
**Figure 9-20. Output Voltage vs Output Current**


Copyright © 2023 Texas Instruments Incorporated



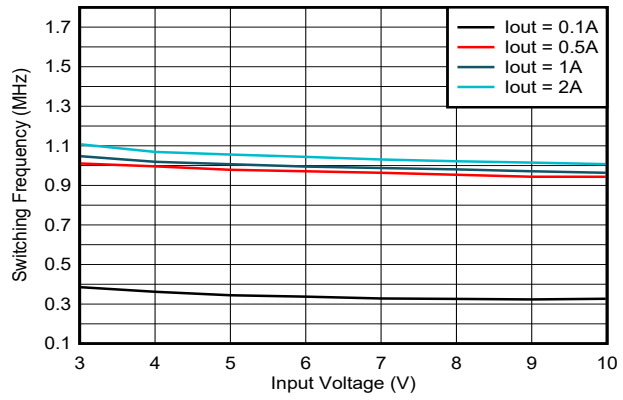

$V_{OUT}$ = 1.2 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-21. Efficiency vs Output Current**



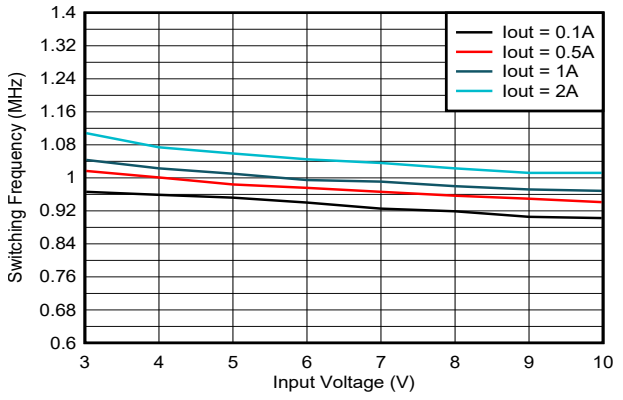

$V_{OUT}$ = 1.2 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-22. Efficiency vs Output Current**



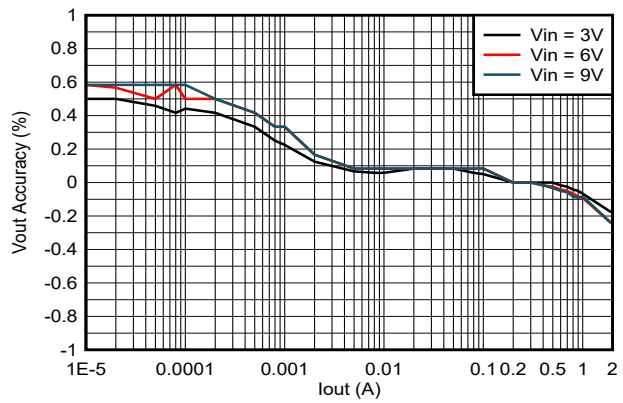

$V_{OUT}$ = 1.2 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-23. Switching Frequency vs Input Voltage**



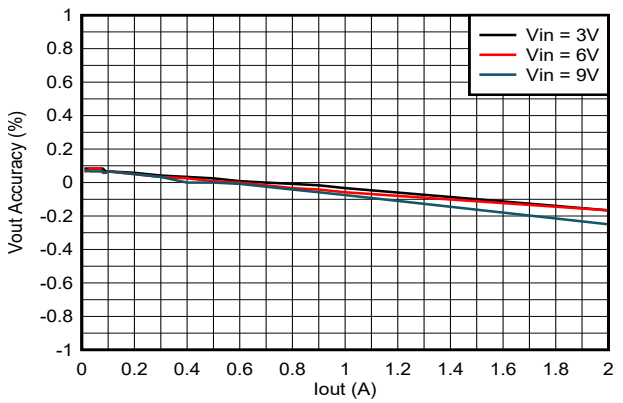

$V_{OUT}$ = 1.2 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-24. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 1.2 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

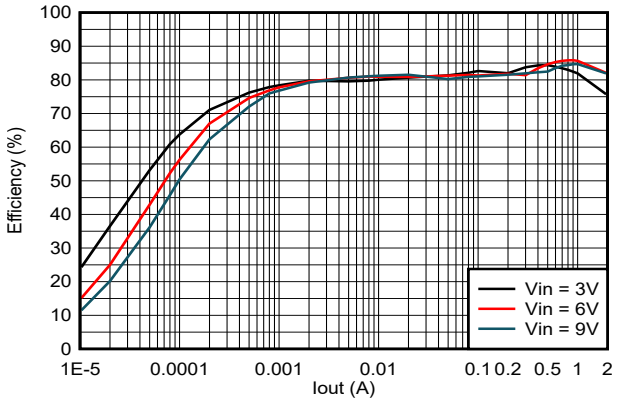
**Figure 9-25. Output Voltage vs Output Current**




$V_{OUT}$ = 1.2 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

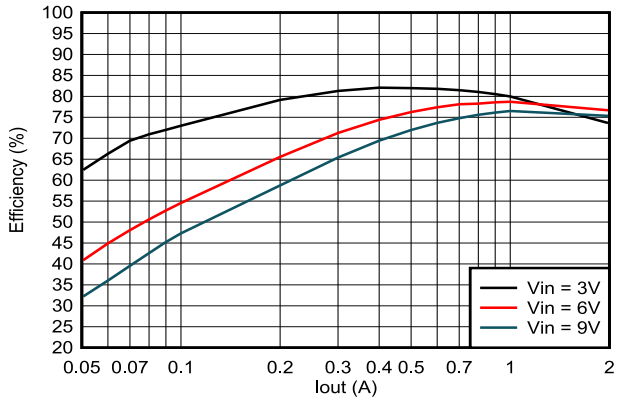
**Figure 9-26. Output Voltage vs Output Current**

### 9.2.3.3 Application Curves Vout = 0.6 V



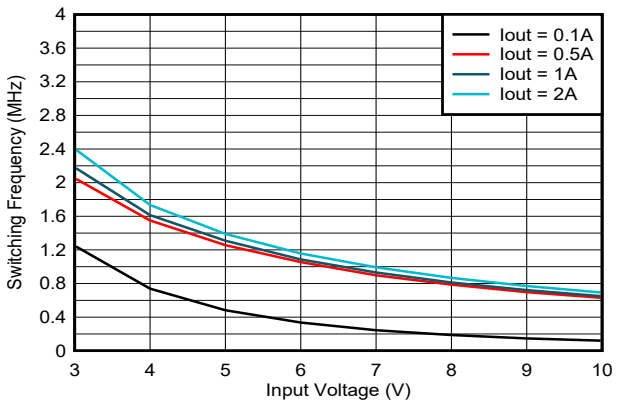

$V_{OUT}$ = 0.6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-27. Efficiency vs Output Current**



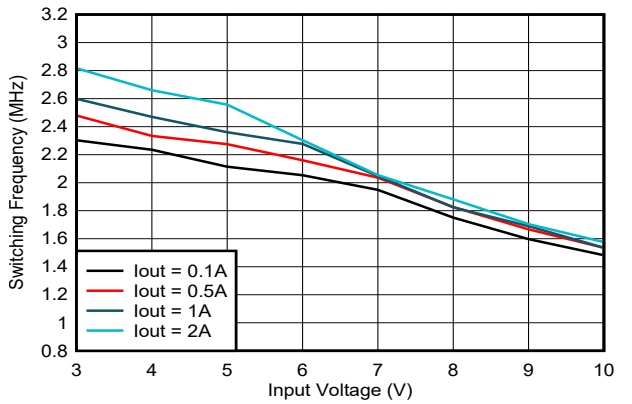

$V_{OUT}$ = 0.6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-28. Efficiency vs Output Current**



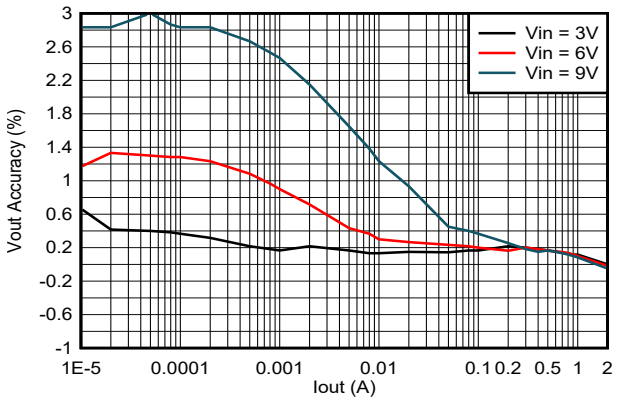

$V_{OUT}$ = 0.6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-29. Switching Frequency vs Input Voltage**



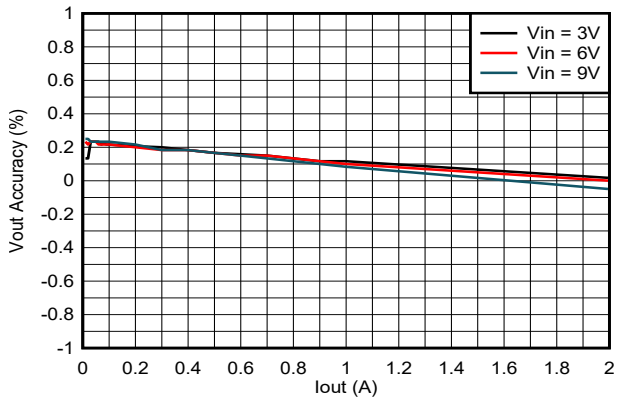

$V_{OUT}$ = 0.6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-30. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 0.6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

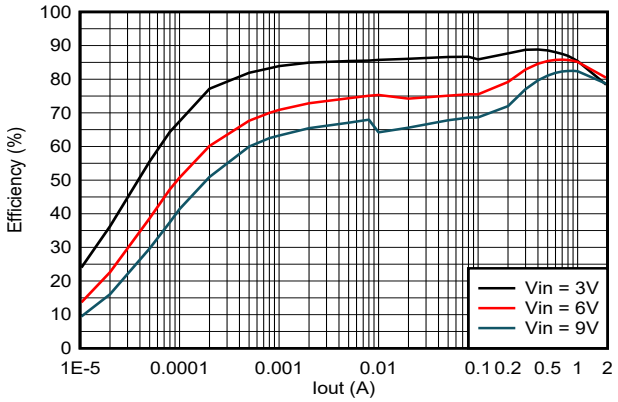
**Figure 9-31. Output Voltage vs Output Current**




$V_{OUT}$ = 0.6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

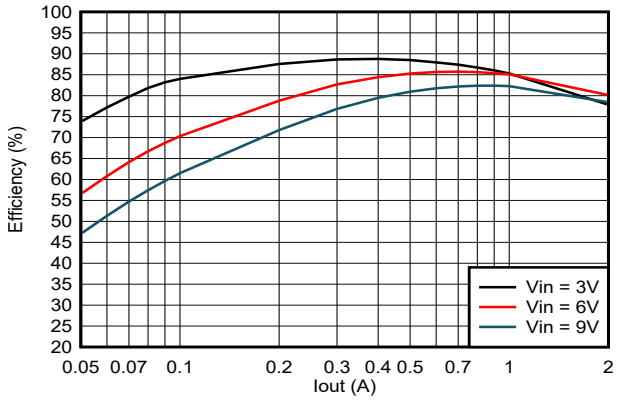
**Figure 9-32. Output Voltage vs Output Current**


Copyright © 2023 Texas Instruments Incorporated



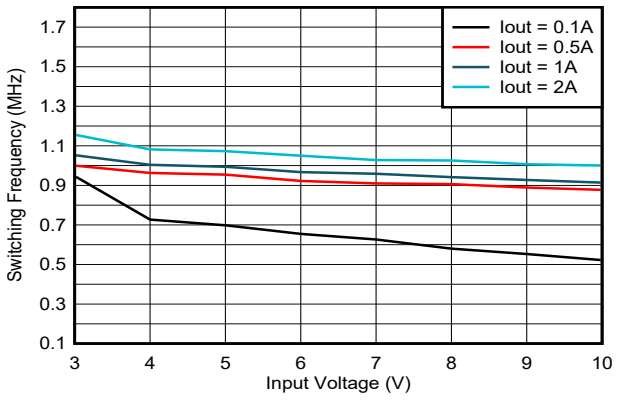

$V_{OUT}$ = 0.6 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-33. Efficiency vs Output Current**



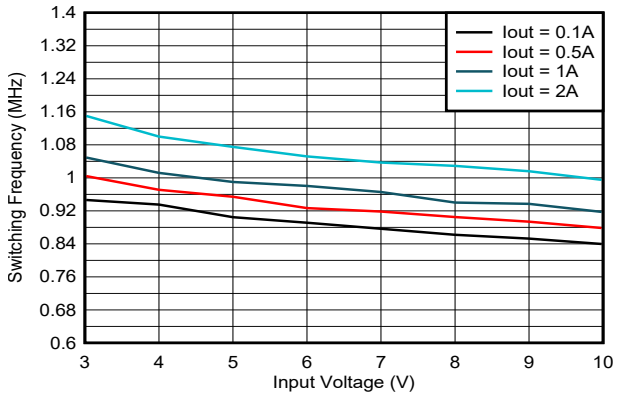

$V_{OUT}$ = 0.6 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-34. Efficiency vs Output Current**



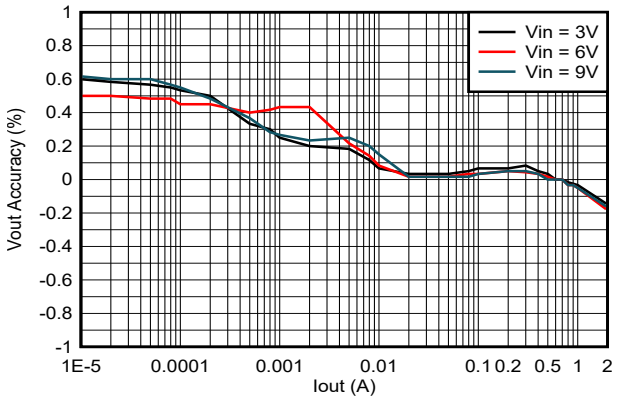

$V_{OUT}$ = 0.6 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-35. Switching Frequency vs Input Voltage**



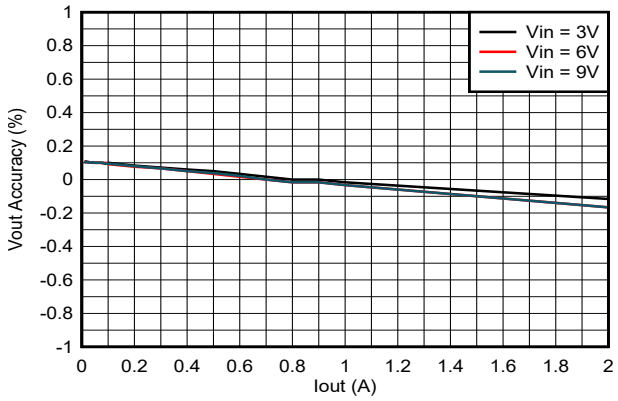

$V_{OUT}$ = 0.6 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-36. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 0.6 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-37. Output Voltage vs Output Current**




$V_{OUT}$ = 0.6 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-38. Output Voltage vs Output Current**

Copyright © 2023 Texas Instruments Incorporated

## 9.3 Typical Application with Selectable $V_{OUT}$ using VSET

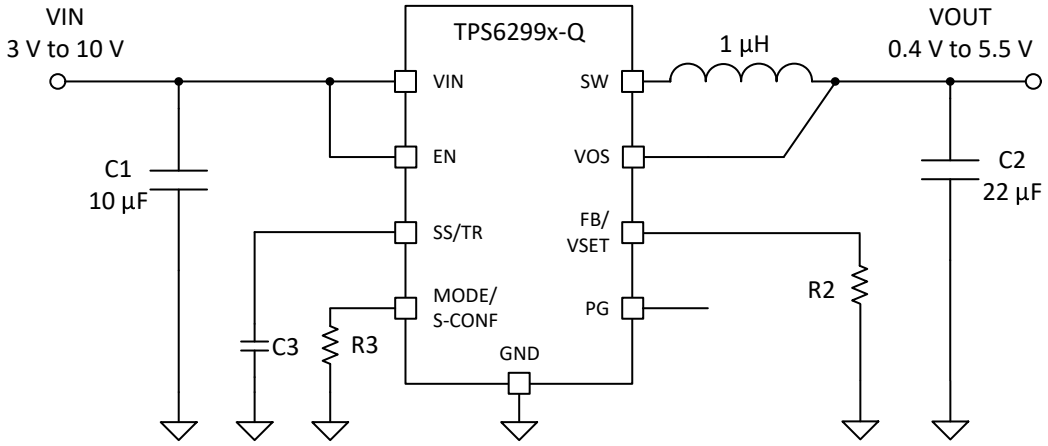



**Figure 9-39. Typical Application Circuit (VSET)**

### 9.3.1 Design Requirements

**Table 9-6. List of Components**

| Reference | Description | Manufacturer |
|---|---|---|
| IC | 10 V, 2-A step-down converter | TPS62992-Q1 series; Texas Instruments |
| L | 1-µH inductor | XGL4020-102; Coilcraft |
| CIN | 10 µF, 25 V, Ceramic, X8R | CGA6P1X8R1E106K250AE, TDK |
| COUT | 22 µF, 16 V, Ceramic, X8L | CGA6P1X8L1C226M250AC, TDK |
| CSS | Depends on soft-start time; see Section 9.2.2.3.3.3. | AEC-Q200 qualified, 16 V, Ceramic, X8R |
| R2 | Depending on $V_{OUT}$; see .Section 8.3.3 | AEC-Q200 qualified, Standard 1% metal film |
| R3 | Depending on device setting, see Section 8.3.1. | AEC-Q200 qualified, Standard 1% metal film |

### 9.3.2 Detailed Design Procedure

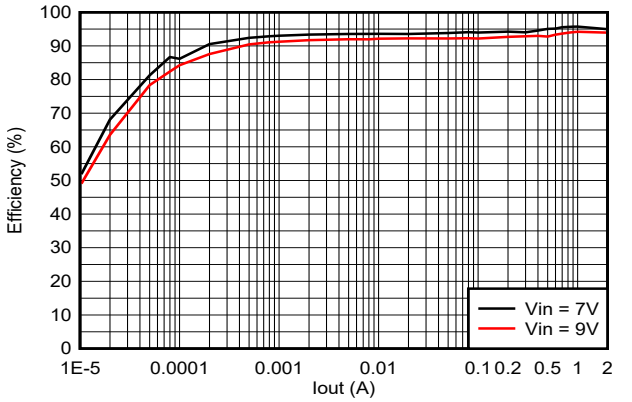
#### *9.3.2.1 Programming the Output Voltage*

When the resitor (R3) on the MODE/S-CONF pin is sized for "VSET" (internal FB) operation (see Table 8-1) , the output voltage of the TPS62992-Q1 becomes selectable with a resistor (R2) from the FB/VSET pin the GND. The output can be programmed to one of 16 different fixed output voltages ranging from 0.4 V to 5.5 V based on Table 8-2.


Copyright © 2023 Texas Instruments Incorporated

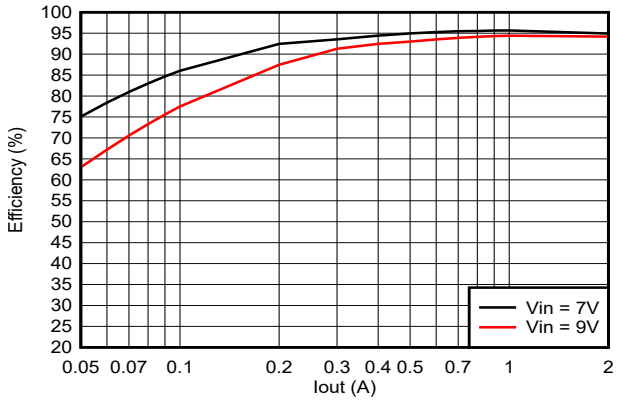
### 9.3.3 Application Curves

#### *9.3.3.1 Application Curves Vout = 5 V*



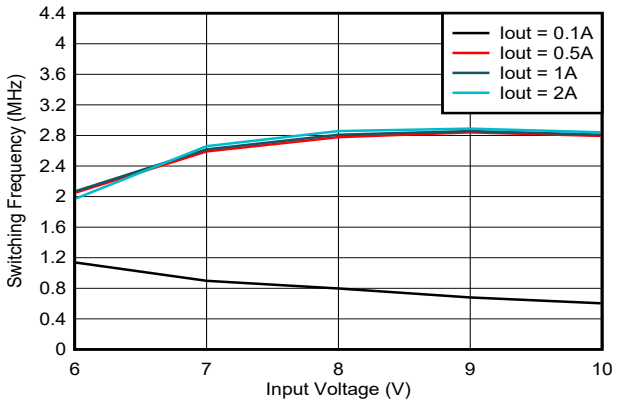

$V_{OUT}$ = 5.0 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-40. Efficiency vs Output Current**



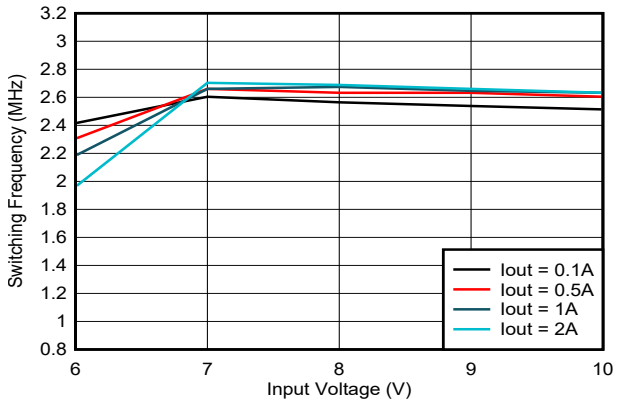

$V_{OUT}$ = 5.0 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-41. Efficiency vs Output Current**



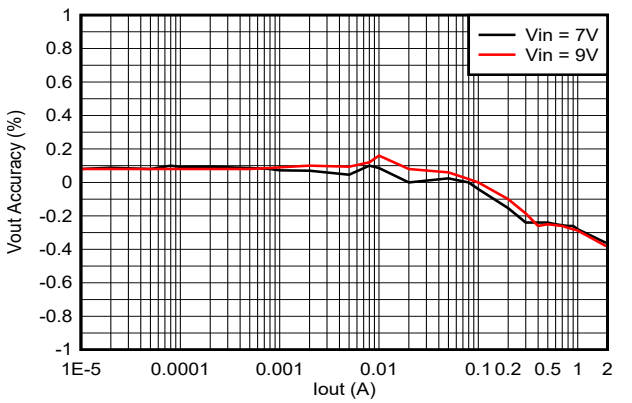

$V_{OUT}$ = 5.0 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-42. Switching Frequency vs Input Voltage**



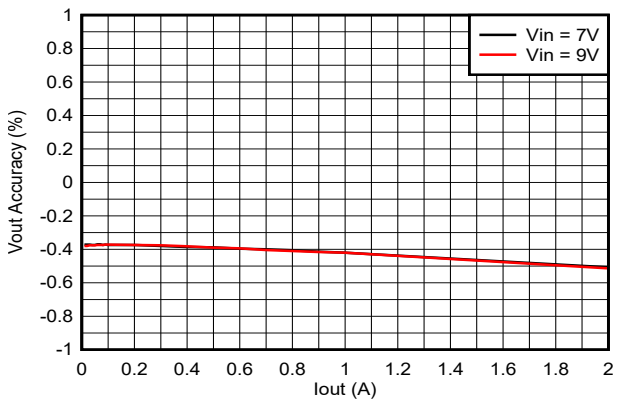

$V_{OUT}$ = 5.0 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-43. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 5.0 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

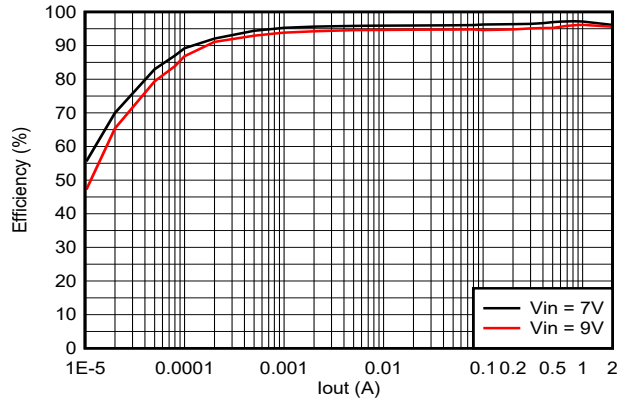
**Figure 9-44. Output Voltage vs Output Current**




$V_{OUT}$ = 5.0 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

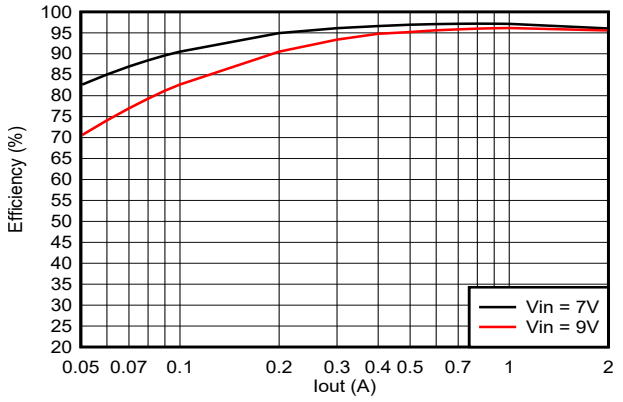
**Figure 9-45. Output Voltage vs Output Current**

Copyright © 2023 Texas Instruments Incorporated



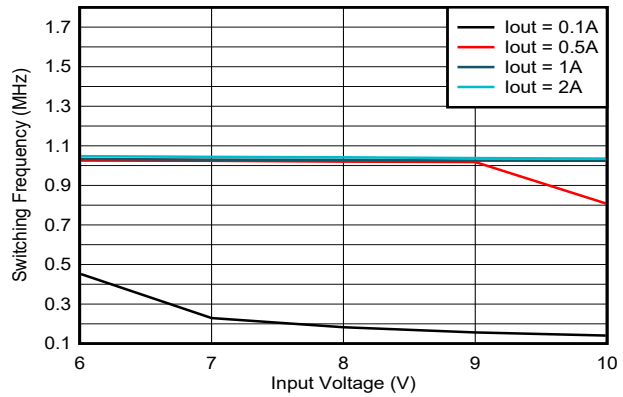

$V_{OUT}$ = 5.0 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-46. Efficiency vs Output Current**



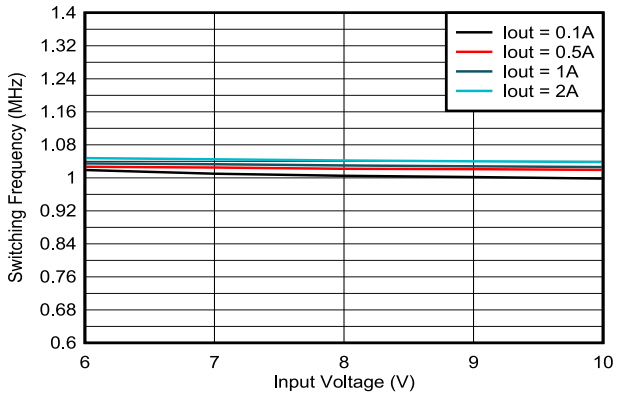

$V_{OUT}$ = 5.0 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-47. Efficiency vs Output Current**



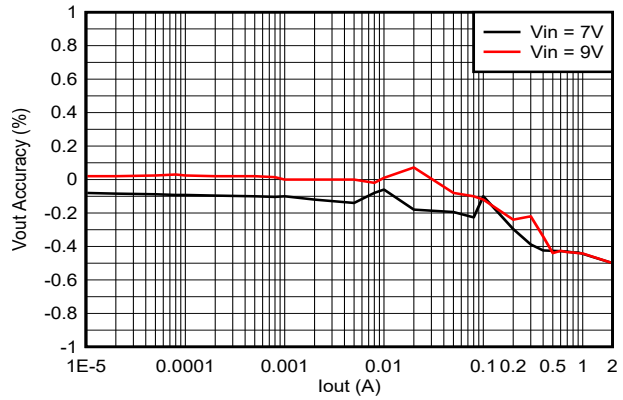

$V_{OUT}$ = 5.0 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-48. Switching Frequency vs Input Voltage**



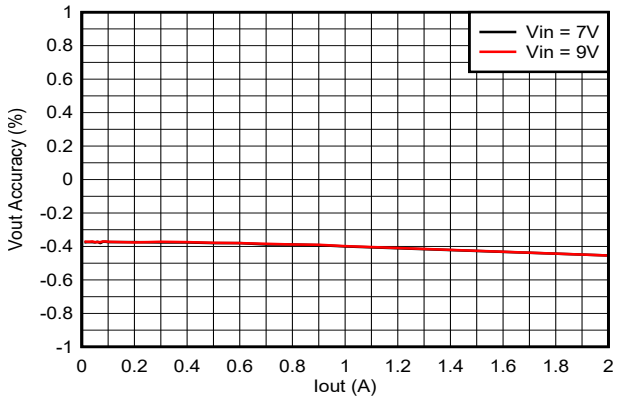

$V_{OUT}$ = 5.0 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-49. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 5.0 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-50. Output Voltage vs Output Current**

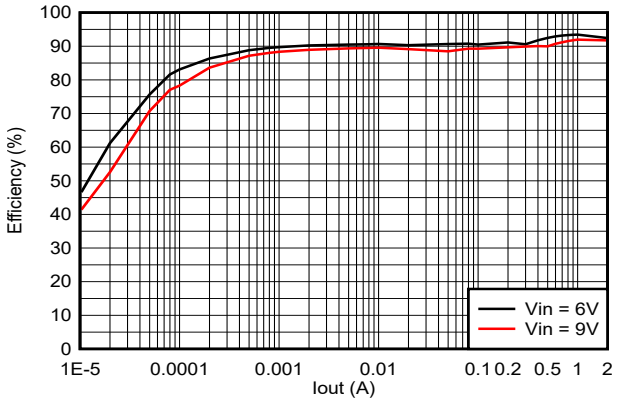



$V_{OUT}$ = 5.0 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-51. Output Voltage vs Output Current**

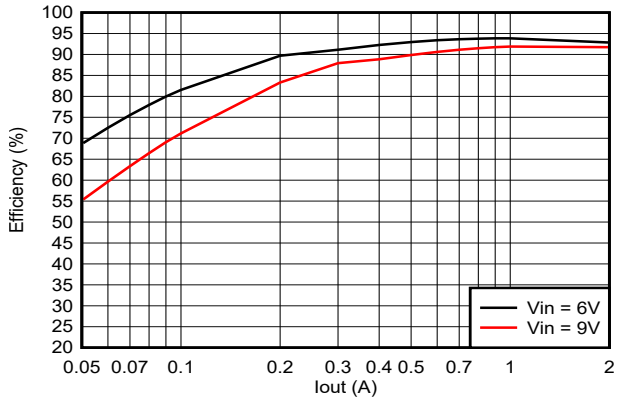

Copyright © 2023 Texas Instruments Incorporated

### 9.3.3.2 Application Curves Vout = 3.3 V



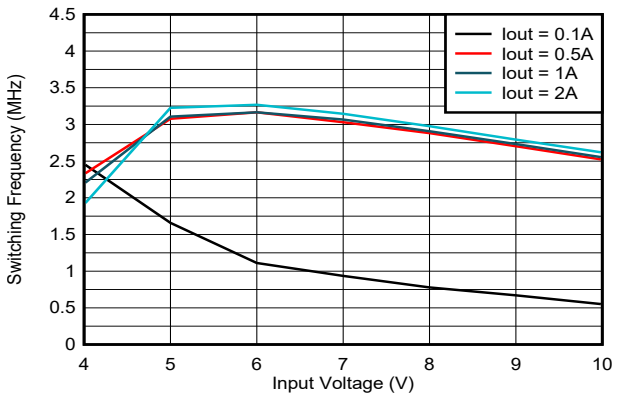

$V_{OUT}$ = 3.3 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-52. Efficiency vs Output Current**



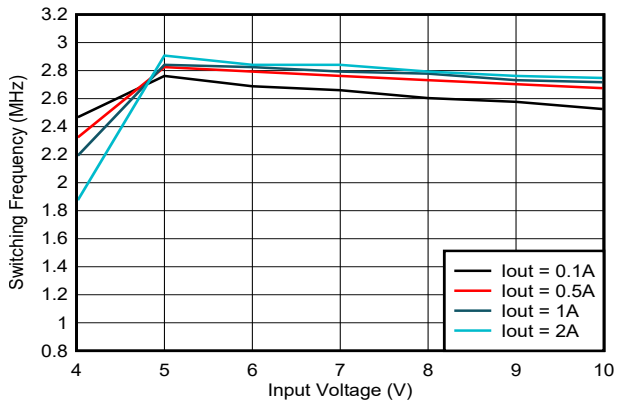

$V_{OUT}$ = 3.3 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-53. Efficiency vs Output Current**



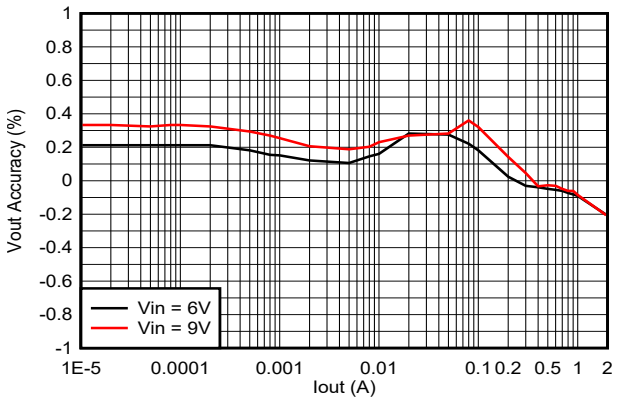

$V_{OUT}$ = 3.3 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-54. Switching Frequency vs Input Voltage**



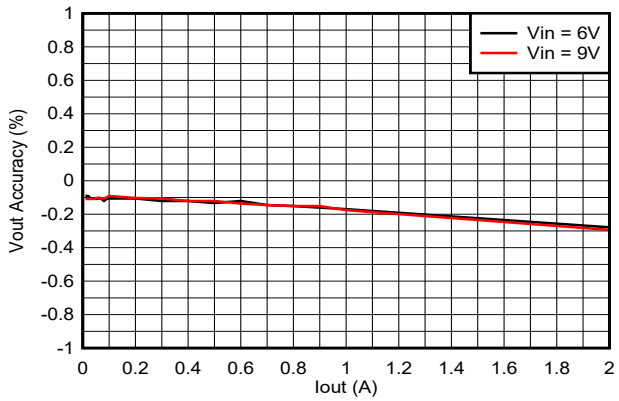

$V_{OUT}$ = 3.3 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-55. Switching Frequency vs Input Voltage**



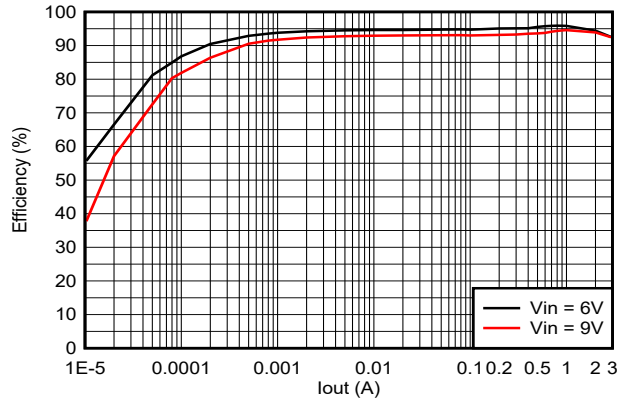

$V_{OUT}$ = 3.3 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Auto PFM/PWM

**Figure 9-56. Output Voltage vs Output Current**



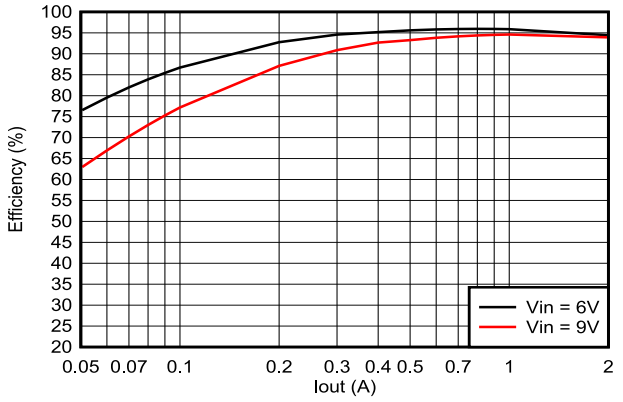

$V_{OUT}$ = 3.3 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
Forced PWM

**Figure 9-57. Output Voltage vs Output Current**



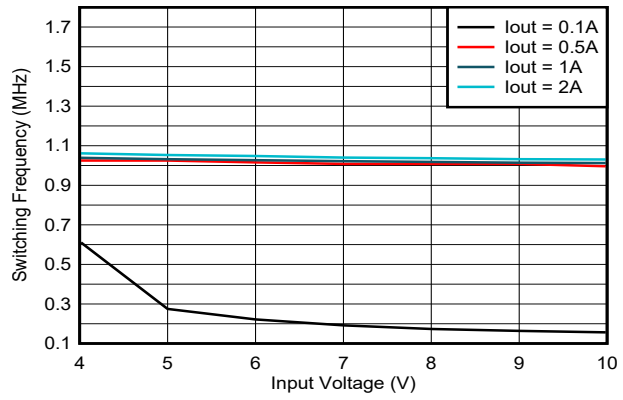

$V_{OUT}$ = 3.3 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-58. Efficiency vs Output Current**



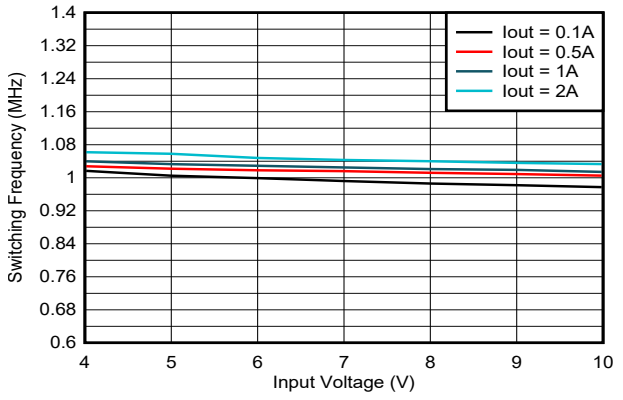

$V_{OUT}$ = 3.3 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-59. Efficiency vs Output Current**



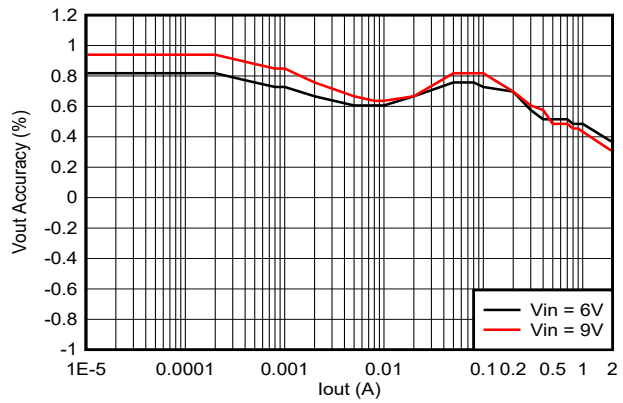

$V_{OUT}$ = 3.3 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

**Figure 9-60. Switching Frequency vs Input Voltage**



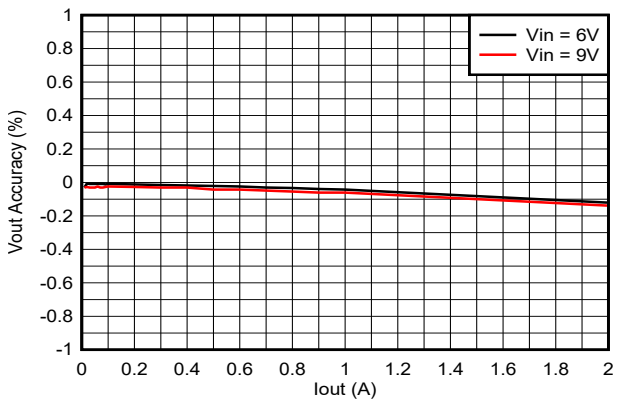

$V_{OUT}$ = 3.3 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

**Figure 9-61. Switching Frequency vs Input Voltage**




$V_{OUT}$ = 3.3 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Auto PFM/PWM

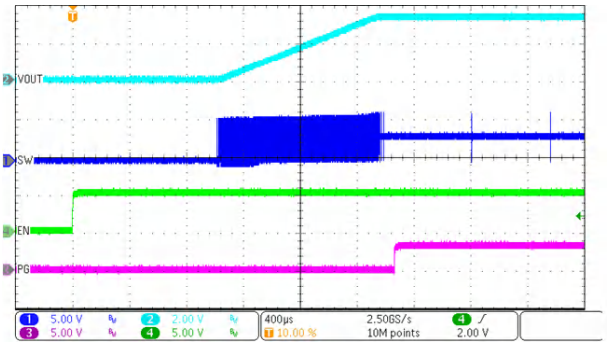
**Figure 9-62. Output Voltage vs Output Current**




$V_{OUT}$ = 3.3 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
Forced PWM

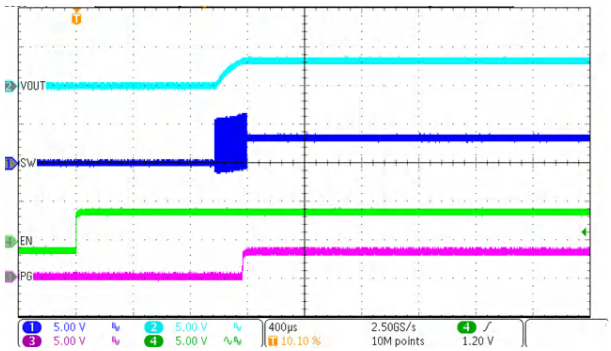
**Figure 9-63. Output Voltage vs Output Current**


Copyright © 2023 Texas Instruments Incorporated



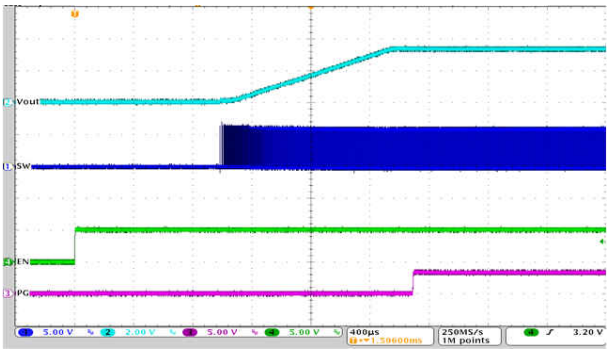

$V_{IN}$ = 6 V $C_{ss}$ = 3.3 nF $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 0 A Auto PFM/PWM

**Figure 9-64. Start-Up Timing**



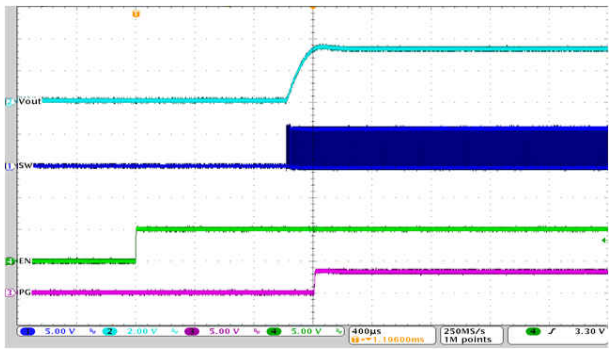

$V_{IN}$ = 6 V $C_{ss}$ = 0 nF $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 0 A Auto PFM/PWM

**Figure 9-65. Start-Up Timing**



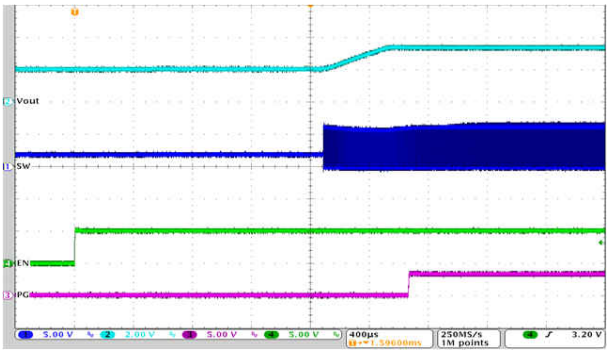

$V_{IN}$ = 6 V $C_{ss}$ = 3.3 nF $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 2 A FPWM

**Figure 9-66. Start-Up Timing**



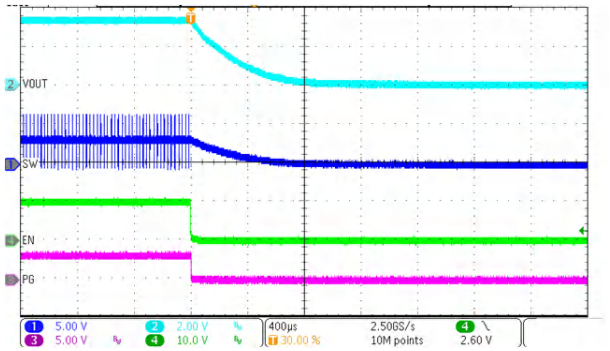

$V_{IN}$ = 6 V $C_{ss}$ = 0 nF $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 2 A FPWM

**Figure 9-67. Start-Up Timing**




$V_{IN}$ = 6 V $C_{ss}$ = 3.3 nF $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 0 A FPWM

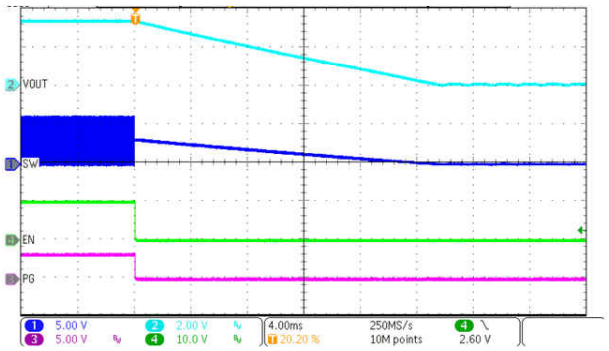
**Figure 9-68. Start-Up into Prebiased Output**




$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 10 mA Auto PFM/PWM

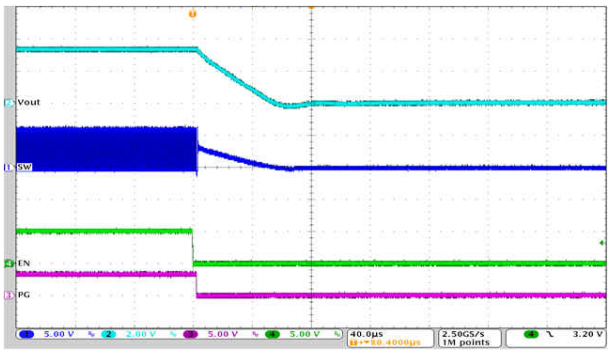
**Figure 9-69. Shutdown Timing with Output Discharge Enabled**

Copyright © 2023 Texas Instruments Incorporated



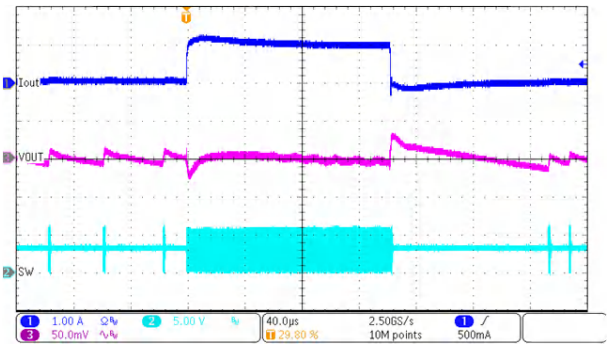

$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 10 mA Auto PFM/PWM

**Figure 9-70. Shutdown Timing with Output Discharge Disabled**



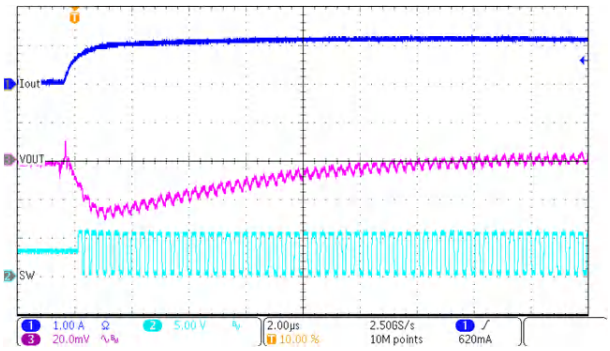

$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 2 A FPWM

**Figure 9-71. Shutdown Timing with Output Discharge Disabled**



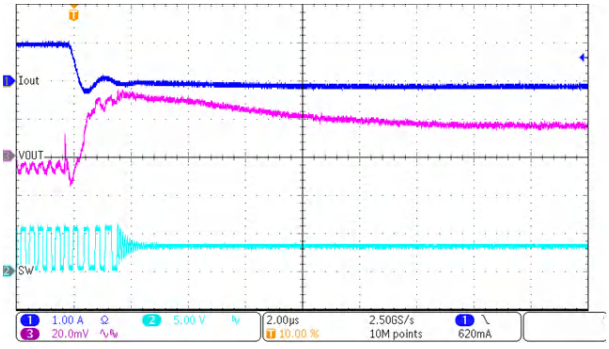

$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 10 mA to 1 A Auto PFM/PWM

**Figure 9-72. Load Transient Response**



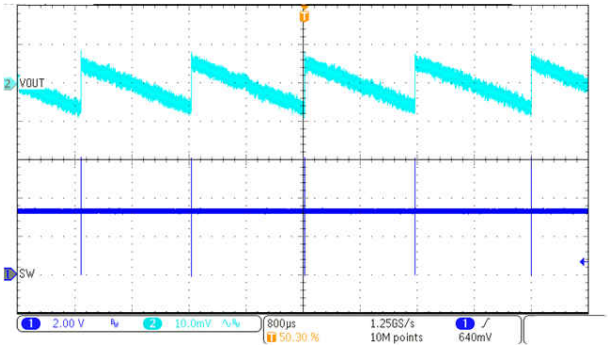

$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 10 mA to 1 A Auto PFM/PWM

**Figure 9-73. Load Transient Response Undershoot**




$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 1 A to 10 mA Auto PFM/PWM

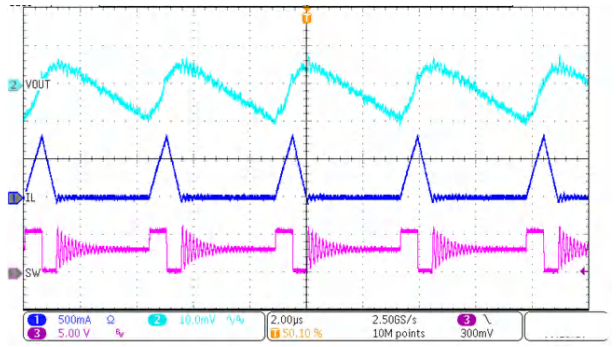
**Figure 9-74. Load Transient Response Overshoot**




$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 0 A Auto PFM/PWM

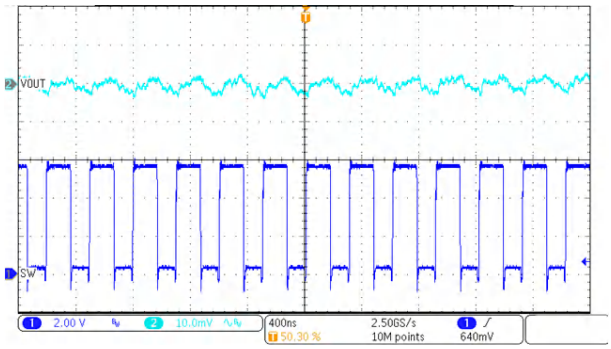
**Figure 9-75. Output Voltage Ripple**


Copyright © 2023 Texas Instruments Incorporated



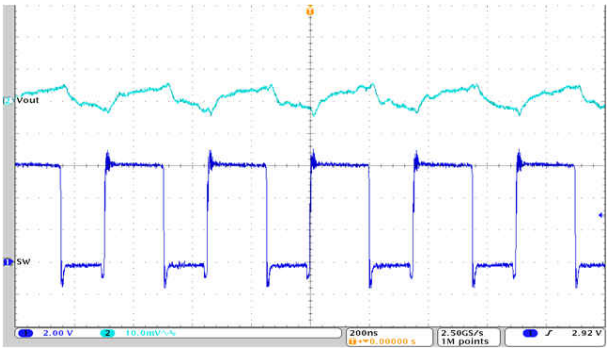

$V_{IN}$ = 6 V L = 2.2 µH $F_{sw}$ = 1.0 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 100 mA Auto PFM/PWM

**Figure 9-76. Output Voltage Ripple**



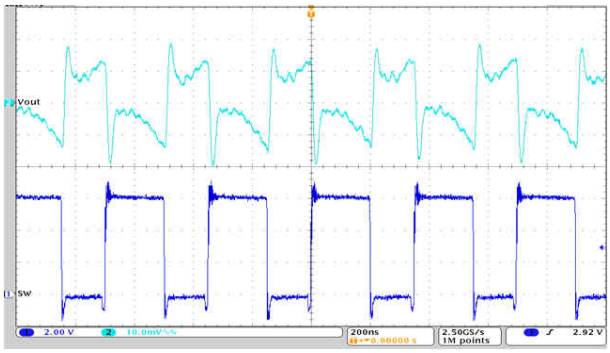

$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 1 A Auto PFM/PWM

**Figure 9-77. Output Voltage Ripple**



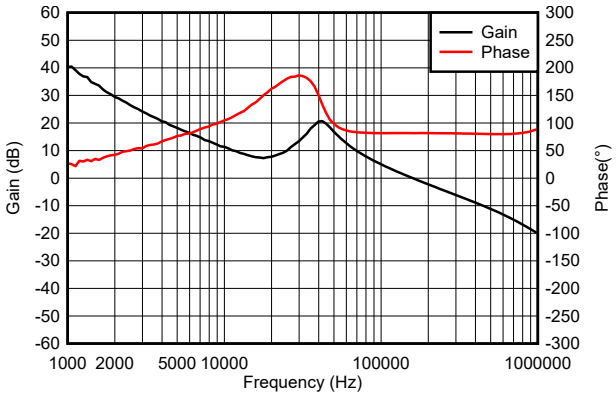

$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 2 A FPWM

**Figure 9-78. Output Voltage Ripple**




$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 2 A FPWM

**Figure 9-79. Input Voltage Ripple**




$V_{IN}$ = 6 V L = 1.0 µH $F_{sw}$ = 2.5 MHz
$V_{OUT}$ = 3.3 V $I_{OUT}$ = 2 A FPWM

**Figure 9-80. Bode Plot**

Copyright © 2023 Texas Instruments Incorporated

## 9.4 System Examples

### 9.4.1 LED Power Supply

The TPS62992-Q1 can be used as a power supply for power LEDs. The FB pin can be easily set to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor (R2) is reduced to avoid excessive power loss. Because the SS/TR pin provides 2.5 µA (typical), the feedback pin voltage can be adjusted by an external resistor per Equation 19. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62992-Q1. Figure 9-81 shows an application circuit, tested with analog dimming.

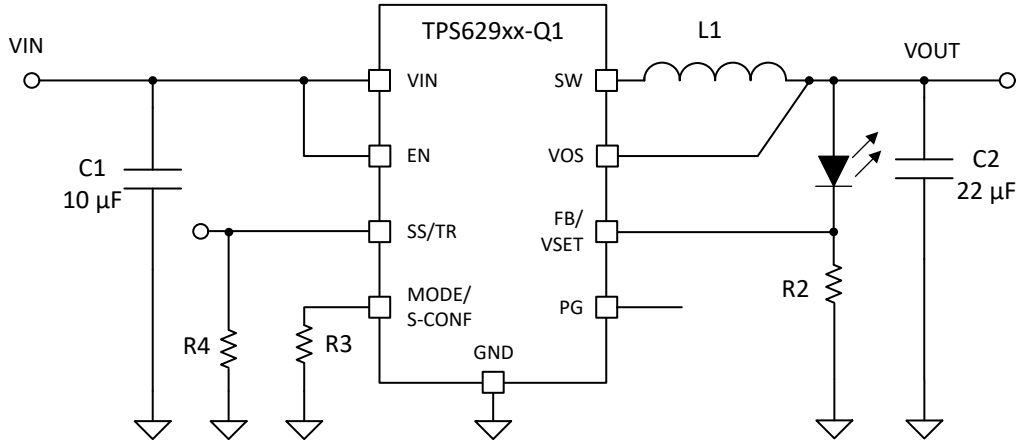



**Figure 9-81. Single Power LED Supply**

The resistor at SS/TR defines the FB voltage. The resistor at SS/TR is set to 304 mV by $R_{SS/TR}$ = R4 = 162 kΩ using Equation 19. This cuts the losses on R2 to half from the nominal 0.6 V of feedback voltage while it still provides good accuracy.

$$V_{FB} = 0.75 \times 2.5\mu A \times R_{SS/TR} \quad (19)$$

The device now supplies a constant current set by resistor R2 from FB/VSET to GND. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the *Step-Down LED Driver With Dimming With the TPS621-Family and TPS821-Family* application report.

### 9.4.2 Powering Multiple Loads

In applications where the TPS62992-Q1 is used to power multiple load circuits, the total capacitance on the output can be very large. To properly regulate the output voltage, there must be an appropriate AC signal level on the VOS pin. Tantalum capacitors have a large enough ESR to keep output voltage ripple sufficiently high on the VOS pin. With low-ESR ceramic capacitors, the output voltage ripple can get very low, so TI does not recommend to use a large capacitance directly on the output of the device. If there are several load circuits with their associated input capacitor on a PCB, these loads are typically distributed across the board. This adds enough trace resistance ($R_{trace}$) to keep a large enough AC signal on the VOS pin for proper regulation.

The minimum total trace resistance on the distributed load is 10 mΩ. The total capacitance n × CIN in the use case below was 32 × 47 µF of ceramic X7R capacitors.


Copyright © 2023 Texas Instruments Incorporated

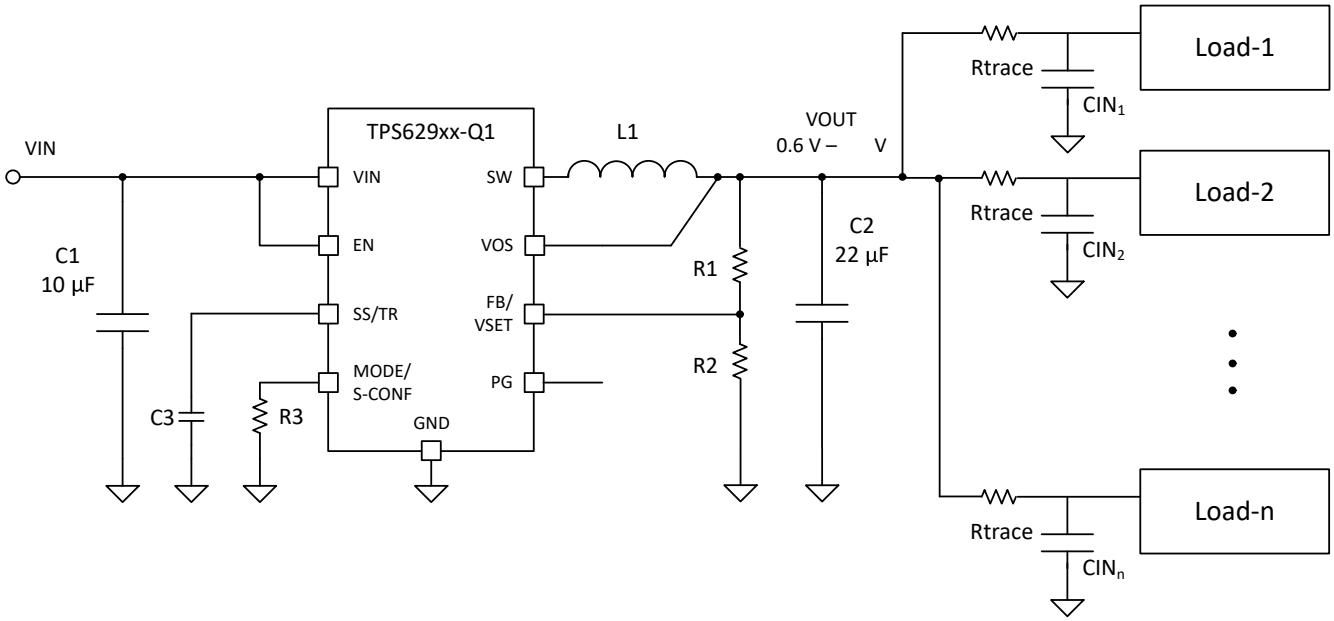



**Figure 9-82. Multiple Loads**

**Note**

Figure 9-82 shows an external feedback configuration, but the internal (VSET) configuration can also be used.

### 9.4.3 Voltage Tracking

Figure 9-83 shows how two TPS62992-Q1s can be configured to tracking output voltages. In this configuration, Device 2 follows the voltage applied to its SS/TR pin from Device 1 output. A ramp on the SS/TR pin of Device 2 to 0.8 V in turn ramps VOUT2 according to the 0.6-V reference on $V_{FB}$ and the R4//R5 resistor divider.

For this example, to track the 3.8 V (VOUT1) of Device 1 a resistor divider (R7//R8) on SS/TR of Device 2 is required to generate 0.8 V when the output voltage (VOUT1) is in regulation. Due to the $I_{SS}$ current of 2.5 µA from the SS/TR pin, the equivalent resistance of R7 // R8 must be kept below 15 kΩ to minimize any offset the $I_{SS}$ current can cause on the SS/TR pin voltage.

Copyright © 2023 Texas Instruments Incorporated

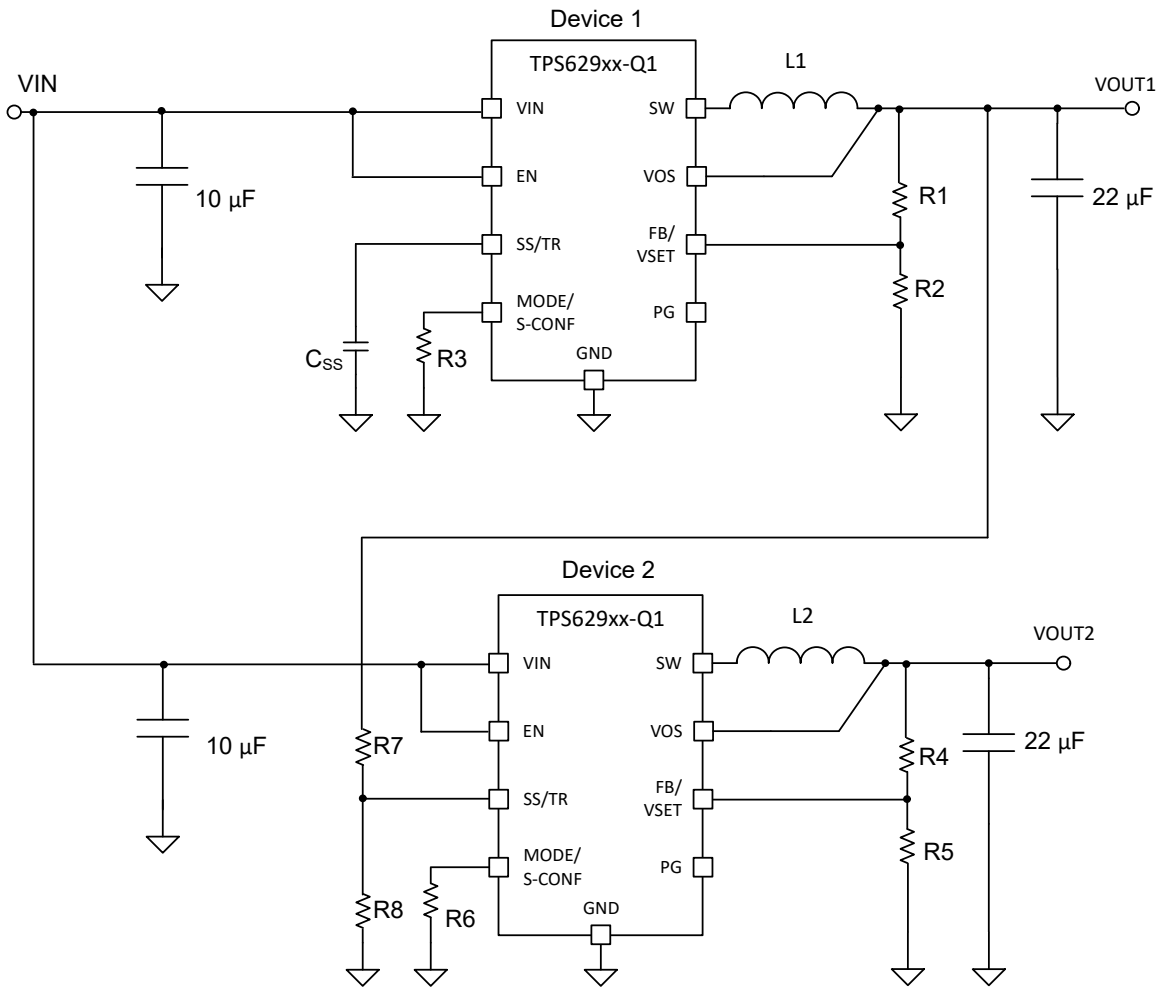



**Figure 9-83. Tracking Example**

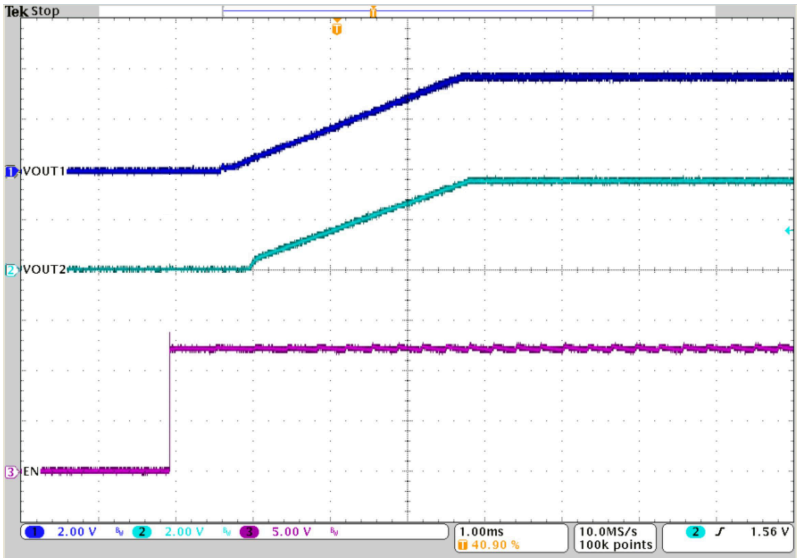



**Figure 9-84. Tracking**


Copyright © 2023 Texas Instruments Incorporated

### 9.4.4 Inverting Buck-Boost (IBB)

The need to generate negative voltage rails for electronic designs is a common challenge. The wide 3-V to 10-V input voltage range of the TPS62992-Q1 makes it ideal for an inverting buck-boost (IBB) circuit, where the output voltage is inverted or negative with respect to ground.

The circuit operation in the IBB topology differs from that in the traditional buck topology. Though the components are connected the same as with a traditional buck converter, the output voltage terminals are reversed. See Figure 9-85.

The maximum input voltage that can be applied to an IBB converter is less than the maximum voltage that can be applied to the TPS62992-Q1 in a typical buck configuration. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is $V_{IN}$ to $V_{OUT}$, and not $V_{IN}$ to ground. Thus, the input voltage range of the TPS62992-Q1 in an IBB configuration becomes 3 V to 10 V + $V_{OUT}$, where $V_{OUT}$ is a negative value.

The output voltage range is the same as when configured as a buck converter, but only negative. Thus, the output voltage for a TPS62992-Q1 in an IBB configuration can be set between –0.4 V and –5.5 V.

The maximum output current for the TPS62992-Q1 in an IBB topology is normally lower than a traditional buck configuration due to the average inductor current being higher in an IBB configuration. Traditionally, lower input or (more negative) output voltages results in a lower maximum output current. However, using a larger inductor value or the higher 2.5-MHz frequency setting can be used to recover some or all of this lost maximum current capability.

When implementing an IBB design, it is important to understand that the IC ground is tied to the negative voltage rail, and in turn, the electrical characteristics of the TPS62992-Q1 device are referenced to this rail. During power up, as there is no charge in the output capacitor and the IC GND pin (and $V_{OUT}$) are effectively 0 V, thus parameters such as the $V_{IN}$ UVLO and EN thresholds are the same as in a typical buck configuration. However, after the output voltage is in regulation, due to the negative voltage on the IC GND pin, the device traditionally continues to operate below what can appear to be the normal UVLO or EN falling thresholds relative to the system ground. Take care if the user is using the dynamic mode change feature on the MODE pin of the TPS62992-Q1 or driving the EN pin from an upstream microcontroller as the high and low thresholds are relative to the negative rail and not the system ground.

More information on using a DCS regulator in an IBB configuration can be found in the *Description Compensating the Current Mode Boost Control Loop*, *Using the TPS6215x in an Inverting Buck-Boost Topology*, and *Using the TPS629210 in an Inverting Buck-Boost Topology* application notes.

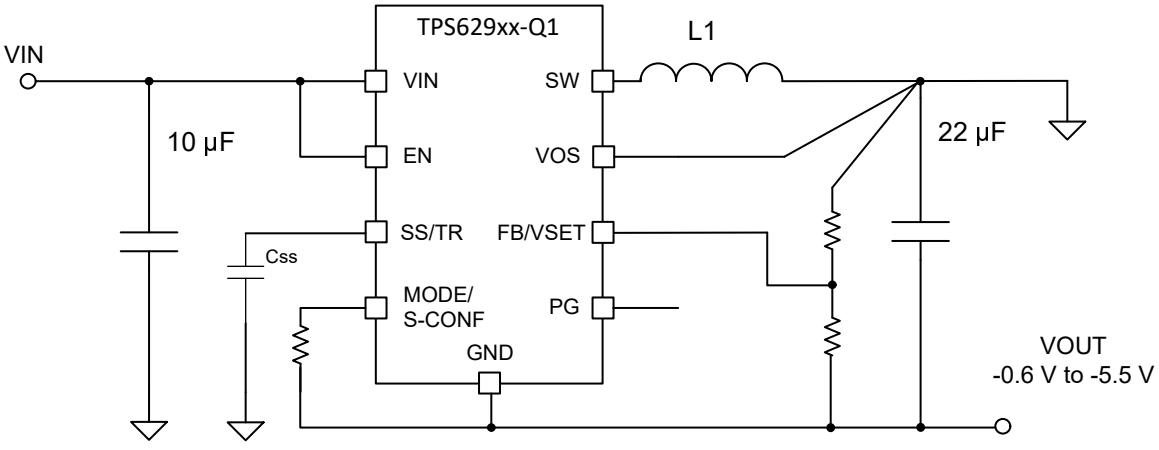



**Figure 9-85. IBB Example with Adjustable Feedback**

**Note**

Figure 9-85 shows an external feedback configuration, but the internal (VSET) configuration can also be used.

## 9.5 Power Supply Recommendations

The power supply to the TPS62992-Q1 must have a current rating according to the supply voltage, output voltage, and output current of the TPS62992-Q1. At a minimum, the input power supply must provide enough power to cover the maximum output power divided by the efficiency at maximum load. A good rule of thumb is to use a supply with an additional 50% of power capability to withstand the additional loading associated with power up, transient events, and potential overload events.

**Note**

For current limited input supplies with a variable supply voltage, the minimum supply voltage must be used to determine if the power supply is sufficient.

## 9.6 Layout

### 9.6.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore, the PCB layout of the TPS62992-Q1 demands careful attention to make sure the device works correctly and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

See Figure 9-86 for the recommended layout of the TPS62992-Q1, which is designed for common external ground connections. The input capacitor must be placed as close as possible between the VIN and GND pin of TPS62992-Q1. Also, connect the VOS pin in the shortest way to VOUT at the output capacitor.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths, conducting the switched load current must be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for traces with high dv/dt. Therefore, the input and output capacitance must be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces must be avoided. Loops that conduct an alternating current must outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example, SW). As they carry information about the output voltage, they must be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R1 and R2, must be kept close to the IC and connected directly to those pins and the system ground plane. The same applies to the VSET resistor if VSET is used to scale the output voltage.

The package uses the pins for power dissipation. Thermal vias on the VIN and GND pins help to spread the heat through the PCB.

In case any of the digital inputs EN and MODE/S-CONF must be tied to the input supply voltage at $V_{IN}$, the connection must be made directly at the input capacitor as indicated in the schematics.

The recommended layout is implemented on the EVM and shown in the *TPS6290x-Q1 Step-Down Converter Evaluation Module* user's guide.


Copyright © 2023 Texas Instruments Incorporated

### 9.6.2 Layout Example

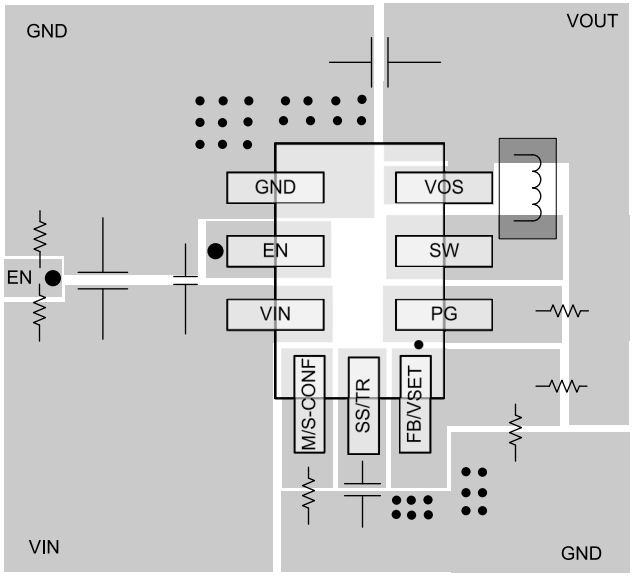



**Figure 9-86. Layout**

### 9.6.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design, for example, increasing copper thickness, thermal vias, number of layers
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics* application reports.

The TPS62992-Q1 is designed for a maximum operating junction temperature ($T_J$) of 165°C. Therefore, the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, TI recommends to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

The device is qualified for long term qualification with 165°C junction temperature. For more details about the derating and life time of the HotRod™ package, see the *Derating and Lifetime Calculations for FCOL Packages HotRod and FC-SOT* application note.

Copyright © 2023 Texas Instruments Incorporated

# 10 Device and Documentation Support

## 10.1 Device Support

### 10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 10.1.2 Development Support

#### *10.1.2.1 Custom Design With WEBENCH® Tools*

Click here to create a custom design using the TPS62992-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 10.2 Documentation Support

### 10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Derating and Lifetime Calculations for FCOL Packages HotRod and FC-SOT* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application report
- Texas Instruments, *TPS6290x-Q1 Step-Down Converter Evaluation Module* user's guide
- Texas Instruments, *Using the TPS629210 in an Inverting Buck-Boost Topology* application report
- Texas Instruments, *Description Compensating the Current Mode Boost Control Loop* application report

## 10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 10.5 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.


Copyright © 2023 Texas Instruments Incorporated

## 10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS62992QRYTRQ1 | Active | Production | VQFN-HR (RYT) \| 9 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 165 | TS92 |
| TPS62992QRYTRQ1.A | Active | Production | VQFN-HR (RYT) \| 9 | 3000 \| LARGE T&R | Yes | SN | Level-2-260C-1 YEAR | -40 to 165 | TS92 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

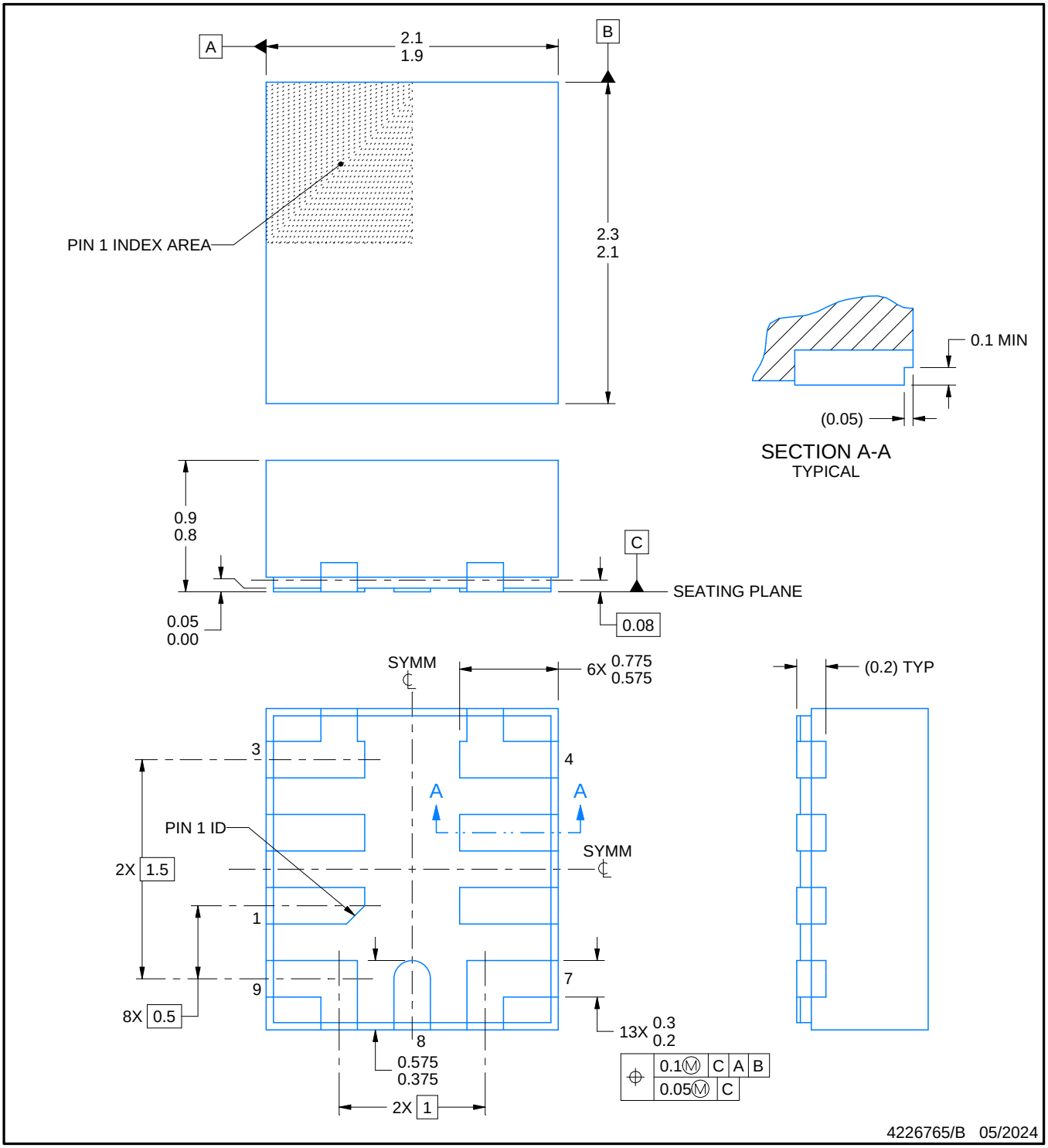
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE OUTLINE

## RYT0009A

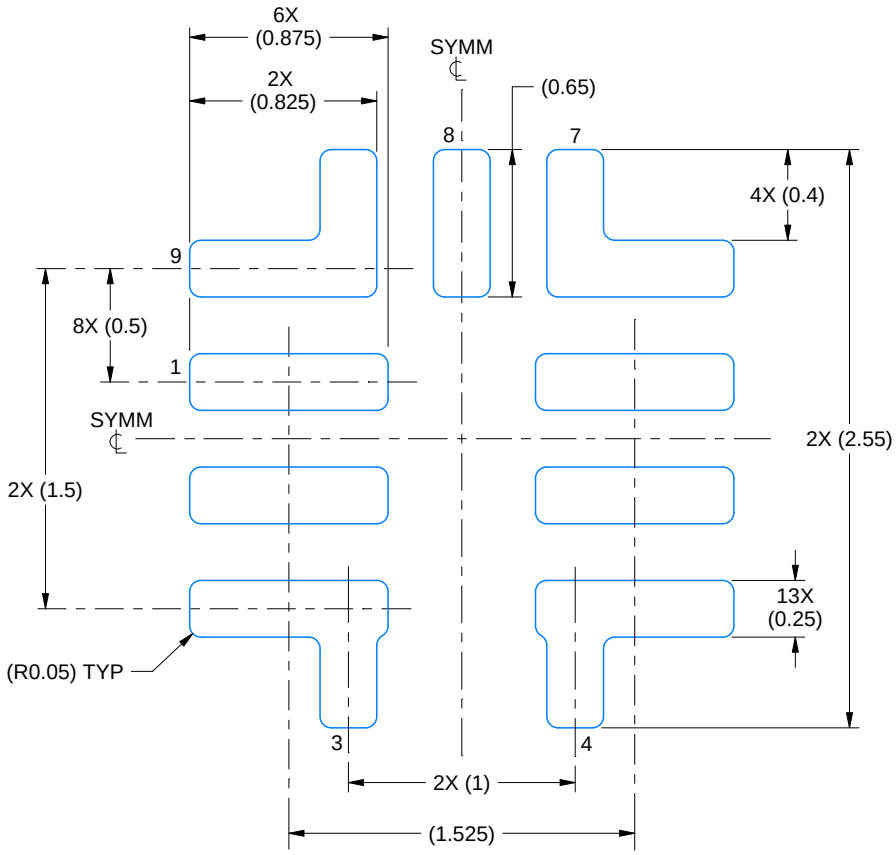
## VQFN-HR - 0.9 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

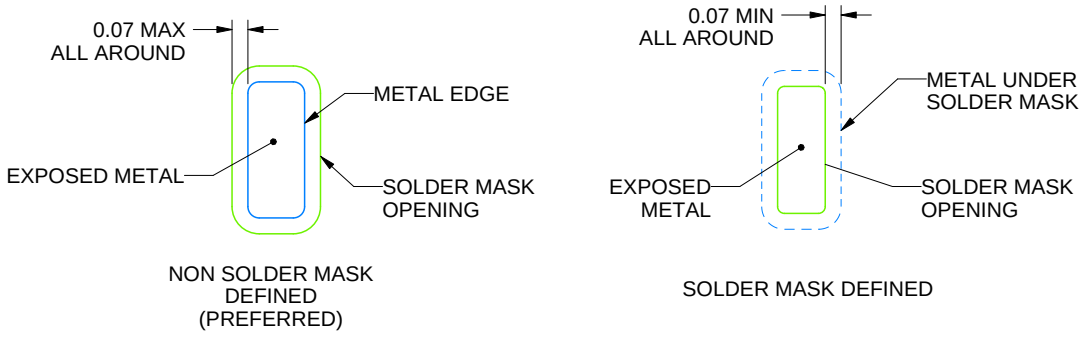



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X




NON SOLDER MASK
DEFINED
(PREFERRED)

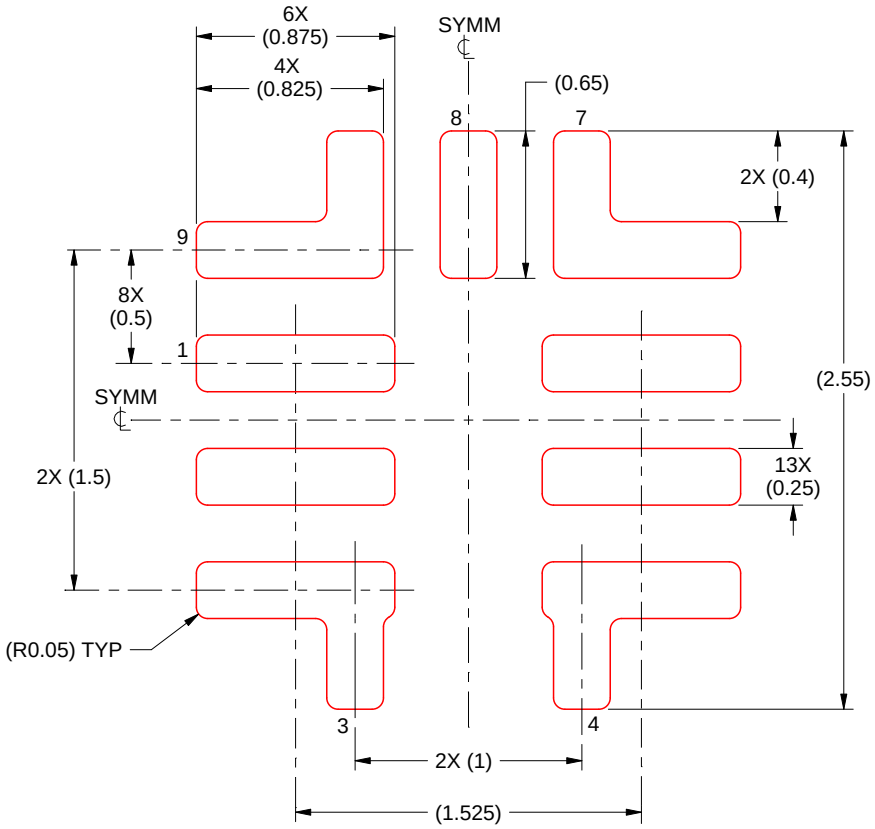
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4226765/B 05/2024

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4226765/B 05/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025