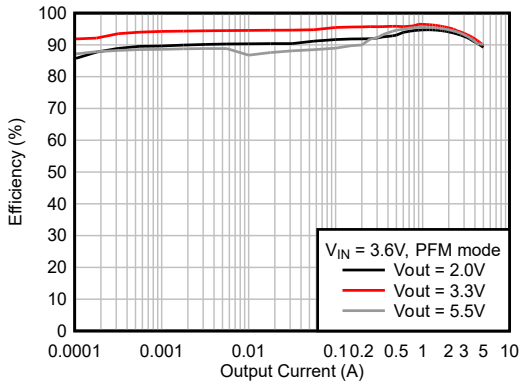
TPS63820 Low Quiescent Current, 4A Buck-Boost Converters With I²C Interface

1 Features

- Input voltage range: 1.8V to 5.5V
  - 2.0V minimum input voltage for start-up
- V_{OUT} range: I²C-configurable 1.2V to 5.5V with 25mV step
- Output current
  - Up to 3.5A for $V_{IN} \geq 2.5V$, $V_{OUT} = 3.3V$
  - Up to 4A for $V_{IN} \geq 3V$, $V_{OUT} = 3.3V$
- High efficiency over the entire load range
  - Low 2.3µA operating quiescent current
  - Automatic power save mode, ultra-sonic mode, and forced PWM mode
  - 91.94% efficiency at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 100µA$ (in buck-boost mode)
  - 95.33% efficiency at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 2A$ (in buck-boost mode)
- Supports 1.2V logic I/O
- Three I²C target addresses available by ADDR pin connection
- Programmable soft-start time, current limit, and buck-boost window
- Output discharge function
- Safety and robust protection features
  - Overtemperature protection
  - Input and output overvoltage protection
  - True load disconnect during shutdown
  - Forward and backward current limit
  - Hiccup protection
- Two device options:
  - TPS63820: preprogrammed 3.3V V_{OUT}
  - TPS638201: program V_{OUT} prior to start-up
- 15-ball WCSP package (2.0mm × 1.2mm)



Efficiency vs I_{OUT}

2 Applications

- System pre-regulator
- Point-of-load regulation
- Optical modules
- Broadband network radio or SoC supply

3 Description

The TPS63820 and TPS638201 are low quiescent current, high output current buck-boost converters fully programmable through I²C. The 2.3µA quiescent current and four low Rdson MOSFETs enable high efficiency from a light to a heavy load range.

Depending on the input voltage, the devices automatically operate in boost, buck, or in buck-boost mode when the input voltage is approximately equal to the output voltage. The transitions between modes occur at defined thresholds and avoid unwanted toggling within the modes which reduces output voltage ripple.

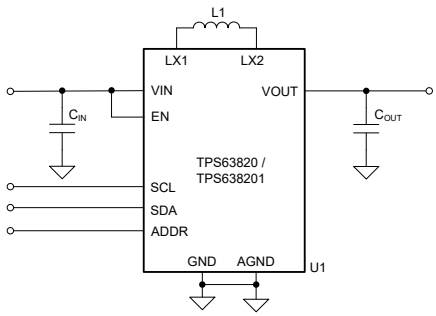
The devices have a fast dynamic response, which enables the regulation of output voltage tightly, even in the event of heavy load transients.

The devices offer a small design size in WCSP. The design size is < 20mm² with only four external components.

Device Information

PART NUMBER(3)	PACKAGE(1)	PACKAGE SIZE(2)
TPS63820	YBG (DSBGA, 15)	2.029mm × 1.257mm
TPS638201		

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.



Simplified Application

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4 Device Comparison Table

PART NUMBER	DEFAULT SETTING OF INTERNAL ENABLE	OUTPUT VOLTAGE
TPS63820YBGR	ENABLE = 1	3.3V
TPS638201YBGR	ENABLE = 0	Programmable at start-up

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5 Pin Configuration and Functions

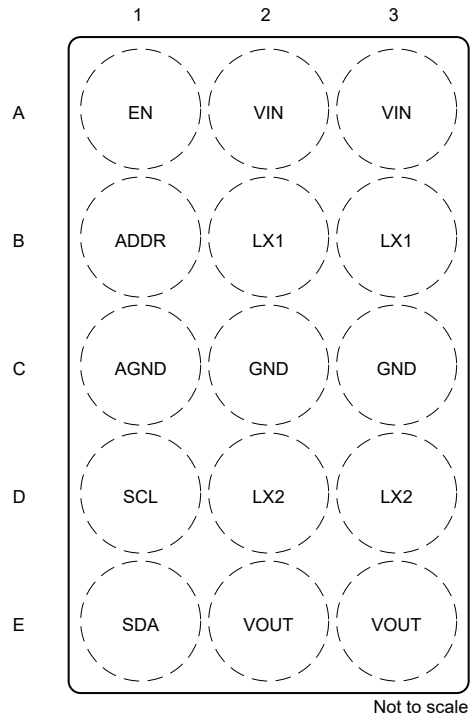

Figure 5-1. TPS63820 and TPS638201 YBG Package, 15-Ball DSBGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	EN	I	Device enable. A high logic level on this pin enables the device; a low logic level on this pin disables the device.
A2, A3	VIN	PWR	Supply voltage for power stage
B1	ADDR	I	I^2C target address selection pin. ADDR = Logic low, I^2C target address is 0x75 ADDR = Logic high, I^2C target address is 0x76 ADDR = floating, I^2C target address is 0x77
B2, B3	LX1	PWR	Inductor connection
C1	AGND	—	Analog ground
C2, C3	GND	PWR	Power ground
D1	SCL	I/O	I^2C serial interface clock. Pull this pin up to the I^2C bus voltage with a resistor.
D2, D3	LX2	PWR	Inductor connection
E1	SDA	I/O	I^2C serial interface data. Pull this pin up to the I^2C bus voltage with a resistor.
E2, E3	VOUT	PWR	Converter output

(1) I = input, O = output, PWR = power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, SCL, SDA, EN, ADDR)[2]	–0.3	6	V
V_I	Input voltage for less than 10 ns (LX1, LX2)[2]	-0.7	8	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 [2]	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.8		5.5	V
V_O	Output voltage		1.2		5.5	V
I_O	Output current[2]	V_{OUT} = 3.3V, V_{IN} ≥ 2.6V			3.5	A
C_I	Input capacitance[1]		5			µF
C_O	Output capacitance[1]	V_{OUT} = 3.3V, V_{IN} ≥ 2.6V, I_{OUT} ≤ 2A	14	16		µF
L	Inductance		390	470	560	nH
T_A	Operating free-air temperature range		–40		85	°C
T_J	Operating junction temperature range		–40		125	°C

(1) Effective capacitance after DC bias effects have been considered.
(2) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.

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6.4 Thermal Information

THERMAL METRIC[1]		TPS63820 YBG (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

T_J = -40℃ to 125℃, V_{IN} = 2.0V to 5.5V. Typical values are at V_{IN} = 3.6V, V_{OUT} = 3.3V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			1.8		5.5	V
V_{IT+}	Positive-going UVLO threshold voltage			1.8	1.9	2.0	V
V_{IT-}	Negative-going UVLO threshold			1.6	1.7	1.8	V
V_{HYS}	Hysteresis voltage				200		mV
I_Q	Quiescent current into VIN		V_{IN} = 3.6V, V_{OUT} = 3.3V, V_{EN} = 3.6V, non-switching, ENABLE bit = 1, T_J = –40°C to 85°C		2.3	4	µA
I_Q	Quiescent current into VOUT		V_{IN} = 3.6V, V_{OUT} = 3.3V, V_{EN} = 3.6V, non-switching, ENABLE bit = 1, T_J = –40°C to 85°C		0.3	1	µA
I_{SD}	Shutdown current into VIN		V_{IN} = 3.6V, V_{OUT} = 0V, V_{EN} = 0V T_J = –40°C to 85°C		0.3	2.5	µA
I/O SIGNALS							
V_{IT+}	Positive-going input threshold voltage	SCL, SDA, ADDR, EN				0.82	V
V_{IT-}	Negative-going input threshold voltage	SCL, SDA, ADDR, EN		0.33			V
V_{IM}	Mid-level input voltage	ADDR			0.6		V
V_{OL}	Low-level output voltage	SDA				0.36	V
I_{IH}	High-level input current	SCL, SDA, ADDR	V_{SCL} = V_{SDA} = V_{ADDR} = 1.2V, no pullup resistor		0.01	0.1	µA
I_{IL}	Low-level input current	SCL, SDA, ADDR	V_{SCL} = V_{SDA} = V_{ADDR} = 0V, no pullup resistor		0.01	0.1	µA
I_{IB}	Input bias current	EN	V_{EN} = 0V to 5.5V		2.5	30	nA
R_{EN}	EN pin pulldown resistor		EN = low		800		kΩ
POWER STAGE							
V_O	Output voltage range			1.2		5.5	V
	Output voltage accuracy		PWM operation, 2V ≤ V_{OUT} < 3V	–1.2		1	%
			PWM operation, 3V≤ V_{OUT} < 4V	-1		1	%
			PWM operation, V_{OUT} ≥ 4V	-1.2		1	%
	PFM valley - DC offset		PFM operation	0.7	1.5	2.5	%
	Valley switching current limit		CURRENT_LIMIT = 00b	5.7	6.5	7	A
	Reverse valley switching current limit			-4.0	-3.3	-2	A
	Hysteresis current		HYS_CURRENT = 00b		800		mA

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6.5 Electrical Characteristics (continued)

T_J = -40℃ to 125℃, V_{IN} = 2.0V to 5.5V. Typical values are at V_{IN} = 3.6V, V_{OUT} = 3.3V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Buck side $R_{DS(on)}$	High-side MOSFET on resistance on buck side			11.6		mΩ
	Low-side MOSFET on resistance on buck side			15.5		
Boost side $R_{DS(on)}$	High-side MOSFET on resistance on boost side			11.6		
	Low-side MOSFET on resistance on boost side			15.3		
I_{lkg}	Leakage current into VIN to LX1	EN = GND, V_{IN}=5.5V, V_{LX1}=0V, T_J = –40°C to 85°C		0.03	4	µA
I_{lkg}	Leakage current into VOUT to LX2	EN = GND, V_{OUT}=5.5V, V_{LX2}=0V, T_J = –40°C to 85°C		0.03	4	µA
I_{lkg}	Leakage current into LX1 to GND	EN = GND, V_{LX1}=5.5V, T_J = –40°C to 85°C		0.02	4	µA
I_{lkg}	Leakage current into LX2 to GND	EN = GND, V_{LX2}=5.5V, T_J = –40°C to 85°C		0.02	4	µA
I_{DISCHG}	Output discharge current	V_{IN} = 3.0V		160		mA
TIMING PARAMETER						
t_{SS}	Soft-start time	SS_RAMP[2:0] = 00b	0.2	0.3	0.4	mS
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of output voltage ramp			200		µS
	Switching frequency at Ultra-sonic mode		24			kHz
SR	Slew rate of internal ramp during dynamic voltage scaling	SLEW = 00b		±1		V/ms
		SLEW = 01b		±5		
		SLEW = 10b		±10		
		SLEW = 11b		±25		
PROTECTION						
$V_{T+(IVP)}$	Input OVP threshold voltage		5.65	5.75	5.95	V
	Input OVP hysteresis			100		mV
$V_{T+(OVP)}$	Output OVP threshold voltage		5.65	5.75	5.95	V
	Output OVP hysteresis			100		mV
$V_{PG_TH_rising}$	Power good threshold for rising			95		%
$V_{PG_TH_falling}$	Power good threshold for falling			90		%
	hiccup on time			2		mS
	hiccup off time			74		mS
	Thermal shutdown threshold temperature	T_J rising		165		°C
	Thermal shutdown hysteresis			20		°C

6.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	LOW period of the SCL clock	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	HIGH period of the SCL clock	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			

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6.6 Timing Requirements (continued)

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BUF}	Bus free time between a STOP and a START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;STA}$	Hold time (repeated) START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
$t_{HD;DAT}$	Data hold time	Standard mode	0			µs
		Fast mode	0			
		Fast mode plus	0			
t_r	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t_f	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	$20 \times V_{DD}/5.5$		300	
		Fast mode plus	$20 \times V_{DD}/5.5$		120	
$t_{su;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{VD;DAT}$	Data valid time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	
$t_{VD;ACK}$	Data valid acknowledge time	Standard mode			3.45	µs
		Fast mode			0.9	
		Fast mode plus			0.45	
C_b	Capacitive load for each bus line	Standard mode			400	
		Fast mode			400	
		Fast mode plus			550	
$t_{w(VSEL)}$	VSEL pulse duration	VSEL = high or low	5			µs

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6.7 Typical Characteristics

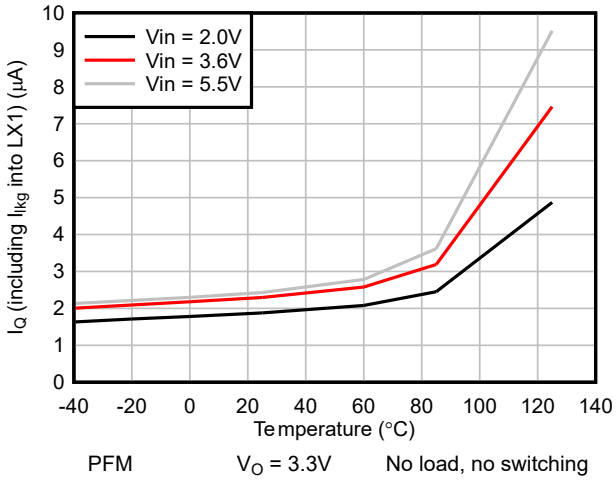


Figure 6-1. I_Q (Including Leakage Into LX1) Versus Temperature

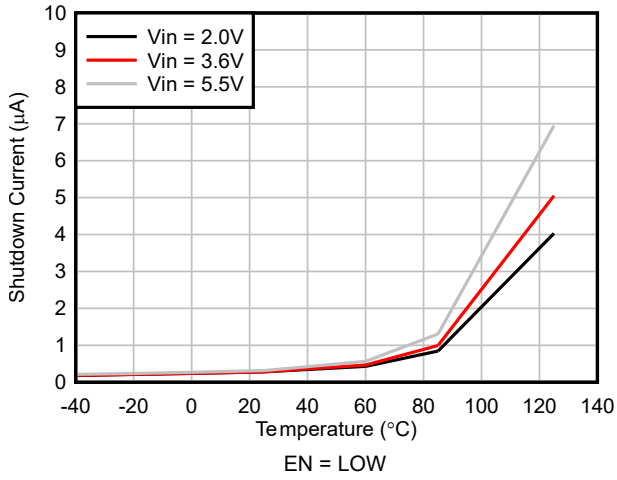


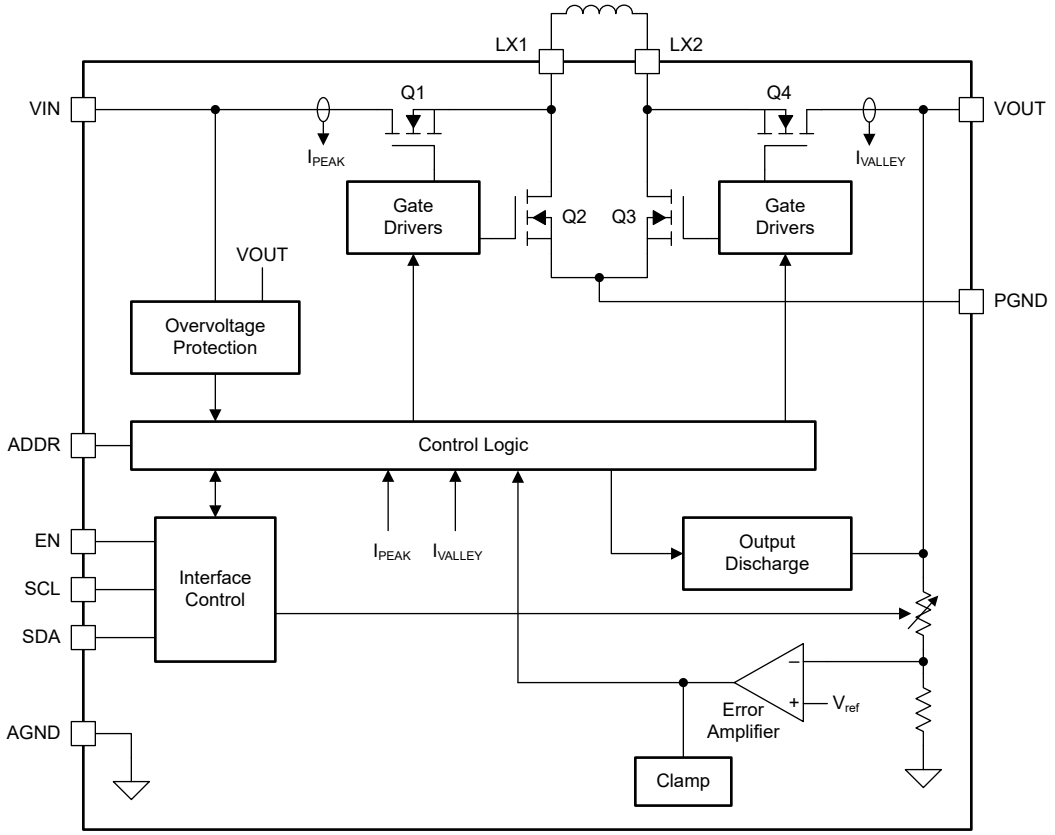
Figure 6-2. Shutdown Current Versus Temperature

7 Detailed Description

7.1 Overview

The TPS63820 and TPS638201 devices are low quiescent current, high-efficiency buck-boost converters. Four switches are integrated to maintain synchronous power conversion under all operating conditions, so that the device achieves high efficiency power conversion over a wide range of input voltages and output currents. The device automatically switches between buck, boost, and buck-boost operation as required by the operating conditions. The device operates as a true buck converter when $V_I > V_O$ and as a true boost converter when $V_I < V_O$. When $V_I \approx V_O$, the device operates in a 3-cycle buck-boost mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Scheme

The device automatically selects the best switching scheme for the operating conditions. To make sure of stable operation, the selection logic includes hysteresis (see Figure 7-1).

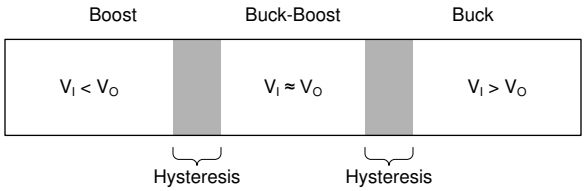


Figure 7-1. Switching Scheme Selection

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7.3.1.1 Buck Operation

When $V_I > V_O$, the device switches like a buck converter:

- Q1 is the switch.
- Q2 is the rectifier.
- Q3 is permanently off.
- Q4 is permanently on.

See Figure 7-2. During buck operation, one switching cycle comprises two phases: on–off.

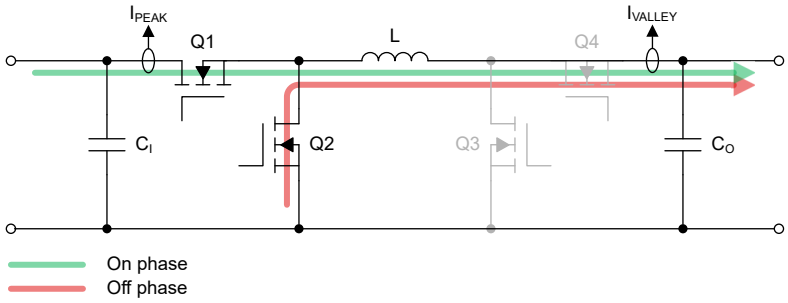

Figure 7-2. Buck Switch Configuration

7.3.1.2 Boost Operation

When $V_I < V_O$, the device switches like a boost converter:

- Q1 is permanently on.
- Q2 is permanently off.
- Q3 is the switch.
- Q4 is the rectifier.

See Figure 7-3. During boost operation, one switching cycle comprises two phases: on–off.

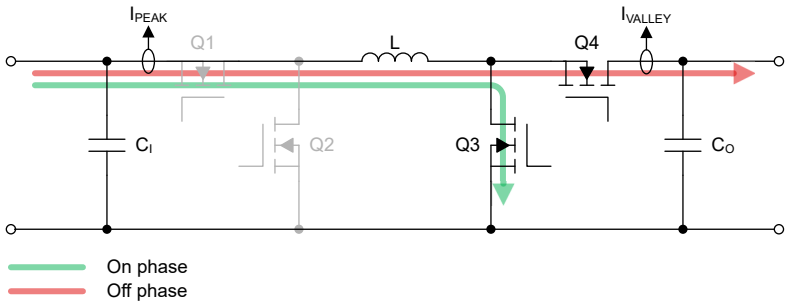

Figure 7-3. Boost Switch Configuration

7.3.1.3 Buck-Boost Operation

When $V_I \approx V_O$, all four transistors switch continuously (see Figure 7-4). During buck-boost operation, one switching cycle comprises three phases: on–commutate–off.

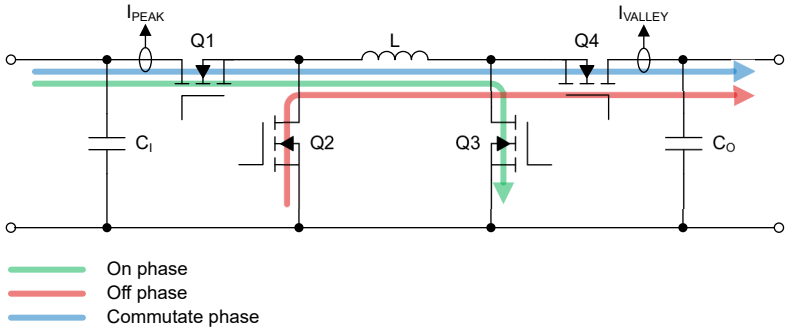

Figure 7-4. Buck-Boost Switch Configuration

7.3.2 PFM Operation

To increase efficiency across a wide range of operating conditions, the device automatically changes from pulse-width modulation (PWM) at medium and high output currents to pulse-frequency modulation (PFM) at low output currents.

- During PWM operation, the device switches continuously and adjusts the duty cycle of each switching cycle to regulate the output voltage.
- During PFM operation, the device switches with a single pulse, separated by periods when the device does not switch. PFM operation increases efficiency at low output currents because when the device does not switch, there are no switching losses and most of the internal circuitry is disabled, which reduces quiescent power consumption. A comparator compares the output voltage of the error amplifier to a predefined PFM threshold voltage.

To enable power-save mode, clear the FPWM bit in the Control register to 0.

Table 7-1. Forced-PWM versus Power-Save Mode Performance Comparison

PERFORMANCE PARAMETER	BEST OPERATING MODE
Low-power efficiency	PFM
Medium- and high-power efficiency	No difference
DC Output voltage accuracy	Forced-PWM
Transient response	Forced-PWM
Output voltage ripple	Forced-PWM

7.3.3 Ultra-sonic Mode Operation

During PFM operation, the time between switching changes with the operating conditions. Because the ceramic capacitors typically used with the device are piezoelectric, certain operating conditions can cause audible noise. The device has an ultra-sonic mode feature that forces the frequency of the switching to be outside the audible range. To enable ultra-sonic mode operation, set the ULTRA_SONIC bit in the CONTROL register to 1. Note that the power conversion efficiency of the device can be slightly reduced when the ultra-sonic mode is enabled at light load.

7.3.4 Forced-PWM Operation (FPWM)

During forced-PWM operation, the device uses PWM for all operating conditions. Forced-PWM operation has lower output voltage ripple and better transient response than power-save mode operation, but lower efficiency at low output currents (see Table 7-1).

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Note that the device inhibits forced-PWM operation during start-up (that is, until the converter output has reached power-good for the first time).

To enable forced-PWM operation, set the FPWM bit in the Control register to 1.

7.3.5 Ramp-PWM Operation (RPWM)

If Ramp-PWM operation is enabled, the device operates in forced-PWM when the device ramps from one output voltage to another during dynamic voltage scaling. This function is useful when the device operates in power-save mode, but make sure that dynamic voltage scaling ramps the output voltage up and down in a controlled way. If the device operates in power-save mode and Ramp-PWM is disabled, the device cannot always control the ramp from a higher output voltage to a lower output voltage, because in power-save mode the device cannot sink current (see Figure 7-5).

To enable Ramp-PWM operation, set the RAMP bit in the Control register to 1. To disable Ramp-PWM operation, clear the RAMP bit in the Control register to 0.

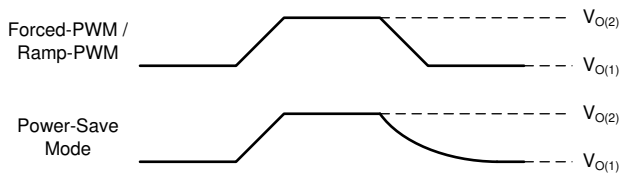

Figure 7-5. Ramp-PWM Operation

7.3.6 Device Enable (EN)

The EN pin enables and disables the device.

- When the EN pin is high, the device is enabled.
- When the EN pin is low, the device is disabled.

The ENABLE bit in the Control register enables and disables the output of the converter (see the *Section 8*).

Table 7-2. Device Enable Truth Table

ENABLE PIN (EN)	ENABLE BIT	DEVICE STATE	OUTPUT STATE
0	X	Device in Shutdown	Output Disabled
1	0	Programming Interface Active	Output Disabled
1	1	Device Active	Output Enabled

7.3.7 Undervoltage Lockout (UVLO)

The input voltage of the VIN pin is continuously monitored if the device is not in shutdown mode. UVLO only stops or starts the converter operation. UVLO avoids a brownout of the device during device operation. In case the supply voltage on the VIN pin is lower than the negative-going threshold of UVLO, the converter stops the operation. If the supply voltage on the VIN pin recovers to be higher than the UVLO rising threshold, the converter returns to operation.

7.3.8 Soft Start

When the input voltage is above the UVLO threshold and the EN pin is pulled above 0.82V, the device is enabled. Once device detects ENABLE bit value = 1, the soft-start begins.

To minimize inrush current and output voltage overshoot during start-up, the device has a soft-start function. The soft-start time can be configured by SS_RAMP bits in CONTROL2 register. The shortest soft-start time is 300us and longest soft-start time is 7.5ms.

When the output voltage is below 1.2V, the device switching current limit is clamped to 3A.

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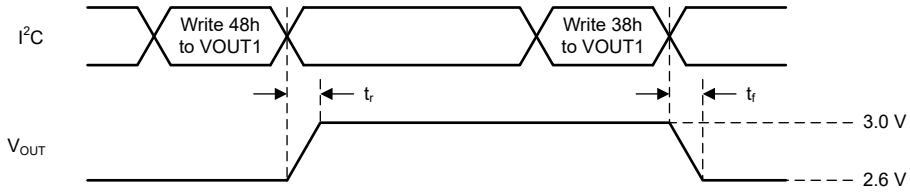
7.3.9 Dynamic Voltage Scaling

The device has a dynamic voltage scaling (DVS) function that changes the output voltage in a controlled way during operation. Figure 7-6 shows the timing diagram when the I²C interface is used to change the output voltage value in one of the VOUT registers. The ramp control block detects when the target output voltage is different from the actual output voltage and ramps the output voltage to the target voltage in 25mV steps. Use the 2-bit SLEW parameter in the Control register to select one of four slew rates from 1V/ms to 25V/ms.



$$t_r = t_f = \frac{|3.0 - 2.6|}{SR}$$

Where SR is the slew rate set by the SLEW bits in the CONTROL register.

Figure 7-6. DVS Timing Using the I²C Interface

7.3.10 Protection Functions

7.3.10.1 Input Voltage Protection (IVP)

Under certain operating conditions, current can flow from the output of the device to the input. For example, this kind of current flow from the output to the input can occur during dynamic voltage scaling when the output ramps down to a lower voltage and the VOUT pin sinks current from the output capacitor. Under such conditions, if the voltage source supplying the device cannot sink current, the voltage on the VIN pin can rise uncontrollably.

To make sure the input voltage stays within the permitted range, the device stops switching if the voltage on the VIN pin is greater than 5.75V. The device automatically starts to switch again when the voltage on the VIN pin is less than 5.65V.

The device sets the VIN_OVP bit in the Status register when an input overvoltage event occurs. The device clears the VIN_OVP bit when the input overvoltage condition no longer exists.

7.3.10.2 Output Voltage Protection (OVP)

The devices have the output overvoltage protection which avoids any damage to the device. When the output voltage threshold 5.75V is reached on the VOUT pin, the protection disables the converter power stage and makes the switching nodes high impedance. The device automatically starts to switch again when the voltage on the VOUT pin is less than 5.65V. The device sets the VOUT_OVP bit in the Status register when an output overvoltage event occurs. The device clears the VOUT_OVP bit when the output overvoltage condition no longer exists.

7.3.10.3 Current Limit Mode and Overcurrent Protection

The device has a clamp circuit which limits the switch current in the event of an overload. The device sets the OC bit in the Status register when current limit event occurs. The device clears the OC bit when the overcurrent event no longer exists.

Overloads increase the power dissipation in the device, which increases the temperature. If the device becomes too hot, the thermal shutdown function turns off the converter. When the device cools down, the thermal shutdown function automatically turns on the converter again. Thus, under a permanent overload condition, the device can periodically turn on and off, as it cools down and then heats up.

7.3.10.4 Output Short-Circuit Protection (Hiccup)

The device implements the output short-circuit protection by entering hiccup mode. After soft start-up time, the device monitors the output voltage. Whenever the output short circuit happens, causing the output voltage below 1.2V and switch current limit is triggered for 2ms, the device shuts down the switching for 74ms (typical) and

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then repeats the soft start. The hiccup mode helps reduce the total power dissipation on the device in the output short-circuit or overcurrent condition. The device sets the SC bit in the Status register when output short-circuit event occurs.

7.3.10.5 Thermal Shutdown

The device has a thermal shutdown function which turns off the converter if the junction temperature is greater than 165°C. The device automatically turns on the converter again when the junction temperature is less than 145°C. Use the I^2C interface to read and write to the registers when the device is in an overtemperature condition.

When the device detects an overtemperature condition, the device sets the TSD bit in the Status register to 1. The device clears the TSD bit to 0 when the overtemperature event no longer exists.

7.3.11 Power Good

The device has a power-good function which indicates if the output of the DC/DC converter is in regulation or not. The device detects a power-good condition when the output voltage is greater than 95% of the nominal value and detects a power-not-good condition when the output voltage is less than 90% of the nominal value.

When a power-not-good condition occurs, the device sets the $\overline{PG}$ bit in the Status register to 1. The device clears the $\overline{PG}$ bit to 0 when a power-good condition exists.

7.3.12 Load Disconnect

During device shutdown, the input is disconnected from the output. This disconnection between the output and the input prevents any current flow from the output to the input or from the input to the output.

7.3.13 Output Discharge

The TPS63820 and TPS638201 provide an active pull down current to quickly discharge output when the EN pin is logic low or the ENABLE bit is set to 0 when EN_DISCHG bit is 1. The output discharge function makes the power on and off sequencing smooth. Pay attention to the output discharge function if use this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground.

The output discharge function is controlled by the bit named EN_DISCHG.

When EN_DISCHG is set to 1, the TPS63820 and TPS638201 also provide discharge current when VIN UVLO falling threshold is triggered. The discharge circuit works until VIN falls to around 1V.

7.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

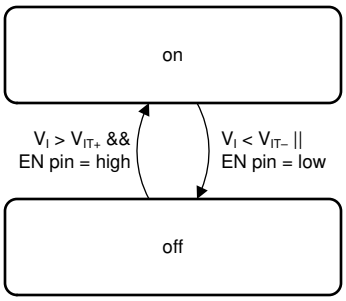

Figure 7-7. Device Functional Modes

7.5 Programming

7.5.1 Serial Interface Description

I²C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see *NXP Semiconductors, UM10204 – I²C-Bus Specification and User Manual*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C-compatible devices connect to the I²C bus through open-drain I/O pins, SDA, and SCL. A controller device, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A target device receives and transmits data on the bus under control of the controller device.

The device works as a target and supports the following data transfer modes, as defined in the I²C-Bus specification:

- Standard-mode (100Kbps)
- Fast-mode (400Kbps)
- Fast-mode Plus (1Mbps)

The interface adds flexibility to the power supply application, enabling most functions to be programmed to new values, depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above $V_{IT+(POR)}$.

The data transfer protocol for standard and fast modes is exactly the same, therefore, the data transfer protocol is referred to as F/S-mode in this document. The device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

To make sure that the I²C function in the device is correctly reset, Ti recommends that the I²C controller initiates a STOP condition on the I²C bus after the initial power up of SDA and SCL pullup voltages.

7.5.2 Standard-, Fast-, and Fast-Mode Plus Protocol

The controller initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 7-8. All I²C-compatible devices recognize a start condition.

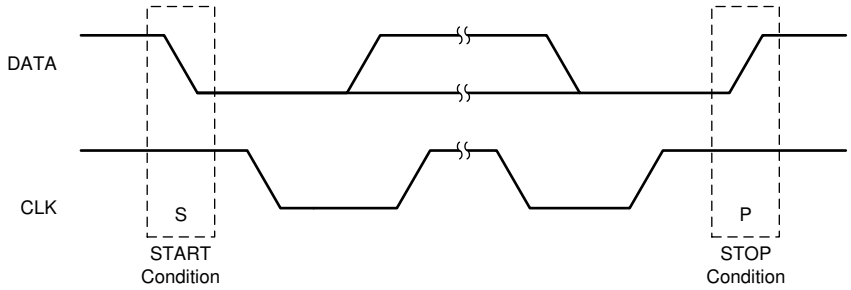

Figure 7-8. START and STOP Conditions

The controller then generates the SCL pulses and transmits the 7-bit address and the read/write direction bit, R/W, on the SDA line. During all transmissions, the controller validates the data. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 7-9). All devices recognize the address sent by the controller and compare to the internal fixed addresses. Only the target device with a matching address generates an acknowledge (see Figure 7-10) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that communication link with a target has been established.

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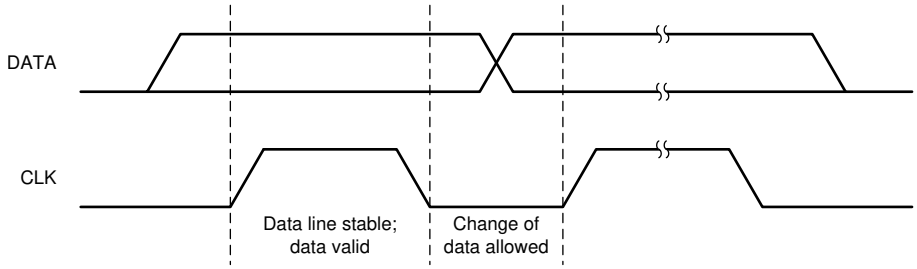

Figure 7-9. Bit Transfer on the Serial Interface

The controller generates further SCL cycles to either transmit data to the target (R/W bit 1) or receive data from the target (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 7-8). This low level to high level transition on the SDA line when the SCL is at high releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released and the devices wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section results in 00h being read out.

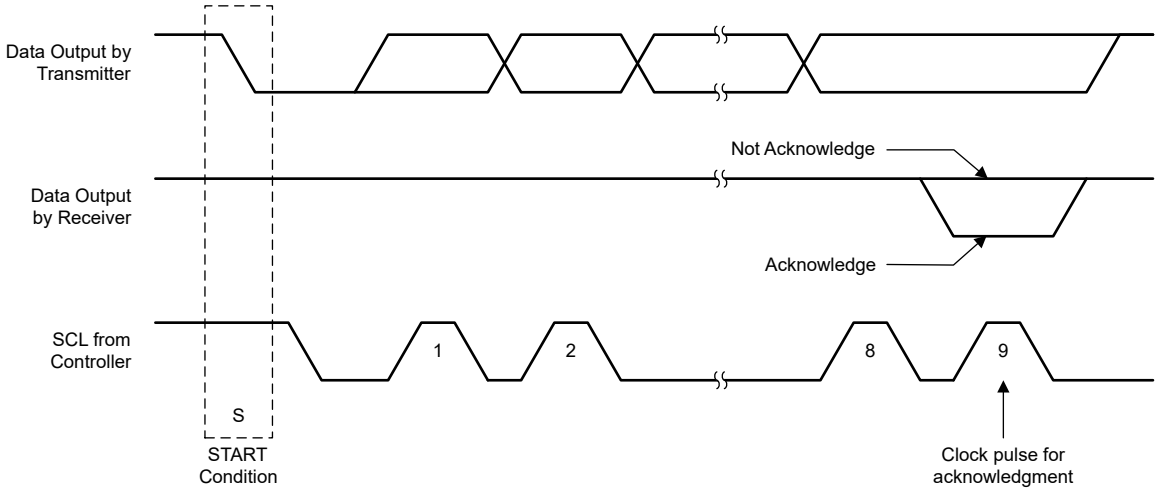

Figure 7-10. Acknowledge on the I^2C Bus

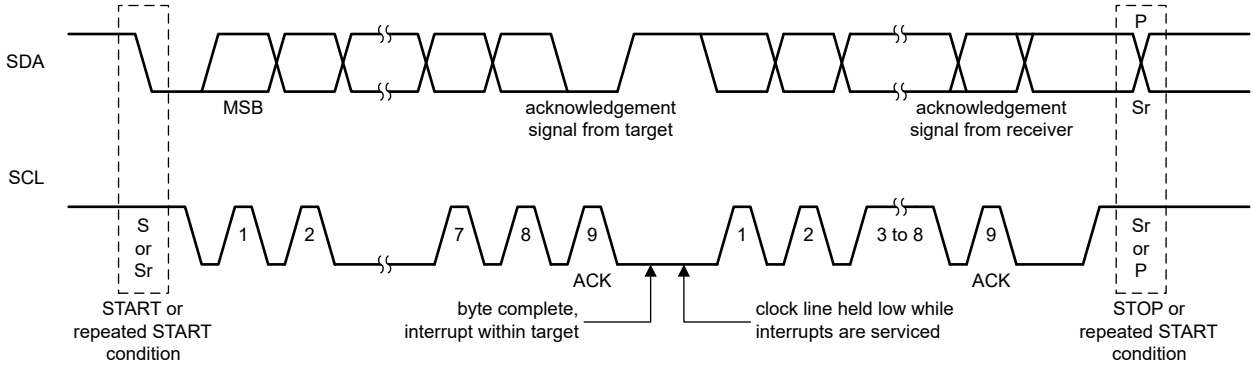

Figure 7-11. Bus Protocol

7.5.3 I²C Update Sequence

A single update requires the following:

- A start condition
- A valid I²C target address
- A register address
- A data byte

To acknowledge the receipt of each byte, the device pulls the SDA line low during the high period of a single clock pulse. The device performs an update on the falling edge of the acknowledge signal that follows the last byte.

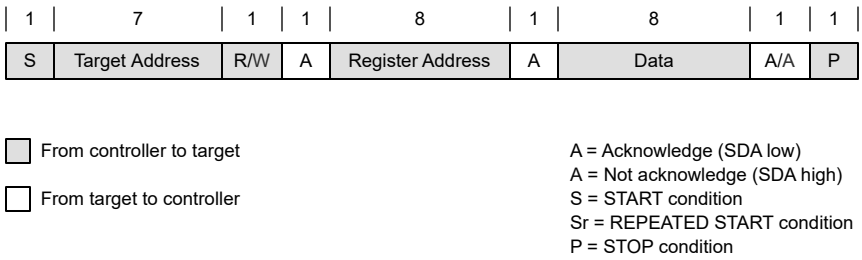

Figure 7-12. "Write" Data Transfer Format in Standard, Fast, and Fast-Plus Modes

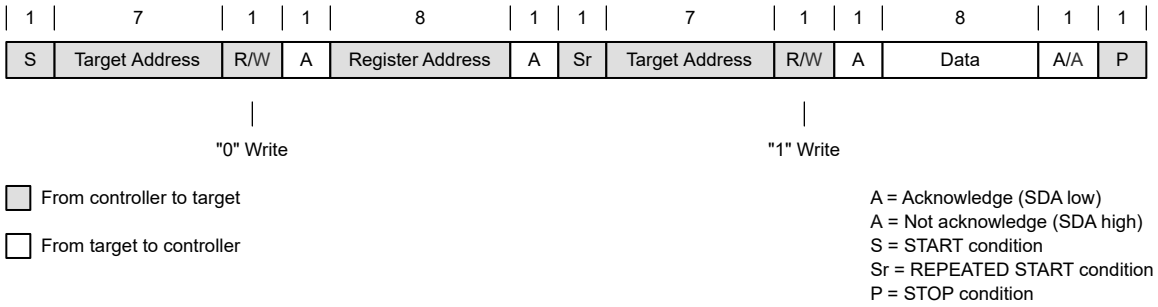

Figure 7-13. "Read" Data Transfer Format in Standard, Fast, and Fast-Plus Modes

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8 Register Map

8.1 Register Description

8.1.1 Register Map

ADDRESS	ACRONYM	REGISTER NAME	SECTION
0x01	CONTROL	Control Register	Go
0x02	STATUS	Status Register	Go
0x03	DEVID	DEVID Register	Go
0x04	VOUT1	VOUT1 Register	Go
0x06	CONTROL2	Control2 Register	Go

8.1.2 Register CONTROL (Register address: 0x01; Default: 0xE0 or 0x40)

Return to Register Map.

Table 8-1. Register CONTROL Format

7	6	5	4	3	2	1	0
EN_DISCHG	EN_SCP	ENABLE	ULTRA_SONIC	FPWM	RPWM	SLEW[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only

Table 8-2. Register CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DISCHG	R/W	X	Enable output discharge function. 0: output discharge function disabled (for TPS638201) 1 : Output discharge function enabled (for TPS63820)
6	EN_SCP	R/W	1	Enable output short circuit protection (Hiccup). 0: output short circuit protection disabled **1 : output short circuit protection enabled**
5	ENABLE	R/W	X	This bit controls operation of the converter. 0 : Converter operation disabled (Start-up value for TPS638201) 1 : Converter operation enabled (Start-up value for TPS63820)
4	ULTRA_SONIC	R/W	0	This bit controls the ultra-sonic mode function. **0: Ultra-sonic mode disabled** 1: Ultra-sonic mode enabled
3	FPWM	R/W	0	This bit controls the forced-PWM function. **0: Forced-PWM operation disabled** 1 : Forced-PWM operation enabled
2	RPWM	R/W	0	This bit controls the ramp-PWM function. **0: Ramp-PWM operation disabled** 1 : Ramp-PWM operation enabled
1:0	SLEW[1:0]	R/W	00	These bits control the slew rate of the DVS function. **00: ±1V/ms** 01: ±5V/ms 10: ±10V/ms 11: ±25V/ms

8.1.3 Register STATUS (Register address: 0x02; Default: 0x00)

Return to Register Map.

Table 8-3. Register STATUS Format

7	6	5	4	3	2	1	0
NIL[1:0]		VIN_OVP	VOUT_OVP	SC	OC	TSD	$\overline{PG}$

Table 8-3. Register STATUS Format (continued)

R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only

Table 8-4. Register STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7:6	NIL[1:0]	R	00	Not used. These bits always return 0 when read.
5	VIN_OVP	R	0	This bit shows the status of the VIN overvoltage function. **0: normal operation** 1 : A VIN overvoltage event was detected.
4	VOUT_OVP	R	0	This bit shows the status of the VOUT overvoltage function. **0: normal operation** 1 : A VOUT overvoltage event was detected.
3	SC	R	0	This bit shows the status of the output short circuit function. **0: normal operation** 1 : An output short circuit event was detected.
2	OC	R	0	This bit shows the status of the over current function. **0: normal operation** 1 : An over current event was detected.
1	TSD	R	0	This bit shows the status of the thermal shutdown function. **0: Temperature good** 1 : An overtemperature event was detected.
0	$\overline{PG}$	R	0	This bit shows the status of the power-good comparator. **0: Power-good** 1 : A power-not-good event was detected.

8.1.4 Register DEVID (Register address: 0x03; Default: 0x20)

Return to Register Map.

Table 8-5. Register DEVID Format

7	6	5	4	3	2	1	0
MANUFACTURER[3:0]				MAJOR[1:0]		MINOR[1:0]	
R				R		R	

LEGEND: R/W = Read/Write; R = Read only

Table 8-6. Register DEVID Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MANUFACTURER[3:0]	R	0010	These bits identify the device manufacturer. **0010: Texas Instruments**
3:2	MAJOR[1:0]	R	00	These bits identify the major silicon revision. **00: A (initial silicon)** 01: B (first major revision) 10: C (second major revision) 11: D (third major revision)
1:0	MINOR[1:0]	R	00	These bits identify the minor silicon revision. **00: 0 (initial silicon)** 01: 1 (first minor revision) 10: 2 (second minor revision) 11: 3 (third minor revision)

8.1.5 Register VOUT1 (Register address: 0x04; Default: 0x54)

Return to Register Map.

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Table 8-7. Register VOUT1 Format

7	6	5	4	3	2	1	0
VOUT1[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only

Table 8-8. Register VOUT1 Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VOUT1[7:0]	R/W	0101 0100	Output voltage = 1.200 + (VOUT1[7 :0] × 0.025) V (low range) (default = 3.3V)

8.1.6 Register CONTROL2 (Register address: 0x06; Default: 0x08)

Return to Register Map.

Table 8-9. Register CONTROL2 Format

7	6	5	4	3	2	1	0
SS_RAMP		CURRENT_LIMIT		BB_WINDOW		HYS_CURRENT	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only

Table 8-10. Register CONTROL Field Descriptions

Bit	Field	Type	Reset	Description
7:6	SS_RAMP	R/W	00	Defines the ramp time for the Vout soft start ramp **00: 0.3 ms** 01: 1.1ms 10: 4.0ms 11: 7.5ms
5:4	CURRENT_LIMIT	R/W	00	Defines the valley switching current limit **00: 6.5A** 01: 5.3A 10: 3.6A 11: 2.7A
3:2	BB_WINDOW	R/W	10	Defines the buck-boost voltage window 00: 200mV 01: 275mV **10: 350mV** 11: 450 mV
1:0	HYS_CURRENT	R/W	00	Define hysteresis current. **00: 800mA** 01: 1000mA 10: 750mA 11: 1100mA

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS63820 and TPS638201 devices are low quiescent current, high efficiency, high current buck-boost converters, designed for applications where the input voltage is higher, lower, or equal to the output voltage. The valley inductor current in the switches is limited to a typical value of 6.5A.

9.2 Typical Applications

9.2.1 1.2V to 5.5V Output Power Supply

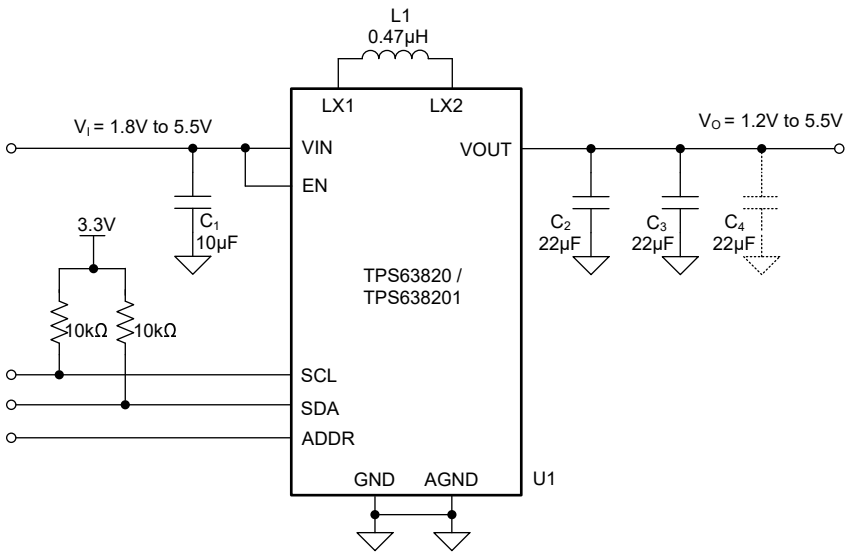

Figure 9-1. Typical Application Schematic

9.2.1.1 Design Requirements

This example uses the design parameters listed in Table 9-1.

Table 9-1. Design Parameters

DESIGN PARAMETER	SYMBOL	EXAMPLE VALUE
Input voltage	V_I	2.0V to 5.5V
Output voltage	V_O	1.2V to 5.5V
Output current	I_O	up to 4A (when $V_I \geq 3.0V$)
I^2C bus voltage	V_{BUS}	3.3V
I^2C bus speed		Fast-mode (400kHz)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Inductor Selection

Ti recommends to use the TPS63820 and TPS638201 devices with 0.47µH inductor. For high efficiencies, use an inductor with a low DC resistance (DCR) and low core losses.

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The saturation current of the inductor must be greater than the maximum inductor current in the application. To include sufficient margin for worst-case and transient operating conditions, use an inductor with saturation current that is at least 20% higher than the maximum inductor current in the application. The maximum current in the inductor occurs when the device operates in boost mode and the following is true:

- The input voltage is at the minimum value.
- The output voltage is at the maximum value.
- The output current is at the maximum value.

To calculate the maximum inductor current, first use Equation 1 to calculate the maximum duty cycle during boost operation (which is when the maximum inductor current occurs).

$$D = \frac{V_O - V_I}{V_O} \tag{1}$$

where

- D is the duty cycle
- V_I is the input voltage
- V_O is the output voltage

Next, use Equation 2 to calculate the maximum inductor current.

$$I_{LM} = \frac{I_O}{\eta(1 - D)} + \frac{DV_I}{2fL} \tag{2}$$

where

- I_{LM} is the peak inductor current
- I_O is the output current
- η is the converter efficiency (use the value from the application curves or assume 90%)
- D is the duty cycle (calculated with Equation 1)
- V_I is the input voltage
- f is the switching frequency (assume 1.5MHz)
- L is the inductance (use 0.47µH)

To include enough margin for transient conditions, use an inductor with a saturation current rating at least 20% higher than the calculated maximum current.

9.2.1.2.2 Output Capacitor Selection

TI recommends a minimum output capacitance (including DC bias effects) of 14µF. Two 22µF, 10V ceramic capacitors are deigned for typical applications with $V_{IN} \geq 2.6V$, $V_{OUT} = 3.3V$, $I_{OUT} \leq 2.0A$. For higher V_{OUT} or bigger I_{OUT}, three 22µF or two 47µF ceramic capacitors are suitable. To minimize switching noise on the output, connect a small ceramic capacitor (100nF is a typical value) in parallel to the two main output capacitors and place the small ceramic capacitor closest to the VOUT pin. Smaller capacitors have lower parasitic inductance and are more effective at filtering high frequencies than the two main output capacitors.

Make sure that the effective capacitance is given according to the recommended value in Section 6.3. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior as higher capacitance reduces transient response overshoot and undershoot and increases transient response time. Table 9-2 lists possible output capacitors.

Table 9-2. List of Recommended Capacitors

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
22	10	4	GRT188R61A226ME13D	Murata	0603 (1608)
47	10	4	LMK316ABJ476ML-T	Taiyo Yuden	1206 (3216)

(1) See the *Third-Party Products Disclaimer*.

9.2.1.2.3 Input Capacitor Selection

TI recommends a minimum input capacitance (including DC bias effects) of 5µF. A 10µF, 6.3V or 22µF, 10V ceramic capacitor is designed for typical applications. If the input supply is located more than a few centimeters from the converter, add additional bulk capacitance (a 47µF electrolytic or tantalum capacitor is a typical choice).

Table 9-3. List of Recommended Input Capacitors

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
10	6.3	4	GRM188R60J106ME84D	Murata	0603 (1608)
22	10	4	GRT188R61A226ME13D	Murata	0603 (1608)

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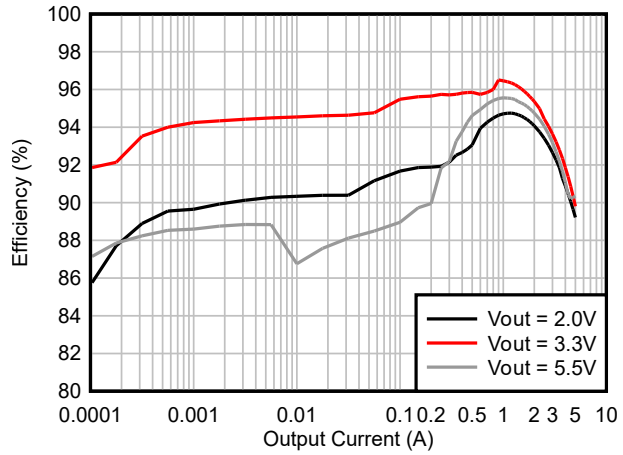
9.2.1.3 Application Curves

Table 9-4 lists the components that were used for the measurements contained in the following pages.

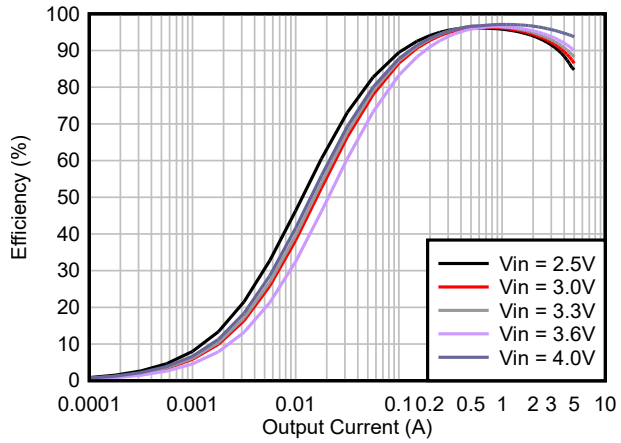
Table 9-4. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1	Capacitor, 10µF, 6.3V, 0603, ceramic	GRM188R60J106ME84D	Murata
C2, C3	Capacitor, 22µF, 10V, 0603, ceramic	GRT188R61A226ME13D	Murata
L1	Inductor, 0.47µH, 7.6mΩ	XFL4015-471MEC	Coilcraft
U1	Integrated circuit	TPS63820YBGR	Texas Instruments



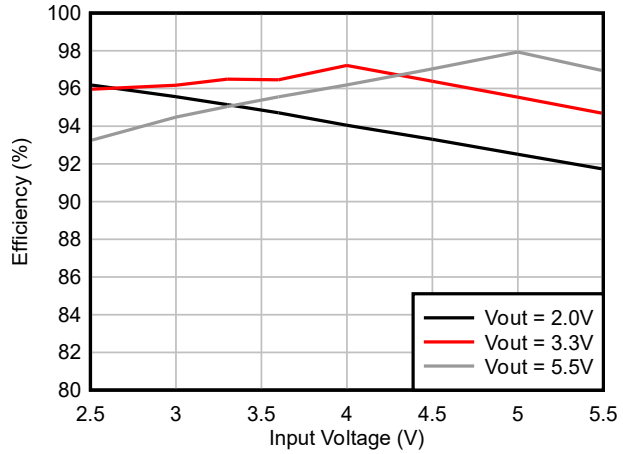
V_I = 3.6V PFM T_A = 25°C

Figure 9-2. Efficiency versus Output Current



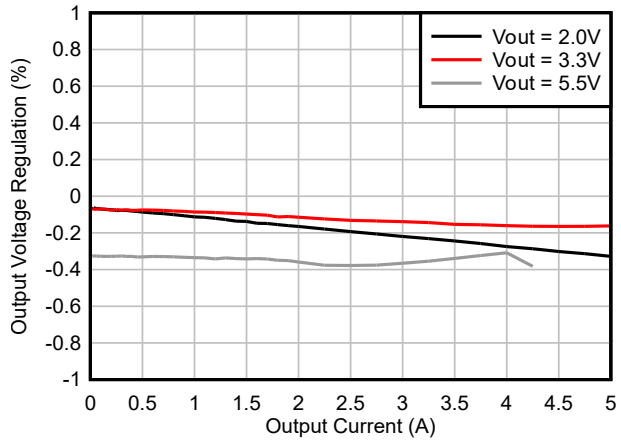
V_I = 3.6V FPWM T_A = 25°C

Figure 9-3. Efficiency versus Output Current



I_O = 1A PFM T_A = 25°C

Figure 9-4. Efficiency versus Input Voltage

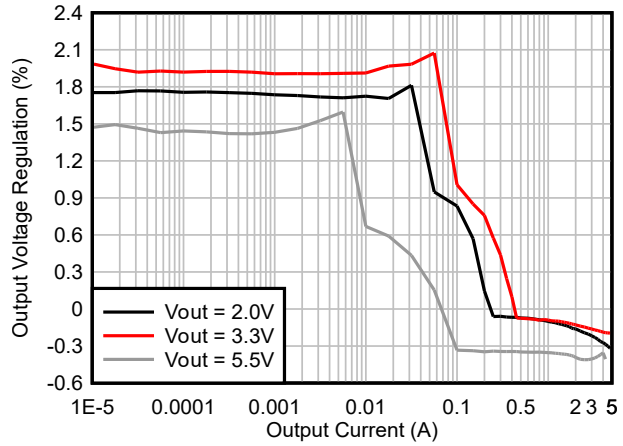


V_I = 3.6V FPWM T_A = 25°C

Figure 9-5. Load Regulation

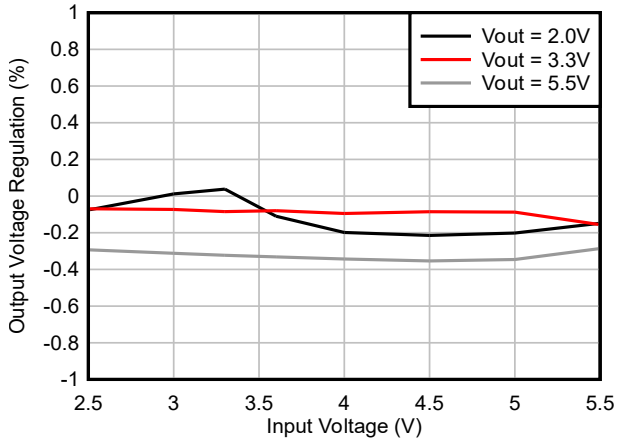
9.2.1.3 Application Curves (continued)

Table 9-4 lists the components that were used for the measurements contained in the following pages.



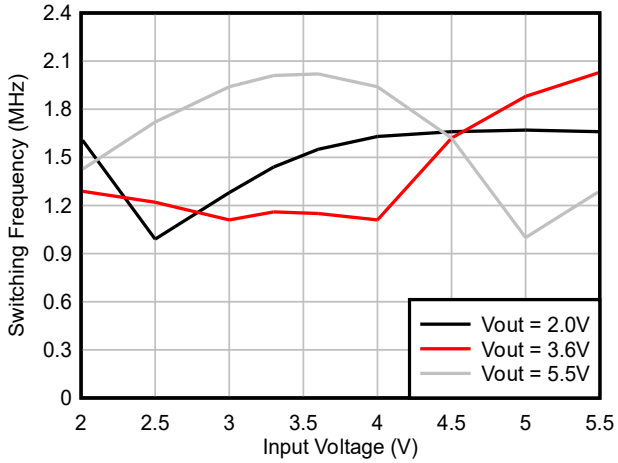
V_I = 3.6V PFM T_A = 25°C

Figure 9-6. Load Regulation



I_O = 1A FPWM T_A = 25°C

Figure 9-7. Line Regulation



I_O = 1A
V_I rising
FPWM
T_A = 25°C

Figure 9-8. Switching Frequency versus Input Voltage

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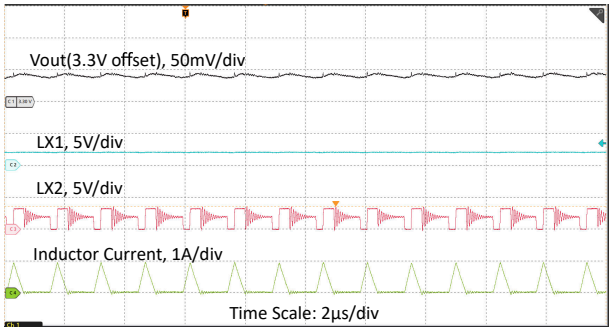
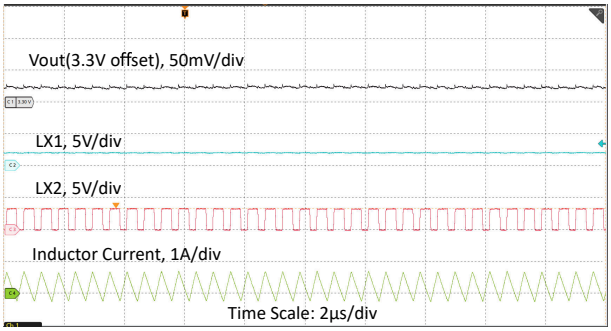
9.2.1.3 Application Curves (continued)

Table 9-4 lists the components that were used for the measurements contained in the following pages.



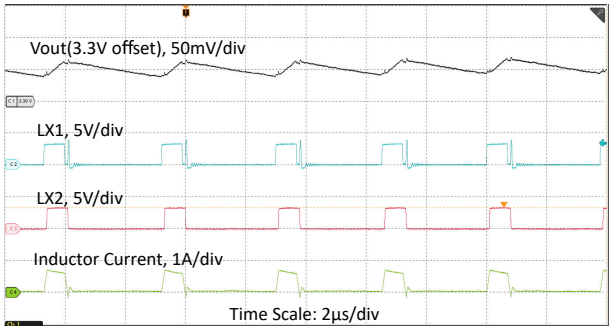
V_{IN} = 2.0V PFM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 9-9. Steady State (Boost Operation)



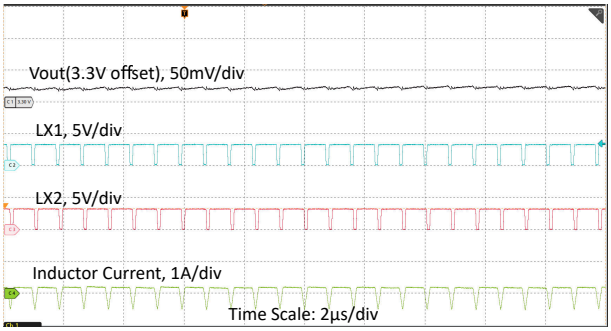
V_{IN} = 2.0V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 9-10. Steady State (Boost Operation)



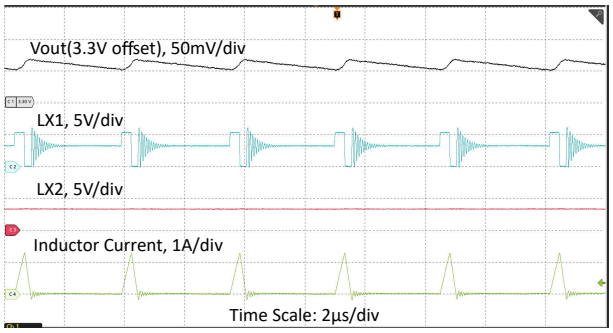
V_{IN} = 3.3V PFM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 9-11. Steady State (Buck-Boost Operation)



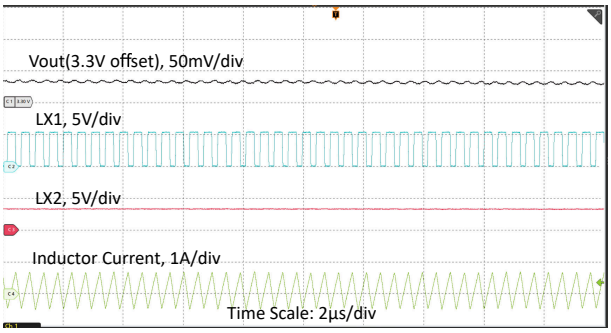
V_{IN} = 3.0V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 9-12. Steady State (Buck-Boost Operation)



V_{IN} = 5.5V PFM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 9-13. Steady State (Buck Operation)

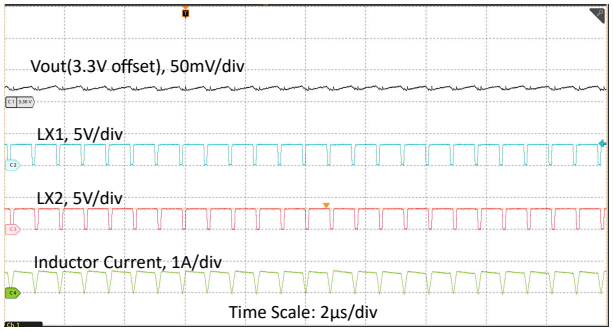


V_{IN} = 5.5V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 9-14. Steady State (Buck Operation)

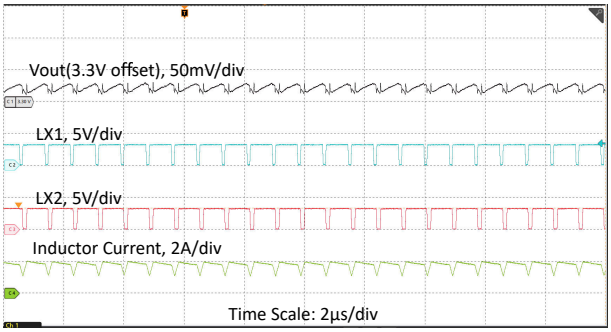
9.2.1.3 Application Curves (continued)

Table 9-4 lists the components that were used for the measurements contained in the following pages.



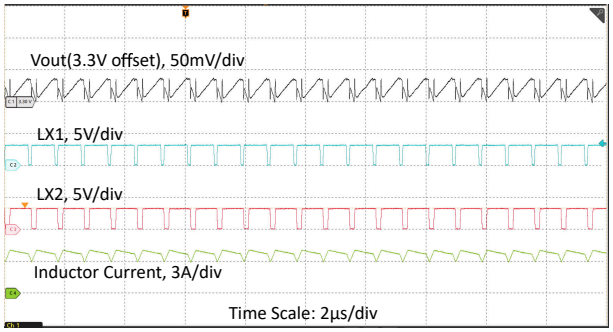
V_{IN} = 3.3V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 500mA

Figure 9-15. Steady State (Buck-Boost Operation)



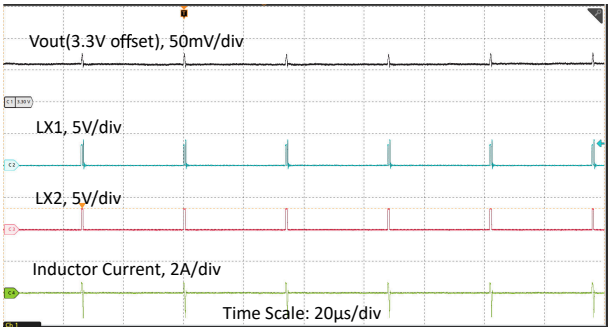
V_{IN} = 3.3V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 1.5A

Figure 9-16. Steady State (Buck-Boost Operation)



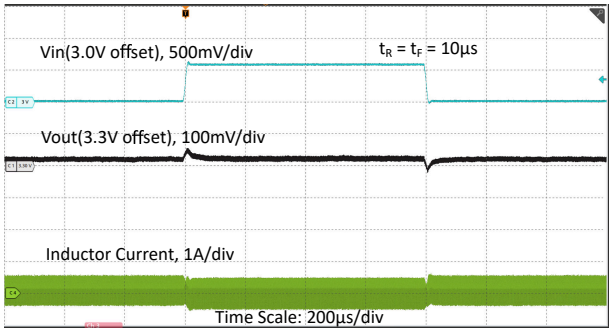
V_{IN} = 3.3V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 3.0A

Figure 9-17. Steady State (Buck-Boost Operation)



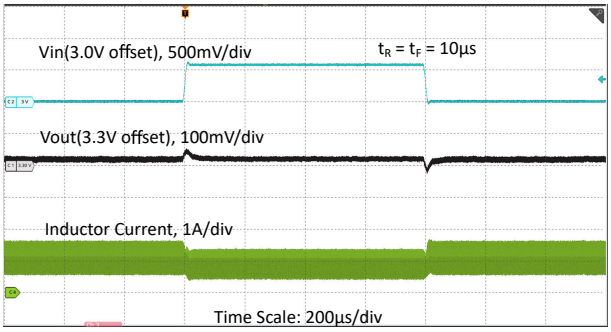
V_{IN} = 3.3V Ultra-Sonic Mode T_A = 25°C
V_{OUT} = 3.3V No load

Figure 9-18. Steady State (Buck-Boost Operation)



V_I = 3.0V to 3.6V to 3.0V PFM T_A = 25°C
V_O = 3.3V I_O = 200mA

Figure 9-19. Line Transient Response



V_I = 3.0V to 3.6V to 3.0V PFM T_A = 25°C
V_O = 3.3V I_O = 1.0A

Figure 9-20. Line Transient Response

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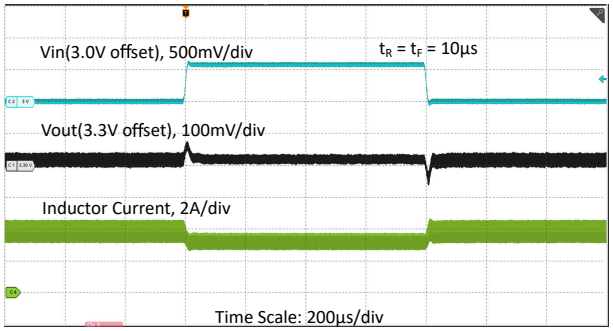
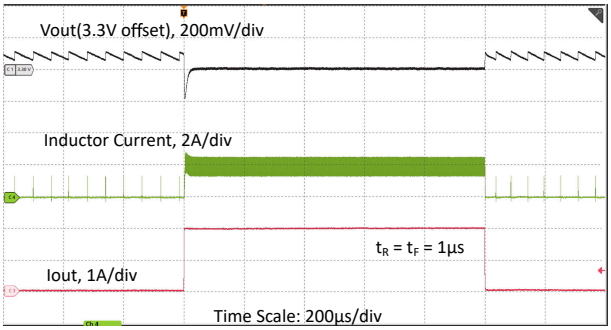
9.2.1.3 Application Curves (continued)

Table 9-4 lists the components that were used for the measurements contained in the following pages.



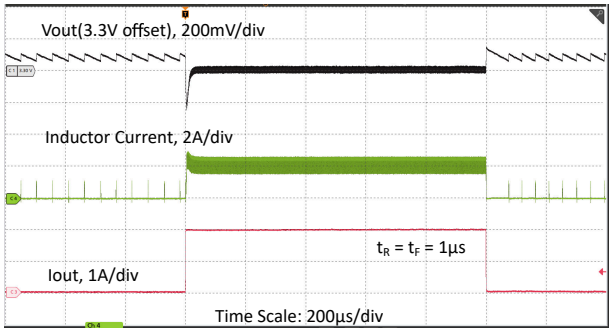
V_I = 3.0V to 3.6V to 3.0V PFM T_A = 25°C
V_O = 3.3V I_O = 3.0A

Figure 9-21. Line Transient Response



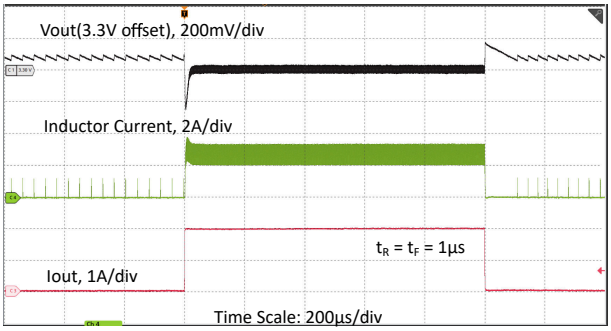
V_I = 4.2V PFM T_A = 25°C
V_O = 3.3V I_O = 10mA to 2A to 10mA

Figure 9-22. Load Transient Response (Buck)



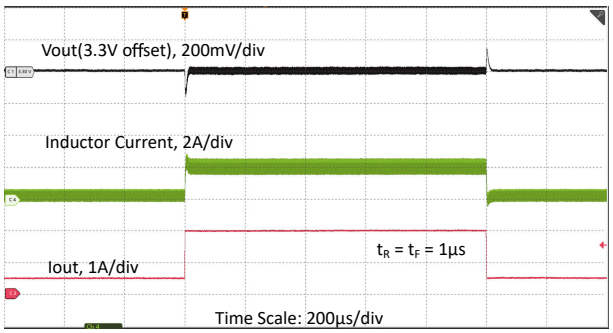
V_I = 3.3V PFM T_A = 25°C
V_O = 3.3V I_O = 10mA to 2A to 10mA

Figure 9-23. Load Transient Response (Buck-Boost)



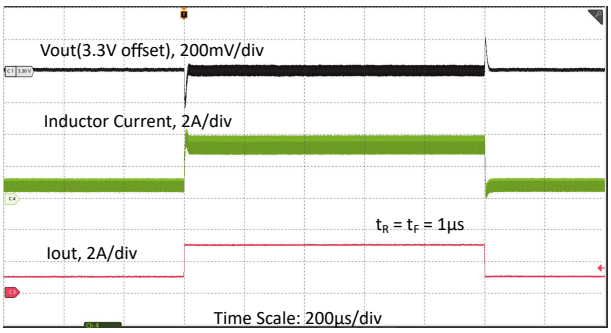
V_I = 2.6V PFM T_A = 25°C
V_O = 3.3V I_O = 10mA to 2A to 10mA

Figure 9-24. Load Transient Response (Boost)



V_I = 3.3V FPWM T_A = 25°C
V_O = 3.3V I_O = 0.5A to 2A to 0.5A

Figure 9-25. Load Transient Response (Buck-Boost)

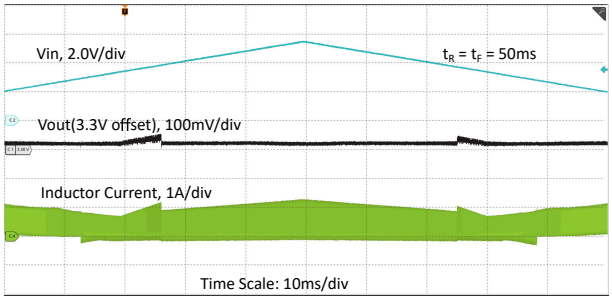


V_I = 3.3V FPWM T_A = 25°C
V_O = 3.3V I_O = 1.0A to 3A to 1.0A

Figure 9-26. Load Transient Response (Buck-Boost)

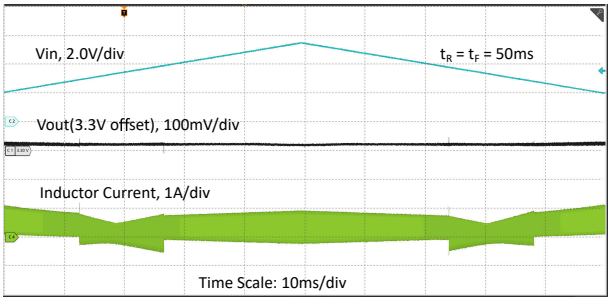
9.2.1.3 Application Curves (continued)

Table 9-4 lists the components that were used for the measurements contained in the following pages.



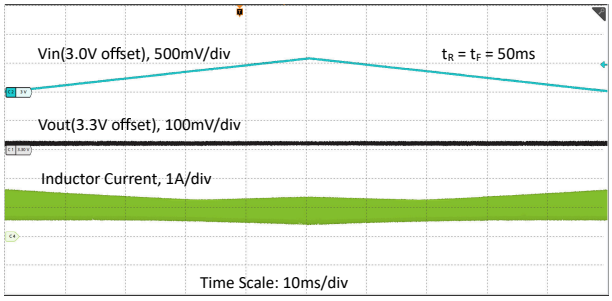
V_I = 2.0V to 5.5V to 2.0V PFM T_A = 25°C
V_O = 3.3 V R_{LOAD} = 10Ω

Figure 9-27. Line Sweep (PFM)



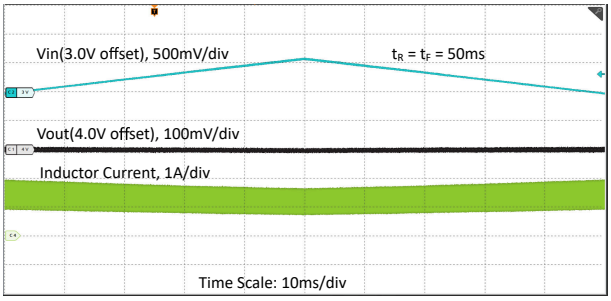
V_I = 2.0V to 5.5V to 2.0V FPWM T_A = 25°C
V_O = 3.3V R_{LOAD} = 10Ω

Figure 9-28. Line Sweep (FPWM)



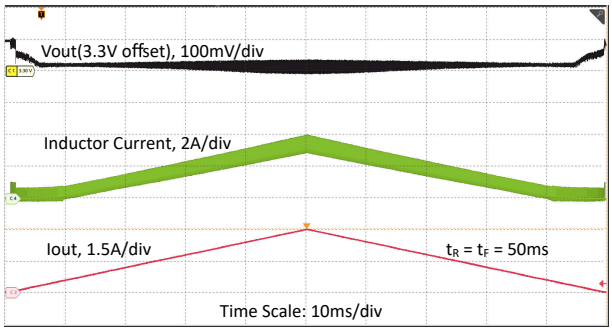
V_I = 3.0V to 3.6V to 3.0V FPWM T_A = 25°C
V_O = 3.3V I_O = 1.0A BB window = 350mV

Figure 9-29. Line Sweep (FPWM, totally in buck-boost)



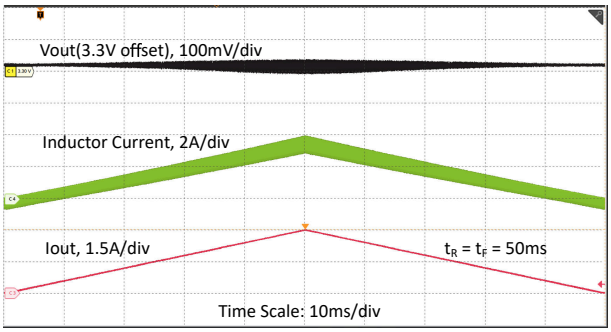
V_I = 3.0V to 3.6V to 3.0V FPWM T_A = 25°C
V_O = 4.0V I_O = 1.0A BB window = 275mV

Figure 9-30. Line Sweep (FPWM, totally in boost)



V_I = 3.3V PFM T_A = 25°C
V_O = 3.3V I_O = 0A to 3A to 0A

Figure 9-31. Load Sweep (PFM)



V_I = 3.3V FPWM T_A = 25°C
V_O = 3.3V I_O = 0A to 3A to 0A

Figure 9-32. Load Sweep (FPWM)

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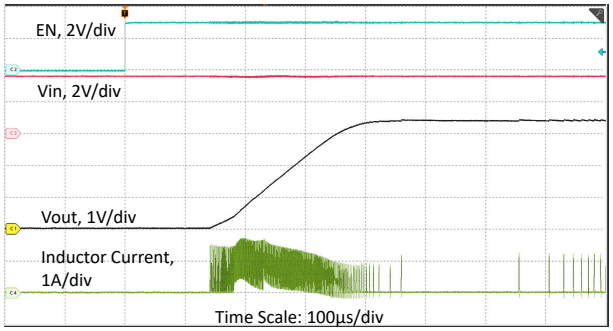
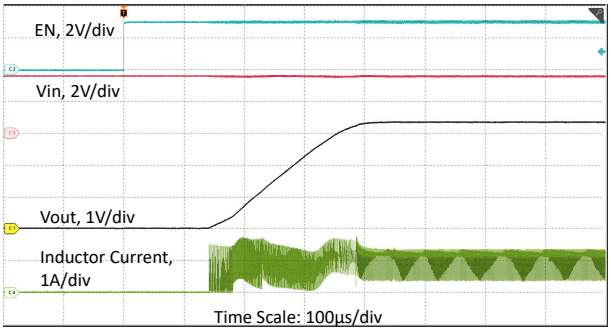
9.2.1.3 Application Curves (continued)

Table 9-4 lists the components that were used for the measurements contained in the following pages.



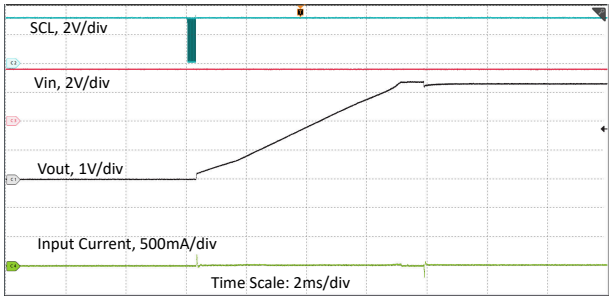
V_I = 3.6V PFM T_A = 25°C
V_O = 3.3V R_{LOAD} = 33Ω

Figure 9-33. Start-Up Waveforms (Light Load)



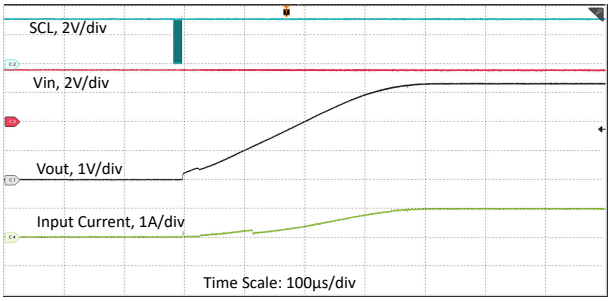
V_I = 3.6V PFM T_A = 25°C
V_O = 3.3V R_{LOAD} = 3.3Ω

Figure 9-34. Start-Up Waveforms (Heavy Load)



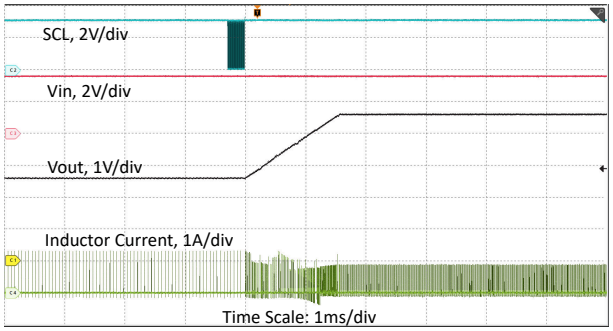
V_I = 3.6V FPWM T_A = 25°C
V_O = 3.3V No load Soft Start = 7.5ms

Figure 9-35. Start-Up Waveforms (No Load)



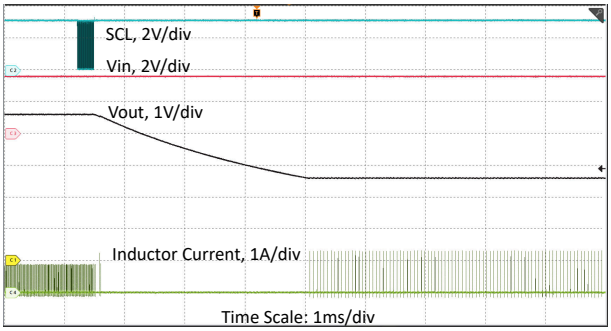
V_I = 3.6V FPWM T_A = 25°C
V_O = 3.3V R_{LOAD} = 3.3Ω Soft Start = 7.5ms

Figure 9-36. Start-Up Waveforms (Heavy Load)



V_I = 3.6V RPWM disable T_A = 25°C
V_O = 2.5V to 4.5V R_L = 330Ω

Figure 9-37. Dynamic Voltage Scaling (RPWM Disable)

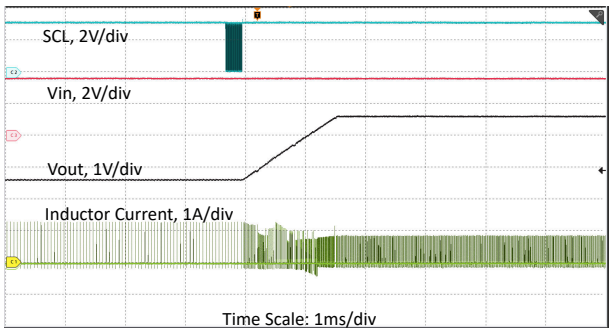


V_I = 3.6V RPWM disable T_A = 25°C
V_O = 4.5V to 2.5V R_L = 330Ω

Figure 9-38. Dynamic Voltage Scaling (RPWM Disable)

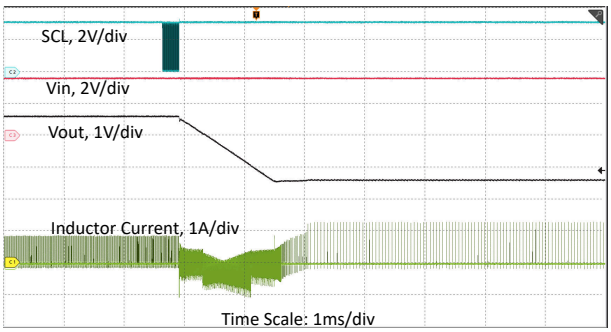
9.2.1.3 Application Curves (continued)

Table 9-4 lists the components that were used for the measurements contained in the following pages.



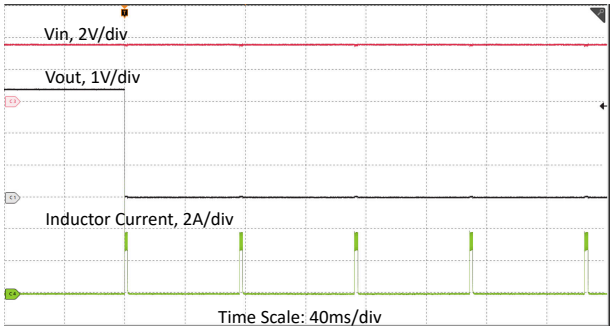
V_I = 3.6V RPWM enable T_A = 25°C
V_O = 2.5V to 4.5V R_L = 330 Ω

Figure 9-39. Dynamic Voltage Scaling (RPWM Enable)



V_I = 3.6V RPWM enable T_A = 25°C
V_O = 4.5V to 2.5V R_L = 330 Ω

Figure 9-40. Dynamic Voltage Scaling (RPWM Enable)



V_I = 3.6V PFM T_A = 25°C
V_O = 3.3V No load

Figure 9-41. Output Short Protection

9.3 Power Supply Recommendations

The device is designed to operate with a DC supply voltage in the range 2.2V to 5.5V. If the input supply is more than a few centimeters from the device, TI recommends adding some bulk capacitance to the ceramic bypass capacitors. A 47µF electrolytic capacitor is a typical selection for the bulk capacitance.

9.4 Layout

9.4.1 Layout Guidelines

Correct PCB layout is necessary to obtain the full performance from the device. TI recommends to follow these basic principles:

- Place input and output capacitors close to the device to minimize the input and output loop areas.
- When combining different-sized capacitors to make up the total input capacitance, place the smallest capacitor closest to the device. The same applies to the output capacitance.
- Keep PCB traces short and wide to minimize parasitic resistance and inductance.
- Use the following PCB layer stack (or something similar):
  - Layer 1 (top): All components and all power traces
  - Layer 2 (inner): Signals
  - Layer 3 (inner): Signals
  - Layer 4 (bottom): Ground plane

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Figure 9-42 shows an example of the PCB layout used for all measurement data in *Application Curves*.

9.4.2 Layout Example

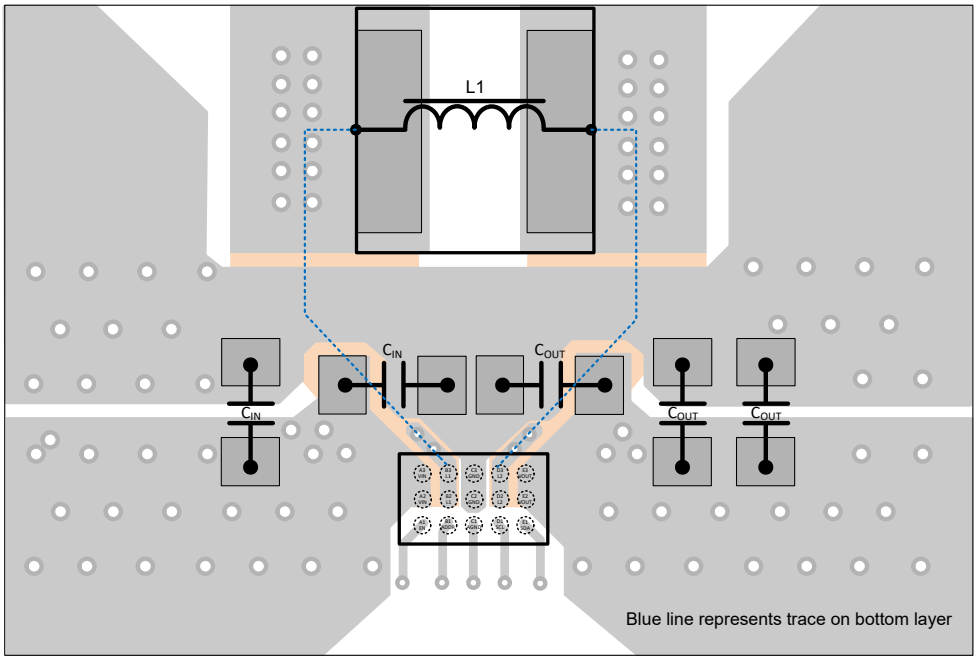

Figure 9-42. Recommended PCB Layout for the TPS63820 Device

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- *NXP Semiconductors, UM10204 – I^2C-Bus Specification and User Manual*
- Texas Instruments, *TPS6381xEVM* user guide

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Revision History

Changes from Revision * (March 2026) to Revision A (June 2026) **Page**

- Deleted product preview note from the TPS638201 in the *Device Information* table.....1
- Added note 3 to the *Device Information* table.....1
- Deleted product preview note from the TPS638201 in the *Device Comparison Table* 3
- Changed the CDM standard from "JEDEC specification JESD22C101" to "ANSI/ESDA/JEDEC JS-002".....5
- Updated table note in the Thermal Information table to current standards 6
- Changed the symbol of Q1 and Q4 from PMOS to NMOS in Figure 7-2 11
- Changed the symbol of Q1 and Q4 from PMOS to NMOS in Figure 7-3 11
- Changed the symbol of Q1 and Q4 from PMOS to NMOS in Figure 7-4 11
- Changed the legend from "Vin" to "Vout" in Figure 9-8 25

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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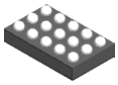
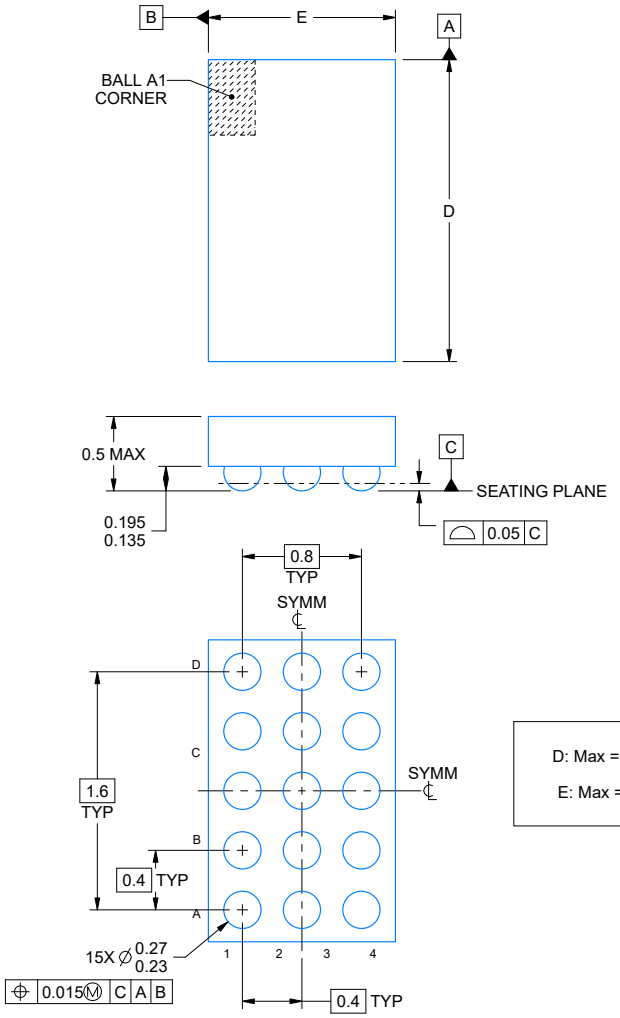
PACKAGE OUTLINE

YBG0015-C01



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 2.049 mm, Min = 2.009 mm

E: Max = 1.277 mm, Min = 1.237 mm

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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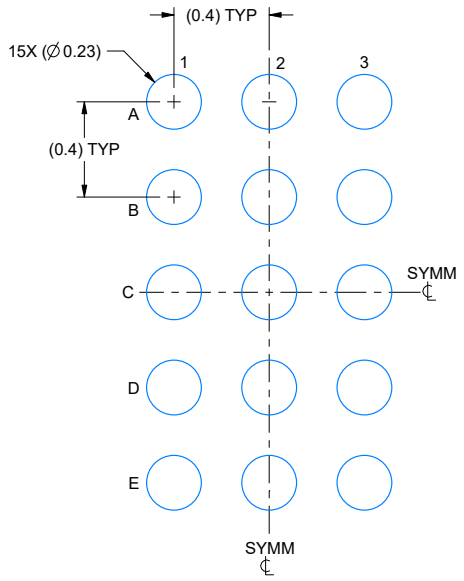
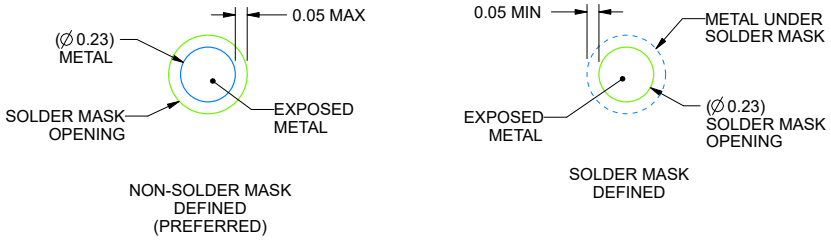
EXAMPLE BOARD LAYOUT

YBG0015-C01 **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

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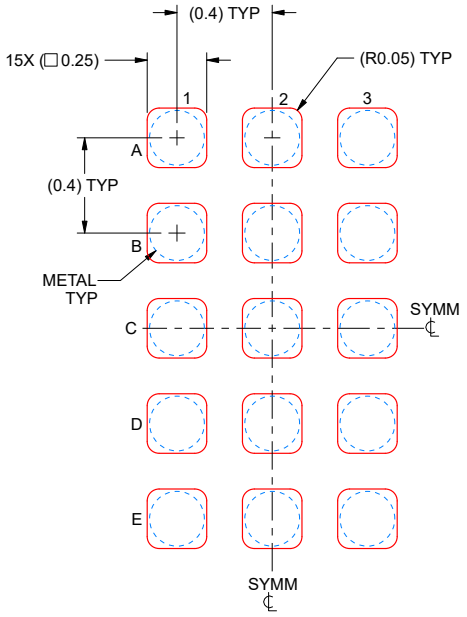
EXAMPLE STENCIL DESIGN

YBG0015-C01 **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS638201YBGR	Active	Production	DSBGA (YBG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	22T
TPS63820YBGR	Active	Production	DSBGA (YBG) | 15	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1ZI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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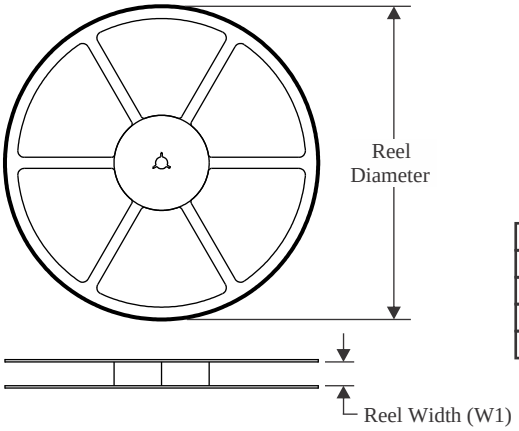
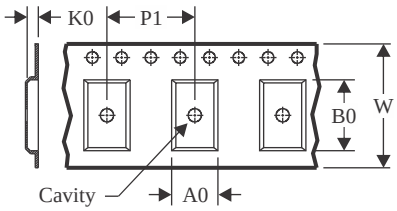
TAPE AND REEL INFORMATION

REEL DIMENSIONS

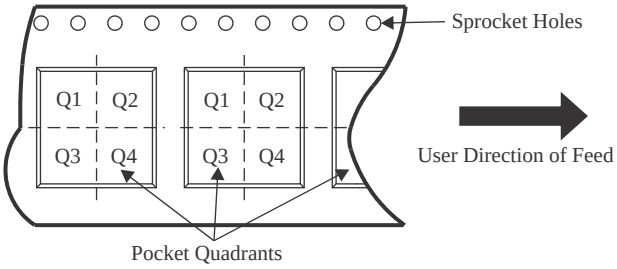


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

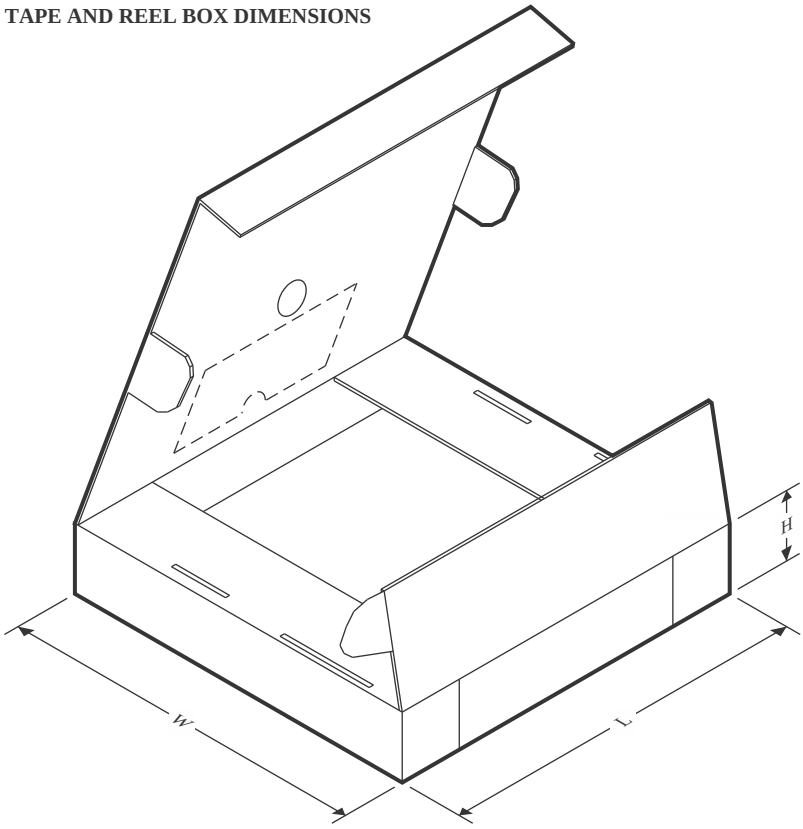
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS638201YBGR	DSBGA	YBG	15	3000	180.0	8.4	1.68	1.72	0.62	4.0	8.0	Q1
TPS63820YBGR	DSBGA	YBG	15	3000	180.0	8.4	1.68	1.72	0.62	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS638201YBGR	DSBGA	YBG	15	3000	182.0	182.0	20.0
TPS63820YBGR	DSBGA	YBG	15	3000	182.0	182.0	20.0

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