TPS63822 and TPS638221 Low Quiescent Current, 4A Buck-Boost Converters

1 Features

- Input voltage range: 1.8V to 5.5V
  - 2.0V minimum input voltage for start-up
- V_{OUT} range: 1.2V to 5.5V
- Output current
  - Up to 3.5A for $V_{IN} \geq 2.5V$, $V_{OUT} = 3.3V$
  - Up to 4A for $V_{IN} \geq 3V$, $V_{OUT} = 3.3V$
- High efficiency over the entire load range
  - Low 2.3µA operating quiescent current
  - 91.94% efficiency at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 100µA$ (in buck-boost mode)
  - 95.33% efficiency at $V_{IN} = 3.6V$, $V_{OUT} = 3.3V$, $I_{OUT} = 2A$ (in buck-boost mode)
- Automatic power save mode, ultra-sonic mode, and forced PWM mode selectable
- Windowed power good indicated by PG pin
- Output discharge function (TPS638221 only)
- Supports 1.2V logic I/O
- Safety and robust protection features
  - Overtemperature protection
  - Input and output overvoltage protection
  - True load disconnect during shutdown
  - Forward and backward current limit
  - Hiccup protection
- 15-ball WCSP package (2.029mm × 1.257mm)

2 Applications

- System pre-regulator
- Point-of-load regulation
- Optical modules
- Broadband network radio or SoC supply

3 Description

The TPS63822 and TPS638221 are low quiescent current, high output current buck-boost converters with a typical valley current limit of 6.5A. The 2.3µA quiescent current and four low Rdson MOSFETs enable high efficiency from a light to a heavy load range.

Depending on the input voltage, the devices automatically operate in boost, buck, or in buck-boost mode when the input voltage is approximately equal to the output voltage. The transitions between modes occur at defined thresholds and avoid unwanted toggling within the modes which reduces output voltage ripple.

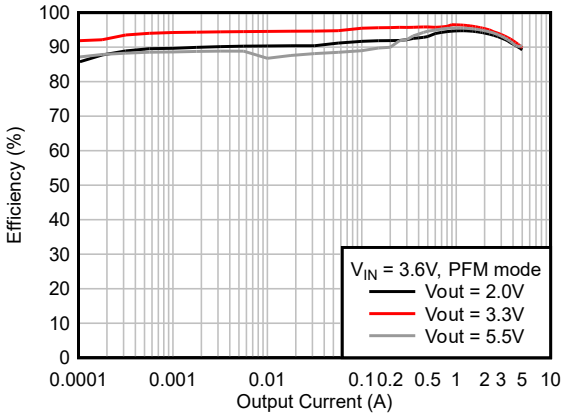
The devices have a fast dynamic response, which enables the regulation of output voltage tightly, even in the event of heavy load transients.

The devices offer a small solution size in WCSP.

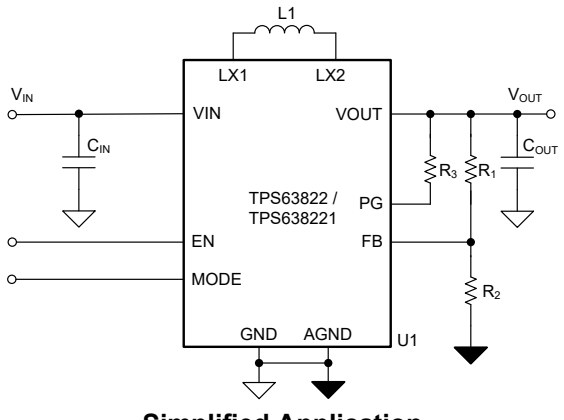
Device Information

PART NUMBER(1)	PACKAGE(2)	PACKAGE SIZE(3)
TPS63822(4)	YBG (DSBGA, 15)	2.029mm × 1.257mm
TPS638221		

(1) See the *Device Comparison Table*.
(2) For more information, see Mechanical, Packaging, and Orderable Information.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.
(4) Product preview. Contact TI factory for more information.



Efficiency vs I_{OUT}



Simplified Application

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4 Device Comparison Table

PART NUMBER	Output Discharge
TPS63822YBGR(1)	No
TPS638221YBGR	Yes

(1) Product preview. Contact TI factory for more information.

5 Pin Configuration and Functions

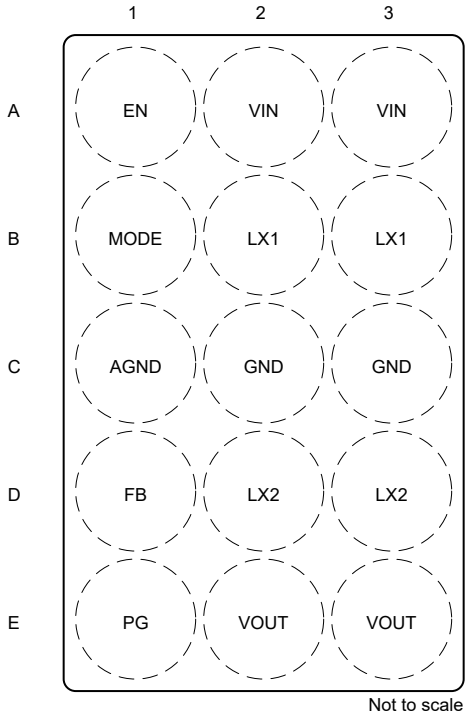


Figure 5-1. TPS63822 and TPS638221 YBG Package, 15-Ball DSBGA (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	EN	I	Device enable. A high logic level on this pin enables the device; a low logic level on this pin disables the device.
A2, A3	VIN	PWR	Supply voltage for power stage
B1	MODE	I	Auto PFM/PWM/Ultrasonic mode selection MODE = Logic low, auto PFM mode MODE = Logic high, FPWM mode MODE = floating, ultrasonic mode
B2, B3	LX1	PWR	Inductor connection
C1	AGND	—	Analog ground
C2, C3	GND	PWR	Power ground
D1	FB	I	Voltage feedback of adjustable versions. When FB is connected to AGND, the output voltage is fixed at 3.3V.
D2, D3	LX2	PWR	Inductor connection
E1	PG	O	Power good indicator and open drain output. If not used, this pin can be left floating.
E2, E3	VOUT	PWR	Converter output

(1) I = input, O = output, PWR = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_I	Input voltage (VIN, LX1, LX2, VOUT, MODE, FB, EN, PG)(2)	-0.3	6	V
V_I	Input voltage for less than 10 ns (LX1, LX2)(2)	-0.7	8	V
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Supply voltage		1.8		5.5	V
V_O	Output voltage		1.2		5.5	V
I_O	Output current(1)	V_{OUT} = 3.3V, V_{IN} ≥ 2.6V			3.5	A
C_I	Input capacitance(2)		5			µF
C_O	Output capacitance(2)	V_{OUT} = 3.3V, V_{IN} ≥ 2.6V, I_{OUT} ≤ 2A	14	16		µF
L	Inductance		390	470	560	nH
T_A	Operating free-air temperature range		-40		85	°C
T_J	Operating junction temperature range		-40		125	°C

(1) The device can sustain the maximum recommended output current only for short durations before its junction temperature gets too hot. Users must verify that the thermal performance of the end application can support the maximum output current.
(2) Effective capacitance after DC bias effects have been considered.

6.4 Thermal Information

THERMAL METRIC[1]		TPS63822 TPS638221 YBG (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.5 Electrical Characteristics

T_J = -40°C to 125°C, V_{IN} = 2.0V to 5.5V. Typical values are at V_{IN} = 3.6V, V_{OUT} = 3.3V and T_J = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			1.8		5.5	V
V_{IT+}	Positive-going UVLO threshold voltage			1.8	1.9	2.0	V
V_{IT-}	Negative-going UVLO threshold			1.6	1.7	1.8	V
V_{HYS}	Hysteresis voltage				200		mV
I_Q	Quiescent current into VIN		V_{IN} = 3.6V, V_{EN} = 3.6V, V_{OUT} = 3.3V, non-switching, T_J = –40°C to 85°C		2.3	4	µA
I_Q	Quiescent current into VOUT		V_{IN} = 3.6V, V_{EN} = 3.6V, V_{OUT} = 3.3V, non-switching, T_J = –40°C to 85°C		0.3	1	µA
I_{SD}	Shutdown current into VIN		V_{IN} = 3.6V, V_{OUT} = 0V, V_{EN} = 0V T_J = –40°C to 85°C		0.3	2.5	µA
I/O SIGNALS							
V_{IT+}	Positive-going input threshold voltage	MODE, EN				0.82	V
V_{IT-}	Negative-going input threshold voltage	MODE, EN		0.33			V
V_{IM}	Mid-level input voltage	MODE			0.6		V
I_{IH}	High-level input current	MODE	V_{MODE} = 1.2V		0.01	0.1	µA
I_{IL}	Low-level input current	MODE	V_{MODE} = 0V		0.01	0.1	µA
I_{IB}	Input bias current	EN	V_{EN} = 0V to 5.5V		2.5	30	nA
R_{EN}	EN pin pulldown resistor		EN = low		800		kΩ
POWER STAGE							
V_O	Output voltage range			1.2		5.5	V
V_{REF}	Feedback Regulation Voltage			0.792	0.800	0.808	V
	PFM valley - DC offset		PFM operation	0.7	1.5	2.5	%
	DC offset		Ultra-sonic operation, V_{OUT} ≥ 2.5V	0.7	1.25	2.5	%
I_{FB_lkg}	Leakage current at FB pin					50	nA
	Valley switching current limit			5.7	6.5	7	A
	Reverse valley switching current limit			-4.0	-3.3	-2	A
	Hysteresis current				800		mA

6.5 Electrical Characteristics (continued)

T_J = -40°C to 125°C, V_{IN} = 2.0V to 5.5V. Typical values are at V_{IN} = 3.6V, V_{OUT} = 3.3V and T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Buck side $R_{DS(on)}$	High-side MOSFET on resistance on buck side			11.6		mΩ
	Low-side MOSFET on resistance on buck side			15.5		
Boost side $R_{DS(on)}$	High-side MOSFET on resistance on boost side			11.6		
	Low-side MOSFET on resistance on boost side			15.3		
I_{lkg}	Leakage current into VIN to LX1	EN = GND, V_{IN}=5.5V, V_{LX1}=0V, T_J = –40°C to 85°C		0.03	4	µA
I_{lkg}	Leakage current into VOUT to LX2	EN = GND, V_{OUT}=5.5V, V_{LX2}=0V, T_J = –40°C to 85°C		0.03	4	µA
I_{lkg}	Leakage current into LX1 to GND	EN = GND, V_{LX1}=5.5V, T_J = –40°C to 85°C		0.02	4	µA
I_{lkg}	Leakage current into LX2 to GND	EN = GND, V_{LX2}=5.5V, T_J = –40°C to 85°C		0.02	4	µA
I_{DISCHG}	Output discharge current	V_{IN} = 3.0V		160		mA
TIMING PARAMETER						
t_{SS}	Soft-start time		0.2	0.3	0.4	mS
$t_{d(EN)}$	Delay between a rising edge on the EN pin and the start of output voltage ramp			200	240	µS
	Switching frequency at ultra-sonic mode		24			kHz
PROTECTION						
$V_{T+(IVP)}$	Input OVP threshold voltage		5.65	5.75	5.95	V
	Input OVP hysteresis			100		mV
$V_{T+(OVP)}$	Output OVP threshold voltage		5.65	5.75	5.95	V
	Output OVP hysteresis			100		mV
$V_{PG\_TH\_rising}$	Power good threshold for rising			95		%
$V_{PG\_TH\_falling}$	Power good threshold for falling			90		%
V_{PG_low}	Power good low level output voltage				0.36	V
I_{lkg}	PG pin leakage current				0.03	µA
	hiccup on time			2		mS
	hiccup off time			74		mS
	Thermal shutdown threshold temperature	T_J rising		165		°C
	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

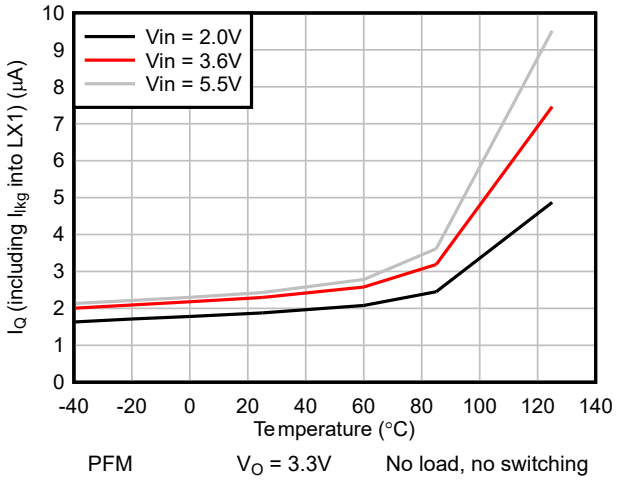


Figure 6-1. I_Q (Including Leakage Into LX1) Versus Temperature

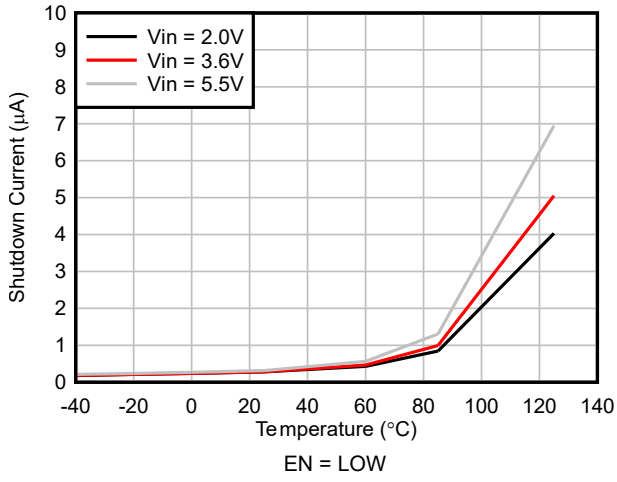


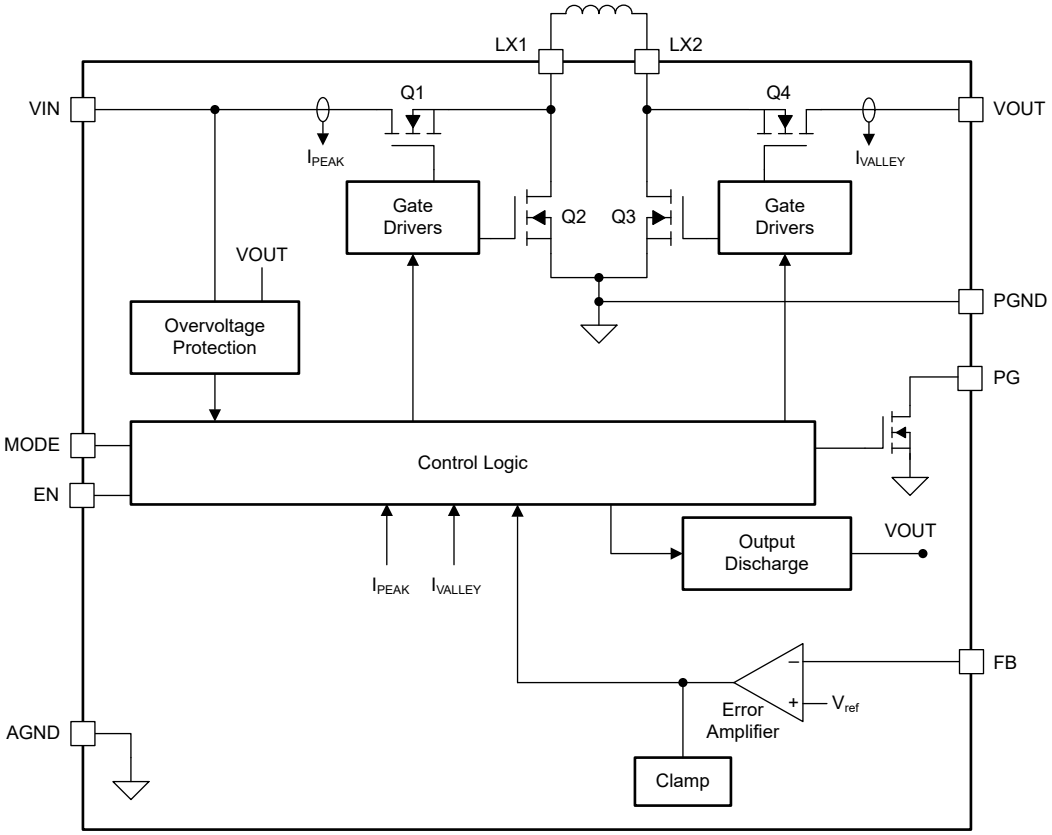
Figure 6-2. Shutdown Current Versus Temperature

7 Detailed Description

7.1 Overview

The TPS63822 and TPS638221 devices are low quiescent current, high-efficiency buck-boost converters. Four switches are integrated to maintain synchronous power conversion under all operating conditions, so that the device achieves high efficiency power conversion over a wide range of input voltages and output currents. The device automatically switches between buck, boost, and buck-boost operation as required by the operating conditions. The device operates as a true buck converter when $V_I > V_O$ and as a true boost converter when $V_I < V_O$. When $V_I \approx V_O$, the device operates in a 3-cycle buck-boost mode.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Scheme

The device automatically selects the best switching scheme for the operating conditions. To make sure of stable operation, the selection logic includes hysteresis (see Figure 7-1).

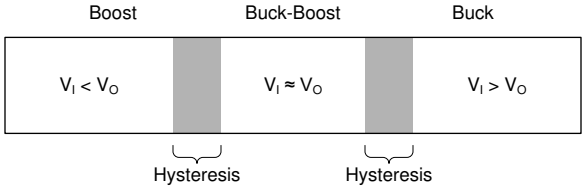


Figure 7-1. Switching Scheme Selection

7.3.1.1 Buck Operation

When $V_I > V_O$, the device switches like a buck converter:

- Q1 is the switch.
- Q2 is the rectifier.
- Q3 is permanently off.
- Q4 is permanently on.

See Figure 7-2. During buck operation, one switching cycle comprises two phases: on–off.

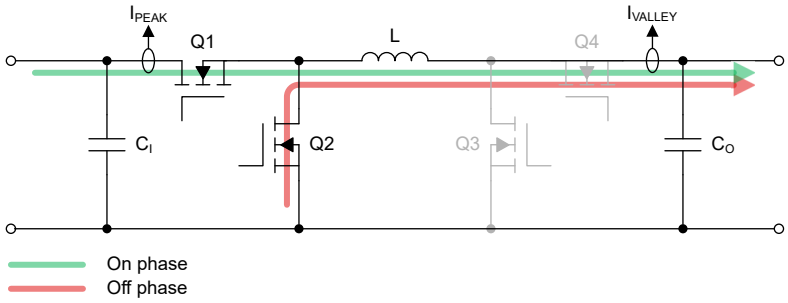


Figure 7-2. Buck Switch Configuration

7.3.1.2 Boost Operation

When $V_I < V_O$, the device switches like a boost converter:

- Q1 is permanently on.
- Q2 is permanently off.
- Q3 is the switch.
- Q4 is the rectifier.

See Figure 7-3. During boost operation, one switching cycle comprises two phases: on–off.

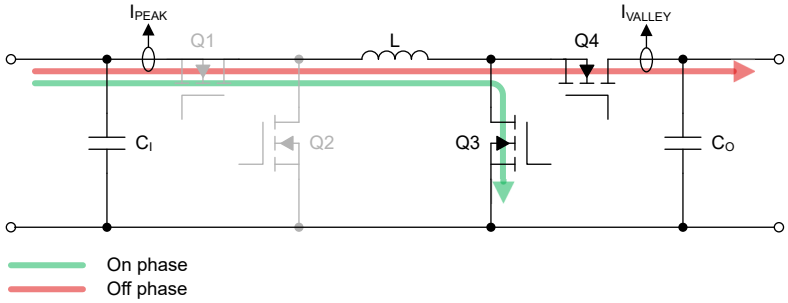


Figure 7-3. Boost Switch Configuration

7.3.1.3 Buck-Boost Operation

When $V_I \approx V_O$, all four transistors switch continuously (see Figure 7-4). During buck-boost operation, one switching cycle comprises three phases: on–commutate–off.

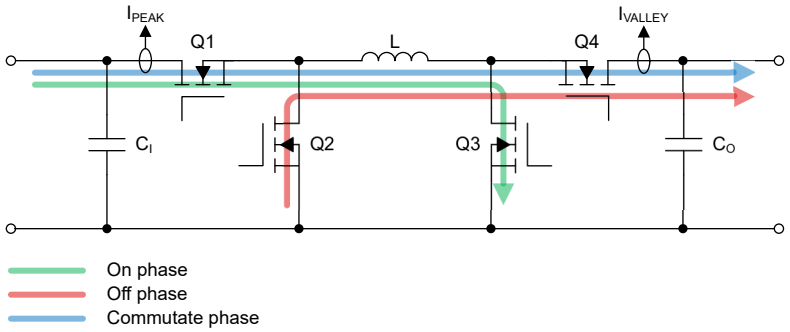


Figure 7-4. Buck-Boost Switch Configuration

7.3.2 Operation Mode

The TPS63822 and TPS638221 have three different operation modes of pulse-frequency modulation (PFM) mode, forced pulse-width modulation (FPWM) mode and ultra-sonic mode. These modes are configured by the MODE pin as follows.

- MODE pin = logic low: PFM mode
- MODE pin = logic high: FPWM mode
- MODE pin = floating: ultrasonic mode

To reduce power consumption, the status of the MODE pin is read during startup and then latched. Once the device has started operating, any changes to the MODE pin are ignored.

7.3.2.1 PFM Operation

To increase efficiency across a wide range of operating conditions, the device automatically changes from pulse-width modulation (PWM) at medium and high output currents to pulse-frequency modulation (PFM) at low output currents.

- During PWM operation, the device switches continuously and adjusts the duty cycle of each switching cycle to regulate the output voltage.
- During PFM operation, the device switches with a single pulse, separated by periods when the device does not switch. PFM operation increases efficiency at low output currents because when the device does not switch, there are no switching losses and most of the internal circuitry is disabled, which reduces quiescent power consumption. A comparator compares the output voltage of the error amplifier to a predefined PFM threshold voltage.

To enable PFM mode, pull the MODE pin to logic low.

Table 7-1. Forced-PWM versus PFM Performance Comparison

PERFORMANCE PARAMETER	BEST OPERATING MODE
Low-power efficiency	PFM
Medium- and high-power efficiency	No difference
DC Output voltage accuracy	Forced-PWM
Transient response	Forced-PWM
Output voltage ripple	Forced-PWM

7.3.2.2 Forced-PWM Operation (FPWM)

During forced-PWM operation, the device uses PWM for all operating conditions. Forced-PWM operation has lower output voltage ripple and better transient response than power-save mode operation, but lower efficiency at low output currents (see Table 7-1).

Note that the device inhibits forced-PWM operation during start-up (that is, until the converter output has reached power-good for the first time).

To enable FPWM mode, pull the MODE pin to logic high.

7.3.2.3 Ultra-sonic Mode Operation

During PFM operation, the time between switching changes with the operating conditions. Because the ceramic capacitors typically used with the device are piezoelectric, certain operating conditions can cause audible noise. The device has an ultra-sonic mode feature that forces the frequency of the switching to be outside the audible range. Note that the power conversion efficiency of the device can be slightly reduced when the ultra-sonic mode is enabled at light load.

To enable ultra-sonic mode, make the MODE pin floating.

7.3.3 Undervoltage Lockout (UVLO)

The input voltage of the VIN pin is continuously monitored if the device is not in shutdown mode. UVLO only stops or starts the converter operation. UVLO avoids a brownout of the device during device operation. In case the supply voltage on the VIN pin is lower than the negative-going threshold of UVLO, the converter stops its operation. If the supply voltage on the VIN pin recovers to be higher than the UVLO rising threshold, the converter returns to operation.

7.3.4 Enable and Soft Start

When the input voltage is above the UVLO threshold and the EN pin is pulled above 0.82V, the device is enabled.

To minimize inrush current and output voltage overshoot during start-up, the device has a soft-start function. When the output voltage is below 1.2V, the device switch peak current limit is clamped to 3A typical.

7.3.5 Protection Functions

7.3.5.1 Input Voltage Protection (IVP)

Under certain operating conditions, current can flow from the output of the device to the input. For example, this kind of current flow from the output to the input can occur during dynamic voltage scaling when the output ramps down to a lower voltage and the VOUT pin sinks current from the output capacitor. Under such conditions, if the voltage source supplying the device cannot sink current, the voltage on the VIN pin can rise uncontrollably.

To make sure the input voltage stays within the permitted range, the device stops switching if the voltage on the VIN pin is greater than 5.75V. The device automatically starts to switch again when the voltage on the VIN pin is less than 5.65V.

7.3.5.2 Output Voltage Protection (OVP)

The devices incorporate output overvoltage protection to help prevent damage to the devices. When the output voltage threshold 5.75V is reached on the VOUT pin, the protection disables the converter power stage and makes the switching nodes high impedance. The device automatically starts to switch again when the voltage on the VOUT pin is less than 5.65V.

7.3.5.3 Current Limit Mode and Overcurrent Protection

The device has a clamp circuit which limits the switch current in the event of an overload.

Overloads increase the power dissipation in the device, which increases its temperature. If the device becomes too hot, the thermal shutdown function turns off the converter. When the device cools down, the thermal shutdown function automatically turns on the converter again. Thus, under a permanent overload condition, the device can periodically turn on and off, as it cools down and then heats up.

7.3.5.4 Output Short Circuit Protection (Hiccup)

The device implements the output short-circuit protection by entering hiccup mode. After soft startup time, the device monitors the output voltage. Whenever the output short circuit happens, causing the output voltage below 1.2V and switch current limit is triggered for 2ms (typical), the device shuts down the switching for 74ms (typical) and then repeats the soft start. The hiccup mode helps reduce the total power dissipation on the device in the output short-circuit or overcurrent condition.

7.3.5.5 Thermal Shutdown

The device has a thermal shutdown function which turns off the converter if the junction temperature is greater than 165°C. The device automatically turns on the converter again when the junction temperature is less than 145°C.

7.3.6 Power Good

The device has a power-good function which indicates if the output of the DC/DC converter is in regulation or not. The device detects a power-good condition when the output voltage is greater than 95% of its nominal value and detects a power-not-good condition when the output voltage is less than 90% of its nominal value.

When a power-not-good condition occurs, the device sets the PG pin to logic low.

The PG signal is valid after a delay of 250µs (typ), when the voltage at the VIN pin is above the UVLO rising and the EN pin is pulled logic high, and the device remains active.

7.3.7 Load Disconnect

During device shutdown, the input is disconnected from the output. This disconnection between the output and the input prevents any current flow from the output to the input or from the input to the output.

7.3.8 Output Discharge

The TPS638221 provides an active pull down current to quickly discharge output when the EN pin is logic low. The output discharge function makes the power on and off sequencing smooth. Pay attention to the output discharge function if use this device in applications such as power multiplexing, because the output discharge circuitry creates a constant current path between the multiplexer output and the ground.

The TPS638221 also provides a discharge current when the VIN UVLO falling threshold is triggered and the load is not ultra-light. The discharge circuit works until VIN falls to around 1V.

7.4 Device Functional Modes

The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.

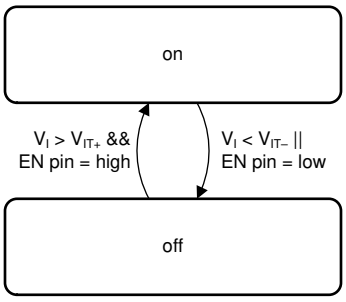


Figure 7-5. Device Functional Modes

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS63822 and TPS638221 devices are low quiescent current, high efficiency, high current buck-boost converters, designed for applications where the input voltage is higher, lower, or equal to the output voltage. The valley inductor current in the switches is limited to a typical value of 6.5A.

8.2 Typical Applications

8.2.1 3.3V Output Power Supply

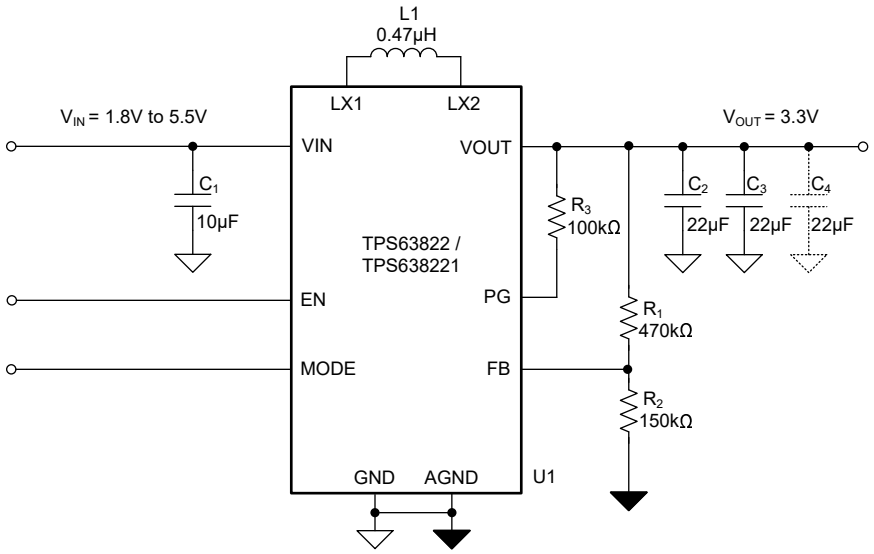


Figure 8-1. Typical Application Schematic

8.2.1.1 Design Requirements

This example uses the design parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETER	SYMBOL	EXAMPLE VALUE
Input voltage	V_I	2.0V to 5.5V
Output voltage	V_O	3.3V
Output current	I_O	up to 4A (when $V_I \geq 3.0V$)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

Ti recommends to use the TPS63822 and TPS638221 devices with 0.47µH inductor. For high efficiencies, use an inductor with a low DC resistance (DCR) and low core losses.

The saturation current of the inductor must be greater than the maximum inductor current in the application. To include sufficient margin for worst-case and transient operating conditions, use an inductor with saturation

current that is at least 20% higher than the maximum inductor current in the application. The maximum current in the inductor occurs when the device operates in boost mode and the following is true:

- The input voltage is at the minimum value.
- The output voltage is at the maximum value.
- The output current is at the maximum value.

To calculate the maximum inductor current, first use Equation 1 to calculate the maximum duty cycle during boost operation (which is when the maximum inductor current occurs).

$$D = \frac{V_O - V_I}{V_O} \quad (1)$$

where

- D is the duty cycle
- V_I is the input voltage
- V_O is the output voltage

Next, use Equation 2 to calculate the maximum inductor current.

$$I_{LM} = \frac{I_O}{\eta(1 - D)} + \frac{DV_I}{2fL} \quad (2)$$

where

- I_{LM} is the peak inductor current
- I_O is the output current
- η is the converter efficiency (use the value from the application curves or assume 90%)
- D is the duty cycle (calculated with)
- V_I is the input voltage
- f is the switching frequency (assume 1.5MHz)
- L is the inductance (use 0.47µH)

To include enough margin for transient conditions, use an inductor with a saturation current rating at least 20% higher than the calculated maximum current.

8.2.1.2.2 Output Capacitor Selection

TI recommends a minimum output capacitance (including DC bias effects) of 14µF. Two 22µF, 10V ceramic capacitors are deigned for typical applications with V_{IN} ≥ 2.6V, V_{OUT} = 3.3V, I_{OUT} ≤ 2.0A. For higher V_{OUT} or bigger I_{OUT}, three 22µF or two 47µF ceramic capacitors are suitable. To minimize switching noise on the output, connect a small ceramic capacitor (100nF is a typical value) in parallel to the two main output capacitors and place the small ceramic capacitor closest to the VOUT pin. Smaller capacitors have lower parasitic inductance and are more effective at filtering high frequencies than the two main output capacitors.

Make sure that the effective capacitance is given according to the recommended value in Recommended Operating Conditions. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a trade-off between size and transient behavior as higher capacitance reduces transient response overshoot and undershoot and increases transient response time. Table 8-2 lists possible output capacitors.

Table 8-2. List of Recommended Capacitors

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER(1)	SIZE (METRIC)
22	10	4	GRT188R61A226ME13D	Murata	0603 (1608)
47	10	4	LMK316ABJ476ML-T	Taiyo Yuden	1206 (3216)

(1) See the *Section 9.1.2*.

8.2.1.2.3 Input Capacitor Selection

TI recommends a minimum input capacitance (including DC bias effects) of 5µF. A 10µF, 6.3V or 22µF, 10V ceramic capacitor is designed for typical applications. If the input supply is located more than a few centimeters from the converter, add additional bulk capacitance (a 47µF electrolytic or tantalum capacitor is a typical choice).

Table 8-3. List of Recommended Input Capacitors

CAPACITOR [µF]	VOLTAGE RATING [V]	ESR [mΩ]	PART NUMBER	MANUFACTURER	SIZE (METRIC)
10	6.3	4	GRM188R60J106ME84D	Murata	0603 (1608)
22	10	4	GRT188R61A226ME13D	Murata	0603 (1608)

8.2.1.2.4 Setting the Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 800mV nominal.

Keep the low-side resistor R2 (between FB and GND) below 200kΩ. The high-side resistor (between FB and VOUT) R1 is calculated with Equation 3.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) \quad (3)$$

where

- V_{FB} = 800mV

When FB is connected to AGND, the output voltage is fixed at 3.3V.

Table 8-4. Resistor Selection For Typical Output Voltages

V_{OUT}	R1	R2
3.3V	470kΩ	150kΩ
5V	680kΩ	130kΩ

8.2.1.3 Application Curves

Table 8-5 lists the components that were used for the measurements contained in the following pages.

Table 8-5. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1	Capacitor, 10µF, 6.3V, 0603, ceramic	GRM188R60J106ME84D	Murata
C2, C3	Capacitor, 22µF, 10V, 0603, ceramic	GRT188R61A226ME13D	Murata
L1	Inductor, 0.47µH, 7.6mΩ	XFL4015-471MEC	Coilcraft
U1	Integrated circuit	TPS638221YBGR	Texas Instruments

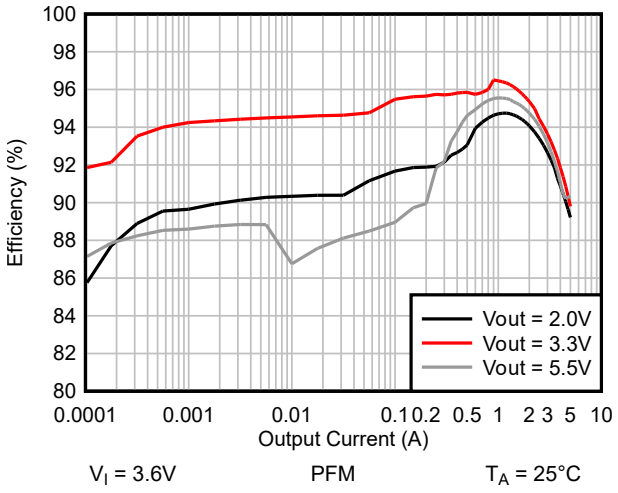


Figure 8-2. Efficiency versus Output Current

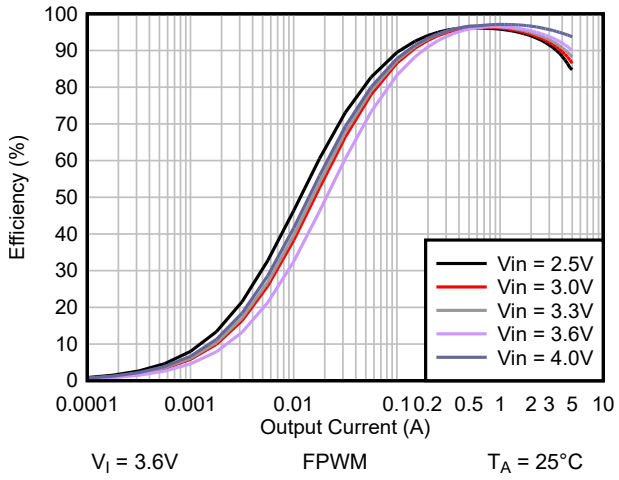


Figure 8-3. Efficiency versus Output Current

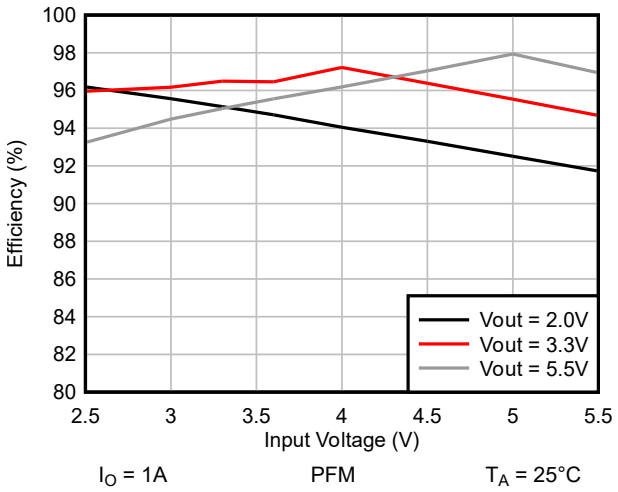


Figure 8-4. Efficiency versus Input Voltage

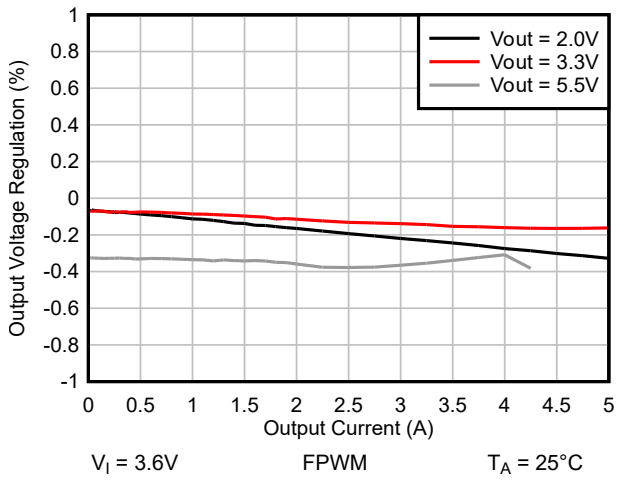
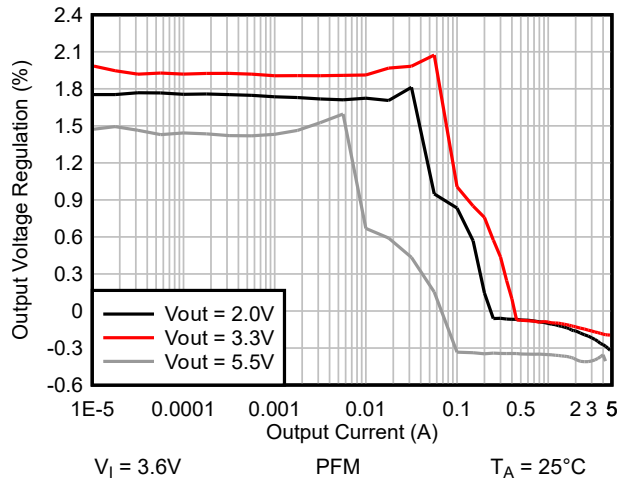


Figure 8-5. Load Regulation

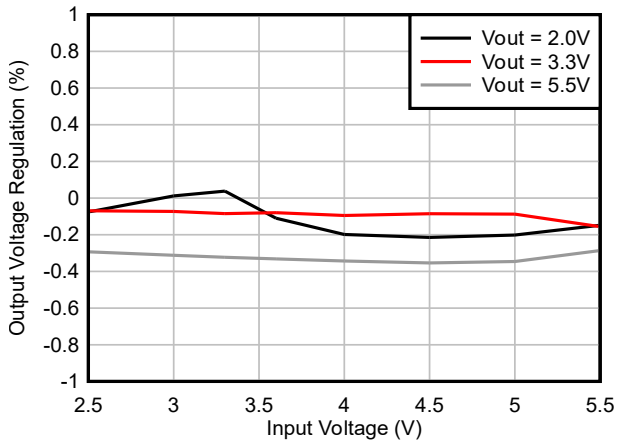
8.2.1.3 Application Curves (continued)

Table 8-5 lists the components that were used for the measurements contained in the following pages.



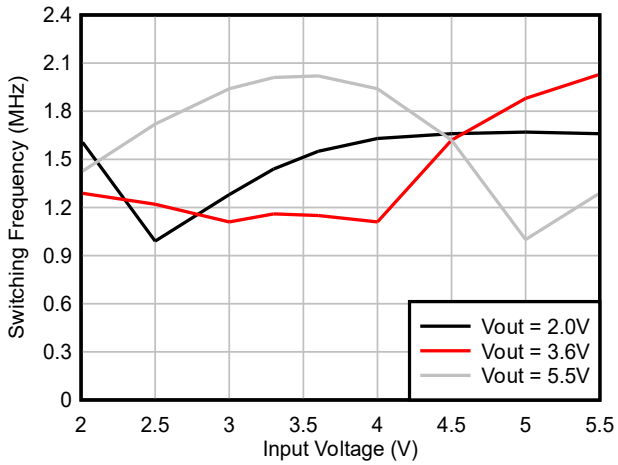
V_I = 3.6V PFM T_A = 25°C

Figure 8-6. Load Regulation



I_O = 1A FPWM T_A = 25°C

Figure 8-7. Line Regulation

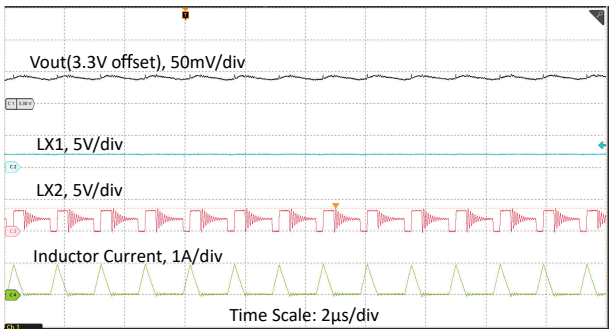


I_O = 1A FPWM T_A = 25°C
V_I rising

Figure 8-8. Switching Frequency versus Input Voltage

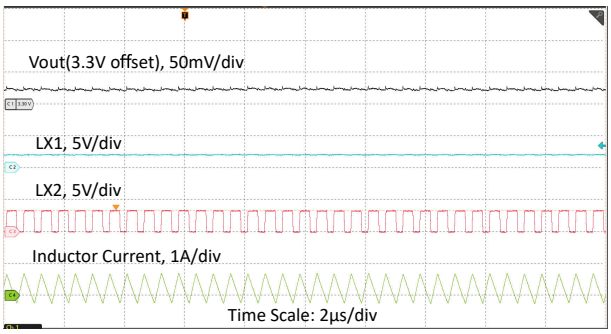
8.2.1.3 Application Curves (continued)

Table 8-5 lists the components that were used for the measurements contained in the following pages.



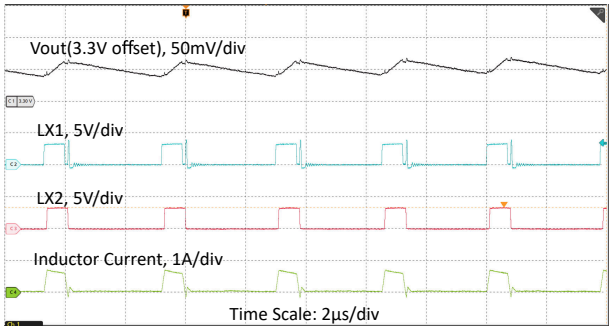
V_{IN} = 2.0V PFM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 8-9. Steady State (Boost Operation)



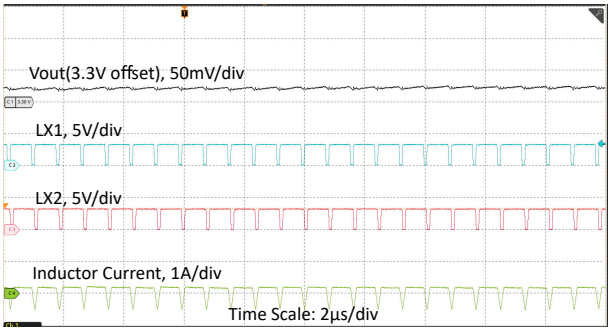
V_{IN} = 2.0V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 8-10. Steady State (Boost Operation)



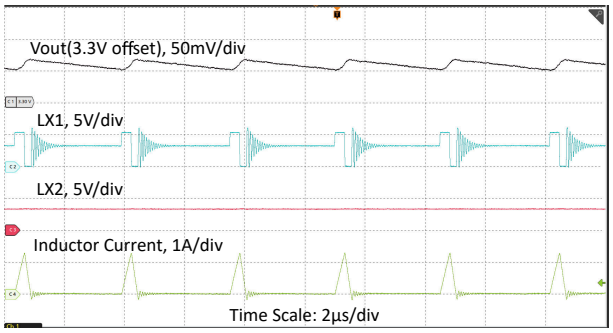
V_{IN} = 3.3V PFM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 8-11. Steady State (Buck-Boost Operation)



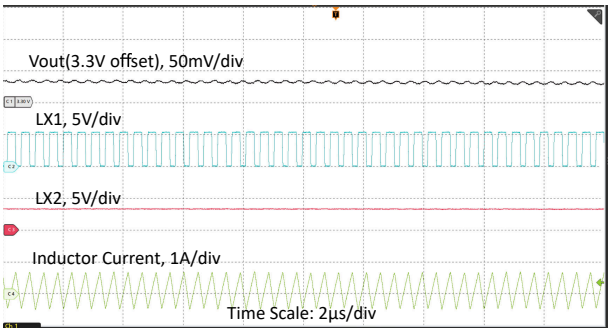
V_{IN} = 3.0V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 8-12. Steady State (Buck-Boost Operation)



V_{IN} = 5.5V PFM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 8-13. Steady State (Buck Operation)

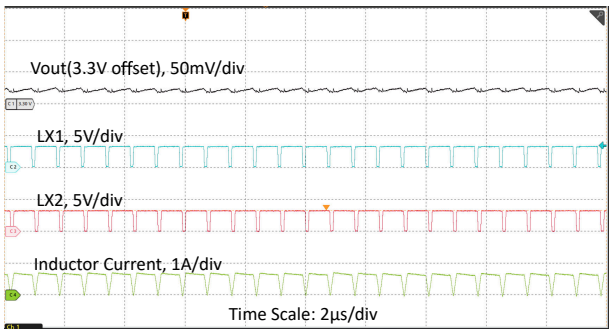


V_{IN} = 5.5V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 100mA

Figure 8-14. Steady State (Buck Operation)

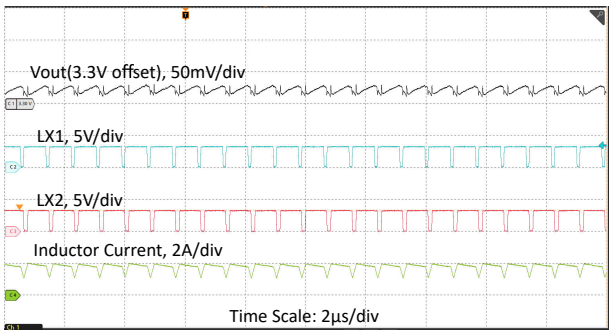
8.2.1.3 Application Curves (continued)

Table 8-5 lists the components that were used for the measurements contained in the following pages.



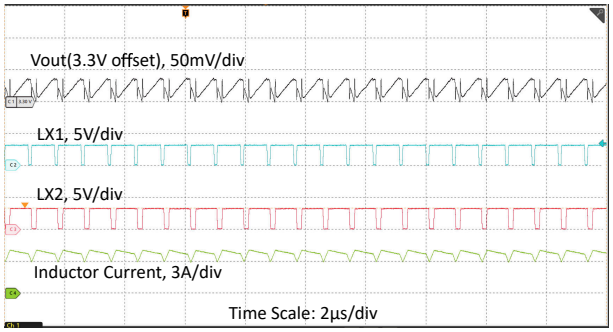
V_{IN} = 3.3V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 500mA

Figure 8-15. Steady State (Buck-Boost Operation)



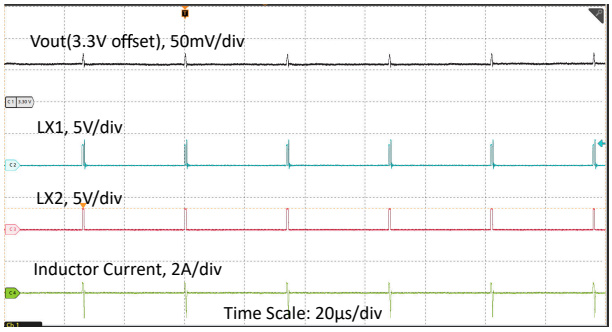
V_{IN} = 3.3V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 1.5A

Figure 8-16. Steady State (Buck-Boost Operation)



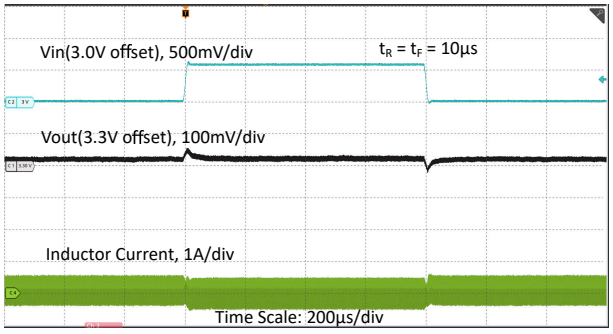
V_{IN} = 3.3V FPWM T_A = 25°C
V_{OUT} = 3.3V I_O = 3.0A

Figure 8-17. Steady State (Buck-Boost Operation)



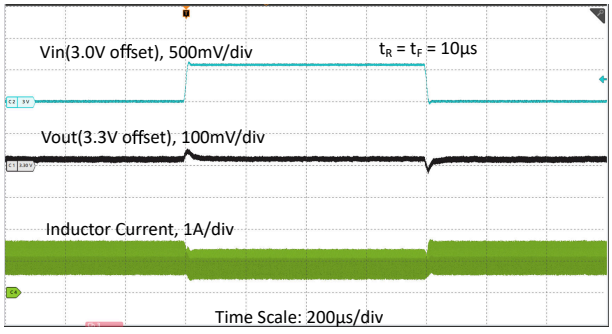
V_{IN} = 3.3V Ultra-Sonic Mode T_A = 25°C
V_{OUT} = 3.3V No load

Figure 8-18. Steady State (Buck-Boost Operation)



V_I = 3.0V to 3.6V to 3.0V PFM T_A = 25°C
V_O = 3.3V I_O = 200mA

Figure 8-19. Line Transient Response

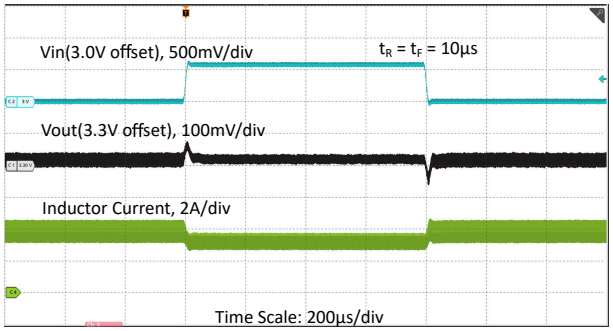


V_I = 3.0V to 3.6V to 3.0V PFM T_A = 25°C
V_O = 3.3V I_O = 1.0A

Figure 8-20. Line Transient Response

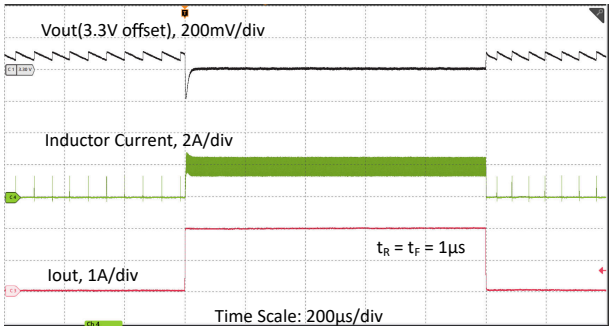
8.2.1.3 Application Curves (continued)

Table 8-5 lists the components that were used for the measurements contained in the following pages.



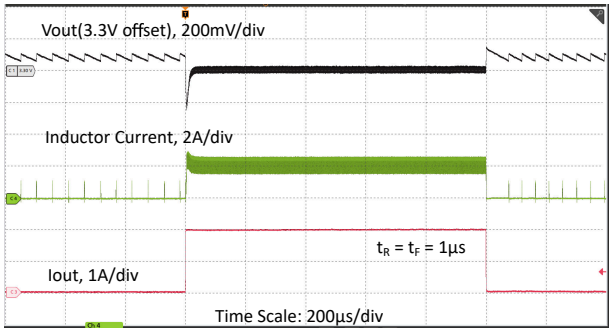
V_I = 3.0V to 3.6V to 3.0V PFM T_A = 25°C
V_O = 3.3V I_O = 3.0A

Figure 8-21. Line Transient Response



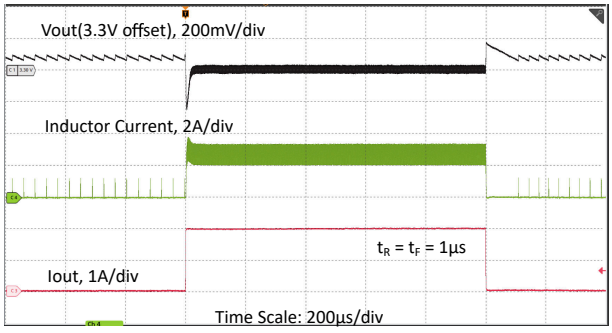
V_I = 4.2V PFM T_A = 25°C
V_O = 3.3V I_O = 10mA to 2A to 10mA

Figure 8-22. Load Transient Response (Buck)



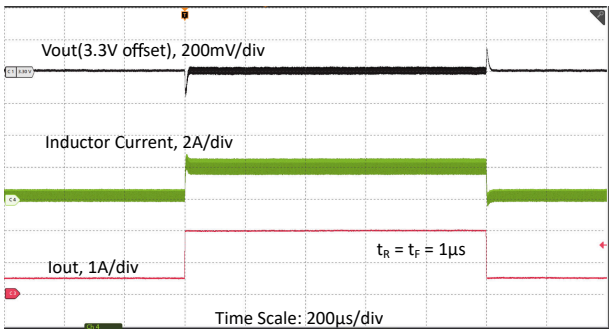
V_I = 3.3V PFM T_A = 25°C
V_O = 3.3V I_O = 10mA to 2A to 10mA

Figure 8-23. Load Transient Response (Buck-Boost)



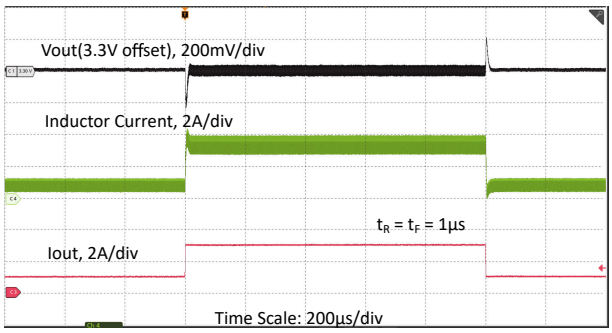
V_I = 2.6V PFM T_A = 25°C
V_O = 3.3V I_O = 10mA to 2A to 10mA

Figure 8-24. Load Transient Response (Boost)



V_I = 3.3V FPWM T_A = 25°C
V_O = 3.3V I_O = 0.5A to 2A to 0.5A

Figure 8-25. Load Transient Response (Buck-Boost)

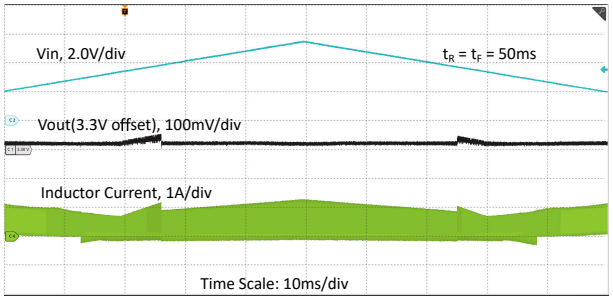


V_I = 3.3V FPWM T_A = 25°C
V_O = 3.3V I_O = 1.0A to 3A to 1.0A

Figure 8-26. Load Transient Response (Buck-Boost)

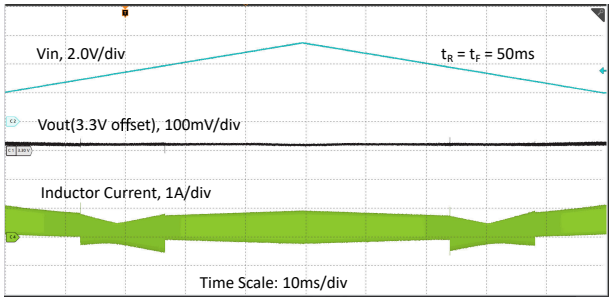
8.2.1.3 Application Curves (continued)

Table 8-5 lists the components that were used for the measurements contained in the following pages.



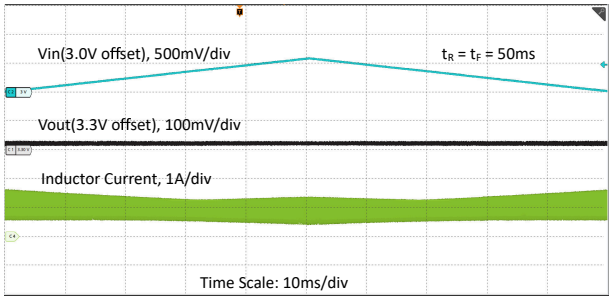
V_I = 2.0V to 5.5V to 2.0V PFM T_A = 25°C
V_O = 3.3 V R_{LOAD} = 10Ω

Figure 8-27. Line Sweep (PFM)



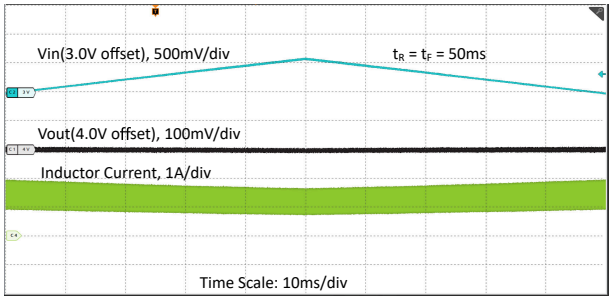
V_I = 2.0V to 5.5V to 2.0V FPWM T_A = 25°C
V_O = 3.3V R_{LOAD} = 10Ω

Figure 8-28. Line Sweep (FPWM)



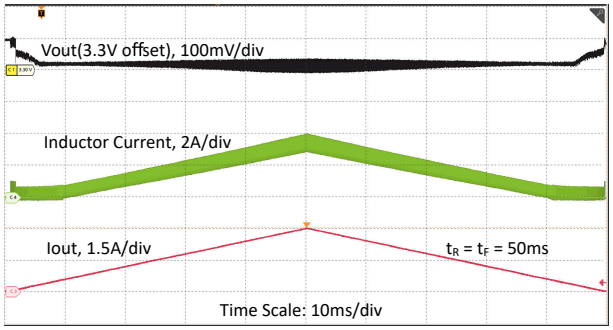
V_I = 3.0V to 3.6V to 3.0V FPWM T_A = 25°C
V_O = 3.3V I_O = 1.0A

Figure 8-29. Line Sweep (FPWM, totally in buck-boost)



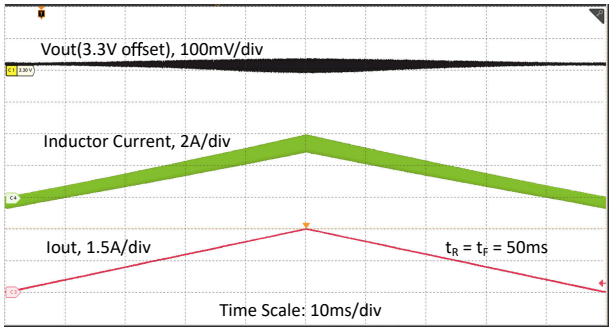
V_I = 3.0V to 3.6V to 3.0V FPWM T_A = 25°C
V_O = 4.0V I_O = 1.0A

Figure 8-30. Line Sweep (FPWM, totally in boost)



V_I = 3.3V PFM T_A = 25°C
V_O = 3.3V I_O = 0A to 3A to 0A

Figure 8-31. Load Sweep (PFM)

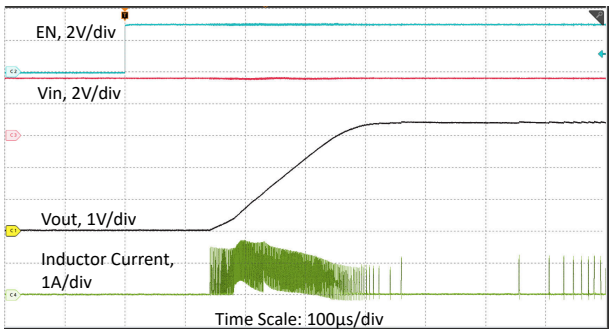


V_I = 3.3V FPWM T_A = 25°C
V_O = 3.3V I_O = 0A to 3A to 0A

Figure 8-32. Load Sweep (FPWM)

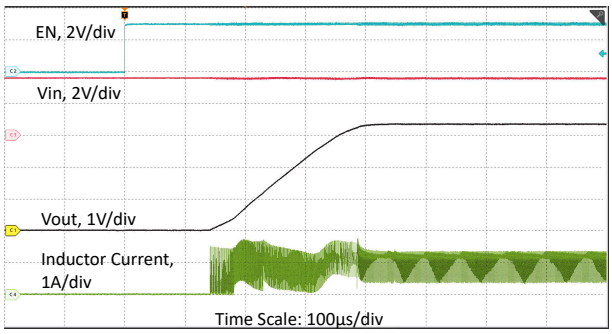
8.2.1.3 Application Curves (continued)

Table 8-5 lists the components that were used for the measurements contained in the following pages.



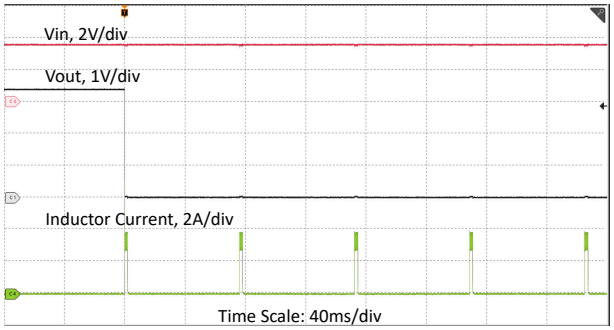
V_I = 3.6V PFM T_A = 25°C
V_O = 3.3V R_{LOAD} = 33Ω

Figure 8-33. Start-Up Waveforms (Light Load)



V_I = 3.6V PFM T_A = 25°C
V_O = 3.3V R_{LOAD} = 3.3Ω

Figure 8-34. Start-Up Waveforms (Heavy Load)



V_I = 3.6V PFM T_A = 25°C
V_O = 3.3V No load

Figure 8-35. Output Short Protection

8.3 Power Supply Recommendations

The TPS63822 and TPS638221 are designed to operate with a DC supply voltage in the range 1.8V to 5.5V. If the input supply is more than a few centimeters from the device, TI recommends adding some bulk capacitance to the ceramic bypass capacitors. A 47µF electrolytic capacitor is a typical selection for the bulk capacitance.

8.4 Layout

8.4.1 Layout Guidelines

Correct PCB layout is necessary to obtain the full performance from the device. TI recommends to follow these basic principles:

- Place input and output capacitors close to the device to minimize the input and output loop areas.
- When combining different-sized capacitors to make up the total input capacitance, place the smallest capacitor closest to the device. The same applies to the output capacitance.
- Keep PCB traces short and wide to minimize parasitic resistance and inductance.
- The sense trace connected to FB is signal trace. Keep these traces away from LX1 and LX2 nodes.
- Use the following PCB layer stack (or something similar):
  - Layer 1 (top): All components and all power traces
  - Layer 2 (inner): Signals
  - Layer 3 (inner): Signals
  - Layer 4 (bottom): Ground plane

Section 8.4.2 shows an example of the PCB layout used for all measurement data in *Application Curves*.

8.4.2 Layout Example

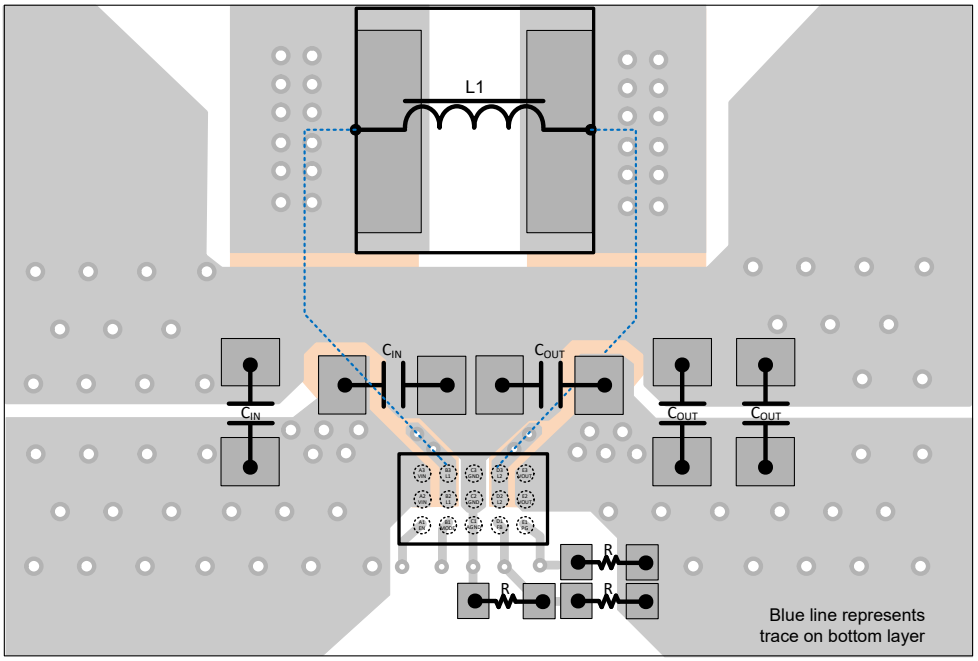


Figure 8-36. Recommended PCB Layout for the TPS638221 Device

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.1.2 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, TPS63820EVM user guide

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

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9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

9.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

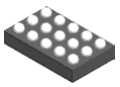
DATE	REVISION	NOTES
September 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

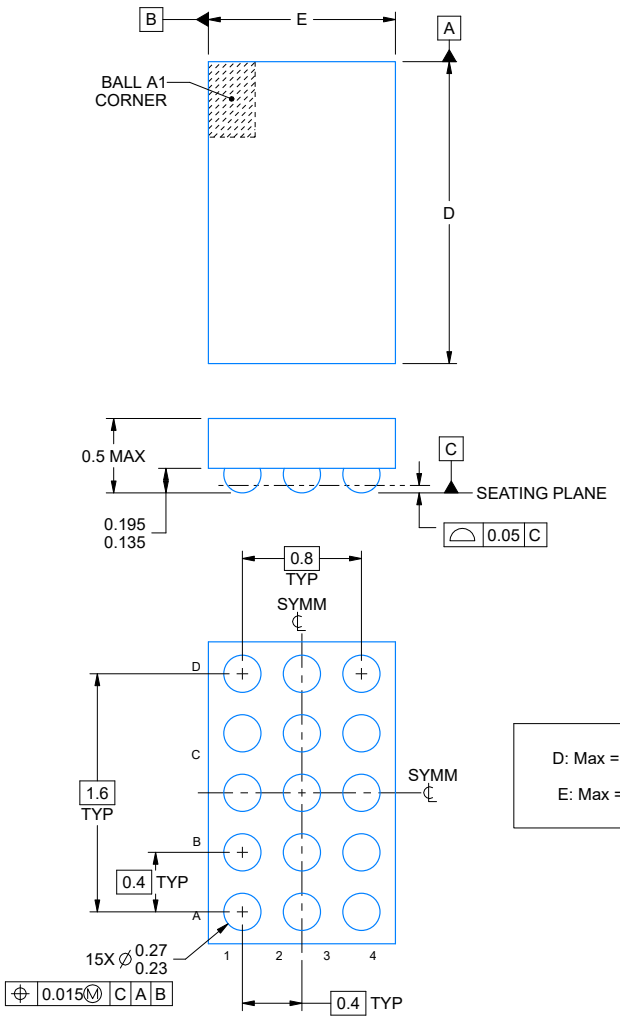
PACKAGE OUTLINE

YBG0015-C01



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

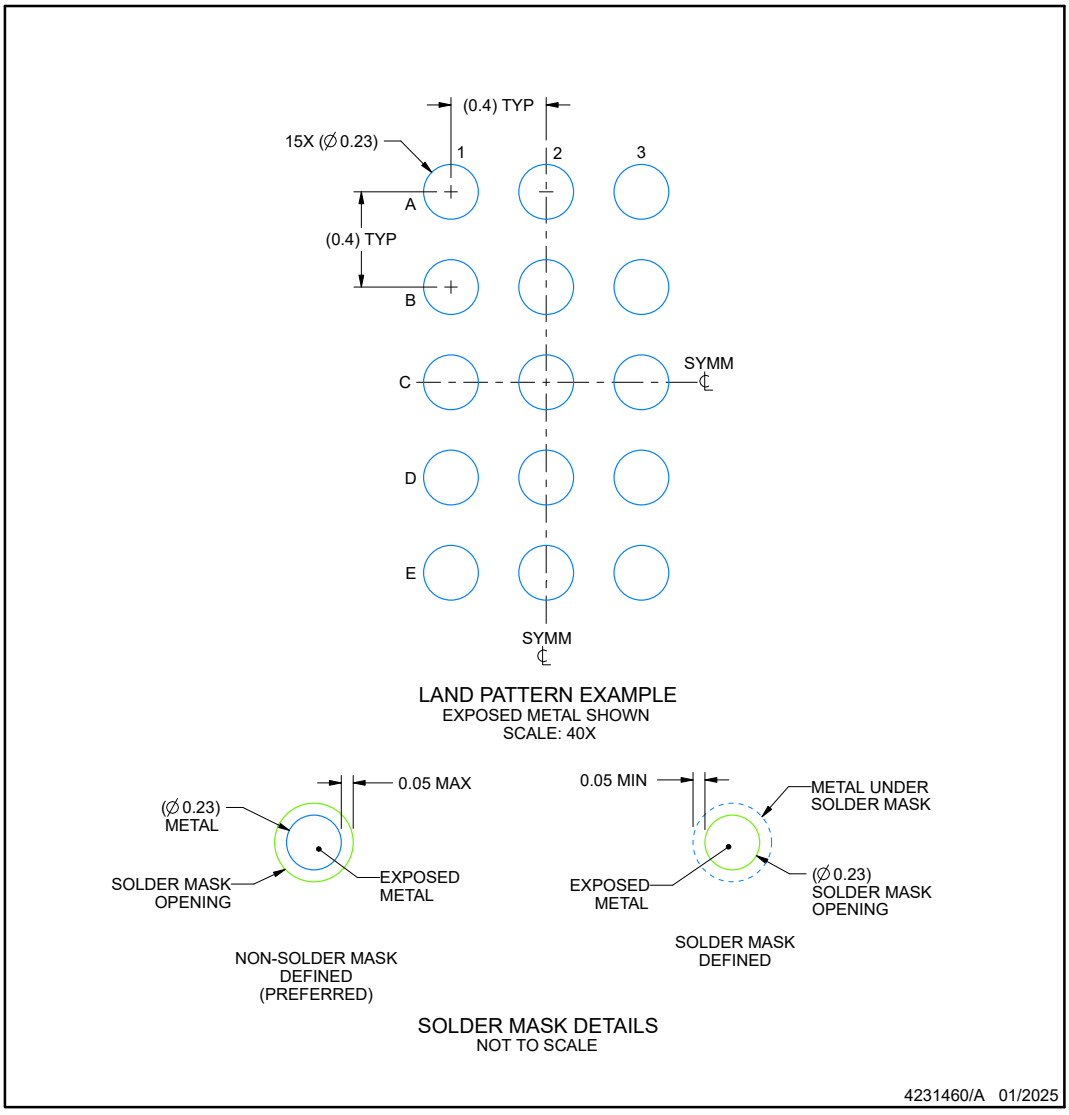
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YBG0015-C01

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



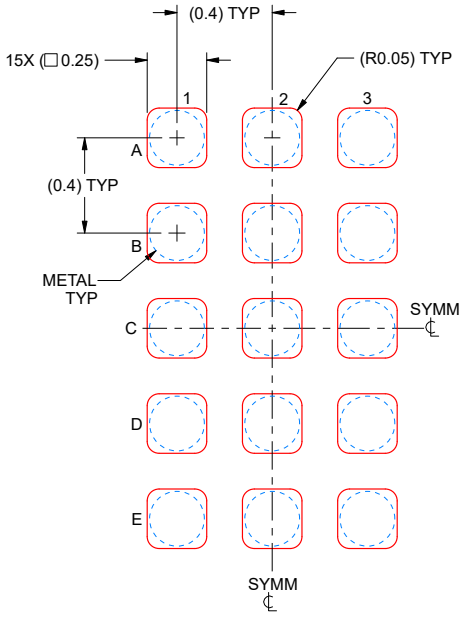
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YBG0015-C01 — **DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

4231460/A 01/2025

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS638221YBGR	Active	Production	null (null) |	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	22U

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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Last updated 10/2025