

Triple High-Voltage Scan Driver for TFT-LCD

 Check for Samples: [TPS65191](#)

FEATURES

- Triple High-Voltage Scan Driver
- Scan Driver Output Charge Share
- High Output-Voltage Level: Up to 35 V
- Low Output-Voltage Level: Down to –28 V
- Logic-Level Inputs

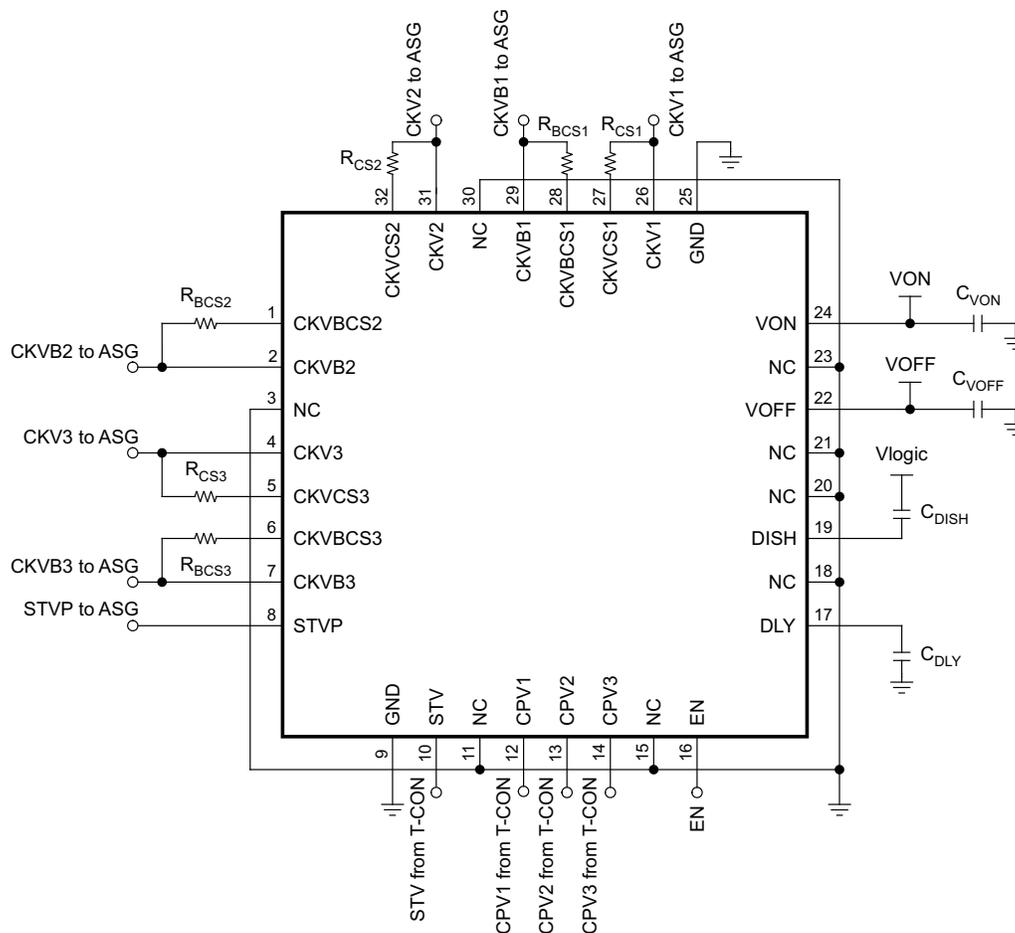
- 32-pin 5-mm × 5-mm QFN Package

APPLICATIONS

- TFT LCD Using ASG (Amorphous Silicon Gate) Technology

DESCRIPTION

The TPS65191 is a triple high-voltage scan driver to drive an ASG (amorphous silicon gate) circuit on TFT glass. Each single high-voltage scan driver receives logic-level inputs of CPVx and generates two high-voltage outputs of CKVx, CKVBx. The device receives a logic-level input of STV and generates a high-voltage output of STVP. These outputs are swings from Voff (–28 V) to Von (35 V) and are used to drive the ASG circuit and charge/discharge the capacitive loads of the TFT LCD. In order to reduce the power dissipation of device, a charge-share function is implemented. The device features discharge function, which shorts Voff to GND in order to shut down the panel faster when the LCD is turned off.



S0418-02



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

T _A	ORDERING P/N	PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65191RHBR	32-pin 5-mm × 5-mm QFN	TPS65191

(1) The RHB package has quantities of 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	VALUE	UNIT
Voltage on pins CPVx, STV	–0.3 to 5.5	V
Voltage on pins EN	–0.3 to 5.5	V
Input voltage on VON ⁽²⁾	40	V
Input voltage on VOFF ⁽²⁾	–30	V
Voltage on CKVx, CKVBx, CKVCSx, CKVBCSx	–30 to 40	V
VON–VOFF	62	V
Voltage on STVP	–30 to 40	V
Voltage on DISH	–3.6 to 5.5	V
ESD rating, HBM	2	kV
ESD rating, MM	200	V
ESD rating, CDM	700	V
Continuous power dissipation	See Dissipation Rating Table	
Operating junction temperature range	–40 to 150	°C
Storage temperature range	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	R _{θJA}	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
32-pin 5-mm × 5-mm QFN	75°C/W (Low-K board)	1.33 W	0.73 W	0.53 W

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VON	Positive high-voltage range	15		35	V
VOFF	Negative low-voltage range	–28		–3	V
VON–VOFF	VON to VOFF voltage range			60	V
f _{CPV}	CPV input frequency			150	kHz
T _A	Operating ambient temperature	–40		85	°C
T _J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

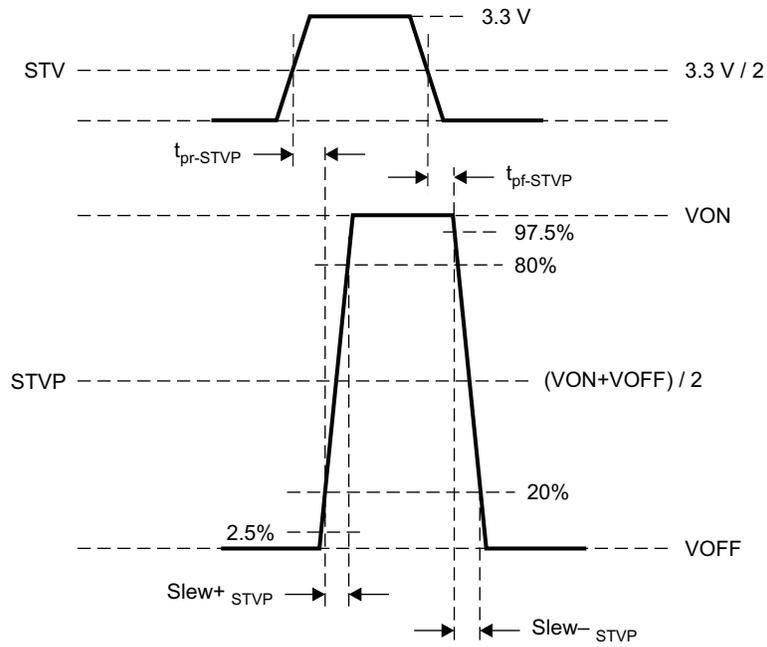
VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
IQIN	Quiescent current into VON	CPVx = GND, STV = 3.3 V		600	900	μA
	Quiescent current out of VOFF			120	200	
ISD	Shutdown current into VON	CPVx = GND, STV = 3.3 V, EN = GND		520	900	μA
	Shutdown current out of VOFF			260	400	
UNDERVOLTAGE LOCKOUT						
VUVLO	Undervoltage lockout threshold on VON	VON rising	10		13	V
		Hysteresis		250		mV
LOGIC SIGNALS EN, CPVx, STV						
VIH	High level input voltage of CPVx, STV, EN		2			V
VIL	Low level input voltage of CPVx, STV, EN				0.5	V
OUTPUT CKVx, CKVBx, STVP, CKVCSx						
VOH	Output high voltage of CKVx, CKVBx	IOH = 10 mA		VON - 0.3		V
	Output high voltage of STVP			VON - 0.8		
VOL	Output low voltage of CKVx, CKVBx	IOL = -10 mA			VOFF + 0.2	V
	Output low voltage of STVP				VOFF + 0.4	
RCHSH	Charge sharing on resistance	IChSH = 10 mA		120		Ω
DISCHARGING CIRCUIT						
RDSCHG	Discharging resistance	DISH = -2 V		1.5		kΩ
RBIAS	Resistance DISH to GND			100		kΩ
CONTROL DELAY						
VDLYREF	Reference voltage for comparator			2.9		V
IDLYREF	Delay charge current			15		μA
RDLY	Delay resistor		140	200	260	kΩ

ELECTRICAL CHARACTERISTICS (continued)

VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC CHARACTERISTICS					
Slew-	Slew rate, Slew- _{STVP}	30	55		V/ μ s
Slew+	Slew rate, Slew+ _{STVP}	20	35		V/ μ s
t _{pf}	Propagation delay, t _{pf-STVP}		40	100	ns
t _{pr}	Propagation delay, t _{pr-STVP}		30	100	ns



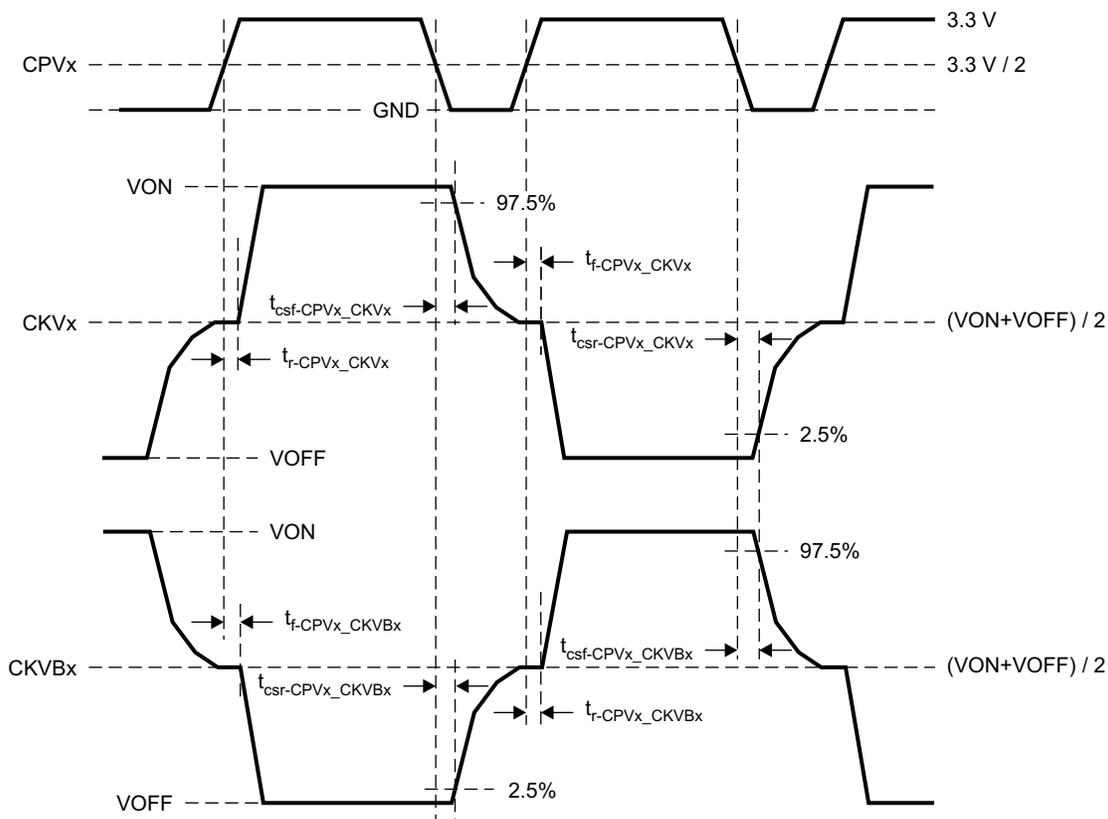
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Figure 1. Switching Characteristics of STVP

CKVx, CKVx SWITCHING CHARACTERISTICS

VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{csf}	t _{csf-CPVx_CKVx} , t _{csf-CPVx_CKVBx}	f _{CPVx} = 85 kHz, STV = GND, See Figure 2, load = 4.7 nF, R _{CS1} = R _{BCS1} = R _{CS2} = R _{BCS2} = 50 Ω		80	150	ns
t _{csr}	t _{csr-CPVx_CKVx} , t _{csr-CPVx_CKVBx}			80	150	ns
t _f	t _{f-CPVx_CKVx} , t _{f-CPVx_CKVBx}			40	100	ns
t _r	t _{r-CPVx_CKVx} , t _{r-CPVx_CKVBx}			30	100	ns



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Figure 2. Switching Characteristics of CKVx, CKVBx (STV = GND)

CKVx, CKVBx SWITCHING CHARACTERISTICS (Continued)

VOFF = -10 V, VON = 30 V, EN = 3.3 V, TA = -40°C to 85°C, typical values are at TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew+	Slew+ _{CKVx} , Slew+ _{CKVBx}	f _{CPVx} = 85 kHz, STV = 3.3 V, See Figure 3, load = 4.7 nF, R _{CSx} = R _{BCSx} = 50 Ω	50	100		V/μs
Slew-	Slew- _{CKVx} , Slew- _{CKVBx}	f _{CPVx} = 85 kHz, STV = 3.3 V, See Figure 3, load = 4.7 nF, R _{CSx} = R _{BCSx} = 50 Ω	70	130		V/μs

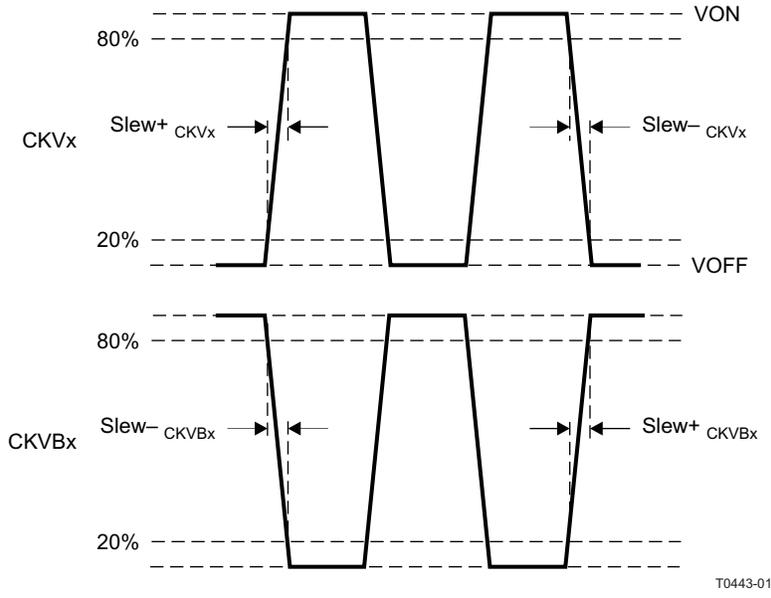
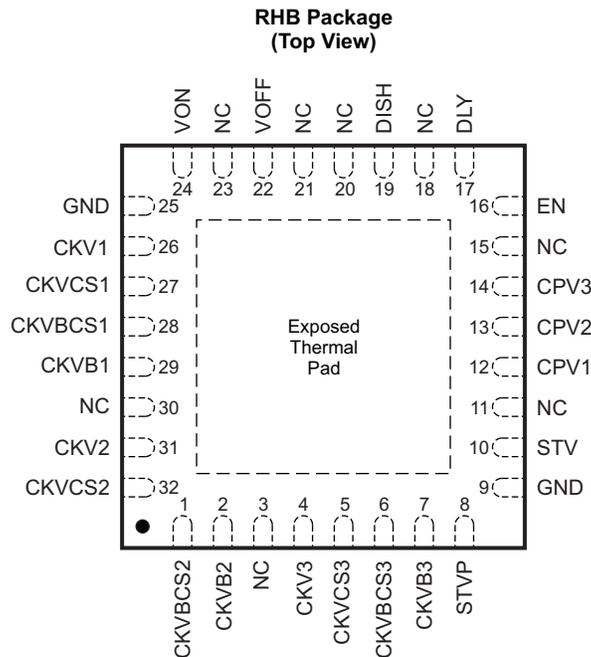


Figure 3. CKVx, CKVBx Output Rise and Fall Times (STV = 3.3 V)

DEVICE INFORMATION



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Exposed thermal pad and NC pins are recommended to be connected with ground on the PCB for better thermal dissipation.

PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
CKV1	26	O	Output vertical-scan clock 1 for ASG
CKV2	31	O	Output vertical-scan clock 2 for ASG
CKV3	4	O	Output vertical-scan clock 3 for ASG
CKVB1	29	O	Inverted-output vertical-scan clock 1 for ASG
CKVB2	2	O	Inverted-output vertical-scan clock 2 for ASG
CKVB3	7	O	Inverted-output vertical-scan clock 3 for ASG
CKVBCS1	28	I	Charge-share input for CKVB1
CKVBCS2	1	I	Charge-share input for CKVB2
CKVBCS3	6	I	Charge-share input for CKVB3
CKVCS1	27	I	Charge-share input for CKV1
CKVCS2	32	I	Charge-share input for CKV2
CKVCS3	5	I	Charge-share input for CKV3
CPV1	12	I	Input vertical-scan clock 1
CPV2	13	I	Input vertical-scan clock 2
CPV3	14	I	Input vertical-scan clock 3
DISH	19	I	VOFF discharge control
DLY	17	O	Connecting a capacitor from this pin to GND allows the setting of the start-up delay.
EN	16	I	Enable pin of device. When this pin is pulled high, the device starts up after a delay time set by DLY has passed.
GND	9, 25	–	Ground
NC	3, 11, 15, 18, 20, 21, 23, 30	–	Not connected

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
STV	10	I	Input vertical-scan start signal
STVP	8	O	Output vertical-scan start signal
VOFF	22	I	Negative low-supply voltage
VON	24	I	Positive high-supply voltage
Thermal pad		–	Not connected

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

SYSTEM PERFORMANCE			FIGURE
Start-up sequence CKVx	EN = HIGH after UVLO, C _{DLY} = 10 nF, STV = LOW		Figure 4
	EN = HIGH before UVLO, C _{DLY} = 10 nF, STV = LOW		Figure 5
Start-up sequence STVP	EN = HIGH after UVLO, C _{DLY} = 10 nF, CPVx = LOW		Figure 6
	EN = HIGH before UVLO, C _{DLY} = 10 nF, CPVx = LOW		Figure 7
OUTPUT CKVx, CKVBx and STVP			
Rise time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF		Figure 8
	STV = LOW, load = 4.7 nF		Figure 9
Fall time / propagation delay of CKVx	STV = HIGH, load = 4.7 nF		Figure 10
	STV = LOW, load = 4.7 nF		Figure 11
Rise time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF		Figure 12
Fall time / propagation delay of STVP	CPV1 = LOW, load = 4.7 nF		Figure 13
STVP output	CPV1 = HIGH		Figure 14
	CPV1 = LOW		Figure 15
CKVx, CKVBx outputs	STV = HIGH		Figure 16
	STV = LOW		Figure 17

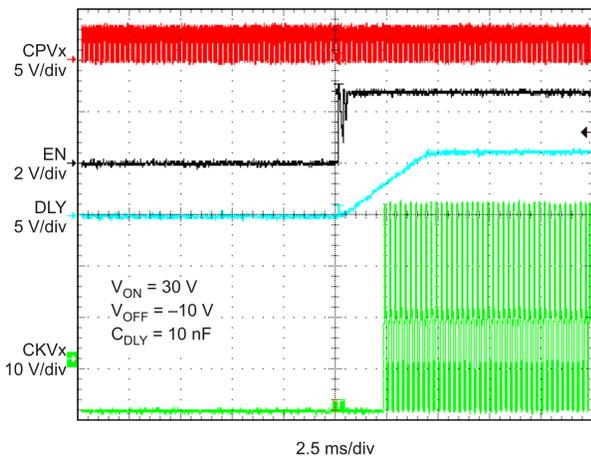


Figure 4. Start-Up Sequence CKVx, EN = HIGH After UVLO

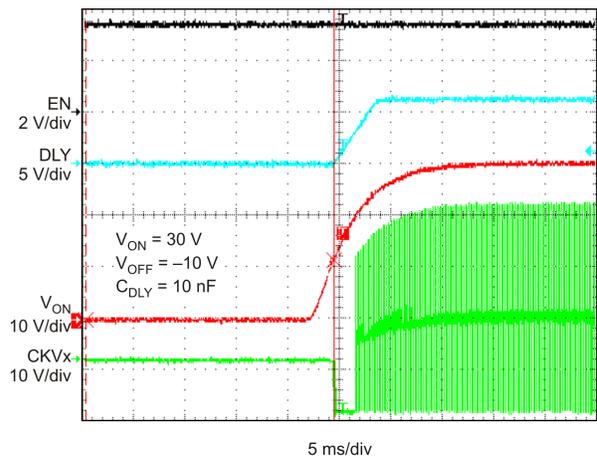


Figure 5. Start-Up Sequence CKVx, EN = HIGH Before UVLO

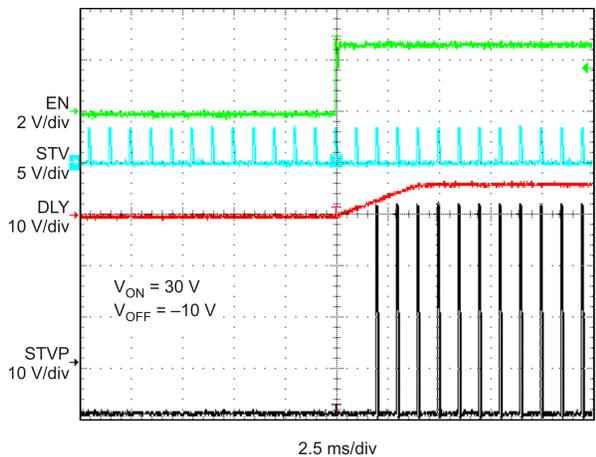


Figure 6. Start-Up Sequence STVP, EN = HIGH After UVLO

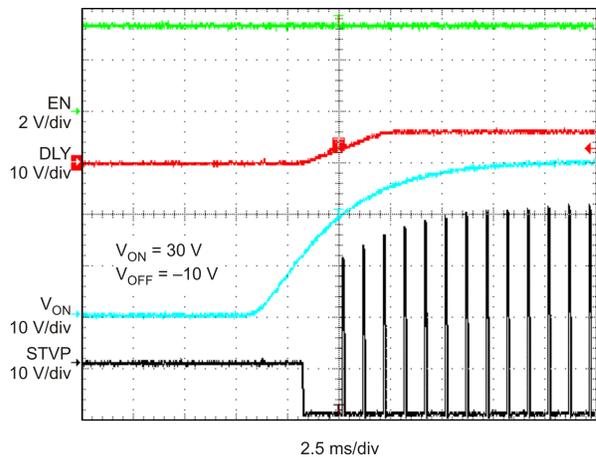


Figure 7. Start-Up Sequence STVP, EN = HIGH Before UVLO

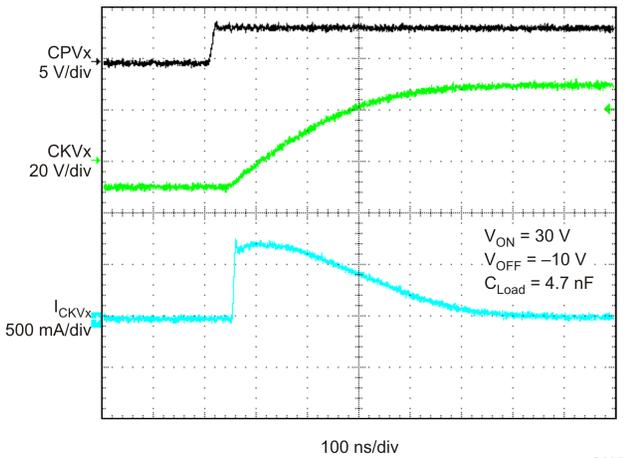


Figure 8. Rise Time / Propagation Delay of CKVx, STV = HIGH

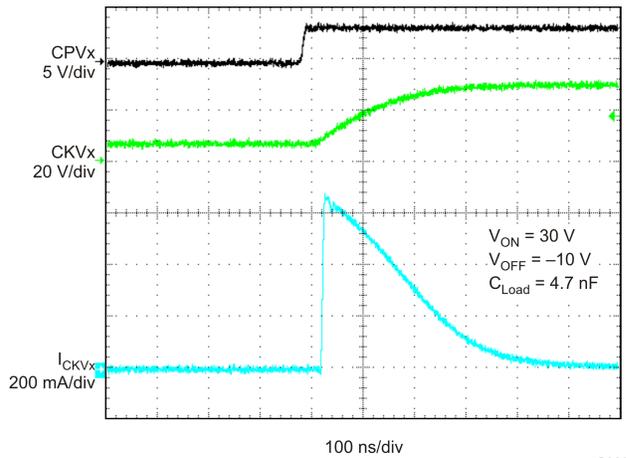


Figure 9. Rise Time / Propagation Delay of CKVx, STV = LOW

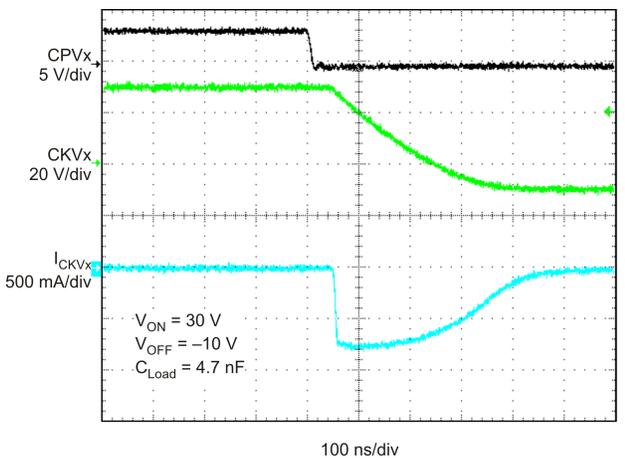


Figure 10. Fall Time / Propagation Delay of CKVx, STV = HIGH

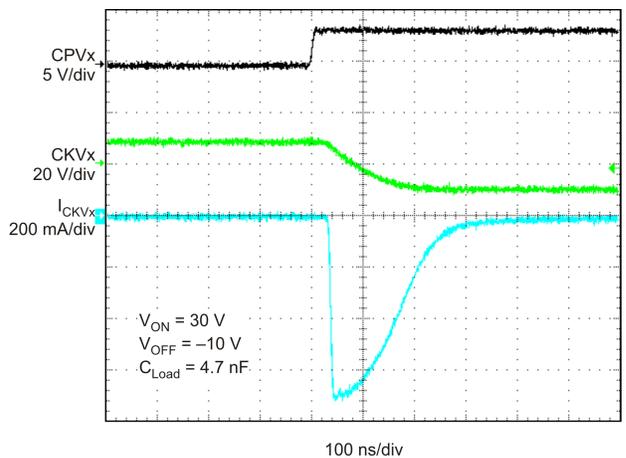


Figure 11. Fall Time / Propagation Delay of CKVx, STV = LOW

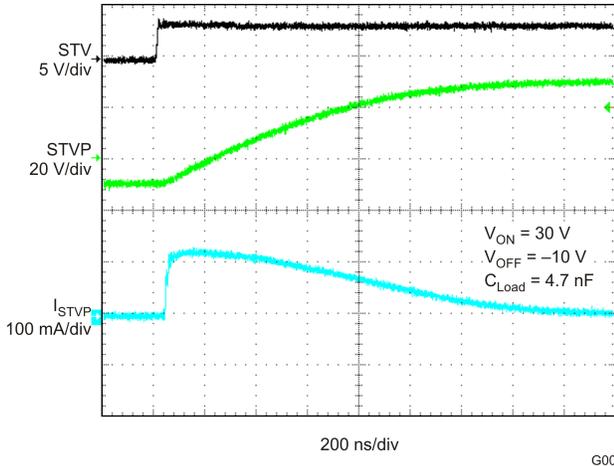


Figure 12. Rise Time / Propagation Delay of STVP, CPV1 = LOW

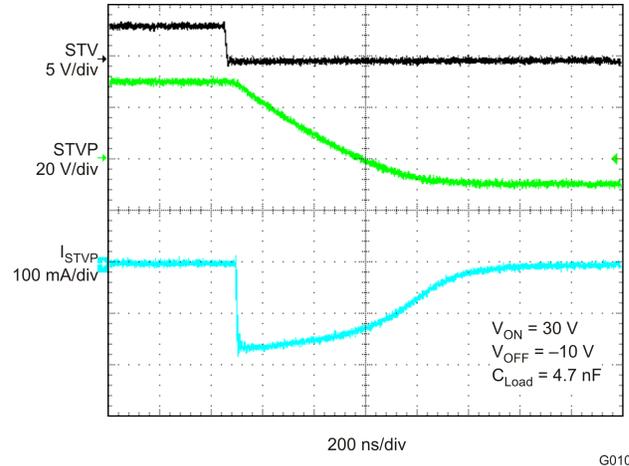


Figure 13. Fall Time / Propagation Delay of STVP, CPV1 = LOW

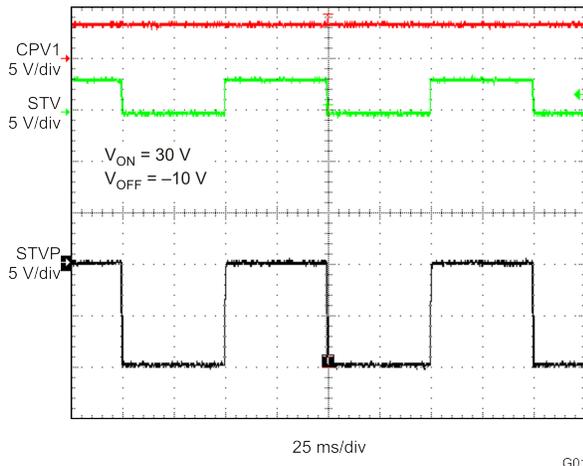


Figure 14. STVP Output, CPV1 = HIGH

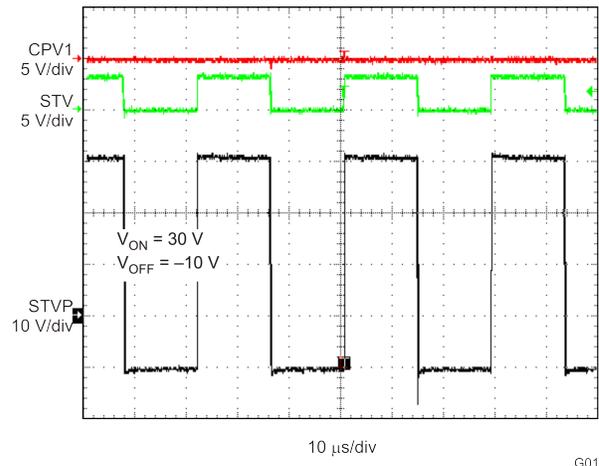


Figure 15. STVP Output, CPV1 = LOW

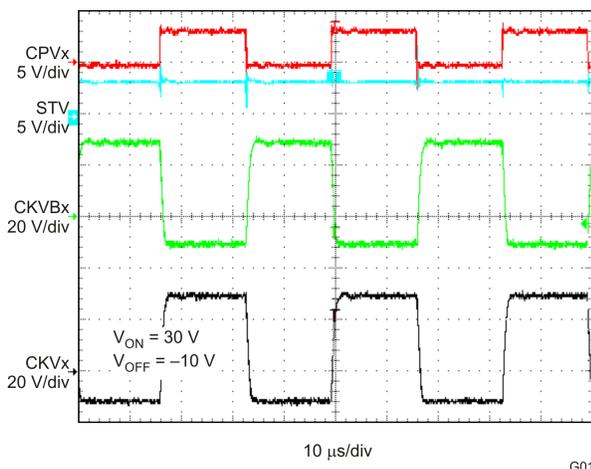


Figure 16. CKVx, CKVx Outputs, STV = HIGH

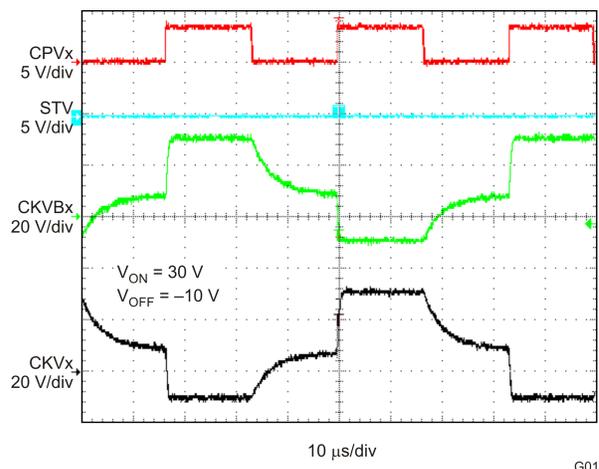
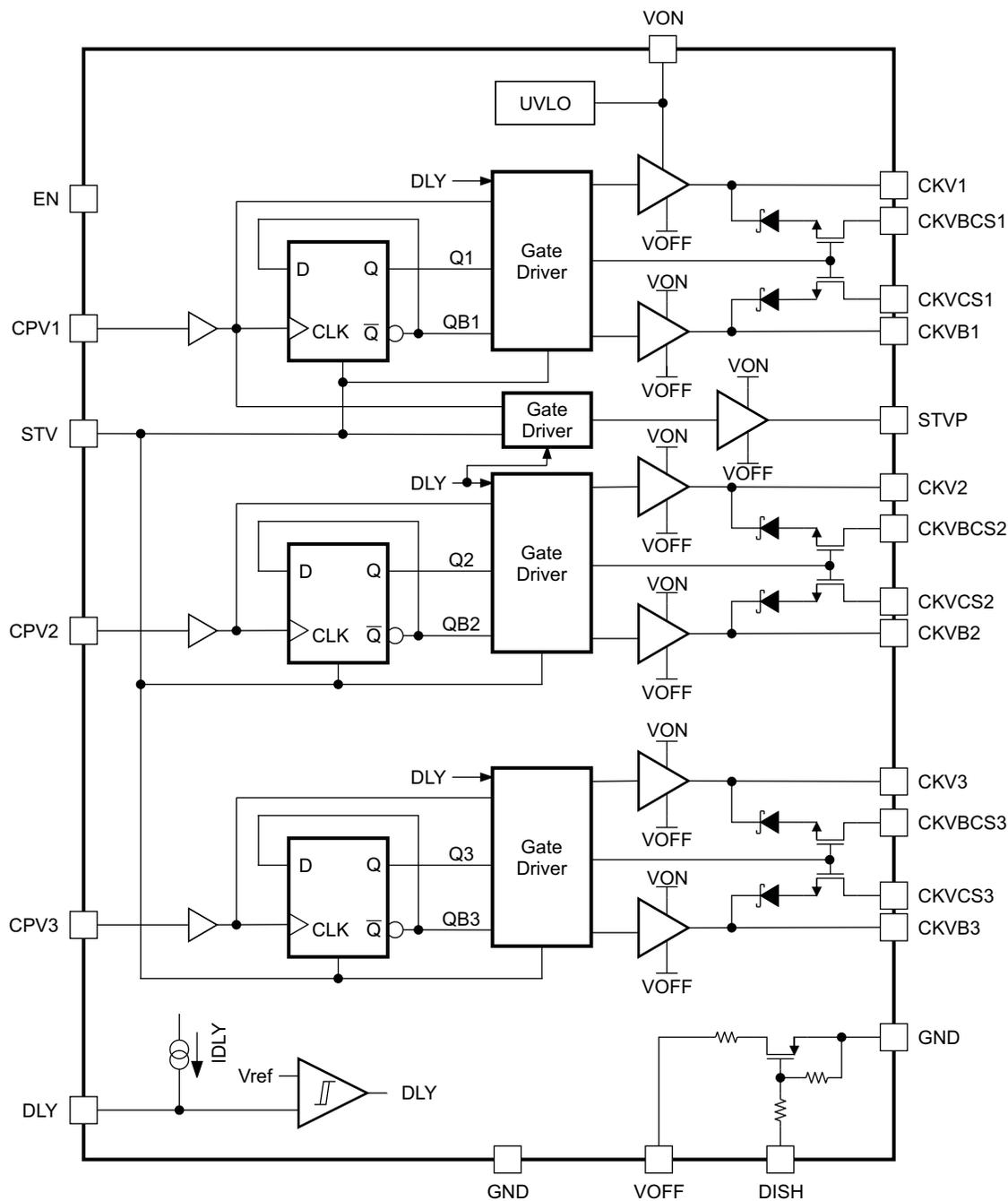


Figure 17. CKVx, CKVx Outputs, STV = LOW

BLOCK DIAGRAM



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DETAILED DESCRIPTION

UNDERVOLTAGE LOCKOUT

The device has an undervoltage lockout feature to avoid improper operation of the device when input voltage VON is low. When VON is lower than 10 V, the device shuts down, and outputs CKVx, CKVBx, and STVP enter the high-impedance state.

INPUT SIGNALS

The timing controller in the system provides input signals of TPS65191. STV is the synchronous signal for picture frames, and its frequency depends on frame rate. CPVx are the synchronous signals for horizontal lines, and their frequency depends on frame rate and vertical resolution.

OUTPUT SIGNALS

The STVP, CKVx, and CKVBx of scan-driver outputs are generated with internal switches. [Table 1](#) and [Table 2](#) show the logic diagrams of the scan-driver outputs.

Table 1. STVP Logic Diagram

INPUT		OUTPUT
STV	CPV1	STVP
LOW	Don't care	VOFF
HIGH	LOW	VON
HIGH	HIGH	High impedance

Table 2. CKVx, CKVBx, and Output Charge-Share Logic

INPUT		OUTPUT		
STV	CPVx	CKVx	CKVBx	CHARGE SHARE
LOW	LOW	High impedance	High impedance	Enable
LOW	Rising edge	Toggle state	Toggle state	Disable
LOW	HIGH	Previous state	Previous state	Disable
HIGH	LOW	VOFF	VON	Disable
HIGH	HIGH	VON	VOFF	Disable

OUTPUT CHARGE SHARE

Power dissipation can be reduced by the output charge share. [Figure 18](#) shows the current flows when the charge share is enabled. CKVCSx and CKVBCSx are charge-share inputs. When the charge share is enabled, the charge that is in the capacitor of the positive voltage line is transferred to the capacitor of the negative voltage line. Charge-sharing resistors R_{CSx} and R_{BCSx} reduce the peak current into charge-share inputs, CKVCSx and CKVBCSx, during the output charge share. These resistors also control the slope of the output charge-share waveform. The smaller R_{CSx} and R_{BCSx} , the higher the peak current into the charge-share inputs and the steeper the slope of output charge-share waveform. The power dissipation in charge-sharing resistors should be taken into consideration. With 0603 size resistors, the power rating of two in parallel is good for most applications.

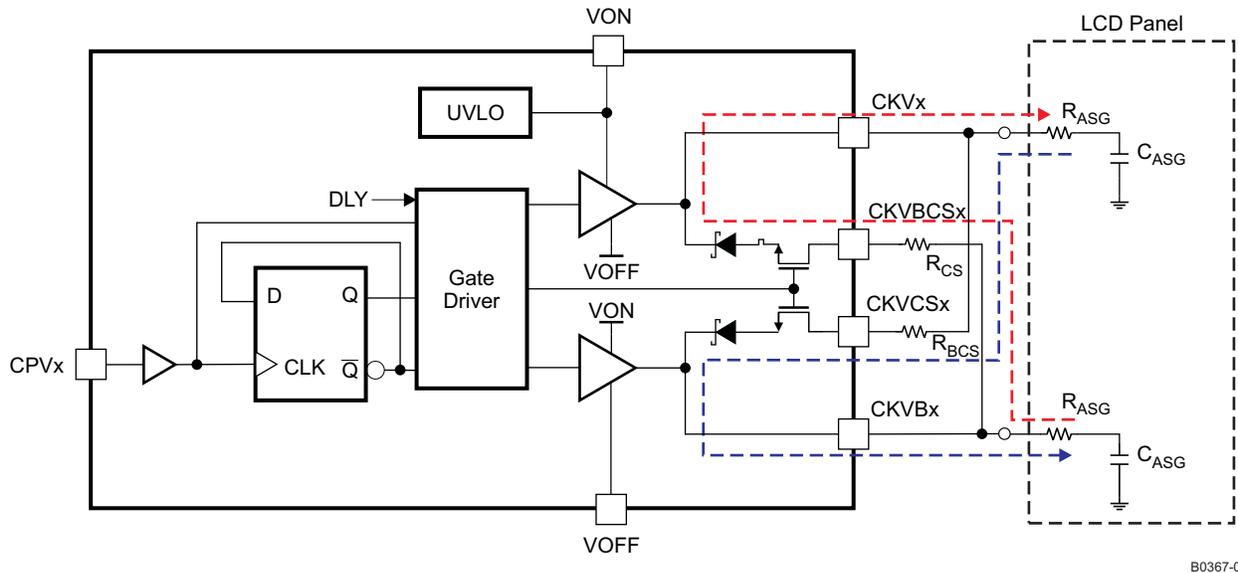


Figure 18. Single-Scan Driver Block Diagram

START-UP SEQUENCE (EN, DLY)

The TPS65191 has an adjustable start-up sequencing that is set by EN and DLY. When VON is below the UVLO threshold, all outputs are at high impedance. When EN is pulled LOW after UVLO threshold is reached, all outputs follow VOFF. Pulling EN high enables the device after a delay time set by the capacitor connected to DLY, and the delay time starts when EN = HIGH. If EN is pulled high before the UVLO threshold is reached, the delay starts when VON reaches the UVLO threshold. Pulling EN low disables the device, and outputs CKVx, CKVBx, and STVP follow VOFF as long as VON is higher than the UVLO threshold. For the typical start-up sequence, see [Figure 19](#) and [Figure 20](#).

SETTING THE DELAY TIME (DLY)

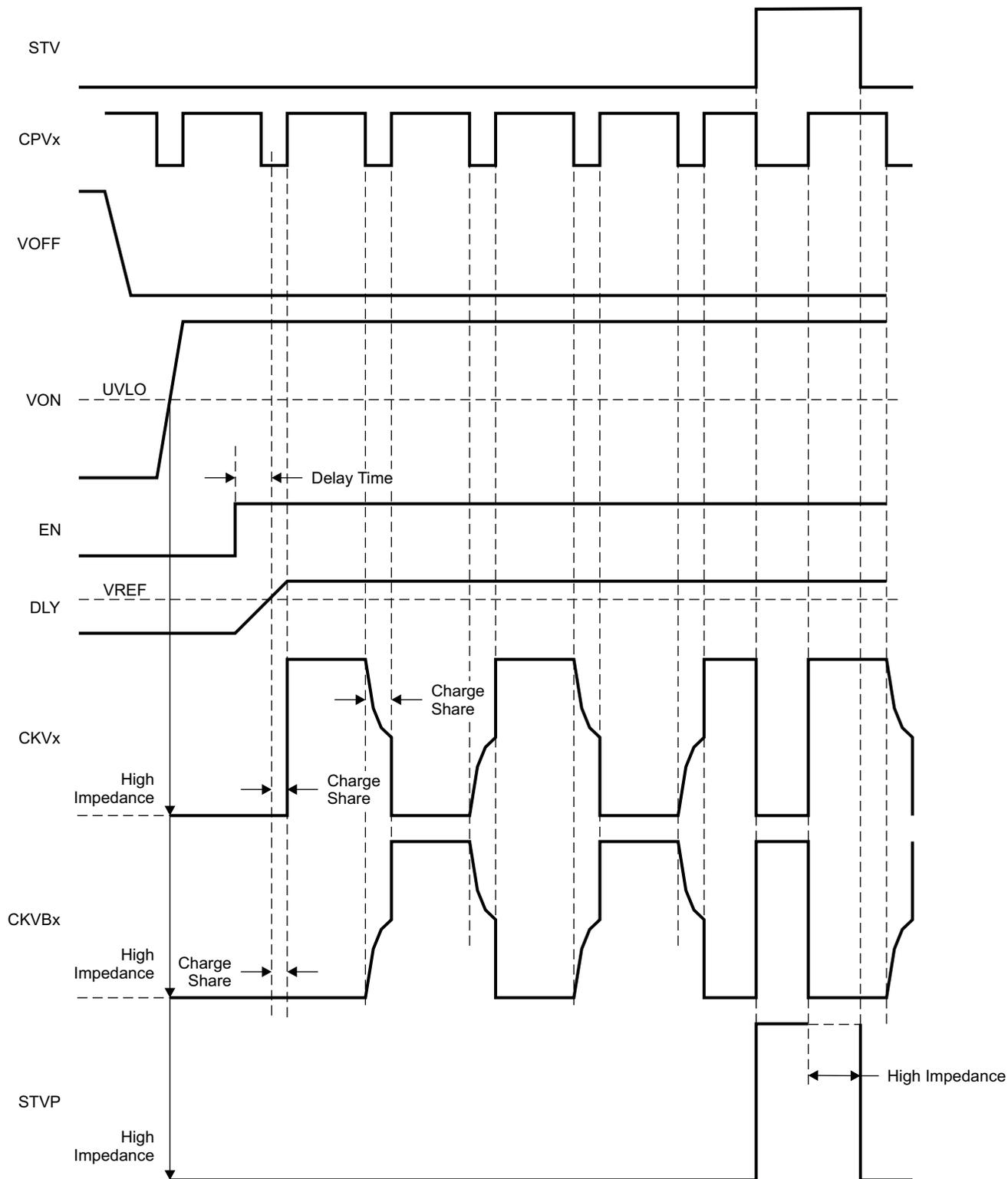
Connecting an external capacitor to the DLY pin sets the delay time. If no delay time is required, the DLY pin can be left floating. The external capacitor is charged with a constant-current source of typically 15 μ A. The delay time is terminated when the capacitor voltage reaches the internal reference voltage of 2.9 V, and the final DLY voltage on an external capacitor is maximum 8 V. The voltage rating of the external capacitor must be higher than 8 V.

The external delay capacitor is calculated using the following formula:

$$C_{DLY} = \frac{\text{Delay time}}{R_{DLY}} = \frac{\text{Delay time}}{200 \text{ k}\Omega} \quad (1)$$

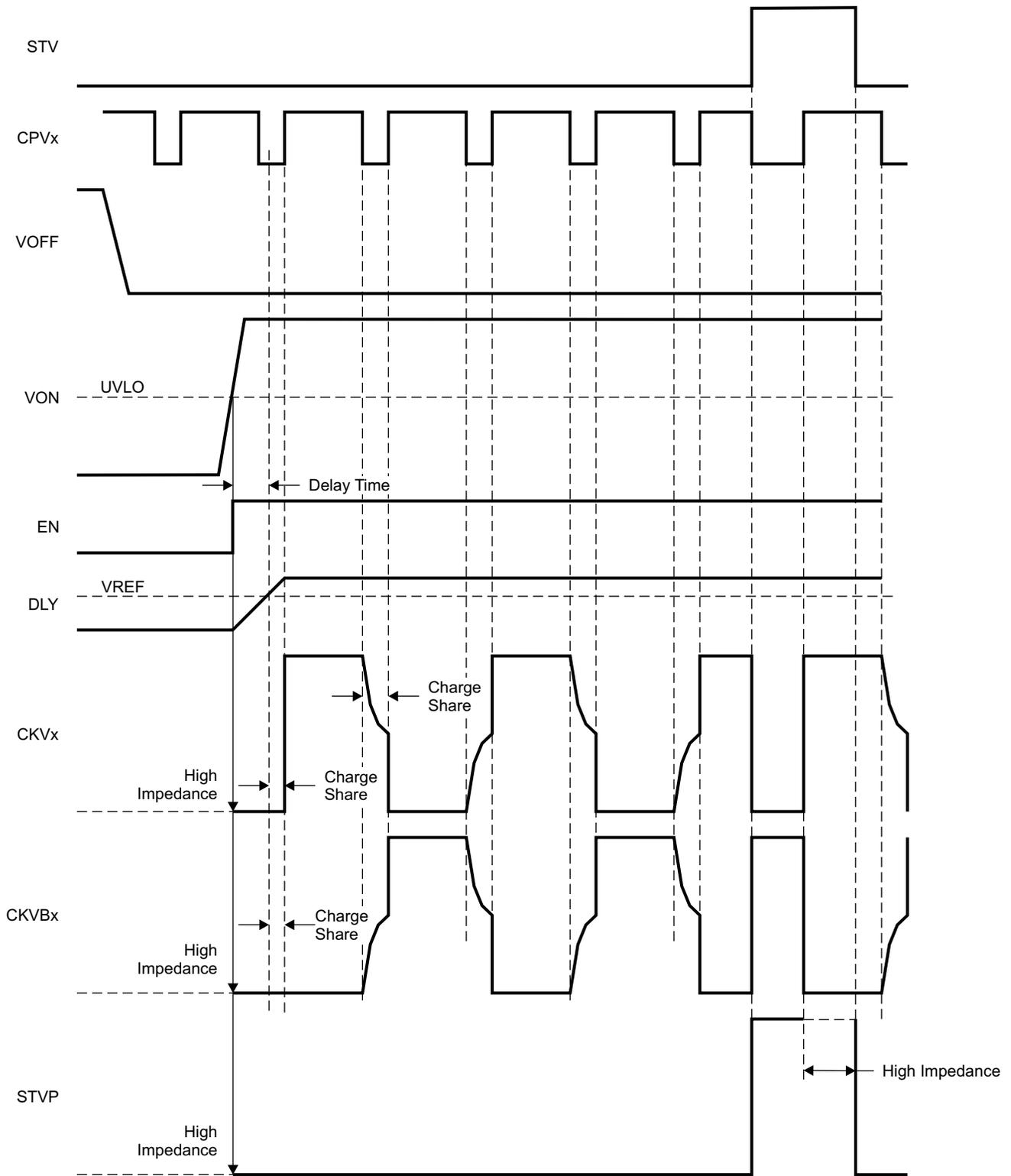
Example for setting a delay time of 10 ms:

$$C_{DLY} = \frac{10 \text{ ms}}{200 \text{ k}\Omega} = 50 \text{ nF} \approx 47 \text{ nF} \quad (2)$$



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Figure 19. Start-Up Sequence With EN = High After UVLO Threshold



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Figure 20. Start-Up Sequence With EN = High Before UVLO Threshold

TIMING DIAGRAM OF SCAN DRIVER

Figure 21 shows the typical timing diagram of the TPS65191.

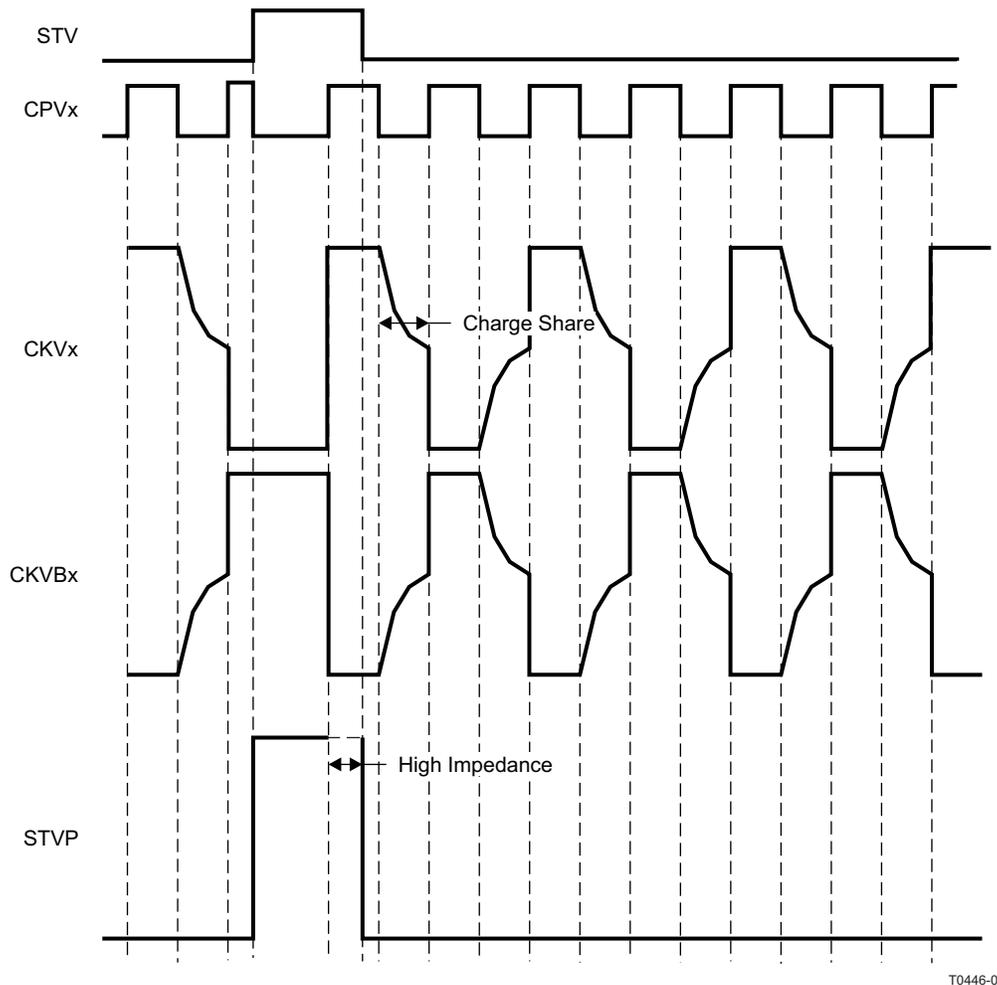


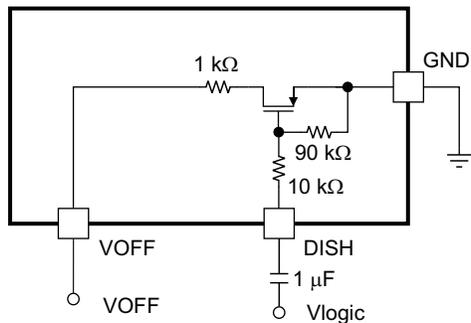
Figure 21. Scan Driver Timing Diagram

SUPPLY VOLTAGE VON and VOFF

The TPS65191 drives the capacitive load. The high peak currents should be supplied from VON on the rising edges of the outputs and VOFF on the falling edges of the outputs, respectively. Bypass capacitors of 1 μF must be placed as close as possible on both the VON and VOFF supplies. Depending on the peak current that the TPS65191 must deliver, the bypass capacitor can be bigger than 1 μF .

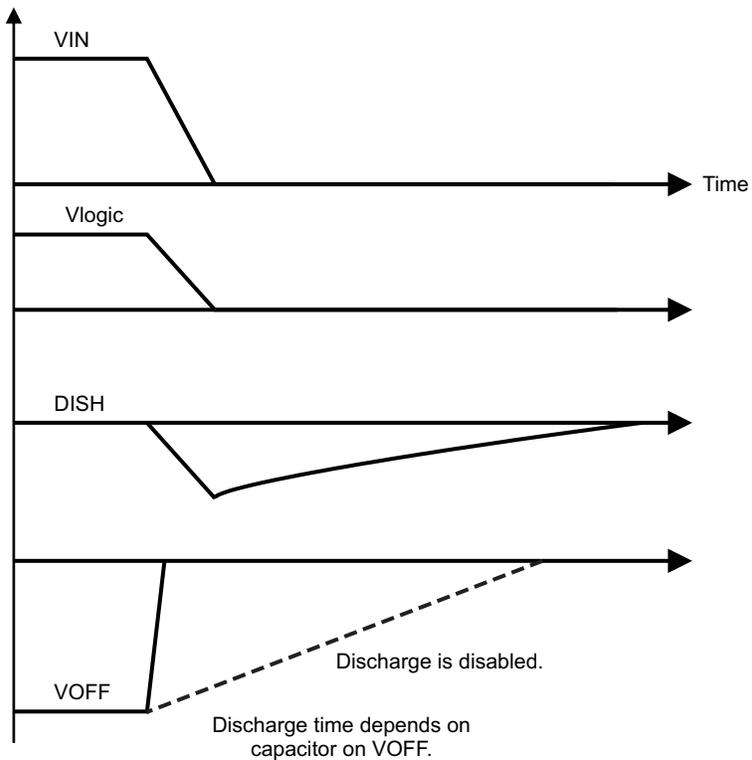
VOFF DISCHARGE

DISH controls the VOFF discharging time during the system power off. Figure 22 shows a typical application for VOFF discharge. DISH is connected to the system logic voltage through a capacitor. During the power off, the system logic voltage falls, and the voltage on DISH falls below ground level. Internal switch turns on when DISH is below -0.6V and VOFF is connected to ground through 1k Ω , which helps VOFF discharge. A 1- μF DISH capacitor is good for most applications. Figure 23 shows the typical power-off sequence of VOFF discharging. VOFF discharge can be disabled by connecting DISH to GND directly.



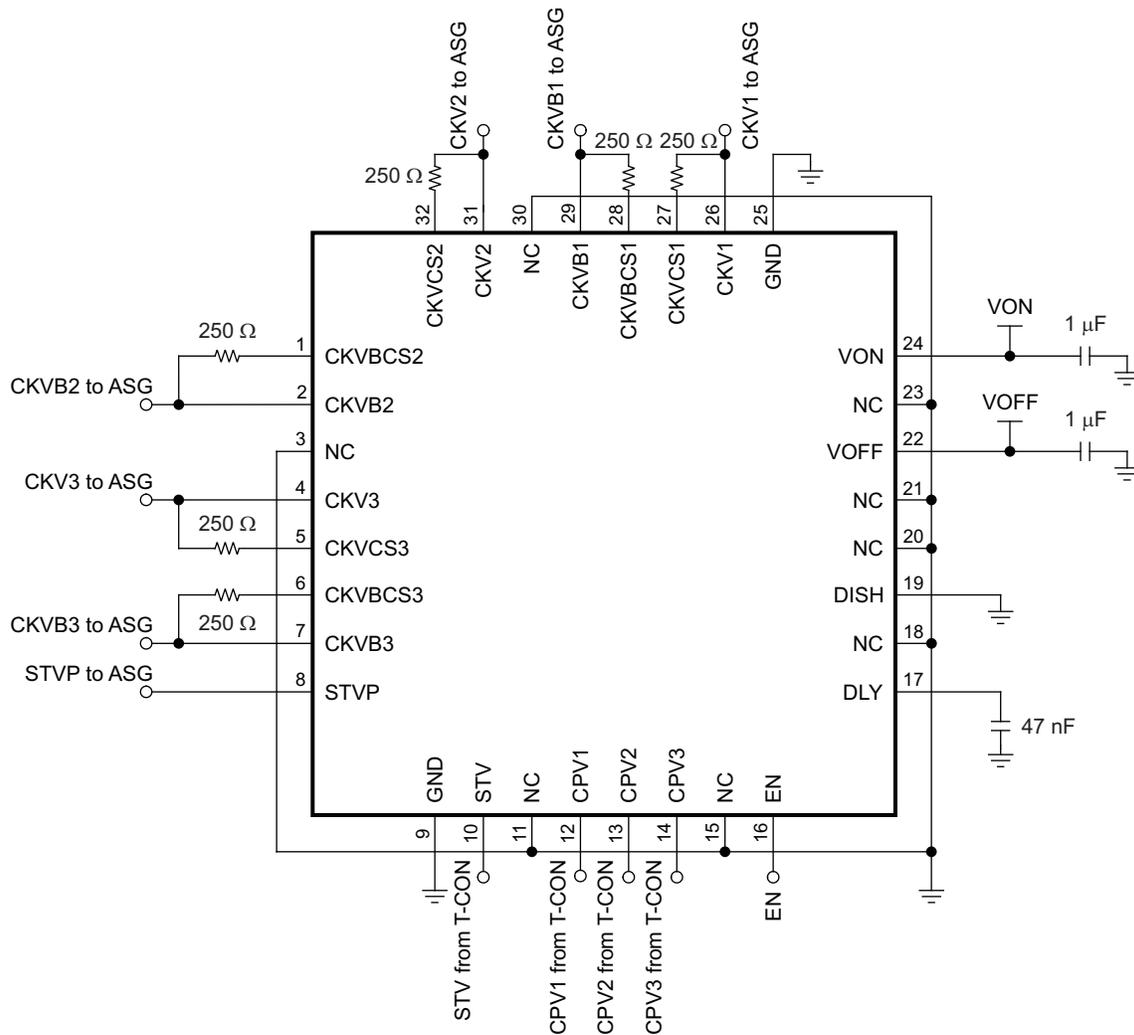
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Figure 22. Typical Application for VOFF Discharge



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Figure 23. Power-Off Sequence of VOFF Discharge



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Figure 25. Typical Application With VOFF Discharge Disabled

REVISION HISTORY

Changes from Revision Original (July 2009) to Revision A	Page
• Changed upper voltage limit from 37 V to 40 V in three places in the Abs Max Ratings table	2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65191RHBR.A	NRND	Production	VQFN (RHB) 32	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65191

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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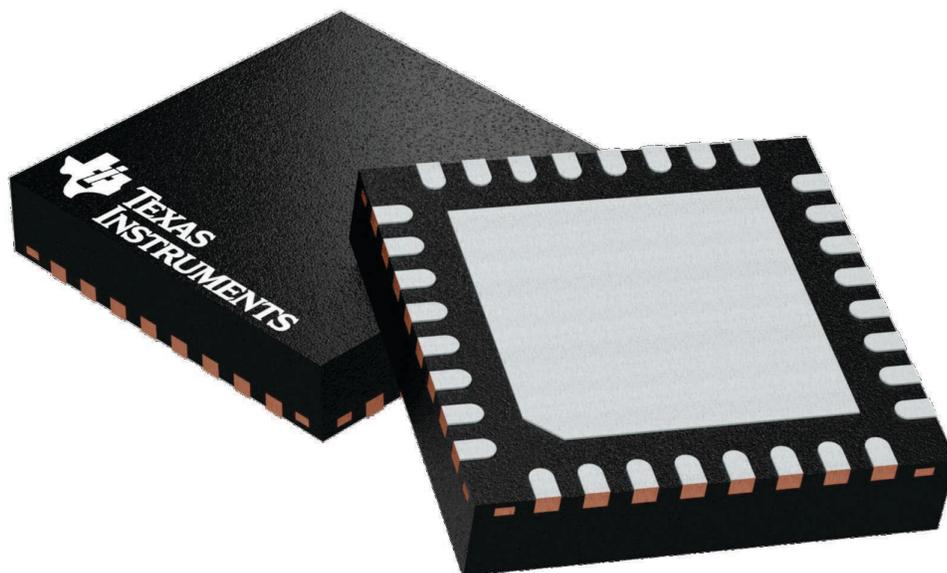
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

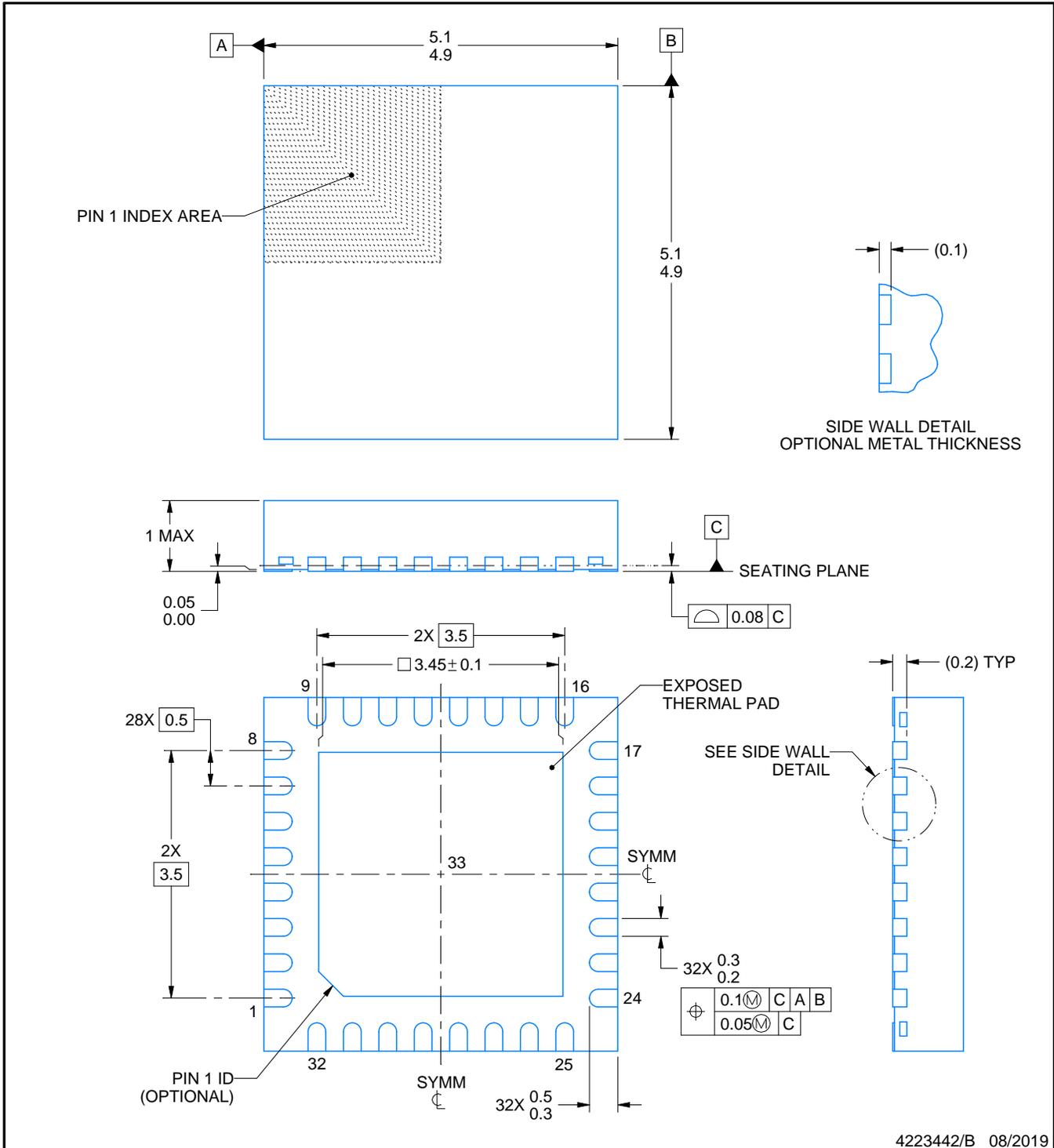
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



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NOTES:

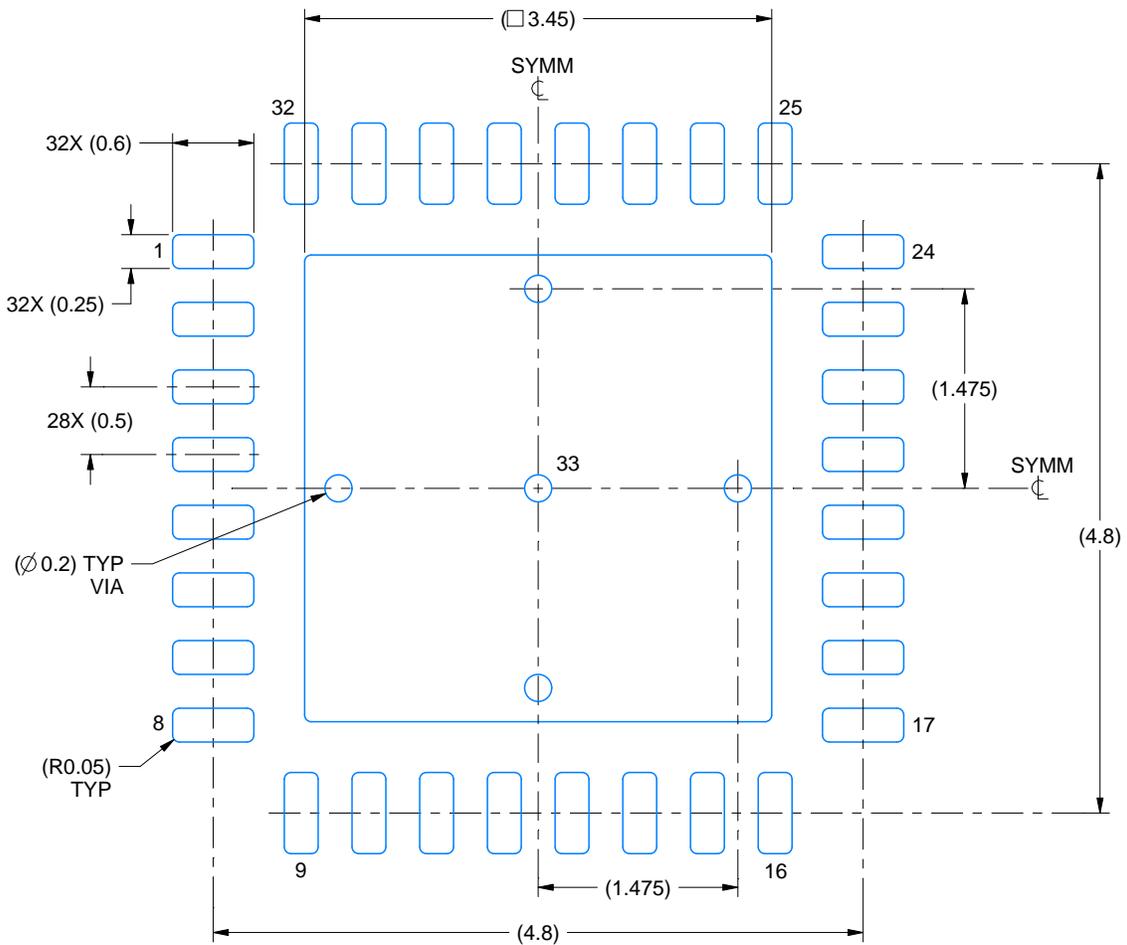
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

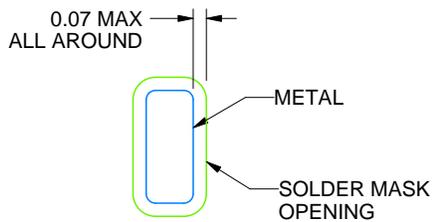
RHB0032E

VQFN - 1 mm max height

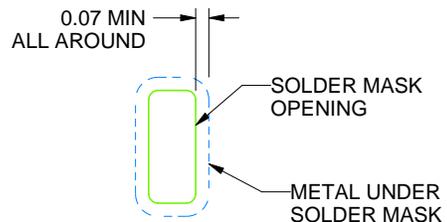
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

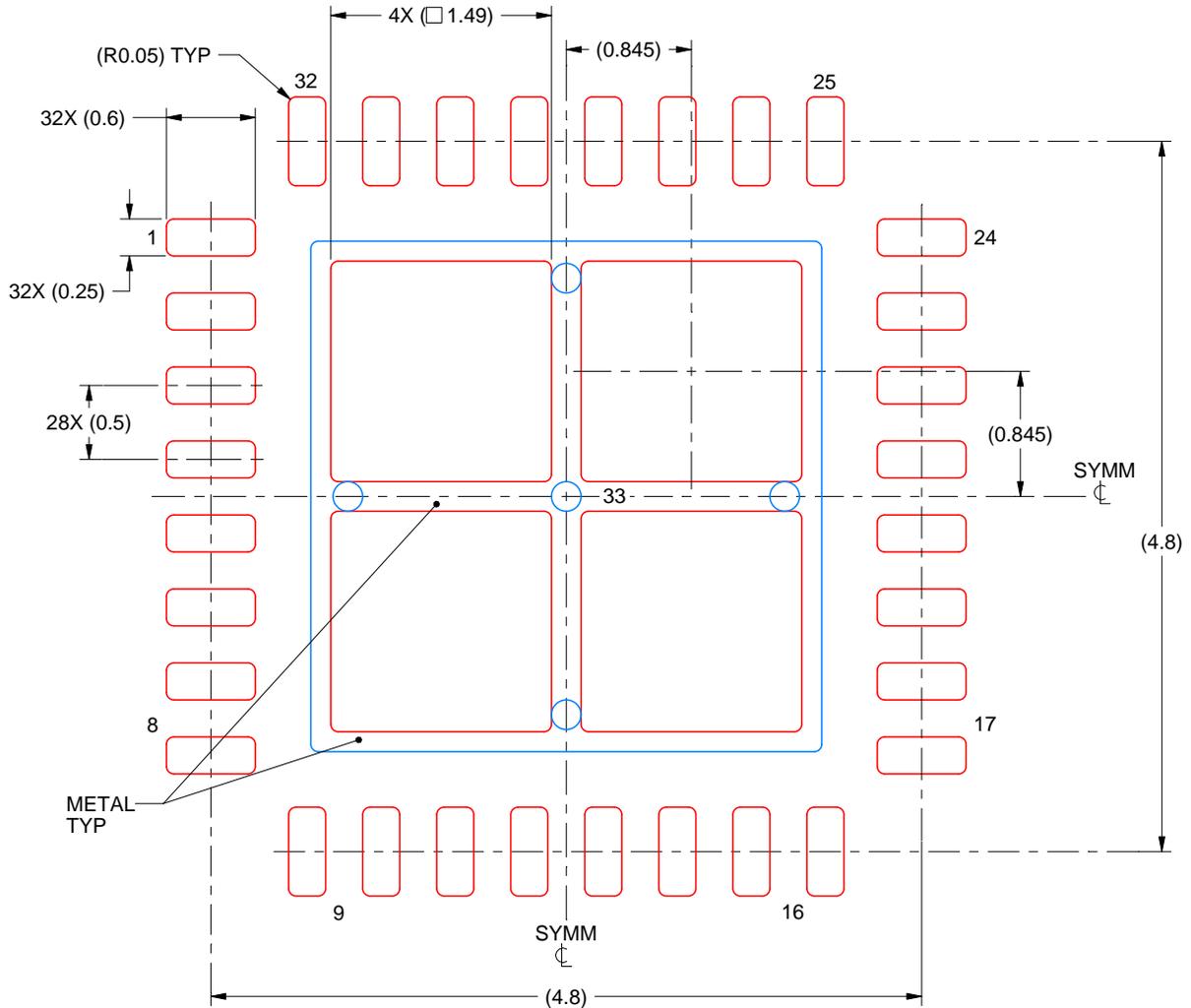
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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