TPS65214 Power Management IC with 3 BUCKs and 2 LDOs for Industrial Applications

1 Features

- 3 buck converters at up to 2.3MHz switching frequency:
  - 3× VIN: 2.5V - 5.5V; I_{OUT}: 2A; V_{OUT} 0.6V - 3.4V
- 2 linear regulators:
  - 1× VIN: 1.4V - 5.5V; I_{OUT}: 300mA; V_{OUT}: 0.6V - 3.3V (configurable as load switch)
  - 1× VIN: 1.4V - 5.5V; I_{OUT}: 500mA; V_{OUT}: 0.6V - 3.3V (configurable as load switch)
- Dynamic voltage scaling on all 3 buck converters
- Low IQ/PFM, PWM-mode (quasi-fixed frequency)
- Programmable power sequencing and default voltages
- I^2C interface, supporting standard, fast-mode and fast-mode+
- 3 multi-function-pins
- One-time programmable (OTP) non-volatile memory (NVM)

2 Applications

- Low power industrial MPUs such as AM62L
- Low power industrial MCUs such as AM261
- Appliances
- Building security
- EV charging infrastructure
- Fire safety system
- HMI
- HVAC
- Industrial PC
- Optical module
- Patient monitoring and diagnostics
- PLC
- Smart meter
- Test and Measurement
- Video surveillance

3 Description

The TPS65214 is a power management IC (PMIC) designed to supply a wide range of SoCs in both portable and stationary applications. The device is characterized across an ambient temperature range of -40°C to +105°C, making the PMIC an excellent choice for various industrial applications. The device includes 3 synchronous stepdown DC-DC converters and 2 linear regulators.

The DC-DC converters are capable of 3× 2A. The converters require a small 470nH inductor, 4.7µF input capacitance, and a minimum 10µF output capacitance per rail.

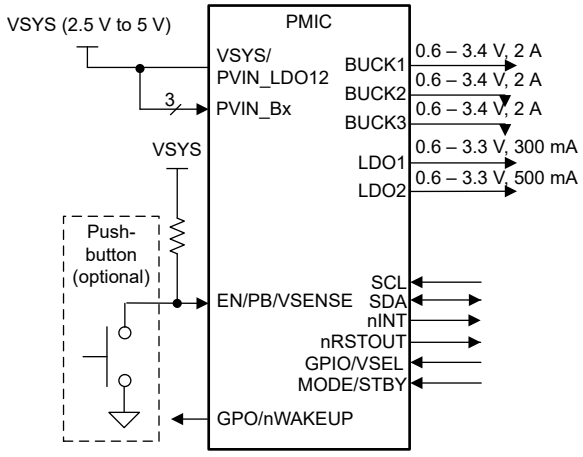
One LDO supports a maximum output current of 300mA and the other a maximum of 500mA. Both LDOs have a regulation output voltage range of 0.6V - 3.3V or can be operated in load-switch mode.

The I2C-interface, IOs, GPIOs and multi-function-pins (MFP) allow a seamless interface to a wide range of SoCs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE (NOM)
TPS65214	24-pin QFN	3.50mm × 3.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Device Comparison

Table 4-1 lists a summary of the pre-configured orderable part numbers (OPNs) and the recommended application use case. This table also includes the collateral resources that are available to support new designs. The applications note describes how the power and digital resources of the TPS65214 PMIC are used to meet the requirements of specific processors and MCUs. A full summary of the default non-volatile memory (NVM) register settings for each orderable can be found in the technical reference manual (TRM).

Table 4-1. Device Comparison Table for TI Processors and MCUs

Device Name	Processor / MCU	Application Use Case		
		Vin	Memory	BUCK1_VSET
TPS6521401(1)	AM62L	3.3V or 5V	LPDDR4	0.75V
TPS6521402	AM62L	3.3V or 5V	LPDDR4 or DDR4	0.75V

(1) The AM62L Evaluation Module comes with the TPS6521401 by default, supporting LPDDR4.

5 Pin Configuration and Functions

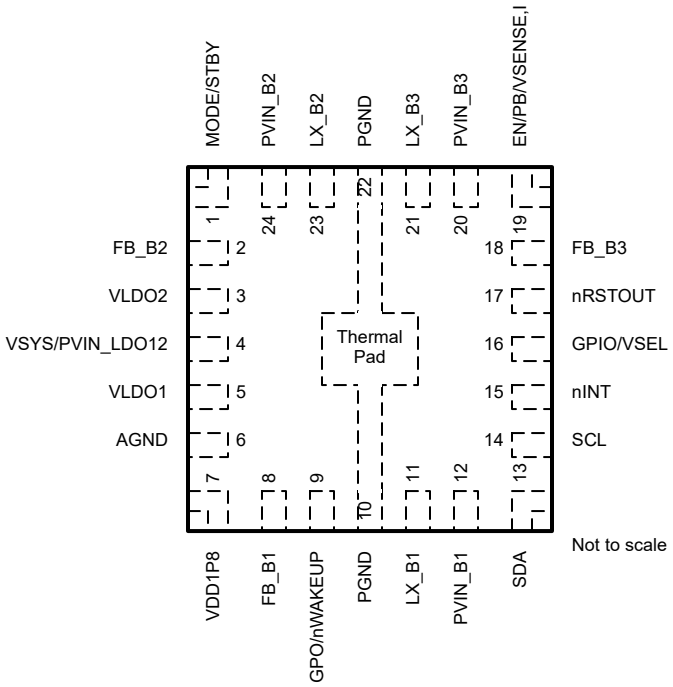


Figure 5-1. TPS65214 VAF Package, 24-pin QFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION	CONNECTION if not used
NAME	NO.			
MODE/STBY	1	I	Configured as MODE: Connected to SoC or hard-wired pull-up/-down. Forces the Buck-converters into PWM or permits auto-entry in PFM-mode.	n/a (tie high or low, dependent on configuration, see PWM/PFM and Low Power Modes (MODE/STBY)
		I	Configured as STBY: Low-power-mode command, powers down selected rails. Both functions, MODE and STBY, can be combined. The pin is level-sensitive.	
FB_B2	2	I	Feedback Input for Buck2. Connect to Buck2 output filter. Nominal output voltage is configured by NVM.	Connect to GND
VLDO2	3	PWR	Output Voltage of LDO2. Nominal output voltage is configured by NVM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.	Leave floating
VSYS/PVIN_LDO12	4	PWR	Input supply for reference system and power input for LDO1 and LDO2. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor.	n/a
VLDO1	5	PWR	Output Voltage of LDO1. Nominal output voltage is configured by NVM. Bypass this pin to ground with a 2.2µF or greater ceramic capacitor.	Leave floating
AGND	6	GND	Ground pin for Analog GND	n/a
VDD1P8	7	PWR	Internal Reference Voltage: For device internal use only. Do not apply an external load. Bypass this pin to ground with a 2.2µF ceramic capacitor.	n/a
FB_B1	8	I	Feedback Input for Buck1. Connect to Buck1 output filter. Nominal output voltage is configured by NVM.	Connect to GND

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	CONNECTION if not used
NAME	NO.			
GPO/nWAKEUP	9	O	Configured as GPO: General purpose open-drain output. Configurable in the power-up and power-down-sequence to enable an external rail.	Leave floating
		O	Configured as nWAKEUP: Signal to the host to indicate a power-on event. This pin is an active-low, open-drain output.	
PGND	10	GND	Power ground. This ground connection must be routed on PCB from both sides (Pin 10 and Pin 22). Connect the exposed pad to a continuous ground plane by multiple interconnect vias directly under the TPS65214 to maximize electrical and thermal conduction.	n/a
LX_B1	11	PWR	Switch Pin for Buck1. Connect one side of the Buck1-inductor to this pin.	Leave floating
PVIN_B1	12	PWR	Power Input for BUCK1. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_B1 pin must not exceed voltage on VSYS pin.	Connect to VSYS
SDA	13	I/O	Data Pin for the I2C Serial Port. The I2C logic levels depend on the external pull-up voltage.	Connect to VIO
SCL	14	I	Clock Pin for the I2C Serial Port. The I2C logic levels depend on the external pull-up voltage.	Connect to VIO
nINT	15	O	Interrupt Request Output. Open-drain driver is pulled low for fault conditions. Released if bit is cleared.	Leave floating
GPIO/VSEL	16	O	Configured as GPO: General purpose open-drain output. Configurable in the power-up and power-down-sequence to enable an external rail.	n/a (float, tie high or tie low, dependent on configuration, see General Purpose Input/Output and Voltage Select Pin (GPIO/VSEL)
		I	Configured as GPI: Configurable in the power-up and power-down-sequence to enable one or more device rails.	
		I	Configured as VSEL_BUCK: Buck1 or Buck3 VOUT selection. Hard-wired pull-up with external resistor, pull-down, or floating.	
nRSTOUT	17	O	Reset-output to SoC. Controlled by sequencer. High in ACTIVE state. Configurable level in STBY state.	Leave floating
FB_B3	18	I	Feedback Input for Buck3. Connect to Buck3 output filter. Nominal output voltage is configured by NVM.	Connect to GND
EN/PB/VSENSE	19	I	Configured as EN: Device enable pin, high level is ON-request, low-level is OFF-request.	n/a (configure as EN and connect to VSYS)
		I	Configured as PB: Push-button monitor input. 600ms low-level is an ON-request, 8s low-level is an OFF-request.	
		I	Configured as VSENSE: Power-fail comparator input. Set sense voltage using a resistor divider connected from the input to the pre-regulator to this pin to ground. Detects rising/falling voltage on pre-regulator and triggers ON- / OFF-request. The pin is edge-sensitive with a wait-time in PB-configuration and deglitch time for EN- and VSENSE-configuration.	

Table 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	CONNECTION if not used
NAME	NO.			
PVIN_B3	20	PWR	Power Input for BUCK3. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_B3 pin must not exceed voltage on VSYS pin.	Connect to VSYS
LX_B3	21	PWR	Switch Pin for Buck3. Connect one side of the Buck3-inductor to this pin.	Leave floating
PGND	22	GND	Power ground. This ground connection must be routed on PCB from both sides (Pin 10 and Pin 22). Connect the exposed pad to a continuous ground plane by multiple interconnect vias directly under the TPS65214 to maximize electrical and thermal conduction.	n/a
LX_B2	23	PWR	Switch Pin for Buck2. Connect one side of the Buck2-inductor to this pin.	Leave floating
PVIN_B2	24	PWR	Power Input for BUCK2. Bypass this pin to ground with a 4.7µF or greater ceramic capacitor. Voltage on PVIN_B2 pin must not exceed voltage on VSYS pin.	Connect to VSYS

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.(1)

POS			MIN	MAX	UNIT
1.1.1	Input voltage	VSYS/PVIN_LDO12	–0.3	6	V
1.1.2	Input voltage	PVIN_B1, PVIN_B2, PVIN_B3	–0.3	6	V
1.1.3	Input voltage vs. VSYS for Bucks	PVIN_B1, PVIN_B2, PVIN_B3 maximum voltage exceeding VSYS		200	mV
1.1.5	Input voltage	FB_B1, FB_B2, FB_B3	–0.3	6	V
1.1.6	Input voltage	EN/PB/VSENSE, MODE/STBY, GPIO/VSEL	–0.3	6	V
1.1.7	Input voltage	PGND	–0.3	0.3	V
1.2.1	Output voltage	LX_B1, LX_B2, LX_B3	–0.3	PVIN_Bx + 0.3 V, up to 6 V	V
1.2.2	Output voltage	LX_B1, LX_B2, LX_B3 spikes for maximum 10ns	–2	10	V
1.2.3	Output voltage	GPO/nWAKEUP, GPIO/VSEL	–0.3	6	V
1.2.4	Output voltage	VLDO1, VLDO2	–0.3	PVIN_LDOx + 0.3 V, up to 6 V	V
1.2.5	Output voltage	VDD1P8	–0.3	2	V
1.2.6	Output voltage	SDA, SCL	–0.3	6	V
1.2.7	Output voltage	nINT, nRSTOUT	–0.3	6	V
1.4.1	Operating junction temperature, T_J			125	°C
1.4.2	Storage temperature, T_{stg}		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

POS				VALUE	UNIT
2.1	$V_{(ESD)}$	Electrostatic discharge, Human Body Model	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
2.2	$V_{(ESD)}$	Electrostatic discharge, Charged Device Model	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS			MIN	NOM	MAX	UNIT
3.1.1a	$V_{VSYS/PVIN\_LDO12}$	Input voltage, LDOx in LDO mode	2.5		5.5	V
3.1.1b	$V_{VSYS/PVIN\_LDO12}$	Input Voltage, LDO1 and/or LDO2 in load switch mode	2.5		3.3	V
3.1.2	V_{PVIN_B1}, V_{PVIN_B2}, V_{PVIN_B3} V_{LX_B1}, V_{LX_B2}, V_{LX_B3}	BUCKx Pins	2.5		5.5 (1)	V
3.1.3	$\Delta V_{VSYS\_PVIN\_Bx}$	Voltage by which V_{PVIN_Bx} may exceed V_{VSYS}			0	mV

6.3 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS				MIN	NOM	MAX	UNIT
3.1.7	C_{PVIN_B1}, C_{PVIN_B2}, C_{PVIN_B3}	BUCKx Input Capacitance		3.9	4.7		µF
3.1.8	L_{B1}, L_{B2}, L_{B3}	BUCKx Output Inductance		330	470	611	nH
3.1.9a	C_{OUT_B1}, C_{OUT_B2}, C_{OUT_B3}	BUCKx Output Capacitance	Low bandwidth case	10		75	µF
3.1.10a			High bandwidth case	30		220	µF
3.1.11	V_{FB_B1}, V_{FB_B2}, V_{FB_B3}	BUCKx FB Pins		0		5.5 (1)	V
3.1.14	V_{PVIN_LDO12}	Allowable delta between V_{PVIN_LDOx} and configured V_{VLDOx} in load switch mode		-400		400	mV
3.1.15	V_{VLDO1}, V_{VLDO2}	LDO Output Voltage Range		0.6		3.3	V
3.1.16	$C_{VSYS/PVIN\_LDO12}$	VSYS and LDOx Input Capacitance		2.2	4.7		µF
3.1.17	C_{VLDO1}, C_{VLDO2}	LDO Output Capacitance		1.2	2.2	40	µF
3.1.22	V_{VDD1P8}	VDD1P8 pin		0		1.8	V
3.1.23	C_{VDD1P8}	Internal Regulator Decoupling Capacitance		1	2.2	4	µF
3.1.25	V_{nINT}, $V_{nRSTOUT}$	Digital Outputs		0		3.4	V
3.1.26b	$V_{GPO/nWAKEUP}$	Digital Outputs		0		5.5	V
3.1.26a	$V_{GPIO/VSEL}$	Digital Outputs		0		5.5 (1)	V
3.1.27	V_{SCL}, V_{SDA}	I2C Interface		0		3.4	V
3.1.28a	$V_{EN/PB/VSENSE}$	Digital Inputs		0		5.5	V
3.1.28b	$V_{GPIO/VSEL}$	Digital Inputs		0		5.5 (1)	V
3.1.28c	$V_{MODE/STBY}$	Digital Inputs		0		3.4	V
3.1.29	V_{PGND}	PGND Pin Voltage			0		V
3.2.1	$t_{VSYS\_RAMP\_RISE}$	Input voltage rising ramp Time, Input voltage controlled by a pre-regulator. V_{VSYS} = V_{PVIN_Bx} = V_{PVIN_LDOx} = 0V to 5V		0.1		600000	ms
3.2.2	$t_{VSYS\_RAMP\_FALL}$	Input voltage falling Ramp Time, V_{VSYS} = V_{PVIN_Bx} = V_{PVIN_LDOx} = 5V to 2.5V		0.4		600000	ms
3.2.3	$t_{MODE/STBY\_PROG\_SLEW}$	MODE/STBY programming voltage rising and falling slew rate, $V_{MODE/STBY}$ = 0V to 8V and 8V to 0V				25	mV/µs
3.3.1	T_A	Operating free-air temperature		–40		105	°C
3.3.2	T_J	Operating junction temperature		–40		125	°C

(1) Must not exceed VSYS

6.4 Thermal Information

THERMAL METRIC(1)		TPS65214 VAF (QFN) 24 PINS, 3.5x3.5mm²	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	45.5	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	30.0	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	14.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.1	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TPS65214 VAF (QFN) 24 PINS, 3.5x3.5mm²	UNIT
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	22.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 System Control Thresholds

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
4.1.1	VSYS	Operating Input Voltage		2.5		5.5	V
4.1.2	$VSYS_{UVLO\_Rising}$	VSYS UVLO rising threshold	Measured on VSYS pin, untrimmed	2.2		2.5	V
4.1.2.2	$VSYS_{POR\_Rising}$	VSYS POR rising threshold	Measured on VSYS pin, untrimmed	1.8		2.275	V
4.1.3	$VSYS_{UVLO\_Falling}$	VSYS UVLO falling threshold	Measured on VSYS pin, trimmed	2.175		2.25	V
4.1.3.2	$VSYS_{POR\_Falling}$	VSYS POR falling threshold	Measured on VSYS pin, trimmed	1.6		2.15	V
4.1.4	$VSYS_{UVLO\_Hyst}$	VSYS UVLO hysteresis	$VSYS_{UVLO\_Rising\_untrimmed}$ - $VSYS_{UVLO\_Falling\_trimmed}$		130		mV
4.1.5	$V_{VSYS\_OVP\_Rise}$	VSYS OVP rising threshold, trimmed	Measured on VSYS pin, trimmed	5.8		6.1	V
4.1.6	$V_{VSYS\_OVP\_Fall}$	VSYS OVP falling threshold, trimmed	Measured on VSYS pin, trimmed	5.7		5.95	V
4.1.7	$V_{VSYS\_OVP\_Hyst}$	VSYS OVP hysteresis	$VSYS_{OVP\_Rising\_trimmed}$ - $VSYS_{OVP\_falling\_trimmed}$	100	140	180	mV
4.1.8	V_{VDD1P8}	VDD1P8 voltage		1.7	1.8	1.9	V
4.2.1a	$I_{INITIALIZE}$	Current Consumption in INITIALIZE state	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. All Monitors are off. T_A = 25°C		13	20	µA
4.2.1b	$I_{INITIALIZE}$	Current Consumption in INITIALIZE state	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. All Monitors are off. T_A = -40°C to 105°C		13	30	µA
4.2.2a	I_{ACTIVE}	ACTIVE State Current Consumption, all rails on	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. T_A = 25°C		230	270	µA
4.2.2b	I_{ACTIVE}	ACTIVE State Current Consumption, all rails on	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. T_A = -40°C to 105°C		230	310	µA

6.5 System Control Thresholds (continued)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4.2.3a	I_{STBY}	STBY State Current Consumption, BUCK2, BUCK3, and LDO2 on	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. BUCK2, BUCK3, and LDO2 on in LDO-mode, Bucks in PFM mode. No Load. T_A = 25°C		130	155	µA
4.2.3b	I_{STBY}	STBY State Current Consumption, BUCK2, BUCK3, and LDO2 on	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. BUCK2, BUCK3, and LDO2 on in LDO-mode, Bucks in PFM mode. No Load. T_A = -40°C to 105°C		155	170	µA
4.2.4a	I_{STBY}	STBY State Current Consumption, all rails on	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. All Outputs are on, all LDOs in LDO-mode, Bucks in PFM mode. No Load. T_A = 25°C		230	270	µA
4.2.4b	I_{STBY}	STBY State Current Consumption, all rails on	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. All Outputs are on, all LDOs in LDO-mo, Bucks in PFM mode. No Load. T_A = -40°C to 105°C		230	310	µA
4.2.6a	I_{SLEEP}	SLEEP State Current Consumption	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. Most blocks off. T_A = 25°C		3	5	µA
4.2.6b	I_{SLEEP}	SLEEP State Current Consumption	Combined Current from VSYS and PVIN_x pins. VSYS = PVIN_Bx = PVIN_LDOx = 3.6V. Most blocks off. T_A = -40°C to 105°C		3	15	µA
Timing Requirements							
4.3.1	$t_{OFF\_TO\_INIT}$	Time from VSYS passing VSYS_UVLO until entering INITIALIZE state, including NVM-read, ready for ON-request	Time from VSYS passing VSYS_UVLO until entering INITIALIZE state. On request execution gated by HOT			6.2	ms
4.3.2a	$t_{TIMEOUT\_UV\_BUCK}$	UV-detection in case a Buck rail does not reach UV-threshold during ramp-up				1.8	ms
4.3.2b	$t_{TIMEOUT\_UV\_LDO}$	UV-detection in case a LDO rail does not reach UV-threshold during ramp-up				1.4	ms
4.3.3	t_{ON_DLY}	Time from valid ON-request received to the first sequence slot	All buck outputs below $V_{BUCKx\_SCG\_TH}$. All LDO outputs below $V_{LDOx\_SCG\_TH}$.			280	µs
4.10.7b	t_{NVM_LOAD}	Time from VDD1P8 > VDD1P8_POR until entering INITIALIZE state, ready for ON-request				4.95	ms

6.6 BUCK1, BUCK2, BUCK3 Converter

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
5.1.1a	V_{IN_BUCKx}	Input Voltage[1]	Buck supply voltage, maximum VSYS	2.5		5.5	V
5.1.1b	V_{OUT_BUCKx}	Buck Output Voltage configurable Range	Output voltage configurable in 25mV-steps for 0.6V ≤ V_{OUT} ≤ 1.4V, in 100mV steps for 1.4V < V_{OUT} ≤ 3.4V	0.6		3.4	V
5.1.2a	I_{Q_BUCKx}	Quiescent Current	PFM, BUCKx enabled, no load, V_{IN} = 3.6V, V_{OUT} = 0.75V, T_J=25°C		8	11	µA
5.1.3a	$V_{HEADROOM\_PWM}$	Input to Output Voltage Headroom[2]	Corner cases at maximum load I_{OUT} = 1.7A	500			mV
5.1.3b	$V_{HEADROOM\_PWM}$	Input to Output Voltage Headroom[2]	Corner cases at I_{OUT} = I_{OUT_MAX}	700			mV
5.1.4	$V_{OUT\_STEP\_LOW}$	Output voltage Steps Buck1	0.6V ≤ V_{OUT} ≤ 1.4V		25		mV
5.1.5	$V_{OUT\_STEP\_HIGH}$	Output voltage Steps Buck1	1.5V ≤ V_{OUT} ≤ 3.4V		100		mV
5.1.6a	$V_{OUT\_ACC\_DC\_PWM}$	DC Output Voltage Accuracy	Forced PWM, low and high BW case, I_{OUT} = I_{OUT_MAX}, 0.7V ≤ V_{OUT} ≤ 3.4V, V_{IN} - V_{OUT} > 700 mV, C_{OUT} = 40µF	–1.5%		1.5%	
5.1.6b	$V_{OUT\_ACC\_DC\_PWM}$	DC Output Voltage Accuracy	Forced PWM, low and high BW case, I_{OUT} = I_{OUT_MAX}, 0.6V ≤ V_{OUT} < 0.7V, V_{IN} - V_{OUT} > 700 mV, C_{OUT} = 40µF	–10		10	mV
5.1.6c	$V_{OUT\_ACC\_DC\_PFM}$	DC Output Voltage Accuracy	Auto-PFM, low and high BW case, I_{OUT} = 1mA, V_{OUT} = 0.6V to 3.4V, V_{IN} - V_{OUT} > 500 mV, C_{OUT} = 40µF	–3.0%		3.5%	
5.1.9	R_{FB_INPUT}	Feedback input impedance	Converter enabled	2.3	3.75	5.0	MΩ
5.2.1a	$V_{LOAD\_REG\_PWM}$	DC Load Regulation	Forced PWM, low BW case, V_{IN} = 5.0V, V_{OUT} = 1.2V, I_{OUT} = 0 to I_{OUT_MAX}, C_{OUT} = 40µF		0.1	0.16	%/A
5.2.2a	V_{LINE_REG}	DC Line Regulation	Forced PWM, low BW case, V_{IN} = 3.3V to 5.5V, V_{OUT} = 1.2V, I_{OUT} = 1mA and I_{OUT_MAX} C_{OUT} = 40µF		0.1	0.16	%/V
5.2.3a	$V_{LOAD\_TRANSIENT}$	Load Transient	Auto-PFM, high BW case, V_{IN} = 5.0V, V_{OUT} = 0.75V, I_{OUT} = 100mA to 1100mA to 100mA, t_R = t_F = 500ns, C_{OUT} = 80µF	–27.5		27.5	mV
5.2.3b	$V_{LOAD\_TRANSIENT}$	Load Transient,	Forced PWM, high BW case, V_{IN} = 5.0V, V_{OUT} = 0.75V, I_{OUT} = 100mA to 1100mA to 100mA, t_R = t_F = 500ns, C_{OUT} = 80 µF	–27.5		27.5	mV

6.6 BUCK1, BUCK2, BUCK3 Converter (continued)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.2.4a	$V_{LOAD\_TRANSIENT}$	Load Transient	Auto-PFM, low BW case, V_{IN} = 5.0V, V_{OUT} = 0.75V, I_{OUT} = 100mA to 600mA to 100mA, t_R = t_F = 500ns, C_{OUT} = 40µF	–30		30	mV
5.2.4b	$V_{LOAD\_TRANSIENT}$	Load Transient	Forced PWM, low BW case, V_{IN} = 5.0V, V_{OUT} = 0.75V, I_{OUT} = 100mA to 600mA to 100mA, t_R = t_F = 500ns, C_{OUT} = 40µF	–30		30	mV
5.2.5a	$V_{LINE\_TRANSIENT}$	Line Transient	Forced PWM, low BW case, V_{IN} = 3.3V to 5.5V in 50µs, V_{OUT} = 0.75V, I_{OUT} = 1mA and I_{OUT_MAX}, C_{OUT} = 40µF	–50		50	mV
5.2.6a	$V_{RIPPLE\_PP\_PWM}$	Output Voltage Ripple in Forced PWM	Low BW case, V_{IN} = 5.0V, V_{OUT} = 2.5V, I_{OUT} = 1A, L = 470nH, DCR = 50mΩ, C_{OUT} = 40uF, X5R, ESR = 10mOhm		10	20	mV_{PP}
5.2.6b	$V_{RIPPLE\_PP\_PFM}$	Output Voltage Ripple in Auto-PFM	Low BW case, V_{IN} = 5.0V, V_{OUT} = 2.5V, I_{OUT} = 20mA, L = 470nH, DCR = 50mΩ, C_{OUT} = 40uF, X5R, ESR = 10mOhm		20	40	mV_{PP}
5.3.1	I_{OUT_MAX}	Maximum Operating Current				2.0	A
5.3.2	$I_{CURRENT\_LIMIT}$	Peak Current Limit	V_{IN} = 2.5V to 5.5V	3.1	3.9	4.7	A
5.3.3	$I_{REV\_CUR\_LIMIT}$	Reverse Peak Current Limit	V_{IN} = 2.5V to 5.5V	–2.0	–1.5	–1.0	A
5.3.4a	R_{DSON_HS}	High Side MOSFET On Resistance	Measured Pin to Pin, V_{IN} = 5V			105	mΩ
5.3.4b	R_{DSON_HS}	High Side MOSFET On Resistance	Measured Pin to Pin, V_{IN} = 3.3V			170	mΩ
5.3.5a	R_{DSON_LS}	Low Side MOSFET On Resistance	Measured Pin to Pin, V_{IN} = 5V			100	mΩ
5.3.5b	R_{DSON_LS}	Low Side MOSFET On Resistance	Measured Pin to Pin, V_{IN} = 3.3V			140	mΩ
5.3.6	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is not enabled	60	125	200	Ω
5.4.1	L_{SW}	Output Inductance	DCR = 50mΩ max	330	470	611	nH
5.4.2a	C_{OUT}	Output Capacitance, Auto-PFM and forced PWM, ESR = 10mΩ max	Low bandwidth case	10		75	µF
5.4.3a			High bandwidth case	30		220	µF
Timing Requirements							
5.5.1	t_{RAMP}	Ramp Time	Time from enable to 98% of target value, assuming no residual voltage	0.3		1.65	ms
5.5.1.1	T_{START}	Start Time	Time from I2C enable signal to the Buck until enable of the Buck (ENABLE_BUCK), enabled individually, assuming no residual voltage			150	µs
5.5.1.2	t_{RAMP_QFF}	Ramp Time	Forced PWM, low BW case, Measured from ENABLE_BUCK to 98% of target value			1.3	ms
5.5.1.4	$t_{SAMPLE\_DEGLITCH}$	Time for sampling and deglitching before UV is released				100	µs

6.6 BUCK1, BUCK2, BUCK3 Converter (continued)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
5.5.2a	DVFS_SLOPE	DVFS Rising Slew Rate	Forced PWM, low BW case, Step-duration during DVFS voltage adjustments from 0.6V to 1.4V	2.9	3.2	3.5	mV/µs
5.5.2c	DVFS_FALL	DVFS Falling Slew Rate	Forced PWM, low BW case, Step-duration during DVFS voltage adjustments from 1.4V to 0.6V	0.45	0.53	0.61	mV/µs
Switching Characteristics							
5.6.1a	f_{SW}	Switching Frequency	Forced PWM, high and low BW case, V_{IN} = 3.3V to 5V, V_{OUT} = 0.8V to 1.8V, I_{OUT} = 1A to 1.8A		2.3		MHz

(1) PVIN_Bx must not exceed VSYS
(2) Refers to DC-regulation only. Transient response may require more headroom. With low headroom, the frequency variation increases for quasi-fixed frequency.

6.7 General Purpose LDOs (LDO1, LDO2)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ELECTRICAL CHARACTERISTICS								
7.8.1	V_{IN}	Input voltage			2.5		5.5	V
7.8.3	V_{OUT}	Output voltage	V_{IN} = 2.5V to 5.5V		0.6		3.3	V
7.8.4	V_{OUT_STEP}	Output voltage Steps	0.6V ≤ V_{OUT} ≤ 3.3V			50		mV
7.8.5	R_{BYPASS}	Bypass resistance	V_{IN} = 3.3V, I_{OUT} = 100mA, LDO in load switch mode				0.8	Ω
7.8.6	$V_{OUT\_DC\_ACCURACY}$	Total DC accuracy including DC load and line regulation for all valid output voltages	LDO-mode, V_{IN} - V_{OUT} > $V_{DROPOUT}$		–2.5		2.5	%
7.8.9	$V_{LOAD\_REGULATION}$	DC Load Regulation	V_{IN} = 3.8V, V_{OUT} = 3.3V, I_{OUT} = 0 to I_{OUT_MAX}			20	35	µV/mA
7.8.10	$V_{LINE\_REGULATION}$	DC Line Regulation	V_{IN} = V_{OUT} + $V_{DROPOUT}$ to 5.5V, V_{OUT} = 1.2V, 1.8V and 3.3V, I_{OUT} = 1mA			0.01	0.1	%/V
7.8.11a	$V_{LOAD\_TRANSIENT}$	Load Transient (LDO1)	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 20% of I_{OUT_MAX} to 80% of I_{OUT_MAX} in 1us		–35		35	mV
7.8.11b	$V_{LOAD\_TRANSIENT}$	Load Transient (LDO2)	VIN = 3.8V, VOUT = 3.3V, IOUT = 20% of IOUT_MAX to 80% of IOUT_MAX in 1us		–45		70	mV
7.8.12	$V_{LINE\_TRANSIENT}$	Line Transient	VIN step = 600 mVPP, T_R = T_F = 10 µs, LDO not in dropout condition		–25		25	mV
7.8.13c	$V_{DROPOUT1}$	LDO1 Dropout Voltage	I_{OUT} = I_{OUT_MAX}, V_{OUT} = 95% × $V_{OUT(NOM)}$	1.8V ≤ V_{OUT} < 3.3V			330	mV
7.8.13d				V_{OUT} = 3.3V			250	mV
7.8.13g	$V_{DROPOUT2}$	LDO2 Dropout Voltage	I_{OUT} = I_{OUT_MAX}, V_{OUT} = 95% × $V_{OUT(NOM)}$	1.8V ≤ V_{OUT} < 3.3V			530	mV
7.8.13h				V_{OUT} = 3.3V			400	mV
7.8.14	PSRR	Power Supply Ripple Rejection	V_{IN} = 2.8V, V_{OUT} = 1.8V, I_{OUT} = 50mA	f = 1kHz		60		db
7.8.15				f = 10kHz		47		db
7.8.16				f = 100kHz		55		db
7.8.17				f = 1MHz		45		db

6.7 General Purpose LDOs (LDO1, LDO2) (continued)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
7.8.18	$NOISE_{RMS}$	RMS Noise	f=100Hz to 100KHz, V_{IN} = 3.8V, I_{OUT} = 300mA, V_{OUT} = 3.3V and 1.8V		105 × V_{OUT}		uV_{RMS}
7.8.19	I_{OUT_MAX1}	Maximum Operating Current (LDO1)				300	mA
7.8.20	I_{OUT_MAX2}	Maximum Operating Current (LDO2)				500	mA
7.8.21	$I_{CURRENT\_LIMIT1}$	Short Circuit Current Limit (LDO1)	V_{IN} = 3.6V, V_{OUT} = 0V	400		900	mA
7.8.22	$I_{CURRENT\_LIMIT2}$	Short Circuit Current Limit (LDO2)	V_{IN} = 3.6V, V_{OUT} = 0V	600		1600	mA
7.8.23	I_{IN_RUSH}	LDO or LSW inrush current	VIN = 3.3V and then LDO is enabled, C_{OUT} = 40uF			1400	mA
7.8.25	$R_{DISCHARGE}$	Output Discharge Resistance	Active only when converter is not enabled, $R_{DISCHARGE}$ = '1'	100	200	300	Ω
7.8.29	I_{Qon}	Quiescent current on mode	V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 0mA, T_J=-40°C to 125°C		70	93	µA
7.8.32	C_{OUT}	Output filtering capacitance		1.2	2.2	4	µF
7.8.34	C_{ESR}	Filtering capacitor ESR max	1 to 10 MHz		10	20	mΩ
7.8.37	C_{OUT_TOTAL}	Total Capacitance at Output (Local + POL)				40	µF
TIMING CHARACTERISTICS							
7.8.50	t_{START}	Start Time	Time from completion of I2C command to output voltage at 0.3V			425	µs
7.8.51	t_{RAMP}	Ramp Time in LDO and LSW mode	Measured from 0.3V to 90% of target value			850	µs
7.8.52	t_{RAMP_SLEW}	Ramp up Slew Rate in LDO and LSW mode	VOUT from 0.3V to 90% of target value	2		12	mV/µs
7.8.53	$t_{TRANS\_1P8\_3P3}$	Transition time 1.8V - 3.3V	V_{IN} = 4.0V, I_{OUT} = 300mA		2		ms
7.8.54	$t_{TRANS\_3P3\_1P8}$	Transition time 3.3V - 1.8V	V_{IN} = 4.0V, I_{OUT} = 300mA		2		ms

6.8 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO/nWAKEUP, GPIO/VSEL, MODE/STBY)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
9.1.1	V_{OL}	Low-level Output Voltage (open-drain)	VIO = 3.6V, I_{OL} = 2mA, GPO/nWAKEUP, GPIO/VSEL, nRSTOUT, nINT			0.40	V
9.1.2	V_{IL}	Low-level Input Voltage	EN/PB, MODE/STBY, and GPIO/VSEL, in INITIALIZE, ACTIVE, or STBY mode			0.4	V
			EN/PB, in SLEEP mode			0.3×VSYS	V

6.8 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO/nWAKEUP, GPIO/VSEL, MODE/STBY) (continued)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.1.3	V_{IH}	High-level Input Voltage	EN/PB, MODE/STBY, and GPIO/VSEL, in INITIALIZE, ACTIVE, or STBY mode	1.26			V
			EN/PB, in SLEEP mode	0.7×VSYS			V
9.1.4	V_{VSENSE}	VSENSE Comparator Threshold (EN/PB/VSENSE)		1.08	1.20	1.32	V
9.1.5	V_{VSENSE_HYS}	VSENSE Comparator Hysteresis (EN/PB/VSENSE)		8	30	55	mV
9.1.6	I_{LKG}	Input leakage current (GPIO/VSEL, EN/PB/VSENSE, MODE/STBY)	V_{IN} = 3.3 V			1.0	µA
9.1.7	C_{IN}	Internal input pin capacitance (GPIO/VSEL, EN/PB/VSENSE, MODE/STBY)				10	pF
9.1.8	I_{PD}	pull-down current, available 100us after VSYS is applied	on pins GPO/nWAKEUP, GPIO/VSEL, MODE/STBY, nINT, nRSTOUT	18	25	35	nA
9.1.9	$I_{LKG\_VSYS\_ONLY}$	Pin leakage when VSYS is present, but digital supply is not	SDA, nINT			1	µA
9.1.10	$V_{PIN\_VSYS\_ONLY}$	Pin voltage when VSYS is present, but digital supply is not	GPO, GPIO, nRSTOUT, I_{OL}=2mA			0.4	V
Timing Requirements							
9.2.1a	t_{FALL}	Output buffer fall time (90% to 10%)	GPO/nWAKEUP, GPIO, nRSTOUT, nINT, C_{OUT} = 10pF			50	ns
9.2.1b	t_{RISE}	GPIO Output buffer rise time (10% to 90%)	GPIO			5	µs
9.2.2a	$t_{PB\_ON\_SLOW}$	EN/PB/VSENSE, Wait Time PB, ON request, slow	PB, falling Edge	540	600	660	ms
9.2.2b	$t_{PB\_ON\_FAST}$	EN/PB/VSENSE, Wait Time PB, ON request, fast	PB, falling Edge	180	200	220	ms
9.2.2c	$t_{EN\_PB\_WAKEUP}$	EN/PB/VSENSE, Wait Time EN/PB, SLEEP exit request	PB, falling Edge or EN, rising Edge	3.5	4.0	4.5	s
9.2.3	t_{PB_OFF}	EN/PB/VSENSE, Wait Time PB, OFF request	PB, falling Edge	7.2	8.0	8.8	s
9.2.4	$t_{DEGL\_PB\_RISE}$	EN/PB/VSENSE, Deglitch time PB, rising edge	PB, rising Edge, applicable after the successful long-press-OFF-request	115	200	275	ms
9.2.5	$t_{DEGL\_PB\_INT}$	EN/PB/VSENSE, Deglitch time PB, rising or falling edge	PB, rising or falling Edge	59	100	137	ms
9.2.6	$t_{DEGL\_EN\_Rise\_Slow}$	EN/PB/VSENSE, DeglitchTime EN slow, rising	EN, rising Edge	45	50	55	ms
9.2.7	$t_{DEGL\_EN\_Rise\_Fast}$	EN/PB/VSENSE, DeglitchTime EN fast, rising	EN, rising Edge	60	120	185	µs
9.2.8	$t_{DEGL\_EN\_Fall}$	EN/PB/VSENSE, DeglitchTime EN, falling	EN, falling Edge	50	70	93	µs
9.2.9	$t_{DEGL\_VSENSE\_Rise}$	VSENSE rising: only gated by $VSYS_{POR\_Rising}$ and VSENSE-voltage	VSENSE, rising Edge		N/A		
9.2.10	$t_{DEGL\_VSENSE\_Fall}$	EN/PB/VSENSE, DeglitchTime VSENSE, falling, regardless of fast/slow setting	VSENSE, falling Edge	50	70	93	µs

6.8 GPIOs and multi-function pins (EN/PB/VSENSE, nRSTOUT, nINT, GPO/nWAKEUP, GPIO/VSEL, MODE/STBY) (continued)

Over operating free-air temperature range (unless otherwise noted). Specified voltage levels are in reference to the AGND ground of the device.

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
9.2.11	$t_{DEGL\_EN/VSENSE\_I2C}$	EN/VSENSE falling edge deglitch time after I2C-triggered shutdown	EN/VSENSE falling edge after previous shutdown request by I2C (shorter than 9.2.8)	12.5	25	37.5	µs
9.2.13	t_{DEGL_MFP}	Deglitch Time MODE/STBY	Rising and falling Edge	90	120	150	µs
9.2.14	t_{DEGL_GPIO}	Deglitch Time GPIO	Rising and falling Edge	6.6	15.6	18	µs

6.9 Voltage and Temperature Monitors

over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
10.1.1	$V_{BUCKx\_UV\_TH\_5}$, $V_{LDOx\_UV\_TH\_5}$	Undervoltage monitoring for buck output, programable low-going threshold accuracy	UV_THR = 0x0		–5%		
10.1.2	$V_{BUCKx\_UV\_TH\_10}$, $V_{LDOx\_UV\_TH\_10}$	Undervoltage monitoring for buck output and LDO output, programable low-going threshold accuracy	UV_THR = 0x1		–10%		
10.1.3	$V_{BUCKx\_UV\_H\_ACC}$, $V_{LDOx\_UV\_H\_ACC}$	Undervoltage Threshold Accuracy, V_{OUT} ≥ 1V	V_{OUT} ≥ 1V	-1%		+1%	
10.1.4	$V_{BUCKx\_UV\_L\_ACC}$, $V_{LDOx\_UV\_L\_ACC}$	Undervoltage Threshold Accuracy, V_{OUT} < 1V	V_{OUT} < 1V	-10		+10	mV
10.1.5	$V_{BUCKx\_UV\_HYS}$, $V_{LDOx\_UV\_HYS}$	Undervoltage Hysteresis		0.5%	1%	1.5%	
10.1.6	$V_{BUCKx\_SCG\_TH}$, $V_{LDOx\_SCG\_TH}$	Short-circuit (SCG) and residual voltage (RV) detection low-going threshold		220	260	300	mV
10.1.7	$V_{BUCKx\_SCG\_HYS}$, $V_{LDOx\_SCG\_HYS}$	Short-circuit (SCG) and residual voltage (RV) detection threshold hysteresis			75		mV
10.2.1a	T_{WARM_Rising}	Temperature rising Warning Threshold (WARM)	for each of the three sensors	110	120	130	°C
10.2.1b	$T_{WARM\_Falling}$	Temperature falling Warning Threshold (WARM)	for each of the three sensors	105	115	125	°C
10.2.2a	T_{HOT_Rising}	Temperature rising Shutdown Threshold (TSD, HOT)	for each of the three sensors	130	140	150	°C
10.2.2b	$T_{HOT\_Falling}$	Temperature falling Shutdown Threshold (TSD, HOT)	for each of the three sensors	125	135	145	°C
10.2.3	T_{HYS}	Temperature Hysteresis for WARM	for each of the three sensors		-5		°C
Timing Requirements							
10.3.1a	$t_{DEGLITCH}$	Buck and LDO Fault Detection Deglitch Time for Undervoltage (UV) and Short to GND (SCG)	Measured from UV/SCG event	13	20	27	µs
10.3.1b	$t_{DEGLITCH\_OC\_short}$	Buck Fault Detection Deglitch Time for Over Current (OC), rising edge, short	Measured from OC event, rising edge	26	35	45	µs
10.3.1c	$t_{DEGLITCH\_OC\_long}$	Buck Fault Detection Deglitch Time for Over Current (OC), rising edge, long	Measured from OC event, rising edge	1.6	2	2.2	ms

6.9 Voltage and Temperature Monitors (continued)

over operating free-air temperature range (unless otherwise noted)

POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
10.3.1d	$t_{DEGLITCH\_OC\_LDO}$	LDO Fault Detection Deglitch Time for Over Current (OC), rising edge	Measured from OC event, rising edge	10	12	14	µs
10.3.2a	$t_{REACTION}$	Buck and LDO Fault Reaction Time for Undervoltage (UV) and Short to GND (SCG) (including deglitch time)	Measured from UV/SCG event to nINT pulled low	26	40	54	µs
10.3.2b	$t_{REACTION\_OC\_short}$	Buck Fault Reaction Time for Over Current (OC) (including deglitch time)	Measured from UV/OC/SCG event to nINT pulled low	45	65	81	µs
10.3.2c	$t_{REACTION\_OC\_long}$	Buck Fault Detection Deglitch Time for Over Current (OC), rising edge, long	Measured from OC event, rising edge	1.6	2	2.2	ms
10.3.2d	$t_{REACTION\_OC\_LDO}$	LDO Fault Reaction Time for Over Current (OC) (including deglitch time)	Measured from UV/OC/SCG event to nINT pulled low	12	18	24	µs
10.3.2e	$t_{REACTION\_WARM}$	Fault Reaction Time for Temperature Warning (WARM), Thermal Shutdown (TSD / HOT)	Measured from WARM/HOT event to nINT pulled low			525	µs

6.10 I²C Interface

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3V or 1.8V.

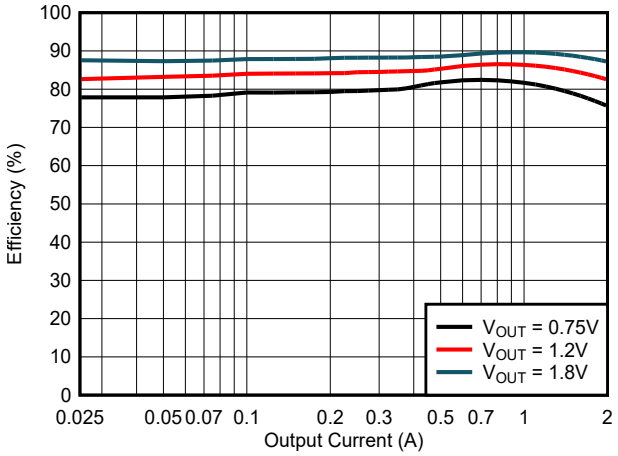
POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Electrical Characteristics							
11.1.1	V_{OL}	Low-level Output Voltage	VIO = 3.6V, I_{OL} = 3mA for Standard mode and Fast mode, I_{OL} = 20mA for Fast mode+, SDA			0.40	V
11.1.2	V_{IL}	Low-level Input Voltage	SDA, SCL			0.40	V
11.1.3	V_{IH}	High-level Input Voltage	SDA, SCL	1.26			V
11.1.4	V_{HYST}	Input buffer Hysteresis	EN_BP/VSENSE, MODE_RESET, MODE_STBY, SDA, SCL, GPIO	100		500	mV
11.1.5	C_B	Capacitive Load for SDA and SCL				400	pF
Timing Requirements							
11.2.1	f_{SCL}	Serial Clock Frequency	Standard mode			100	kHz
11.2.2			Fast mode			400	
11.2.3			Fast mode+			1	MHz
11.3.1	t_{LOW}	SCL low Time	Standard mode	4.7			µs
11.3.2			Fast mode	1.3			
11.3.3			Fast mode+	0.50			
11.4.1	t_{HIGH}	SCL high Time	Standard mode	4.0			µs
11.4.2			Fast mode	0.60			
11.4.3			Fast mode+	0.26			
11.5.1	$t_{SU;DAT}$	Data setup Time	Standard mode	250			ns
11.5.2			Fast mode	100			
11.5.3			Fast mode+	50			
11.6.1	$t_{HD;DAT}$	Data hold Time	Standard mode	10		3450	ns
11.6.2			Fast mode	10		900	
11.6.6			Fast mode+	10			

6.10 I²C Interface (continued)

Over operating free-air temperature range (unless otherwise noted). Device supports standard mode (100 kHz), fast mode (400 kHz), and fast mode+ (1 MHz) when VIO is 3.3V or 1.8V.

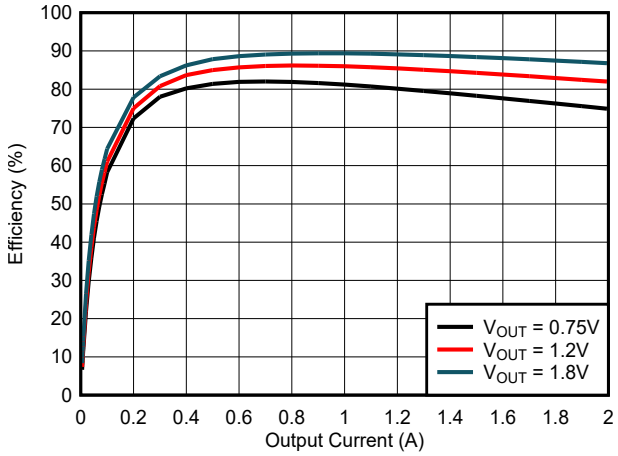
POS	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
11.7.1	$t_{SU;STA}$	Setup Time for a Start or a REPEATED Start Condition	Standard mode	4.7			µs
11.7.2			Fast mode	0.60			
11.7.3			Fast mode+	0.26			
11.8.1	$t_{HD;STA}$	Hold Time for a Start or a REPEATED Start Condition	Standard mode	4.7			µs
11.8.2			Fast mode	0.60			
11.8.3			Fast mode+	0.26			
11.9.1	t_{BUF}	Bus free Time between a STOP and Start Condition	Standard mode	4.7			µs
11.9.2			Fast mode	1.3			
11.9.3			Fast mode+	0.50			
11.10.1	$t_{SU;STO}$	Setup Time for a STOP Condition	Standard mode	0.60			µs
11.10.2			Fast mode	0.60			
11.10.3			Fast mode+	0.26			
11.10.1	t_{rDA}	Rise Time of SDA Signal	Standard mode, VIO = 1.8V, R_{PU} = 10 kΩ and C_B = 400 pF			1000	ns
11.10.2			Fast mode, VIO = 1.8V, R_{PU} = 1 kΩ and C_B = 400 pF	20		300	
11.10.3			Fast mode+, VIO = 1.8V, R_{PU} = 330 Ω and C_B = 400 pF			120	
11.12.1	t_{fDA}	Fall Time of SDA Signal	Standard mode, VIO = 1.8V, R_{PU} = 10 kΩ and C_B = 400 pF			300	ns
11.12.2			Fast mode, VIO = 1.8V, R_{PU} = 1 kΩ and C_B = 400 pF	6.5		300	
11.12.3			Fast mode+, VIO = 1.8V, R_{PU} = 330 Ω and C_B = 400 pF	6.5		120	
11.13.1	t_{rCL}	Rise Time of SCL Signal	Standard mode, VIO = 1.8V, R_{PU} = 10 kΩ and C_B = 400 pF			1000	ns
11.13.2			Fast mode, VIO = 1.8V, R_{PU} = 1 kΩ and C_B = 400 pF	20		300	
11.13.3			Fast mode+, VIO = 1.8V, R_{PU} = 330 Ω and C_B = 400 pF			120	
11.14.1	t_{fCL}	Fall Time of SCL Signal	Standard mode, VIO = 1.8V, R_{PU} = 10 kΩ and C_B = 400 pF			300	ns
11.14.2			Fast mode, VIO = 1.8V, R_{PU} = 1 kΩ and C_B = 400 pF	6.5		300	
11.14.3			Fast mode+, VIO = 1.8V, R_{PU} = 330 Ω and C_B = 400 pF	6.5		120	
11.15.1	t_{SP}	Pulse Width of Spike suppressed (SCL and SDA Spikes that are less than the indicated Width are suppressed)	Fast mode, and fast mode+			50	ns

6.11 Typical Characteristics



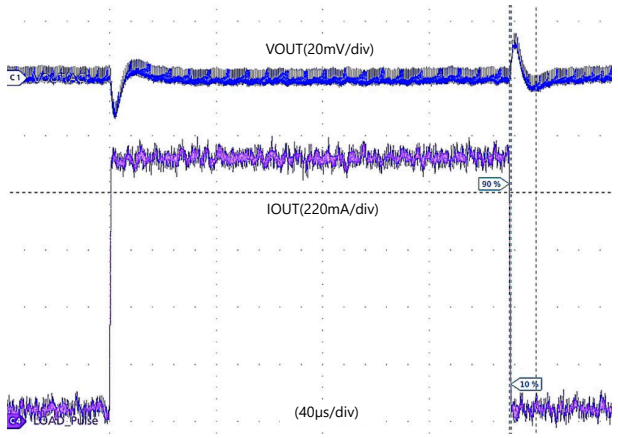
V_{IN} = 5V T_A = 25°C

Figure 6-1. BUCK Efficiency, Auto-PFM



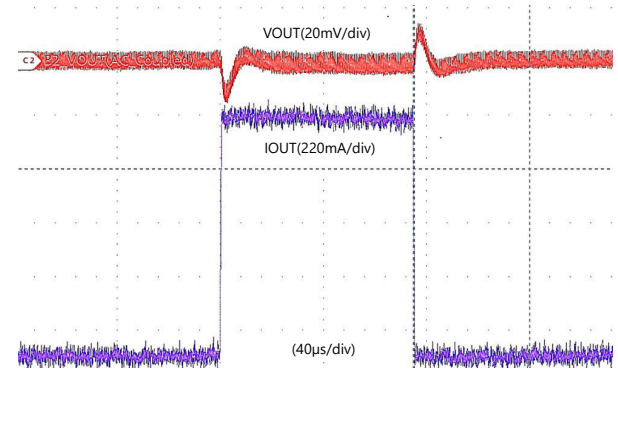
V_{IN} = 5V T_A = 25°C

Figure 6-2. BUCK Efficiency, Forced-PWM



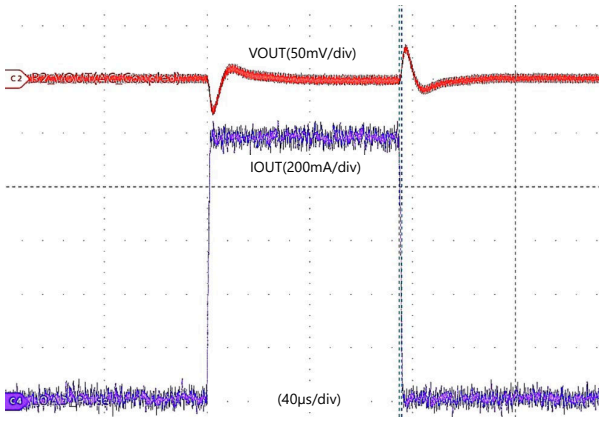
V_{IN} = 5.0V V_{OUT} = 0.75V T_A = 25°C
I_{OUT} = 100mA to 1.1A to 100mA, C_{OUT_total} = 57µF
t_{rise} = t_{fall}= 500ns

Figure 6-3. BUCK Load-Step Response - High Bandwidth, Forced PWM



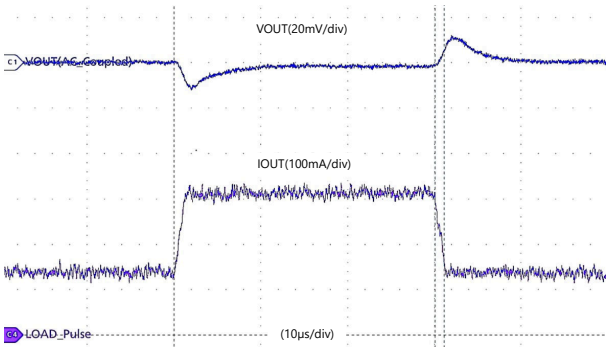
V_{IN} = 5.0V V_{OUT} = 1.2V T_A = 25°C
I_{OUT} = 1mA to 1A to 1mA, C_{OUT_total} = 57µF
t_{rise}=t_{fall}=1µs

Figure 6-4. BUCK Load-Step Response - High Bandwidth, Forced PWM



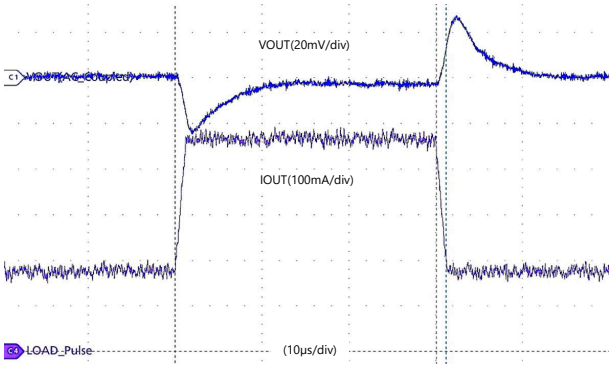
V_{IN} = 5.0V V_{OUT} = 1.8V T_A = 25°C
I_{OUT} = 1mA to 1A to 1mA, C_{OUT_total} = 28µF
t_{rise} = t_{fall} = 1µs

Figure 6-5. BUCK Load-Step Response - Low Bandwidth, Forced PWM



V_{IN} = 3.3V V_{OUT} = 1.8V T_A = 25°C
I_{OUT} = 60mA to 240mA to 60mA, C_{OUT} = 10µF
t_{rise} = t_{fall} = 1µs

Figure 6-6. LDO1 Load-Step Response



V_{IN} = 3.8V V_{OUT} = 3.3V T_A = 25°C
I_{OUT} = 100mA to 400mA to 100mA, C_{OUT} = 10µF
t_{rise} = t_{fall} = 1µs

Figure 6-7. LDO2 Load-Step Response

7 Detailed Description

7.1 Overview

The TPS65214 provides three step-down converters, two LDOs, two general-purpose I/Os and three multifunction pins. The system can be supplied by a single cell Li-Ion battery, two primary cells or a regulated supply. The device is characterized across a -40°C to +105°C temperature range, which makes the PMIC an excellent choice for various industrial applications.

The I2C interface provides comprehensive features for using TPS65214. The status of all rails, the GPO and the GPIO can be controlled via the interface. Voltage thresholds for the undervoltage monitoring can also be customized.

The integrated voltage supervisor monitors Buck1-3 and LDO1-2 for undervoltage. The monitor has two sensitivity settings. A power good signal is provided to report the successful ramp of the five rails and GPOs. The nRSTOUT pin is pulled low until the device enters ACTIVE state. When powering down from ACTIVE- or STBY-state, nRSTOUT is pulled low again. The nRSTOUT pin has an open-drain output. A fault-pin, nINT, notifies the SoC about faults.

Buck1 can supply up to 2A at an output voltage range of 0.6V - 3.4V. Buck2 and Buck3 step-down converters can supply up to 2A of current each at an output voltage range of 0.6V - 3.4V. The default output voltages for each converter can be adjusted through the I2C interface. All three buck-converters feature dynamic voltage scaling. The step-down converters operate in a low power mode at light load or can be forced into PWM operation for noise sensitive applications.

LDO1 can support output currents of 300mA while LDO2 supports 500mA. Both LDOs support a regulation output voltage range of 0.6V - 3.3V or load-switch operation.

The I2C-interface, IOs, GPIOs, and multi-function-pins (MFP) allow a seamless interface to a wide range of SoCs.

All configurations of the rails, for example output-voltages, sequencing, are backed up by NVM. Please refer to the Technical Reference Manual (TRM) of the chosen configuration.

7.2 Functional Block Diagram

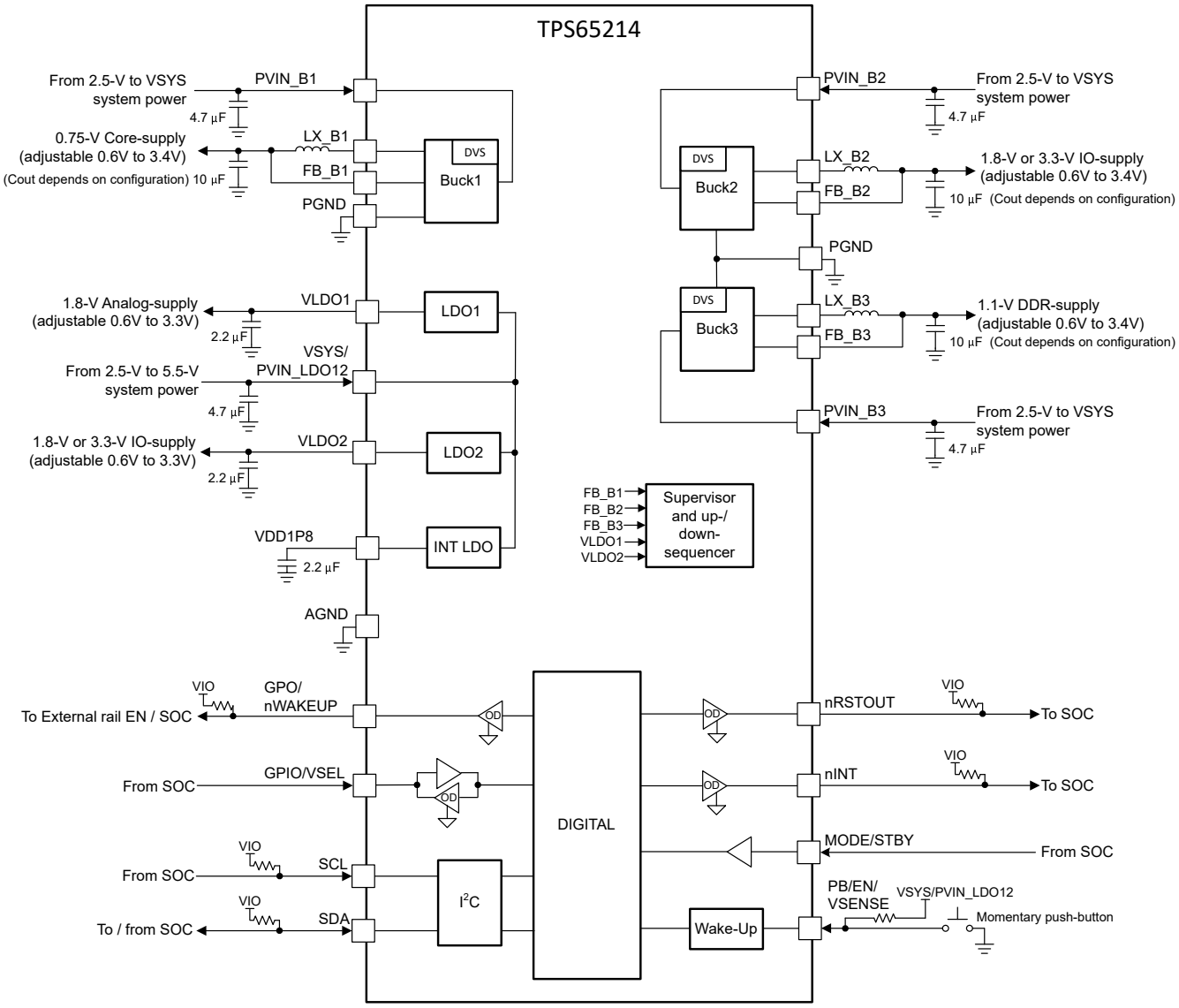


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Power-Up Sequencing

The TPS65214 allows flexible sequencing of the rails. The order of the rails, including GPO and GPIO for the external rails, and the nRSTOUT pin is defined by the NVM. Prior to starting the power-up sequence, the device checks if the voltage on all rails fell below the SCG-threshold to avoid starting into a pre-biased rail. The sequence is timing based. In addition, the previous rail must have passed the UV-threshold, else the subsequent rail is not enabled. If UV is masked, the sequence proceeds even if the UV-threshold is not reached. GPO, GPIO, and LDOs configured in LSW-mode are not monitored for undervoltage, thus their outputs do not gate subsequent rails.

In case the sequence is interrupted due to an unmasked fault on a rail, the device powers down. The TPS65214 attempts to power up two more times. If both of those re-tries fail to enter ACTIVE state, the device remains in INITIALIZE state until VSYS is power-cycled. This retry-counter is encouraged to remain active but can be deactivated by setting bit MASK_RETRY_COUNT in INT_MASK_UV register. When set, the device attempts to retry infinitely.

The TPS65214 allows to configure the power-down sequence independent from the power-up sequence. The sequences are configured in the non-volatile memory.

At initial power-up, the device monitors the VSYS supply voltage and allows power-up and transition to INITIALIZE state only if VSYS passed the $VSYS_{POR\_Rising}$ threshold.

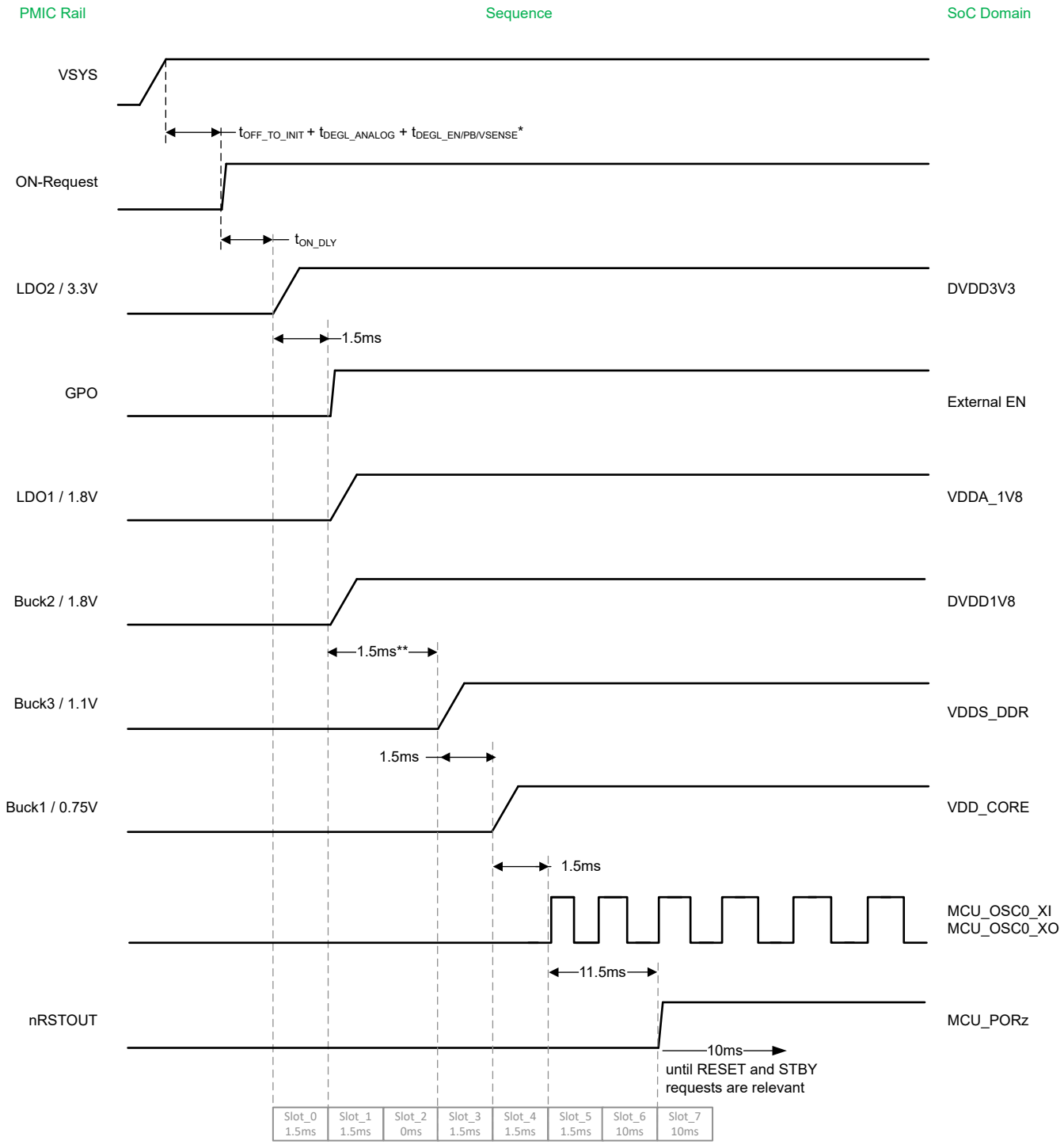
The power-up sequence is configured as follows:

- The slot (respectively the position in the sequence) for each rail, GPO, GPIO, and nRSTOUT is defined using the corresponding *_SEQUENCE_SLOT registers, the four MSB for the power-up sequence, the four LSB for the power-down sequence.
- The duration of each slot is defined in the POWER_UP_SLOT_DURATION_x registers and can be configured as 0ms, 1.5ms, 3ms or 10ms. In total, 8 slots can be configured.
- In addition to the timing as defined above, the power-up-sequence is also gated by the UV-monitor: a subsequent rail only gets enabled after the previous one passed the undervoltage threshold (unless UV is masked). If a rail has not reached the UV-threshold by the end of t_{RAMP} (respectively t_{RAMP_LSW}, t_{RAMP_SLOW}, t_{RAMP_FAST}), the sequence is aborted and the device sequences down at the end of the slot-duration. For the respective rail, the device sets INT_BUCK_x_y_IS_SET respectively INT_LDO_x_y_IS_SET bit in INT_SOURCE register and BUCKx_UV respectively LDOx_UV bit in INT_BUCK_x_y respectively INT_LDO_x_y register as well as bit TIMEOUT in the INT_TIMEOUT_RV_SD register.
- The initiation of the sequence is gated by the die-temperature: if any one of the WARM detections is unmasked, the device does not power-up until the temperature on all sensors fell below $T_{WARM\_falling}$ threshold if INITIALIZE state was entered due to a thermal event, respectively until the temperature on all sensors is below T_{WARM_rising} threshold if INITIALIZE state was entered from OFF-state. If all thermal sensors are masked (WARM detection not causing a power-down), the device does not power-up until the temperature on all sensors is below $T_{HOT\_falling}$ threshold

Note

All rails get discharged prior to enable (irrespective if discharge-function is deactivated).

An ON-request is deglitched to not trigger on noise. The time from the deglitch to the first slot of the sequence is given by t_{ON_DLY}. Figure 7-2 shows an example power-up-sequence.



* depends on EN / PB / VSENSE and long/short configuration, ~0 if FSD is enabled
** if applicable, slot-duration needs to adopt for enable- & ramp-time of external rail

Figure 7-2. Power-Up Sequencing (example)

For details on ON-requests see Push Button and Enable Input (EN/PB/VSENSE).

CAUTION

The times shown in the timing diagrams reflect the POWER_UP_SLOT_DURATION_x registers. The programmed times have a ±10% tolerance. When measured in the application, the start time (t_{START}) for the BUCKs and LDOs are added to the programmed slot times.

CAUTION

I2C commands must only be issued after NVM-load completed.

7.3.2 Power-Down Sequencing

An OFF-request or a shut-down-fault triggers the power-down sequence. The OFF-request can be triggered by a falling edge on EN/PB/VSENSE if configured for EN or VSENSE respectively a long press of the push-button if configured as PB or by an I2C-command to I2C_OFF_REQ in MFP_CTRL register. This bit self-clears.

An I2C-triggered shut-down requires a renewed ON-request on the EN/PB/VSENSE pin. In case of EN- or VSENSE-configuration, a low-going edge followed by a high-going-edge is required on the EN/PB/VSENSE-pin. The falling-edge deglitch time for EN or VSENSE configuration $t_{DEGL\_EN/VSENSE\_I2C}$ is shorter than the deglitch-time for pin-induced OFF-requests ($t_{DEGL\_EN\_Fall}$ and $t_{DEGL\_VSENSE\_Fall}$). The deglitch-times for PB-configuration remain.

In many cases, the power-down sequence follows the reverse power-up sequence. In some applications, all rails can be required to shut down at the same time with no delay between rails or require wait-times to allow discharging of rail.

The power-down sequence is configured as follows:

- The slot (respectively the position in the sequence) for each rail, GPO, GPIO, and nRSTOUT is defined using the corresponding *_SEQUENCE_SLOT registers, the four MSB for the ON-sequence, the four LSB for the down-sequencing.
- The duration of each slot is defined in the POWER_DOWN_SLOT_DURATION_x registers and can be configured as 0ms, 1.5ms, 3ms or 10ms. In total, 8 slots can be configured.
- In addition to the slot-duration, the power-down sequence is also gated by the previous rail being discharged below the SCG-threshold, unless active discharge is deactivated on the previous rail. If that does not occur, the power-down of subsequent rails is paused. To allow for power-down in case of biased or shorted rails, the sequence continues despite an incomplete discharge of the previous rail after eight times the slot-duration (or 12ms in case of slot-duration of 0ms).
- To bypass the discharge-check, set the BYPASS_RV_FOR_RAIL_ENABLE bit in the GENERAL_CONFIG register to '1'.

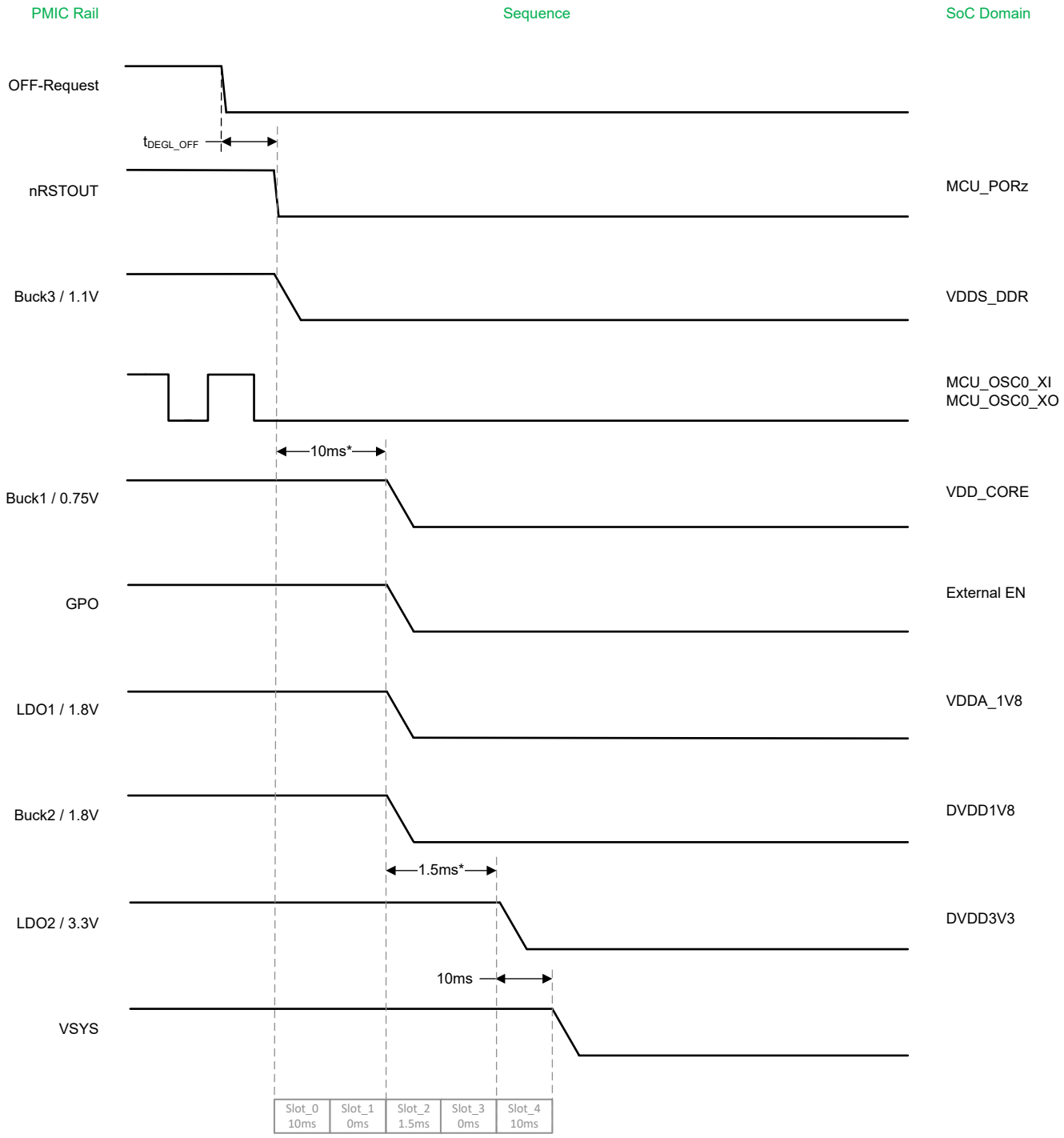
Note

In case active discharge on a rail is deactivated, unsuccessful discharge of the rail within the slot duration does not gate the power down of the subsequent rail, but the sequence is purely timing based. In case of residual voltage, the RV-bit is set regardless.

Active discharge is enabled by default and not NVM based. Thus, if desired, discharge needs to be deactivated after each VSYS-power-cycle. During RESET or OFF-request, the discharge configuration is not reset, as long as VSYS is present. However, in INITIALIZE state and prior to the power-up-sequence, all rails get discharged, regardless of the setting.

During the power-down-sequence, non-NVM-backed bits get reset, with the exception of *_DISCHARGE_EN bits and certain interrupt bits. See Table 7-8 for details.

Below graphic shows the power-down-sequence for NVM-ID 0x01, revision 0x2 as an example:



* discharge-duration depends on Vout, Cout and load. Slot-duration needs to adopt. Slot-duration extends up to 8x its configured value.

Figure 7-3. Power-Down Sequencing (Example)

CAUTION

Do not change the registers related to an ongoing sequence by I2C-command!

Non-NVM-bits are not accessible for approximately 80µs after starting a transition into INITIALIZE state.

7.3.3 Push Button and Enable Input (EN/PB/VSENSE)

The EN/PB/VSENSE pin is used to enable the PMIC. The pin can be configured in three ways:

Device Enable (EN)

When configured as EN, this pin needs to be pulled high to generate an ON-request. Pulling this pin low generates an OFF-request.

- The deglitch-time of the EN-pin is configured by EN_PB_VSENSE_DEGL in MFP_2_CONFIG register.
- The power-up sequence starts if the EN input is above the V_{IL}-threshold low for the configured $t_{DEGL\_EN\_Rise}$.
- To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER_UP_FROM_EN_PB_VSENSE in POWER_UP_STATUS_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
- The power-down sequence starts if the EN input is below the V_{IH}-threshold for $t_{DEGL\_EN\_Fall}$.
- In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence if EN input is still above the V_{IH}-threshold. (EN considered level-sensitive)
- In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required. The device automatically executes the power-up sequence if EN input is still above the V_{IH}-threshold. (EN considered level-sensitive)
- In case EN is pulled low after entering SLEEP state, the pin must be pulled high again to enter the INITIALIZE state. EN must remain high for $t_{EN\_PB\_WAKEUP}$ to continue to the ACTIVE state. If EN is pulled low before $t_{EN\_PB\_WAKEUP}$ elapses, the device re-enters the SLEEP state.

Push-Button (PB)

When configured as PB, a CMOS-type input used to power-up the PMIC. Typically, the PB pin is connected to a momentary switch to ground and an external pullup resistor.

- The hold-time of the push-button is configured by EN_PB_VSENSE_DEGL in MFP_2_CONFIG register.
- The power-up sequence starts if the PB input is below the V_{IL}-threshold low for the configured t_{PB_ON}.
- To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER_UP_FROM_EN_PB_VSENSE in POWER_UP_STATUS_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
- The PB pin has a rising-edge deglitch $t_{DEGL\_PB\_RISE}$ to filter bouncing of the switch
- The power-down sequence starts if the PB input is held low for t_{PB_OFF}-time (not configurable).
- In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence without a PB-press.
- In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required. The device automatically executes the power-up sequence without a PB-press.
- In case the device is in SLEEP state, a falling edge on PB transitions to the INITIALIZE state. PB must remain low for $t_{EN\_PB\_WAKEUP}$ to continue to the ACTIVE state. If PB is is released before $t_{EN\_PB\_WAKEUP}$ elapses, the device re-enters the SLEEP state.
- A push-button press is only recognized after VSYS is above VSYS_POR-threshold or the PB must be held long enough after VSYS is above VSYS_POR-threshold.
- Following bits in the signify the PB-press events:
  - PB_FALLING_EDGE_DETECTED: PB was pressed for for a time-interval longer than $t_{DEGL\_PB\_INT}$ since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB='0'). Write W1C to clear.

- PB_RISING_EDGE_DETECTED: PB was released for a time-interval longer than $t_{DEGL\_PB\_INT}$ since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB='0'). Write W1C to clear.
- PB_REAL_TIME_STATUS: Deglitched ($t_{DEGL\_PB\_INT}$) real-time status of PB pin. Valid only when EN/PB/VSENSE pin is configured as PB. This bit does not assert the nINT pin.

Power-Fail Comparator Input (VSENSE)

When configured as VSENSE, this pin can be used to sense the supply-voltage of the pre-regulator. Connect a resistor divider from the pre-regulator output to configure the sense voltage.

- The deglitch-time of the VSENSE-pin is configurable by EN_PB_VSENSE_DEGL in MFP_2_CONFIG register.
- Power-up is gated by VSYS being above the $VSYS_{POR\_Rising}$-threshold and the VSENSE input is above the V_{VSENSE}-threshold (not deglitched)
- The power-up sequence starts if the VSENSE input rises above V_{VSENSE}.
- To signify the power-up based on an EN/PB/VSENSE pin-event, the device sets bit POWER_UP_FROM_EN_PB_VSENSE in POWER_UP_STATUS_REG register. This bit does not assert the nINT pin. Write W1C to clear the bit.
- The power-down sequence starts if the VSENSE input falls below the V_{VSENSE}-threshold for $t_{DEGL\_VSENSE\_Fall}$, to avoid an un-sequenced power-off due to the loss of VSYS-supply-voltage.
- In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power-up sequence if VSENSE input is still above the V_{VSENSE}-threshold.
- In case of a cold reset (regardless if by RESET-pin or I2C-request), no renewed on-request is required. The device automatically executes the power-up sequence if VSENSE input is still above the V_{VSENSE}-threshold.
- In case the device is in SLEEP state, VSENSE cannot be used to transition directly to the INITIALIZE state. The device can only enter INITIALIZE following the OFF state.

7.3.4 OFF-Request by I2C Command

An OFF-request can also be triggered by an I2C-command to I2C_OFF_REQ in MFP_CTRL register. After such an OFF-request, a new ON-request is required:

- In case of EN-configuration, the EN input requires a rising edge (EN considered edge-sensitive)
- In case of PB-configuration, the PB needs to be pressed for a valid ON-request
- In case of VSENSE-configuration, the VSENSE input requires a rising edge (VSENSE considered edge-sensitive). A rising edge on the VSENSE input can be achieved by power cycling the pre-regulator.
- The falling-edge deglitch time for EN or VSENSE configuration $t_{DEGL\_EN/VSENSE\_I2C}$ is shorter than the deglitch-time for pin-induced OFF-requests ($t_{DEGL\_EN\_Fall}$ and $t_{DEGL\_VSENSE\_Fall}$). The deglitch-times for PB-configuration remain.

7.3.5 First Supply Detection (FSD)

First Supply detection (FSD) allows power-up as soon as supply voltage is applied, even if EN/PB/VSENSE pin is at OFF_REQ status. FSD can be used in combination with any ON-request configuration, EN, PB or VSENSE, and is enabled by setting bit PU_ON_FSD in register MFP_2_CONFIG. At first power-up the EN/PB/VSENSE pin is treated as if the pin had a valid ON request. Once VSYS is above the $VSYS_{POR\_Rising}$-threshold, the PMIC

- loads the NVM
- enters INITIALIZE state
- initiates the power-up-sequence, regardless of the EN/PB/VSENSE-pin-state

To signify the power-up based on FSD, the device sets bit POWER_UP_FROM_FSD in POWER_UP_STATUS_REG register. The nINT-pin does not toggle based on this bit. Write W1C to clear the bit.

The EN/PB/VSENSE-pin is treated as if the pin had a valid ON-request until valid entry into the ACTIVE state (at the expiration of the last slot in the power-up-sequence). Following entry into the ACTIVE state, the device adheres to post-deglitch EN/PB/VSENSE-pin-status: if pin status has changed prior to entering ACTIVE state or in ACTIVE state, the device does adhere to the pin state. For example, if the EN/PB/VSENSE-pin is configured for EN, the device does power down in case the EN-pin is low (for longer than the deglitch time) at the time the

device enters ACTIVE state. The duration for how long the ON-request is considered valid, regardless of the pin-state, can be controlled by length of nRSTOUT slot (and empty slots thereafter), as the PMIC enters ACTIVE state only after the last slot of the sequence expired.

7.3.6 Input Voltage Slew Rate With Automatic Power-up

Note

For a stable power-up, sufficient input-to-output voltage headroom is required for each output rail when the rail is enabled in the power sequence. The required headroom are specified as $V_{HEADROOM\_PWM}$ for the buck regulators and $V_{DROPOUT}$ for the LDOs.

In applications where the PMIC is expected to power up automatically with the system input voltage, (for example, when FSD is enabled or EN externally pulled up to VSYS/PVIN_LDO12), the device starts the power sequence after the input voltage reaches $VSYS_{POR\_Rising}$ and t_{NVM_LOAD} elapses. The required input voltage slew rate to support each regulator is calculated based on the headroom requirement and the assigned slot *y* in the power sequence. For output rails assigned to SLOT_0, the calculation only needs to include t_{NVM_LOAD}. Cases where SR_{VIN} is zero or negative do not need to be considered since the minimum input voltage required for regulation is already met at the $VSYS_{POR\_Rising}$ threshold. For all other cases, the pre-regulator that generates the system input voltage must meet the highest required slew rate.

$$SR_{VSYS} \geq \frac{V_{OUT} + V_{HEADROOM} - VSYS_{POR\_Rising}}{t_{NVM\_LOAD} + t_{SLOT\_0} + t_{SLOT\_1} + \cdots + t_{SLOT\_(y-1)}} \left(V/ms\right) \quad (1)$$

If the highest required slew rate is not supported, the insufficient headroom for the output rail creates a -UV fault once enabled in the power sequence. The device increments RETRY_COUNT and attempts to power up 2 more times as shown in Figure 7-4. If the input voltage still does not provide sufficient headroom for the output rail, the device enters the INITIALIZE state until VSYS/PVIN_LDO12 is cycled to renew an ON-request.

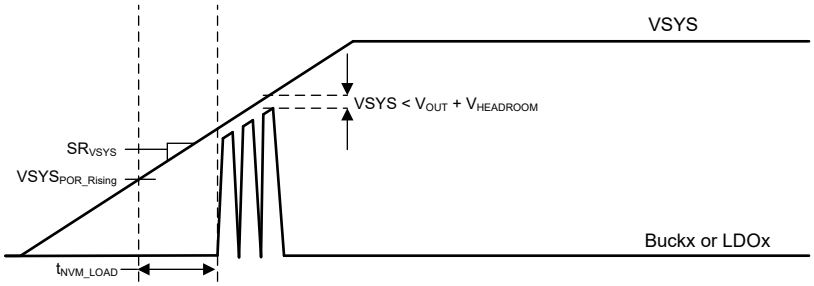


Figure 7-4. VSYS Slow Ramp With FSD and MASK_RETRY_COUNT_ON_FIRST_PU = '0'

For applications that require automatic power-up and cannot meet the slew rate requirements, the RETRY_COUNT can be masked on the first power up by bit MASK_RETRY_COUNT_ON_FIRST_PU in register MFP_2_CONFIG. When this bit is set, the device masks RETRY_COUNT until after the power-up sequence is completed as shown in Figure 7-5. After power-up, the RETRY_COUNT is unmasked to enable a device shutdown in the event of a permanent fault.

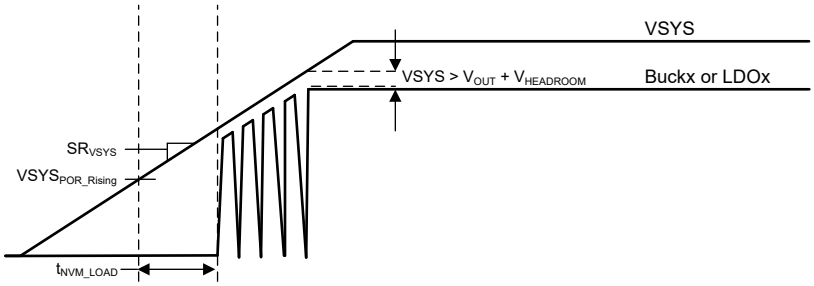


Figure 7-5. VSYS Slow Ramp With FSD and MASK_RETRY_COUNT_ON_FIRST_PU = '1'

7.3.7 Buck Converters (Buck1, Buck2, and Buck3)

The TPS65214 provides three buck converters. Buck1 is capable of supporting up to 2A of load current. Buck2 and Buck3 are capable of supporting up to 2A of load current. The buck converters have an input voltage range from 2.5V - 5.5V, and can be connected either directly to the system power or the output of another buck converter. The output voltage is programmable in the range of 0.6V - 3.4V: in 25mV-steps up to 1.4V, in 100mV-steps between 1.4V and 3.4V.

- The ON/OFF state of the buck converters in ACTIVE state is controlled by the corresponding BUCKx_EN bit in the ENABLE_CTRL register.
- The ON/OFF state of the buck converters in STBY state is controlled by the corresponding BUCKx_STBY_EN bit in the STBY_1_CONFIG register.
- In INITIALIZE and SLEEP state, the buck converters are off, regardless of bit-settings.

CAUTION
In case of buck-regulators that are not to be used at all, the FB_Bx pin must be tied to GND and the LX_Bx pin must be left floating.

- The converters activity can be controlled by the sequencer or through I2C communication.

Buck Switch Modes: Quasi-Fixed-Frequency Mode

The converters can operate in forced-PWM mode, irrespective of load-current, or can be allowed to enter pulse-frequency-modulation (PFM) for low load-currents. The mode is controlled by the MODE/STBY pin when configured as 'MODE' or 'MODE&STBY'. An I2C-command to MODE_I2C_CTRL bit in MFP_1_CONFIG register can also configure the buck converters for forced-PWM or PFM operation. For more details see Pin Configuration and Functions and PWM/PFM and Low Power Modes (MODE/STBY).

- During a transition to ACTIVE state or to INITIALIZE state, the buck converters operate in forced-PWM, irrespective of the pin-state. PFM-entry is allowed once the device enters the ACTIVE state, upon completion of the sequence and expiration of the last power-up slot.
- In case of a DVFS-induced output voltage change, the TPS65214 temporarily forces the buck-regulators into PWM until the voltage change is completed. If PFM is allowed, the entry and exit into PFM is load-current dependent. PFM starts when the inductor current reaches 0A, which is the case at a load current approximately calculated by:

$$I_{LOAD} = \frac{1}{2} \times \frac{V_{PVIN\_Bx} - V_{BUCKx}}{L} \times \frac{V_{BUCKx}}{V_{PVIN\_Bx}} \times \frac{1}{f_{SW}} \quad (2)$$

Configurable Converter Bandwidth

The converters can be individually configured further for a high-bandwidth-mode for optimum transient-response or lower bandwidth, allowing minimum output filter capacitance. The selection is done by the BUCKx_BW_SEL bits in GENERAL_CONFIG register. This bit must only change if this regulator is not enabled. Please note the higher output-capacitance requirements for high bandwidth use case.

Externally Configurable Output Voltage

If GPIO/VSEL is configured as 'VSEL' by bit GPIO_VSEL_CONFIG in register MFP_1_CONFIG, the output voltage of Buck1 or Buck3 can be controlled by pulling the GPIO/VSEL pin high, low or leave the pin floating. These settings support multiple core supply voltages or DDR3LV, DDR4, and DDR4LV supply voltages without an NVM change. See General Purpose Inputs/Outputs and Voltage Select Pin (GPIO/VSEL) for details.

CAUTION
When GPIO/VSEL is configured for VSEL operation, the pin needs to be hard-wired and must not change during operation.

Active Discharge

The buck converters have an active discharge function. The discharge function can be deactivated individually per rail in the DISCHARGE_CONFIG register. If discharge is enabled, the device discharges the output is discharged to ground whenever a rail is deactivated.

- Prior to enabling a rail in the power sequence, the device discharges the rail to avoid starting into a pre-biased output.
- If a rail is enabled by an I2C-command, active discharge is not enforced, but the rail is only enabled if the output voltage is below the SCG-threshold.
- This register is not NVM-backed and does reset if the device enters OFF-state.
- When in INITIALIZE state (during RESET or an I2C-OFF-request), the discharge configuration is not reset. Note: the power-down-sequence can be violated if the discharge function is not enabled.

Dynamic Voltage Scaling

All buck converters support Dynamic Voltage Frequency Scaling (DVFS). The output-voltage can be changed during the operation to optimize the operating voltage for the operation point of the SoC in the lower output voltage range between 0.6V and 1.375V. The voltage change is controlled by writing to BUCKx_VSET in the corresponding BUCKx_VOUT register. During a DVFS-induced voltage transition, the active discharge function is temporarily enabled, irrespective of the discharge-configuration.

The buck converters can be configured for DVFS upon STBY-request via the MODE/STBY pin or I2C. When a STBY-request is received, all bucks that are enabled in the STBY_1_CONFIG register and configured for DVFS by bit BUCKx_DVS_STBY are changed to the output voltages specified by BUCKx_VSET_STBY in the corresponding BUCKx_VOUT_STBY registers. If BUCKx_DVS_STBY is cleared while in STBY, the output voltage reverts to BUCKx_VSET. If BUCKx_DVS_STBY is not set, the corresponding BUCKx output voltage is not changed when transitioning from the ACTIVE to STBY state. When transitioning back to ACTIVE state, the output voltage reverts to BUCKx_VSET.

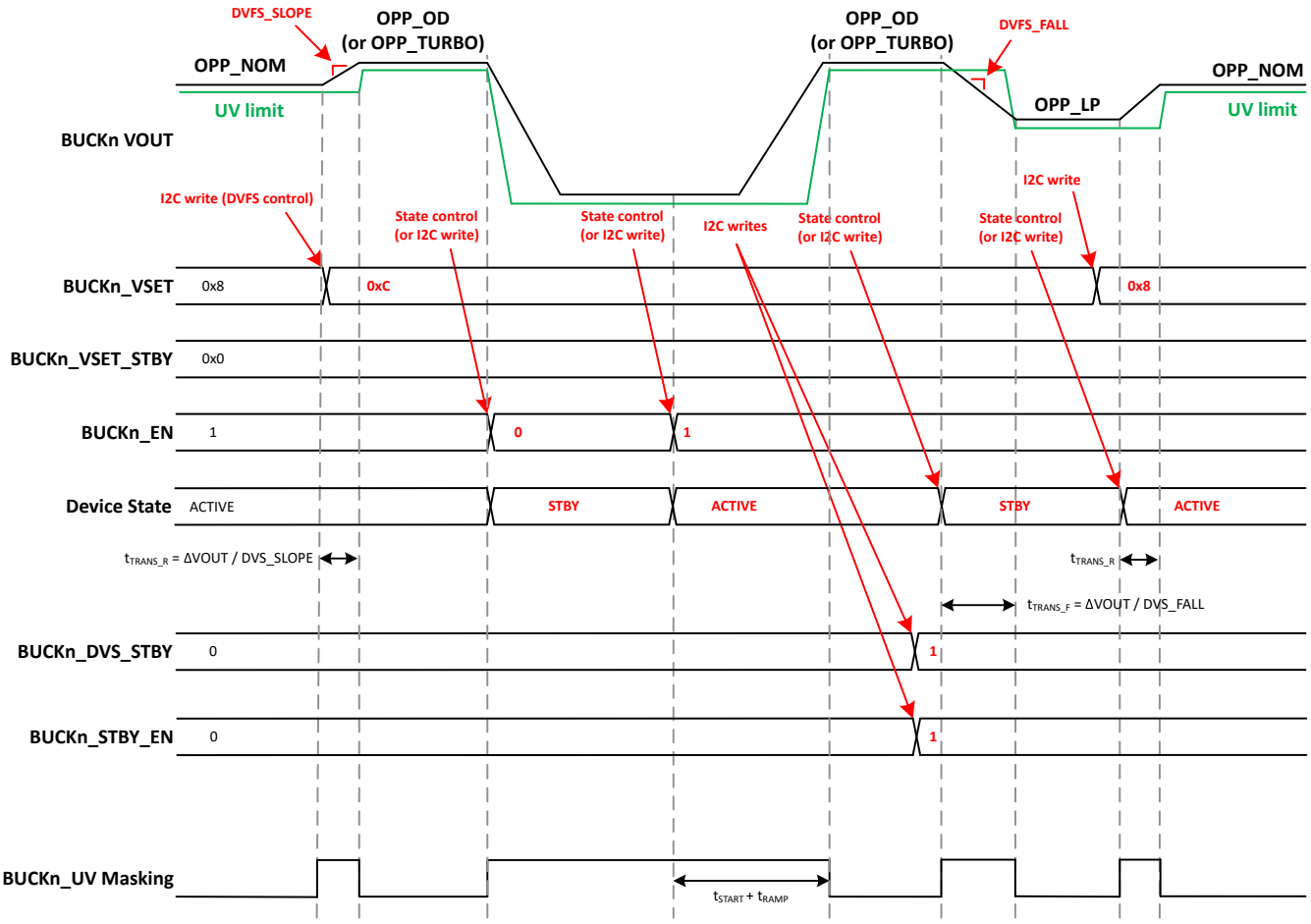


Figure 7-6. Buck DVS Timing Diagram

Output Capacitance Requirements

The buck converters require sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:

- For low-bandwidth configuration, a minimum capacitance of 10uF is required and a maximum total capacitance of 75uF is supported
- For high-bandwidth configuration, a minimum capacitance of 30uF is required and a maximum total capacitance of 220uF is supported

Buck Fault Handling

Undervoltage (UV) monitoring

The TPS65214 detects undervoltages on the buck converter outputs. The undervoltage threshold is configured by the BUCKx_UV_THR bit in the BUCKx_VOUT register. The reaction to an undervoltage detection is dependent on the configuration of the respective BUCKx_UV_MASK bit and the MASK_EFFECT bit in the MASK_CONFIG register. If not masked, the device sets the respective INT_BUCK_1_2_IS_SET or INT_BUCK_3_IS_SET bit in the INT_SOURCE register. The device also sets the corresponding BUCKx_UV bit in the INT_BUCK_1_2 or INT_BUCK_3 register.

During a voltage transition (for example, when triggered by a DVFS induced voltage change), the device blanks the undervoltage detection by default and activates the undervoltage detection when the voltage transition completed. If the device detects an undervoltage during the sequence into ACTIVE state (from INITIALIZE or STBY) and UV is not masked, the power-down-sequence starts at the end of the current slot.

If the device detects an undervoltage in ACTIVE-state or STBY-state and UV is not masked by bit BUCKx_UV_MASK in register INT_MASK_UV, the power-down sequence starts immediately. OC-detection is not maskable.

Over-Current (OC) Limit

The TPS65214 provides cycle-by-cycle current-limit on the buck converter outputs. If the device detects over-current for $t_{DEGLITCH\_OC\_short}$, respectively for $t_{DEGLITCH\_OC\_long}$ (configurable individually per rail with EN_LONG_DEGL_FOR_OC_BUCKx in OC_DEGL_CONFIG register; applicable for rising-edge only), the device sets INT_BUCK_1_2_IS_SET respectively INT_BUCK_3_IS_SET bit in INT_SOURCE register and bit BUCKx_OC (for positive over-current) respectively BUCKx_NEG_OC (for negative over-current) in INT_BUCK_1_2 respectively INT_BUCK_3 register.

During a voltage transition (for example, when triggered by a DVFS induced voltage change), the over current detection is blanked and only gets activated when the voltage transition is completed.

If the over-current occurs during the sequence into ACTIVE state (from INITIALIZE or STBY), the device deactivates the affected rail immediately and starts the power-down-sequence at the end of the current slot.

If the over-current occurs in ACTIVE-state or STBY-state, the device deactivates the affected rail immediately and starts the power-down sequence.

OC-detection is not maskable, but the deglitch-time is configurable. TI recommends configuring the shortest deglitch time, $t_{DEGLITCH\_OC\_short}$. Extended over-current can lead to increased aging or overshoot upon recovery.

Short-Circuit-to-Ground (SCG) Monitoring

The TPS65214 detects short-to-ground (SCG) faults on the buck-outputs. The reaction to the detection of an SCG event is to set INT_BUCK_1_2_IS_SET respectively INT_BUCK_3_IS_SET bit in INT_SOURCE register and bit BUCKx_SCG in INT_BUCK_1_2 respectively INT_BUCK_3 register. The affected rail is deactivated immediately. The device sequences down all outputs and transitions into the INITIALIZE state.

SCG-detection is not maskable.

If a rail gets enabled, the device blanks SCG detection initially to allow the rail to ramp above the SCG-threshold.

Residual Voltage (RV) Monitoring

The TPS65214 detects residual voltage (RV) faults on the buck-outputs. The reaction to the detection of an RV event is to set INT_RV_IS_SET bit in INT_SOURCE register and bit BUCKx_RV in INT_RV register. The RV-detection is not maskable, but the nINT-reaction can be configured globally for all rails by MASK_INT_FOR_RV in INT_MASK_WARM register. The BUCKx_RV-flag is set regardless of masking, INT_RV_IS_SET bit is only set if nINT is asserted. The fault-reaction time and potential state-transition depends on the situation when residual voltage is detected:

- If the device detects residual voltage during power-up, ACTIVE_TO_STANDBY, or STANDBY_TO_ACTIVE sequences, the sequence is aborted and the device powers down. The shutdown-fault-reaction is maskable by bit BYPASS_RV_FOR_RAIL_ENABLE in register GENERAL_CONFIG.
- If the device detects residual voltage for more than 80ms on any rail that was deactivated during STBY state during a request to leave STBY state, the device transitions into INITIALIZE state. The device sets the BUCKx_RV-bit if the condition persists for 4ms to 5ms, but less than 80ms.
- If residual voltage is detected during an EN-command of the rail by I2C, the BUCKx_RV-flag is set immediately, but no state transition occurs.

Temperature Monitoring

The buck converters have a local over-temperature sensor. The reaction to a temperature warning is dependent on the configuration of the respective SENSOR_x_WARM_MASK bit in MASK_CONFIG register and the MASK_EFFECT bits in INT_MASK_BUCKS register. If the temperature at the sensor exceeds T_{WARM_Rising} and is not masked, the device sets INT_SYSTEM_IS_SET bit in INT_SOURCE register and SENSOR_x_WARM

bit in INT_SYSTEM register. In case the sensor detects a temperature exceeding T_{HOT_Rising} , the converters power dissipation and junction temperature exceeds safe operating value. The device powers down all active outputs immediately and sets INT_SYSTEM_IS_SET bit in INT_SOURCE register and SENSOR_x_HOT bit in INT_SYSTEM register. The TPS65214 automatically recovers once the temperature drops below the $T_{WARM\_Falling}$ threshold value (or below the $T_{HOT\_Falling}$ threshold value in case T_WARM is masked). The _HOT bit remains set and needs to be cleared by writing '1'. The HOT-detection is not maskable.

CAUTION

The buck can only supply output currents up to the respective current limit, including during start-up. Depending on the charge-current into the filter- and load-capacitance, the device potentially cannot drive the full output current to the load while ramping. As a rule of thumb, for a total load-capacitance exceeding 50µF, the load current must not exceed 25% of the rated output current. This limit applies also for dynamic output-voltage changes.

CAUTION

The TPS65214 does not offer differential feedback pins. The device does not support remote sensing. Since a single-ended trace is susceptible to noise and must be as short as possible and thus connect directly to the output filter.

Table 7-1. BUCK Output Voltage Settings

BUCKx_VSET [decimal]	BUCKx_VSET [binary]	BUCKx_VSET [hexadecimal]	VOUT (Buck1 & Buck2 and Buck3) [V]
0	000000	00	0.600
1	000001	01	0.625
2	000010	02	0.650
3	000011	03	0.675
4	000100	04	0.700
5	000101	05	0.725
6	000110	06	0.750
7	000111	07	0.775
8	001000	08	0.800
9	001001	09	0.825
10	001010	0A	0.850
11	001011	0B	0.875
12	001100	0C	0.900
13	001101	0D	0.925
14	001110	0E	0.950
15	001111	0F	0.975
16	010000	10	1.000
17	010001	11	1.025
18	010010	12	1.050
19	010011	13	1.075
20	010100	14	1.100
21	010101	15	1.125
22	010110	16	1.150
23	010111	17	1.175
24	011000	18	1.200
25	011001	19	1.225
26	011010	1A	1.250

Table 7-1. BUCK Output Voltage Settings (continued)

BUCKx_VSET [decimal]	BUCKx_VSET [binary]	BUCKx_VSET [hexadecimal]	VOUT (Buck1 & Buck2 and Buck3) [V]
27	011011	1B	1.275
28	011100	1C	1.300
29	011101	1D	1.325
30	011110	1E	1.350
31	011111	1F	1.375
32	100000	20	1.400
33	100001	21	1.500
34	100010	22	1.600
35	100011	23	1.700
36	100100	24	1.800
37	100101	25	1.900
38	100110	26	2.000
39	100111	27	2.100
40	101000	28	2.200
41	101001	29	2.300
42	101010	2A	2.400
43	101011	2B	2.500
44	101100	2C	2.600
45	101101	2D	2.700
46	101110	2E	2.800
47	101111	2F	2.900
48	110000	30	3.000
49	110001	31	3.100
50	110010	32	3.200
51	110011	33	3.300
52	110100	34	3.400
53	110101	35	3.400
54	110110	36	3.400
55	110111	37	3.400
56	111000	38	3.400
57	111001	39	3.400
58	111010	3A	3.400
59	111011	3B	3.400
60	111100	3C	3.400
61	111101	3D	3.400
62	111110	3E	3.400
63	111111	3F	3.400

7.3.8 Linear Regulators (LDO1 and LDO2)

The TPS65214 offers a total of two linear regulators. LDO1 is a general purpose LDO intended to provide power to analog circuitry on the SOC or peripherals. The LDO supports an output current of 300mA. LDO2 is a general purpose LDO intended to provide power to digital circuitry on the SOC and peripherals. The LDO supports an output current of 500mA.

Operational Modes

Both LDO1 and LDO2 have an input voltage range from 2.5V to 5.5V, and must be connected directly to the system power. The output voltage is programmable in the range of 0.6V to 3.3V in 50 mV-steps. The LDOs support Load-switch mode (LSW_mode): in this case, output voltages of 2.5V up to 3.4V are supported. In LSW_mode, the desired voltage does not need to be configured in the LDOx_VOUT register.

- The LDOs can be configured as linear regulators or configured as a load-switch (LSW-mode). The mode is configured by LDOx_LSW_CONFIG bit in LDOx_VOUT register.

CAUTION
In LSW-mode, the LDO acts as a switch, where VOUT is VIN minus the drop over the FET-resistance (R_{LSW}).

- The ON/OFF state of the LDOs in ACTIVE state is controlled by the corresponding LDOx_EN bit in the ENABLE_CTRL register.
- The ON/OFF state of the LDOs in STBY state is controlled by the corresponding LDOx_STBY_EN bit in the STBY_1_CONFIG register.
- In INITIALIZE and SLEEP state, the LDOs are off, regardless of bit-settings.

CAUTION
In case of linear regulators that are not to be used at all, the VLDOx pin must be left floating.

Active Discharge

The LDOs have an active discharge function. Whenever LDOx is not enabled, the output is discharged to ground. The discharge function can be deactivated individually per rail in the DISCHARGE_CONFIG register.

- Prior to enabling a rail in the power sequence, the device discharges the rail to avoid starting into a pre-biased output.
- If a rail is enabled by an I2C-command, active discharge is not enforced, but the rail is only enabled if the output voltage is below the SCG-threshold.
- This register is not EEPROM-backed and is reset if the device enters OFF-state.
- When in INITIALIZE state (during RESET or an I2C-OFF-request), the discharge configuration is not reset. Note: the power-down-sequence can be violated if the discharge function is not enabled.

Dynamic Voltage Scaling

All LDOs support Dynamic Voltage Scaling (DVS). The output-voltage can be changed during the operation to optimize the operating voltage for the operation point of the load. The voltage change is controlled by writing to LDO1_VSET or LDO2_VSET in the corresponding LDO1_VOUT or LDO2_VOUT register. During a DVS-induced voltage transition, the active discharge function is temporarily enabled, irrespective of the discharge-configuration.

The LDOs can be configured for DVS upon STBY-request via the MODE/STBY pin or I2C. When a STBY-request is received, all LDOs that are enabled in the STBY_1_CONFIG register and configured for DVFS by bit LDOx_DVS_STBY are changed to the output voltages specified by LDOx_VSET_STBY in the LDOx_VOUT_STBY registers. If LDOx_DVS_STBY is cleared while in STBY, the output voltage reverts to LDOx_VSET. If LDOx_DVS_STBY is not set, the corresponding LDOx output voltage is not changed when transitioning from the ACTIVE to STBY state.

CAUTION
When an LDO is configured for DVS in STBY, the corresponding power-up slot duration must be long enough to support the complete voltage ramp during the STBY to ACTIVE power sequence. If the slot duration is not long enough, the device registers a TIMEOUT fault.

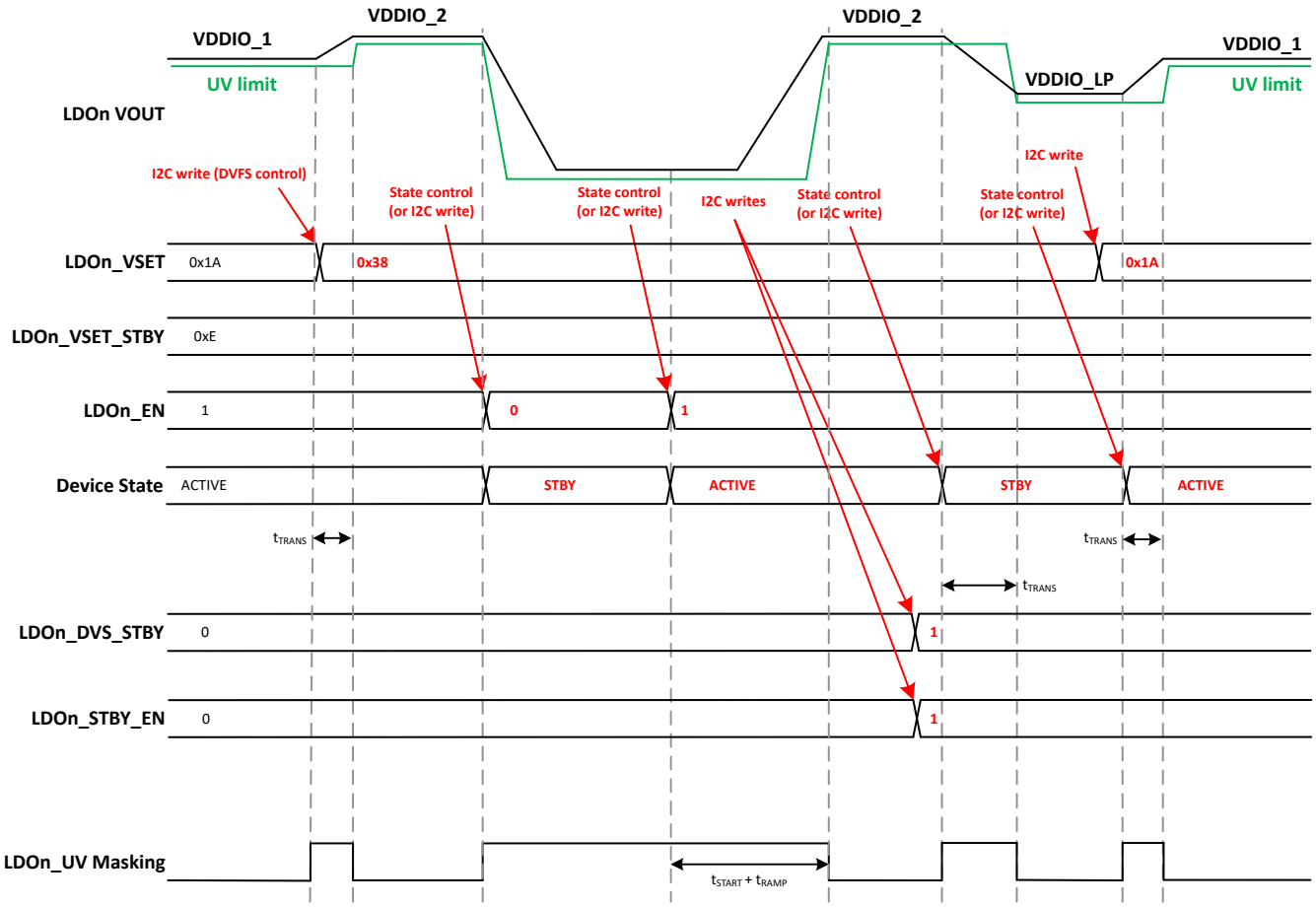


Figure 7-7. LDO DVS Timing Diagram

Output Capacitance Requirements

The LDO regulators require sufficient output-capacitance for stability. The required minimum and supported maximum capacitance depends on the configuration:

- In LDO-mode, a minimum capacitance of 1.2uF is required and a maximum total load capacitance (output filter and point-of-load combined) of 40uF is supported
- In LSW-mode, a minimum capacitance of 1.2uF is required and a maximum total capacitance (output filter and point-of-load combined) of 50uF is supported

LDO Fault Handling

Undervoltage (UV) Monitor

The TPS65214 detects undervoltages on the LDO-outputs. The undervoltage threshold is configured by the LDOx_UV_THR bit in the LDOx_VOUT register. The reaction to an undervoltage detection is dependent on the configuration of the LDOx_UV_MASK bit in INT_MASK_LDO register and the MASK_EFFECT in INT_MASK_BUCKS register. If not masked, the device sets bit INT_LDO_1_2_IS_SET in INT_SOURCE register and bit LDOx_UV in INT_LDO_1_2 register.

During a voltage transition (for example, at power-up), the device blanks
the undervoltage detection by default and activates the undervoltage detection when the voltage transition completed. If the device detects an undervoltage during the sequence into ACTIVE state (from INITIALIZE or STBY) and UV is not masked, the power-down-sequence starts at the end of the current slot.

If the device detects an undervoltage during the sequence into ACTIVE state (from INITIALIZE or STBY) and UV is not masked, the power-down-sequence starts at the end of the current slot.

If the device detects an undervoltage in ACTIVE-state or STBY-state and UV is not masked, the power-down sequence starts immediately. OC-detection is not maskable.

CAUTION
If a LDO is configured in LSW-mode, UV-detection is not supported.

Over-Current (OC) Limit

The TPS65214 provides current-limit on the LDO-outputs. If the PMIC detects over-current for $t_{DEGLITCH\_OC\_short}$, respectively for $t_{DEGLITCH\_OC\_long}$ (configurable individually per rail with EN_LONG_DEGL_FOR_OC_LDOx in OC_DEGL_CONFIG register; applicable for rising-edge only), the device sets INT_LDO_1_2_IS_SET in INT_SOURCE register and bit LDOx_OC in INT_LDO_1_2. The effected rail is deactivated immediately.

During a voltage transition (for example, at power-up), the overcurrent detection is blanked and gets activated when the voltage transition completed.

If the over-current occurs during the sequence into ACTIVE state (from INITIALIZE or STBY), the device deactivates the affected rail immediately and starts the power-down-sequence at the end of the current slot.

If the over-current occurs in ACTIVE-state or STBY-state, the device deactivates the affected rail immediately and starts the power-down sequence.

OC-detection is not maskable, but the deglitch-time is configurable. TI recommends to use $t_{DEGLITCH\_OC\_short}$. Extended over-current can lead to increased aging or overshoot upon recovery.

Short-Circuit-to-Ground (SCG) Monitor

The TPS65214 detects short-to-ground (SCG) faults on the LDO-outputs. The reaction to the detection of an SCG event is to set INT_LDO_1_2_IS_SET in INT_SOURCE register and bit LDOx_SCG in INT_LDO_1_2 register. The affected rail is deactivated immediately. The device sequences down all outputs and transitions into INTIALIZE state.

SCG-detection is not maskable.

If a rail gets enabled, the device blanks SCG detection initially to allow the rail to ramp above the SCG-threshold.

Residual Voltage (RV) Monitor

The TPS65214 detects residual voltage (RV) faults on the LDO-outputs. The reaction to the detection of an RV event is to set INT_RV_IS_SET bit in INT_SOURCE register and bit LDOx_RV in INT_RV register. The RV-detection is not maskable, but the nINT-reaction can be configured globally for all rails by MASK_INT_FOR_RV in INT_MASK_WARM register. The device sets the LDOx_RV-flag regardless of masking, INT_RV_IS_SET bit is only set if nINT is asserted. The fault-reaction time and potential state-transition depends on the situation when the faults are detected:

- If the device detects residual voltage during power-up, ACTIVE_TO_STANDBY, or STANDBY_TO_ACTIVE sequences, the sequence is aborted and the device powers down. The shutdown-fault-reaction is maskable by bit BYPASS_RV_FOR_RAIL_ENABLE in register GENERAL_CONFIG.
- If the device detects residual voltage for more than 80ms on any rail that was deactivated during STBY state during a request to leave STBY state, the device transitions into INITIALIZE state. The device sets the LDOx_RV-bit if the condition persists for 4ms to 5ms, but less than 80ms.
- If residual voltage is detected during an EN-command of the rail by I2C, the LDOx_RV-bit is set immediately, but no state transition occurs.

Temperature Monitor

The LDOs have a local over-temperature sensor. The reaction to a temperature warning is dependent on the configuration of the respective SENSOR_x_WARM_MASK bit in and the MASK_EFFECT bit in INT_MASK_BUCKS register. If the temperature at the sensor exceeds T_{WARM_Rising} and is not masked, the device sets INT_SYSTEM_IS_SET bit in INT_SOURCE register and SENSOR_x_WARM bit in INT_SYSTEM register. In case the sensor detects a temperature exceeding T_{HOT_Rising} , the converters power dissipation and junction temperature exceeds safe operating value. The device powers down all active outputs immediately and sets INT_SYSTEM_IS_SET bit in INT_SOURCE register and SENSOR_x_HOT bit in INT_SYSTEM register. The TPS65214 automatically recovers once the temperature drops below the $T_{WARM\_FAlling}$ threshold value (or below the $T_{HOT\_FAlling}$ threshold value in case T_WARM is masked). The _HOT bit remains set and needs to be cleared by writing '1'. The HOT-detection is not maskable.

Table 7-2. LDO Output Voltage Settings

LDOx_ VSET [decimal]	LDOx_VSET [binary]	LDOx_ VSET [hexa- decimal]	VOUT (LDO1 and LDO2, LDO mode) [V]
0	000000	00	0.60
1	000001	01	0.60
2	000010	02	0.60
3	000011	03	0.65
4	000100	04	0.70
5	000101	05	0.75
6	000110	06	0.80
7	000111	07	0.85
8	001000	08	0.90
9	001001	09	0.95
10	001010	0A	1.00
11	001011	0B	1.05
12	001100	0C	1.10
13	001101	0D	1.15
14	001110	0E	1.20
15	001111	0F	1.25
16	010000	10	1.30
17	010001	11	1.35
18	010010	12	1.40
19	010011	13	1.45
20	010100	14	1.50
21	010101	15	1.55
22	010110	16	1.60
23	010111	17	1.65
24	011000	18	1.70
25	011001	19	1.75
26	011010	1A	1.80
27	011011	1B	1.85
28	011100	1C	1.90

Table 7-2. LDO Output Voltage Settings (continued)

LDOx_ VSET [decimal]	LDOx_VSET [binary]	LDOx_ VSET [hexa- decimal]	VOUT (LDO1 and LDO2, LDO mode) [V]
29	011101	1D	1.95
30	011110	1E	2.00
31	011111	1F	2.05
32	100000	20	2.10
33	100001	21	2.15
34	100010	22	2.20
35	100011	23	2.25
36	100100	24	2.30
37	100101	25	2.35
38	100110	26	2.40
39	100111	27	2.45
40	101000	28	2.50
41	101001	29	2.55
42	101010	2A	2.60
43	101011	2B	2.65
44	101100	2C	2.70
45	101101	2D	2.75
46	101110	2E	2.80
47	101111	2F	2.85
48	110000	30	2.90
49	110001	31	2.95
50	110010	32	3.00
51	110011	33	3.05
52	110100	34	3.10
53	110101	35	3.15
54	110110	36	3.20
55	110111	37	3.25
56	111000	38	3.30
57	111001	39	3.30
58	111010	3A	3.30
59	111011	3B	3.30
60	111100	3C	3.30
61	111101	3D	3.30
62	111110	3E	3.30
63	111111	3F	3.30

7.3.9 Reset to SoC (nRSTOUT)

The reset output (nRSTOUT) is an open-drain output, intended to release the reset to the SoC or FPGA at the end of the power-up sequence. The timing for nRSTOUT is configured in the sequence. nRSTOUT is driven low until the device enters ACTIVE state or when powering-down from ACTIVE- or STBY-state. The pin is driven high during ACTIVE state. In STBY-state, the pin is driven high or low depending on bit nRSTOUT_STBY_CONFIG in register STBY_2_CONFIG.

7.3.10 Interrupt Pin (nINT)

During power-up, the output of the nINT pin does depend on whether any INT_SOURCE flags are set and the configuration of the MASK_EFFECT bit in INT_MASK_BUCKS register-. If one or more flags are set, then nINT pin is pulled low and is only released high after those flags have been cleared by writing ‘1’ to them. Note, the nINT-pin can only transition 'high' if a VIO-voltage for the pull-up is available.

In SLEEP state, the nINT pin is always released high. In ACTIVE or STBY state, the nINT pin can be driven low to signal an event or fault condition to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is driven low. In case the device transitions to INITIALIZE state, the nINT pin is pulled low as well, regardless if the transition is triggered by an OFF-request or a fault.

If the fault is no longer present, a W1C (write '1' to clear) needs to be performed on the failure bits. This command also allows the nINT-pin to release (return to Hi-Z state). If the failure persists, the corresponding bit remains set and the INT pin remains low.

The UV-faults can be individually masked per rail in INT_MASK_UV registers. The thermal sensors can individually be masked by SENSOR_x_WARM_MASK in the MASK_CONFIG register. The effect of the masking for UV and WARM is defined globally by MASK_EFFECT bits in MASK_CONFIG register.

The nINT reaction for RV-faults is defined globally by MASK_INT_FOR_RV bits in MASK_CONFIG register.

- 00b = no state change, no nINT reaction, no bit set
- 01b = no state change, no nINT reaction, bit set
- 10b = no state change, nINT reaction, bit set (same as 11b)
- 11b = no state change, nINT reaction, bit set (same as 10b)

CAUTION

Masking poses a risk to the device or the system. In case the masking is performed by I2C-command, the masking bits do get reset to NVM-based default after transitioning to INITIALIZE state. Bits corresponding to faults newly configured via I2C as SD-faults do not get cleared.

TI does not recommend masking OC- and UV-detection on the same rail.

7.3.11 PWM/PFM and Low Power Modes (MODE/STBY)

The TPS65214 supports low power modes through the I2C-control or through the MODE/STBY pin. The configuration of the pin is selected by MODE_STBY_CONFIG in MFP_2_CONFIG register. The polarity of this pin can be configured by writing to MODE_STBY_POLARITY in MFP_1_CONFIG register. The polarity-configuration must not change after power-up.

MODE/STBY Configured as 'MODE'

If configured as 'MODE', the pin-status determines the switching-mode of the buck-converters. Forcing this pin for longer than $t_{DEGLITCH\_MFP}$ forces the buck-regulators into PWM-mode (irrespective of load current). De-asserting this pin low allows the buck regulators to enter PFM-mode. The entry into PFM and exit from PFM is governed by the load current.

- The selection of auto-PFM/forced-PWM can also be controlled by writing to the bit MODE_I2C_CTRL in MFP_1_CONFIG register.
- A change of the MODE does not cause a state-transition.
- During power-up of any one of the three bucks, a MODE change is blanked on this rail and only takes effect after the ramp completed.

Table 7-3. MODE Configuration

Pin	Pin-Setting	Polarity	Pin-State	MODE_I2C_CTRL bit	Device Mode
MODE/STBY	MODE	x	x	1	forced PWM
MODE/STBY	MODE	0	L	0	auto-PFM
MODE/STBY	MODE	0	H	0	forced PWM
MODE/STBY	MODE	1	L	0	forced PWM
MODE/STBY	MODE	1	H	0	auto-PFM

MODE/STBY Configured as 'STBY'

If configured as 'STBY', forcing this pin for longer than $t_{DEGLITCH\_MFP}$ sequences the device into the STBY or SLEEP state depending on bit STBY_SLEEP_CONFIG in register STBY_2_CONFIG.

- If configured for STBY state, the device sequences down the rails selected in the STBY_1_CONFIG and STBY_2_CONFIG registers. De-asserting this pin sequences the selected rails on again.
- If configured for SLEEP state, the device sequences down all rails and ignores the MODE/STBY pin state.

A transition into and out of STBY or SLEEP state can also be controlled by writing to the bit STBY_I2C_CTRL in MFP_CTRL register, provided I2C communication is supported during STBY state.

- A change of the MODE/STBY pin configured as 'STBY' does cause a state-transition by definition.
- Regardless of the pin-setting, the device always powers up into ACTIVE state. The device reacts to the STBY-pin-state or I2C-commands only after entering ACTIVE state.

Table 7-4. STBY Configuration

Pin	Pin-Setting	Polarity	Pin-State	STBY_I2C_CTRL bit	Device State
MODE/STBY	STBY	x	x	1	STBY or SLEEP
MODE/STBY	STBY	0	L	0	STBY or SLEEP
MODE/STBY	STBY	0	H	0	ACTIVE
MODE/STBY	STBY	1	L	0	ACTIVE
MODE/STBY	STBY	1	H	0	STBY or SLEEP

MODE/STBY Configured as 'MODE & STBY'

The pin can be configured to perform both functions, MODE and STBY simultaneously. The dual functionality is only realized when STBY_SLEEP_CONFIG is configured for STBY state.

Forcing this pin for longer than $t_{DEGLITCH\_MFP}$ sequences down the rails selected to turn off in the STBY_1_CONFIG and STBY_2_CONFIG registers (STBY function). Any buck-regulators configured to remain on in STBY operate in auto-PFM mode (MODE function). De-asserting this pin sequences the selected rails on again and forces the buck-regulators to forced-PWM. Polarity settings need to be harmonized for this configuration.

- If a transition into and out of STBY state is commanded by writing to the bit STBY_I2C_CTRL in MFP_CTRL register (provided I2C communication is supported during STBY state), a separate command for the MODE-change is required by writing to the bit MODE_I2C_CTRL in MFP_1_CONFIG register.
- A change of the MODE/STBY pin configured as 'MODE&STBY' does cause a state-transition by definition.

- By default STBY is deasserted and the pin is ignored until the device completed the power-up-sequence. During power-up of any one of the three bucks, a MODE-change is blanked on this rail and only takes effect after the ramp completed. A state-change commanded by STBY-pin is reacted to even during the ramp of rails (except during INITIALIZE-to-ACTIVE transition).

Please see below truth-table for pin- and I2C-commands.

Table 7-5. MODE and STBY Configuration

Pin	Pin-setting	Polarity	Pin-state	STBY_I2C_CTRL bit	MODE_I2C_CTRL bit	Device State	Device Mode
MODE/STBY	MODE & STBY	0	L	x	0	STBY or SLEEP	auto-PFM
MODE/STBY	MODE & STBY	0	L	x	1	STBY or SLEEP	forced PWM
MODE/STBY	MODE & STBY	0	H	0	x	ACTIVE	forced PWM
MODE/STBY	MODE & STBY	0	H	1	x	STBY or SLEEP	forced PWM
MODE/STBY	MODE & STBY	1	L	0	x	ACTIVE	forced PWM
MODE/STBY	MODE & STBY	1	L	1	x	STBY or SLEEP	forced PWM
MODE/STBY	MODE & STBY	1	H	x	0	STBY or SLEEP	auto-PFM
MODE/STBY	MODE & STBY	1	H	x	1	STBY or SLEEP	forced PWM

7.3.12 General Purpose Input/Output and Voltage Select Pin (GPIO/VSEL)

The TPS65214 GPIO/VSEL pin function can be configured through bit GPIO_VSEL_CONFIG in MFP_1_CONFIG register.

CAUTION
GPIO_VSEL_CONFIG must not change during operation.

GPIO/VSEL Configured as 'GPIO':

If configured as 'GPIO', the pin is configurable as an input or an output through bit GPIO_CONFIG in GENERAL_CONFIG register. GPIO configuration bits are changeable during device operation.

- When configured as an input, the pin level can be used as a sequence input with slot assignment by the GPIO_SEQUENCE_SLOT register with the corresponding slot duration. The internal sequencer waits for the GPIO/VSEL pin to reach the on state configured by the GPIO_SEQUENCE_POLARITY bit before proceeding with the power sequence. If the pin does not reach the on state within 80ms, the device sets the TIMEOUT bit and transitions to the INITIALIZE state.
- When configured as an output, the pin can be used to sequence external rails. The pin can be included in the power sequence or be controlled via I2C-interface, writing GPIO_EN in GENERAL_CONFIG register. The GPIO is released high if activated. The polarity is not changeable.

GPIO/VSEL Configured as 'VSEL':

If configured as 'VSEL', the pin level is used to set the output voltage of Buck1 or Buck3 through bit VSEL_RAIL in MFP_1_CONFIG register. The table below shows the various combinations.

CAUTION
VSEL functionality is hard-wired and must not change during operation.

Table 7-6. GPIO/VSEL Configuration options

GPIO_VSEL_CONFIG	GPIO_CONFIG	VSEL_RAIL	PIN Status	Output (V)	Rail
0:GPIO	0 = output	X	GPIO_EN	VIO	GPIO
0:GPIO	1 = input	X	Externally driven	n/a	GPIO
1:VSEL	X	0 = Buck1	0	BUCK1_VOUT	BUCK1
1:VSEL	X	0 = Buck1	open	0.75V	BUCK1
1:VSEL	X	0 = Buck1	1	1.1V	BUCK1
1:VSEL	X	1 = Buck3	0	BUCK3_VOUT	BUCK3
1:VSEL	X	1 = Buck3	open	1.1V	BUCK3
1:VSEL	X	1 = Buck3	1	1.2V	BUCK3

7.3.13 General Purpose Output and nWAKEUP (GPO/nWAKEUP)

The TPS65214 GPO/nWAKEUP function can be configured through bit GPO_nWAKEUP_CONFIG in MFP_2_CONFIG register. This function is changeable during operation.

GPO/nWAKEUP Configured as 'GPO'

If configured as 'GPO', the pin can be used to sequence external rails. The GPO can be included in the sequence or be controlled via I2C-interface, writing to GPO_EN in GENERAL_CONFIG register. The GPO is released high if activated. The polarity is not changeable.

GPO/nWAKEUP Configured as 'nWAKEUP'

If configured as 'nWAKEUP', the pin is a signal to the host indicating a power-on event. nWAKEUP is driven low prior to the device entering the INITIALIZE state and is held low until the device exits the INITIALIZE state. In all other states and state transitions, nWAKEUP is released high. The polarity is not changeable. See Device Functional Modes for details.

7.3.14 RESET-Request by I2C Command

A reset of the device can be triggered by writing to the bit WARM_RESET_I2C_CTRL respectively the bit COLD_RESET_I2C_CTRL in MFP_CTRL register. RESET requests via I2C are only serviced if the device is in ACTIVE state, STBY state, or transitions between these 2 states.

COLD Reset

When requesting a COLD reset, the device executes the power down sequence and transitions to INITIALIZE state. Then, the NVM is reloaded and rails power-up again in normal power-up-sequence, provided there are no faults and no OFF-request. A COLD reset returns all NVM-backed register bits to their boot-value. Register bits that are not NVM-backed maintain their values, except for STBY_I2C_CTRL, POWER_UP_FROM_OFF, POWER_UP_FROM_EN_PB_VSENSE, POWER_UP_FROM_FSD, CUST_PROG_DONE, CUST_NVM_VERIFY_DONE, and CUST_NVM_VERIFY_ERR. For details on which registers are NVM-backed, see Section 8.

The execution of a COLD-reset sets the bit COLD_RESET_ISSUED in POWER_UP_STATUS_REG register. The read-out of this bit allows the host to track if a COLD-reset was performed. The nINT-pin does not toggle based on this bit. Write W1C to clear the bit.

WARM Reset

When requesting a WARM reset, all enabled rails remain on, but the output voltage of rails that support dynamic voltage change is reset to the boot-voltage. Specifically, following configurations get reset to their boot-value: BUCK1_VSET, BUCK2_VSET, BUCK3_VSET, LDO1_VSET, and LDO2_VSET. All other bits, even in the same register, remain at their current state. For example, LDOx_LSW_CONFIG, BUCKx_BW_SEL, BUCKx_UV_THR_SEL and the MFP_1_CONFIG register bits do NOT get reset during a WARM-reset.

Note

Shut-down-faults and OFF-requests take priority over a RESET-request. If a RESET-requests occurs simultaneously with one of those, the device enters INITIALIZE state and requires a new ON-request to start up.

7.3.15 Register Access Control

Write access to the device registers is restricted via the REG_LOCK register to prevent inadvertant changes. Any register that contains an access type of R/W is protected by REG_LOCK. The REG_ACCESS_CMD of 5Ah must be written to the REG_LOCK register to unlock the protected registers for modification. Once changes are complete, write any value other than 5Ah to the REG_LOCK register to lock the protected registers.

Table 7-7. TPS65214 writable registers NOT protected by REG_LOCK

Register Address	Register Name
0x29	MFP_CTRL
0x34	USER_NVM_CMD_REG

7.3.16 I²C-Compatible Interface

The default I²C1 7-bit device address of the TPS65214 is set to 0x30 (0b0110000 in binary), but can be changed if needed.

The I²C-compatible synchronous serial interface provides access to the configurable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a controller or a target depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed somewhere on the line and remain HIGH even when the bus is idle. The TPS65214 supports standard mode (100kHz), fast mode (400kHz), and fast mode plus (1MHz) when VIO is 3.3V or 1.8V.

CAUTION

I2C transactions to some or all registers may not be valid during the following time periods:

- for t_{NVM_LOAD}, to all registers, when entering the INITIALIZE state
- for 60us, to NVM-backed registers, when starting a WARM reset
- for 80us, to non-NVM-backed registers, when starting a transition into the INITIALIZE state

See Section 8 for details on which registers are NVM-backed.

7.3.16.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when clock signal is LOW.

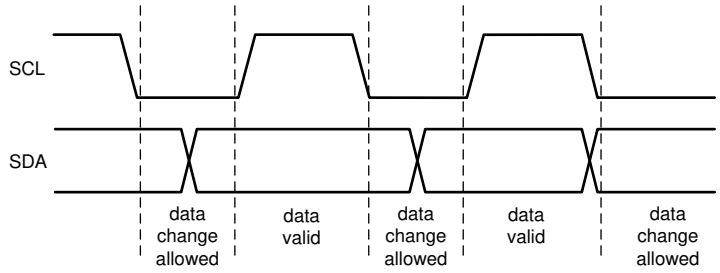


Figure 7-8. Data Validity Diagram

7.3.16.2 Start and Stop Conditions

The device is controlled through an I²C-compatible interface. START and STOP conditions classify the beginning and end of the I²C session. A START condition is defined as the SDA signal going from HIGH to LOW while the SCL signal is HIGH. A STOP condition is defined as the SDA signal going from LOW to HIGH while the SCL signal is HIGH. The I²C controller device always generates the START and STOP conditions.

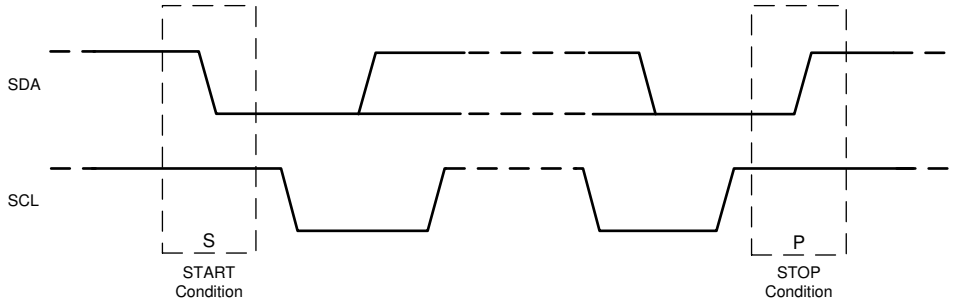


Figure 7-9. Start and Stop Sequences

The I²C bus is considered busy after a START condition and free after a STOP condition. The I²C controller device can generate repeated START conditions during data transmission. A START and a repeated START condition are equivalent function-wise. Figure 7-10 shows the SDA and SCL signal timing for the I²C-compatible bus. For timing values, see the *Specification* section.

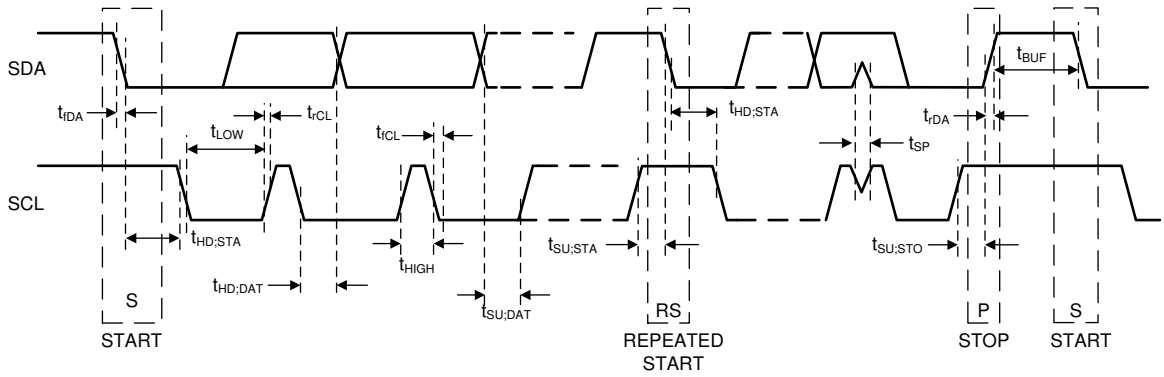


Figure 7-10. I²C-Compatible Timing

7.3.16.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated

by the controller device. The controller device releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the *acknowledge after every byte* rule. When the controller device is the receiver, it must indicate to the transmitter an end of data by not-acknowledging (*negative acknowledge*) the last byte clocked out of the target device. This *negative acknowledge* still includes the acknowledge clock pulse (generated by the controller device), but the SDA line is not pulled down.

After the START condition, the bus controller device sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register. Figure 7-11 shows an example bit format of device address 110000-Bin = 60Hex.

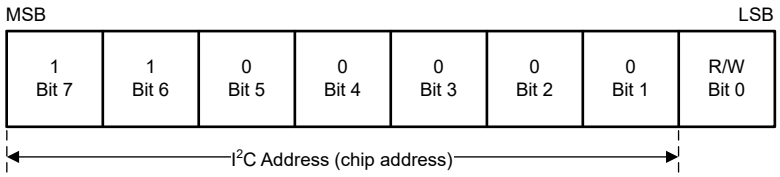


Figure 7-11. Example Device Address

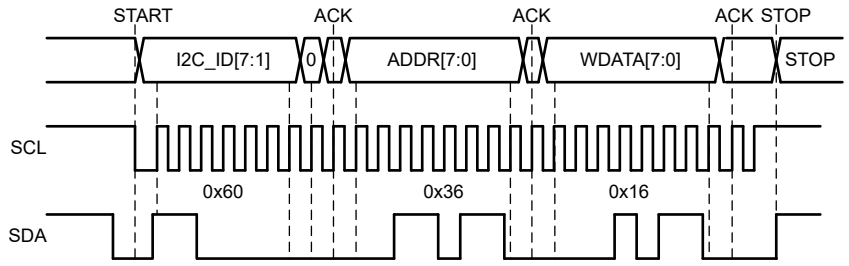
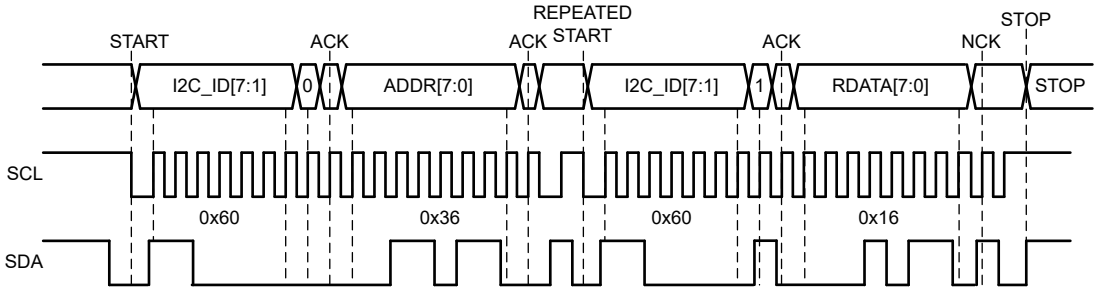


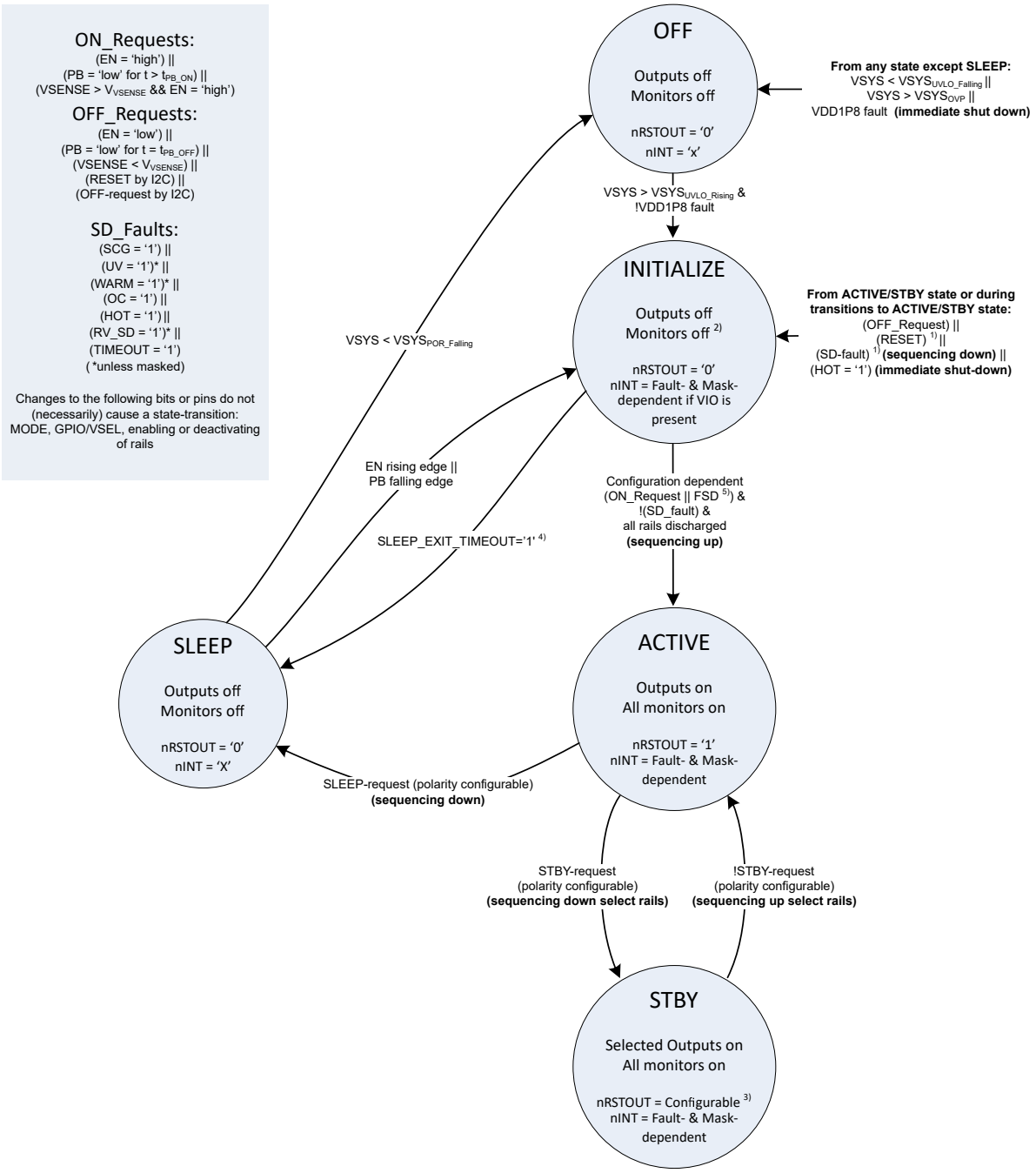
Figure 7-12. I²C Write Cycle



When READ function is to be accomplished, a WRITE function must precede the READ function as shown above.

Figure 7-13. I²C Read Cycle

7.4 Device Functional Modes



1) In case of a RESET or a SD-fault, the device transitions from INITIALIZE state to the ACTIVE state without a new Push-button-ON_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

2) If INITIALIZE state was entered due to a Thermal-Shut-Down, the temperature monitors remain active until the temperature on all sensors fell below T_{WARM} threshold. Thermal-Shut-Down causes immediate shut-down, no sequencing down.

3) State of nRSTOUT driver is determined by nRSTOUT_STBY_CONFIG bit.

4) SLEEP can only be entered from INITIALIZE via SLEEP_EXIT_TIMEOUT.

5) First Supply Detection (FSD) only applicable when VSYS is applied.

Figure 7-14. State Diagram

7.4.1 Modes of Operation

7.4.1.1 OFF State

In OFF state, the PMIC is insufficiently supplied. Neither internal logic nor external rails are available. If VSYS exceeds $VSYS_{UVLO\_Rising}$ voltage and the internal 1.8V-rail (VDD1P8) is in regulation, the device enters the INITIALIZE state.

7.4.1.2 INITIALIZE State

In INITIALIZE state, the device is completely shut down with the exception of a few circuits to monitor the EN/PB/VSENSE input. Whenever entering the INITIALIZE state, the PMIC reads the memory and loads the registers to their NVM-default values. The I^2C communication interface is turned off.

Entry to INITIALIZE state is gated if any one of the thermal sensors is above the T_{WARM_Rising} threshold and WARM-detection is not masked.

The NVM load time is given by t_{NVM_LOAD}. The power-up sequence can only execute after the NVM-load is complete.

If INITIALIZE state was entered from OFF state, bit POWER_UP_FROM_OFF in POWER_UP_STATUS_REG register is set and remains set until a write-1-clear is issued. Read-out of this bit allows to determine if INITIALZE state was entered from OFF state or due to a Shut-down-fault or OFF-request.

In INITIALIZE state, the nINT pin status is dependent if faults are and masking thereof. If no faults are present or nINT-reaction for those are masked, nINT-pin is pulled high, provided a VIO-voltage for the pull-up is available.

To transition from the INITIALIZE state to the ACTIVE state, one of the ON-requests must occur:

- The EN input is 'high' (if EN/PB/VSENSE is configured as 'EN' or 'VSENSE')
- The PB input is pulled low for at least $t_{PB\_ON\_SLOW}$ respectively $t_{PB\_ON\_FAST}$ (if EN/PB/VSENSE is configured as 'PB')

Note

The DISCHARGE_CONFIG register is purposefully omitted from RESET when entering INITIALIZE state from ACTIVE or STBY state. When entering INITIALIZE state from OFF state, the NVM content is loaded. If the discharge configuration changed after power-up, a different start-up behavior can occur, depending if the INITIALIZE state was entered from OFF state or from ACTIVE/STBY.

7.4.1.3 ACTIVE State

The ACTIVE state is the normal mode of operation when the system is up and running. All enabled bucks converters and LDOs are operational and can be controlled through the I2C interface. ACTIVE state can also be directly entered from STBY state by de-asserting the STBY pin high or by an I2C command. See STBY State for details. To transition to STBY, the STBY pin must be forced or an I2C command to STBY_I2C_CTRL in MFP_CTRL register must be issued.

To transition to INITIALIZE state, one of the following OFF_Requests must occur:

- The EN input is 'low' (if EN/PB/VSENSE is configured as 'EN' or 'VSENSE')
- The PB input is pulled low for at least t_{PB_OFF} (if EN/PB/VSENSE is configured as 'PB')
- An I2C OFF-request is issued

If a shut-down-fault (SD_Fault) occurs while in the ACTIVE state, TPS65214 sequences down the active outputs and transition to the INITIALIZE state. The device does transition to ACTIVE state without a new Push-button-ON_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

7.4.1.4 STBY State

STBY state is a low-power mode of operation intended to support system standby. The mode can be entered by the MODE/STBY pin, if configured as 'STBY' or by an I2C-command to STBY_I2C_CTRL in MFP_CTRL register. Typically, the majority of power rails are turned off with the exception of rails required by the SoC during

this state. Which rails power down in STBY state can be configured in STBY_1_CONFIG and STBY_2_CONFIG register.

The monitoring functions are all available: Undervoltage- (UV), Short-to-GND- (SCG) and Over-current- (OC) detection, thermal warning (WARM) and thermal-shutdown (TSD/HOT) remain active.

The device enters ACTIVE state if STBY is de-asserted or an I2C command is received (provided VIO-supply remained active). The sequence into and out of STBY state is the same as for power-down respectively for power-up. Rails that remain on in STBY are skipped, but the respective slots are still executed.

CAUTION
The device must enter the ACTIVE state before transitioning to the STBY state.

CAUTION
Only rails that were enabled in ACTIVE state can remain enabled in STBY. Deactivated rails cannot be turned on in STBY-state. Activity in STBY-state requires a AND-combination of LDOx_EN / BUCKx_EN and LDOx_STBY_EN/BUCKx_STBY_EN.

CAUTION
Do not change the registers related to an ongoing sequence by I2C-command!

Non-NVM-bits are not accessible for approximately 80us after starting a transition into INITIALIZE state.

7.4.1.5 SLEEP State

SLEEP state is an ultra-low-power mode of operation intended to minimize power consumption. After setting the STBY_SLEEP_CONFIG bit, SLEEP mode can be entered by the MODE/STBY pin, if configured as 'STBY' or by an I2C-command to STBY_I2C_CTRL in MFP_CTRL register. All power rails and most functional blocks, including all monitors, are turned off in this state. The only active I/Os is EN/PB/VSENSE, which must be configured as EN or PB to transition from SLEEP directly to INITIALIZE. If EN/PB/VSENSE is configured as VSENSE, the device can only exit the SLEEP state by going to the OFF state.

When EN/PB/VSENSE is configured as EN or PB via 'EN_PB_VSENSE_CONFIG', the device transitions from the SLEEP state to the INITIALIZE state upon detection of EN rising edge or PB falling edge and associated deglitch ($t_{DEGL\_ANALOG\_EN}$ followed by $t_{OFF\_TO\_INIT}$). The PMIC reads the NVM contents and loads the NVM-default values to the registers. The PMIC then waits for $t_{EN\_PB\_WAKEUP}$ and associated deglitch to elapse. After the timer elapses, the POWER_UP_FROM_EN_PB_VSENSE bit in POWER_UP_STATUS_REG register is set, the device transitions to the ACTIVE state, and begins the power-up sequence if no other faults are present. If the state of the EN/PB/VSENSE pin changes and surpasses the associated deglitch ($t_{DEGL\_EN\_RISE\_Fall}$ or $t_{DEGL\_PB\_RISE}$) before $t_{EN\_PB\_WAKEUP}$ elapses, a PB_EN_SLEEP_EXIT_TIMEOUT is detected, and the device transitions back to the SLEEP state.

The sequence into SLEEP state is the same as the power-down sequence. See Figure 7-15 for more details.

CAUTION
The device can only transition to the SLEEP state from the ACTIVE state (via 'STBY' or STBY_I2C_CTRL) or from the INITIALIZE state (via SLEEP_EXIT_TIMEOUT).

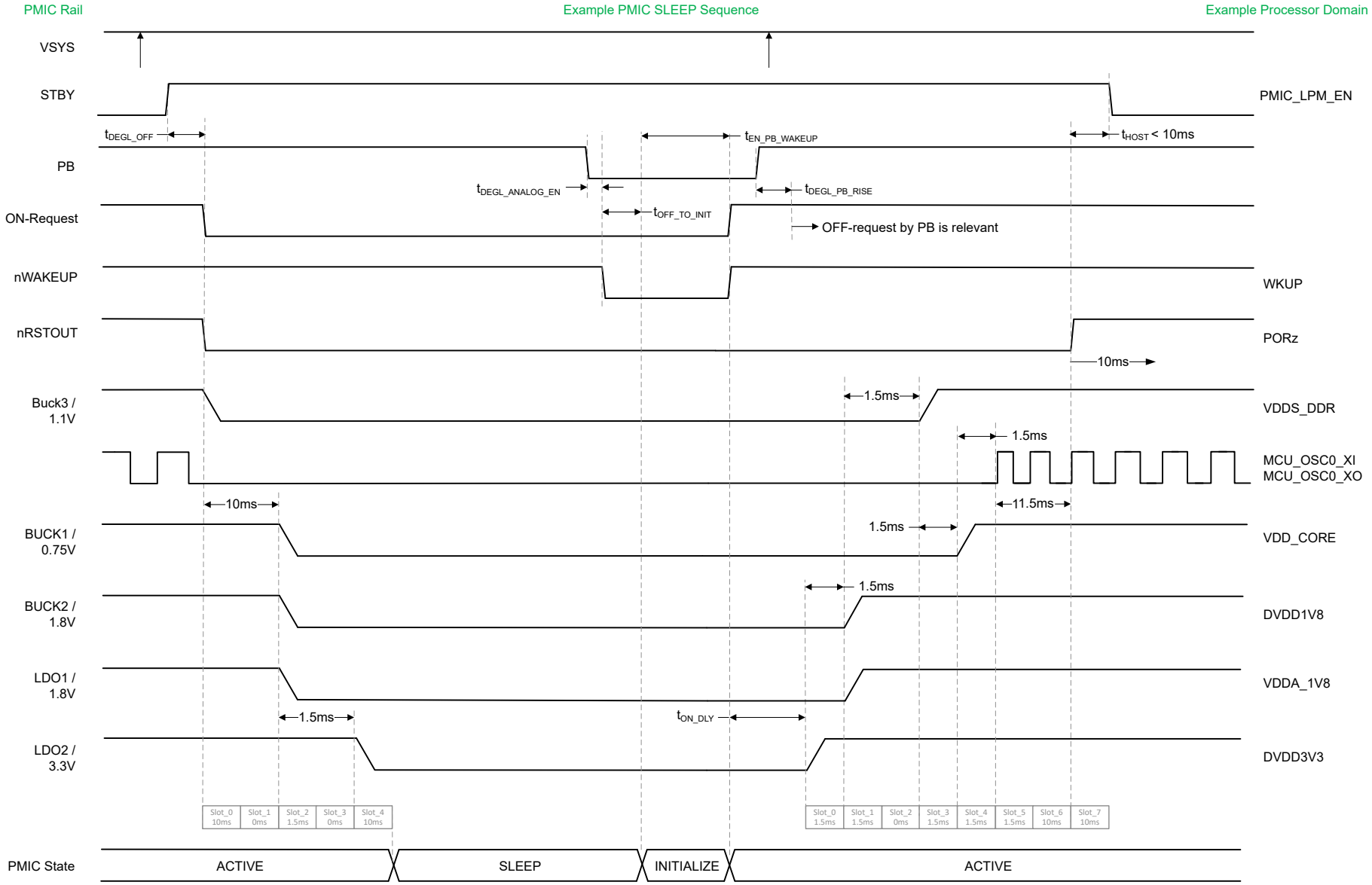
CAUTION
The 'EN_PB_VSENSE_CONFIG' setting can be changed during operation. For wakeup detection, the device refers to the 'EN_PB_VSENSE_CONFIG' setting when the SLEEP state is entered.

CAUTION

Do not change the registers related to an ongoing sequence by I2C-command!

Non-NVM-bits are not accessible for approximately 80us after starting a transition into INITIALIZE state.

Figure 7-15. SLEEP Sequencing (example)



7.4.1.6 Fault Handling

The TPS65214 offers various fault-detections. Per default, all of them lead to a sequenced shut-down. Some of them are maskable and the reaction to masked faults is configurable.

Supply Voltage Monitoring

The device provides the following fault-detections on the supply voltage (VSYS) and internal voltage supply (VDD1P8). None of these faults are maskable.

- Undervoltage on VSYS, resulting in transition to OFF state or gating start-up
- Overvoltage-protection on VSYS, resulting in transition to OFF state
- Under- or Overvoltage on internal 1.8V-supply (VDD1P8), resulting in transition to OFF state or gating start-up.

Regulator Output Monitoring

The TPS65214 provides the following fault-detections on the buck- and LDO-outputs:

- Undervoltage detection (UV)
- Over Current detection (OC), triggering on positive as well as (for buck-converters) negative current-limit
- Short-to-GND detection (SCG)
- Temperature warning (WARM) and Thermal Shut Down (TSD / HOT)
- Residual Voltage (RV) and Residual Voltage - Shutdown (RV_SD)
- Timeout (TO)

SCG, OC, HOT, and TO are not maskable. If any one of those occurs, the device powers down. Positive and negative current limit share the same mask-bit per regulator.

The reaction to UV, RV and WARM faults is configurable. If not masked, a fault triggers a sequenced shut-down. UV, RV and WARM can be masked individually per regulator in INT_MASK_BUCKS, INT_MASK_LDOS and INT_MASK_WARM registers. No state-transition occurs in case of a masked fault. Whether bits are set and if nINT is pulled low can be configured globally by MASK_EFFECT bits in MASK_CONFIG register. Positive and negative current limit share the same mask-bit per regulator.

- 00b = no state change, no nINT reaction, no bit set
- 01b = no state change, no nINT reaction, bit set
- 10b = no state change, nINT reaction, bit set (same as 11b)
- 11b = no state change, nINT reaction, bit set (same as 10b)

For any fault that corresponds to a shut-down condition, the fault-bit remains asserted until a W1C (write-one-clear) operation is performed via I2C (assuming the fault is not present any more). In case of a shut-down fault, no renewed on-request is required. The device automatically executes the power up sequence if the fault is no longer present as long as EN/VSENSE is still high and no PB-press is required for a restart.

For any fault that is not a shut-down condition (for example because the fault is masked), the bit is cleared when going to the INITIALIZE state.

Thermal Warning and Shutdown

There are two thermal thresholds: Thermal-warning (WARM) and Thermal Shutdown (TSD / HOT).

Thermal Warning, WARM-threshold

If the temperature exceeds T_{WARM_Rising} threshold, the SENSOR_x_WARM-bit is set and the PMIC sequences down (unless masked). When the temperature fell below $T_{WARM\_Falling}$ threshold, the device powers up again, without a new
Push-button-ON_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

If the temperature exceeds T_{WARM_Rising} threshold, but SENSOR_x_WARM_MASK bit is /bits are set, the PMIC remains in ACTIVE state. Fault-reporting occurs as configured by MASK_EFFECT bits. The processor makes the decision to either sequence the power down or throttles back on the running applications to reduce the power consumption and hopefully avoiding a Thermal Shutdown situation.

Thermal Shutdown, HOT-threshold

If the temperature exceeds T_{HOT_Rising} threshold, the SENSOR_x_HOT-bit is set and the PMIC powers off all rails immediately. This power down is simultaneously and not sequenced.

- If ALL sensors are masked for WARM-detection (all SENSOR_x_WARM_MASK bits are set), the PMIC does power back up once the temperature drops below the $T_{HOT\_Falling}$ threshold, provided a valid ON-request is present.
- If any one of the sensors is unmasked for WARM-detection, the PMIC does power back up once the temperature drops below the $T_{WARM\_Falling}$ threshold, without a new Push-button-ON_Request. In EN or VSENSE configuration, the ON-request must still be valid to transition to ACTIVE state.

Residual Voltage

Residual voltage checks are performed for each power rail before the rail is enabled, regardless if during the sequence or by I2C-command. The treatment of RV-faults depends on the situation when the fault occurs. A simplified state diagram to illustrate residual voltage checking is shown in Figure 7-16.

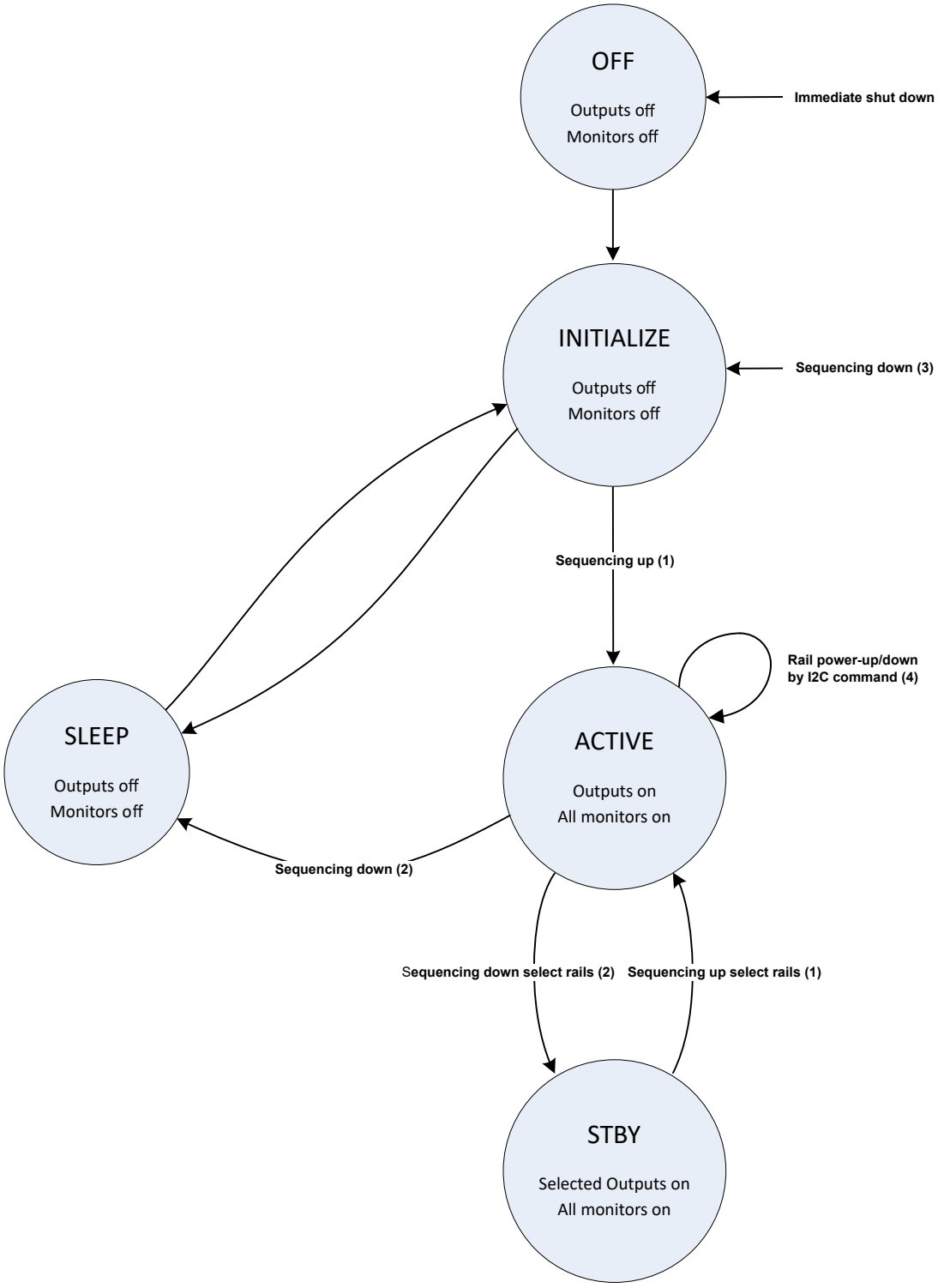


Figure 7-16. Residual Voltage Checking

1. In the case of residual voltage when sequencing up, the device sets the respective INT_TIMEOUT_RV_SD_IS_SET bit in INT_SOURCE register, LDOx_RV_SD respectively BUCKx_RV_SD bit and bit TIMEOUT in INT_TIMEOUT_RV_SD register, and initiates the power-down sequence at the end of the slot.

2. In case of residual voltage when sequencing down to the STBY or SLEEP state, the device gates the power-down of subsequent rails for up to eight times the power-down slot duration. If the residual voltage is still present, the device sets the following bits and initiates the power-down sequence.
   a. Bit INT_TIMEOUT_RV_SD_IS_SET in register INT_SOURCE
   b. Respective bit LDOx_RV_SD or BUCKx_RV_SD in register INT_TIMEOUT_RV_SD
   c. Bit TIMEOUT in register INT_TIMEOUT_RV_SD
3. In case of residual voltage when sequencing down to the INITIALIZE state, no status bits are set, and the power-down sequence continues after eight times the power-down slot-duration.
4. In case of residual voltage during the power-up or power-down of a rail via I2C command, the device sets the respective LDOx_RV or BUCKx_RV bit. If the MASK_INT_FOR_RV bit is not set (RV is unmasked), the device pulls the nINT pin low.

Note

In case active discharge on a rail is deactivated, the unsuccessful discharge of that rail within the slot duration does not gate the power-down of the subsequent rail. Additionally, the device does not set RV-bits nor RV_SD-bits during power-down.

The shutdown-fault-reaction in case of residual voltage detection when sequencing up or down is maskable by the BYPASS_RV_FOR_RAIL_ENABLE bit in the GENERAL_CONFIG register. The reaction of the nINT pin in case of residual voltage detection by I2C command is maskable by the MASK_INT_FOR_RV bit in the MASK_CONFIG register.

A timeout occurs if the residual voltage cannot be discharged after the power-up slot-duration, or after eight times the power-down slot-duration. The device sets the TIMEOUT bit in the INT_TIMEOUT_RV_SD register.

Retry Counter

For every detected Shut-Down fault, the retry counter (RETRY_COUNT in POWER_UP_STATUS_REG register) is incremented. The device attempts two retries to power-up. If both fail, a power-cycle on VSYS is required to reset the retry counter. Any successful power-up also resets the retry counter. Masked faults do not cause a shut-down and do not increment the retry counter.

The retry counter can be deactivated on first power up via the MASK_RETRY_COUNT_ON_FIRST_PU bit in the MFP_2_CONFIG register. When set, the device retries infinitely until the first power-up sequence is completed.

The retry counter can also be deactivated permanently by the MASK_RETRY_COUNT bit in the INT_MASK_UV register. When set, the device retries infinitely following any shut-down fault.

Fault Reaction Overview

Below table gives an overview of the fault-behavior in ACTIVE and STBY states if unmasked and whether a fault is maskable.

CAUTION

Masking of faults can pose a risk to the device or the system, including but not limited to starting into a pre-biased output.

TI does not recommend to mask both OC- and UV-detection on the same rail.

Table 7-8. Interrupt and Fault Handling

Block	Event	State Transition (when not masked)	Maskable	Interrupt Status Bit (set depending on MASK_EFFECT)	Interrupt Status Bit Clear
PB/EN/VSENSE	Push-Button rising edge	No state transition	No	PB_RISING_EDGE_DETECTED	W1C, INITIALIZE state, or VSYS UVLO
PB/EN/VSENSE	Push-Button falling edge	No state transition	No	PB_FALLING_EDGE_DETECTED	W1C, INITIALIZE state, or VSYS UVLO
PB/EN/VSENSE	Sleep exit timeout	Transition to SLEEP state	No	PB_EN_SLEEP_EXIT_TIMEOUT	W1C or VSYS UVLO
BUCK & LDO	Residual voltage - RV	No state transition	Yes	*_RV	W1C, INITIALIZE state, or VSYS UVLO
BUCK & LDO	Residual voltage - shutdown-Fault - RV_SD(1)	Sequenced shut-down to INITIALIZE state	Yes	*_RV_SD	W1C or VSYS UVLO
BUCK & LDO	Timeout - TO (1)	Sequenced shut-down to INITIALIZE state	Partial (MASK_UV)	TIMEOUT	W1C or VSYS UVLO
BUCK & LDO	Undervoltage - UV	Sequenced shut-down to INITIALIZE state	Yes	*_UV	W1C, INITIALIZE state (if masked), or VSYS UVLO
BUCK & LDO	Overcurrent - OC	Sequenced shut-down to INITIALIZE state	No	*_OC	W1C or VSYS UVLO
BUCK & LDO	Short-to-GND - SCG	Sequenced shut-down to INITIALIZE state	No	*_SCG	W1C or VSYS UVLO
BUCK & LDO	Temperature warning - WARM	Sequenced shut-down to INITIALIZE state	Yes	SENSOR_x_WARM	W1C, INITIALIZE state (if masked), or VSYS UVLO
BUCK & LDO	Temperature shut-down - HOT	Immediate shut-down to INITIALIZE state (not sequenced)	No	SENSOR_x_HOT	W1C or VSYS UVLO
VSYS	Undervoltage - UV	Immediate shut-down to OFF state (not sequenced)	No	None	N/A
VSYS	Overvoltage Protection - OVP	Immediate shut-down to OFF state (not sequenced)	No	None	N/A
VDD1P8	Undervoltage or Overvoltage - UV or OV	Immediate shut-down to OFF state (not sequenced)	No	None	N/A

(1) RV_SD and TIMEOUT faults can only occur during a sequence

8 User Registers

The registers up to register USER_GENERAL_NVM_STORAGE_REG (address 27h) are backed up by NVM. The reset value corresponds to the configuration of the orderable part number and is signified by an 'X'. Please refer to the Technical Reference Manual (TRM) of the respective orderable part-number.

The registers MANUFACTURING_VER (28h) through SPARE_3 (37h) are not NVM-backed and reset to the value shown in the register map.

Registers TI_DEV_ID (00h), NVM_ID (01h), MANUFACTURING_VER (28h) and FACTORY_CONFIG_2 (41h) cannot be changed by the user.

8.1 Device Registers

Table 8-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 8-1 should be considered as reserved locations and the register contents should not be modified.

Table 8-1. DEVICE Registers

Offset	Acronym	Register Name	Section
0h	TI_DEV_ID	Device ID	Go
1h	NVM_ID	NVM configuration ID	Go
2h	ENABLE_CTRL	Enable/Push-Button/Vsense Control	Go
3h	REG_LOCK	Lock/Unlock command register	Go
4h	LDO1_VOUT_STBY	LDO1 Configuration in STBY	Go
5h	LDO1_VOUT	LDO1 Configuration	Go
6h	LDO2_VOUT	LDO2 Configuration	Go
7h	LDO2_VOUT_STBY	LDO2 Configuration in STBY	Go
8h	BUCK3_VOUT	Buck3 Configuration	Go
9h	BUCK2_VOUT	Buck2 Configuration	Go
Ah	BUCK1_VOUT	Buck1 Configuration	Go
Ch	LDO1_SEQUENCE_SLOT	Power-up and -down slot for LDO1	Go
Dh	LDO2_SEQUENCE_SLOT	Power-up and -down slot for LDO2	Go
Fh	BUCK3_SEQUENCE_SLOT	Power-up and -down slot for Buck3	Go
10h	BUCK2_SEQUENCE_SLOT	Power-up and -down slot for Buck2	Go
11h	BUCK1_SEQUENCE_SLOT	Power-up and -down slot for Buck1	Go
12h	nRST_SEQUENCE_SLOT	Power-up and -down slot for nRSTOUT	Go
13h	GPIO_SEQUENCE_SLOT	Power-up and -down slot for GPIO	Go
15h	GPO_SEQUENCE_SLOT	Power-up and -down slot for GPO	Go
16h	POWER_UP_SLOT_DURATION_1	Slot-duration at power-up for slot0-3	Go
17h	POWER_UP_SLOT_DURATION_2	Slot-duration at power-up for slot4-7	Go
19h	BUCK3_VOUT_STBY	Buck3 Configuration in STBY	Go
1Ah	POWER_DOWN_SLOT_DURATION_1	Slot-duration at power-down for slot0-3	Go
1Bh	POWER_DOWN_SLOT_DURATION_2	Slot-duration at power-down for slot4-7	Go
1Ch	BUCK2_VOUT_STBY	Buck2 Configuration in STBY	Go
1Dh	BUCK1_VOUT_STBY	Buck1 Configuration in STBY	Go
1Eh	GENERAL_CONFIG	LDO-undervoltage and GPO-enable	Go
1Fh	MFP_1_CONFIG	Multi-Function pin configuration1	Go
20h	MFP_2_CONFIG	Multi-Function pin configuration2	Go
21h	STBY_1_CONFIG	STBY configuration LDOs and Bucks	Go
22h	STBY_2_CONFIG	STBY configuration GPIO and GPO	Go
23h	OC_DEGL_CONFIG	Overcurrent deglitch time per rail	Go
24h	INT_MASK_UV	Undervoltage fault-masking	Go
25h	MASK_CONFIG	WARM-masking and mask-effect	Go
26h	I2C_ADDRESS_REG	I2C-address	Go
27h	USER_GENERAL_NVM_STORAGE_REG	User-configurable register (NVM-backed)	Go
28h	MANUFACTURING_VER	Silicon-revision (read-only)	Go
29h	MFP_CTRL	I2C-control for RESET, STBY, OFF	Go
2Ah	DISCHARGE_CONFIG	Discharge configuration per rail	Go
2Bh	INT_SOURCE	Interrupt source	Go
2Dh	INT_LDO_1_2	OC, UV, SCG for LDO1 and LDO2	Go

Table 8-1. DEVICE Registers (continued)

Offset	Acronym	Register Name	Section
2Eh	INT_BUCK_3	OC, UV, SCG for Buck3	Go
2Fh	INT_BUCK_1_2	OC, UV, SCG for Buck1 and Buck2	Go
30h	INT_SYSTEM	WARM and HOT fault flags	Go
31h	INT_RV	RV (residual voltage) per rail	Go
32h	INT_TIMEOUT_RV_SD	RV (residual voltage) per rail causing shut-down	Go
33h	INT_PB	PushButton status and edge-detection	Go
34h	USER_NVM_CMD_REG	DIY - user programming commands	Go
35h	POWER_UP_STATUS_REG	Power-up status and STATE	Go
36h	SPARE_2	Spare register (not NVM-backed)	Go
37h	SPARE_3	Spare register (not NVM-backed)	Go

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

8.1.1 TI_DEV_ID Register (Offset = 0h) [Reset = XXh]

TI_DEV_ID is shown in Figure 8-1 and described in Table 8-3.

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Figure 8-1. TI_DEV_ID Register

7	6	5	4	3	2	1	0
TI_NVM_REV			TI_DEVICE_ID				
R/W-Xh			R/W-Xh				

Table 8-3. TI_DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	TI_NVM_REV	R/W	X	Device NVM revision Note: This register can be programmed only by the manufacturer! Refer to Technical Reference Manual / User's Guide for specific numbering and associated configuration. (Default from NVM memory) 0h = V0 1h = V1..
4-0	TI_DEVICE_ID	R/W	X	Device GPN Note: This register can be programmed only by the manufacturer! Refer to Technical Reference Manual / User's Guide for specific numbering and associated configuration. (Default from NVM memory)

8.1.2 NVM_ID Register (Offset = 1h) [Reset = XXh]

NVM_ID is shown in Figure 8-2 and described in Table 8-4.

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Figure 8-2. NVM_ID Register

7	6	5	4	3	2	1	0
TI_NVM_ID							
R/W-XXh							

Table 8-4. NVM_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TI_NVM_ID	R/W	X	NVM ID of the IC Note: This register can be programmed only by the manufacturer! Refer to Technical Reference Manual / User's Guide for specific numbering and associated configuration. (Default from NVM memory)

8.1.3 ENABLE_CTRL Register (Offset = 2h) [Reset = XXh]

ENABLE_CTRL is shown in Figure 8-3 and described in Table 8-5.

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Figure 8-3. ENABLE_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO1_EN	LDO2_EN	RESERVED	BUCK3_EN	BUCK2_EN	BUCK1_EN
R-0h	R-0h	R/W-Xh	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R/W-Xh

Table 8-5. ENABLE_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	LDO1_EN	R/W	X	Enable LDO1 regulator (Default from NVM memory) 0h = Not enabled 1h = Enabled
4	LDO2_EN	R/W	X	Enable LDO2 regulator (Default from NVM memory) 0h = Not enabled 1h = Enabled
3	RESERVED	R	0h	Reserved
2	BUCK3_EN	R/W	X	Enable BUCK3 regulator (Default from NVM memory) 0h = Not enabled 1h = Enabled
1	BUCK2_EN	R/W	X	Enable BUCK2 regulator (Default from NVM memory) 0h = Not enabled 1h = Enabled
0	BUCK1_EN	R/W	X	Enable BUCK1 regulator (Default from NVM memory) 0h = Not enabled 1h = Enabled

8.1.4 REG_LOCK Register (Offset = 3h) [Reset = 00h]

REG_LOCK is shown in Figure 8-4 and described in Table 8-6.

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Figure 8-4. REG_LOCK Register

7	6	5	4	3	2	1	0
REG_ACCESS_CMD							
R-0h							

Table 8-6. REG_LOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REG_ACCESS_CMD	R	0h	Write to this register to either lock or unlock the protected registers. A readback of this register results in '0h'. Any unacceptable write (that is, other than 5Ah) locks the protected registers. 5Ah = Unlocks the protected registers

8.1.5 LDO1_VOUT_STBY Register (Offset = 4h) [Reset = XXh]

LDO1_VOUT_STBY is shown in Figure 8-5 and described in Table 8-7.

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Figure 8-5. LDO1_VOUT_STBY Register

7	6	5	4	3	2	1	0
RESERVED	LDO1_DVS_STBY	LDO1_VSET_STBY					
R-0h	R/W-Xh	R/W-Xh					

Table 8-7. LDO1_VOUT_STBY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	LDO1_DVS_STBY	R/W	X	LDO1 DVS transition in STANDBY mode. 0h = No DVS transition in STBY 1h = DVS transition in STBY to output voltage configured by LDO1_VSET_STBY

Table 8-7. LDO1_VOUT_STBY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	LDO1_VSET_STBY	R/W	X	Voltage selection for LDO1 in STANDBY. The output voltage range is from 0.6V to 3.3V. (Default from NVM memory) 0h = 0.600V 1h = 0.600V 2h = 0.600V 3h = 0.650V 4h = 0.700V 5h = 0.750V 6h = 0.800V 7h = 0.850V 8h = 0.900V 9h = 0.950V Ah = 1.000V Bh = 1.050V Ch = 1.100V Dh = 1.150V Eh = 1.200V Fh = 1.250V 10h = 1.300V 11h = 1.350V 12h = 1.400V 13h = 1.450V 14h = 1.500V 15h = 1.550V 16h = 1.600V 17h = 1.650V 18h = 1.700V 19h = 1.750V 1Ah = 1.800V 1Bh = 1.850V 1Ch = 1.900V 1Dh = 1.950V 1Eh = 2.000V 1Fh = 2.050V 20h = 2.100V 21h = 2.150V 22h = 2.200V 23h = 2.250V 24h = 2.300V 25h = 2.350V 26h = 2.400V 27h = 2.450V 28h = 2.500V 29h = 2.550V 2Ah = 2.600V 2Bh = 2.650V 2Ch = 2.700V 2Dh = 2.750V 2Eh = 2.800V 2Fh = 2.850V 30h = 2.900V 31h = 2.950V 32h = 3.000V 33h = 3.050V 34h = 3.100V 35h = 3.150V 36h = 3.200V 37h = 3.250V 38h = 3.300V 39h = 3.300V 3Ah = 3.300V 3Bh = 3.300V 3Ch = 3.300V 3Dh = 3.300V 3Eh = 3.300V

Table 8-7. LDO1_VOUT_STBY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 3.300V

8.1.6 LDO1_VOUT Register (Offset = 5h) [Reset = XXh]

LDO1_VOUT is shown in Figure 8-6 and described in Table 8-8.

Return to the Summary Table.

Figure 8-6. LDO1_VOUT Register

7	6	5	4	3	2	1	0
RESERVED	LDO1_LSW_CONFIG	LDO1_VSET					
R-0h	R/W-Xh	R/W-Xh					

Table 8-8. LDO1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	LDO1_LSW_CONFIG	R/W	X	LDO1 LDO or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS NOT ENABLED! (Default from NVM memory) 0h = LDO Mode 1h = LSW Mode

Table 8-8. LDO1_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	LDO1_VSET	R/W	X	Voltage selection for LDO1. The output voltage range is from 0.6V to 3.3V. (Default from NVM memory) 0h = 0.600V 1h = 0.600V 2h = 0.600V 3h = 0.650V 4h = 0.700V 5h = 0.750V 6h = 0.800V 7h = 0.850V 8h = 0.900V 9h = 0.950V Ah = 1.000V Bh = 1.050V Ch = 1.100V Dh = 1.150V Eh = 1.200V Fh = 1.250V 10h = 1.300V 11h = 1.350V 12h = 1.400V 13h = 1.450V 14h = 1.500V 15h = 1.550V 16h = 1.600V 17h = 1.650V 18h = 1.700V 19h = 1.750V 1Ah = 1.800V 1Bh = 1.850V 1Ch = 1.900V 1Dh = 1.950V 1Eh = 2.000V 1Fh = 2.050V 20h = 2.100V 21h = 2.150V 22h = 2.200V 23h = 2.250V 24h = 2.300V 25h = 2.350V 26h = 2.400V 27h = 2.450V 28h = 2.500V 29h = 2.550V 2Ah = 2.600V 2Bh = 2.650V 2Ch = 2.700V 2Dh = 2.750V 2Eh = 2.800V 2Fh = 2.850V 30h = 2.900V 31h = 2.950V 32h = 3.000V 33h = 3.050V 34h = 3.100V 35h = 3.150V 36h = 3.200V 37h = 3.250V 38h = 3.300V 39h = 3.300V 3Ah = 3.300V 3Bh = 3.300V 3Ch = 3.300V 3Dh = 3.300V 3Eh = 3.300V

Table 8-8. LDO1_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 3.300V

8.1.7 LDO2_VOUT Register (Offset = 6h) [Reset = XXh]

LDO2_VOUT is shown in Figure 8-7 and described in Table 8-9.

Return to the Summary Table.

Figure 8-7. LDO2_VOUT Register

7	6	5	4	3	2	1	0
LDO2_LSW_CONFIG	RESERVED	LDO2_VSET					
R/W-Xh	R-0h	R/W-Xh					

Table 8-9. LDO2_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO2_LSW_CONFIG	R/W	X	LDO2 LDO or LSW Mode. NOTE: ONLY CHANGE WHILE RAIL IS NOT ENABLED! (Default from NVM memory) 0h = LDO Mode 1h = LSW Mode
6	RESERVED	R	0h	Reserved

Table 8-9. LDO2_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	LDO2_VSET	R/W	X	Voltage selection for LDO2. The output voltage range is from 0.6V to 3.3V in LDO mode. (Default from NVM memory) 0h = 0.600V 1h = 0.600V 2h = 0.600V 3h = 0.650V 4h = 0.700V 5h = 0.750V 6h = 0.800V 7h = 0.850V 8h = 0.900V 9h = 0.950V Ah = 1.000V Bh = 1.050V Ch = 1.100V Dh = 1.150V Eh = 1.200V Fh = 1.250V 10h = 1.300V 11h = 1.350V 12h = 1.400V 13h = 1.450V 14h = 1.500V 15h = 1.550V 16h = 1.600V 17h = 1.650V 18h = 1.700V 19h = 1.750V 1Ah = 1.800V 1Bh = 1.850V 1Ch = 1.900V 1Dh = 1.950V 1Eh = 2.000V 1Fh = 2.050V 20h = 2.100V 21h = 2.150V 22h = 2.200V 23h = 2.250V 24h = 2.300V 25h = 2.350V 26h = 2.400V 27h = 2.450V 28h = 2.500V 29h = 2.550V 2Ah = 2.600V 2Bh = 2.650V 2Ch = 2.700V 2Dh = 2.750V 2Eh = 2.800V 2Fh = 2.850V 30h = 2.900V 31h = 2.950V 32h = 3.000V 33h = 3.050V 34h = 3.100V 35h = 3.150V 36h = 3.200V 37h = 3.250V 38h = 3.300V 39h = 3.300V 3Ah = 3.300V 3Bh = 3.300V 3Ch = 3.300V 3Dh = 3.300V 3Eh = 3.300V

Table 8-9. LDO2_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 3.300V

8.1.8 LDO2_VOUT_STBY Register (Offset = 7h) [Reset = XXh]

LDO2_VOUT_STBY is shown in Figure 8-8 and described in Table 8-10.

Return to the Summary Table.

Figure 8-8. LDO2_VOUT_STBY Register

7	6	5	4	3	2	1	0
RESERVED	LDO2_DVS_STBY	LDO2_VSET_STBY					
R-0h	R/W-Xh	R/W-Xh					

Table 8-10. LDO2_VOUT_STBY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	LDO2_DVS_STBY	R/W	X	LDO2 DVS transition in STANDBY mode. 0h = No DVS transition in STBY 1h = DVS transition in STBY to output voltage configured by LDO2_VSET_STBY

Table 8-10. LDO2_VOUT_STBY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	LDO2_VSET_STBY	R/W	X	Voltage selection for LDO2 in STANDBY. The output voltage range is from 0.6V to 3.3V. (Default from NVM memory) 0h = 0.600V 1h = 0.600V 2h = 0.600V 3h = 0.650V 4h = 0.700V 5h = 0.750V 6h = 0.800V 7h = 0.850V 8h = 0.900V 9h = 0.950V Ah = 1.000V Bh = 1.050V Ch = 1.100V Dh = 1.150V Eh = 1.200V Fh = 1.250V 10h = 1.300V 11h = 1.350V 12h = 1.400V 13h = 1.450V 14h = 1.500V 15h = 1.550V 16h = 1.600V 17h = 1.650V 18h = 1.700V 19h = 1.750V 1Ah = 1.800V 1Bh = 1.850V 1Ch = 1.900V 1Dh = 1.950V 1Eh = 2.000V 1Fh = 2.050V 20h = 2.100V 21h = 2.150V 22h = 2.200V 23h = 2.250V 24h = 2.300V 25h = 2.350V 26h = 2.400V 27h = 2.450V 28h = 2.500V 29h = 2.550V 2Ah = 2.600V 2Bh = 2.650V 2Ch = 2.700V 2Dh = 2.750V 2Eh = 2.800V 2Fh = 2.850V 30h = 2.900V 31h = 2.950V 32h = 3.000V 33h = 3.050V 34h = 3.100V 35h = 3.150V 36h = 3.200V 37h = 3.250V 38h = 3.300V 39h = 3.300V 3Ah = 3.300V 3Bh = 3.300V 3Ch = 3.300V 3Dh = 3.300V 3Eh = 3.300V

Table 8-10. LDO2_VOUT_STBY Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 3.300V

8.1.9 BUCK3_VOUT Register (Offset = 8h) [Reset = XXh]

BUCK3_VOUT is shown in Figure 8-9 and described in Table 8-11.

Return to the Summary Table.

Figure 8-9. BUCK3_VOUT Register

7	6	5	4	3	2	1	0
BUCK3_BW_SEL	BUCK3_UV_THR_SEL	BUCK3_VSET					
R/W-Xh	R/W-Xh	R/W-Xh					

Table 8-11. BUCK3_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK3_BW_SEL	R/W	X	BUCK3 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS NOT ENABLED! (Default from NVM memory) 0h = low bandwidth 1h = high bandwidth
6	BUCK3_UV_THR_SEL	R/W	X	UV threshold selection for BUCK3. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection

Table 8-11. BUCK3_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	BUCK3_VSET	R/W	X	Voltage selection for BUCK3. The output voltage range is from 0.6V to 3.4V. (Default from NVM memory) 0h = 0.600V 1h = 0.625V 2h = 0.650V 3h = 0.675V 4h = 0.700V 5h = 0.725V 6h = 0.750V 7h = 0.775V 8h = 0.800V 9h = 0.825V Ah = 0.850V Bh = 0.875V Ch = 0.900V Dh = 0.925V Eh = 0.950V Fh = 0.975V 10h = 1.000V 11h = 1.025V 12h = 1.050V 13h = 1.075V 14h = 1.100V 15h = 1.125V 16h = 1.150V 17h = 1.175V 18h = 1.200V 19h = 1.225V 1Ah = 1.250V 1Bh = 1.275V 1Ch = 1.300V 1Dh = 1.325V 1Eh = 1.350V 1Fh = 1.375V 20h = 1.400V 21h = 1.500V 22h = 1.600V 23h = 1.700V 24h = 1.800V 25h = 1.900V 26h = 2.000V 27h = 2.100V 28h = 2.200V 29h = 2.300V 2Ah = 2.400V 2Bh = 2.500V 2Ch = 2.600V 2Dh = 2.700V 2Eh = 2.800V 2Fh = 2.900V 30h = 3.000V 31h = 3.100V 32h = 3.200V 33h = 3.300V 34h = 3.400V 35h = 3.400V 36h = 3.400V 37h = 3.400V 38h = 3.400V 39h = 3.400V 3Ah = 3.400V 3Bh = 3.400V 3Ch = 3.400V 3Dh = 3.400V 3Eh = 3.400V

Table 8-11. BUCK3_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 3.400V

8.1.10 BUCK2_VOUT Register (Offset = 9h) [Reset = XXh]

BUCK2_VOUT is shown in Figure 8-10 and described in Table 8-12.

Return to the Summary Table.

Figure 8-10. BUCK2_VOUT Register

7	6	5	4	3	2	1	0
BUCK2_BW_SEL	BUCK2_UV_THR_SEL	BUCK2_VSET					
R/W-Xh	R/W-Xh	R/W-Xh					

Table 8-12. BUCK2_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_BW_SEL	R/W	X	BUCK2 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS NOT ENABLED! (Default from NVM memory) 0h = low bandwidth 1h = high bandwidth
6	BUCK2_UV_THR_SEL	R/W	X	UV threshold selection for BUCK2. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection

Table 8-12. BUCK2_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	BUCK2_VSET	R/W	X	Voltage selection for BUCK2. The output voltage range is from 0.6V to 3.4V. (Default from NVM memory) 0h = 0.600V 1h = 0.625V 2h = 0.650V 3h = 0.675V 4h = 0.700V 5h = 0.725V 6h = 0.750V 7h = 0.775V 8h = 0.800V 9h = 0.825V Ah = 0.850V Bh = 0.875V Ch = 0.900V Dh = 0.925V Eh = 0.950V Fh = 0.975V 10h = 1.000V 11h = 1.025V 12h = 1.050V 13h = 1.075V 14h = 1.100V 15h = 1.125V 16h = 1.150V 17h = 1.175V 18h = 1.200V 19h = 1.225V 1Ah = 1.250V 1Bh = 1.275V 1Ch = 1.300V 1Dh = 1.325V 1Eh = 1.350V 1Fh = 1.375V 20h = 1.400V 21h = 1.500V 22h = 1.600V 23h = 1.700V 24h = 1.800V 25h = 1.900V 26h = 2.000V 27h = 2.100V 28h = 2.200V 29h = 2.300V 2Ah = 2.400V 2Bh = 2.500V 2Ch = 2.600V 2Dh = 2.700V 2Eh = 2.800V 2Fh = 2.900V 30h = 3.000V 31h = 3.100V 32h = 3.200V 33h = 3.300V 34h = 3.400V 35h = 3.400V 36h = 3.400V 37h = 3.400V 38h = 3.400V 39h = 3.400V 3Ah = 3.400V 3Bh = 3.400V 3Ch = 3.400V 3Dh = 3.400V 3Eh = 3.400V

Table 8-12. BUCK2_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 3.400V

8.1.11 BUCK1_VOUT Register (Offset = Ah) [Reset = XXh]

BUCK1_VOUT is shown in Figure 8-11 and described in Table 8-13.

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Figure 8-11. BUCK1_VOUT Register

7	6	5	4	3	2	1	0
BUCK1_BW_SEL	BUCK1_UV_THR_SEL	BUCK1_VSET					
R/W-Xh	R/W-Xh	R/W-Xh					

Table 8-13. BUCK1_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK1_BW_SEL	R/W	X	BUCK1 Bandwidth selection. NOTE: ONLY CHANGE WHILE RAIL IS NOT ENABLED! (Default from NVM memory) 0h = low bandwidth 1h = high bandwidth
6	BUCK1_UV_THR_SEL	R/W	X	UV threshold selection for BUCK1. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection

Table 8-13. BUCK1_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-0	BUCK1_VSET	R/W	X	Voltage selection for BUCK1. The output voltage range is from 0.6V to 3.4V. (Default from NVM memory) 0h = 0.600V 1h = 0.625V 2h = 0.650V 3h = 0.675V 4h = 0.700V 5h = 0.725V 6h = 0.750V 7h = 0.775V 8h = 0.800V 9h = 0.825V Ah = 0.850V Bh = 0.875V Ch = 0.900V Dh = 0.925V Eh = 0.950V Fh = 0.975V 10h = 1.000V 11h = 1.025V 12h = 1.050V 13h = 1.075V 14h = 1.100V 15h = 1.125V 16h = 1.150V 17h = 1.175V 18h = 1.200V 19h = 1.225V 1Ah = 1.250V 1Bh = 1.275V 1Ch = 1.300V 1Dh = 1.325V 1Eh = 1.350V 1Fh = 1.375V 20h = 1.400V 21h = 1.500V 22h = 1.600V 23h = 1.700V 24h = 1.800V 25h = 1.900V 26h = 2.000V 27h = 2.100V 28h = 2.200V 29h = 2.300V 2Ah = 2.400V 2Bh = 2.500V 2Ch = 2.600V 2Dh = 2.700V 2Eh = 2.800V 2Fh = 2.900V 30h = 3.000V 31h = 3.100V 32h = 3.200V 33h = 3.300V 34h = 3.400V 35h = 3.400V 36h = 3.400V 37h = 3.400V 38h = 3.400V 39h = 3.400V 3Ah = 3.400V 3Bh = 3.400V 3Ch = 3.400V 3Dh = 3.400V 3Eh = 3.400V

Table 8-13. BUCK1_VOUT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				3Fh = 3.400V

8.1.12 LDO1_SEQUENCE_SLOT Register (Offset = Ch) [Reset = XXh]

LDO1_SEQUENCE_SLOT is shown in Figure 8-12 and described in Table 8-14.

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Figure 8-12. LDO1_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
RESERVED	LDO1_SEQUENCE_ON_SLOT			RESERVED	LDO1_SEQUENCE_OFF_SLOT		
R-0h	R/W-Xh			R-0h	R/W-Xh		

Table 8-14. LDO1_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	LDO1_SEQUENCE_ON_SLOT	R/W	X	LDO1 slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	LDO1_SEQUENCE_OFF_SLOT	R/W	X	LDO1 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.13 LDO2_SEQUENCE_SLOT Register (Offset = Dh) [Reset = XXh]

LDO2_SEQUENCE_SLOT is shown in Figure 8-13 and described in Table 8-15.

Return to the Summary Table.

Figure 8-13. LDO2_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
RESERVED	LDO2_SEQUENCE_ON_SLOT			RESERVED	LDO2_SEQUENCE_OFF_SLOT		
R-0h	R/W-Xh			R-0h	R/W-Xh		

Table 8-15. LDO2_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	LDO2_SEQUENCE_ON_SLOT	R/W	X	LDO2 slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	LDO2_SEQUENCE_OFF_SLOT	R/W	X	LDO2 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.14 BUCK3_SEQUENCE_SLOT Register (Offset = Fh) [Reset = XXh]

BUCK3_SEQUENCE_SLOT is shown in Figure 8-14 and described in Table 8-16.

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Figure 8-14. BUCK3_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
RESERVED	BUCK3_SEQUENCE_ON_SLOT			RESERVED	BUCK3_SEQUENCE_OFF_SLOT		
R-0h	R/W-Xh			R-0h	R/W-Xh		

Table 8-16. BUCK3_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	BUCK3_SEQUENCE_ON_SLOT	R/W	X	BUCK3 slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	BUCK3_SEQUENCE_OFF_SLOT	R/W	X	BUCK3 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.15 BUCK2_SEQUENCE_SLOT Register (Offset = 10h) [Reset = XXh]

BUCK2_SEQUENCE_SLOT is shown in Figure 8-15 and described in Table 8-17.

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Figure 8-15. BUCK2_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
RESERVED	BUCK2_SEQUENCE_ON_SLOT			RESERVED	BUCK2_SEQUENCE_OFF_SLOT		
R-0h	R/W-Xh			R-0h	R/W-Xh		

Table 8-17. BUCK2_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	BUCK2_SEQUENCE_ON_SLOT	R/W	X	BUCK2 Slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	BUCK2_SEQUENCE_OFF_SLOT	R/W	X	BUCK2 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.16 BUCK1_SEQUENCE_SLOT Register (Offset = 11h) [Reset = XXh]

BUCK1_SEQUENCE_SLOT is shown in Figure 8-16 and described in Table 8-18.

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Figure 8-16. BUCK1_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
RESERVED	BUCK1_SEQUENCE_ON_SLOT			RESERVED	BUCK1_SEQUENCE_OFF_SLOT		
R-0h	R/W-Xh			R-0h	R/W-Xh		

Table 8-18. BUCK1_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	BUCK1_SEQUENCE_ON_SLOT	R/W	X	BUCK1 Slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	BUCK1_SEQUENCE_OFF_SLOT	R/W	X	BUCK1 slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.17 nRST_SEQUENCE_SLOT Register (Offset = 12h) [Reset = XXh]

nRST_SEQUENCE_SLOT is shown in Figure 8-17 and described in Table 8-19.

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Figure 8-17. nRST_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
RESERVED	nRST_SEQUENCE_ON_SLOT			RESERVED	nRST_SEQUENCE_OFF_SLOT		
R-0h	R/W-Xh			R-0h	R/W-Xh		

Table 8-19. nRST_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	nRST_SEQUENCE_ON_SLOT	R/W	X	nRST slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	nRST_SEQUENCE_OFF_SLOT	R/W	X	nRST slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.18 GPIO_SEQUENCE_SLOT Register (Offset = 13h) [Reset = XXh]

GPIO_SEQUENCE_SLOT is shown in Figure 8-18 and described in Table 8-20.

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Figure 8-18. GPIO_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
GPIO_SEQUENCE_POLARITY	GPIO_SEQUENCE_ON_SLOT			RESERVED	GPIO_SEQUENCE_OFF_SLOT		
R/W-Xh	R/W-Xh			R-0h	R/W-Xh		

Table 8-20. GPIO_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_SEQUENCE_POLARITY	R/W	X	GPIO as a sequence input on/off polarity 0h = LOW - off / HIGH - on 1h = HIGH - off / LOW - on
6-4	GPIO_SEQUENCE_ON_SLOT	R/W	X	GPIO slot number for power-up. When configured as an output, the pin is sequenced on according to the slot. When configured as an input, the sequencer waits for the pin to reach the on state. (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	GPIO_SEQUENCE_OFF_SLOT	R/W	X	GPIO slot number for power-down. When configured as an output, the pin is sequenced off according to the slot. When configured as an input, the sequencer waits for the pin to reach the off state. (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.19 GPO_SEQUENCE_SLOT Register (Offset = 15h) [Reset = XXh]

GPO_SEQUENCE_SLOT is shown in Figure 8-19 and described in Table 8-21.

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Figure 8-19. GPO_SEQUENCE_SLOT Register

7	6	5	4	3	2	1	0
RESERVED	GPO_SEQUENCE_ON_SLOT			RESERVED	GPO_SEQUENCE_OFF_SLOT		
R-0h	R/W-Xh			R-0h	R/W-Xh		

Table 8-21. GPO_SEQUENCE_SLOT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6-4	GPO_SEQUENCE_ON_SLOT	R/W	X	GPO slot number for power-up (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7
3	RESERVED	R	0h	Reserved
2-0	GPO_SEQUENCE_OFF_SLOT	R/W	X	GPO slot number for power-down (Default from NVM memory) 0h = slot 0 1h = slot 1 2h = slot 2 3h = slot 3 4h = slot 4 5h = slot 5 6h = slot 6 7h = slot 7

8.1.20 POWER_UP_SLOT_DURATION_1 Register (Offset = 16h) [Reset = XXh]

POWER_UP_SLOT_DURATION_1 is shown in Figure 8-20 and described in Table 8-22.

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Figure 8-20. POWER_UP_SLOT_DURATION_1 Register

7	6	5	4	3	2	1	0
POWER_UP_SLOT_0_DURATION		POWER_UP_SLOT_1_DURATION		POWER_UP_SLOT_2_DURATION		POWER_UP_SLOT_3_DURATION	
R/W-Xh		R/W-Xh		R/W-Xh		R/W-Xh	

Table 8-22. POWER_UP_SLOT_DURATION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	POWER_UP_SLOT_0_DURATION	R/W	X	Duration of slot 0 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_UP_SLOT_1_DURATION	R/W	X	Duration of slot 1 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
3-2	POWER_UP_SLOT_2_DURATION	R/W	X	Duration of slot 2 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_UP_SLOT_3_DURATION	R/W	X	Duration of slot 3 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms

8.1.21 POWER_UP_SLOT_DURATION_2 Register (Offset = 17h) [Reset = XXh]

POWER_UP_SLOT_DURATION_2 is shown in Figure 8-21 and described in Table 8-23.

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Figure 8-21. POWER_UP_SLOT_DURATION_2 Register

7	6	5	4	3	2	1	0
POWER_UP_SLOT_4_DURATION		POWER_UP_SLOT_5_DURATION		POWER_UP_SLOT_6_DURATION		POWER_UP_SLOT_7_DURATION	
R/W-Xh		R/W-Xh		R/W-Xh		R/W-Xh	

Table 8-23. POWER_UP_SLOT_DURATION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	POWER_UP_SLOT_4_DURATION	R/W	X	Duration of slot 4 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_UP_SLOT_5_DURATION	R/W	X	Duration of slot 5 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
3-2	POWER_UP_SLOT_6_DURATION	R/W	X	Duration of slot 6 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_UP_SLOT_7_DURATION	R/W	X	Duration of slot 7 during the power-up and standby-to-active sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms

8.1.22 BUCK3_VOUT_STBY Register (Offset = 19h) [Reset = XXh]

BUCK3_VOUT_STBY is shown in Figure 8-22 and described in Table 8-24.

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Figure 8-22. BUCK3_VOUT_STBY Register

7	6	5	4	3	2	1	0
RESERVED	BUCK3_DVS_STBY	RESERVED	BUCK3_VSET_STBY				
R-0h	R/W-Xh	R-0h	R/W-Xh				

Table 8-24. BUCK3_VOUT_STBY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	BUCK3_DVS_STBY	R/W	X	BUCK3 DVS transition in STANDBY mode. 0h = No DVS transition in STBY 1h = DVS transition in STBY to output voltage configured by BUCK3_VSET_STBY
5	RESERVED	R	0h	Reserved
4-0	BUCK3_VSET_STBY	R/W	X	Voltage selection in STANDBY for BUCK3. The output voltage range is from 0.6V to 1.375V. (Default from NVM memory) 0h = 0.600V 1h = 0.625V 2h = 0.650V 3h = 0.675V 4h = 0.700V 5h = 0.725V 6h = 0.750V 7h = 0.775V 8h = 0.800V 9h = 0.825V Ah = 0.850V Bh = 0.875V Ch = 0.900V Dh = 0.925V Eh = 0.950V Fh = 0.975V 10h = 1.000V 11h = 1.025V 12h = 1.050V 13h = 1.075V 14h = 1.100V 15h = 1.125V 16h = 1.150V 17h = 1.175V 18h = 1.200V 19h = 1.225V 1Ah = 1.250V 1Bh = 1.275V 1Ch = 1.300V 1Dh = 1.325V 1Eh = 1.350V 1Fh = 1.375V

8.1.23 POWER_DOWN_SLOT_DURATION_1 Register (Offset = 1Ah) [Reset = XXh]

POWER_DOWN_SLOT_DURATION_1 is shown in Figure 8-23 and described in Table 8-25.

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Figure 8-23. POWER_DOWN_SLOT_DURATION_1 Register

7	6	5	4	3	2	1	0
POWER_DOWN_SLOT_0_DURATION		POWER_DOWN_SLOT_1_DURATION		POWER_DOWN_SLOT_2_DURATION		POWER_DOWN_SLOT_3_DURATION	
R/W-Xh		R/W-Xh		R/W-Xh		R/W-Xh	

Table 8-25. POWER_DOWN_SLOT_DURATION_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	POWER_DOWN_SLOT_0_DURATION	R/W	X	Duration of slot 0 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_DOWN_SLOT_1_DURATION	R/W	X	Duration of slot 1 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
3-2	POWER_DOWN_SLOT_2_DURATION	R/W	X	Duration of slot 2 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_DOWN_SLOT_3_DURATION	R/W	X	Duration of slot 3 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms

8.1.24 POWER_DOWN_SLOT_DURATION_2 Register (Offset = 1Bh) [Reset = XXh]

POWER_DOWN_SLOT_DURATION_2 is shown in Figure 8-24 and described in Table 8-26.

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Figure 8-24. POWER_DOWN_SLOT_DURATION_2 Register

7	6	5	4	3	2	1	0
POWER_DOWN_SLOT_4_DURATION		POWER_DOWN_SLOT_5_DURATION		POWER_DOWN_SLOT_6_DURATION		POWER_DOWN_SLOT_7_DURATION	
R/W-Xh		R/W-Xh		R/W-Xh		R/W-Xh	

Table 8-26. POWER_DOWN_SLOT_DURATION_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	POWER_DOWN_SLOT_4_DURATION	R/W	X	Duration of slot 4 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
5-4	POWER_DOWN_SLOT_5_DURATION	R/W	X	Duration of slot 5 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
3-2	POWER_DOWN_SLOT_6_DURATION	R/W	X	Duration of slot 6 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms
1-0	POWER_DOWN_SLOT_7_DURATION	R/W	X	Duration of slot 7 during the power-down and active-to-standby sequences. (Default from NVM memory) 0h = 0ms 1h = 1.5ms 2h = 3ms 3h = 10ms

8.1.25 BUCK2_VOUT_STBY Register (Offset = 1Ch) [Reset = XXh]

BUCK2_VOUT_STBY is shown in Figure 8-25 and described in Table 8-27.

Return to the Summary Table.

Figure 8-25. BUCK2_VOUT_STBY Register

7	6	5	4	3	2	1	0
RESERVED	BUCK2_DVS_STBY	RESERVED	BUCK2_VSET_STBY				
R-0h	R/W-Xh	R-0h	R/W-Xh				

Table 8-27. BUCK2_VOUT_STBY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	BUCK2_DVS_STBY	R/W	X	BUCK2 DVS transition in STANDBY mode. 0h = No DVS transition in STBY 1h = DVS transition in STBY to output voltage configured by BUCK2_VSET_STBY
5	RESERVED	R	0h	Reserved
4-0	BUCK2_VSET_STBY	R/W	X	Voltage selection in STANDBY for BUCK2. The output voltage range is from 0.6V to 1.375V. (Default from NVM memory) 0h = 0.600V 1h = 0.625V 2h = 0.650V 3h = 0.675V 4h = 0.700V 5h = 0.725V 6h = 0.750V 7h = 0.775V 8h = 0.800V 9h = 0.825V Ah = 0.850V Bh = 0.875V Ch = 0.900V Dh = 0.925V Eh = 0.950V Fh = 0.975V 10h = 1.000V 11h = 1.025V 12h = 1.050V 13h = 1.075V 14h = 1.100V 15h = 1.125V 16h = 1.150V 17h = 1.175V 18h = 1.200V 19h = 1.225V 1Ah = 1.250V 1Bh = 1.275V 1Ch = 1.300V 1Dh = 1.325V 1Eh = 1.350V 1Fh = 1.375V

8.1.26 BUCK1_VOUT_STBY Register (Offset = 1Dh) [Reset = XXh]

BUCK1_VOUT_STBY is shown in Figure 8-26 and described in Table 8-28.

Return to the Summary Table.

Figure 8-26. BUCK1_VOUT_STBY Register

7	6	5	4	3	2	1	0
RESERVED	BUCK1_DVS_STBY	RESERVED	BUCK1_VSET_STBY				
R-0h	R/W-Xh	R-0h	R/W-Xh				

Table 8-28. BUCK1_VOUT_STBY Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	BUCK1_DVS_STBY	R/W	X	BUCK1 DVS transition in STANDBY mode. 0h = No DVS transition in STBY 1h = DVS transition in STBY to output voltage configured by BUCK1_VSET_STBY
5	RESERVED	R	0h	Reserved
4-0	BUCK1_VSET_STBY	R/W	X	Voltage selection in STANDBY for BUCK1. The output voltage range is from 0.6V to 1.375V. (Default from NVM memory) 0h = 0.600V 1h = 0.625V 2h = 0.650V 3h = 0.675V 4h = 0.700V 5h = 0.725V 6h = 0.750V 7h = 0.775V 8h = 0.800V 9h = 0.825V Ah = 0.850V Bh = 0.875V Ch = 0.900V Dh = 0.925V Eh = 0.950V Fh = 0.975V 10h = 1.000V 11h = 1.025V 12h = 1.050V 13h = 1.075V 14h = 1.100V 15h = 1.125V 16h = 1.150V 17h = 1.175V 18h = 1.200V 19h = 1.225V 1Ah = 1.250V 1Bh = 1.275V 1Ch = 1.300V 1Dh = 1.325V 1Eh = 1.350V 1Fh = 1.375V

8.1.27 GENERAL_CONFIG Register (Offset = 1Eh) [Reset = XXh]

GENERAL_CONFIG is shown in Figure 8-27 and described in Table 8-29.

Return to the Summary Table.

Figure 8-27. GENERAL_CONFIG Register

7	6	5	4	3	2	1	0
BYPASS_RV_FOR_RAIL_ENABLE	RESERVED	LDO1_UV_THR	LDO2_UV_THR	RESERVED	GPIO_EN	GPIO_CONFIG	GPO_EN
R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R/W-Xh

Table 8-29. GENERAL_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BYPASS_RV_FOR_RAIL_ENABLE	R/W	X	Bypass the check for RV(Pre-biased) condition prior to enabling a regulator. (Default from NVM memory) 0h = Discharged checks enforced 1h = Discharged checks bypassed
6	RESERVED	R	0h	Reserved
5	LDO1_UV_THR	R/W	X	UV threshold selection bit for LDO1. Only applicable if configured as LDO. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection
4	LDO2_UV_THR	R/W	X	UV threshold selection bit for LDO2. Only applicable if configured as LDO. (Default from NVM memory) 0h = -5% UV detection 1h = -10% UV detection
3	RESERVED	R	0h	Reserved
2	GPIO_EN	R/W	X	Both an enable and state control of GPIO. This bit enables the GPIO function and also controls the state of the GPIO pin. (Default from NVM memory) 0h = The GPIO function is not enabled. The output state is 'low'. 1h = The GPIO function is enabled. The output state is 'high'.
1	GPIO_CONFIG	R/W	X	GPIO Pin configuration. (Default from NVM memory) 0h = Configured as an input 1h = Configured as an output
0	GPO_EN	R/W	X	Both an enable and state control of GPO. This bit enables the GPO function and also controls the state of the GPO pin. (Default from NVM memory) 0h = GPO not enabled. The output state is low. 1h = GPO enabled. The output state is Hi-Z.

8.1.28 MFP_1_CONFIG Register (Offset = 1Fh) [Reset = XXh]

MFP_1_CONFIG is shown in Figure 8-28 and described in Table 8-30.

Return to the Summary Table.

Figure 8-28. MFP_1_CONFIG Register

7	6	5	4	3	2	1	0
MODE_I2C_CTRL	RESERVED	RESERVED	MODE_STBY_POLARITY	GPIO_VSEL_CONFIG	VSEL_RAIL	RESERVED	RESERVED
R/W-Xh	R-0h	R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R-0h	R-0h

Table 8-30. MFP_1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MODE_I2C_CTRL	R/W	X	MODE control using I2C. Consolidated with MODE control via MODE/STBY pin. Refer to table in the data sheet. (Default from NVM memory) 0h = Auto PFM 1h = Forced PWM
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	MODE_STBY_POLARITY	R/W	X	MODE_STBY Pin Polarity configuration. Note: Ok to change during operation, but consider immediate reaction: MODE-change or STATE-change! (Default from NVM memory) 0h = [if configured as MODE] LOW - auto-PFM / HIGH - forced PWM. [if configured as a STBY] LOW - STBY state / HIGH - ACTIVE state. 1h = [if configured as MODE] HIGH - auto-PFM / LOW - forced PWM. [if configured as a STBY] HIGH - STBY state / LOW - ACTIVE state.
3	GPIO_VSEL_CONFIG	R/W	X	GPIO_VSEL Pin configuration. NOTE: ONLY CHANGE IN INITIALIZE STATE! (Default from NVM memory) 0h = Configured as GPIO 1h = Configured as VSEL
2	VSEL_RAIL	R/W	X	BUCK controlled by GPIO/VSEL when configured as VSEL. NOTE: ONLY CHANGE IN INITIALIZE STATE! (Default from NVM memory) 0h = BUCK1 1h = BUCK3
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

8.1.29 MFP_2_CONFIG Register (Offset = 20h) [Reset = XXh]

MFP_2_CONFIG is shown in Figure 8-29 and described in Table 8-31.

Return to the Summary Table.

Figure 8-29. MFP_2_CONFIG Register

7	6	5	4	3	2	1	0
PU_ON_FSD	MASK_RETRY_COUNT_ON_FIRST_PU	EN_PB_VSENSE_CONFIG		EN_PB_VSENSE_DEGL	GPO_nWAKEUP_CONFIG	MODE_STBY_CONFIG	
R/W-Xh	R/W-Xh	R/W-Xh		R/W-Xh	R/W-Xh	R/W-Xh	

Table 8-31. MFP_2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PU_ON_FSD	R/W	X	Power up upon First Supply Detected (FSD). So when VSYS is applied, device does power up to ACTIVE state even if EN/PB/VSENSE pin is at OFF_REQ status. (Default from NVM memory) 0h = First Supply Detection (FSD) Not enabled. 1h = First Supply Detection (FSD) Enabled.
6	MASK_RETRY_COUNT_ON_FIRST_PU	R/W	X	Mask RETRY_COUNT during first power up. RETRY_COUNT is unmasked once the device enters the ACTIVE state. 0h = RETRY_COUNT is not masked on first power-up. 1h = RETRY_COUNT is masked on first power-up.
5-4	EN_PB_VSENSE_CONFIG	R/W	X	Enable / Push-Button / VSENSE Configuration. Do not change via I2C after NVM load (except as a precursor before programming NVM) (Default from NVM memory) 0h = Push Button Configuration 1h = Device Enable Configuration 2h = VSENSE Configuration 3h = Device Enable Configuration
3	EN_PB_VSENSE_DEGL	R/W	X	Enable / Push-Button / VSENSE Deglitch NOTE: ONLY CHANGE IN INITIALIZE STATE! Consider immediate reaction when changing from EN/VSENSE to PB or vice versa: power-up! (Default from NVM memory) 0h = short (typ: 120us for EN/VSENSE and 200ms for PB) 1h = long (typ: 50ms for EN/VSENSE and 600ms for PB)
2	GPO_nWAKEUP_CONFIG	R/W	X	GPO/nWAKEUP Configuration (Default from NVM memory) 0h = GPO 1h = nWAKEUP
1-0	MODE_STBY_CONFIG	R/W	X	MODE_STBY Configuration (Default from NVM memory) 0h = MODE 1h = STBY 2h = MODE and STBY 3h = MODE

8.1.30 STBY_1_CONFIG Register (Offset = 21h) [Reset = XXh]

STBY_1_CONFIG is shown in Figure 8-30 and described in Table 8-32.

Return to the Summary Table.

Figure 8-30. STBY_1_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO1_STBY_EN	LDO2_STBY_EN	RESERVED	BUCK3_STBY_EN	BUCK2_STBY_EN	BUCK1_STBY_EN
R-0h	R-0h	R/W-Xh	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R/W-Xh

Table 8-32. STBY_1_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	LDO1_STBY_EN	R/W	X	Enable LDO1 in STANDBY state. (Default from NVM memory) 0h = Not enabled in STBY Mode 1h = Enabled in STBY Mode
4	LDO2_STBY_EN	R/W	X	Enable LDO2 in STANDBY state. (Default from NVM memory) 0h = Not enabled in STBY Mode 1h = Enabled in STBY Mode
3	RESERVED	R	0h	Reserved
2	BUCK3_STBY_EN	R/W	X	Enable BUCK3 in STANDBY state. (Default from NVM memory) 0h = Not enabled in STBY Mode 1h = Enabled in STBY Mode
1	BUCK2_STBY_EN	R/W	X	Enable BUCK2 in STANDBY state. (Default from NVM memory) 0h = Not enabled in STBY Mode 1h = Enabled in STBY Mode
0	BUCK1_STBY_EN	R/W	X	Enable BUCK1 in STANDBY state. (Default from NVM memory) 0h = Not enabled in STBY Mode 1h = Enabled in STBY Mode

8.1.31 STBY_2_CONFIG Register (Offset = 22h) [Reset = XXh]

STBY_2_CONFIG is shown in Figure 8-31 and described in Table 8-33.

Return to the Summary Table.

Figure 8-31. STBY_2_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	STBY_SLEEP_CONFIG	nRSTOUT_STBY_CONFIG	GPIO_STBY_EN	RESERVED	GPO_STBY_EN
R-0h	R-0h	R-0h	R/W-Xh	R/W-Xh	R/W-Xh	R-0h	R/W-Xh

Table 8-33. STBY_2_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	STBY_SLEEP_CONFIG	R/W	X	Device operation via STBY-request. (Default from NVM memory) 0h = STBY Mode 1h = SLEEP Mode
3	nRSTOUT_STBY_CONFIG	R/W	X	nRSTOUT configuration in STANDBY state. (Default from NVM memory) 0h = nRSTOUT asserted in STBY Mode 1h = nRSTOUT de-asserted in STBY Mode
2	GPIO_STBY_EN	R/W	X	Enable GPIO in STANDBY state. (Default from NVM memory) 0h = Not enabled in STBY Mode 1h = Enabled in STBY Mode
1	RESERVED	R	0h	Reserved
0	GPO_STBY_EN	R/W	X	Enable GPO in STANDBY state. (Default from NVM memory) 0h = Not enabled in STBY Mode 1h = Enabled in STBY Mode

8.1.32 OC_DEGL_CONFIG Register (Offset = 23h) [Reset = 0Xh]

OC_DEGL_CONFIG is shown in Figure 8-32 and described in Table 8-34.

Return to the Summary Table.

Figure 8-32. OC_DEGL_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	EN_LONG_DEGL_FOR_OC_BUCK3	EN_LONG_DEGL_FOR_OC_BUCK2	EN_LONG_DEGL_FOR_OC_BUCK1
R-0h	R-0h	R-0h	R-0h	R-0h	R/W-Xh	R/W-Xh	R/W-Xh

Table 8-34. OC_DEGL_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	EN_LONG_DEGL_FOR_OC_BUCK3	R/W	X	When set, enables the long-deglitch option for OverCurrent signals of BUCK3. When clear, enables the short-deglitch option for OverCurrent signals of BUCK3. (Default from NVM memory) 0h = Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us 1h = Deglitch duration for OverCurrent signals for BUCK3 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms
1	EN_LONG_DEGL_FOR_OC_BUCK2	R/W	X	When set, enables the long-deglitch option for OverCurrent signals of BUCK2. When clear, enables the short-deglitch option for OverCurrent signals of BUCK2. (Default from NVM memory) 0h = Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us 1h = Deglitch duration for OverCurrent signals for BUCK2 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms
0	EN_LONG_DEGL_FOR_OC_BUCK1	R/W	X	When set, enables the long-deglitch option for OverCurrent signals of BUCK1. When clear, enables the short-deglitch option for OverCurrent signals of BUCK1. (Default from NVM memory) 0h = Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~20us 1h = Deglitch duration for OverCurrent signals for BUCK1 (High-Side Overcurrent, Low-Side Overcurrent and Low-Side Reverse/Negative OverCurrent) is ~2ms

8.1.33 INT_MASK_UV Register (Offset = 24h) [Reset = XXh]

INT_MASK_UV is shown in Figure 8-33 and described in Table 8-35.

Return to the Summary Table.

Figure 8-33. INT_MASK_UV Register

7	6	5	4	3	2	1	0
MASK_RETRY_COUNT	BUCK3_UV_MASK	BUCK2_UV_MASK	BUCK1_UV_MASK	RESERVED	LDO1_UV_MASK	LDO2_UV_MASK	RESERVED
R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R-0h	R/W-Xh	R/W-Xh	R-0h

Table 8-35. INT_MASK_UV Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_RETRY_COUNT	R/W	X	When set, device can power up even after two retries. (Default from NVM memory) 0h = Device does retry up to 2 times, then stay off 1h = Device does retry infinitely
6	BUCK3_UV_MASK	R/W	X	BUCK3 Undervoltage Mask. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
5	BUCK2_UV_MASK	R/W	X	BUCK2 Undervoltage Mask. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
4	BUCK1_UV_MASK	R/W	X	BUCK1 Undervoltage Mask. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
3	RESERVED	R	0h	Reserved
2	LDO1_UV_MASK	R/W	X	LDO1 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
1	LDO2_UV_MASK	R/W	X	LDO2 Undervoltage Mask - Always masked in BYP or LSW modes. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
0	RESERVED	R	0h	Reserved

8.1.34 MASK_CONFIG Register (Offset = 25h) [Reset = XXh]

MASK_CONFIG is shown in Figure 8-34 and described in Table 8-36.

Return to the Summary Table.

Figure 8-34. MASK_CONFIG Register

7	6	5	4	3	2	1	0
MASK_INT_FOR_PB	MASK_EFFECT		MASK_INT_FOR_RV	SENSOR_0_WARM_MASK	SENSOR_1_WARM_MASK	SENSOR_2_WARM_MASK	RESERVED
R/W-Xh	R/W-Xh		R/W-Xh	R/W-Xh	R/W-Xh	R/W-Xh	R-0h

Table 8-36. MASK_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK_INT_FOR_PB	R/W	X	Masking bit to control whether nINT pin is sensitive to PushButton (PB) press/release events or not. (Default from NVM memory) 0h = un-masked (nINT pulled low for any PB events) 1h = masked (nINT not sensitive to any PB events)
6-5	MASK_EFFECT	R/W	X	Effect of masking (global) (Default from NVM memory) 0h = no state change, no nINT reaction, no bit set for Faults 1h = no state change, no nINT reaction, bit set for Faults 2h = no state change, nINT reaction, bit set for Faults (same as 11b) 3h = no state change, nINT reaction, bit set for Faults (same as 10b)
4	MASK_INT_FOR_RV	R/W	X	Masking bit to control whether nINT pin is sensitive to RV (Residual Voltage) events or not. (Default from NVM memory) 0h = un-masked (nINT pulled low for any RV events during transition to ACTIVE state or during enabling of rails) 1h = masked (nINT not sensitive to any RV events)
3	SENSOR_0_WARM_MASK	R/W	X	Die Temperature Warm Fault Mask, Sensor 0. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
2	SENSOR_1_WARM_MASK	R/W	X	Die Temperature Warm Fault Mask, Sensor 1. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
1	SENSOR_2_WARM_MASK	R/W	X	Die Temperature Warm Fault Mask, Sensor 2. (Default from NVM memory) 0h = un-masked (Faults reported) 1h = masked (Faults not reported)
0	RESERVED	R	0h	Reserved

8.1.35 I2C_ADDRESS_REG Register (Offset = 26h) [Reset = XXh]

I2C_ADDRESS_REG is shown in Figure 8-35 and described in Table 8-37.

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Figure 8-35. I2C_ADDRESS_REG Register

7	6	5	4	3	2	1	0
DIY_NVM_PROGRAM_CMD_ISSUED	I2C_ADDRESS						
R/W-Xh	R/W-Xh						

Table 8-37. I2C_ADDRESS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIY_NVM_PROGRAM_CMD_ISSUED	R/W	X	Bit that indicates whether a DIY program command was attempted. Once set, remains always set. (Default from NVM memory) 0h = NVM data not changed 1h = NVM data attempted to be changed via DIY program command
6-0	I2C_ADDRESS	R/W	X	I2C secondary address. Note: Ok to change during operation, but consider immediate reaction: new address for read/write! (Default from NVM memory)

8.1.36 USER_GENERAL_NVM_STORAGE_REG Register (Offset = 27h) [Reset = XXh]

USER_GENERAL_NVM_STORAGE_REG is shown in Figure 8-36 and described in Table 8-38.

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Figure 8-36. USER_GENERAL_NVM_STORAGE_REG Register

7	6	5	4	3	2	1	0
USER_CONFIG_PROG	USER_GENERAL_NVM_STORAGE						
R/W-Xh	R/W-Xh						

Table 8-38. USER_GENERAL_NVM_STORAGE_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	USER_CONFIG_PROG	R/W	X	Indicate User Config area of NVM has been Programmed. (Default from NVM memory) 0h = User Area has not been programmed 1h = User Area has been programmed
6-0	USER_GENERAL_NVM_STORAGE	R/W	X	8-bit NVM-based register available to the user to use to store user-data, for example NVM-ID of customer-modified NVM-version or other purposes. (Default from NVM memory)

8.1.37 MANUFACTURING_VER Register (Offset = 28h) [Reset = 00h]

MANUFACTURING_VER is shown in Figure 8-37 and described in Table 8-39.

Return to the Summary Table.

Figure 8-37. MANUFACTURING_VER Register

7	6	5	4	3	2	1	0
SILICON_REV							
R-0h							

Table 8-39. MANUFACTURING_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SILICON_REV	R	0h	SILICON_REV[7:6] - Reserved SILICON_REV[5:3] - ALR SILICON_REV[2:0] - Metal Silicon Revision - Hard wired (not under NVM control)

8.1.38 MFP_CTRL Register (Offset = 29h) [Reset = 00h]

MFP_CTRL is shown in Figure 8-38 and described in Table 8-40.

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Figure 8-38. MFP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	GPIO_STATUS	WARM_RESET_I2C_CTRL	COLD_RESET_I2C_CTRL	STBY_I2C_CTRL	I2C_OFF_REQ
R-0h	R-0h	R-0h	R-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 8-40. MFP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	GPIO_STATUS	R	0h	Indicates the real-time value of GPIO pin 0h = The GPIO pin is currently '0' 1h = The GPIO pin is currently '1'
3	WARM_RESET_I2C_CTRL	R/W	0h	Triggers a WARM RESET when written as '1'. Note: This bit self-clears automatically, so cannot be read as '1' after the write. 0h = normal operation 1h = WARM_RESET
2	COLD_RESET_I2C_CTRL	R/W	0h	Triggers a COLD RESET when set high. Cleared upon entry to INITIALIZE. 0h = normal operation 1h = COLD_RESET
1	STBY_I2C_CTRL	R/W	0h	STBY control using I2C. Consolidated with STBY control via MODE/STBY pin. Refer to MODE and STBY configuration table and STBY_SLEEP_CONFIG bit. 0h = normal operation 1h = STBY or SLEEP mode
0	I2C_OFF_REQ	R/W	0h	When '1' is written to this bit: Trigger OFF request. When '0': No effect. Does self-clear. 0h = No effect 1h = Trigger OFF Request

8.1.39 DISCHARGE_CONFIG Register (Offset = 2Ah) [Reset = 37h]

DISCHARGE_CONFIG is shown in Figure 8-39 and described in Table 8-41.

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Figure 8-39. DISCHARGE_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO1_DISCHARGE_EN	LDO2_DISCHARGE_EN	RESERVED	BUCK3_DISCHARGE_EN	BUCK2_DISCHARGE_EN	BUCK1_DISCHARGE_EN
R-0h	R-0h	R/W-1h	R/W-1h	R-0h	R/W-1h	R/W-1h	R/W-1h

Table 8-41. DISCHARGE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	LDO1_DISCHARGE_EN	R/W	1h	Discharge setting for LDO1 0h = No Discharge 1h = 250 W
4	LDO2_DISCHARGE_EN	R/W	1h	Discharge setting for LDO2 0h = No Discharge 1h = 200 W
3	RESERVED	R	0h	Reserved
2	BUCK3_DISCHARGE_EN	R/W	1h	Discharge setting for BUCK3 0h = No Discharge 1h = 125 W
1	BUCK2_DISCHARGE_EN	R/W	1h	Discharge setting for BUCK2 0h = No Discharge 1h = 125 W
0	BUCK1_DISCHARGE_EN	R/W	1h	Discharge setting for BUCK1 0h = No Discharge 1h = 125 W

8.1.40 INT_SOURCE Register (Offset = 2Bh) [Reset = 00h]

INT_SOURCE is shown in Figure 8-40 and described in Table 8-42.

Return to the Summary Table.

Figure 8-40. INT_SOURCE Register

7	6	5	4	3	2	1	0
INT_PB_IS_SET	RESERVED	INT_LDO_1_2_IS_SET	INT_BUCK_3_IS_SET	INT_BUCK_1_2_IS_SET	INT_SYSTEM_IS_SET	INT_RV_IS_SET	INT_TIMEOUT_RV_SD_IS_SET
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 8-42. INT_SOURCE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_PB_IS_SET	R	0h	One or more sources of the INT present in register INT_PB 0h = No bits set in INT_PB 1h = One or more bits set in INT_PB
6	RESERVED	R	0h	Reserved
5	INT_LDO_1_2_IS_SET	R	0h	One or more sources of the INT present in register INT_LDO_1_2 0h = No bits set in INT_LDO_1_2 1h = One or more bits set in INT_LDO_1_2
4	INT_BUCK_3_IS_SET	R	0h	One or more sources of the INT present in register INT_BUCK_3 0h = No bits set in INT_BUCK_3 1h = One or more bits set in INT_BUCK_3
3	INT_BUCK_1_2_IS_SET	R	0h	One or more sources of the INT present in register INT_BUCK_1_2 0h = No bits set in INT_BUCK_1_2 1h = One or more bits set in INT_BUCK_1_2
2	INT_SYSTEM_IS_SET	R	0h	One or more sources of the INT present in register INT_SYSTEM 0h = No bits set in INT_SYSTEM 1h = One or more bits set in INT_SYSTEM
1	INT_RV_IS_SET	R	0h	One or more sources of the INT present in register INT_RV 0h = No bits set in INT_RV 1h = One or more bits set in INT_RV
0	INT_TIMEOUT_RV_SD_IS_SET	R	0h	One or more sources of the INT present in register INT_TIMEOUT_RV_SD 0h = No bits set in INT_TIMEOUT_RV_SD 1h = One or more bits set in INT_TIMEOUT_RV_SD

8.1.41 INT_LDO_1_2 Register (Offset = 2Dh) [Reset = 00h]

INT_LDO_1_2 is shown in Figure 8-41 and described in Table 8-43.

Return to the Summary Table.

Figure 8-41. INT_LDO_1_2 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO2_UV	LDO2_OC	LDO2_SCG	LDO1_UV	LDO1_OC	LDO1_SCG
R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-43. INT_LDO_1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	LDO2_UV	R/W1C	0h	LDO2 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1' 0h = No Fault detected 1h = Fault detected
4	LDO2_OC	R/W1C	0h	LDO2 Overcurrent Fault 0h = No Fault detected 1h = Fault detected
3	LDO2_SCG	R/W1C	0h	LDO2 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected
2	LDO1_UV	R/W1C	0h	LDO1 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1' 0h = No Fault detected 1h = Fault detected
1	LDO1_OC	R/W1C	0h	LDO1 Overcurrent Fault 0h = No Fault detected 1h = Fault detected
0	LDO1_SCG	R/W1C	0h	LDO1 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected

8.1.42 INT_BUCK_3 Register (Offset = 2Eh) [Reset = 00h]

INT_BUCK_3 is shown in Figure 8-42 and described in Table 8-44.

Return to the Summary Table.

Figure 8-42. INT_BUCK_3 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	BUCK3_UV	BUCK3_NEG_OC	BUCK3_OC	BUCK3_SCG
R-0h	R-0h	R-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-44. INT_BUCK_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	BUCK3_UV	R/W1C	0h	BUCK3 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1' 0h = No Fault detected 1h = Fault detected
2	BUCK3_NEG_OC	R/W1C	0h	BUCK3 Negative Overcurrent Fault 0h = No Fault detected 1h = Fault detected
1	BUCK3_OC	R/W1C	0h	BUCK3 Positive Overcurrent Fault 0h = No Fault detected 1h = Fault detected
0	BUCK3_SCG	R/W1C	0h	BUCK3 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected

8.1.43 INT_BUCK_1_2 Register (Offset = 2Fh) [Reset = 00h]

INT_BUCK_1_2 is shown in Figure 8-43 and described in Table 8-45.

Return to the Summary Table.

Figure 8-43. INT_BUCK_1_2 Register

7	6	5	4	3	2	1	0
BUCK2_UV	BUCK2_NEG_OC	BUCK2_OC	BUCK2_SCG	BUCK1_UV	BUCK1_NEG_OC	BUCK1_OC	BUCK1_SCG
R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-45. INT_BUCK_1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BUCK2_UV	R/W1C	0h	BUCK2 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1' 0h = No Fault detected 1h = Fault detected
6	BUCK2_NEG_OC	R/W1C	0h	BUCK2 Negative Overcurrent Fault 0h = No Fault detected 1h = Fault detected
5	BUCK2_OC	R/W1C	0h	BUCK2 Positive Overcurrent Fault 0h = No Fault detected 1h = Fault detected
4	BUCK2_SCG	R/W1C	0h	BUCK2 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected
3	BUCK1_UV	R/W1C	0h	BUCK1 Undervoltage Fault. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_UV_MASK bit in register INT_MASK_UV is '1' 0h = No Fault detected 1h = Fault detected
2	BUCK1_NEG_OC	R/W1C	0h	BUCK1 Negative Overcurrent Fault 0h = No Fault detected 1h = Fault detected
1	BUCK1_OC	R/W1C	0h	BUCK1 Positive Overcurrent Fault 0h = No Fault detected 1h = Fault detected
0	BUCK1_SCG	R/W1C	0h	BUCK1 Short Circuit to Ground Fault 0h = No Fault detected 1h = Fault detected

8.1.44 INT_SYSTEM Register (Offset = 30h) [Reset = 00h]

INT_SYSTEM is shown in Figure 8-44 and described in Table 8-46.

Return to the Summary Table.

Figure 8-44. INT_SYSTEM Register

7	6	5	4	3	2	1	0
SENSOR_0_HOT	SENSOR_1_HOT	SENSOR_2_HOT	RESERVED	SENSOR_0_WARM	SENSOR_1_WARM	SENSOR_2_WARM	RESERVED
R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h

Table 8-46. INT_SYSTEM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SENSOR_0_HOT	R/W1C	0h	TSD Hot detection for sensor 0 0h = No Fault detected 1h = Fault detected
6	SENSOR_1_HOT	R/W1C	0h	TSD Hot detection for sensor 1 0h = No Fault detected 1h = Fault detected
5	SENSOR_2_HOT	R/W1C	0h	TSD Hot detection for sensor 2 0h = No Fault detected 1h = Fault detected
4	RESERVED	R	0h	Reserved
3	SENSOR_0_WARM	R/W1C	0h	TSD Warm detection for sensor 0. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1' 0h = No Fault detected 1h = Fault detected
2	SENSOR_1_WARM	R/W1C	0h	TSD Warm detection for sensor 1. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1' 0h = No Fault detected 1h = Fault detected
1	SENSOR_2_WARM	R/W1C	0h	TSD Warm detection for sensor 2. Is automatically cleared upon a transition to INITIALIZE state, if corresponding *_WARM_MASK bit in register MASK_CONFIG is '1' 0h = No Fault detected 1h = Fault detected
0	RESERVED	R	0h	Reserved

8.1.45 INT_RV Register (Offset = 31h) [Reset = 00h]

INT_RV is shown in Figure 8-45 and described in Table 8-47.

Return to the Summary Table.

Figure 8-45. INT_RV Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	LDO2_RV	RESERVED	LDO1_RV	BUCK3_RV	BUCK2_RV	BUCK1_RV
R-0h	R-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-47. INT_RV Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	LDO2_RV	R/W1C	0h	RV event detected on LDO2 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state 0h = No RV detected 1h = RV detected
4	RESERVED	R	0h	Reserved
3	LDO1_RV	R/W1C	0h	RV event detected on LDO1 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state 0h = No RV detected 1h = RV detected
2	BUCK3_RV	R/W1C	0h	RV event detected on BUCK3 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state 0h = No RV detected 1h = RV detected
1	BUCK2_RV	R/W1C	0h	RV event detected on BUCK2 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state 0h = No RV detected 1h = RV detected
0	BUCK1_RV	R/W1C	0h	RV event detected on BUCK1 rail during rail-turn-on, or after 4-5 ms during discharge checks prior to entering power sequence to ACTIVE state 0h = No RV detected 1h = RV detected

8.1.46 INT_TIMEOUT_RV_SD Register (Offset = 32h) [Reset = 00h]

INT_TIMEOUT_RV_SD is shown in Figure 8-46 and described in Table 8-48.

Return to the Summary Table.

Figure 8-46. INT_TIMEOUT_RV_SD Register

7	6	5	4	3	2	1	0
TIMEOUT	RESERVED	LDO1_RV_SD	LDO2_RV_SD	RESERVED	BUCK3_RV_SD	BUCK2_RV_SD	BUCK1_RV_SD
R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R-0h	R/W1C-0h	R/W1C-0h	R/W1C-0h

Table 8-48. INT_TIMEOUT_RV_SD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TIMEOUT	R/W1C	0h	Is set if ShutDown occurred due to a TimeOut while: 1. Transitioning to ACTIVE state, and one or more rails did not rise past the UV level at the end of the assigned slot (and UV on this rail is configured as a SD fault). Which rail(s) is/are indicated by the *_UV bits in the INT_* registers. 2. Transitioning to STANDBY state, and one or more rails did not fall below the SCG level at the end of the assigned slot and discharge is enabled for that rail (which rail(s) is/are indicated by the corresponding RV_SD bit(s) in this register). 0h = No SD due to TimeOut occurred 1h = SD due to TimeOut occurred
6	RESERVED	R	0h	Reserved
5	LDO1_RV_SD	R/W1C	0h	RV on LDO1 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was shutdown and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case) 0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO1 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on LDO1 occurred
4	LDO2_RV_SD	R/W1C	0h	RV on LDO2 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was shutdown and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case) 0h = No SD due to RV/DISCHARGE_TIMEOUT on LDO2 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on LDO2 occurred
3	RESERVED	R	0h	Reserved
2	BUCK3_RV_SD	R/W1C	0h	RV on BUCK3 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was shutdown and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case) 0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK3 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK3 occurred

Table 8-48. INT_TIMEOUT_RV_SD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	BUCK2_RV_SD	R/W1C	0h	RV on BUCK2 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was shutdown and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case) 0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK2 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK2 occurred
0	BUCK1_RV_SD	R/W1C	0h	RV on BUCK2 rail caused a shutdown during: 1. A transition to STANDBY state, this rail did not discharge at the end of the assigned slot and discharge is enabled for this rail 2. A transition to STANDBY state, RV was observed on this rail during the transition after this rail was shutdown and discharge was enabled 3. A transition to ACTIVE state, RV was observed on this rail during the transition when this rail was OFF (rails are expected to be discharged before commencing the sequence to ACTIVE) 4. This rail did not discharge and therefore caused a Timeout-SD while attempting to discharge all rails at the start of a transition from STANDBY to ACTIVE (TIMEOUT bit gets also set in this case) 0h = No SD due to RV/DISCHARGE_TIMEOUT on BUCK1 occurred 1h = SD due to RV/DISCHARGE_TIMEOUT on BUCK1 occurred

8.1.47 INT_PB Register (Offset = 33h) [Reset = 04h]

INT_PB is shown in Figure 8-47 and described in Table 8-49.

Return to the Summary Table.

Figure 8-47. INT_PB Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	PB_EN_SLEEP_EXIT_TIMEOUT	PB_REAL_TIME_STATUS	PB_RISING_EDGE_DETECTED	PB_FALLING_EDGE_DETECTED
R-0h	R-0h	R-0h	R-0h	R/W1C-0h	R-1h	R/W1C-0h	R/W1C-0h

Table 8-49. INT_PB Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RESERVED	R	0h	Reserved
5	RESERVED	R	0h	Reserved
4	RESERVED	R	0h	Reserved
3	PB_EN_SLEEP_EXIT_TIMEOUT	R/W1C	0h	Device re-entered SLEEP state following a wakeup timeout. Valid only when EN/PB/VSENSE pin is configured as PB or EN. 0h = No SLEEP mode exit timeout detected 1h = SLEEP mode exit timeout detected
2	PB_REAL_TIME_STATUS	R	1h	Deglitched (64-128ms) real-time status of PB pin. Valid only when EN/PB/VSENSE pin is configured as PB. 0h = Current deglitched status of PB: PRESSED 1h = Current deglitched status of PB: RELEASED
1	PB_RISING_EDGE_DETECTED	R/W1C	0h	PB was released for > deglitch period (64-128ms) since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB='0'). 0h = No PB-release detected 1h = PB-release detected
0	PB_FALLING_EDGE_DETECTED	R/W1C	0h	PB was pressed for > deglitch period (64-128ms) since the previous time this bit was cleared. This bit when set, does assert nINT pin (if config bit MASK_INT_FOR_PB='0'). 0h = No PB-press detected 1h = PB-press detected

8.1.48 USER_NVM_CMD_REG Register (Offset = 34h) [Reset = 00h]

USER_NVM_CMD_REG is shown in Figure 8-48 and described in Table 8-50.

Return to the Summary Table.

Figure 8-48. USER_NVM_CMD_REG Register

7	6	5	4	3	2	1	0
CUST_NVM_VERIFY_ERR	CUST_NVM_VERIFY_DONE	CUST_PROG_DONE	I2C_OSC_ON	USER_NVM_CMD			
R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h	R-0h			

Table 8-50. USER_NVM_CMD_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CUST_NVM_VERIFY_ERR	R/W1C	0h	Flag indicating a NVM verify error, set immediately after the NVM verify function has been run. 0h = PASS 1h = FAIL
6	CUST_NVM_VERIFY_DONE	R/W1C	0h	Is set to '1' after a CUST_NVM_VERIFY_CMD is executed. Remains '1' until W1C by user. 0h = Not yet done / not in progress 1h = Done
5	CUST_PROG_DONE	R/W1C	0h	Is set to '1' after a CUST_PROG_CMD is executed. Remains '1' until W1C by user. 0h = Not yet done / not in progress 1h = Done
4	I2C_OSC_ON	R	0h	This register field is set to '1' if an EN_OSC_DIY is received. 0h = OSC not controlled via I2C 1h = OSC unconditionally ON due to I2C command EN_OSC_DIY
3-0	USER_NVM_CMD	R	0h	Commands to enter DIY programming mode and program user NVM space. Always reads as 0. 6h = DIS_OSC_DIY 7h = CUST_NVM_VERIFY_CMD 9h = EN_OSC_DIY Ah = CUST_PROG_CMD

8.1.49 POWER_UP_STATUS_REG Register (Offset = 35h) [Reset = 00h]

POWER_UP_STATUS_REG is shown in Figure 8-49 and described in Table 8-51.

Return to the Summary Table.

Figure 8-49. POWER_UP_STATUS_REG Register

7	6	5	4	3	2	1	0
POWER_UP_FROM_FSD	POWER_UP_FROM_EN_PB_VSENSE	COLD_RESET_ISSUED	STATE		RETRY_COUNT		POWER_UP_FROM_OFF
R/W1C-0h	R/W1C-0h	R/W1C-0h	R-0h		R-0h		R/W1C-0h

Table 8-51. POWER_UP_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	POWER_UP_FROM_FSD	R/W1C	0h	Is set if ON_REQ was triggered due to FSD 0h = No power-up via FSD detected 1h = Power-up via FSD detected
6	POWER_UP_FROM_EN_PB_VSENSE	R/W1C	0h	Is set if ON_REQ was triggered due to EN/PB/VSENSE pin 0h = No power-up via pin detected 1h = Power-up via pin detected
5	COLD_RESET_ISSUED	R/W1C	0h	Is set if we received a COLD_RESET over I2C 0h = No COLD RESET received 1h = COLD RESET received through I2C
4-3	STATE	R	0h	Indicates the current device state 0h = Transition state 1h = INITIALIZE 2h = STANDBY 3h = ACTIVE
2-1	RETRY_COUNT	R	0h	Reads the current retry count in the state machine. If RETRY_COUNT = 3 and is not masked, device does not power up.
0	POWER_UP_FROM_OFF	R/W1C	0h	Indicates if we powered up from OFF state (UVLO was asserted) 0h = OFF state not entered since the previous clearing of this bit 1h = OFF state was entered since the previous clearing of this bit

8.1.50 SPARE_2 Register (Offset = 36h) [Reset = 00h]

SPARE_2 is shown in Figure 8-50 and described in Table 8-52.

Return to the Summary Table.

Figure 8-50. SPARE_2 Register

7	6	5	4	3	2	1	0
SPARE_2_1							
R/W-0h							

Table 8-52. SPARE_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPARE_2_1	R/W	0h	Spare bit in user non-NVM space

8.1.51 SPARE_3 Register (Offset = 37h) [Reset = 01h]

SPARE_3 is shown in Figure 8-51 and described in Table 8-53.

Return to the Summary Table.

Figure 8-51. SPARE_3 Register

7	6	5	4	3	2	1	0
SPARE_3_1							REG_LOCK_STATUS
R/W-0h							R-1h

Table 8-53. SPARE_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SPARE_3_1	R/W	0h	Spare bit in user non-NVM space
0	REG_LOCK_STATUS	R	1h	Register lock status 0h = Write access allowed based on REG_LOCK register 1h = Write access not allowed based on REG_LOCK register

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections provide detail on the proper usage of the PMIC. Each orderable part number has unique default non-volatile memory (NVM) settings and the relevant Technical Reference Manual (TRM) for that orderable is available in the product folder, under Technical Documentation. Refer to these TRMs for specific application information. More generic topics and some examples are outlined here.

To help with new designs, a variety of tools and documents are available in the product folder. Some examples are:

- Evaluation module and user guide.
- GUI to communicate with the PMIC
- Schematic and layout checklist
- User's guide describing how to power specific processors and SoCs with the PMIC.
- Technical Reference Manual (TRM) describing the default register settings on each orderable.

9.2 Typical Application

The TPS65214 PMIC contains 5 regulators; 3 Buck converters and 2 Low Drop-out Regulators (LDOs). In addition to the power resources, it also integrates 3 configurable multi-function pins, 1 GPO and I2C communication making this power management IC a cost and size optimized device for powering a wide range of processors, microcontrollers, and SoCs. There are several considerations to take into account when designing the TPS65214 to power a processor and peripherals. The number of regulators needed, the required sequencing, the load current requirements, and the voltage characteristics are all critical in determining the number of supply rails as well as the external components used with it. The following section provides a generic case. For specific cases, refer to the relevant user's guide and TRM based on the orderable part number.

9.2.1 Typical Application Example

In this example, a single TPS65214 PMIC is used to power a generic processor. This power distribution network (PDN) shows a 3.3V input supply to the Bucks and LDOs . Since Buck1 is the regulator with the highest current capabilities, it was assigned to supply the CORE rail of the processor. Buck3 is assigned to power VDDQ of the application DRAM. The GPIO/VSEL multifunction pin configured as GPIO to sequence the discrete power switch supplying 3.3V. Buck2 powers the system 1.8V IO voltage to support peripheral current requirements such as a companion WiFi device. Low-noise LDO1 supplies SoC analog power and LDO2 supplies 2.5V peripheral rail.

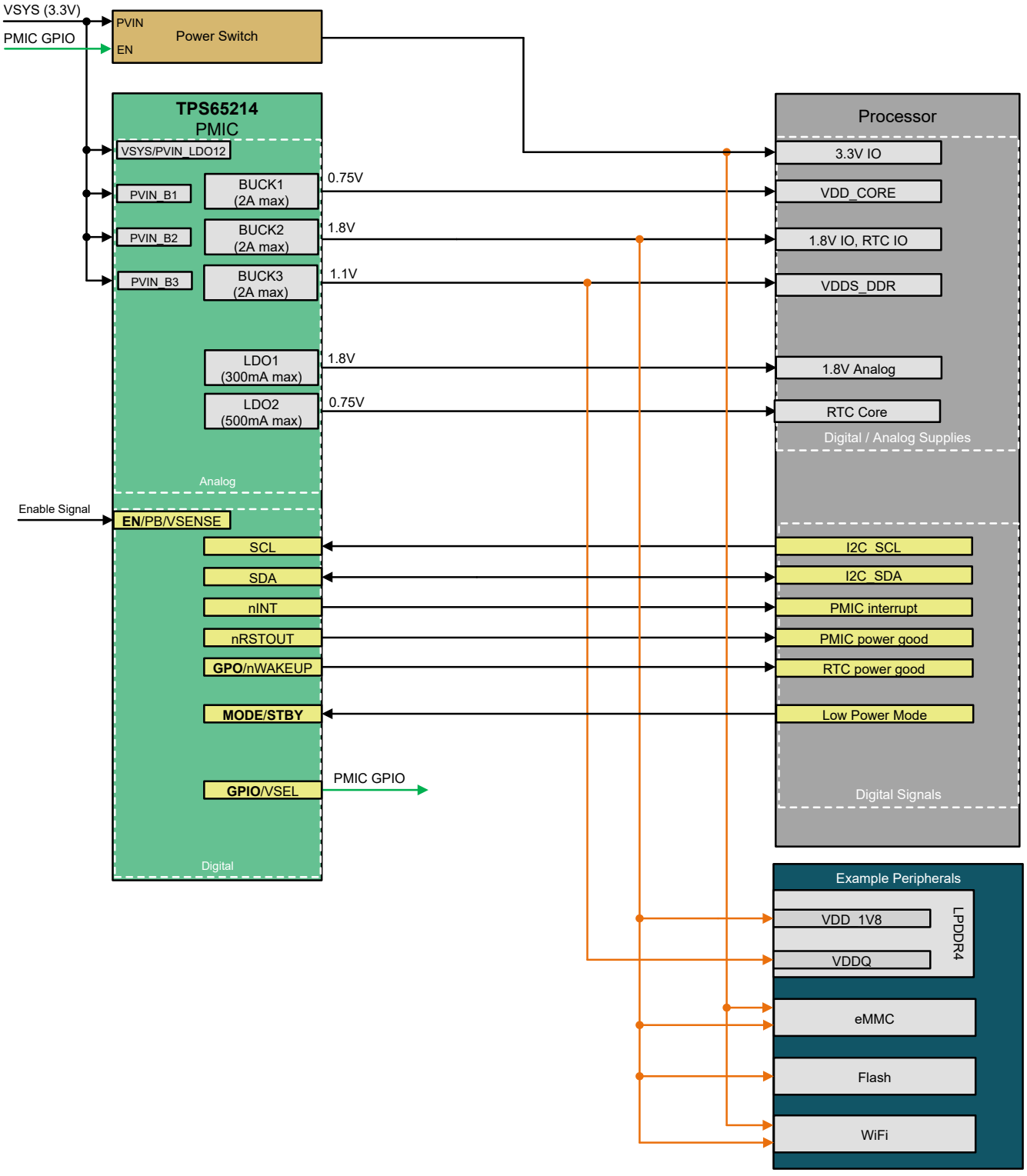


Figure 9-1. Example Power Map

9.2.2 Design Requirements

The design requirements for the typical application described on this section are outlined below:

- VDD CORE rail requires 0.75V rail with high load transient response.
- Low noise 1.8V required to supply the analog.
- 3.3V and 1.8V required to supply processor IO domains and peripherals.
- LPDDR4 requires a 1.1V rail.

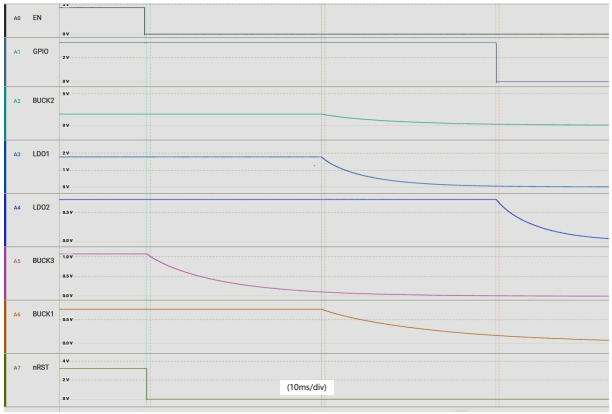
9.2.3 Detailed Design Procedure

This section describes the design procedure for each of the power modules integrated in the TPS65214 PMIC. Please note, most of the external component values that are mentioned in this section are based on the typical spec. For minimum and maximum values, refer to the corresponding parameter in the Specifications section.

9.2.3.1 Application Curves

Slot#	Duration	Assigned Rail
0	3ms	GPIO
1	0ms	
2	3ms	BUCK2 / LDO1 / LDO2
3	0ms	
4	1.5ms	BUCK3
5	1.5ms	BUCK1
6	10ms	nRSTOUT
7	10ms	

Figure 9-2. Configurable Power-up Sequence - Example



Slot#	Duration	Assigned Rail
0	10ms	nRSTOUT / BUCK3
1	0ms	
2	10ms	BUCK1 / BUCK2 / LDO1
3	0ms	
4	10ms	LDO2 / GPIO
5	0ms	
6	0ms	
7	0ms	

Figure 9-3. Configurable Power-down Sequence - Example

9.2.3.2 Buck1, Buck2, Buck3 Design Procedure

Input Capacitance - Buck1, Buck2, Buck3

Each of the Buck converters require an input capacitor on the corresponding PVIN_Bx pin. The capacitor value must be selected taking into account the voltage and temperature de-rating. Due to the nature of the switching converter, a low ESR ceramic capacitor is required for best input voltage filtering. The typical recommended capacitance is 4.7uF, 10V capacitor. Higher input capacitance can be used if the PCB size allows larger footprint.

Output Capacitance - Buck1, Buck2, Buck3

Every Buck output requires a local output capacitor to form the capacitive part of the LC output filter. Ceramic capacitor with X7 temperature coefficient are recommended. Non-automotive applications can use X6 or lower based on the operating temperature. The buck converters have two bandwidth configurations that impact the output capacitor selection. The bandwidth selection is an independent register field for each Buck converter.

Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the NVM configuration and the corresponding output capacitance requirements. Table 9-1 shows the required minimum and maximum capacitance (after derating) for each switching mode and bandwidth configuration. DC bias voltage characteristics of ceramic capacitors, tolerance, aging and temperature effects must be considered. ESR must be 10mΩ or lower.

Table 9-1. Buck Output Capacitance

Switching Mode	Bandwidth Selection	Spec parameter	Capacitance	
	Register fields: BUCK1_BW_SEL, BUCK2_BW_SEL, BUCK3_BW_SEL		Min	Max (Includes local + point of load)
Quasi-fixed frequency (auto-PFM or forced-PWM)	Low Bandwidth	COUT	10uF	75uF
	High Bandwidth	COUT_HIGH_BW	30uF	220uF

Inductor Selection - Buck1, Buck2, Buck3

Internal parameters for the buck converters are optimized for 470nH inductor. DCR must be 50mΩ or lower. Select an inductor that is rated to support saturation current of at least 5.4A.

9.2.3.3 LDO1, LDO2 Design Procedure

Input Capacitance - LDO1, LDO2

The input supply pin for LDO1 and LDO2 require an input decoupling capacitor to minimize input ripple voltage. These two LDOs share the same input supply pin with VSYS. Using a minimum of 4.7µF input capacitance is recommended. Depending on the input voltage of the LDO, a 6.3V or higher rated capacitor can be used. The same input capacitance requirements applies when the LDO is configured as LDO or load-switch.

Output Capacitance - LDO1, LDO2

LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2µF local capacitance for each LDO output with ESR of 100mOhms or less is recommended. The total capacitance (local + point of load) that each LDO can support depends on the NVM configuration. LDOx Output Capacitance shows the maximum total output capacitance allowed. Refer to the Technical Reference Manual (TRM) for the specific orderable part number to identify the LDO configuration based on the register settings and the applicable maximum total capacitance.

Table 9-2. LDOx Output Capacitance

Register setting	LDO configuration	Max total capacitance (2.2uF local + point of load)
LDOx_LSW_CONFIG		
0	LDO	40uF
1	Load-switch	50uF

9.2.3.4 VSYS, VDD1P8

The VSYS pin provides power to LDO1, LDO2, the internal VDD1P8 LDO and other internal functions. This pin requires a typical of 4.7uF ceramic capacitor. The input capacitor can be increased without any limit for better input-voltage filtering. On a typical application, this pin is connected to the same pre-regulator that supplies the PVIN_Bx pins.

VDD1P8 is an internal reference LDO and must not have any load. This pin requires a 2.2uF ceramic capacitor.

9.2.3.5 Digital Signals Design Procedure

This section describes the external connections required for the digital pins. A VIO supply of 3.3V or 1.8V is commonly used as the voltage level for the digital signals that require an external pull-up. However, higher

voltage can be used (up to the maximum spec). The VIO supply for the digital pins on the PMIC must be the same as the IO domain for the digital signal that is connected to on the processor. 100kΩ is the recommended pull-up resistor for EN/PB/VSENSE. Pull-up resistor for I2C pins can be calculated based on system requirements. All other digital pins can use 10kΩ.

If GPO or GPIO is assigned to the first slot of the power-up sequence to enable an external discrete, they can be pulled up to VSYS.

The EN/PB/VSENSE pin can be driven externally to enable the PMIC. However, if the application does not have an external signal dedicated to drive this pin, it can be pulled up to VSYS.

Note

Driving the EN/PB/VSENSE pin with an external signal is needed to wake-up the PMIC after an I2C OFF request is sent by I2C (I2C_OFF_REQ). If an OFF request is sent by I2C and the EN/PB/VSENSE is not driven by an external signal, a power cycle on VSYS must be performed to transfer the PMIC from Initialize state to Active.

Table 9-3. Digital Signals Requirements

Digital Pin	External Connection
nINT	Open-drain output. Requires external pull-up.
nRSTOUT	Open-drain output. Requires external pull-up.
EN/PB/VSENSE	When configured as EN, this signal can be driven by external logic to enable the PMIC. When configured as PB, this signal requires a pull-up resistor connected to the VSYS pin. Push-button is optional. When configured as VSENSE, this signal requires an external resistor divider to monitor the pre-regulator.
SDA	I2C clock signal. Requires external pull-up.
SCL	I2C data signal. Requires external pull-up.
GPIO/VSEL	When configured as GPIO, this pin requires external pull-up. When configured as VSEL, the initial state (pull-up or pull-down) must be set before the assigned PMIC rail ramps up. For example, if this pin is used to set the voltage on BUCK3, the state must be set before BUCK3 powers up.
GPO/nWAKEUP	Open-drain general purpose output or power-on event signal for the host. Requires external pull-up.
MODE/STBY	Input digital pin. The initial state (pull-up or pull-down) must be set before the power-up sequence is complete.

9.3 Power Supply Recommendations

The device is designed to operate with an input voltage supply range between 2.5V and 5.5V. This input supply can be generated from a single cell Li-Ion battery, two primary cells or a regulated pre-regulator. The voltage headroom required for each of the PMIC regulators must be taken into account when defining selecting the supply voltage. For the buck converters, the input supply is recommended to exceed the output voltage by at least $V_{HEADROOM\_PWM}$. For the LDOs, the input supply is recommended to exceed the output voltage by at least $V_{DROPOUTx}$. The resistance of the input supply rail must be low to prevent a UVLO fault occurring during input current transients. If the input supply is located more than a few inches from the device, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47µF is a typical choice. When using a pre-regulator to supply the PMIC, TI recommends selecting a pre-regulator without active discharge to hold the voltage at the input of the PMIC for as long as possible during a uncontrolled power-down.

CAUTION
Sequencing and Voltage requirements: The voltage on PVIN_Bx must not exceed VSYS. The Pull-up supply for the digital signals must not exceed VSYS at any point.

9.4 Layout

9.4.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design. If the layout is not carefully done, the regulators can have stability and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the device. The output capacitors must have a low impedance to ground. Use multiple VIAS (at least three) directly at the ground landing pad of the capacitor. Here are some layout guidelines:

- **PVIN_Bx**: Place the input capacitor as close to the IC as allowed by the layout DRC rules. Any extra parasitic inductance between the input cap and the PVIN_Bx pin can create a voltage spike. Use wide, short traces or polygon to help minimize trace inductance. Do not route any sensitive signals close to the input cap and the device pin as this node has high frequency switching currents. Add 3-4 vias per amp of current on the GND pads for each DCDC. If there is limited space that does not allow for the placement of the input capacitors on the same layer as the PMIC, then place the input capacitors on the opposite layer with VIAS.
- **LX_Bx**: Place the inductor close to the PMIC without compromising the PVIN input caps and use short and wide traces or polygons to connect the pin to the inductor. Do not route any sensitive signals close to this node. The inductor must be placed in the same layer as the IC to prevent having to use VIAS in the SW node. The SW-node is the main generator of EMI due to voltage swings from the input voltage to ground with very fast rise and fall times. If needed, to reduce EMI, a RC snubber can be added to the SW node.
- **FB_Bx**: Route each of the FB_Bx pins as a trace to the output capacitor. Do not extend the output voltage polygon to the FB_Bx pin as this pin requires to be routed as a trace. The trace resistance from the output capacitor to the FB_Bx pin must be less than 1Ω. The TPS65214 does not support remote sensing so the FB_Bx pins must be connected to the local capacitor of the PMIC. Avoid routing the FB_Bx close to any noisy signals such as the switch node or under the inductor to avoid coupling. If space is constraint, FB_Bx pin can be routed through an inner layer. See example layout.
- **Bucks Cout**: The local output capacitors must be placed as close to the inductor as possible to minimize electromagnetic emissions.
- **VSYS/PVIN_LDO12**: Place the input capacitor as close as possible to the VSYS/PVIN_LDO12 pin. Route this input trace away from PVIN_Bx to minimize noise coupling. If the space is limited and does not allow placement of the input capacitors on the same layer as the PMIC, then place the input capacitors on the opposite layer with VIAS, close to the IC.
- **VLDOx**: Place the output capacitor close to the VLDOx pin. For the LDO regulators, the feedback connection is internal. Therefore, keep the PCB resistance between LDO output and target load in the range of the acceptable voltage, IR, drop for LDOs.
- **VDD1P8**: Place the 2.2uF cap as close as possible to the VDD1P8 pin. This capacitor needs to be placed in the same layer as the IC. Two to Three VIAS can be used to connect the GND side of the capacitor to the GND plane of the PCB.
- **Power Pad**: The thermal pad must be connected to the PCB ground plane with a minimum of two VIAS.
- **AGND**: Do not connect AGND to the power pad (or thermal pad). The AGND pin must be connected to the PCB ground planes through a VIA. Keep the trace from the AGND pin to the VIA short.

9.4.2 Layout Example

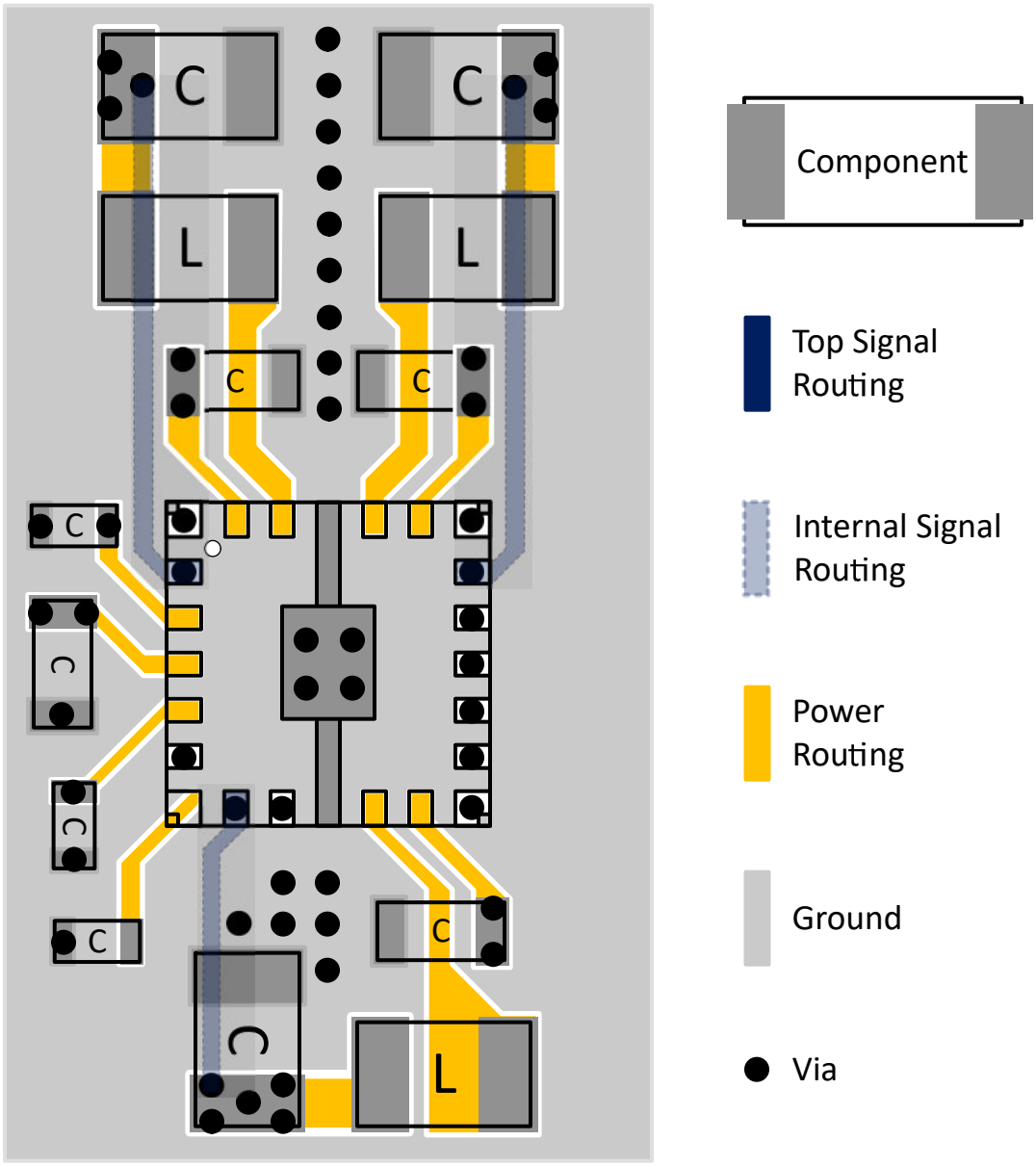


Figure 9-4. Example PMIC Layout

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2025) to Revision A (November 2025)	Page
• Changed the device status from Advance Information to Production Data	1
• Updated the Features, Device Comparison, Electrical Characteristics table, Typical Characteristics images, Feature Description, Registers, Application Information, Design Requirements, and Layout Recommendations for production data release	1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTPS6521401VAFR	Active	Preproduction	WQFN-HR (VAF) | 24	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
PTPS6521401VAFR.A	Active	Preproduction	WQFN-HR (VAF) | 24	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
TPS6521401VAFR	Active	Production	WQFN-HR (VAF) | 24	3000 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	O21401

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

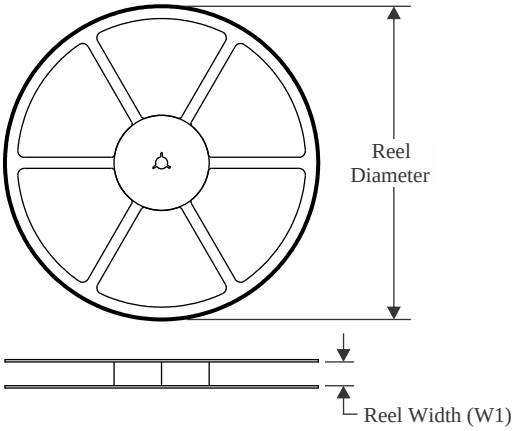
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

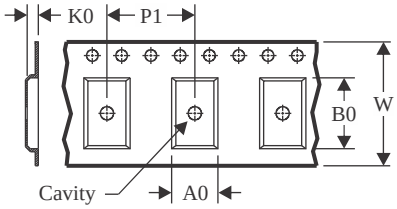
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

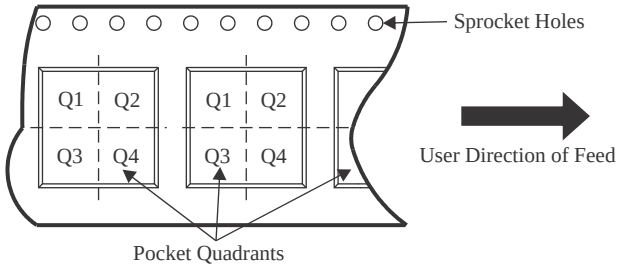


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

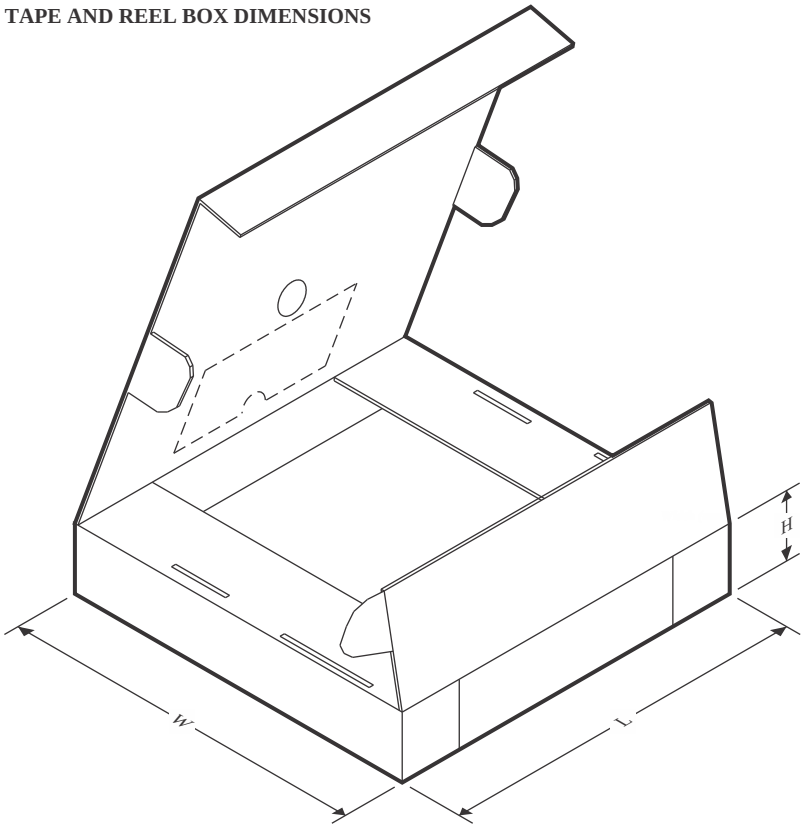
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6521401VAFR	WQFN-HR	VAF	24	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

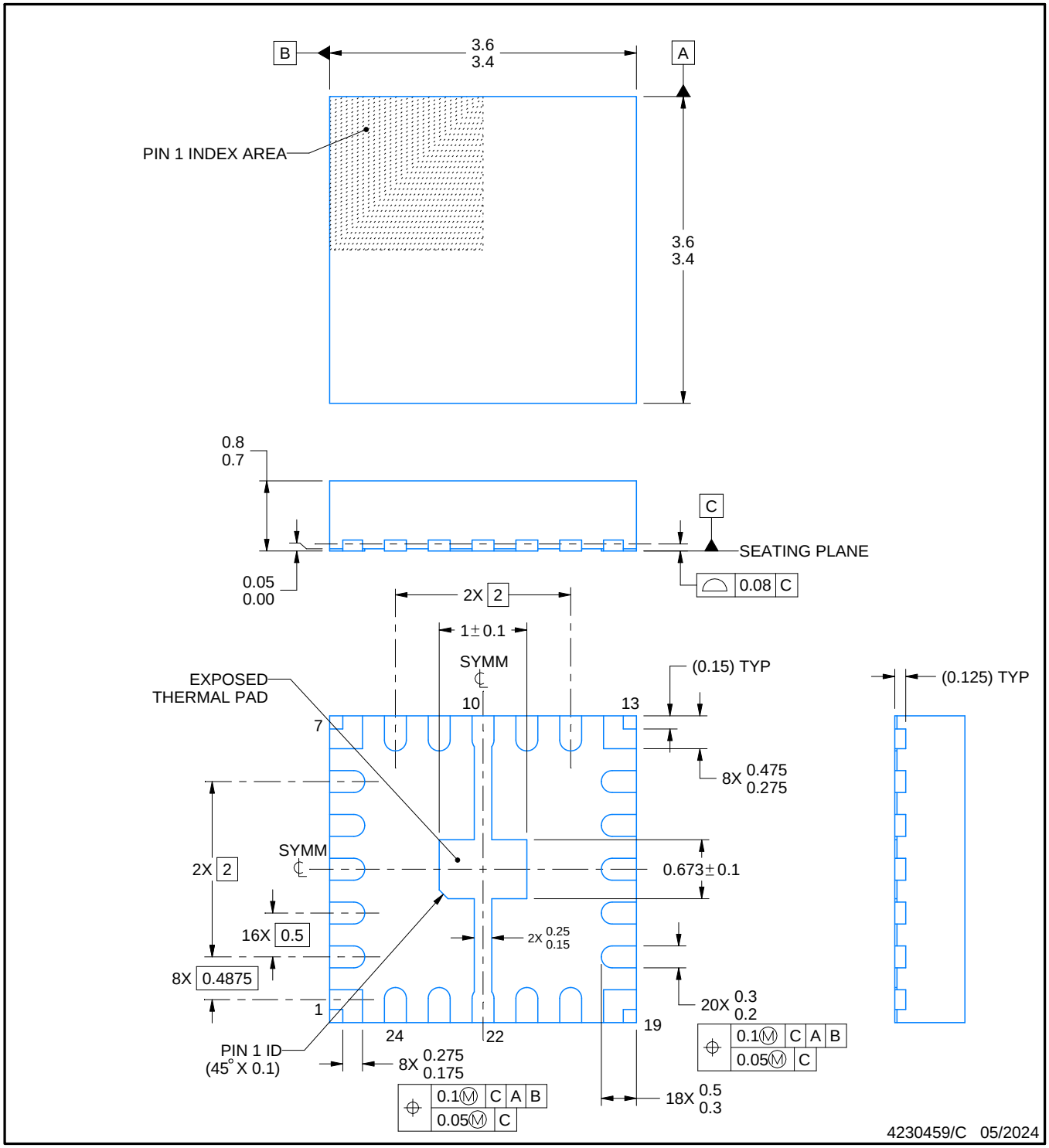
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6521401VAFR	WQFN-HR	VAF	24	3000	360.0	360.0	36.0

PACKAGE OUTLINE

VAF0024A

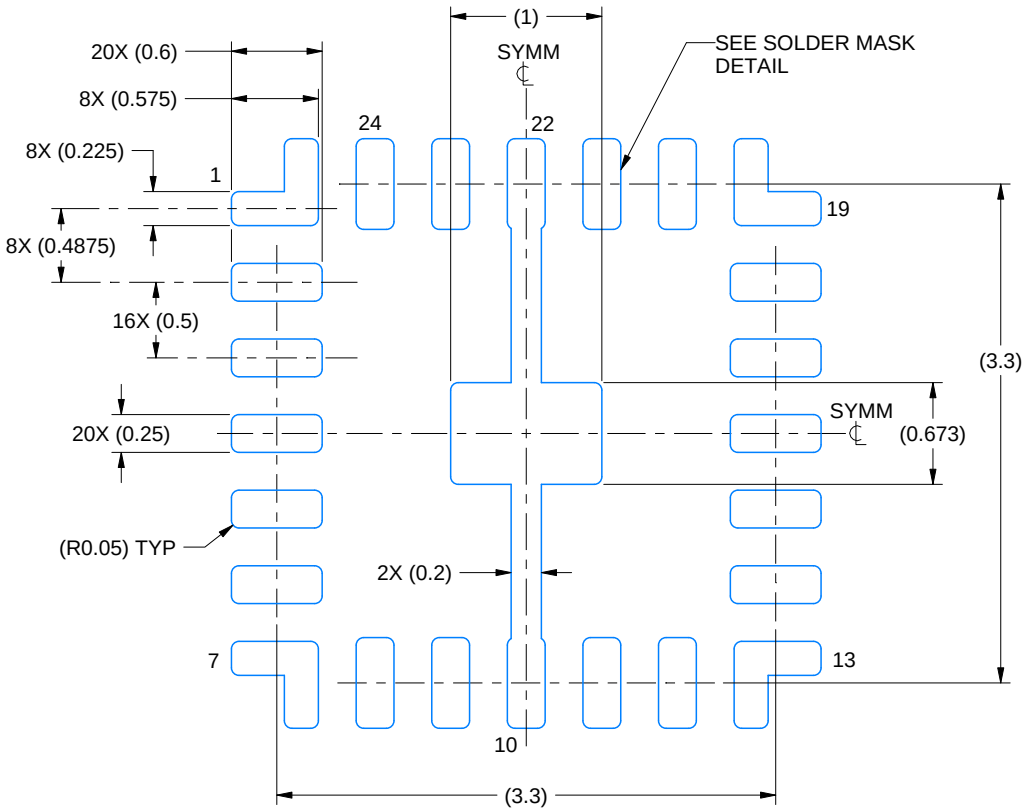
WQFN-HR - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

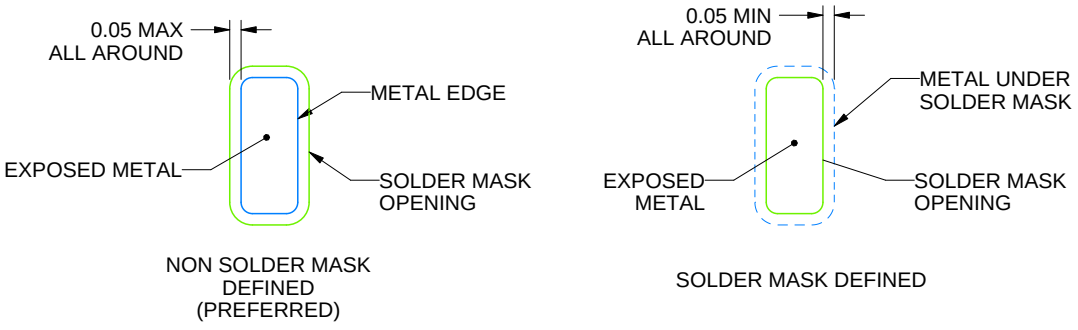


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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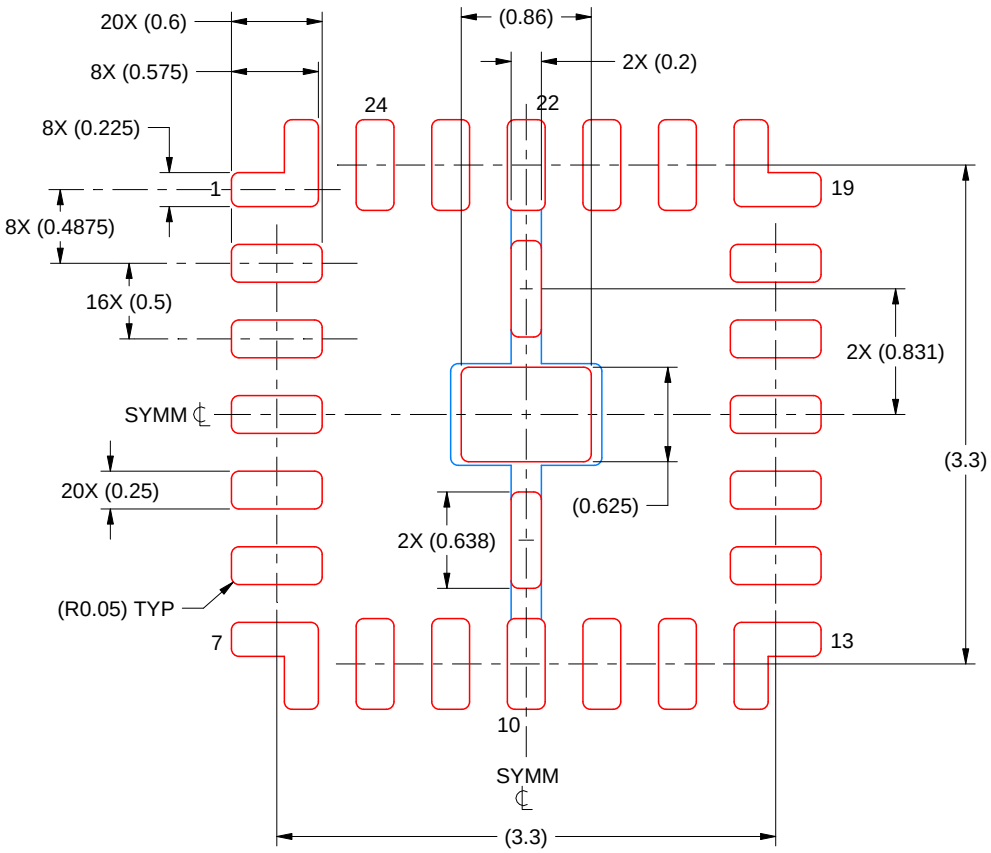
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

EXPOSED PAD CONNECTED TO PINS 10 & 22
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025