

TPS657095 PMU for Embedded Camera Module

1 Features

- Two 100mA LDOs
- Output Voltage Accuracy $\pm 1.5\%$
- V_{IN} Range From 3.7V to 6V
- LED Driver with PWM Dimming
- 1 GPO
- 1 GPIO
- I²C™ Interface
- 4KByte User OTP memory
- Available in 16-Ball DSBGA with 0.4mm Pitch

2 Applications

- Laptops
- Detachables
- Tablets
- Monitors
- Smartphones

3 Description

The TPS657095 is a power management unit targeted for embedded camera modules or other portable low power consumer end equipments. It contains two LDOs enabled by the I²C™ Interface, a PWM-dimmable current sink for driving one LED, one general purpose output (GPO), a programmable clock generator and 4K Byte of User OTP memory. The operation of the device is disabled if the input voltage supply is below the internal undervoltage lockout.

The device comes in a 16-ball die-size ball grid array package (DSBGA) with 0.4mm ball pitch.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-------------------|
| TPS657095 | DSBGA (16) | 1.70 mm x 1.70 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Circuit

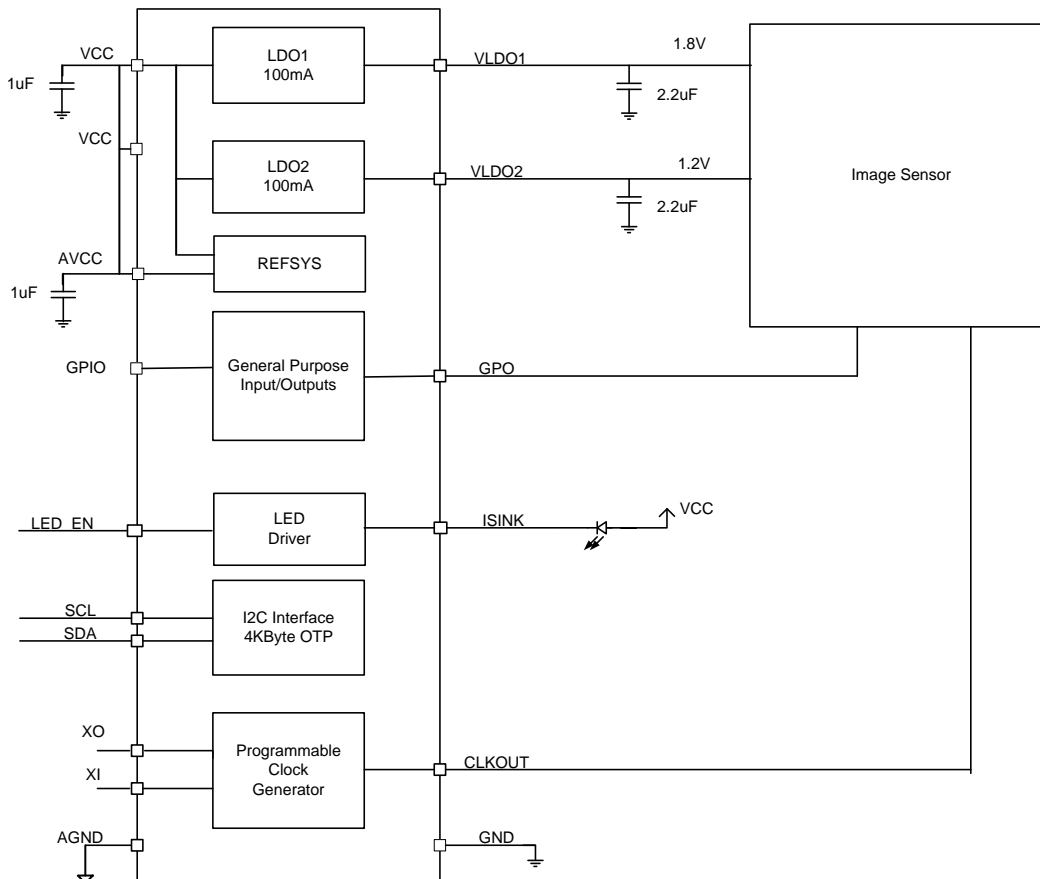


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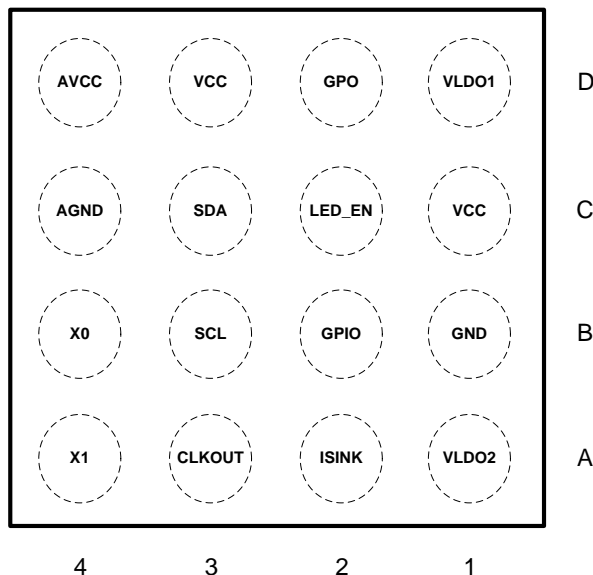
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4 Revision History

| DATE | REVISION | NOTES |
|---------------|----------|--|
| February 2016 | A | Contact TI for Rev A datasheet changes |

5 Pin Configuration and Functions

**YFF Package
16-Pin DSBGA
Top View**



Pin Functions

| PIN | | I/O | DESCRIPTION |
|--------|--------|-----|---|
| NAME | NUMBER | | |
| VCC | C1, D3 | I | Supply Input. Connect a 1uF cap close to the C1 pin. Connect pins C1 and D3 together externally. |
| GND | B1 | I | Ground connection (main device ground - connect to ground plane on PCB) |
| AVCC | D4 | I | Analog Supply Input. Connect a 1uF cap close to pin. The D4 pin must be connected externally to the D3 and C1 pins. |
| AGND | C4 | I | Analog Ground connection (device quiet ground - connect to ground plane on PCB) |
| VLDO1 | D1 | O | Output voltage from LDO1 |
| VLDO2 | A1 | O | Output voltage from LDO2 |
| ISINK | A2 | O | Open drain current sink; connect to the cathode of LED |
| GPO | D2 | O | general purpose output |
| LED_EN | C2 | I | LED enable pin (0 = disabled, 1 = enabled) |
| GPIO | B2 | I | General Purpose Input/Output (see GPIO_CTRL Register for details) As an input, it is used to enable LDO2 |
| SCL | B3 | I | clock input for the I2C compatible interface |
| SDA | C3 | I/O | data input for the I2C compatible interface |
| XO | B4 | I | connection for external crystal to clock generator (input of amplifier) |
| XI | A4 | I | connection for external crystal to clock generator (output of amplifier) |
| CLKOUT | A3 | O | clock output |

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------------------------|---|------|----------------|------|
| Voltage | All pins except GND pin with respect to AGND | -0.3 | 7 | V |
| | GPIO and GPO pull-up voltage if configured as open drain output | -0.3 | $V_{CC} + 0.3$ | V |
| | Pin VLDO1 and VLDO2 with respect to AGND | -0.3 | 3.6 | V |
| Current | VLDO1, VLDO2, VCC | | 200 | mA |
| | GND, ISINK, GPIO, GPO | | 50 | mA |
| | All other pins | | 3 | mA |
| Operating free-air temperature, T_A | | -40 | 85 | °C |
| Maximum junction temperature, T_J | | | 125 | °C |
| Storage temperature range, T_{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|-------------|-------------------------|--|-------|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 500 | V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------|---|-----|-----|-----|------|
| VCC /AVCC | Input voltage range | 3.7 | | 6 | V |
| C_{VCC} | Input capacitor at VCC | 1 | | | μF |
| C_{AVCC} | Input capacitor at AVCC | 1 | | | μF |
| V_{LDOx} | Output voltage range for LDO1 and LDO2 | 0.8 | | 3.3 | V |
| I_{LDO} | Output current at LDO1 or LDO2 | | | 75 | mA |
| $C_{OUTLDO1/2}$ | Output capacitance at V_{LDO1} , V_{LDO2} | 2.2 | | 6.8 | μF |
| LED_EN | Voltage range | 1.3 | | 6 | V |
| GPIO | Voltage range (configured as an input) | 1.3 | | 3.3 | V |
| T_A | Operating ambient temperature | -40 | | 85 | °C |
| T_J | Operating junction temperature | -40 | | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS657095 | UNIT |
|-------------------------------|--|-------------|------|
| | | YFF (DSBGA) | |
| | | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 78.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 0.6 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 13.2 | |
| Ψ_{JT} | Junction-to-top characterization parameter | 2.5 | |
| Ψ_{JB} | Junction-to-board characterization parameter | 13 | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted: $V_{CC} = AV_{CC} = 5V$, $C_{VCC} = 1\mu F$; $C_{OUTLDOx} = 2.2\mu F$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------|--|------|-------------------|------------|---------|
| SUPPLY CURRENT | | | | | | |
| V_{CC} , AV_{CC} | Supply voltage | During normal operation | 3.7 | | 6 | V |
| | | During programming (writing) of OTP memory | -5% | 5 | +5% | V |
| I_Q | Operating quiescent current | LDO1 disabled LDO2 disabled No I ² C communications LED_EN = 0 CLKout_EN = 0 24MHz crystal disabled | | 25 | 30 | μA |
| | | LDO1 disabled LDO2 enabled, $I_{OUT(LDO2)} = 0$ mA No I ² C communications LED_EN = 0 CLKout_EN = 0 24MHz crystal disabled | | 40 | 55 | μA |
| | | LDO1 enabled, $I_{OUT(LDO1)} = 0$ mA LDO2 disabled No I ² C communications LED_EN = 0 CLKout_EN = 0 24MHz crystal disabled | | 40 | 55 | μA |
| | | LDO1 enabled, $I_{OUT(LDO1)} = 0$ mA LDO2 enabled, $I_{OUT(LDO2)} = 0$ mA No I ² C communications LED_EN = 0 CLKout_EN = 0 24MHz crystal disabled | | 60 | 80 | μA |
| | | LDO1 enabled, $I_{OUT(LDO1)} = 0$ mA LDO2 enabled, $I_{OUT(LDO2)} = 0$ mA No I ² C communications LED_EN = 0 CLKout_EN = 1 24MHz crystal enabled | | 2900 | 3550 | μA |
| | | LDO1 enabled, $I_{OUT(LDO1)} = 0$ mA LDO2 enabled, $I_{OUT(LDO2)} = 0$ mA No I ² C communications LED_EN = 1, PWM Duty Cycle set to 99.9%, ISINK = 2mA CLKout_EN = 1 24MHz crystal enabled | | 3000 | 3600 | μA |
| I_{SD} | Shutdown current | Device disabled; V_{CC} and $AV_{CC} < 1.8V$ | | 45 | 85 | μA |
| LED_ENABLE | | | | | | |
| V_{IH} | High level input voltage | | 1.1 | | V_{CC} | V |
| V_{IL} | Low level input voltage | | | | 0.4 | V |
| $I_{(in)lk}$ | Input Leakage Current | | | | 0.1 | μA |
| | Input Deglitch | With a minimum pulse period of 500ns before another glitch is received | | | 100 | ns |
| GENERAL PURPOSE INPUT/OUTPUT (GPIO) | | | | | | |
| V_{IH} | High level input voltage | For VLDO1 = 1.8V | 1.1 | | VLDO1 | V |
| V_{IH} | High level input voltage | For VLDO1 = 3.3V | 1.37 | | VLDO1 | V |
| V_{IL} | Low level input voltage | For VLDO1 = 1.8V | 0 | | 0.4 | V |
| V_{IL} | Low level input voltage | For VLDO1 = 3.3V | 0 | | 0.6 | V |
| $I_{(in)lk}$ | Input leakage current | GPIO programmed as input and tied to GND or V_{CC} | | 0.01 | 0.1 | μA |
| V_{OH} | High level output voltage | Configured as a push-pull output, $I_{OH} = 1$ mA, VLDO1 $\geq 1.8V$ | 1.2 | $V_{LDO1} - 0.2V$ | V_{LDO1} | V |

Electrical Characteristics (continued)

 Unless otherwise noted: $V_{CC} = AV_{CC} = 5V$, $C_{VCC} = 1\mu F$; $C_{OUTLDOx} = 2.2\mu F$, $T_A = -40^\circ C$ to $85^\circ C$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-----|-------------------|------------|---------|
| V_{OH} | High level output voltage | Configured as a push-pull output, $I_{OH} = 1mA$, $1.3V \leq VLDO1 \leq 1.8V$ | 1.0 | | V_{LDO1} | V |
| V_{OL} | Low level output voltage | Configured as a push-pull output, $I_{OL} = 2mA$, $VLDO1 \geq 1.8V$ | | | 0.25 | V |
| V_{OL} | Low level output voltage | Configured as a push-pull output, $I_{OL} = 2mA$, $1.3V \leq VLDO1 \leq 1.8V$ | | | 0.3 | V |
| V_{OL} | Low level output voltage | Configured as an open-drain output, $I_{OL} = 4mA$, $VLDO1 \geq 1.8V$ | | | 0.6 | V |
| V_{OL} | Low level output voltage | Configured as an open-drain output, $I_{OL} = 2mA$, $1.3V \leq VLDO1 \leq 1.8V$ | | | 0.6 | V |
| $I_{(out)lkg}$ | Output leakage current | Configured as an open-drain output, GPIO connected to VLDO1 | | 0.01 | 0.1 | μA |
| GENERAL PURPOSE OUTPUT (GPO) | | | | | | |
| V_{OH} | High level output voltage | Configured as a push-pull output, $I_{OH} = 1mA$, $VLDO1 \geq 1.8V$ | 1.2 | $V_{LDO1} - 0.2V$ | V_{LDO1} | V |
| V_{OH} | High level output voltage | Configured as a push-pull output, $I_{OH} = 1mA$, $1.3V \leq VLDO1 \leq 1.8V$ | 1.0 | | V_{LDO1} | V |
| V_{OL} | Low level output voltage | Configured as a push-pull output, $I_{OL} = 2mA$, $VLDO1 \geq 1.8V$ | | | 0.25 | V |
| V_{OL} | Low level output voltage | Configured as a push-pull output, $I_{OL} = 2mA$, $1.3V \leq VLDO1 \leq 1.8V$ | | | 0.3 | V |
| V_{OL} | Low level output voltage | Configured as an open-drain output, $I_{OL} = 4mA$, $VLDO1 \geq 1.8V$ | | | 0.6 | V |
| V_{OL} | Low level output voltage | Configured as an open-drain output, $I_{OL} = 2mA$, $1.3V \leq VLDO1 \leq 1.8V$ | | | 0.6 | V |
| $I_{(out)lkg}$ | Output leakage current | Configured as an open-drain output, GPO connected to VLDO1 | | 0.01 | 0.1 | μA |
| SCL, SDA | | | | | | |
| V_{IH} | High level input voltage on SCL, SDA | | 1.2 | | V_{CC} | V |
| V_{IL} | Low level input voltage on SCL, SDA | | 0 | | 0.4 | V |
| I_{lkg} | Pin leakage current on SCL, SDA (includes leakage current for the open-drain output) | Input at V_{IL} or V_{IH} | | | 100 | nA |
| V_{OL} | Low level output voltage on SDA | For $I_{OL} = 1mA$ | | | 0.25 | V |
| UNDERVOLTAGE LOCKOUT (UVLO), SENSED AT PIN AVCC | | | | | | |
| UVLO | Internal undervoltage lockout threshold | AV_{CC} rising | 3.4 | 3.6 | 3.7 | V |
| | Internal undervoltage lockout threshold hysteresis | AV_{CC} falling | | 130 | | mV |
| CLOCK GENERATOR | | | | | | |
| f_{osc} | Frequency of external crystal | | | 24 | | MHz |
| f_{CLKOUT} | Frequency on pin CLKOUT | For OSC_FREQ[1,0] = 00 | | 24 | | MHz |
| | | For OSC_FREQ[1,0] = 01 | | 12 | | |
| | | For OSC_FREQ[1,0] = 10 | | 6 | | |
| | | For OSC_FREQ[1,0] = 11 | | 3 | | |
| | Period jitter; rms | Measured period compared to the Average Period of 10,000 randomly selected cycles | | | 600 | ps |
| | Peak period to period jitter | Measured period compared to the Average Period of 10,000 randomly selected cycles | | | 600 | ps |
| | Duty cycle of CLKout | | 40% | 50% | 60% | |
| | Rise time / fall time for clock output | 10% to 90% of output voltage, $1.3V \leq VLDO1 \leq 3.3V$ | | | 10 | ns |

Electrical Characteristics (continued)

 Unless otherwise noted: $V_{CC} = AV_{CC} = 5V$, $C_{VCC} = 1\mu F$; $C_{OUTLDOx} = 2.2\mu F$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|-------|-------------------|------------|-------------|
| | Load capacitance | Defines the maximum capacitance that can be driven by the CLKOUT buffer and still meet the specified rise/fall times | | | 15 | pF |
| | Output impedance | | | 50 | | Ω |
| V_{OH} | High level output voltage | Internally connected to $V_{LDO1} \geq 1.8V$: for $C_{OUT} = 15pF$, $I_{OH} = 1mA$ | 1.6 | $V_{LDO1} - 0.2V$ | V_{LDO1} | V |
| V_{OL} | Low level output voltage | For $C_{OUT} = 15pF$, $I_{OL} = 1mA$ | | 0.2 | 0.3 | V |
| t_{start} | Oscillator start-up time | Time from CLKout_EN=1 to CLKout active for the NXTBD-24.000M crystal, not tested in production but based on simulations | | | 10 | ms |
| THERMAL PROTECTION | | | | | | |
| T_{SD} | Thermal shutdown | Increasing junction temperature | | 150 | | $^{\circ}C$ |
| | Thermal shutdown hysteresis | Decreasing junction temperature | | 30 | | $^{\circ}C$ |
| VLDO1, VLDO2 LOW DROPOUT REGULATORS | | | | | | |
| V_{CC} | Input voltage range for LDO1 and LDO2 | | 3.7 | | 6 | V |
| V_{LDO1} | LDO1 output voltage | See LDO1_CTRL Register definition for all available voltage settings. | 0.8 | 1.8 | 3.3 | V |
| V_{LDO2} | LDO2 output voltage | See LDO2_CTRL Register definition for all available voltage settings. | 0.8 | 1.2 | 3.3 | V |
| I_O | Output current for LDO1 and LDO2 | | | | 100 | mA |
| I_{SC} | LDO1 and LDO2 short circuit current limit | $V_{LDOx} = GND$ | 110 | | 220 | mA |
| | Dropout voltage at LDO1 and LDO2 | $I_O = 75mA$; $V_{CC} \geq 3.7V$ | | | 700 | mV |
| | Output voltage accuracy for LDO1 and LDO2 | $V_{CC} = VLDO + 0.6V$ (min 3.7V) to 6V, $I_O = 2mA$ through 75mA $T = 0^{\circ}C$ to $85^{\circ}C$ | -1.5% | | 1.5% | |
| | Load Transient | $V_{CC} = AV_{CC} = 5V$, $I_{O(LDOx)} = 0A$ to 75mA in 1us | | | 10% | |
| PSRR | Power supply rejection ratio | $f = 10kHz$, $C_{OUT} \geq 2.2\mu F$ $V_{INLDOx} = 5V$, $V_{OUT} = 1.8V$, $I_{OUT} = 75mA$, | | 56 | | dB |
| | Output voltage rms noise | Voltage ripple and noise from 10kHz to 5MHz; Normal mode | | | 4 | mV |
| t_{Ramp} | V_{OUT} ramp time | Time to ramp from 5% to 95% of V_{OUT} | 24 | 50 | 200 | μs |
| R_{DIS} | Internal discharge resistor at VLDO1 and VLDO2 | $V_{IN} < UVLO$ | 200 | 400 | 550 | Ω |
| LED CURRENT SINK | | | | | | |
| I_{LED} | Isink current (LED current for 99.9% duty cycle) | | | 10 | | mA |
| | Minimum voltage drop from ISINK to GND needed for proper regulation | At $ISINK = 10mA$ | 0.3 | | | V |
| | ISINK accuracy | $ISINK = 10mA$, Duty Cycle set to 99.9% | -10% | | 5% | V |
| | PWM frequency settings | For $PWM_FREQ[1,0] = 00$ | | 23.5 | | kHz |
| | | For $PWM_FREQ[1,0] = 01$ | | 11.7 | | |
| | | For $PWM_FREQ[1,0] = 10$ | | 5.8 | | |
| | | For $PWM_FREQ[1,0] = 11$ | | 2.9 | | |
| | PWM duty cycle range | Limited by $ISINK$ rise / fall time for $PWM_FREQ[1:0]$ other than 2'b11 setting | 0% | | 99.9% | |
| | $ISINK$ rise / fall time | $V_{(ISINK)} \geq 0.6V$ for $2mA \leq ISINK \leq 30mA$ | | 400 | | ns |

6.6 Timing Requirements

| | | MIN | MAX | UNIT |
|--------------|--|------|-----|------|
| f_{MAX} | Clock frequency | | 400 | kHz |
| $t_{(HIGH)}$ | Clock high time | 600 | | ns |
| $t_{(LOW)}$ | Clock low time | 1300 | | ns |
| t_r | DATA and CLK rise time | | 300 | ns |
| t_f | DATA and CLK fall time | | 300 | ns |
| $t_{hd;STA}$ | Hold time (repeated) START condition (after this period the first clock pulse is generated) | 600 | | ns |
| $t_{su;STA}$ | Setup time for repeated START condition | 600 | | ns |
| $t_{hd;DAT}$ | Data input hold time | 10 | | ns |
| $t_{su;DAT}$ | Data input setup time | 100 | | ns |
| $t_{su;STO}$ | STOP condition setup time | 600 | | ns |
| t_{BUF} | Bus free time | 1300 | | ns |
| CI | Load capacitance on SDA and SCL (with a 730Ω or smaller pull-up resistor on SDA and SCL pulled up to 1.8V) | | 400 | pF |

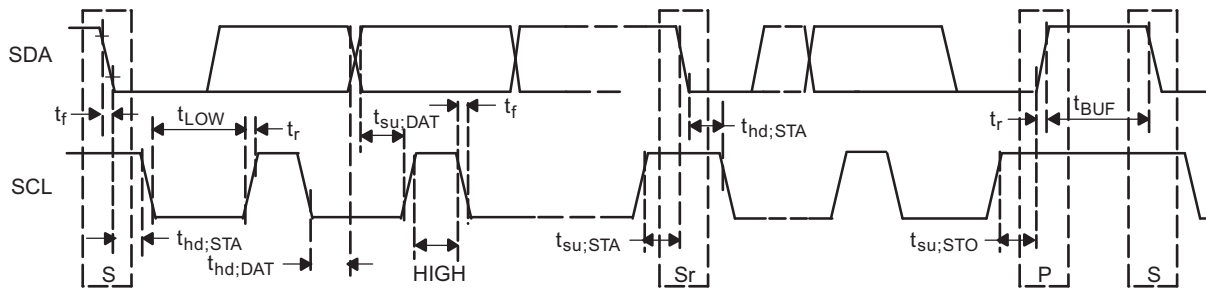


Figure 1. Serial I/f Timing Diagram

6.7 Typical Characteristics

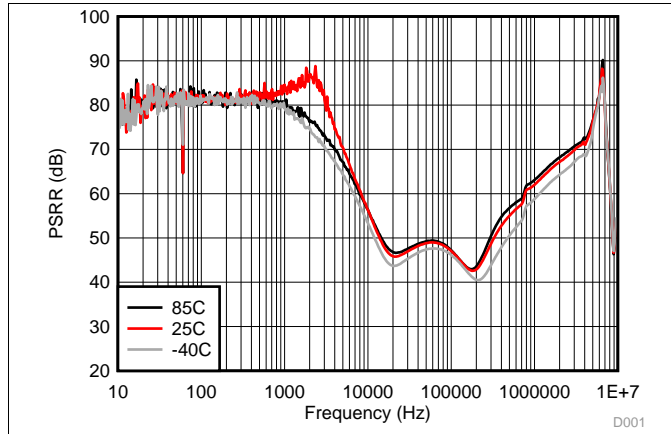


Figure 2. Power Supply Rejection Ratio (PSRR) for LDO1 at 1mA

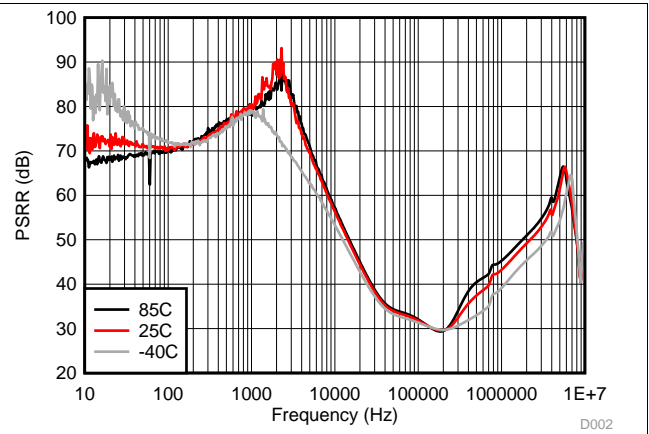


Figure 3. Power Supply Rejection Ratio (PSRR) for LDO1 at 75mA

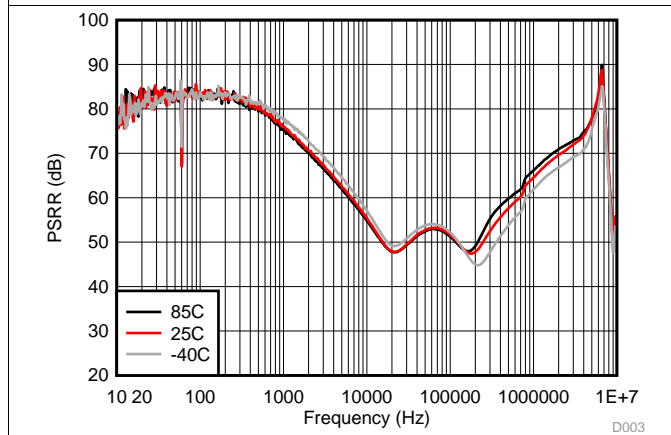


Figure 4. Power Supply Rejection Ratio (PSRR) for LDO2 at 1mA

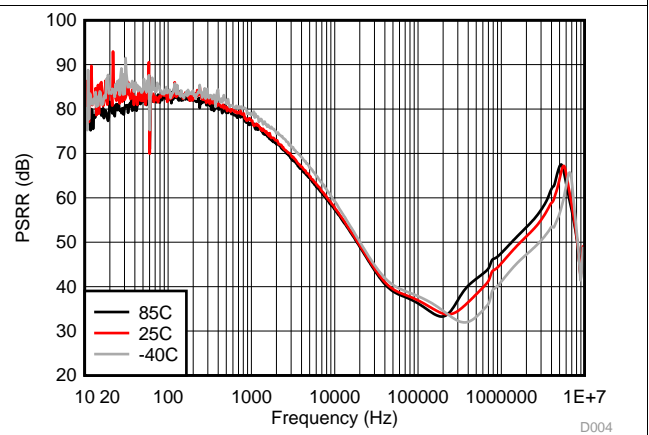


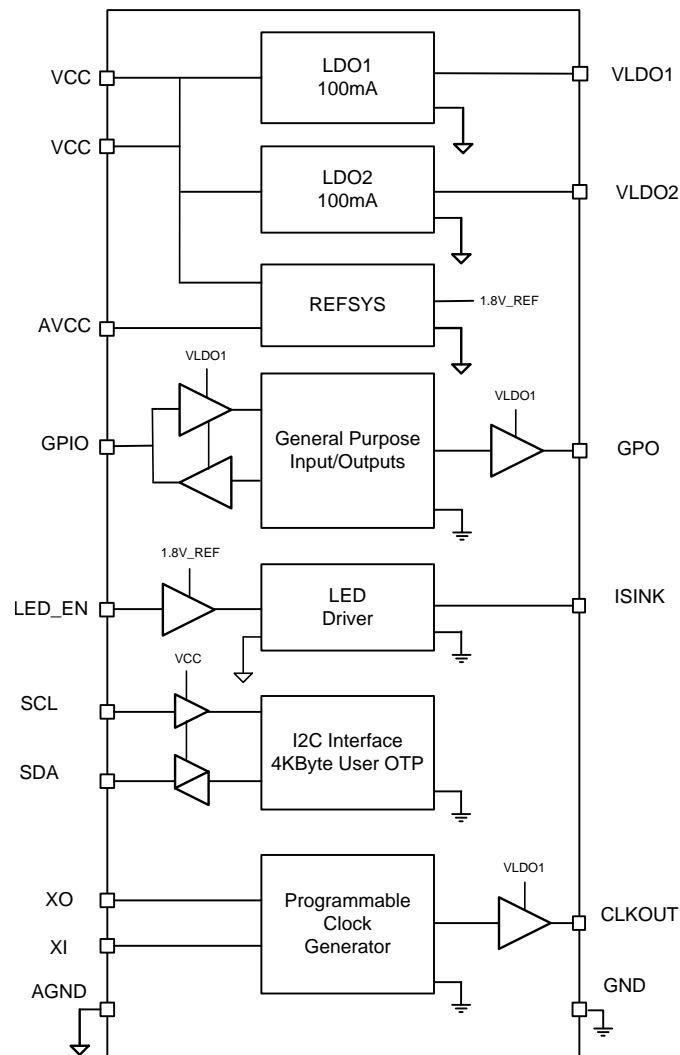
Figure 5. Power Supply Rejection Ratio (PSRR) for LDO2 at 75mA

7 Detailed Description

7.1 Overview

The TPS657095 integrates two LDOs, a PWM-dimmable current sink for driving an LED, one GPIO for controlling an external device and one GPO for controlling an embedded camera module.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 State Diagram

The state diagram below details the basic operation of this device.

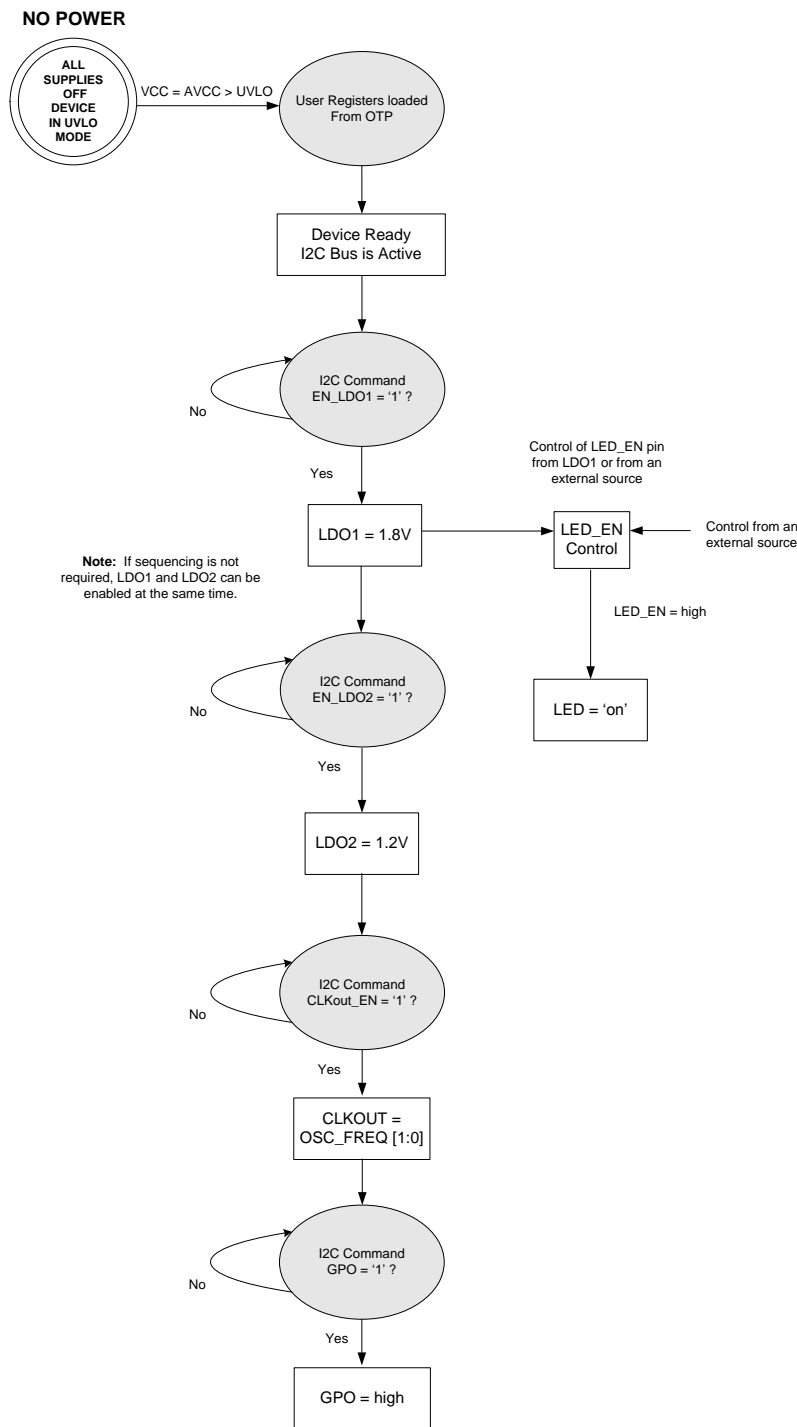


Figure 6. State Diagram

Feature Description (continued)

7.3.2 Power-up Timing

The timing diagram below details the state of the input signals and output voltages in a power-up event.

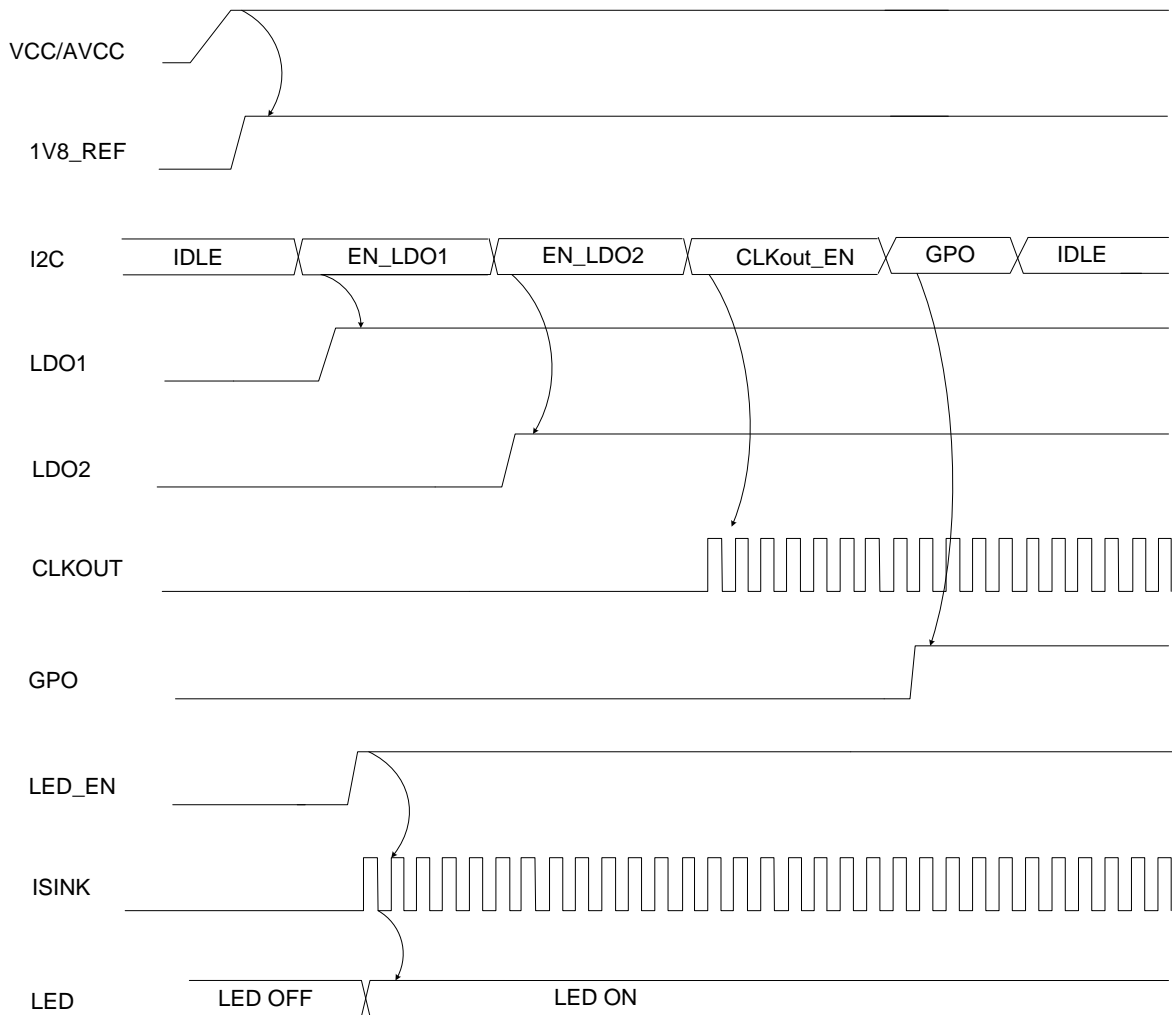


Figure 7. Power-Up Timing

Feature Description (continued)

7.3.3 GPO

The TPS657095 has one general purpose output (GPO) that can be used to control a camera image sensor. Bit 0 of the GPIO_CTRL Register can be used to set the output level and bit 1 of the GPIO_CTRL Register can be used to define whether the output is an open-drain or push-pull output. Internally, the GPO output buffer is connected to LDO1. Therefore, LDO1 has to be enabled in order for the GPO output to operate. In the open-drain configuration, the external pull-up resistor should be pulled up to a voltage that is equal to or less than VCC at all times. Connecting the pull-up resistor to a voltage source that is greater than VCC or present whenever VCC is not present may cause an unwanted leakage path.

7.3.4 GPIO

The TPS657095 has one general purpose input/output (GPIO) that can be used to control an external device when configured as an output. When configured as an input, the GPIO pin serves as a dedicated LDO2 enable. This discrete pin is 'ORed' with the software LDO2 enable. The functionality is shown in the following table.

Table 1. LDO2 Output Control

| GPIO (configured as an input) | EN_LDO2 (bit 1 of the LDO_CTRL REGISTER) | LDO2 OUTPUT |
|-------------------------------|--|-------------|
| 0 | 0 | Off |
| 0 | 1 | On |
| 1 | 0 | On |
| 1 | 1 | On |

The GPIO_CTRL register contains the bits used to configure this GPIO. Bit 3 of the GPIO_CTRL Register can be used to set the output level, bit 4 can be used to configure the GPIO as an input or an output, and bit 5 of the GPIO_CTRL Register can be used to define whether the output is an open-drain or push-pull output. Internally, the GPIO output buffer is connected to LDO1. Therefore, LDO1 has to be enabled in order for the GPIO to operate. In the open-drain configuration, the external pull-up resistor should be pulled up to a voltage that is equal to or less than VCC at all times. Connecting the pull-up resistor to a voltage source that is greater than VCC or present whenever VCC is not present may cause an unwanted leakage path.

7.3.5 LED_EN

The TPS657095 has a pin, LED_EN, which is used to control a privacy LED. The privacy LED can only be turned on or off using the LED_EN pin. No other means to control the privacy LED exists in this device. The LED driver circuit of this device is internally biased by an internal 1.8V reference which is automatically powered once a valid voltage is present on the VCC/AVCC pins of this device. The input leakage current specified in the [Electrical Characteristics](#) section of this datasheet will not be exceeded even if a logic high voltage is applied to this pin while VCC/AVCC are not present.

7.3.6 PWM Dimming

LED_EN serves as the enable for the internal PWM.

- LED_EN = 0: LED is OFF
- LED_EN = 1: LED is ON / internal PWM is enabled

Since the crystal oscillator is needed for the internal PWM dimming, it is automatically enabled based on the status of the LED_EN pin and on the CLKout_EN register bit.

| CLKout_EN | LED_EN | ISINK | CRYSTAL OSCILLATOR ENABLED | CLKout |
|-----------|--------|-------------------|----------------------------|--------|
| 0 | 0 | OFF | OFF | OFF |
| 0 | 1 | ON - internal PWM | ON | OFF |
| 1 | 0 | OFF | ON | ON |
| 1 | 1 | ON - internal PWM | ON | ON |

7.3.7 Crystal Oscillator and CLKOUT

The crystal oscillator is used to provide a clock signal to the camera image sensor via the CLKOUT pin. It is also used to control the internal PWM for dimming the LED. The crystal oscillator is enabled by either the CLKout_EN bit in the PWM_OSC_CNTRL register or by driving the LED_EN pin to a high state.

The CLKOUT buffer is internally supplied by LDO1, hence LDO1 needs to be enabled for proper functionality of the clock output. The CLKOUT buffer is enabled only when bit 2 of the PWM_OSC_CNTRL Register is set to a logic one. If bit 2 of the PWM_OSC_CNTRL register is set to a logic one while LDO1 is disabled, the crystal oscillator will run but the clock output will not be present on the CLKOUT pin. The OSC_FREQ[1:0] bits in the PWM_OSC_CNTRL Register should be set prior to enabling the CLKOUT buffer.

In addition, the crystal oscillator is driving the internal charge pump that generates the programming voltage for the 4kByte OTP memory. For programming the OTP, the oscillator has to be enabled by setting CLKout_EN to a logic '1' at least 10ms before the OTP is written to allow the crystal to stabilize.

The oscillator circuit used does not require external components other than the crystal itself on pins XI and XO. Internally, the oscillator circuit contains two 16pF capacitors connected from XI to GND and from XO to GND. It is designed for an equivalent series resistance of the crystal to be less than 100Ω. Therefore, a crystal must be used with a series resistance of less than this value and no other resistors in series or in parallel to the crystal must be added.

The signal on CLKOUT is delayed from the CLKout_EN bit enabling the output buffer until the oscillator is stable. Once it has stabilized, an additional internal wait time of 131072 clk cycles x 1/24MHz has been added internally to the design before the output is set active. Given the typical start-up time of the crystal oscillator, it is safe to assume the total start-up time which depends on the crystal used including the 131072 cycles of clk delay is less than 10ms.

Table 2. Tested Crystals

| TYPE | NOMINAL FREQUENCY | LOAD CAPACITANCE | EQUIVALENT SERIES RESISTANCE | SUPPLIER |
|-----------------|-------------------|------------------------|------------------------------|----------|
| 8Q-24.000MEEV-T | 24MHz | 8pF (16pF on each pin) | 100Ω maximum | TXC |

7.3.8 LDOs

The low dropout voltage regulators are designed to operate with low value ceramic input and output capacitors. Both LDOs contain a current limit feature which is used at start up to control the voltage ramp time.

LDO1 is enabled by bit 0 of the LDO_CTRL register. LDO2 can be enabled by either bit 1 of the LDO_CTRL register or by the GPIO if configured as an input. Since the input buffer for the GPIO is powered by LDO1, LDO1 must be enabled before the GPIO pin can be used to enable LDO1. In the case of a thermal event, the register enable bits will be cleared with no auto-re-start feature so as to allow the application software to control the power sequencing of the LDOs.

7.3.9 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the complete device at low input voltages.

The supply voltage to the TPS657095 is internally sensed at pin AVCC. When the voltage at AVCC exceeds the UVLO limit, the internal enable signals turns HIGH and allows the device to operate. When the supply voltage drops below the UVLO limit, TPS657095 is forced OFF, all functions are disabled and the LDO output voltage discharge circuitry is forced ON to ramp down the output voltage. However, if the input voltage drops below 2V, the discharge circuit becomes inactive.

7.3.10 Power Up/Power Down Default States

The GPO, GPIO and CLKOUT pins contain internal buffers powered by LDO1. The following table shows their state during a power up (UVLO Rising) and power down (UVLO Falling) event.

Table 3. Power Up/Power Down Events

| CIRCUIT | EVENT | | | |
|---------------|------------------------------|--|-----------------------------|---|
| | VCC > UVLO, LDO1 TURN-OFF | VCC RISING > UVLO, LDO1 IN AN 'OFF' STATE | VCC > UVLO, LDO1 TURN-ON | VCC FALLING < UVLO, LDO1 IN AN 'OFF' STATE |
| GPO | Off ⁽¹⁾ | Off ⁽¹⁾ | Push-Pull, Low Level | Off ⁽¹⁾ |
| GPIO | Off ⁽¹⁾⁽²⁾ | Off ⁽¹⁾⁽²⁾ | Input ⁽³⁾ | Off ⁽¹⁾ |
| Register Bits | no change | OTP Load State | no change | Reset State |
| CLKOUT | Off ⁽¹⁾ | Off ⁽¹⁾ | Low (CLKOUT_EN = low) | Off ⁽¹⁾ |

(1) Output is 'off' as a result of no power supply. The output follows LDO1 to within a diode drop.

(2) The GPIO_STATE bit (bit 3 in the GPIO_CTRL register) is forced to a logic low.

(3) The default setting is configured as an input. This can be modified by using the GPIO_CTRL register.

7.3.11 Output Voltage Discharge for LDO1 and LDO2

The LDOs contain an output capacitor discharge feature which makes sure that the capacitor is discharged to GND when the supply voltage drops below the undervoltage lockout threshold. The discharge function is enabled when voltage is applied at AVCC starting at about 2.1V until the LDOs are enabled.

7.3.12 Power-Good Status Bits for LDO1 and LDO2

Bits PGOOD_LDO1 and PGOOD_LDO2 in register LDO_CTRL are driven by a comparator inside the LDOs to indicate when the output voltage is in regulation. The Bits are set 'high' when the LDO is in regulation. When the LDO is enabled but the voltage is not above the power-good threshold, the bit is set to a 'low' state. The bit is also set to a 'low' state if the LDO is disabled.

7.3.13 Short-Circuit Protection

All outputs are short circuit protected with a maximum output current as defined in the electrical specifications.

7.3.14 Thermal Shutdown

As soon as the junction temperature, T_J , exceeds 150°C (typically) for any of the LDOs, the LDO will go into thermal shutdown. In this case, the LDOs are turned-off. After the temperature has fallen below the threshold, the LDO remains off until it is enabled again by the I²C interface. There is no automatic power-on feature once the thermal event is past.

7.3.15 LED Driver

The TPS657095 contains a LED driver for a current of up to 30mA. ISINK is an open drain current sink that regulates a current in a LED. The anode of the LED needs to be tied to a positive supply voltage e.g., V_{CC} or any other voltage within the limits of the electrical spec of TPS657095, depending on the forward voltage of the LED. The cathode of the LED is connected to ISINK which sets a constant current to GND. ISINK is regulated internally based on the default current set internally. If the LED_EN pin is pulled LOW, the LED driver is disabled and its output ISINK is high resistive. If LED_EN is HIGH, the current sink regulates to the current defined by the setting in the ISINK_CURRENT Register.

The internal PWM generator allows for internal dimming with a frequency of 3kHz, 6kHz, 12kHz or 24kHz. A 10Bit duty cycle register allows to set the duty cycle in a range from 0% to 99.9% using 8Bits PWM resolution and another 2Bits of dithering.

A signal applied at the LED_EN pin is used to synchronously enable and disable the internal PWM signal.

7.3.16 4kByte OTP Memory

The TPS657095 contains 4kBytes of one-time-programmable (OTP) memory to store user data. The memory has a linear address range from 0x0000 to 0x0FFF and uses two Byte addressing as described in the serial interface description. Reading beyond the specified linear address range will result in reading all zeros. Writes to an address space beyond the specified linear address range are inhibited.

The 4kByte OTP memory requires a programming voltage higher than 5V. The program voltage is generated internally by a charge pump which uses the VCC voltage as its input. During programming, Vcc has to be kept at 5V +/-5% (a voltage of 5.25V is recommended) and the internal oscillator has to be enabled 10ms before programming to allow the 24MHz crystal to stabilize. The 24MHz clock is needed for the internal charge pump to generate the programming voltage from Vcc.

As an added security measure, programming the 4kByte OTP memory requires a two byte sequential password to be written to in the PMU register space at address 0x0F. The two bytes must be written back to back with no restriction on the delay between the writes. Any data written at address 0x0F that does not match the password and sequence will disable the ability to program the 4kByte OTP memory.

7.3.16.1 Programming the 4KByte OTP Memory

1. Apply 5V +/-5% to the VCC and AVCC pins.
2. Enable the internal oscillator by driving the LED_EN pin to a high state or setting the CLKout_EN bit to a '1'.
3. Wait at least 10ms for the crystal to stabilize.
3. Using the PMU register I2C address, write the password to the 4K_OTP_PASSWORD register.
4. Using the 4kByte OTP memory I2C address, write the desired value to a specific address using the protocol shown in Figure 6.
5. Exit the programming of the 4KByte OTP memory by over writing the 4K_OTP_PASSWORD register with an incorrect password or by removing power to the device.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The TPS657095 is in a 'Shutdown' mode if the voltage on the AVCC pin is below 1.8V. In this mode, the device will not respond to I2C commands nor will the LED_EN pin be operational.

7.4.2 Operational Mode

The TPS657095 enters an 'Operational' mode mode once a voltage greater than the UVLO limit is present on both the VCC and AVCC pins. In this mode, the I2C is active, the operation of the LED is controllable via the LED_EN pin and the LDOs can be enabled.

NOTE

The voltage on the AVCC and VCC pins should not be left in a state between the Shutdown Mode voltage and the Operational Mode voltage. Keeping the input voltage to the device in this indeterminate state will result in unwanted quiescent current consumption.

7.5 Programming

7.5.1 Serial Interface

The serial interface is compatible with the standard and fast mode I²C specifications, allowing transfers at up to 400kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as VCC remains above the UVLO threshold. The I²C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface. Additional features supported by the I²C compatible interface are:

- multi-byte read/write capability
- clock stretching; specifically needed during OTP write

The 7bit device address for TPS657095 is:

- "100 1000" for the PMU user registers
- "101 1000" for the 4kByte OTP memory

Programming (continued)

For the PMU, at address "100 1000", the device address is followed by the 1Byte register address and 1Byte data (for a write instruction)

For the 4kByte OTP memory, at address "101 1000", the device address is followed by the 1Byte register address [7:0] followed by the second address Byte [15:8] and 1Byte data (for a write instruction) giving a 4kByte linear address range for the memory. Please note that the supply voltage range at pins VCC and AVCC during programming (writing) of the OTP memory is limited to 5V ±5%.

Attempting to read data from register addresses not listed in this section will result in 00h being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS657095 generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS657095 must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge-related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave device TPS657095 must leave the data line high to enable the master to generate the stop condition.

The interface is reset by the internal UVLO signal of TPS657095 or by a STOP condition. If the SCL and SDA signal is not stable at the time the UVLO threshold on pin Vcc is exceeded, the first communication may not be acknowledged and will have to be re-transmitted after a STOP condition.

Upon the application of power on the VCC/AVCC pins, the internal I²C buffers may sequence up in a manner that produces a false START. If a false START is detected, an internal synchronization clock will be enabled until a STOP condition is received. During the time that the internal synchronization clock is active, the device will consume an additional 120µA of current.

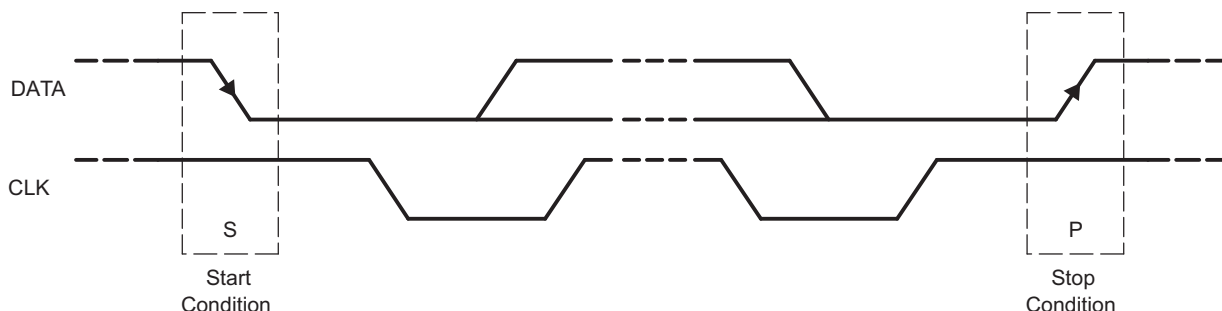
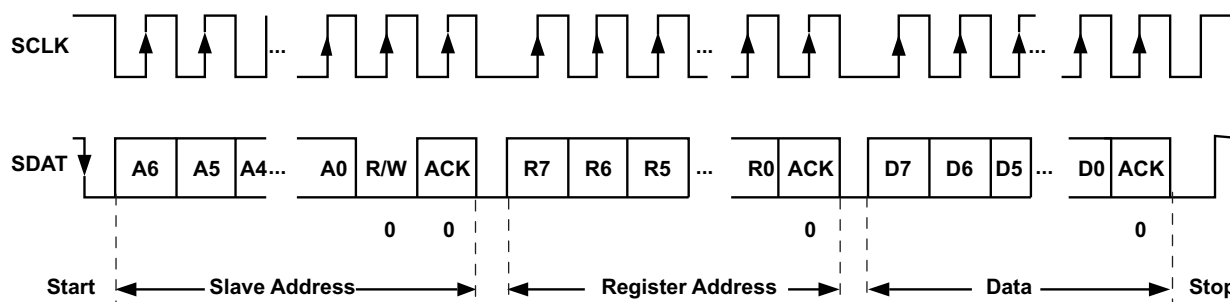


Figure 8. START and STOP Conditions



Note: Slave = This Device

Figure 9. Serial Interface WRITE to TPS657095 User Registers

Programming (continued)

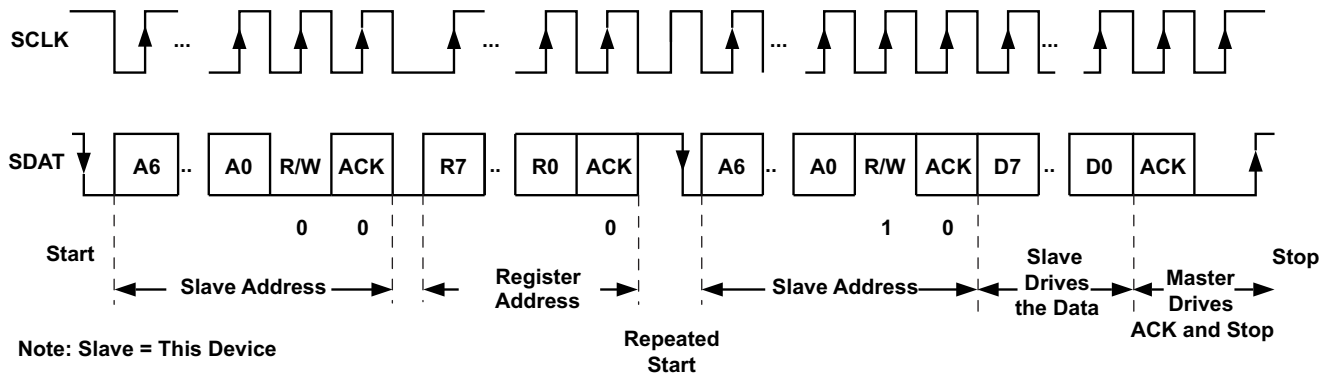


Figure 10. Serial Interface READ from TPS657095 User Registers

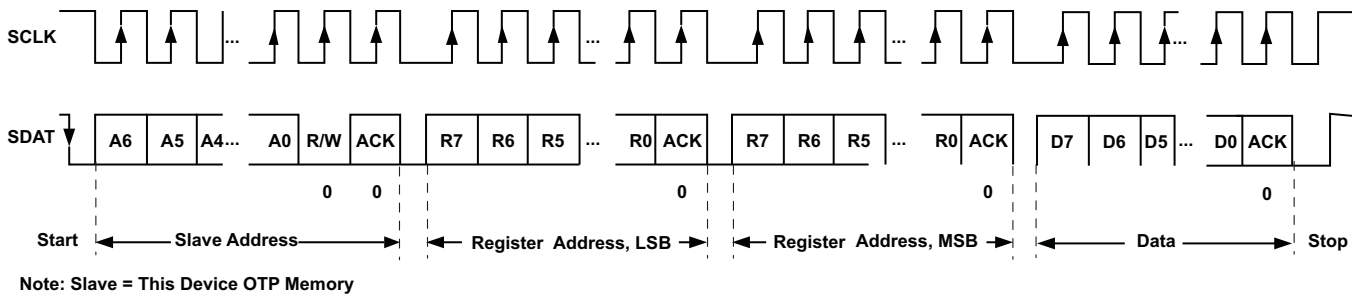


Figure 11. Serial Interface WRITE to TPS657095 OTP Memory

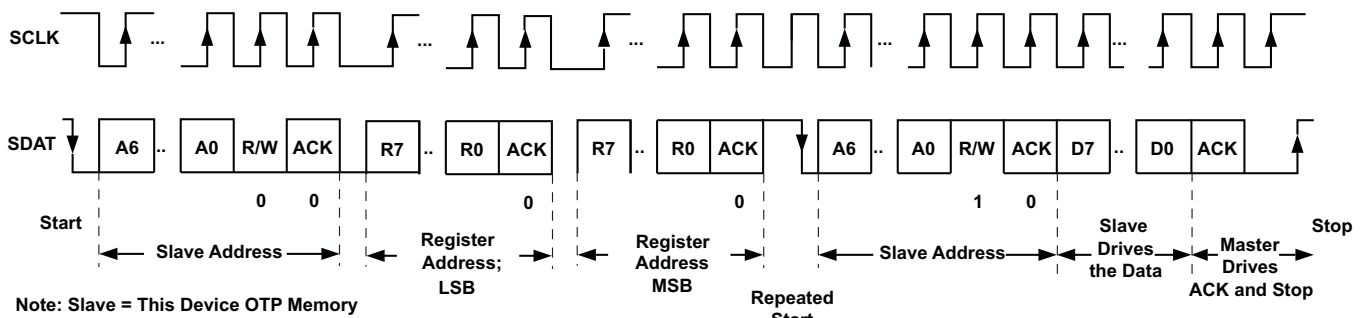


Figure 12. Serial Interface READ from TPS657095 OTP Memory

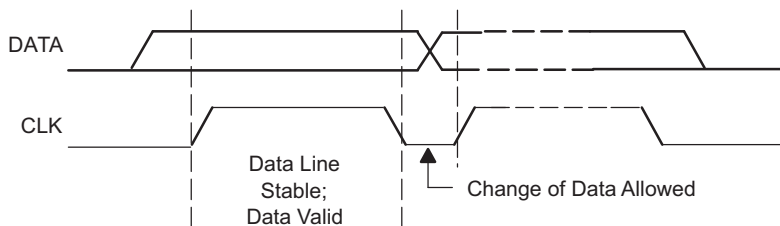


Figure 13. Bit Transfer on the Serial Interface

Programming (continued)

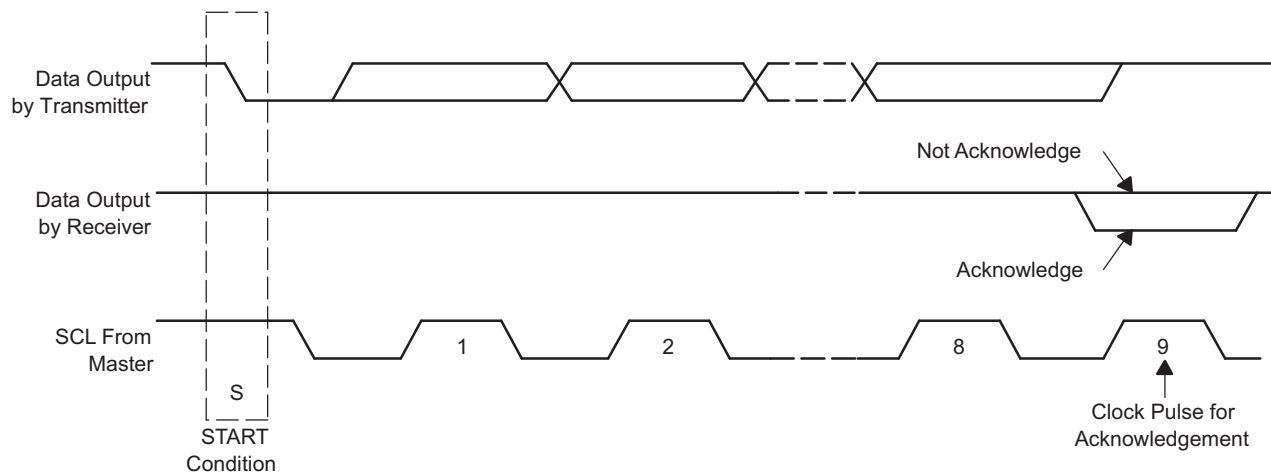


Figure 14. Acknowledge on the I²C Bus

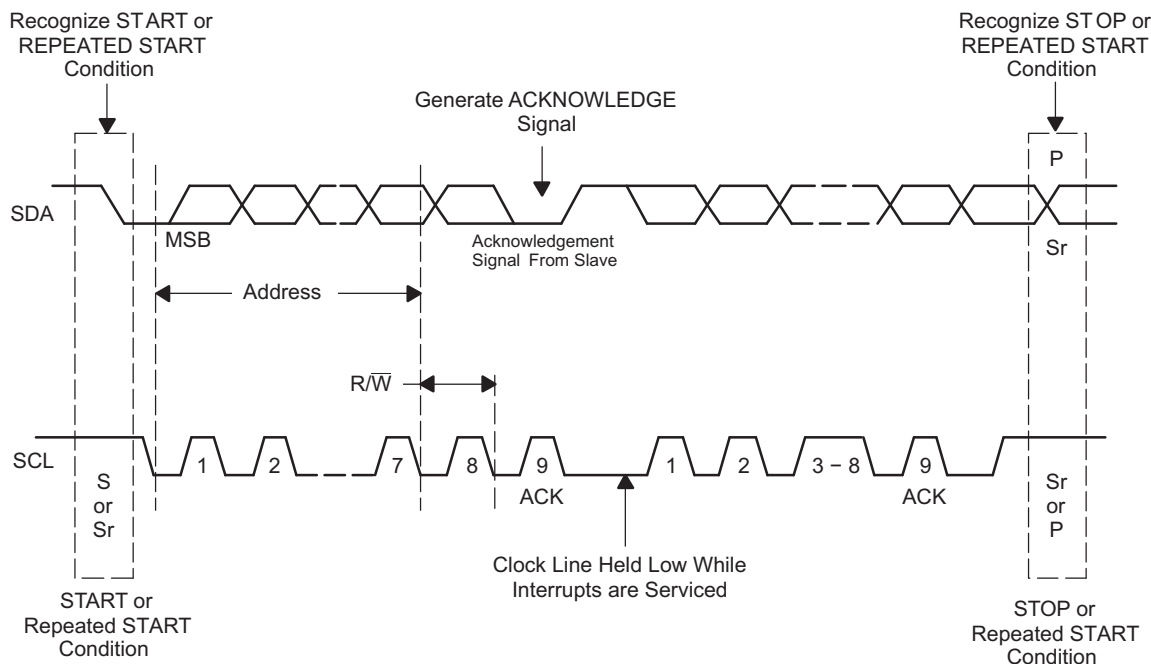


Figure 15. Bus Protocol

7.6 Register Map

7.6.1 DEV_AND_REV_ID Register Address: 00h

Figure 16. DEV_AND_REV_ID Register

| DEV_AND_REV_ID | B7 | B6 | B5 | B4 | B3 | B2 | B1 | BO |
|--------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit name and function | DEV_ID[3] | DEV_ID[2] | DEV_ID[1] | DEV_ID[0] | REV_ID[3] | REV_ID[2] | REV_ID[1] | REV_ID[0] |
| Default | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only;

Table 4. DEV_AND_REV_ID Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|-------------|------|-------|-------------------------------|
| Bit 7:4 | DEV_ID[3:0] | R | 0101 | Device ID: TPS657095 = 0101 |
| Bit 3:0 | REV_ID[3:0] | R | 0100 | Die Revision ID: PG1.0 = 0100 |

7.6.2 OTP_REV Register Address: 01h

Figure 17. OTP_REV Register Address: 01h Register

| OTP_REV | B7 | B6 | B5 | B4 | B3 | B2 | B1 | BO |
|--------------------------|------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| Bit name and function | RSVD | OTP_REV [6] | OTP_REV [5] | OTP_REV [4] | OTP_REV [3] | OTP_REV [2] | OTP_REV [1] | OTP_REV [0] |
| Default | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only;

Table 5. OTP_REV Register Address: 01h Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|--------------|------|---------|--|
| Bit 7 | RSVD | R | 0 | |
| Bit 6:0 | OTP_REV[6:0] | R | 1000000 | Reserved: 100_0000: Production PG1.0 programming |

7.6.3 GPIO_CTRL Register Address: 02h

Figure 18. GPIO_CTRL Register

| GPIO_CTRL | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|-------|-------|-------------|----------|------------|-------|------------|------|
| Bit name and function | SPARE | SPARE | GPIO_driver | GPIO_DIR | GPIO_STATE | SPARE | GPO_driver | GPO |
| Default | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R/W | R/W | R/W | R | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

Table 6. GPIO_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|-------------|------|-------|---|
| Bit 7:6 | SPARE | R | 00 | |
| Bit 5 | GPIO_driver | R/W | 1 | 0 = GPIO is configured as push pull output; internally connected to LDO1 1 = GPIO is configured as open drain output |
| Bit 4 | GPIO_DIR | R/W | 1 | 0 = GPIO is configured as an input and used to enable LDO2 1 = GPIO is configured as an output |
| Bit 3 | GPIO_STATE | R/W | 1 | 0 = actively pulled low 1 = high impedance output if the GPIO_driver bit is configured as an open-drain output / internally pulled up to the LDO1 voltage setting if the GPIO_driver bit is configured as a push-pull output |
| Bit 2 | SPARE | R | 0 | |
| Bit 1 | GPO_driver | R/W | 0 | 0 = GPO is configured as push pull output; internally connected to LDO1 1 = GPO is configured as open drain output |
| Bit 0 | GPO | R/W | 0 | 0 = actively pulled low 1 = high impedance output if the GPO_driver bit is configured as an open-drain output / internally pulled up to the LDO1 voltage setting if the GPO_driver bit is configured as a push-pull output |

7.6.4 PWM_OSC_CNTRL Register Address: 03h

Figure 19. PWM_OSC_CNTRL Register

| OSCILLATOR_CONTROL | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|-------|-------|-------|-------------|-------------|-----------|-------------|-------------|
| Bit name and function | SPARE | SPARE | SPARE | PWM_FREQ[1] | PWM_FREQ[0] | CLKout_EN | OSC_FREQ[1] | OSC_FREQ[0] |
| Default | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

Table 7. PWM_OSC_CNTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|---------------|------|-------|--|
| Bit 7:5 | SPARE | R | 000 | |
| Bit 4:3 | PWM_FREQ[1:0] | R/W | 11 | Frequency divider for internally generated PWM signal: 00 : f(PWM) = 23.5KHz 01 : f(PWM) = 11.7KHz 10 : f(PWM) = 5.8KHz 11 : f(PWM) = 2.9KHz |
| Bit 2 | CLKout_EN | R/W | 0 | 0 = CLKOUT is disabled and the output is held LOW 1 = the crystal oscillator is forced ON; CLKOUT is enabled and is switching with the frequency defined by OSC_FREQ[1..0]; LDO1 needs to be enabled for CLKout being active Please note that the crystal oscillator itself is active once the Bit is set high, independently of the status of LDO1. |
| Bit 1:0 | OSC_FREQ[1:0] | R/W | 00 | Frequency divider for CLKOUT generated from 24MHz crystal 00 : f(CLKOUT) = f(OSC) = 24MHz 01 : f(CLKOUT) = f(OSC) / 2 = 12MHz 10 : f(CLKOUT) = f(OSC) / 4 = 6MHz 11 : f(CLKOUT) = f(OSC) / 8 = 3MHz |

7.6.5 ISINK_CURRENT Register Address: 04h

Figure 20. ISINK_CURRENT Register

| ISINK_CURRENT | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|-------|-------|-------|----------|----------|----------|----------|----------|
| Bit name and function | SPARE | SPARE | SPARE | ISINK[4] | ISINK[3] | ISINK[2] | ISINK[1] | ISINK[0] |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only;

Table 8. ISINK_CURRENT Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|------------|------|-------|--|
| Bit 7:5 | SPARE | R | 000 | |
| Bit 4:0 | ISINK[4:0] | R | 01000 | ISINK dc current setting TPS657095: Factory programmed to 5'b01000 (10mA) |

7.6.6 LDO_CTRL Register Address: 05h
Figure 21. LDO_CTRL Register

| LDO_CTRL | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|-------|-------|---------------|---------------|-------|-------|---------|---------|
| Bit name and function | SPARE | SPARE | PGOOD_LDO2 | PGOOD_LDO1 | SPARE | SPARE | EN_LDO2 | EN_LDO1 |
| Default | 0 | 0 | - | - | 0 | 0 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | PGOOD of LDO2 | PGOOD of LDO1 | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R | R | R | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

Table 9. LDO_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|------------|------|-------|--|
| Bit 7:6 | SPARE | R | 00 | |
| Bit 5 | PGOOD LDO2 | R | – | Power good status Bit for LDO2 (power good threshold relative to target value: 95% rising and 90% falling) 0 = the output voltage of LDO2 is below the power good threshold or LDO2 is disabled; default value as LDO2 is disabled by default 1 = the output voltage of LDO2 is above the power good threshold |
| Bit 4 | PGOOD LDO1 | R | – | Power good status Bit for LDO1 (power good threshold relative to target value: 95% rising and 90% falling) 0 = the output voltage of LDO1 is below the power good threshold or LDO1 is disabled; default value as LDO1 is disabled by default 1 = the output voltage of LDO1 is above the power good threshold |
| Bit 3 | NC: | R | 0 | |
| Bit 2 | SPARE | R | 0 | |
| Bit 1 | EN_LDO2 | R/W | 0 | 0 = LDO2 is disabled (Default: TPS657095) 1 = LDO2 is enabled |
| Bit 0 | EN_LDO1 | R/W | 0 | 0 = LDO1 is disabled (Default: TPS657095) 1 = LDO1 is enabled |

7.6.7 LDO1_VCTRL Register Address: 06h
Figure 22. LDO1_VCTRL Register

| LDO1_VCTRL | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|-------|-------|---------|---------|---------|---------|---------|---------|
| Bit name and function | SPARE | SPARE | LDO1[5] | LDO1[4] | LDO1[3] | LDO1[2] | LDO1[1] | LDO1[0] |
| Default | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

Table 10. LDO1_VCTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|-----------|------|--------|---|
| Bit 7:6 | SPARE | R | 00 | |
| Bit 5:0 | LDO1[5:0] | R/W | 100100 | Output voltage setting for LDO1 ⁽¹⁾⁽²⁾ |

- (1) A Voltage change during operation must not exceed 8% of the value set in the register for each I2C write access as this may trigger the internal power good comparator and will trigger the Reset of the device. This limitation is only for a voltage step to higher voltages. There is no limitation for programming lower voltages by I2C.
- (2) The output voltage setting cannot be changed if the LOCK_BIT in the OTP_REV_LOCK_BIT register is set to a logic '1'.

7.6.8 LDO2_VCTRL Register Address: 07h
Figure 23. LDO2_VCTRL Register

| LDO2_VCTRL | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|-------|-------|---------|---------|---------|---------|---------|---------|
| Bit name and function | SPARE | SPARE | LDO2[5] | LDO2[4] | LDO2[3] | LDO2[2] | LDO2[1] | LDO2[0] |
| Default | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

Table 11. LDO2_VCTRL Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|-----------|------|--------|---|
| Bit 7:6 | SPARE | R | 00 | |
| Bit 5:0 | LDO2[5:0] | R/W | 010000 | Output voltage setting for LDO2 ⁽¹⁾⁽²⁾ |

- (1) A Voltage change during operation must not exceed 8% of the value set in the register for each I2C write access as this may trigger the internal power good comparator and will trigger the Reset of the device. This limitation is only for a voltage step to higher voltages. There is no limitation for programming lower voltages by I2C.
- (2) The output voltage setting cannot be changed if the LOCK_BIT in the OTP_REV_LOCK_BIT register is set to a logic '1'.

| | OUTPUT VOLTAGE [V] | B5 | B4 | B3 | B2 | B1 | B0 |
|---|--------------------|----|----|----|----|----|----|
| 0 | 0.800 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0.825 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0.850 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0.875 | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | 0.900 | 0 | 0 | 0 | 1 | 0 | 0 |
| 5 | 0.925 | 0 | 0 | 0 | 1 | 0 | 1 |

| | OUTPUT VOLTAGE [V] | B5 | B4 | B3 | B2 | B1 | B0 |
|----|--------------------|----|----|----|----|----|----|
| 6 | 0.950 | 0 | 0 | 0 | 1 | 1 | 0 |
| 7 | 0.975 | 0 | 0 | 0 | 1 | 1 | 1 |
| 8 | 1.000 | 0 | 0 | 1 | 0 | 0 | 0 |
| 9 | 1.025 | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | 1.050 | 0 | 0 | 1 | 0 | 1 | 0 |
| 11 | 1.075 | 0 | 0 | 1 | 0 | 1 | 1 |
| 12 | 1.100 | 0 | 0 | 1 | 1 | 0 | 0 |
| 13 | 1.125 | 0 | 0 | 1 | 1 | 0 | 1 |
| 14 | 1.150 | 0 | 0 | 1 | 1 | 1 | 0 |
| 15 | 1.175 | 0 | 0 | 1 | 1 | 1 | 1 |
| 16 | 1.200 | 0 | 1 | 0 | 0 | 0 | 0 |
| 17 | 1.225 | 0 | 1 | 0 | 0 | 0 | 1 |
| 18 | 1.250 | 0 | 1 | 0 | 0 | 1 | 0 |
| 19 | 1.275 | 0 | 1 | 0 | 0 | 1 | 1 |
| 20 | 1.300 | 0 | 1 | 0 | 1 | 0 | 0 |
| 21 | 1.325 | 0 | 1 | 0 | 1 | 0 | 1 |
| 22 | 1.350 | 0 | 1 | 0 | 1 | 1 | 0 |
| 23 | 1.375 | 0 | 1 | 0 | 1 | 1 | 1 |
| 24 | 1.400 | 0 | 1 | 1 | 0 | 0 | 0 |
| 25 | 1.425 | 0 | 1 | 1 | 0 | 0 | 1 |
| 26 | 1.450 | 0 | 1 | 1 | 0 | 1 | 0 |
| 27 | 1.475 | 0 | 1 | 1 | 0 | 1 | 1 |
| 28 | 1.500 | 0 | 1 | 1 | 1 | 0 | 0 |
| 29 | 1.525 | 0 | 1 | 1 | 1 | 0 | 1 |
| 30 | 1.550 | 0 | 1 | 1 | 1 | 1 | 0 |
| 31 | 1.575 | 0 | 1 | 1 | 1 | 1 | 1 |
| 32 | 1.600 | 1 | 0 | 0 | 0 | 0 | 0 |
| 33 | 1.650 | 1 | 0 | 0 | 0 | 0 | 1 |
| 34 | 1.700 | 1 | 0 | 0 | 0 | 1 | 0 |
| 35 | 1.750 | 1 | 0 | 0 | 0 | 1 | 1 |
| 36 | 1.800 | 1 | 0 | 0 | 1 | 0 | 0 |
| 37 | 1.850 | 1 | 0 | 0 | 1 | 0 | 1 |
| 38 | 1.900 | 1 | 0 | 0 | 1 | 1 | 0 |
| 39 | 1.950 | 1 | 0 | 0 | 1 | 1 | 1 |
| 40 | 2.000 | 1 | 0 | 1 | 0 | 0 | 0 |
| 41 | 2.050 | 1 | 0 | 1 | 0 | 0 | 1 |
| 42 | 2.100 | 1 | 0 | 1 | 0 | 1 | 0 |
| 43 | 2.150 | 1 | 0 | 1 | 0 | 1 | 1 |
| 44 | 2.200 | 1 | 0 | 1 | 1 | 0 | 0 |
| 45 | 2.250 | 1 | 0 | 1 | 1 | 0 | 1 |
| 46 | 2.300 | 1 | 0 | 1 | 1 | 1 | 0 |
| 47 | 2.350 | 1 | 0 | 1 | 1 | 1 | 1 |
| 48 | 2.400 | 1 | 1 | 0 | 0 | 0 | 0 |
| 49 | 2.450 | 1 | 1 | 0 | 0 | 0 | 1 |
| 50 | 2.500 | 1 | 1 | 0 | 0 | 1 | 0 |
| 51 | 2.550 | 1 | 1 | 0 | 0 | 1 | 1 |
| 52 | 2.600 | 1 | 1 | 0 | 1 | 0 | 0 |
| 53 | 2.650 | 1 | 1 | 0 | 1 | 0 | 1 |
| 54 | 2.700 | 1 | 1 | 0 | 1 | 1 | 0 |

| | OUTPUT VOLTAGE [V] | B5 | B4 | B3 | B2 | B1 | B0 |
|----|--------------------|----|----|----|----|----|----|
| 55 | 2.750 | 1 | 1 | 0 | 1 | 1 | 1 |
| 56 | 2.800 | 1 | 1 | 1 | 0 | 0 | 0 |
| 57 | 2.850 | 1 | 1 | 1 | 0 | 0 | 1 |
| 58 | 2.900 | 1 | 1 | 1 | 0 | 1 | 0 |
| 59 | 2.950 | 1 | 1 | 1 | 0 | 1 | 1 |
| 60 | 3.000 | 1 | 1 | 1 | 1 | 0 | 0 |
| 61 | 3.100 | 1 | 1 | 1 | 1 | 0 | 1 |
| 62 | 3.200 | 1 | 1 | 1 | 1 | 1 | 0 |
| 63 | 3.300 | 1 | 1 | 1 | 1 | 1 | 1 |

7.6.9 PWM_DUTY_THR_L Register Address: 08h

Figure 24. PWM_DUTY_THR_L Register

| PWM_DUTY_THR_L | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| Bit name and function | PWM_DC_TH[7] | PWM_DC_TH[6] | PWM_DC_TH[5] | PWM_DC_TH[4] | PWM_DC_TH[3] | PWM_DC_TH[2] | PWM_DC_TH[1] | PWM_DC_TH[0] |
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only;

Table 12. PWM_DUTY_THR_L Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|----------------|------|----------|---|
| Bit 7:0 | PWM_DC_TH[7:0] | R | 11111111 | Lower 8 bits of PWM duty cycle threshold for internally generated PWM on ISINK ⁽¹⁾ |

(1) The contents of the PWM_DUTY_THR_L register is factory programmed and read only.

7.6.10 PWM_DUTY_THR_H Register Address: 09h
Figure 25. PWM_DUTY_THR_H Register

| PWM_DUTY_THR_H | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|------|------|------|------|------|------|--------------|------------------|
| Bit name and function | | | | | | | PWM_DC_TH[9] | PWM_DC_T H[8] |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default set by: | OTP | OTP | OTP | OTP | OTP | OTP | OTP | OTP |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R | R | R | R | R |

LEGEND: R/W = Read/Write; R = Read only;

Table 13. PWM_DUTY_THR_H Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|----------------|------|----------|---|
| Bit 7:0 | PWM_DC_TH[7:0] | R | 00000000 | Higher 2 Bits of PWM duty cycle threshold for internally generated PWM on ISINK |
| | PWM_DC_TH[9:0] | R | 00000000 | 000h = 0% duty cycle 3FFh = 99.9% duty cycle |

(1) The contents of the PWM_DUTY_THR_H register is factory programmed and read only.

7.6.11 RESERVED Register Address: 0Ah

Reserved

7.6.12 PWM_DUTY_L Register Address: 0Bh

Figure 26. PWM_DUTY_L Register

| PWM_DUTY_L | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-------------------|
| Bit name and function | PWM_DC[7] | PWM_DC[6] | PWM_DC[5] | PWM_DC[4] | PWM_DC[3] | PWM_DC[2] | PWM_DC[1] | PWM_DC[0]; LSB |
| Default | see (1) | see (1) | see (1) | see (1) | see (1) | see (1) | see (1) | see (1) |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

- (1) The default value in the register is 0x00. Any value written to the PWM_DUTY_1 and PWM_DUTY_2 registers is internally compared to PWM_DUTY_THR_L and PWM_DUTY_THR_H. A value below <PWM_DUTY_THR_H><PWM_DUTY_THR_L> is latched to the register but is internally ignored for setting the duty cycle and will result in a PWM signal with the minimum duty cycle defined by <PWM_DUTY_THR_H><PWM_DUTY_THR_L>

Table 14. PWM_DUTY_L Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|-------------|------|----------|---|
| Bit 7:0 | PWM_DC[7:0] | R/W | 00000000 | Lower 8 bits for duty cycle of internally generated PWM on ISINK ⁽¹⁾⁽²⁾⁽³⁾ |

- (1) The default value in the register is 0x00. Any value written to the PWM_DUTY_1 and PWM_DUTY_2 registers is internally compared to PWM_DUTY_THR_L and PWM_DUTY_THR_H. A value below <PWM_DUTY_THR_H><PWM_DUTY_THR_L> is latched to the register but is internally ignored for setting the duty cycle and will result in a PWM signal with the minimum duty cycle defined by <PWM_DUTY_THR_H><PWM_DUTY_THR_L>
- (2) A new value in PWM_DUTY_L and PWM_DUTY_H is internally valid after writing to PWM_DUTY_H AND the dithering cycle is completed, therefore PWM_DUTY_L should be written to first.
- (3) A Duty Cycle of 1% or less may not be visible when the PWM frequency is 3KHz. At 24KHz, a Duty Cycle of 8% or less may not be visible.

7.6.13 PWM_DUTY_H Register Address: 0Ch

Figure 27. PWM_DUTY_H Register

| PWM_DUTY_H | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|------|------|------|------|------|------|----------------|-----------|
| Bit name and function | | | | | | | PWM_DC[9]; MSB | PWM_DC[8] |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | see Note1 | see Note1 |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R | R | R | R | R | R | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

Table 15. PWM_DUTY_H Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|-------------|------|--------|--|
| Bit 7:2 | | R | 000000 | |
| Bit 1:0 | PWM_DC[9:8] | R/W | 00 | Higher 2 Bits for duty cycle of internally generated PWM on ISINK ⁽¹⁾⁽²⁾⁽³⁾ |
| | PWM_DC[9:0] | | | 00h = 0% duty cycle 3FFh = 99.9% duty cycle |

- (1) The default value in the register is 0x00. Any value written to the PWM_DUTY_L and PWM_DUTY_H registers is internally compared to PWM_DUTY_THR_L and PWM_DUTY_THR_H. A value below <PWM_DUTY_THR_H><PWM_DUTY_THR_L> is latched to the register but is internally ignored for setting the duty cycle and will result in a PWM signal with the minimum duty cycle defined by <PWM_DUTY_THR_H><PWM_DUTY_THR_L>
- (2) A new value in PWM_DUTY_L and PWM_DUTY_H is internally valid after writing to PWM_DUTY_H AND the dithering cycle is completed, therefore PWM_DUTY_L should be written to first.
- (3) A Duty Cycle of 1% or less may not be visible when the PWM frequency is 3KHz. At 24KHz, a Duty Cycle of 8% or less may not be visible.

7.6.14 RESERVED Register Address: 0Dh

Reserved

7.6.15 SPARE Register Address: 0Eh
Figure 28. SPARE Register

| SPARE | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|--------------------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit name and function | SPARE[7] | SPARE[6] | SPARE[5] | SPARE[4] | SPARE[3] | SPARE[2] | SPARE[1] | SPARE[0] |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

LEGEND: R/W = Read/Write; R = Read only;

Table 16. SPARE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|------------|------|----------|---------------------|
| Bit 7:0 | SPARE[7:0] | R/W | 00000000 | Spare Register Bits |

7.6.16 4K_OTP_PASSWORD Register Address: 0Fh
Figure 29. 4K_OTP_PASSWORD Register

| 4K_OTP_PASSWORD | B7 | B6 | B5 | B4 | B3 | B2 | B1 | BO |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Bit name and function | PW[7] | PW[6] | PW[5] | PW[4] | PW[3] | PW[2] | PW[1] | PW[0] |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Default value loaded by: | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO | UVLO |
| Read/write | W | W | W | W | W | W | W | W |

LEGEND: R/W = Read/Write; R = Read only;

Table 17. 4K_OTP_PASSWORD Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---------|---------|------|----------|--|
| Bit 7:0 | PW[7:0] | W | 00000000 | User 4K OTP Password Register: The correct password enables the qualifier for writing to the User 4K OTP. The password is Implemented as a 2 Byte sequential write which must be performed back to back with no restriction on the delay between the writes. If the correct password is not set, writing to the User 4K OTP memory is disabled. |

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The target application for the TPS657095 device is powering an embedded camera module.

8.2 Typical Application

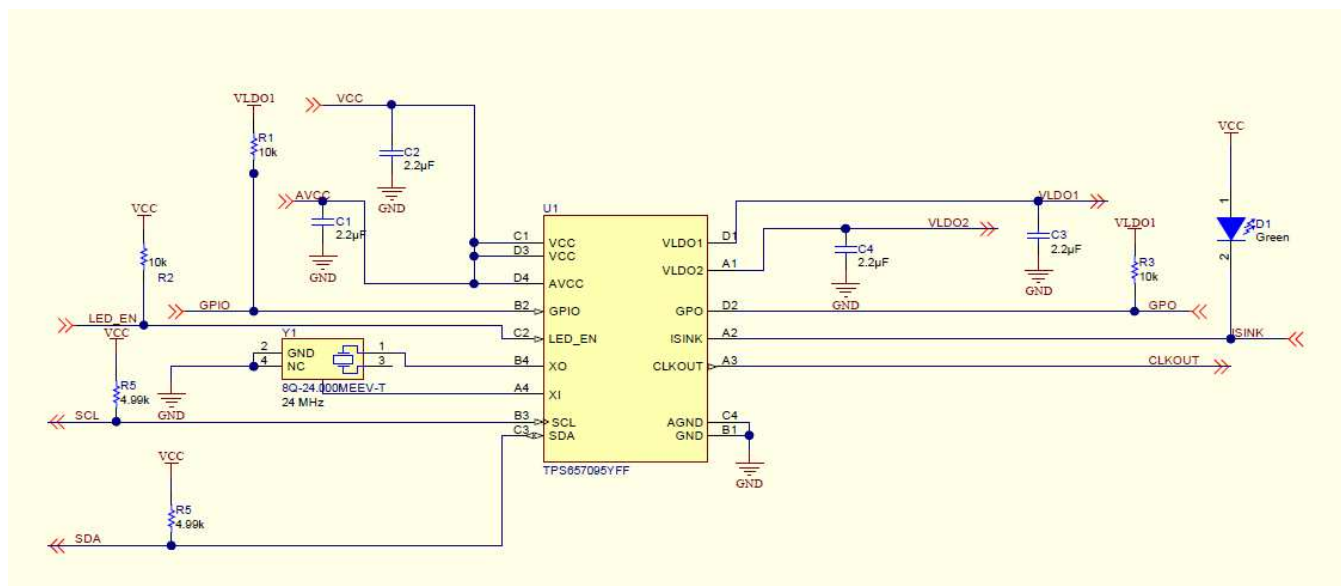


Figure 30. Application Schematic

8.2.1 Design Requirements

Table 18. Design Parameters

| DESIGN PARAMETER | VALUE |
|-----------------------|-----------------------|
| Typical Input Voltage | 5V |
| LDO1 Output Voltage | 1.8V (off by default) |
| LDO2 Output Voltage | 1.2V (off by default) |

8.2.2 Detailed Design Procedure

8.2.2.1 Output Capacitor Selection

The control loop of the LDOs is internally compensated such that they operate with small ceramic output capacitors of 2.2 μ F.

8.2.2.2 Input Capacitor Selection

A low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits. The LDOs need a ceramic input capacitor with a minimum capacitance of 1.0 μ F. The input capacitor can be increased without any limit for better input voltage filtering.

Table 19. Tested Capacitors

| TYPE | VALUE | VOLTAGE RATING | SIZE | SUPPLIER | MATERIAL |
|--------------------|-------------|----------------|------|----------|-------------|
| GRM155R60J225ME15D | 2.2 μ F | 6.3 V | 0402 | Murata | Ceramic X5R |
| GRM185R60J225 | 2.2 μ F | 6.3 V | 0603 | Murata | Ceramic X5R |
| GRM185R60J105K | 1 μ F | 6.3 V | 0603 | Murata | Ceramic X5R |

8.2.3 Application Curves

The graphs below were taken using the TPS657095EVM with the passive components as listed below:

- $C_{IN}(VCC) = GRM185R60J105K$ (1 μ F / 6.3V)
- $C_{OUT}(LDO1) = C_{OUT}(LDO2) = GRM185R60J225$ (2.2 μ F / 6.3 V)
- $V_{CC} = 5$ V unless otherwise noted

Table 20. Table of Graphs

| DESCRIPTION | | FIGURE |
|---|---|---------------------------|
| Line Transient Response LDO1 | $V_{CC} = 3.6V$ to 5V to 3.6V; $I_{OUT} = 75mA$; $V_{OUT} = 1.8V$ | Figure 31 |
| Line Transient Response LDO2 | $V_{CC} = 3.6V$ to 5V to 3.6V; $I_{OUT} = 75mA$; $V_{OUT} = 2.8V$ | Figure 32 |
| Load Transient Response LDO1 | $V_{CC} = 5V$; $I_{OUT} = 7.5mA$ to 68mA to 7.5mA; $V_{OUT} = 1.8V$ | Figure 33 |
| Load Transient Response LDO2 | $V_{CC} = 5V$; $I_{OUT} = 7.5mA$ to 68mA to 7.5mA; $V_{OUT} = 2.8V$ | Figure 34 |
| LDO1 and LDO2 Start-up Timing | $V_{CC} = 5V$; $I_{OUT} = 0mA$ | Figure 35 |
| LDO1 and LDO2 Start-up Timing | $V_{CC} = 5V$; $I_{OUT} = 75mA$ | Figure 36 |
| Duty Cycle on CLKout vs Programmed Frequency | $V_{CC} = 5V$; $f_{(crystal)} = 24MHz$; $V_{LDO1} = 1.8V$ | Figure 37 |
| Period Jitter on CLKout vs Temperature and Output Frequency | $V_{CC} = 5V$; $f_{(crystal)} = 24MHz$; $V_{LDO1} = 1.8V$ | Figure 38 |

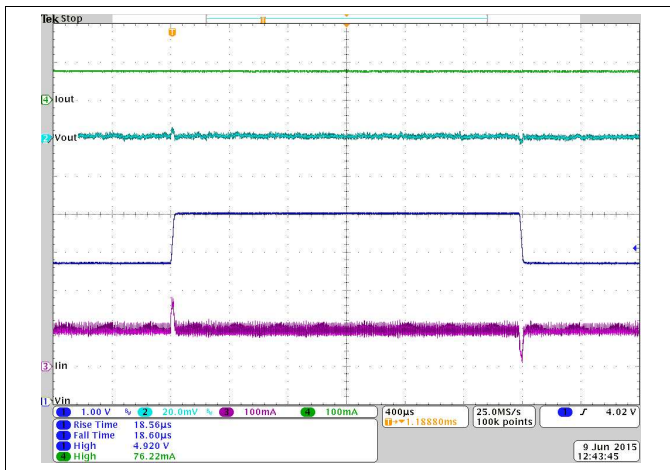


Figure 31. Line Transient Response LDO1

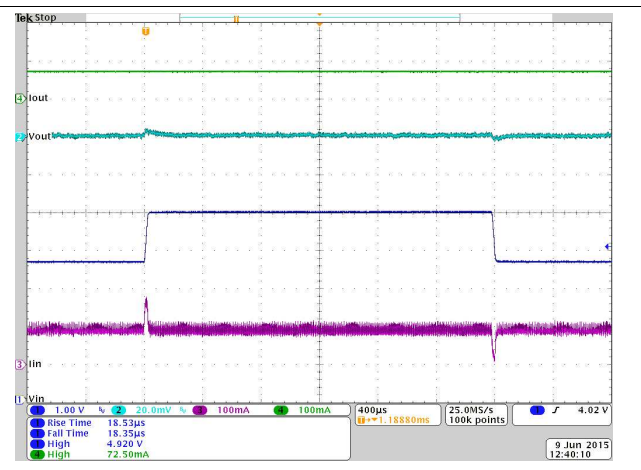


Figure 32. Line Transient Response LDO2

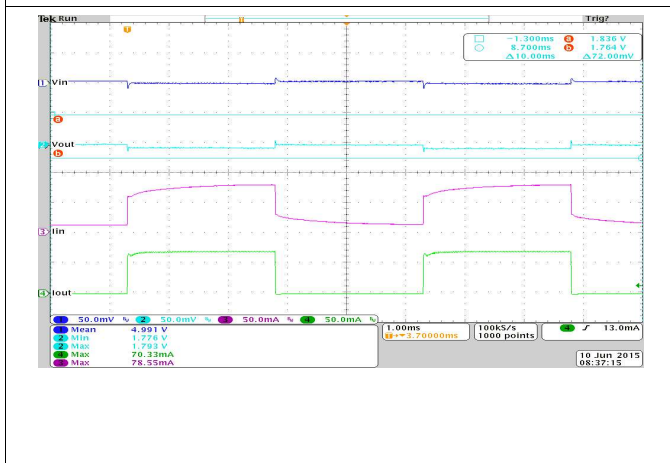


Figure 33. Load Transient Response LDO1

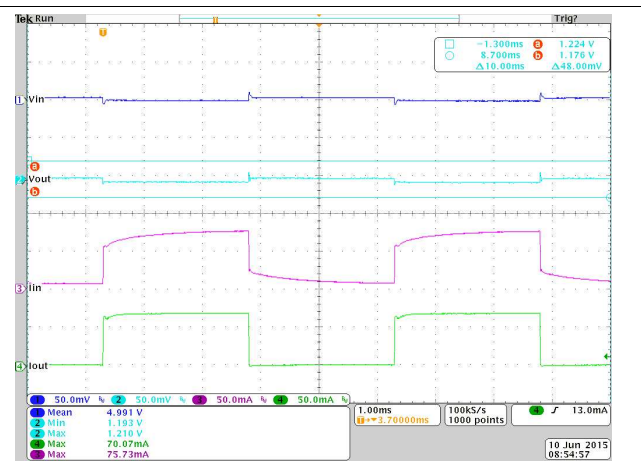


Figure 34. Load Transient Response LDO2

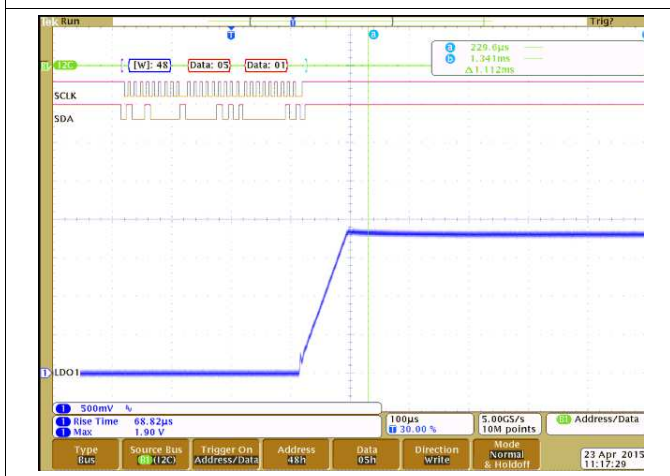


Figure 35. LDO1 Start-up Timing

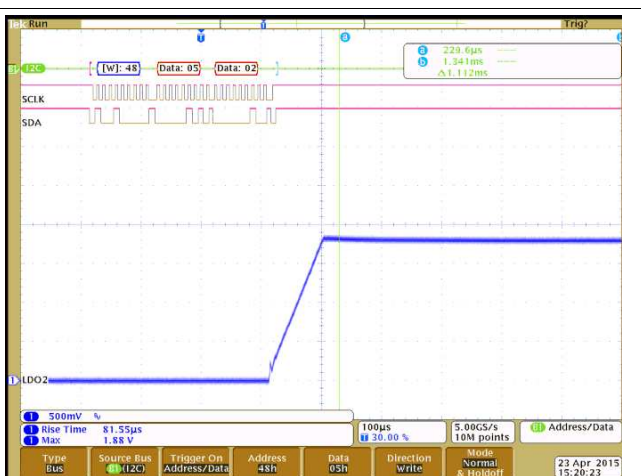
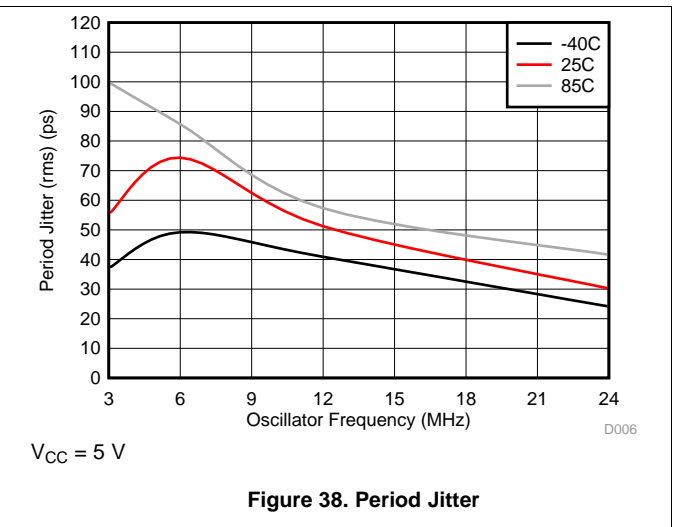
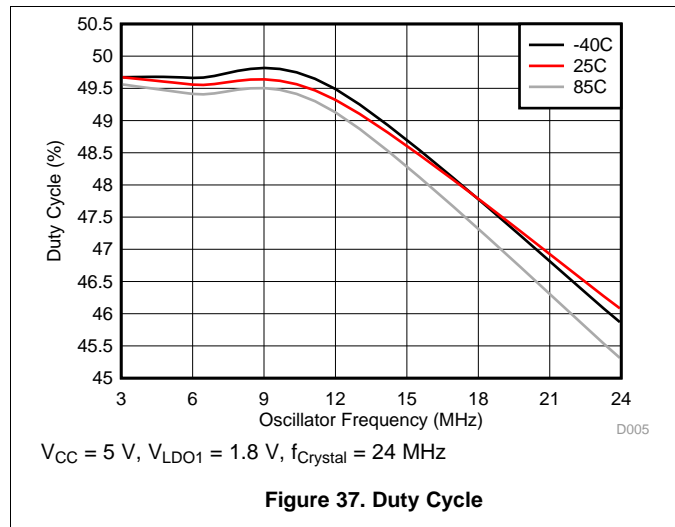


Figure 36. LDO2 Start-up Timing



9 Power Supply Recommendations

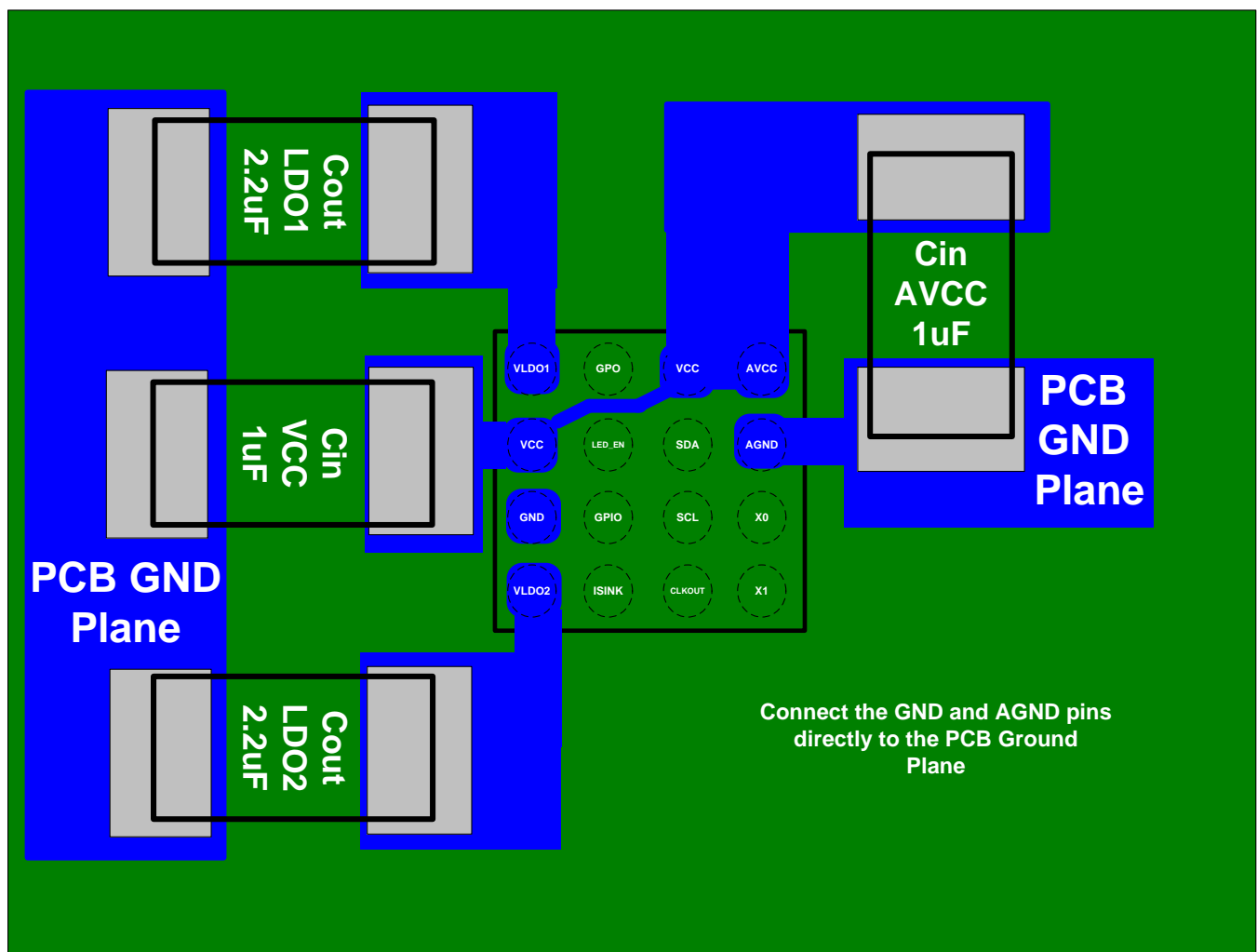
The TPS657095 devices are designed to operate from an input voltage range of 3.7V to 6V. The input supply should be well regulated.

10 Layout

10.1 Layout Guidelines

- The VCC and AVCC terminals should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 1uF with a X5R or X7R dielectric.
- The optimum placement is closest to the AVCC terminal and the AGND terminal.
- The AGND and GND terminals should be tied to the pcb ground plane at the terminal of the IC

10.2 Layout Example



11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E, NanoFree are trademarks of Texas Instruments.

I²C is a trademark of NXP B.V Corporation.

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Summary

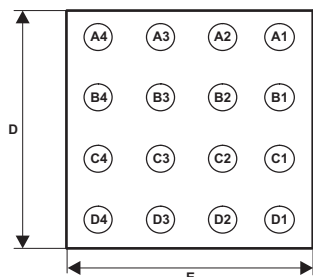


Figure 39. Chip Scale Package (Bottom View)

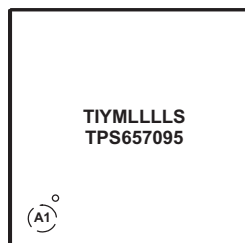


Figure 40. Chip Scale Package (Top View)

Code:

- YM — Year Month date code
- LLLL — Lot trace code
- S — Assembly site code

12.2 Chip Scale Package Dimensions

The TPS657095 device is available in a 16-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

- D = ca. 1700 ±25 μm
- E = ca. 1700 ±25 μm

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS657095YFFR | Active | Production | DSBGA (YFF) 16 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 657095 |
| TPS657095YFFR.B | Active | Production | DSBGA (YFF) 16 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 657095 |
| TPS657095YFFT | Active | Production | DSBGA (YFF) 16 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 657095 |
| TPS657095YFFT.B | Active | Production | DSBGA (YFF) 16 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TPS 657095 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

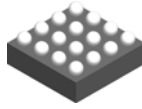
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS657095YFFR | DSBGA | YFF | 16 | 3000 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |
| TPS657095YFFT | DSBGA | YFF | 16 | 250 | 180.0 | 8.4 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS657095YFFR | DSBGA | YFF | 16 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS657095YFFT | DSBGA | YFF | 16 | 250 | 182.0 | 182.0 | 20.0 |

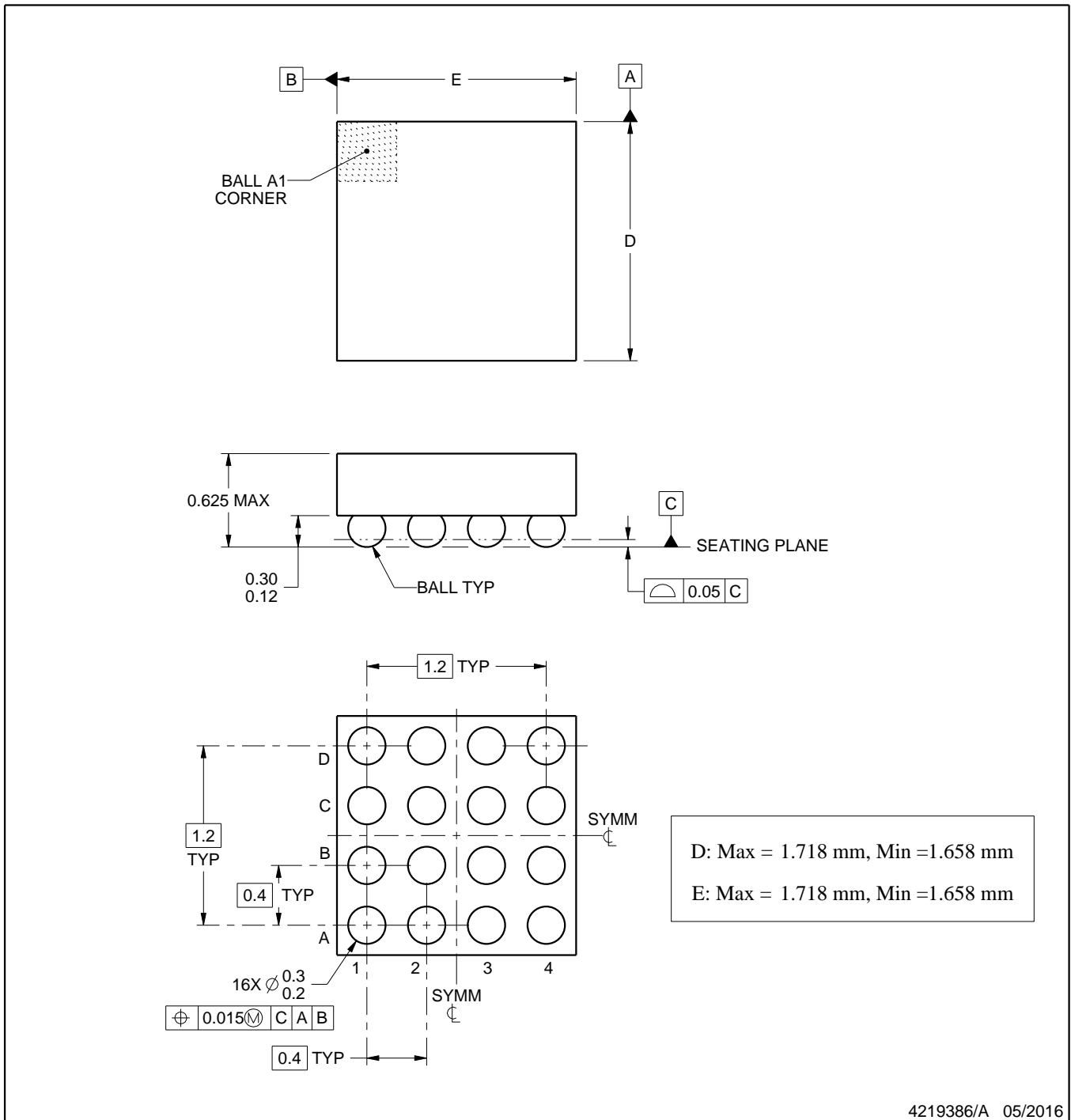
YFF0016



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

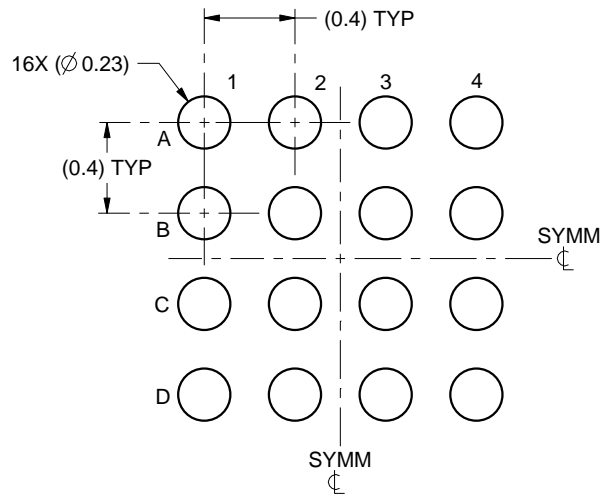
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

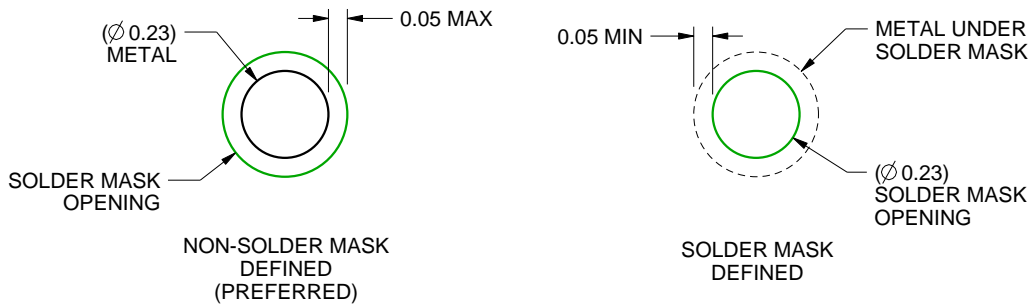
YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

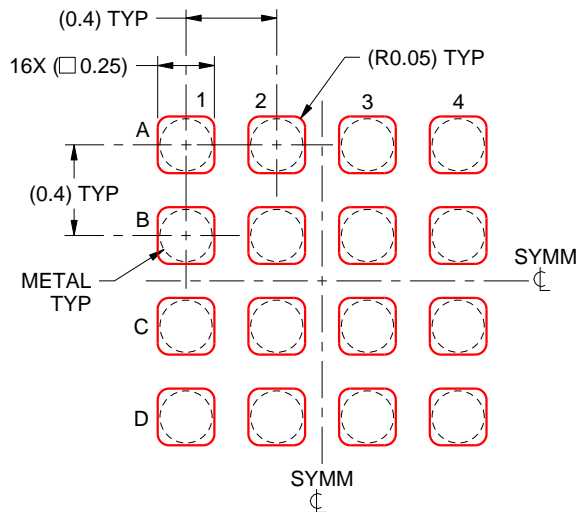
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0016

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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