TPS763 150mA, 10V, Low-Dropout Voltage Regulator

1 Features

- Input voltage range V_{IN}: 2.7V to 10V
- Output voltage range V_{OUT}:
  - Fixed device: 1.6V to 5.0V
  - Adjustable device: 1.5V to 6.5V
- Output current: up-to 150mA
- Output voltage accuracy:
  - New chip: ±1.0% (typical)
  - Legacy chip: ±2.0% (typical)
- Low quiescent current I_Q:
  - New chip: 65µA (typ) at I_{OUT} = 0mA
  - New chip: 765µA (typ) at I_{OUT} = 150mA
  - Legacy chip: 85µA (typ) at I_{OUT} = 1mA to 150mA
- Dropout voltage:
  - New chip: 175mV (typical) at I_{OUT} = 150mA
  - Legacy chip: 360mV (typical) at I_{OUT} = 150mA
- Thermal shutdown and overcurrent limitation
- Active over-shoot pulldown protection (new chip)
- Operating junction temperature: –40°C to 125°C
- 5-pin SOT-23 (DBV), $R_{\theta JA}$ = 178.6°C/W (new chip)

2 Applications

- Smoke and heat detectors
- Thermostats
- Motion detectors (PIR, uWave, and so forth)
- Cordless power tools
- Appliance battery packs
- Electricity meters
- Water meters

3 Description

The TPS763 family of low-dropout (LDO) linear voltage regulators supports wide input voltage range of 2.7V to 10V and up-to 150mA of load current. The output range is from 1.6V to 5.0V for fixed version, and 1.5V to 6.5V for adjustable version.

The TPS763 has a ±1.5% (across line/load/temp for the new chip) output accuracy that is required for powering digital loads with tight supply requirements. The internal soft-start circuit reduces inrush current during start-up (for new chip), thus allowing for smaller input capacitance.

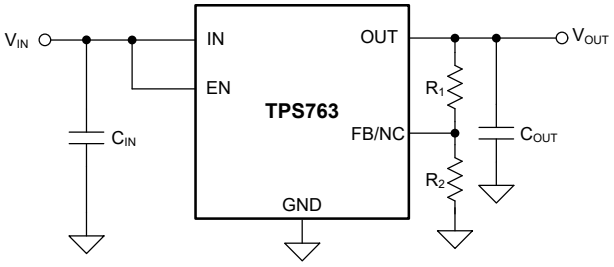
The TPS763 family of low-dropout (LDO) voltage regulators offers the benefits of low-dropout voltage, low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and quiescent currents compared to conventional LDO regulators. Offered in a 5-pin, small outline integrated-circuit SOT-23 package, the TPS763 series devices are and excellent choice for cost-sensitive designs and applications where board space is at a premium.

The TPS763 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1µA maximum at T_J = 25°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS763	DBV (SOT-23, 5)	2.9mm × 2.8mm

(1) For more information, see the Mechanical, Packaging, and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application Circuit

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4 Pin Configuration and Functions

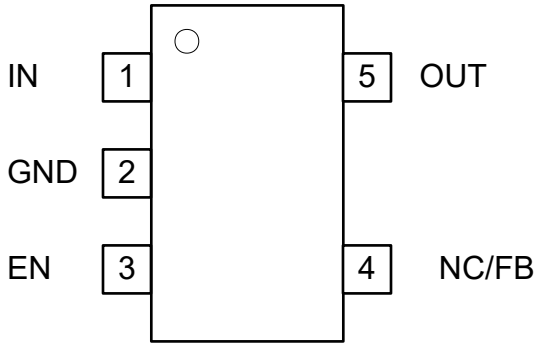


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
EN	3	—	Enable pin for the LDO. Driving the EN pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the Section 5.5 table. Tie this pin to V_{IN} if unused (for new chip).
FB	4	I	Feedback pin to set the output voltage with help of the feedback divider. See the Section 5.3 section for more information (for TPS763 Adjustable only).
GND	2	—	Ground
IN	1	I	Input supply pin. Use a capacitor with a value of 1µF or larger from this pin to ground. See the Section 5.3, Section 7.1.3 and Section 7.1.4 section for more information.
NC	4	—	No connection (fixed-voltage option only).
OUT	5	O	Output of the regulator. Use a capacitor with a value of 2.2µF or larger from this pin to ground. See the Section 7.1.4 and Section 7.1.3 section for more information.

(1) I = input, O = output

Note

The nominal output capacitance must be greater than 1µF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1µF.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	V_{IN} (for legacy chip)	–0.3	10	V
	V_{IN} (for new chip)	–0.3	18	
	V_{OUT}	–0.3	7	
	V_{FB} (for legacy chip)	–0.3	7	
	V_{FB} (for new chip)	–0.3	3	
	Voltage range at EN (for legacy chip)	–0.3	V_{IN} + 0.3	
	Voltage range at EN (for new chip)	–0.3	18	
Current	Maximum output current	Internally Limited		A
Temperature	Operating junction (T_J)	–40	150	°C
	Storage (T_{STG})	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages with respect to GND.

5.2 ESD Ratings

			VALUE (new chip)	VALUE (legacy chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22C101, all pins(2)	±1000	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		10	V
EN	Enable voltage (for new chip)	0		10	
V_{OUT}	Output voltage (for new chip)	1.2		6.5	
I_{OUT}	Output current	0		150	mA
C_{OUT}	Output capacitance (for legacy chip)	4.7			µF
	Output capacitance (for new chip)	1	2.2	220	
C_{OUT} ESR	Output capacitor ESR (for legacy chip)	0.3		10	Ω
	Output capacitor ESR (for new chip)	0		1	
C_{IN}	Input capacitance (for new chip)		0.47		µF
T_J	Junction temperature (for legacy chip)	–40		125	°C
	Junction temperature (for new chip)	–40		150	°C

5.4 Thermal Information

THERMAL METRIC (1)		Legacy chip SOT-23 (DBV) 5 PINS	New chip SOT-23 (DBV) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.3	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	125.1	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	47.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.2	15.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	33.8	46.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

Specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.7V (whichever is greater), I_{OUT} = 1mA, EN = V_{IN}, C_{IN} = 1.0µF, C_{OUT} = 4.7µF (unless otherwise noted). Typical values are at T_J= 25ºC.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	TPS76301 (for legacy chip)	3.25V > V_{IN} ≥ 2.7V, 2.5V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 75mA, T_J = 25°C	0.98 × V_{OUT}	V_{OUT}	1.02 × V_{OUT}	V
			3.25V > V_{IN} ≥ 2.7V, 2.5V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 75mA	0.97 × V_{OUT}	V_{OUT}	1.03 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 100mA, T_J = 25°C	0.98 × V_{OUT}		1.02 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 100mA	0.97 × V_{OUT}		1.03 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 150mA, T_J = 25°C	0.975 × V_{OUT}		1.025 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 150mA	0.9625 × V_{OUT}		1.0375 × V_{OUT}	
V_{OUT}	Output voltage	TPS76301 (for new chip)	3.25V > V_{IN} ≥ 2.7V, 2.5V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 75mA, T_J = 25°C	0.99 × V_{OUT}	V_{OUT}	1.01 × V_{OUT}	V
			3.25V > V_{IN} ≥ 2.7V, 2.5V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 75mA	0.985 × V_{OUT}	V_{OUT}	1.015 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 100mA, T_J = 25°C	0.99 × V_{OUT}		1.01 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 100mA	0.985 × V_{OUT}		1.015 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 150mA, T_J = 25°C	0.99 × V_{OUT}		1.01 × V_{OUT}	
			V_{IN} ≥ 3.25V, 5.0V ≥ V_{OUT} ≥ 1.5V, I_{OUT} = 1mA to 150mA	0.985 × V_{OUT}		1.015 × V_{OUT}	
V_{OUT}	Output voltage	TPS76316 (for legacy chip)	V_{IN} = 2.7V, I_{OUT} = 1mA to 75mA, T_J = 25°C	1.568	1.6	1.632	V
			V_{IN} = 2.7V, I_{OUT} = 1mA to 75mA	1.552	1.6	1.648	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 100mA, T_J = 25°C	1.568	1.6	1.632	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 100mA	1.552	1.6	1.648	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 150mA, T_J = 25°C	1.56	1.6	1.64	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 150mA	1.536	1.6	1.664	

5.5 Electrical Characteristics (continued)

Specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.7V (whichever is greater), I_{OUT} = 1mA, EN = V_{IN}, C_{IN} = 1.0µF, C_{OUT} = 4.7µF (unless otherwise noted). Typical values are at T_J= 25ºC.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	TPS76318 (for legacy chip)	V_{IN} = 2.7V, I_{OUT} = 1mA to 75mA, T_J = 25°C	1.764	1.8	1.836	V
			V_{IN} = 2.7V, I_{OUT} = 1mA to 75mA	1.746	1.8	1.854	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 100mA, T_J = 25°C	1.764	1.8	1.836	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 100mA	1.746	1.8	1.854	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 150mA, T_J = 25°C	1.755	1.8	1.845	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 150mA	1.733	1.8	1.867	
V_{OUT}	Output voltage	TPS76318 (for new chip)	V_{IN} = 2.7V, I_{OUT} = 1mA to 75mA, T_J = 25°C	1.773	1.8	1.827	V
			V_{IN} = 2.7V, I_{OUT} = 1mA to 75mA	1.764	1.8	1.836	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 100mA, T_J = 25°C	1.773	1.8	1.827	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 100mA	1.764	1.8	1.836	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 150mA, T_J = 25°C	1.773	1.8	1.827	
			V_{IN} = 3.25V, I_{OUT} = 1mA to 150mA	1.764	1.8	1.836	
V_{OUT}	Output voltage	TPS76325 (for legacy chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	2.45	2.5	2.55	V
			I_{OUT} = 1mA to 100mA	2.425	2.5	2.575	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	2.438	2.5	2.562	
			I_{OUT} = 1mA to 150mA	2.407	2.5	2.593	
V_{OUT}	Output voltage	TPS76325 (for new chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	2.4625	2.5	2.5375	V
			I_{OUT} = 1mA to 100mA	2.45	2.5	2.55	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	2.4625	2.5	2.5375	
			I_{OUT} = 1mA to 150mA	2.45	2.5	2.55	
V_{OUT}	Output voltage	TPS76327 (for legacy chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	2.646	2.7	2.754	V
			I_{OUT} = 1mA to 100mA	2.619	2.7	2.781	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	2.632	2.7	2.767	
			I_{OUT} = 1mA to 150mA	2.599	2.7	2.801	
V_{OUT}	Output voltage	TPS76328 (for legacy chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	2.744	2.8	2.856	V
			I_{OUT} = 1mA to 100mA	2.716	2.8	2.884	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	2.73	2.8	2.87	
			I_{OUT} = 1mA to 150mA	2.695	2.8	2.905	
V_{OUT}	Output voltage	TPS76328 (for new chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	2.758	2.8	2.842	V
			I_{OUT} = 1mA to 100mA	2.744	2.8	2.856	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	2.758	2.8	2.842	
			I_{OUT} = 1mA to 150mA	2.744	2.8	2.856	
V_{OUT}	Output voltage	TPS76330 (for legacy chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	2.94	3	3.06	V
			I_{OUT} = 1mA to 100mA	2.91	3	3.09	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	2.925	3	3.075	
			I_{OUT} = 1mA to 150mA	2.888	3	3.112	

5.5 Electrical Characteristics (continued)

Specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.7V (whichever is greater), I_{OUT} = 1mA, EN = V_{IN}, C_{IN} = 1.0µF, C_{OUT} = 4.7µF (unless otherwise noted). Typical values are at T_J= 25ºC.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage	TPS76330 (for new chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	2.955	3	3.045	V
			I_{OUT} = 1mA to 100mA	2.94	3	3.06	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	2.955	3	3.045	
			I_{OUT} = 1mA to 150mA	2.94	3	3.06	
V_{OUT}	Output voltage	TPS76333 (for legacy chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	3.234	3.3	3.366	V
			I_{OUT} = 1mA to 100mA	3.201	3.3	3.399	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	3.218	3.3	3.382	
			I_{OUT} = 1mA to 150mA	3.177	3.3	3.423	
V_{OUT}	Output voltage	TPS76333 (for new chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	3.2505	3.3	3.3495	V
			I_{OUT} = 1mA to 100mA	3.234	3.3	3.366	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	3.2505	3.3	3.3495	
			I_{OUT} = 1mA to 150mA	3.234	3.3	3.366	
V_{OUT}	Output voltage	TPS76338 (for new chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	3.724	3.8	3.876	V
			I_{OUT} = 1mA to 100mA	3.705	3.8	3.895	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	3.686	3.8	3.914	
			I_{OUT} = 1mA to 150mA	3.667	3.8	3.933	
V_{OUT}	Output voltage	TPS76350 (for legacy chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	4.875	5	5.125	V
			I_{OUT} = 1mA to 100mA	4.825	5	5.175	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	4.85	5	5.15	
			I_{OUT} = 1mA to 150mA	4.8	5	5.2	
V_{OUT}	Output voltage	TPS76350 (for new chip)	I_{OUT} = 1mA to 100mA, T_J = 25°C	4.925	5	5.075	V
			I_{OUT} = 1mA to 100mA	4.9	5	5.1	
			I_{OUT} = 1mA to 150mA, T_J = 25°C	4.925	5	5.075	
			I_{OUT} = 1mA to 150mA	4.9	5	5.1	
I_Q	Quiescent current (GND current)	For legacy chip	I_{OUT} = 1mA to 150mA, T_J = 25°C		85	100	µA
			I_{OUT} = 1mA to 150mA			140	
		For new chip	I_{OUT} = 0mA		65	125	
			I_{OUT} = 1mA to 150mA, T_J = 25°C		765	890	
			I_{OUT} = 1mA to 150mA			1060	
$\Delta V_{OUT(\Delta VOUT)}$	Output voltage line regulation ($\Delta V_{OUT}/V_{OUT}$)	For legacy chip	$V_{OUT(NOM)}$ +1.0V ≤ V_{IN} ≤ 10V, V_{IN} ≥ 3.5V, T_J = 25°C		0.04	0.07	%/V
			$V_{OUT(NOM)}$ +1.0V ≤ V_{IN} ≤ 10V, V_{IN} ≥ 3.5V			0.1	
		For new chip	$V_{OUT(NOM)}$ +1.0V ≤ V_{IN} ≤ 10V, V_{IN} ≥ 3.5V, T_J = 25°C			0.01	
			$V_{OUT(NOM)}$ +1.0V ≤ V_{IN} ≤ 10V, V_{IN} ≥ 3.5V			0.01	
V_n	Output noise voltage	For legacy chip	BW = 300Hz to 50kHz, V_{OUT} = 3.3V , C_{OUT} = 10µF		140		μV_{RMS}
		For new chip	BW = 300Hz to 50kHz, V_{OUT} = 3.3V , C_{OUT} = 4.7µF		165		
I_{CL}	Output current limit	For legacy chip	V_{OUT} = 0V, T_J = 25°C	0.5	0.8	1.5	A
		For new chip	V_{OUT} = 0V		0.8	1.05	

5.5 Electrical Characteristics (continued)

Specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.7V (whichever is greater), I_{OUT} = 1mA, EN = V_{IN}, C_{IN} = 1.0µF, C_{OUT} = 4.7µF (unless otherwise noted). Typical values are at T_J= 25ºC.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{STANDBY}$	Standby current	For legacy chip	EN < 0.5V, T_J = 25°C		0.5	1	µA
			EN < 0.5V			2	
		For new chip	EN < 0.15V, T_J = 25°C		1.25		
			EN < 0.15V		1.12	2.75	
EN	High level enable input voltage	For legacy chip			1.4	2	V
	Low level enable input voltage			0.5	1.2		
	High level enable input voltage	For new chip			0.85	1.6	
	Low level enable input voltage			0.15	0.72		
PSRR	Power-supply ripple rejection	For legacy chip	C_{OUT} = 10µF, f = 1kHz, T_J = 25 °C		60		dB
		For new chip	C_{OUT} = 4.7µF, f = 1kHz, T_J = 25 °C		58		
I_{EN}	Input current (EN)	For legacy chip	EN = 0V		–0.01	–0.5	µA
			EN = V_{IN}		–0.01	–0.5	
		For new chip	EN = 0V		–0.35	–0.7	
			EN = V_{IN}		0.008	0.8	
V_{DO}	Dropout voltage	TPS76325 (for legacy chip)	I_{OUT} = 0mA, T_J = 25°C		0.2		mV
			I_{OUT} = 1mA, T_J = 25°C		3		
			I_{OUT} = 50mA, T_J = 25°C		120	150	
			I_{OUT} = 50mA			200	
			I_{OUT} = 75mA, T_J = 25°C		180	225	
			I_{OUT} = 75mA			300	
			I_{OUT} = 100mA, T_J = 25°C		240	300	
			I_{OUT} = 100mA			400	
			I_{OUT} = 150mA, T_J = 25°C		360	450	
			I_{OUT} = 150mA			600	
V_{DO}	Dropout voltage	TPS76333 (for legacy chip)	I_{OUT} = 0mA, T_J = 25°C		0.2		mV
			I_{OUT} = 1mA, T_J = 25°C		3		
			I_{OUT} = 50mA, T_J = 25°C		100	125	
			I_{OUT} = 50mA			166	
			I_{OUT} = 75mA, T_J = 25°C		150	188	
			I_{OUT} = 75mA			250	
			I_{OUT} = 100mA, T_J = 25°C		200	250	
			I_{OUT} = 100mA			333	
			I_{OUT} = 150mA, T_J = 25°C		300	375	
			I_{OUT} = 150mA			500	

5.5 Electrical Characteristics (continued)

Specified at T_J = –40°C to 125°C, V_{IN} = $V_{OUT(nom)}$ + 1.0V or V_{IN} = 2.7V (whichever is greater), I_{OUT} = 1mA, EN = V_{IN}, C_{IN} = 1.0µF, C_{OUT} = 4.7µF (unless otherwise noted). Typical values are at T_J= 25ºC.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DO}	Dropout voltage	TPS76350 (for legacy chip)	I_{OUT} = 0mA, T_J = 25°C		0.2		mV
			I_{OUT} = 1mA, T_J = 25°C		2		
			I_{OUT} = 50mA, T_J = 25°C		60	75	
			I_{OUT} = 50mA			100	
			I_{OUT} = 75mA, T_J = 25°C		90	113	
			I_{OUT} = 75mA			150	
			I_{OUT} = 100mA, T_J = 25°C		120	150	
			I_{OUT} = 100mA			200	
			I_{OUT} = 150mA, T_J = 25°C		180	225	
			I_{OUT} = 150mA			300	
V_{DO}	Dropout voltage	TPS763xx (for new chip)	I_{OUT} = 0mA, T_J = 25°C		1	2.75	mV
			I_{OUT} = 1mA, T_J = 25°C		11.5	14	
			I_{OUT} = 50mA, T_J = 25°C		120	145	
			I_{OUT} = 50mA			184	
			I_{OUT} = 75mA, T_J = 25°C		135	155	
			I_{OUT} = 75mA			195	
			I_{OUT} = 100mA, T_J = 25°C		145	165	
			I_{OUT} = 100mA			215	
			I_{OUT} = 150mA, T_J = 25°C		180	198	
			I_{OUT} = 150mA			254	

5.6 Typical Characteristics

at operating temperature T_J = 25°C, I_{OUT} = 1mA, V_{EN} = 0.9V, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, and V_{IN} = $V_{OUT(typ)}$ + 1.0V or 2.7V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

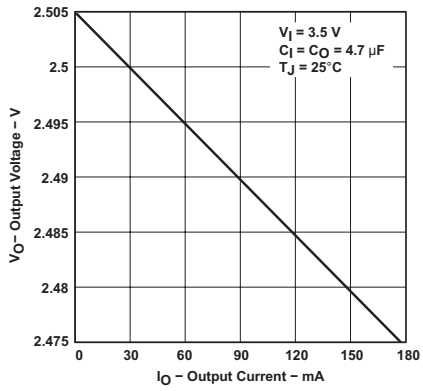


Figure 5-1. TPS76325 Output Voltage vs Output Current (Legacy Chip)

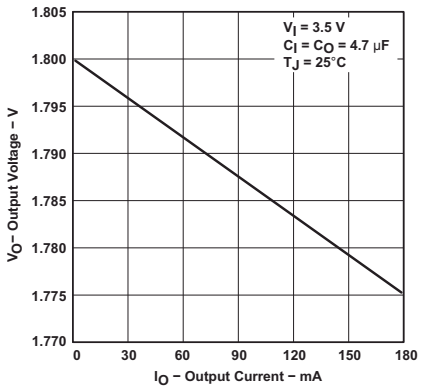


Figure 5-2. TPS76318 Output Voltage vs Output Current (Legacy Chip)

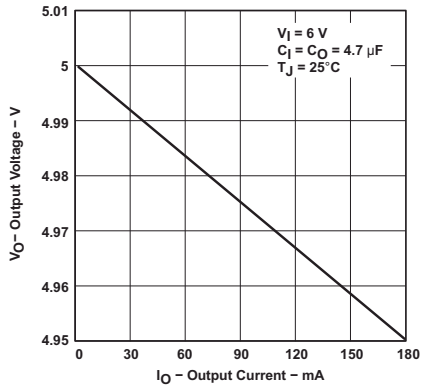


Figure 5-3. TPS76350 Output Voltage vs Output Current (Legacy Chip)

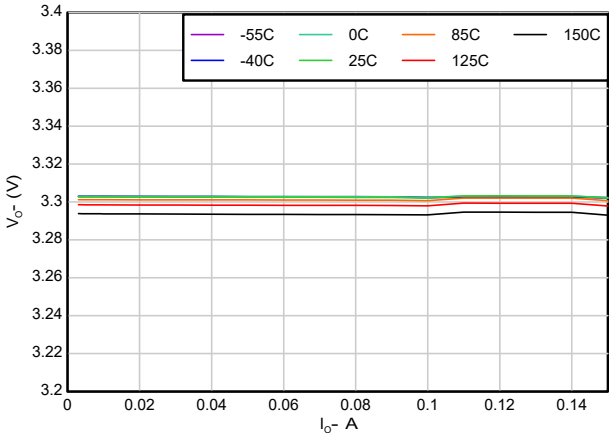


Figure 5-4. TPS76333 Output Voltage vs Output Current (new chip)

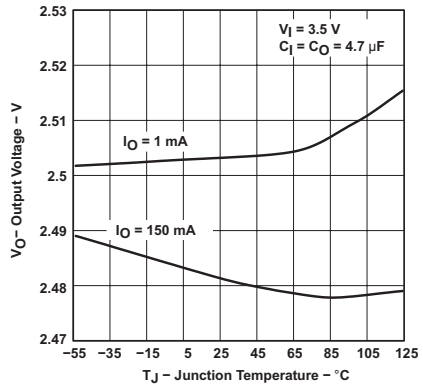


Figure 5-5. TPS76325 Output Voltage vs Free-Air Temperature (Legacy Chip)

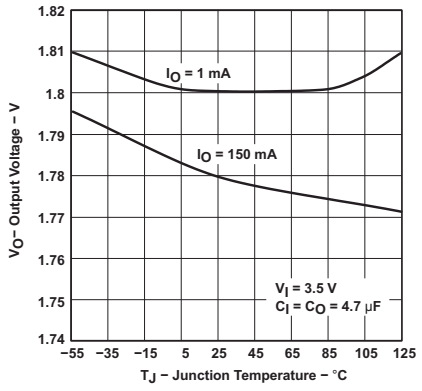


Figure 5-6. TPS76318 Output Voltage vs Free-Air Temperature (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, V_{EN} = 0.9V, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, and V_{IN} = $V_{OUT(typ)}$ + 1.0V or 2.7V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

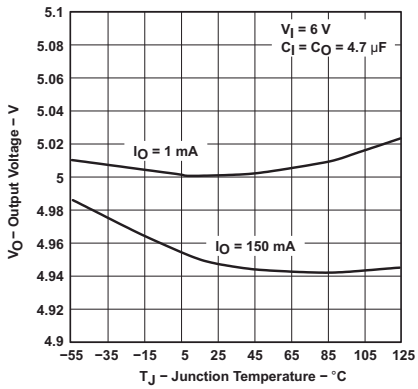


Figure 5-7. TPS76350 Output Voltage vs Free-Air Temperature (Legacy Chip)

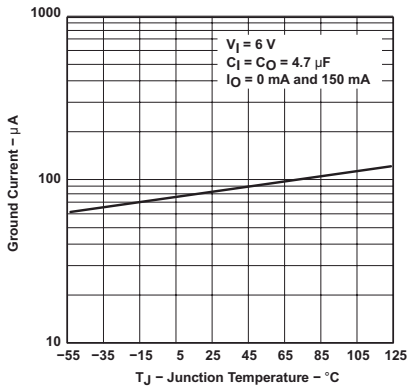


Figure 5-8. TPS76350 Ground Current vs Free-Air Temperature (Legacy Chip)

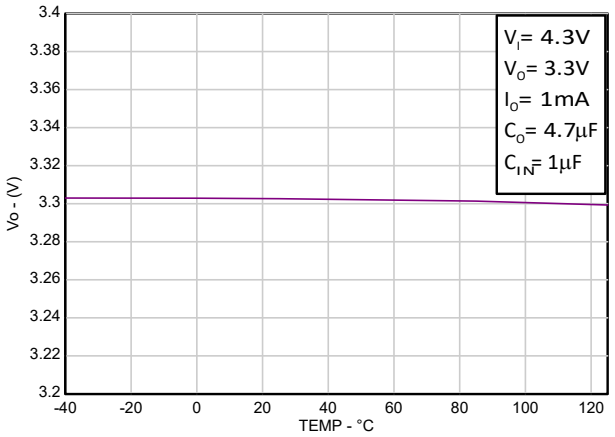


Figure 5-9. TPS76333 Output Voltage vs Free-Air Temperature (new chip)

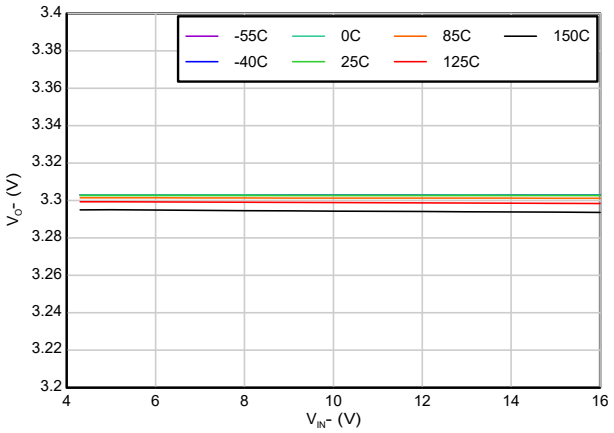


Figure 5-10. TPS76333 Output Voltage vs Input Voltage (new chip)

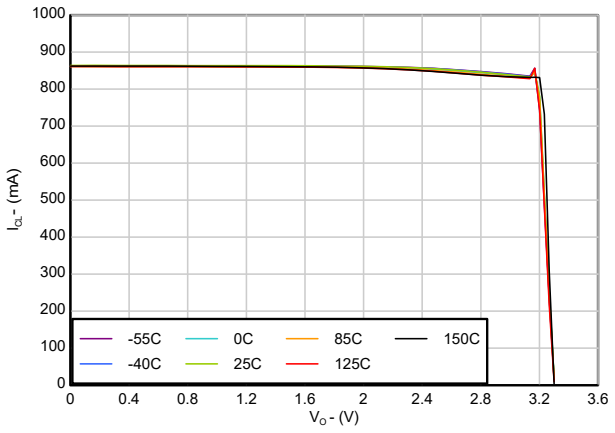


Figure 5-11. TPS76333 Short-circuit current vs Output voltage (new chip)

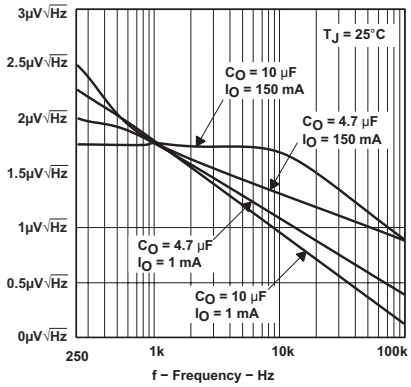


Figure 5-12. Output Noise vs Frequency (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, V_{EN} = 0.9V, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, and V_{IN} = $V_{OUT(typ)}$ + 1.0V or 2.7V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

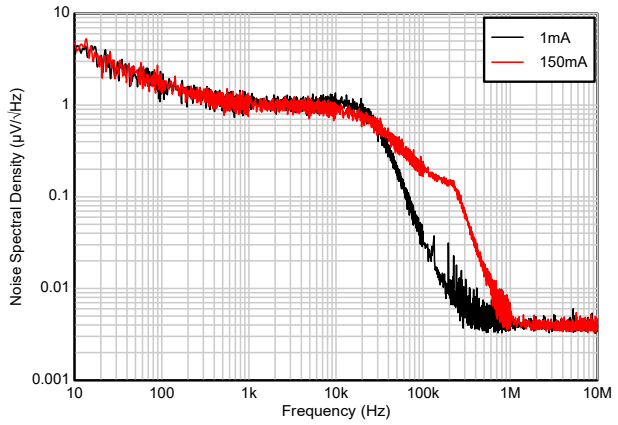


Figure 5-13. Output Noise Density versus Load Current (I_L) Frequency (New Chip)

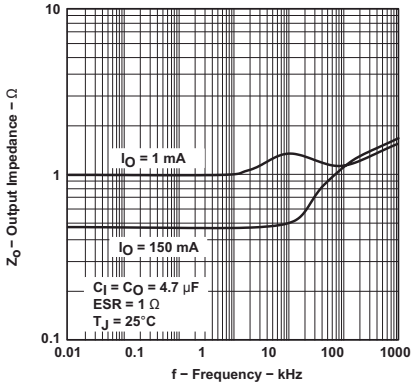


Figure 5-14. Output Impedance vs Frequency (Legacy Chip)

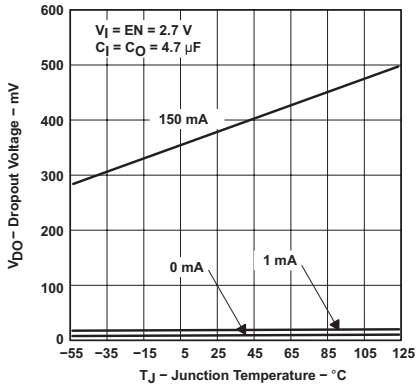


Figure 5-15. TPS76325 Dropout Voltage vs Free-Air Temperature (Legacy Chip)

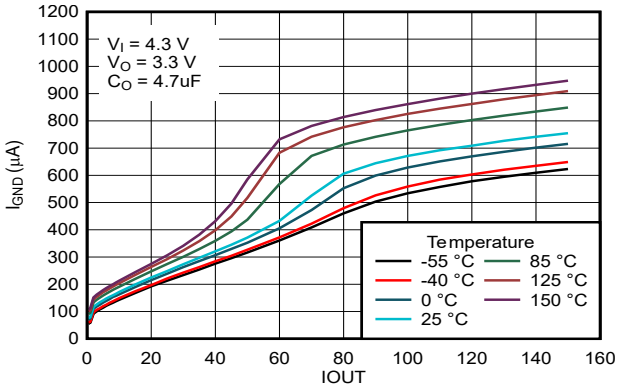


Figure 5-16. Ground Pin Current vs Load Current (new chip)

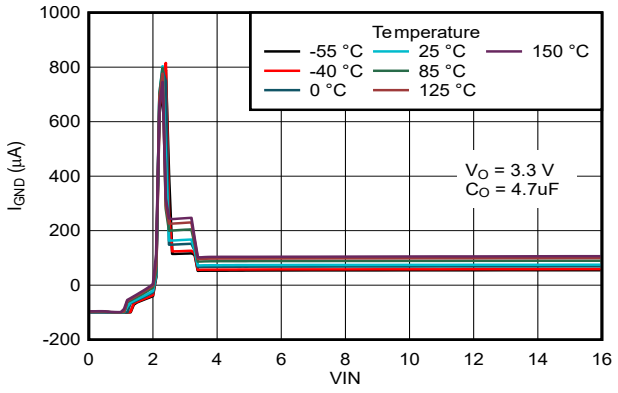


Figure 5-17. Input Current vs Input Voltage (new chip)

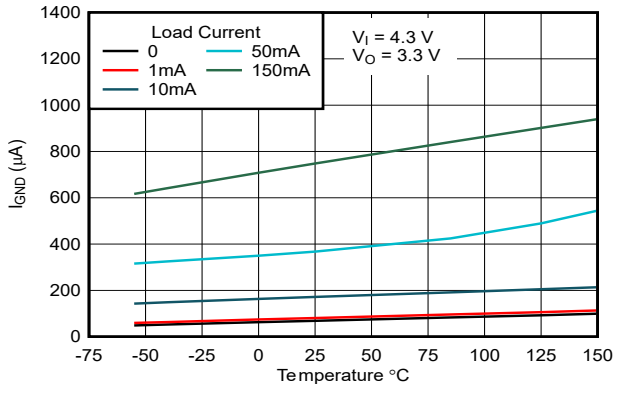


Figure 5-18. Ground-Pin Current vs Temperature (new chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, V_{EN} = 0.9V, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, and V_{IN} = $V_{OUT(typ)}$ + 1.0V or 2.7V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

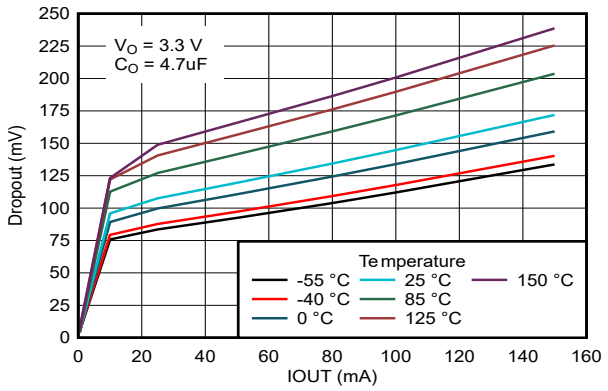


Figure 5-19. TPS76333 Dropout Voltage vs Load Current (new chip)

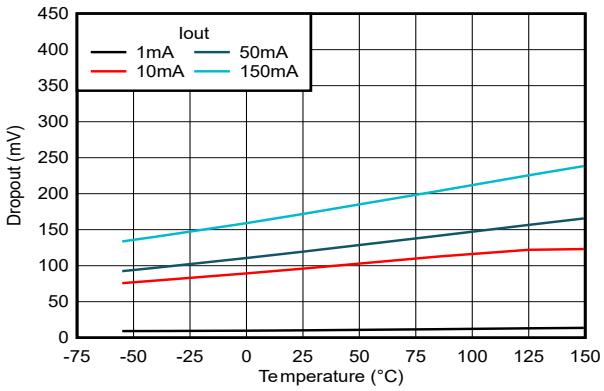


Figure 5-20. TPS76333 Dropout Voltage vs Temperature (new chip)

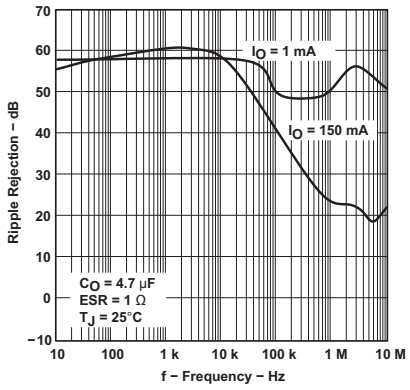


Figure 5-21. TPS76325 Ripple Rejection vs Frequency (Legacy Chip)

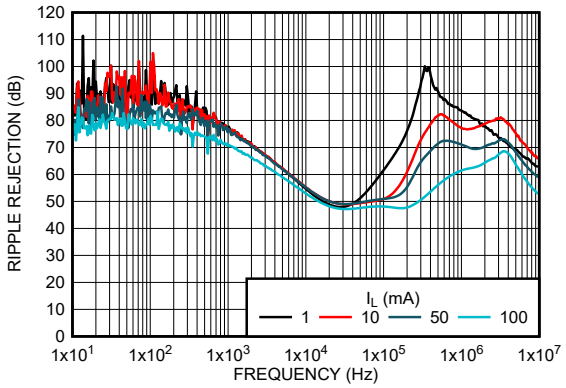


Figure 5-22. Ripple Rejection versus Load Current (I_L) and Frequency (New Chip)

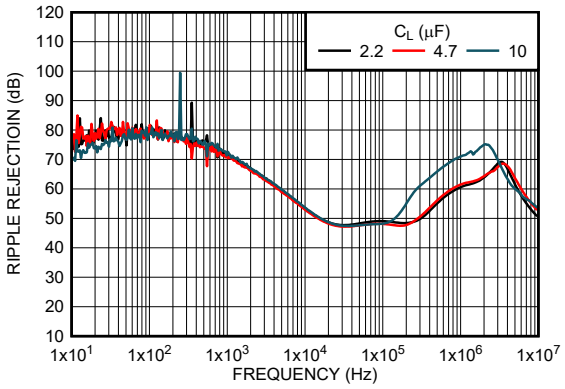


Figure 5-23. Ripple Rejection versus Output Capacitor (C_L) and Frequency (New Chip)

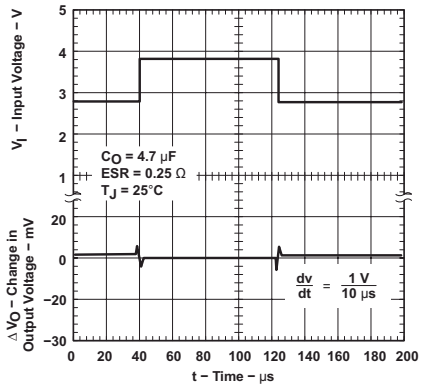
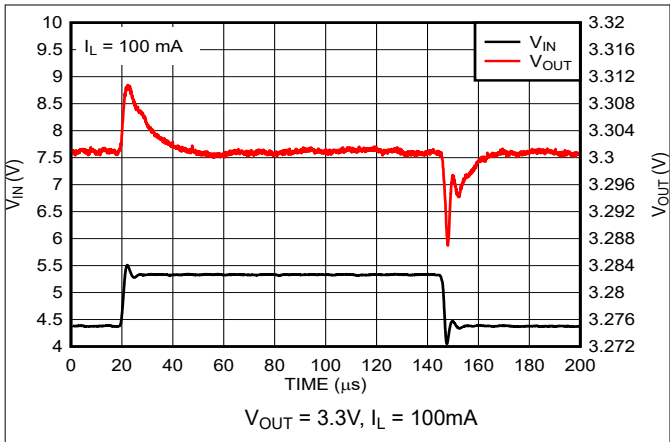


Figure 5-24. TPS76318 Line Transient Response (Legacy Chip)

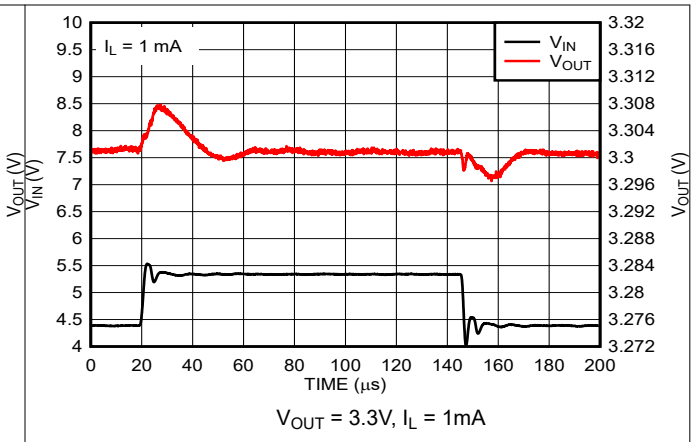
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, V_{EN} = 0.9V, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, and V_{IN} = $V_{OUT(typ)}$ + 1.0V or 2.7V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



V_{OUT} = 3.3V, I_L = 100mA

Figure 5-25. Line Transient Response (New Chip)



V_{OUT} = 3.3V, I_L = 1mA

Figure 5-26. Line Transient Response (New Chip)

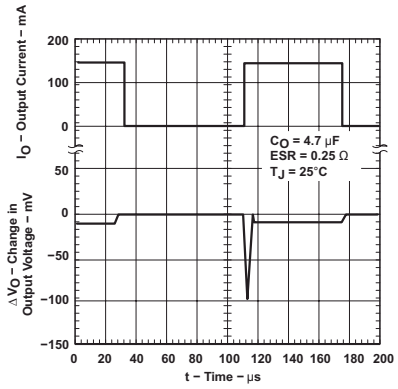
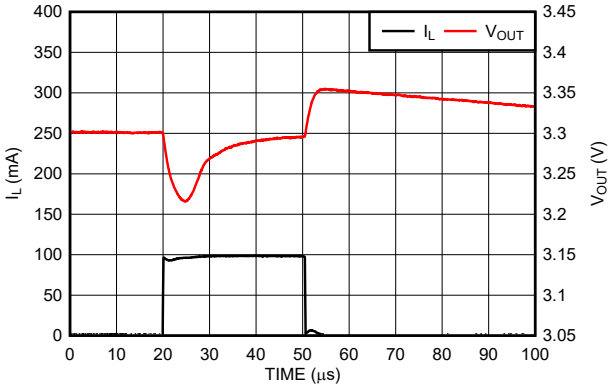


Figure 5-27. TPS76318 Load Transient Response (Legacy Chip)



V_{OUT} = 3.3V, C_{OUT} = 2.2µF

Figure 5-28. Load Transient Response (New Chip)

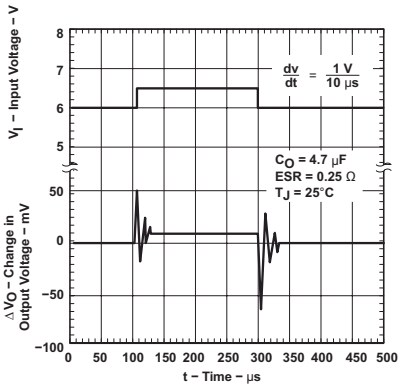


Figure 5-29. TPS76350 Line Transient Response (Legacy Chip)

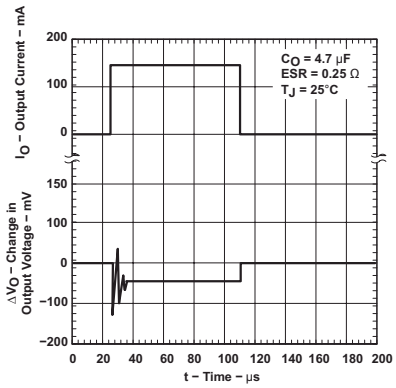
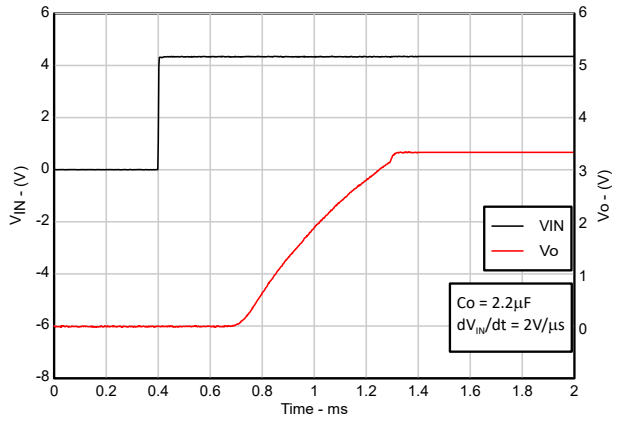


Figure 5-30. TPS76350 Load Transient Response (Legacy Chip)

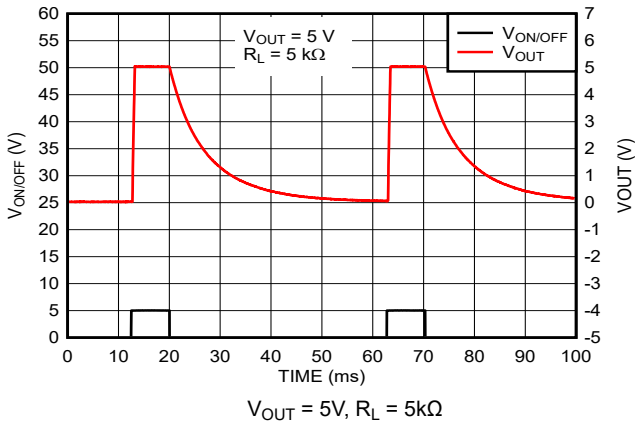
5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, V_{EN} = 0.9V, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, and V_{IN} = $V_{OUT(typ)}$ + 1.0V or 2.7V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C



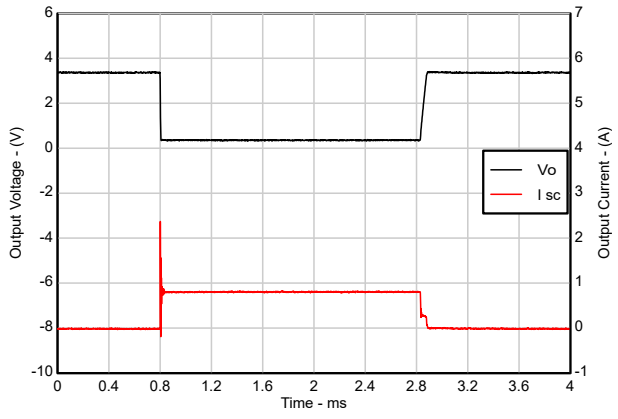
V_{OUT} = 3.3V, R_L = 3.3kΩ

Figure 5-31. Turn-on Waveform (New Chip)



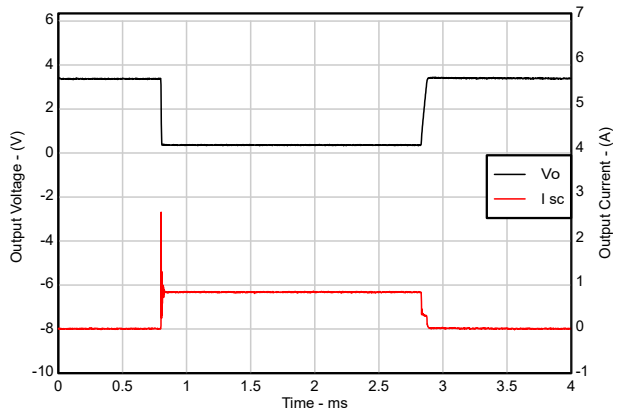
V_{OUT} = 5V, R_L = 5kΩ

Figure 5-32. Turn-off Waveform (New Chip)



V_{IN} = 4.3V

Figure 5-33. Short Circuit Current versus Time (New Chip)



V_{IN} = 10.0V

Figure 5-34. Short Circuit Current versus Time (New Chip)

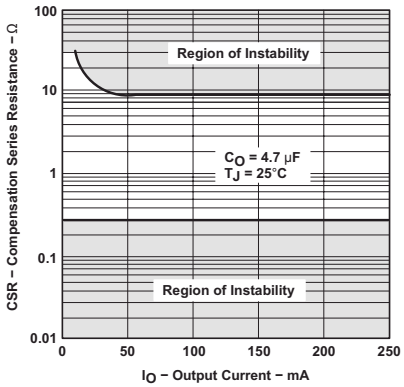


Figure 5-35. Compensation Series Resistance (CSR) vs Output Current (Legacy Chip)

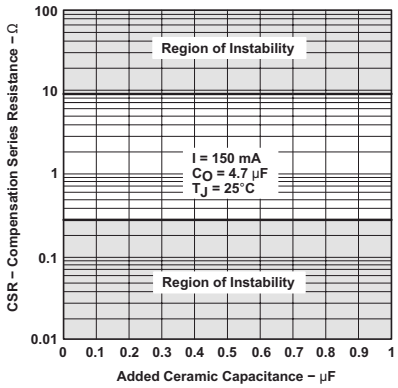


Figure 5-36. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance (Legacy Chip)

5.6 Typical Characteristics (continued)

at operating temperature T_J = 25°C, I_{OUT} = 1mA, V_{EN} = 0.9V, C_{IN} = 2.2µF, C_{OUT} = 2.2µF, and V_{IN} = $V_{OUT(typ)}$ + 1.0V or 2.7V (whichever is greater), unless otherwise noted; typical values are at T_J = 25°C

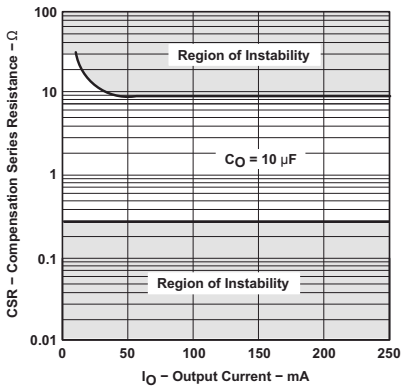


Figure 5-37. Compensation Series Resistance (CSR) vs Output Current (Legacy Chip)

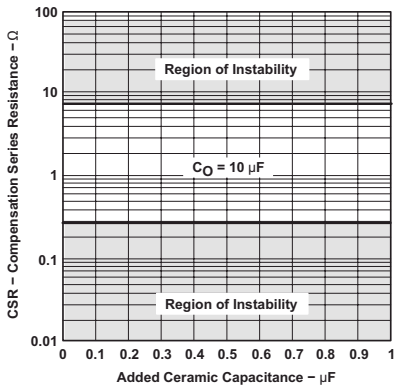


Figure 5-38. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance (Legacy Chip)

6 Detailed Description

6.1 Overview

The TPS763 family of low-dropout (LDO) linear voltage regulators supports wide input voltage range of 2.7V to 10V and up to 150mA of load current. The output range is from 1.6V to 5.0V for the fixed version, and from 1.5V to 6.5V for the adjustable version.

The TPS763 has a ±1.5% output accuracy (across line/load and temp for new chip) that is required for powering digital loads with tight supply requirements. The TPS763 (new chip) has an internal soft start mechanism that provides a uniform start-up with controlled inrush current. This LDO also has over-current and thermal protection during a load-short or fault condition on the output for better reliability.

6.2 Functional Block Diagrams

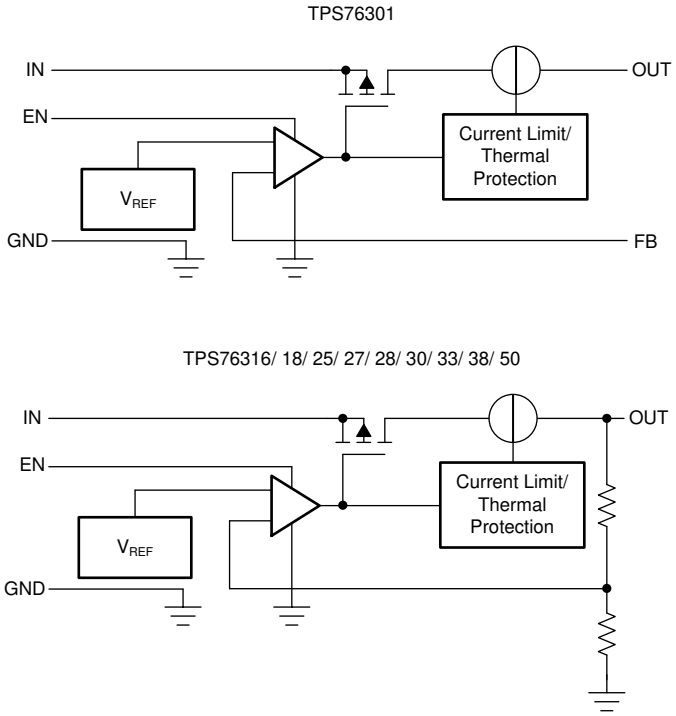


Figure 6-1. Functional Block Diagram (Legacy Chip)

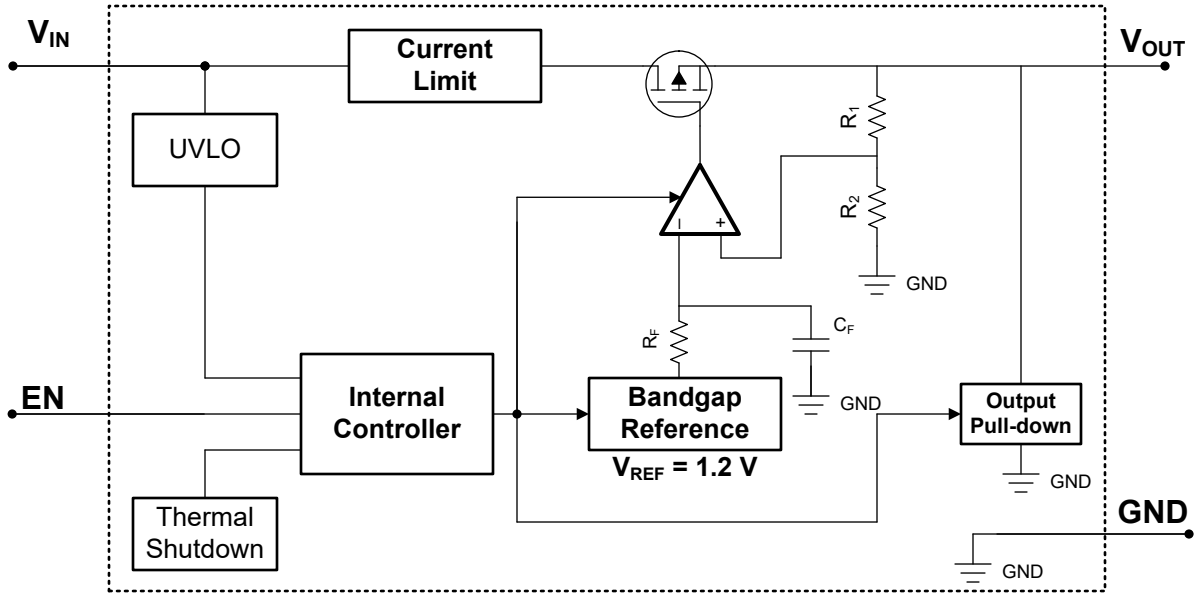


Figure 6-2. Functional Block Diagram (Fixed, New Chip)

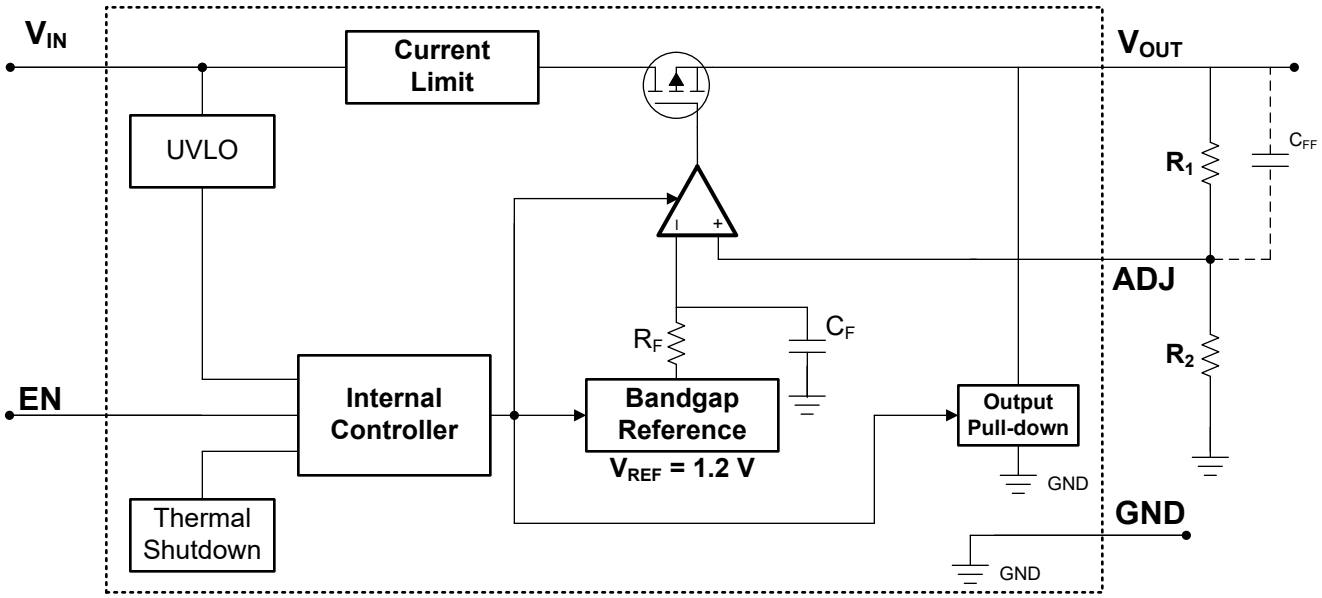


Figure 6-3. Functional Block Diagram (Adjustable, New Chip)

6.3 Feature Description

6.3.1 Output Enable

The EN pin for the device is an active-high pin. The output voltage is enabled when the voltage of the EN pin is greater than the high-level input voltage of the EN pin and disabled with the EN pin voltage is less than the low-level input voltage of the EN pin. If independent control of the output voltage is not needed, connect the EN pin to the input of the device.

The device has an internal pulldown circuit that activates when the device is disabled by pulling the EN pin voltage lower than the low-level input voltage of the EN pin to actively discharge the output voltage.

6.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Section 5.3* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

6.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Section 5.5* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [$(V_{IN} – V_{OUT}) \times I_{CL}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-4 illustrates a diagram of the current limit.

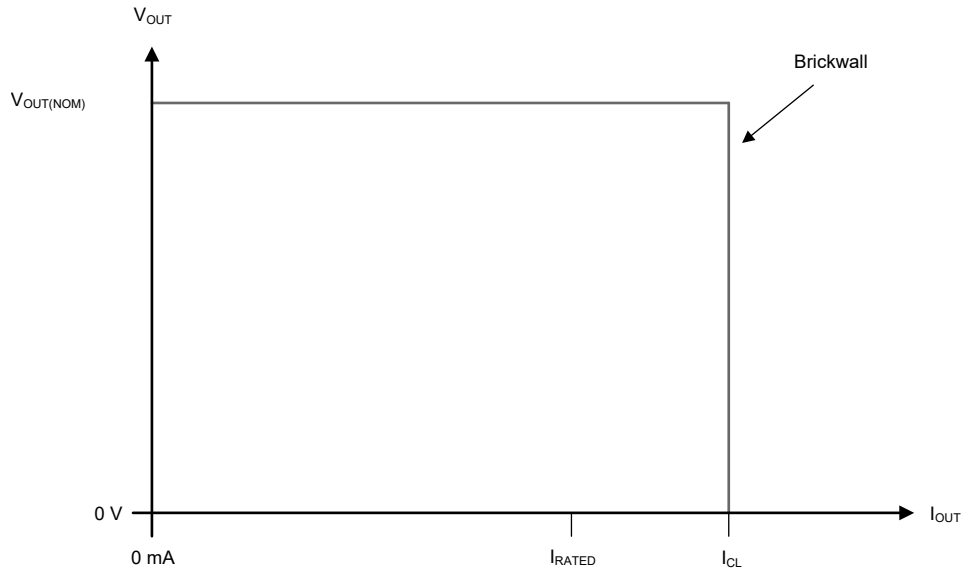


Figure 6-4. Current Limit

6.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis verifies that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

When the thermal limit is triggered with load currents near the value of the current limit, the output can oscillate prior to the output switching off.

For reliable operation, limit the junction temperature to the maximum listed in the *Section 5.3* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.3.5 Output Pulldown

The new chip version of TPS763 has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{EN} < V_{EN(LOW)}$)
- If 1.0V < V_{IN} < 2.7V (for new chip)

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Section 7.1.5* section for more details.

6.4 Device Functional Modes

6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < 2.7V$	$V_{EN} < V_{EN(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the EN pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Adjustable Device Feedback Resistors

The adjustable-version device requires external feedback divider resistors to set the output voltage. V_{OUT} is set using the feedback divider resistors, R_1 and R_2, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

7.1.2 Capacitor Selection (Legacy Chip)

Like all low dropout regulators, the TPS763 requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 µF and the ESR (equivalent series resistance) must be between 0.3Ω and 10Ω. Capacitor values 4.7 µF or larger are acceptable, provided the ESR is less than 10Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided the capacitors meet the requirements described above. Most of the commercially available 4.7 µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above (see Table 7-1). Supported ESR range across output load current and added ceramic capacitance is captured in Figure 5-35, Figure 5-36, Figure 5-37 and Figure 5-38.

Table 7-1. Capacitor Selection

PART NO.	MFR	VALUE	MAX ESR	SIZE (H × L × W)
T494B475K016AS	Kemet	4.7 µF	1.5Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	Sprague	10 µF	1.5Ω	1.3 × 7 × 2.7
695D106x003562T	Sprague	10 µF	1.3Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6Ω	2.6 × 6 × 3.2

7.1.3 Recommended Capacitor Types (New Chip)

The new chip is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Maximum supported ESR range across complete temperature (−40°C to +150°C) and load current range (0mA-150mA) is less than 1Ω. If in an existing implementation where different type of capacitors with higher ESR are used, use a low-ESR, 100nF MLCC capacitor. Place this capacitor as close as possible to the device output pin (V_{OUT}).

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the Recommended Operating Conditions table account for an effective capacitance of approximately 50% of the nominal value.

7.1.4 Input and Output Capacitor Requirements (New Chip)

For legacy chip, although not required, a 0.047µF or larger ceramic bypass input capacitor, connected between IN and GND and located close to the TPS763, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor can be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

For new chip, although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

For the new chip, dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Procedures* table for stability.

7.1.5 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3V$.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 7-1 shows one approach for protecting the device.

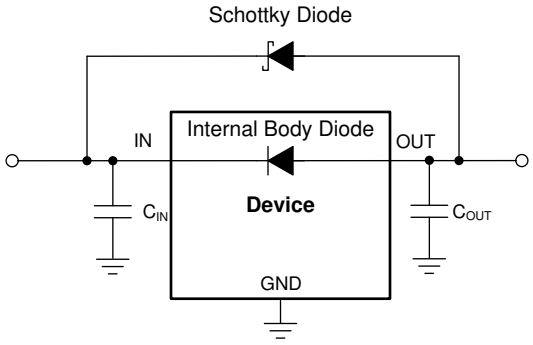


Figure 7-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

Figure 7-2 shows another, more commonly used, approach in high input voltage applications.

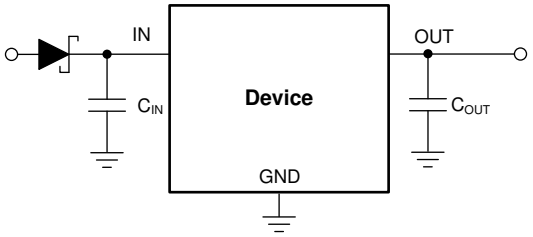


Figure 7-2. Reverse Current Prevention Using a Diode Before the LDO

7.1.6 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

7.1.7 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 3 calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (3)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 4, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (4)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

7.1.8 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J). As described in Equation 5, use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. As described in Equation 6, use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (5)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (6)$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

7.1.9 Special Consideration for Line Transients (New Chip)

During a line transient, the response of this LDO to a very large or fast input voltage change can cause a brief shutdown lasting up to a few hundred microseconds from the voltage transition. This shutdown can be avoided by reducing the voltage step size, increasing the transition time, or a combination of both. Figure 7-3 provides a boundary to follow to avoid this behavior. If necessary, reduce slew rate and the voltage step size to stay below the curve.

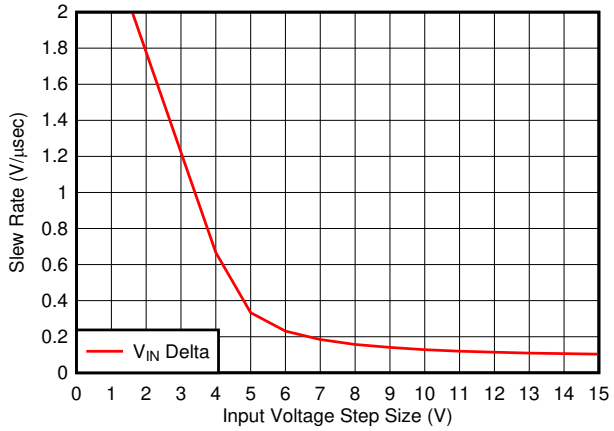


Figure 7-3. Recommended Input Voltage Step and Slew Rate in a Line Transient

7.2 Typical Application

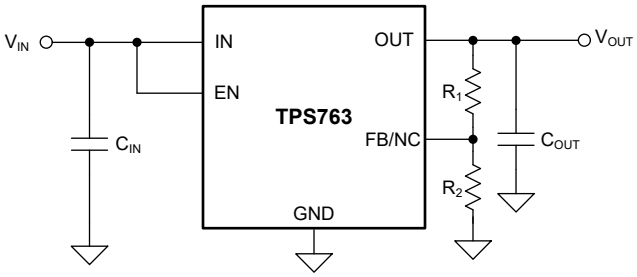


Figure 7-4. Typical Application Circuit

7.2.1 Design Requirements

Table 7-2 summarizes the design requirements for Figure 7-4.

Table 7-2. Design Parameters

PARAMETER	DESIGN VALUES
V_{IN}	5.3V
V_{OUT}	3.3V ±1.25%
$I_{(IN)}$ (no load)	< 5µA
I_{OUT} (max)	150mA
T_A	57.88°C (max)

7.2.2 Detailed Design Procedure

Select a 3.3V output, fixed or adjustable device to generate the 3.3V rail. The fixed-version LDO has internal feedback divider resistors, and thus has lower quiescent current. The adjustable-version LDO requires external feedback divider resistors, and is described in the *Selecting Feedback Divider Resistors* section.

7.2.2.1 Transient Response

As with any regulator, increasing the output capacitor value reduces over- and undershoot magnitude, but increases transient response duration.

7.2.2.2 Selecting Feedback Divider Resistors

The output voltage of the TPS76301 adjustable regulator is programmed using an external resistor divider as illustrated in Figure 7-5. The output voltage is calculated using Equation 7.

$$V_O = 0.995 \times V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (7)$$

where:

- Vref = 1.192V typical (the internal reference voltage)
- 0.995 is a constant used to center the load regulator (1%)

Resistors R1 and R2 must be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values must be avoided as leakage currents at FB increase the output voltage error. TI recommends choosing a design procedure of R2 = 169kΩ to set the divider current at 7 µA and then calculate R1 using Equation 8.

$$R1 = \left(\frac{V_O}{0.995 \times V_{ref}} - 1\right) \times R2 \quad (8)$$

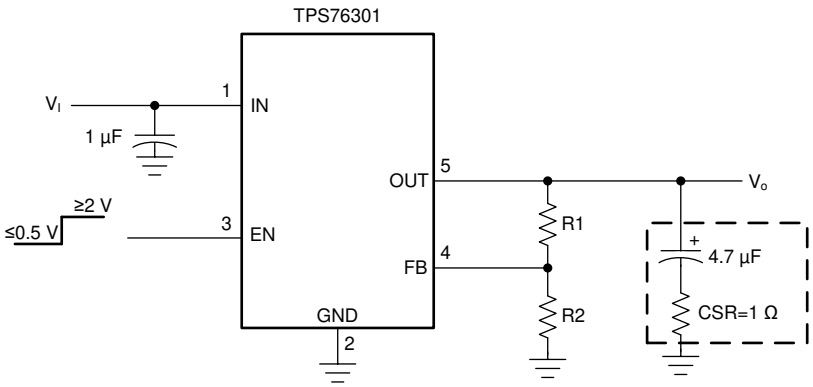


Figure 7-5. TPS76301 Adjustable LDO Regulator Programming

7.2.2.3 Thermal Dissipation

Junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation (P_D). Use Equation 9 to calculate the power dissipation. Multiply P_D by $R_{\theta JA}$ and add the ambient temperature (T_A), as Equation 10 shows, to calculate the junction temperature (T_J).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (9)$$

$$T_J = R_{\theta JA} \times P_D + T_A \quad (10)$$

Equation 11 calculates the maximum ambient temperature. Equation 12 calculates the maximum ambient temperature for typical design applications.

$$T_{A(MAX)} = T_{J(MAX)} - (R_{\theta JA} \times P_D) \quad (11)$$

$$T_{A(MAX)} = 125°C - [167.8°C/W \times (5.3V - 3.3V) \times 0.2A] = 57.88°C \quad (12)$$

7.2.3 Application Curves

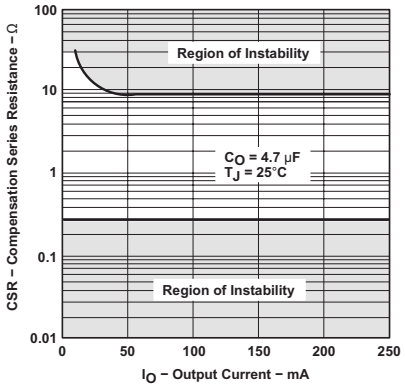


Figure 7-6. Compensation Series Resistance (CSR) vs Output Current (Legacy Chip)

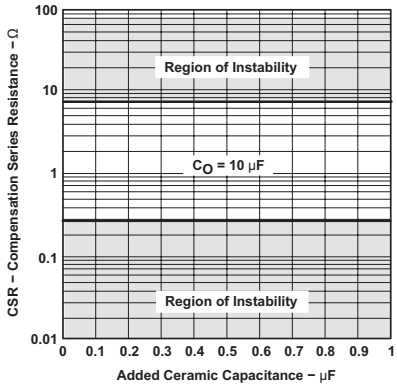


Figure 7-7. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance (Legacy Chip)

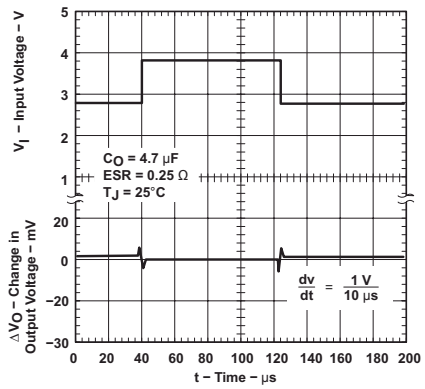
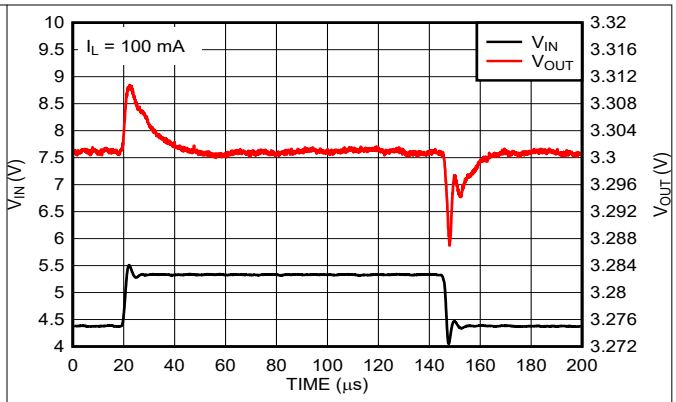
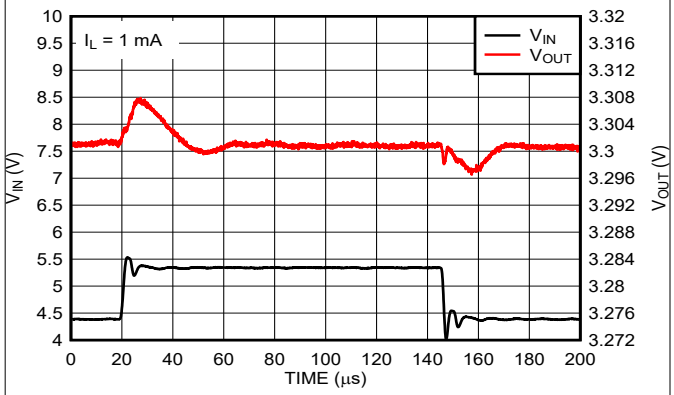


Figure 7-8. TPS76318 Line Transient Response (Legacy Chip)



V_{OUT} = 3.3V, I_L = 100mA

Figure 7-9. Line Transient Response (New Chip)



V_{OUT} = 3.3V, I_L = 1mA

Figure 7-10. Line Transient Response (New Chip)

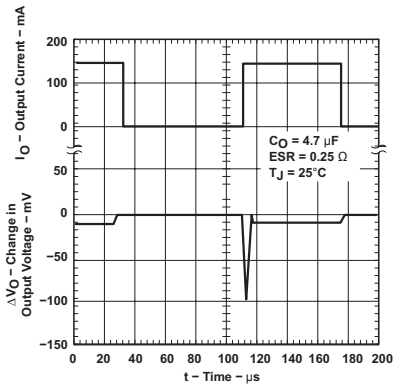
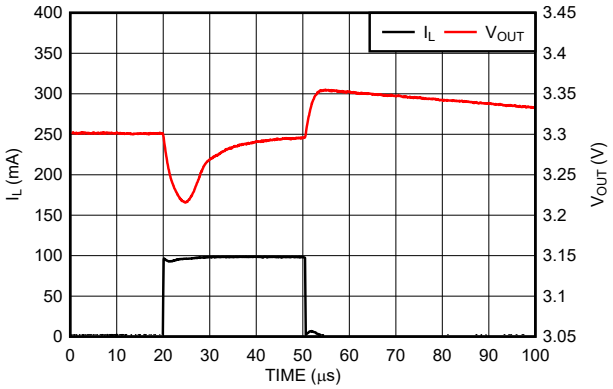


Figure 7-11. TPS76318 Load Transient Response (Legacy Chip)



V_{OUT} = 3.3V, C_{OUT} = 2.2µF

Figure 7-12. Load Transient Response (New Chip)

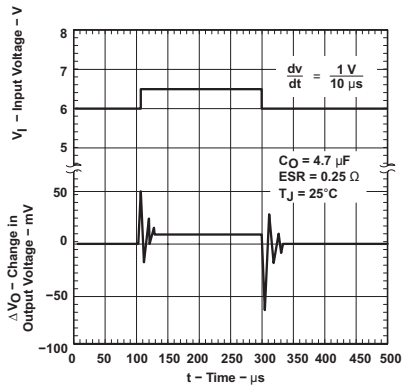


Figure 7-13. TPS76350 Line Transient Response (Legacy Chip)

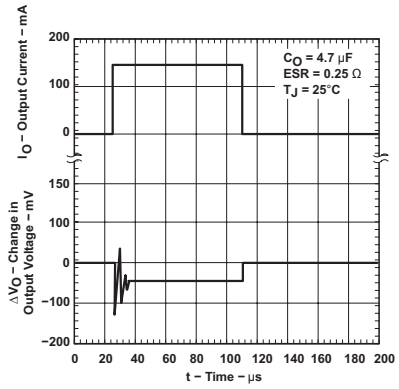
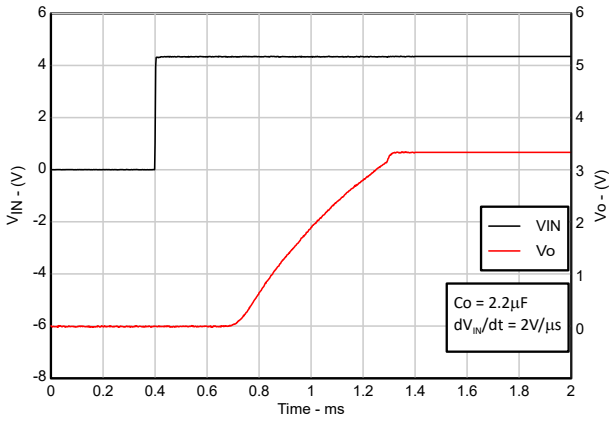
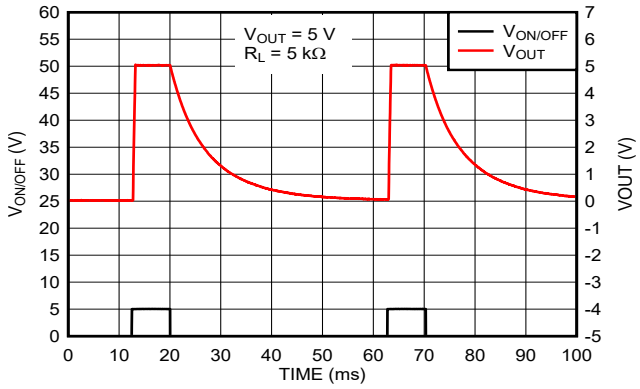


Figure 7-14. TPS76350 Load Transient Response (Legacy Chip)



V_{OUT} = 3.3V, R_L = 3.3kΩ

Figure 7-15. Turn-on Waveform (New Chip)



V_{OUT} = 5V, R_L = 5kΩ

Figure 7-16. Turn-off Waveform (New Chip)

7.3 Power Supply Recommendations

The device is designed to operate with an input supply range of 2.4V to 18V (for new chip). If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance. Connect a low output impedance power supply to the input pin of the TPS763. In order to optimize regulation, see the *Features* section for more information on operation modes and performance features.

7.4 Layout

7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.

7.4.2 Layout Example

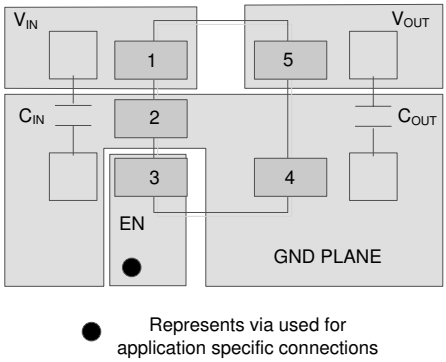


Figure 7-17. Layout Example for the DBV Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT[1]	V_{OUT}
TPS763**xxyyyz** Legacy chip	**xx** is the nominal output voltage (for example, 50 = 5.0V; 33 = 3.3V). 01 indicates adjustable output version. **yyy** is the package designator. **z** is the package quantity. R is for large quantity reel.Fab source on the packaging label, **CSO: SFB**.
TPS763**xxyyyz** New chip	**xx** is the nominal output voltage (for example, 50 = 5.0V; 33 = 3.3V). 01 indicates adjustable output version. **yyy** is the package designator. **z** is the package quantity. R is for large quantity reel.Fab source on the packaging label, **CSO: RFAB**.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *Impact of board layout on LDO thermal performance*

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (September 2019) to Revision K (December 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed entire document to align with current family format	1
• Added differentiation between legacy and new chip information throughout document	1

Changes from Revision I (December 2016) to Revision J (September 2019)	Page
• Changed minimum specification from 4.75V to 4.85V in VO parameter for TPS76350, IO = 1mA to 150mA row in *Electrical Characteristics* table	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76301DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI
TPS76301DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI
TPS76301DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI
TPS76301DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI
TPS76301DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI
TPS76301DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI
TPS76316DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI
TPS76316DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI
TPS76316DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI
TPS76316DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI
TPS76316DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI
TPS76318DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76318DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76318DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76318DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76318DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76318DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76318DBVT1G4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76318DBVT1G4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI
TPS76325DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI
TPS76325DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI
TPS76325DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI
TPS76325DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI
TPS76325DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI
TPS76325DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI
TPS76327DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBCI
TPS76327DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBCI
TPS76327DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBCI
TPS76327DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBCI

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS76327DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBCI
TPS76328DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBDI
TPS76328DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBDI
TPS76328DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBDI
TPS76328DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBDI
TPS76330DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBII
TPS76330DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBII
TPS76330DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBII
TPS76330DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBII
TPS76333DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI
TPS76333DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI
TPS76333DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI
TPS76333DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI
TPS76333DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI
TPS76333DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI
TPS76333DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI
TPS76338DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBFI
TPS76338DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBFI
TPS76338DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBFI
TPS76338DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBFI
TPS76350DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI
TPS76350DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI
TPS76350DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI
TPS76350DBVRG4.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI
TPS76350DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI
TPS76350DBVT.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI
TPS76350DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI
TPS76350DBVTG4.A	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS763 :

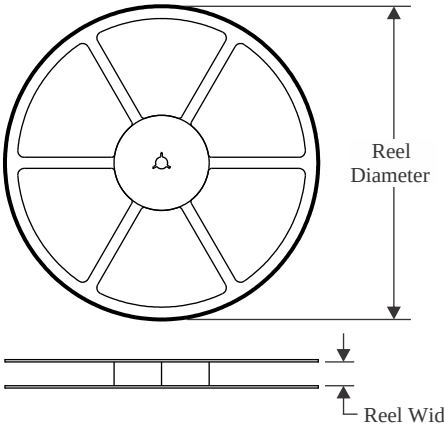
- Automotive : TPS763-Q1

NOTE: Qualified Version Definitions:

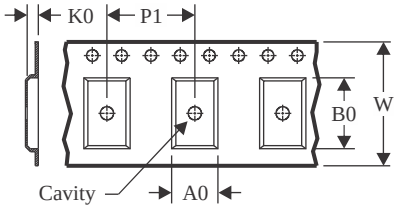
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

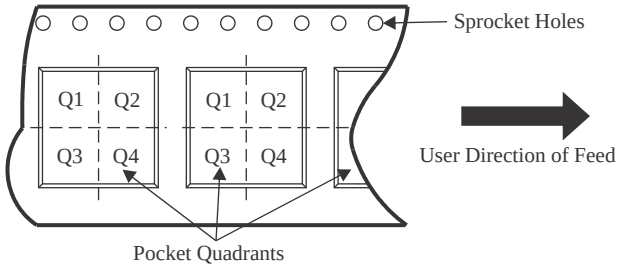


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

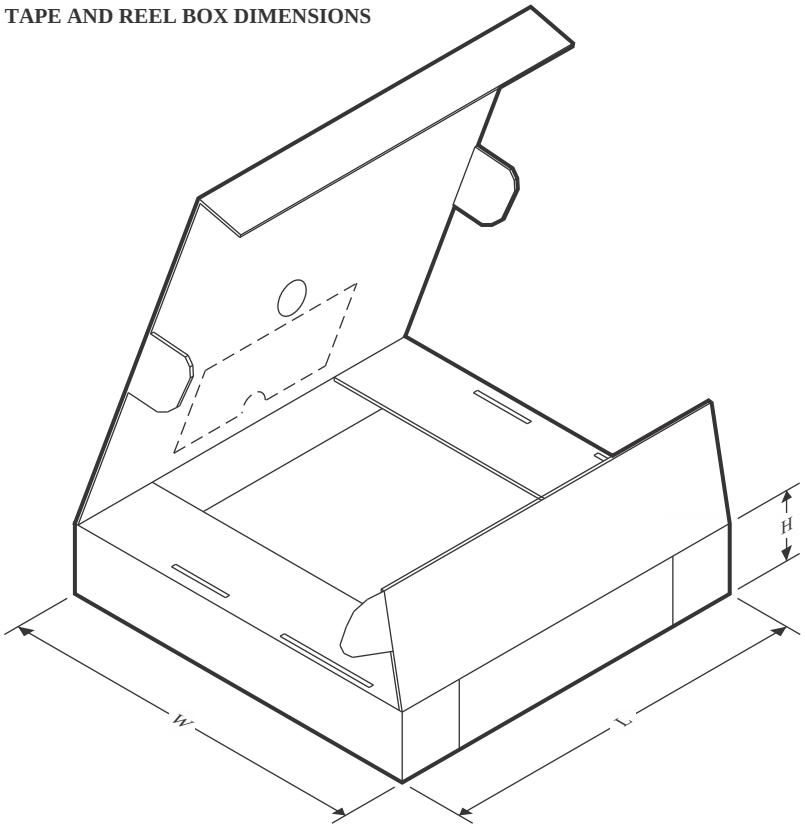


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76301DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76301DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76301DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76316DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76316DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76318DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS76318DBVRG4	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76318DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS76318DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76318DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76318DBVT1G4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76325DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76325DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76325DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76327DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76327DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76328DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76328DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76330DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76330DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76333DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76333DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76333DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76333DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76338DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76338DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76350DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76350DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76350DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS76350DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76301DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76301DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76301DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76316DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76316DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76318DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76318DBVRG4	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS76318DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76318DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76318DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS76318DBVT1G4	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76325DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76325DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76325DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76327DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76327DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76328DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76328DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

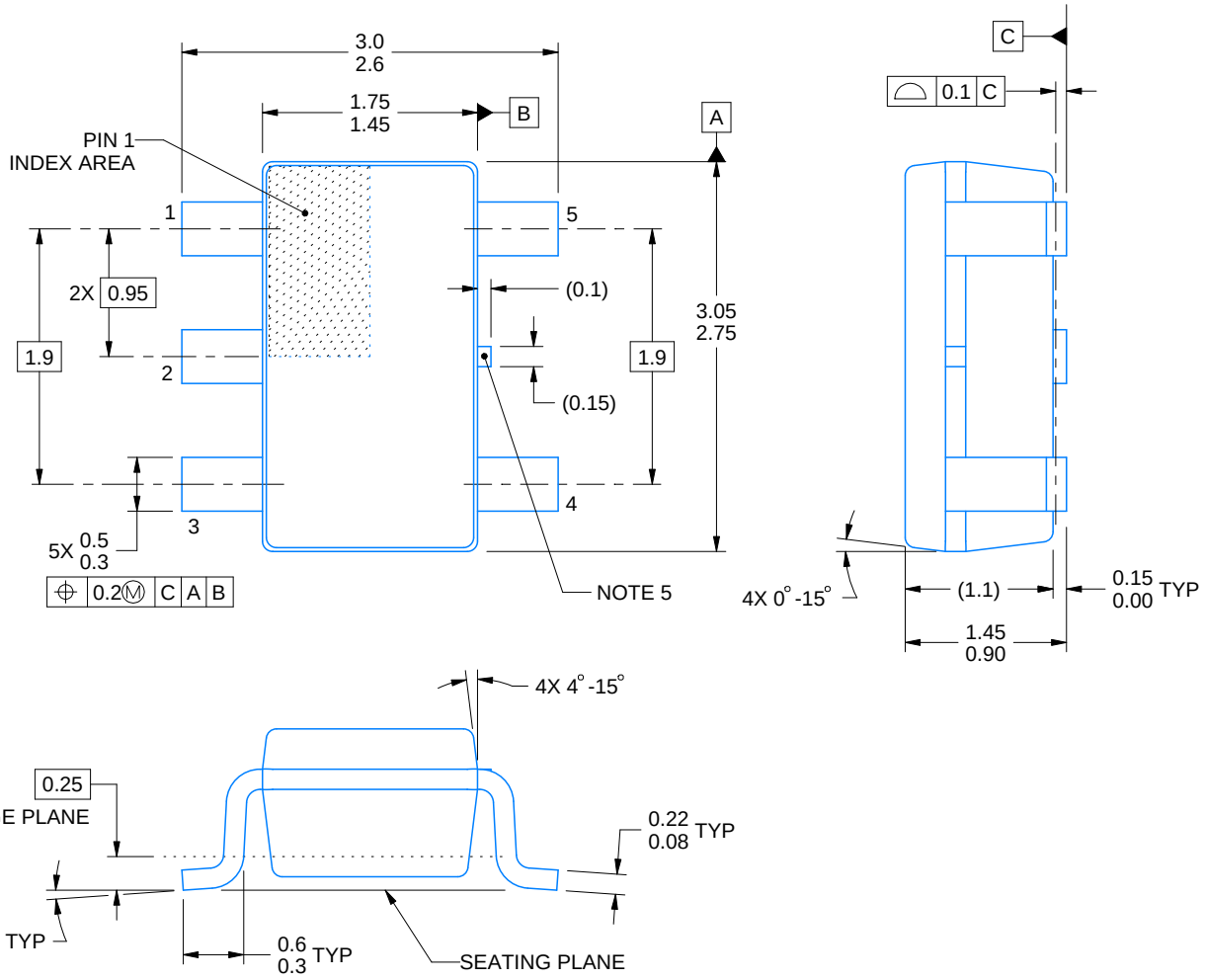
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76330DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76330DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76333DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76333DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76333DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS76333DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76338DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76338DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76350DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76350DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76350DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76350DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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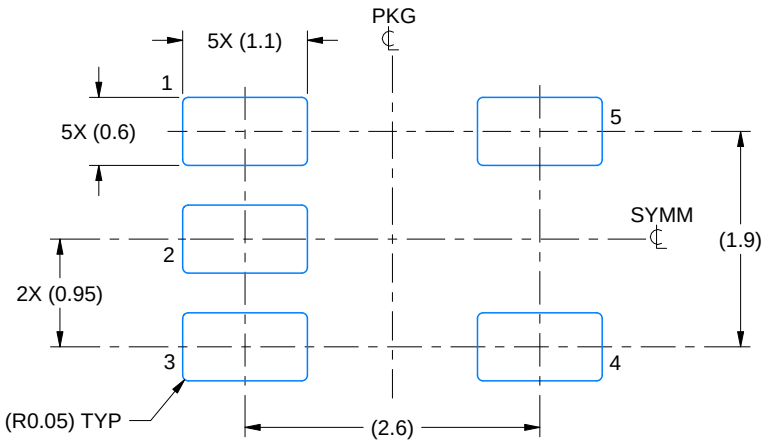
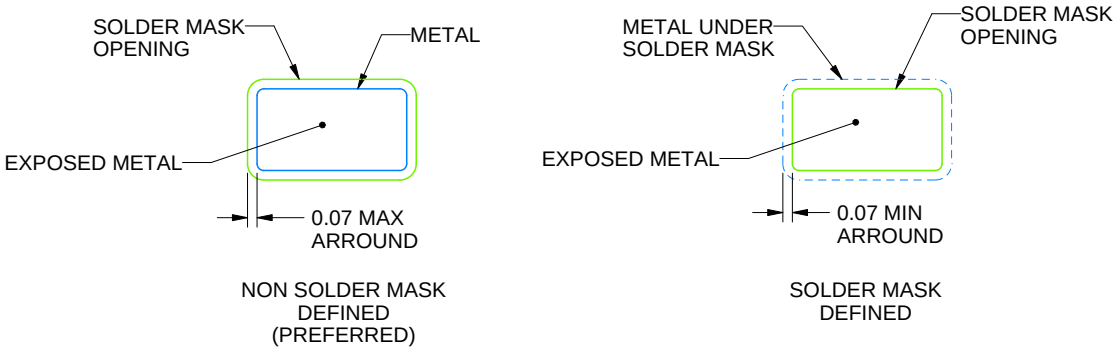
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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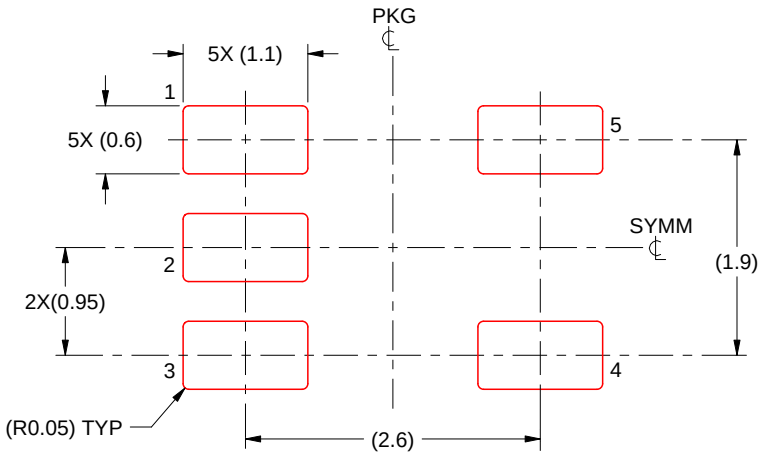
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025