# TPS7A03 Nanopower $I_Q$, 200nA, 200mA, Low-Dropout Voltage Regulator With Fast Transient Response

## 1 Features

- Ultra-low $I_Q$: 200nA (typ), even in dropout
- Shutdown $I_Q$: 3nA (typ)
- Excellent transient response (1mA to 50mA)
  - < 10µs settling time
  - 80mV undershoot
- Packages:
  - 1.0mm × 1.0mm X2SON
  - SOT23-5
  - 0.64mm × 0.64mm DSBGA
- Input voltage range: 1.5V to 6.0V
- Output voltage range: 0.8V to 5.0V (fixed)
- Output accuracy: 1.5% over temperature
- Smart enable pulldown
- Very low dropout:
  - 270mV (max) at 200mA ($V_{OUT}$ = 3.3V)
- Stable with a 1µF or larger capacitor

## 2 Applications

- Wearables electronics
- Thermostats, smoke and heat detectors
- Gas, heat, and water meters
- Blood glucose monitors and pulse oximeters
- Residential circuit breakers and fault indicators
- Building security and video surveillance devices
- EPOS card readers

## 3 Description

The TPS7A03 is an ultra-small, ultra-low quiescent current low-dropout linear regulator (LDO) that sources 200mA with excellent transient performance.

The TPS7A03, with an ultra-low $I_Q$ of 200nA, is designed specifically for applications where very-low quiescent current is a critical parameter. This device maintains low $I_Q$ consumption even in dropout mode to further increase battery life. When in shutdown or disabled mode, the device consumes ultra-low, 3nA $I_Q$ that helps increase battery shelf life. The TPS7A03 has an output range of 0.8V to 5.0V available in 50mV steps to support the lower core voltages of modern microcontrollers (MCUs).

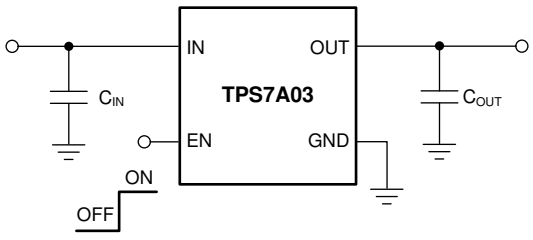
The TPS7A03 features a smart enable circuit with an internally controlled pulldown resistor that keeps the LDO disabled even when the EN pin is left floating. This circuit also helps minimize the external components used to pulldown the EN pin. This circuit also helps minimize the current drawn through the external pulldown circuit when the device is enabled.

The TPS7A03 is fully specified for $T_J$ = –40°C to +125°C operation.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TPS7A03 | DQN (X2SON, 4) | 1mm × 1mm |
| | YCH (DSBGA, 4) | 0.637mm × 0.637mm |
| | DBV (SOT-23, 5) | 2.9mm × 2.8mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application Circuit**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features**....1
**2 Applications**....1
**3 Description**....1
**4 Pin Configuration and Functions**....3
**5 Specifications**....4
5.1 Absolute Maximum Ratings....4
5.2 ESD Ratings....4
5.3 Recommended Operating Conditions....5
5.4 Thermal Information....5
5.5 Electrical Characteristics....6
5.6 Switching Characteristics....7
5.7 Typical Characteristics....8
**6 Detailed Description**....18
6.1 Overview....18
6.2 Functional Block Diagram....18
6.3 Feature Description....19
6.4 Device Functional Modes....21
**7 Application and Implementation**....23
7.1 Application Information....23
7.2 Typical Application....26
7.3 Power Supply Recommendations....27
7.4 Layout....27
**8 Device and Documentation Support**....29
8.1 Device Support....29
8.2 Receiving Notification of Documentation Updates....29
8.3 Support Resources....29
8.4 Trademarks....29
8.5 Electrostatic Discharge Caution....29
8.6 Glossary....29
**9 Revision History**....30
**10 Mechanical, Packaging, and Orderable Information**....30


Copyright © 2026 Texas Instruments Incorporated

# 4 Pin Configuration and Functions

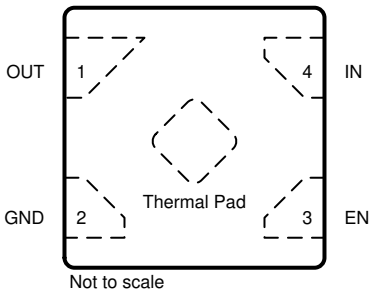



**Figure 4-1. DQN Package, 1mm × 1mm, 4-Pin X2SON (Top View)**

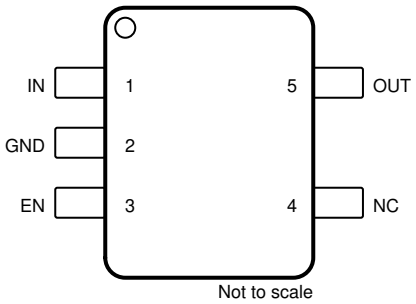



**Figure 4-2. DBV Package, 5-Pin SOT-23 (Top View)**

**Table 4-1. Pin Functions: DQN, DBV**

| PIN | | | I/O[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | DQN | DBV | | |
| EN | 3 | 3 | Input | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low or floating this pin disables the device. This pin features an internal pulldown resistor, which is disconnected when EN is driven high externally and the device has started up. |
| GND | 2 | 2 | — | Ground pin. Connect this pin to ground on the board. |
| IN | 4 | 1 | Input | Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground. See the *Recommended Operating Conditions* table. Place the input capacitor as close to the input of the device as possible. |
| NC | — | 4 | — | No connect pin. This pin is not internally connected. Connect to ground or leave floating. |
| OUT | 1 | 5 | Output | Regulated output pin. A 0.5µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table. |
| Thermal pad | | — | — | Connect the thermal pad to a large-area ground plane. The thermal pad is internally connect to ground. |

(1) NC = No internal connection.

Copyright © 2026 Texas Instruments Incorporated

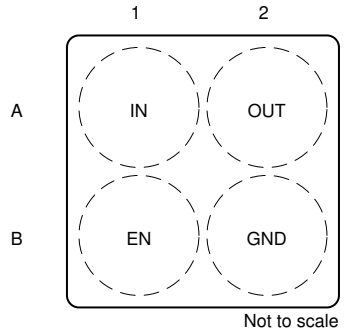



**Figure 4-3. YCH Package, 4-Pin DSBGA, 0.35mm Pitch (Top View)**

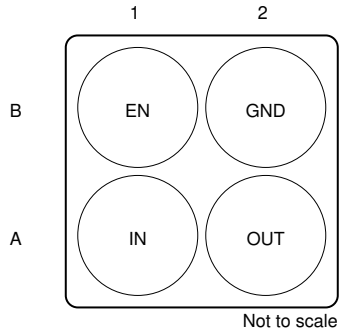



**Figure 4-4. YCH Package, 4-Pin DSBGA, 0.35mm Pitch (Bottom View)**

**Table 4-2. Pin Functions: YCH**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| YCH | NAME | | |
| A1 | IN | Input | Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground. See the *Recommended Operating Conditions* table. Place the input capacitor as close to input of the device as possible. |
| A2 | OUT | Output | Regulated output pin. A 0.5µF or greater effective capacitance is required from OUT to ground for stability. For best transient response, use a 1µF or larger ceramic capacitor from OUT to ground. Place the output capacitor as close to output of the device as possible; see the *Recommended Operating Conditions* table. |
| B1 | EN | Input | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low or floating this pin disables the device. This pin features an internal pulldown resistor, which is disconnected when EN is driven high externally and the device has started up. |
| B2 | GND | — | Ground pin. Connect this pin to ground and the thermal pad. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | $V_{IN}$ | –0.3 | 6.5 | V |
| | $V_{EN}$ | –0.3 | 6.5 | |
| | $V_{OUT}$ | –0.3 | $V_{IN}$ + 0.3 or 5.5(2) | |
| Current | Maximum output | Internally limited | | A |
| Temperature | Operating junction, $T_J$ | –40 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum is $V_{IN}$ + 0.3 V or 5.5 V, whichever is smaller.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.


Copyright © 2026 Texas Instruments Incorporated

## 5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 1.5 | | 6.0 | V |
| $V_{EN}$ | Enable voltage | 0 | | 6.0 | V |
| $V_{OUT}$ | Output voltage | 0.8 | | 5.0 | V |
| $I_{OUT}$ | Output current | 0 | | 200 | mA |
| $C_{IN}$ | Input capacitor | | 1 | | µF |
| $C_{OUT}$ | Output capacitor(1) (2) | 1 | 1 | 22 | µF |
| $F_{EN}$ | EN toggle frequency | | | 10 | kHz |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) Effective output capacitance of 0.5 µF minimum required for stability.
(2) 22 µF is the maximum derated capacitance that can be used for stability.

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TPS7A03 | | | UNIT |
|---|---|---|---|---|---|
| | | DQN (X2SON) | DBV (SOT-23-5) | YCH (DSBGA) | |
| | | 4 PINS | 5 PINS | 4 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 179.1 | 181.9 | 201.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 137.6 | 53.0 | 2.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 116.3 | 88.1 | 67.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 6.1 | 27.1 | 1.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 116.3 | 52.7 | 67.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | 112.3 | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2026 Texas Instruments Incorporated

## 5.5 Electrical Characteristics

Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Nominal accuracy | $T_J$ = 25°C, $V_{OUT}$ ≥ 1.5 V, 1 µA[3] ≤ $I_{OUT}$ ≤ 1 mA | | –1 | | 1 | % |
| | | $T_J$ = 25°C; $V_{OUT}$ < 1.5 V | | –15 | | 15 | mV |
| | Accuracy over temperature | $V_{OUT}$ ≥ 1.5 V | $T_J$ = –40°C to +125°C | –1.5 | | 1.5 | % |
| | | $V_{OUT}$ < 1.5 V | | –20 | | 20 | mV |
| $\Delta V_{OUT}(\Delta V_{IN})$ | Line regulation | $V_{OUT(nom)}$ + 0.5 V ≤ $V_{IN}$ ≤ 6.0 V[1] | $T_J$ = –40°C to +125°C | | | 5 | mV |
| $\Delta V_{OUT}(\Delta I_{OUT})$ | Load regulation[2] | 1 mA ≤ $I_{OUT}$ ≤ 200 mA, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V[1] | $T_J$ = –40°C to +85°C | | 20 | 38 | mV |
| | | | $T_J$ = –40°C to +125°C | | | 50 | |
| $I_{GND}$ | Ground current | $I_{OUT}$ = 0 mA | $T_J$ = 25°C | | 200 | 250 | nA |
| | | | $T_J$ = –40°C to +85°C | | | 300 | |
| $I_{GND}/I_{OUT}$ | Ground current vs load current | 20 µA ≤ $I_{OUT}$ < 1 mA | $T_J$ = 25°C | | 1 | | % |
| | | 1 mA ≤ $I_{OUT}$ ≤ 100 mA | | | 0.25 | | |
| | | $I_{OUT}$ ≥ 100 mA | | | 0.15 | | |
| $I_{GND(DO)}$ | Ground current in dropout[3] | $I_{OUT}$ = 0 mA, $V_{IN}$ = 95% x $V_{OUT\ (NOM)}$ | $T_J$ = 25°C | | 220 | | nA |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ = 0 V, 1.5 V ≤ $V_{IN}$ ≤ 5.0 V, $T_J$ = 25°C | | | 3 | 10 | nA |
| $I_{CL}$ | Output current limit | $V_{OUT}$ = 90% × $V_{OUT(nom)}$ | $V_{OUT}$ < 2.5V, $V_{IN}$ = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 1.0 V | 240 | 450 | 750 | mA |
| | | | $V_{OUT}$ ≥ 2.5V, $V_{IN}$ = $V_{OUT(nom)}$ + $V_{DO(max)}$ + 0.5 V | 240 | 450 | 750 | mA |
| $I_{SC}$ | Short-circuit current limit | $V_{OUT}$ = 0 V | | | 65 | | mA |
| $V_{DO}$ | Dropout voltage[4] | $T_J$ = –40°C to +85°C | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | | 1050 | mV |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | | 790 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | | 650 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | | 490 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | | 400 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | | 310 | |
| | | | 3.3 V ≤ $V_{OUT}$ ≤ 5.0 V | | | 270 | |
| | | $T_J$ = –40°C to +125°C | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | | 1100 | |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | | 850 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | | 700 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | | 560 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | | 450 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | | 360 | |
| | | | 3.3 V ≤ $V_{OUT}$ ≤ 5.0 V | | | 310 | |
| PSRR | Power-supply rejection ratio | f = 1 kHz, $I_{OUT}$ = 30 mA | | | 55 | | dB |
| $V_N$ | Output voltage noise | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 0.8 V, $I_{OUT}$ = 30 mA | | | 130 | | $\mu V_{RMS}$ |
| $V_{UVLO}$ | UVLO threshold | $V_{IN}$ rising | | 1.23 | 1.3 | 1.47 | V |
| | | $V_{IN}$ falling | | 1.0 | 1.12 | 1.41 | |
| $V_{UVLO(HYST)}$ | UVLO hysteresis | $V_{IN}$ hysteresis | | | 180 | | mV |


Copyright © 2026 Texas Instruments Incorporated

## 5.5 Electrical Characteristics (continued)

Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{EN(HI)}$ | EN pin logic high voltage | | 1.1 | | | V |
| $V_{EN(LOW)}$ | EN pin logic low voltage | | | | 0.3 | V |
| $I_{EN}$ | EN pin leakage current | $V_{EN}$ = $V_{IN}$ = 6.0 V | | 10 | | nA |
| $R_{EN(PULLDOWN)}$ | Smart enable pulldown resistor | $V_{EN}$ = 0.3 V | | 500 | | KΩ |
| $R_{PULLDOWN}$ | Pulldown resistor | $V_{IN}$ = 3.3 V, device disabled | | 60 | | Ω |
| $T_{SD(shutdown)}$ | Thermal shutdown temperature | Shutdown, temperature increasing | | 170 | | °C |
| $T_{SD(reset)}$ | Thermal shutdown reset temperature | Reset, temperature decreasing | | 145 | | |

(1) $V_{IN}$ = 2.0 V for $V_{OUT}$ ≤ 1.5 V.
(2) Load Regulation is normalized to the output voltage at $I_{OUT}$ = 1 mA.
(3) Specified by design
(4) Dropout is measured by ramping $V_{IN}$ down until $V_{OUT}$ = $V_{OUT\ (nom)}$ x 95%, with $I_{OUT}$ = 200 mA.

## 5.6 Switching Characteristics

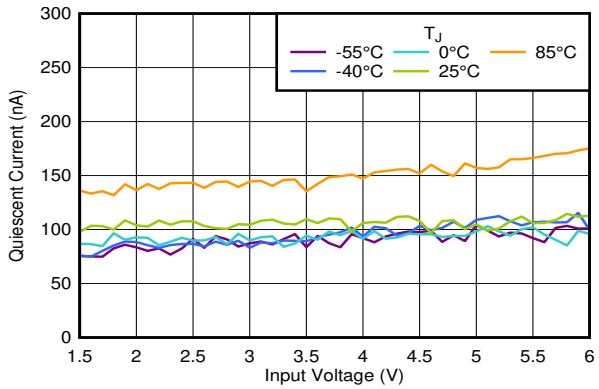
Specified at $T_J$ = –40°C to +125°C, $V_{IN}$ = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted). Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{STR}$ | Start-up time | From EN assertion to $V_{OUT}$ = 90% × $V_{OUT(nom)}$ | 0.8V ≤ $V_{OUT}$ ≤ 1.5 V | | 500 | 800 | µs |
| | | | 1.5V < $V_{OUT}$ ≤ 3.0 V | | 750 | 1200 | |
| | | | 3.0V < $V_{OUT}$ ≤ 5.0 V | | 1200 | 1600 | |

Copyright © 2026 Texas Instruments Incorporated

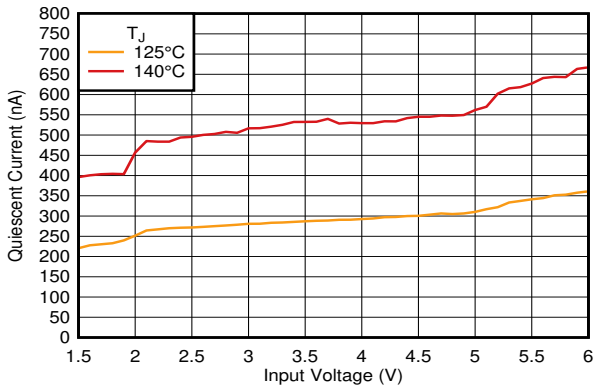
## 5.7 Typical Characteristics

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



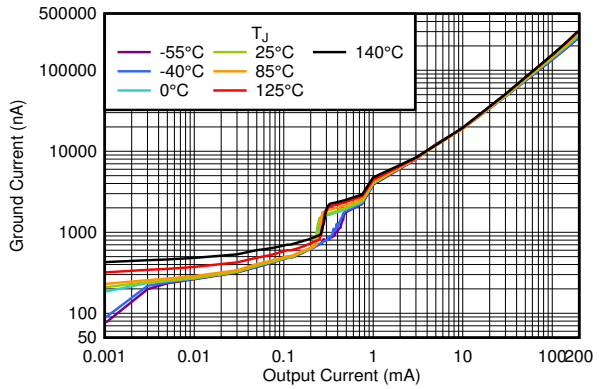

$V_{OUT}$ = 1.8V, $V_{IN}$ = $V_{EN}$ = 2.3V

**Figure 5-1. $I_Q$ vs $V_{IN}$ and Temperature**



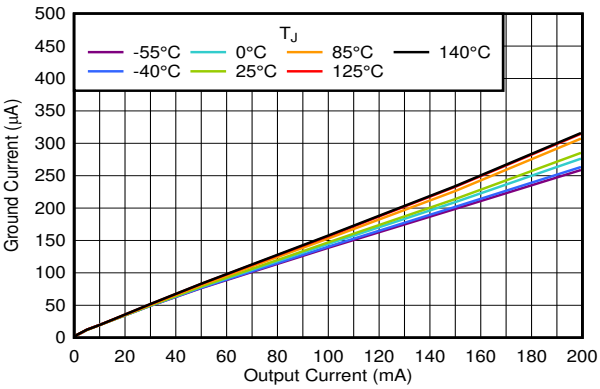

$I_{OUT}$ = 0mA, $V_{EN}$ = $V_{IN}$

**Figure 5-2. $I_Q$ vs $V_{IN}$ and Temperature**



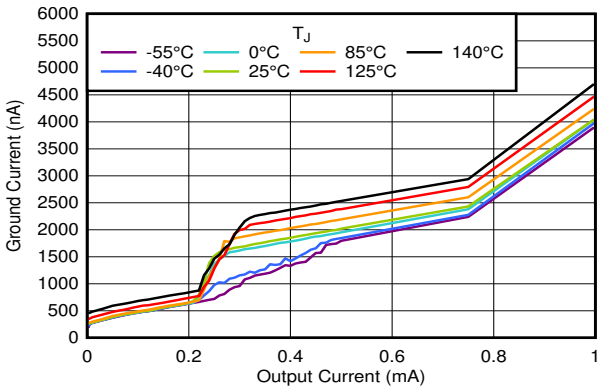

$V_{OUT}$ = 1.8V, $V_{IN}$ = $V_{EN}$ = 2.3V

**Figure 5-3. $I_Q$ vs $I_{OUT}$ and Temperature Up to 200mA**



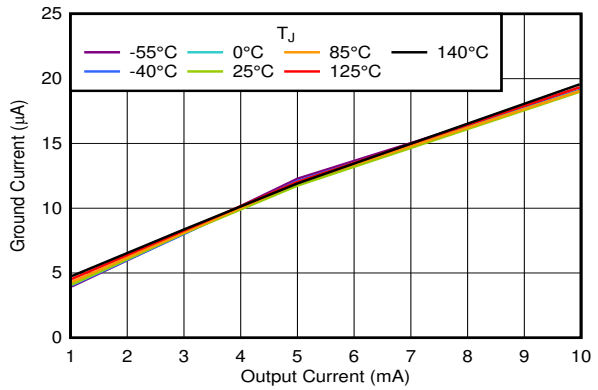

$V_{OUT}$ = 1.8V, $V_{IN}$ = $V_{EN}$ = 2.3V

**Figure 5-4. $I_Q$ vs $I_{OUT}$ and Temperature Up to 200mA**




$V_{OUT}$ = 1.8V, $V_{IN}$ = $V_{EN}$ = 2.3V

**Figure 5-5. $I_Q$ vs $I_{OUT}$ and Temperature Up to 1mA**



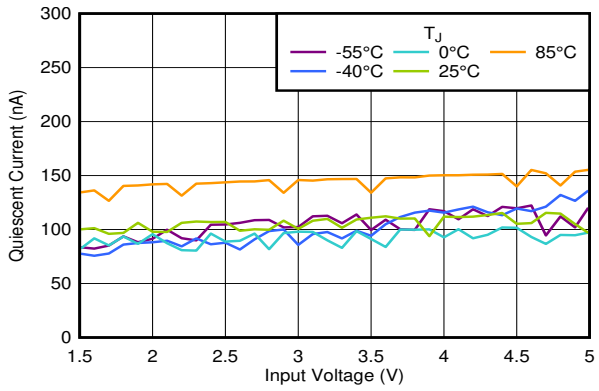

$V_{OUT}$ = 1.8V, $V_{IN}$ = $V_{EN}$ = 2.3V

**Figure 5-6. $I_Q$ vs $I_{OUT}$ and Temperature for 1mA to 10mA**


Copyright © 2026 Texas Instruments Incorporated

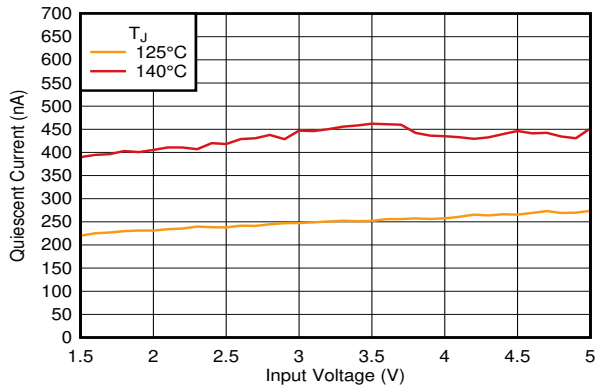
## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



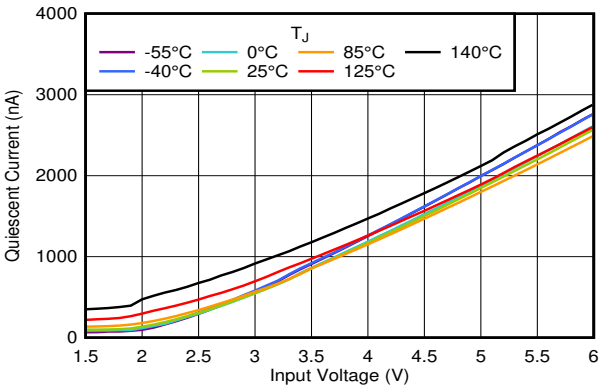

$V_{OUT}$ = 5.0V, $V_{IN}$ = $V_{EN}$

**Figure 5-7. $I_Q$ in Dropout vs $V_{IN}$ and Temperature**



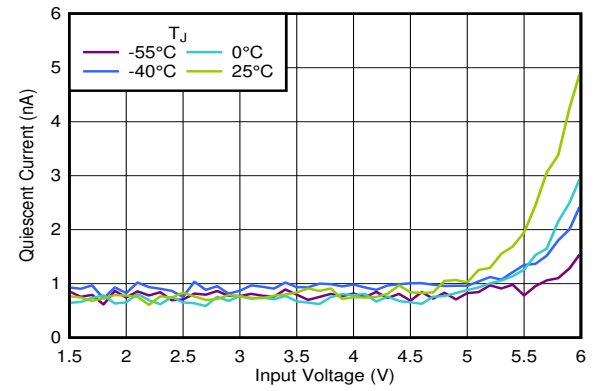

$V_{OUT}$ = 5.0V, $V_{IN}$ = $V_{EN}$

**Figure 5-8. $I_Q$ in Dropout vs $V_{IN}$ and Temperature**



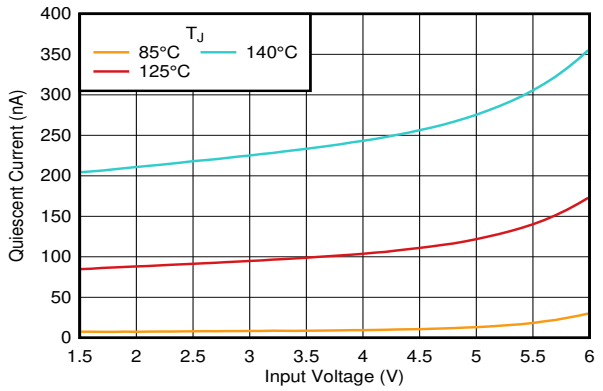

$I_{OUT}$ = 0mA, $V_{EN}$ = 1.1V

**Figure 5-9. $I_Q$ vs $V_{IN}$ and Temperature**



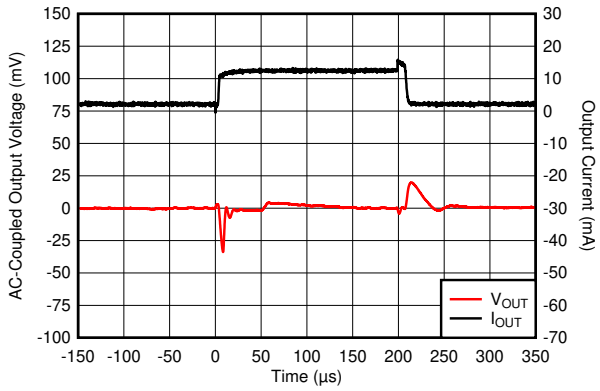

$V_{EN}$ = 0V

**Figure 5-10. $I_{SHDN}$ vs $V_{IN}$ and Temperature**




$V_{EN}$ = 0V

**Figure 5-11. $I_{SHDN}$ vs $V_{IN}$ and Temperature**



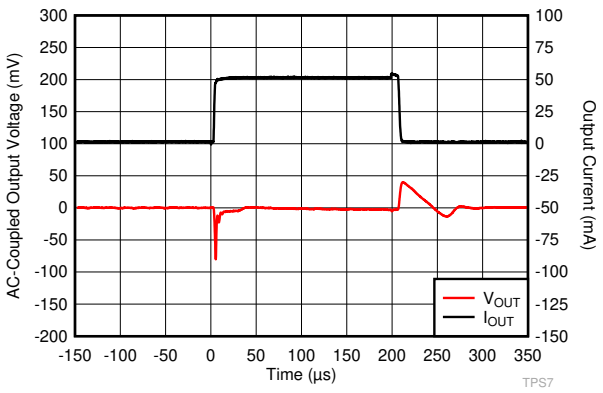

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-12. $I_{OUT}$ Transient From 1mA to 10mA**

Copyright © 2026 Texas Instruments Incorporated

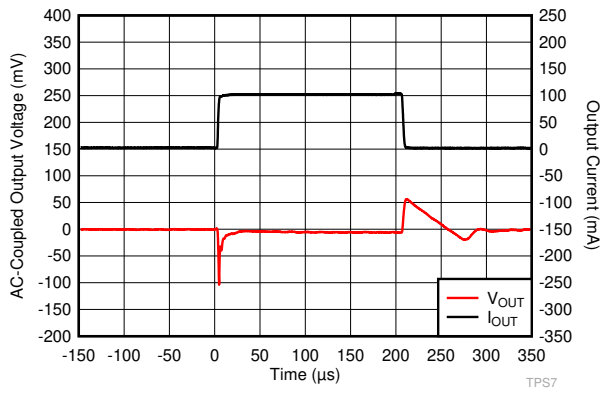
## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



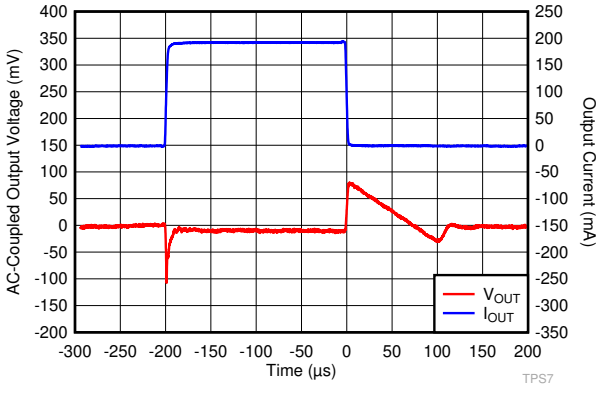

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-13. $I_{OUT}$ Transient From 1mA to 50mA**



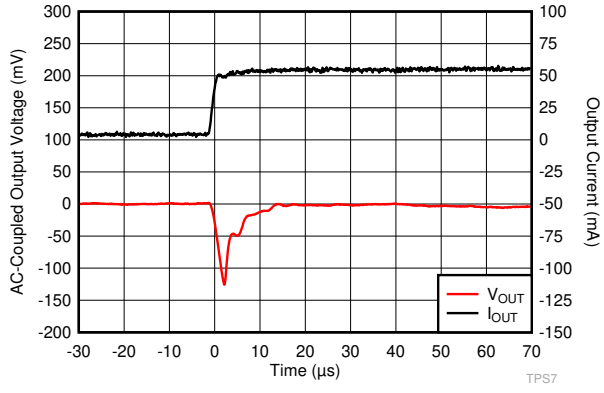

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-14. $I_{OUT}$ Transient From 1mA to 100mA**



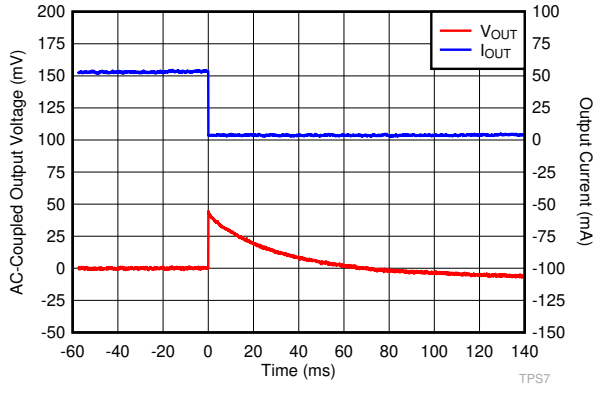

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-15. $I_{OUT}$ Transient From 1mA to 200mA**



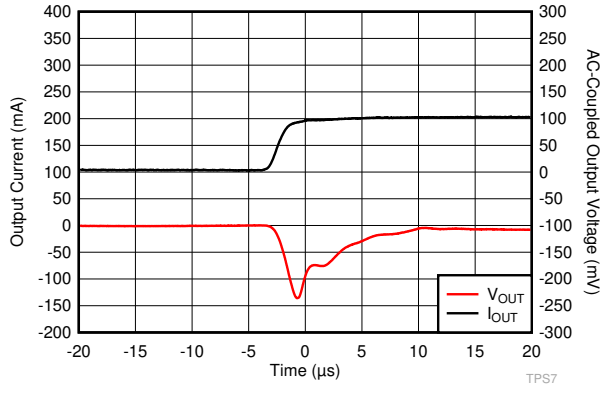

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-16. $I_{OUT}$ Transient From 0mA to 50mA**




$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-17. $I_{OUT}$ Transient From 50mA to 0mA**



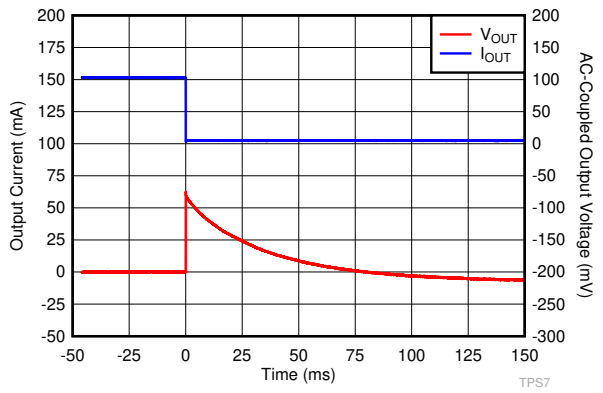

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-18. $I_{OUT}$ Transient From 0mA to 100mA**


Copyright © 2026 Texas Instruments Incorporated

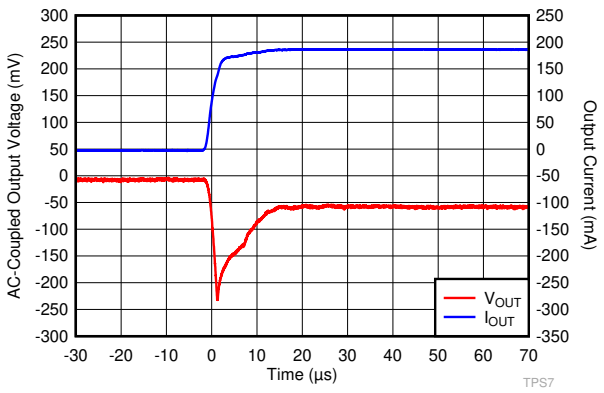
## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



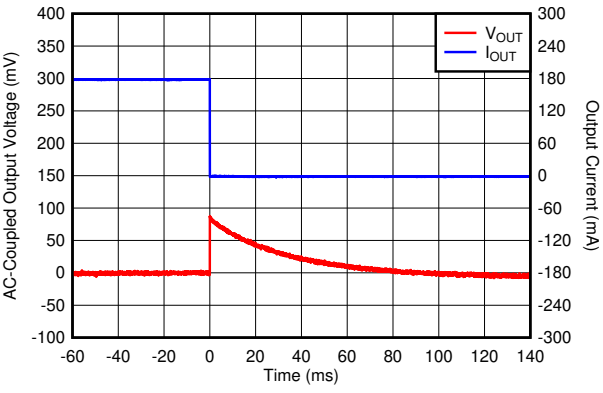

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-19. $I_{OUT}$ Transient From 100mA to 0mA**



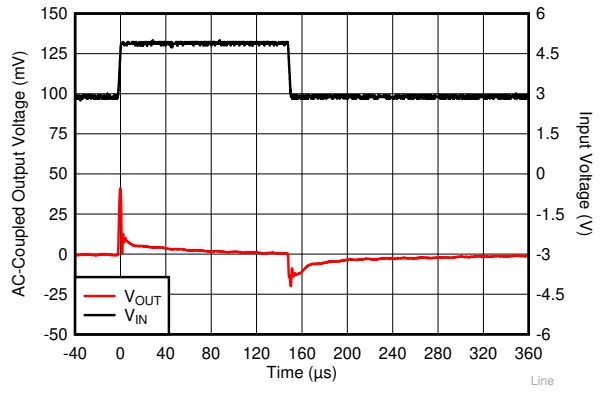

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-20. $I_{OUT}$ Transient From 0mA to 200mA**



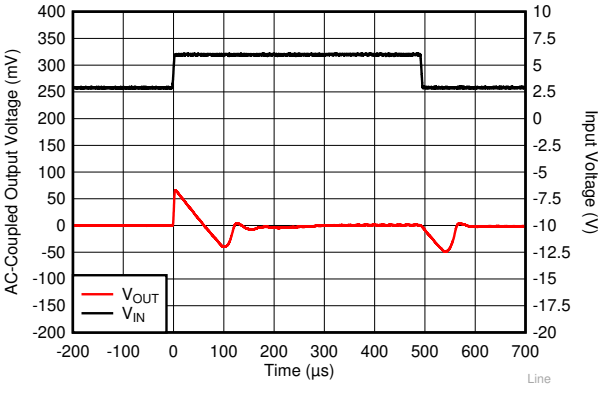

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF, $t_r$ = $t_f$ = 1µs

**Figure 5-21. $I_{OUT}$ Transient From 200mA to 0mA**



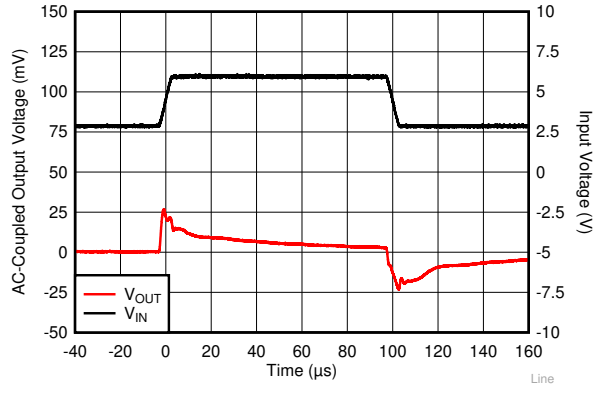

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 200mA, $C_{OUT}$ = 1µF, slew rate = 1V/µs

**Figure 5-22. $V_{IN}$ Transient From 2.8V to 4.8V**




$V_{OUT}$ = 1.8V, $I_{OUT}$ = 1mA, $C_{OUT}$ = 1µF, slew rate = 1V/µs

**Figure 5-23. $V_{IN}$ Transient From 2.8V to 6.0V**



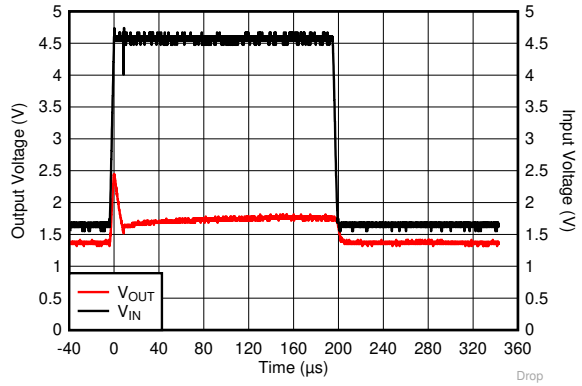

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 200mA, $C_{OUT}$ = 1µF, slew rate = 1V/µs

**Figure 5-24. $V_{IN}$ Transient From 2.8V to 6.0V**

Copyright © 2026 Texas Instruments Incorporated

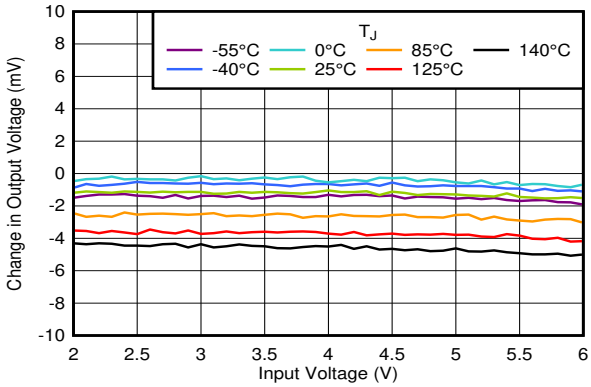
## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



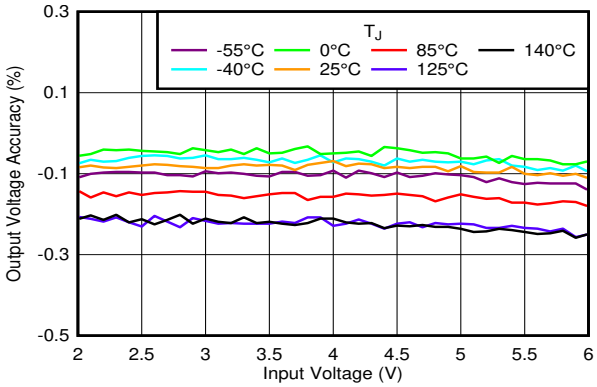

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 100mA, $C_{OUT}$ = 1µF, slew rate = 1V/µs

**Figure 5-25. $V_{IN}$ Transient From 1.5V to 4.5V**



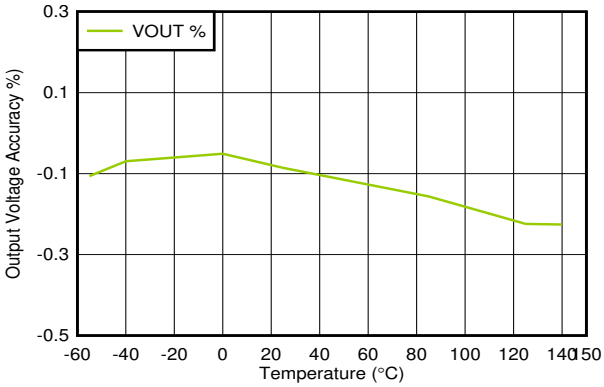

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 1mA

**Figure 5-26. Line Regulation vs $V_{IN}$ and Temperature**



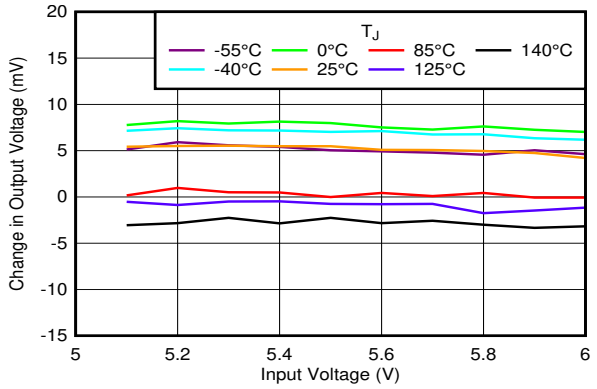

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 1mA

**Figure 5-27. Output Accuracy vs $V_{IN}$ and Temperature**



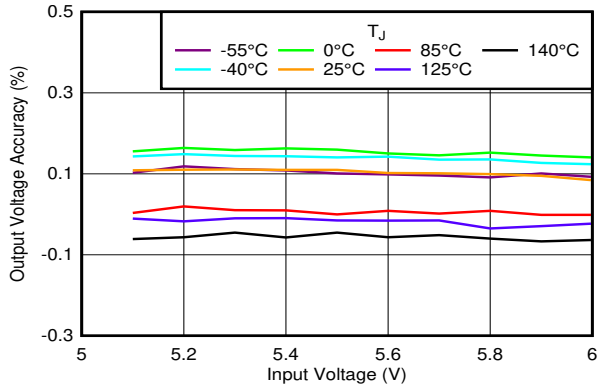

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 1mA

**Figure 5-28. Output Accuracy vs Temperature**




$V_{OUT}$ = 5.0V, $I_{OUT}$ = 1mA

**Figure 5-29. Line Regulation vs $V_{IN}$ and Temperature**



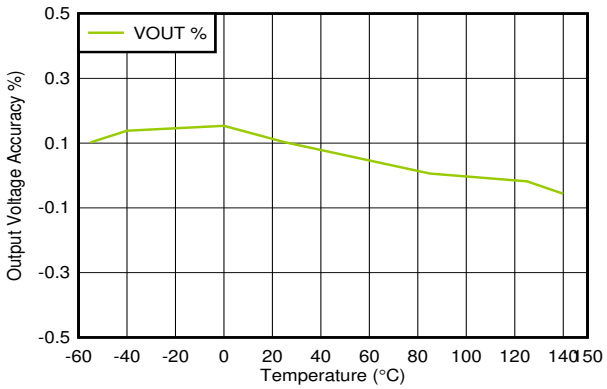

$V_{OUT}$ = 5.0V, $I_{OUT}$ = 1mA

**Figure 5-30. Output Accuracy vs $V_{IN}$ and Temperature**


Copyright © 2026 Texas Instruments Incorporated

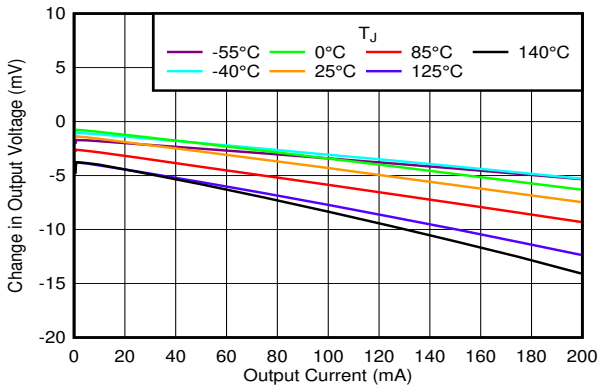
## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



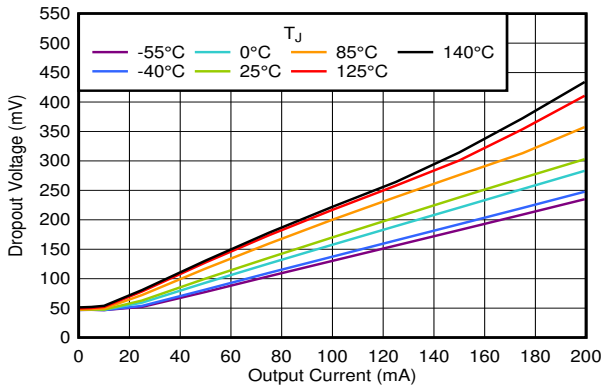

$V_{OUT}$ = 5.0V, $I_{OUT}$ = 1mA

**Figure 5-31. Output Accuracy vs Temperature**



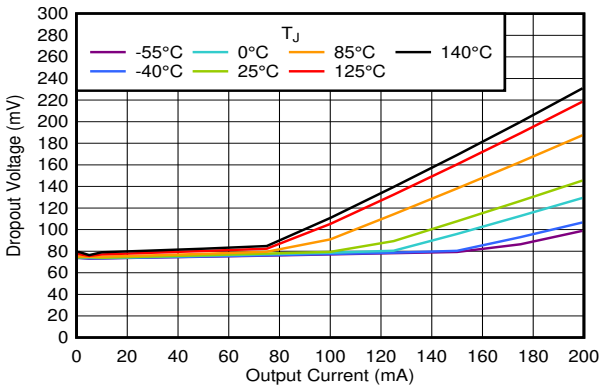

$V_{OUT}$ = 1.8V

**Figure 5-32. Load Regulation vs $V_{IN}$ and Temperature**



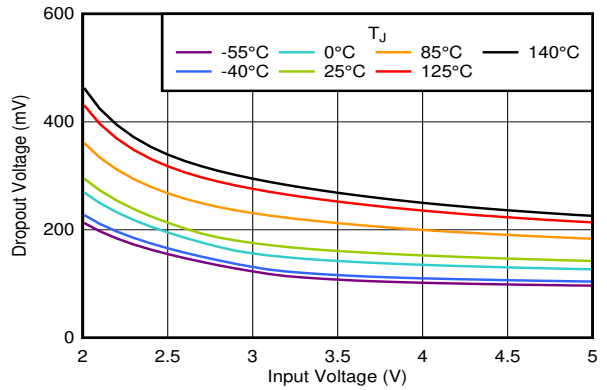

$V_{OUT}$ = 1.8V

**Figure 5-33. Dropout vs $I_{OUT}$ and Temperature**



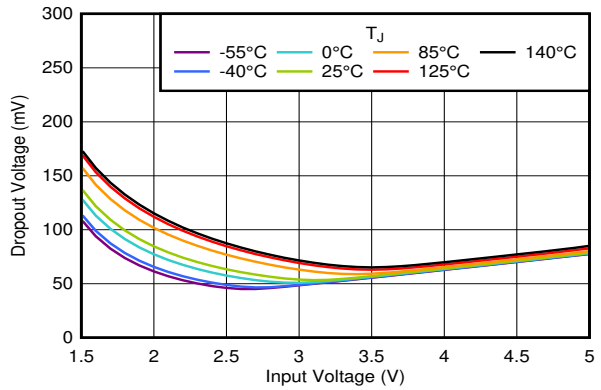

$V_{OUT}$ = 5.0V

**Figure 5-34. Dropout vs $I_{OUT}$ and Temperature**




$I_{OUT}$ = 200mA

**Figure 5-35. Dropout vs $V_{IN}$ and Temperature**




$I_{OUT}$ = 50mA

**Figure 5-36. Dropout vs $V_{IN}$ and Temperature**

Copyright © 2026 Texas Instruments Incorporated

## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)

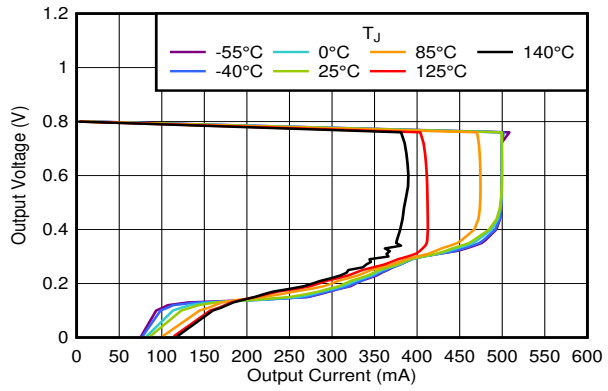



**Figure 5-37. Foldback Current Limit vs $I_{OUT}$ and Temperature**

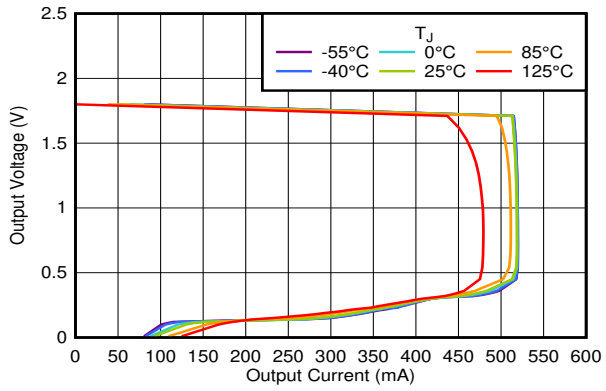



**Figure 5-38. Foldback Current Limit vs $I_{OUT}$ and Temperature**

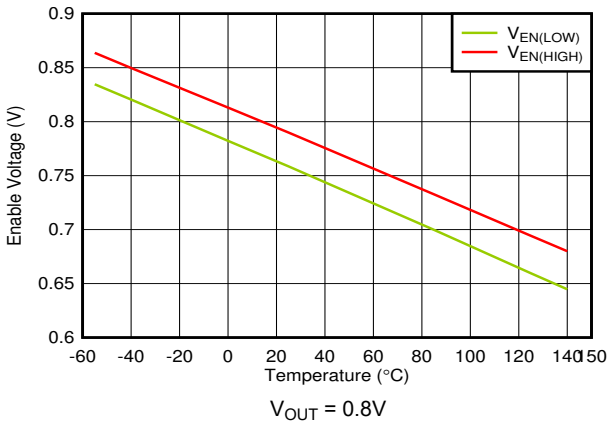



**Figure 5-39. EN High and Low Threshold vs Temperature**

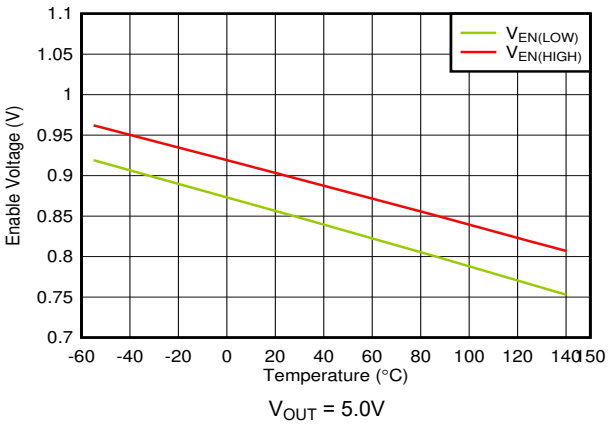



**Figure 5-40. EN High and Low Threshold vs Temperature**

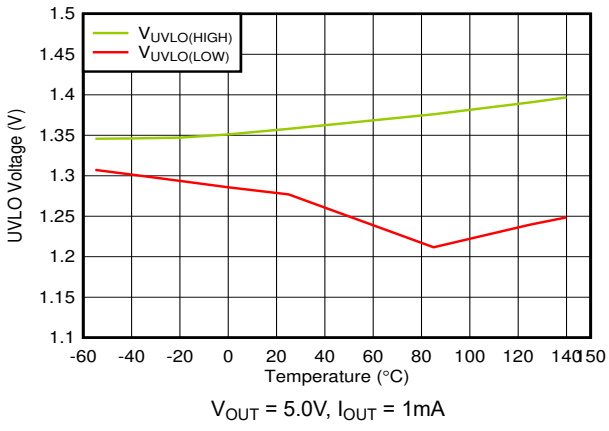



**Figure 5-41. UVLO Rising and Falling Threshold vs Temperature**

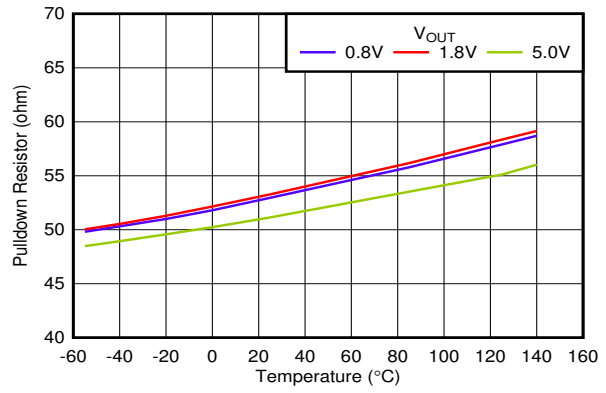



**Figure 5-42. Pulldown Resistor vs Temperature and $V_{OUT}$**


Copyright © 2026 Texas Instruments Incorporated

## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)

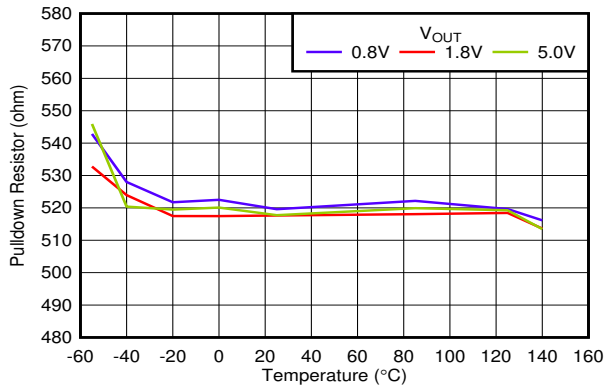
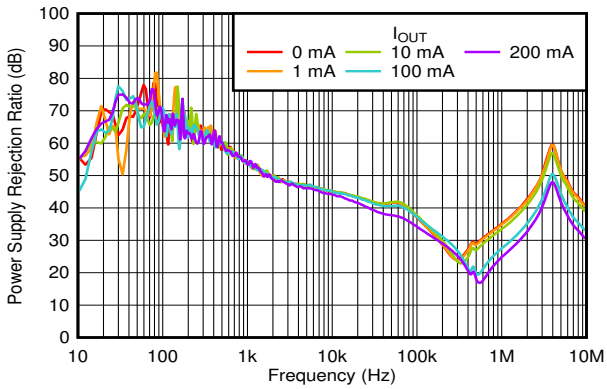
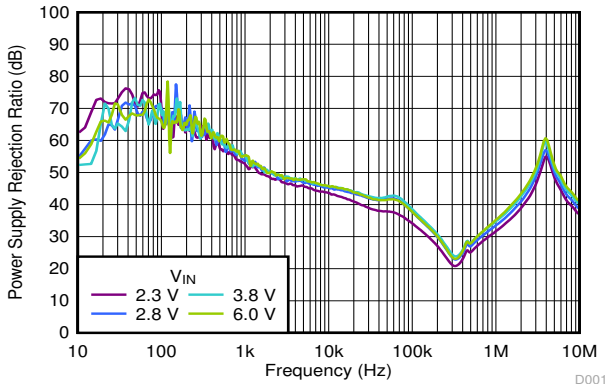



**Figure 5-43. Smart Enable Pulldown Resistor vs Temperature and $V_{OUT}$**



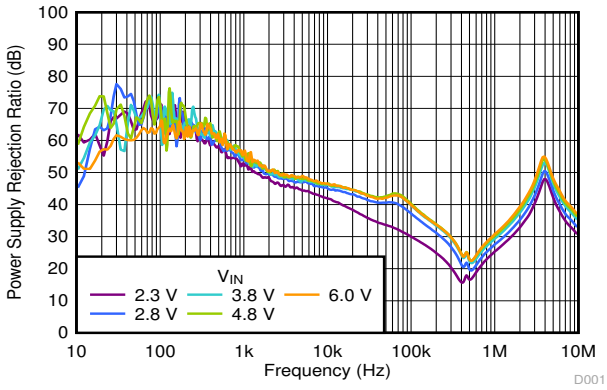

$V_{IN}$ = 2.8V, $V_{OUT}$ = 1.8V, $C_{OUT}$ = 1µF

**Figure 5-44. PSRR vs Frequency and $I_{OUT}$**



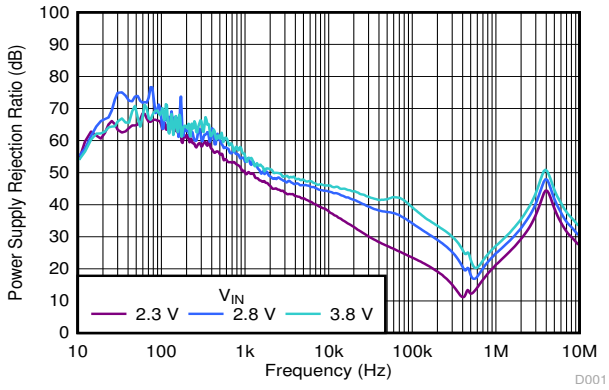

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 10mA, $C_{OUT}$ = 1µF

**Figure 5-45. PSRR vs Frequency and $V_{IN}$**



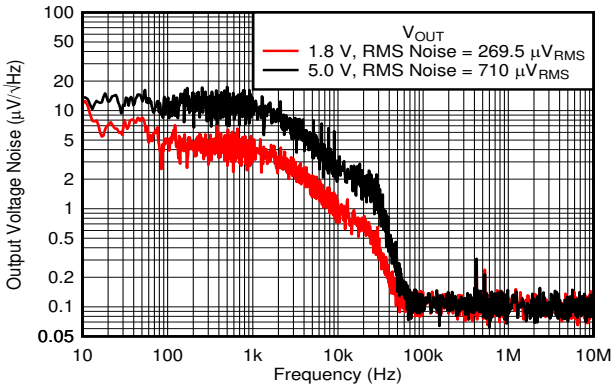

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 100mA, $C_{OUT}$ = 1µF

**Figure 5-46. PSRR vs Frequency and $V_{IN}$**




$V_{OUT}$ = 1.8V, $I_{OUT}$ = 200mA, $C_{OUT}$ = 1µF

**Figure 5-47. PSRR vs Frequency and $V_{IN}$**



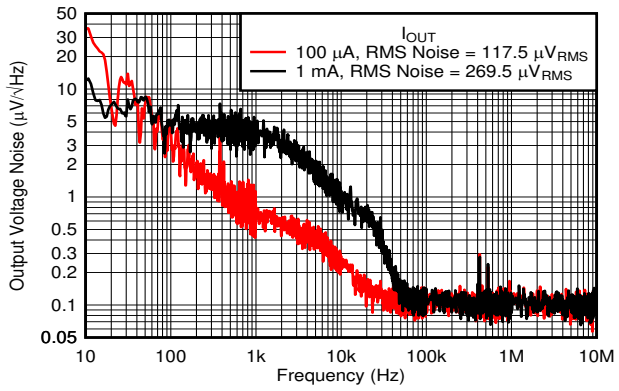

$V_{IN}$ = $V_{OUT}$ + 1.0V, $I_{OUT}$ = 1mA, $C_{OUT}$ = 1µF

**Figure 5-48. Output Noise vs Frequency and $V_{OUT}$**

Copyright © 2026 Texas Instruments Incorporated

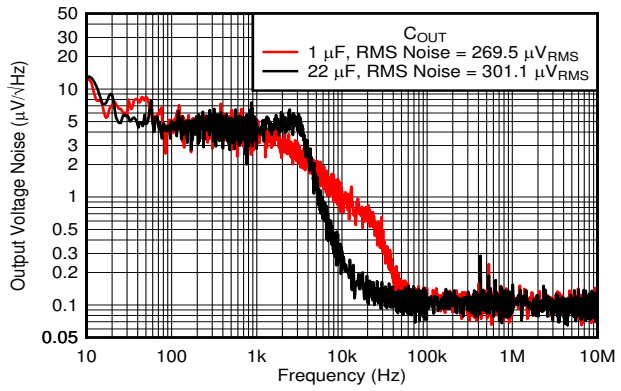
## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



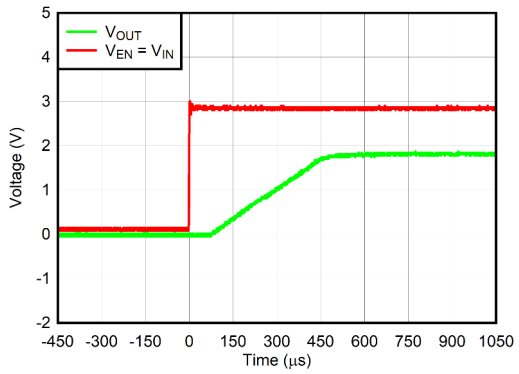

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $C_{OUT}$ = 1µF

**Figure 5-49. Output Noise vs Frequency and $I_{OUT}$**



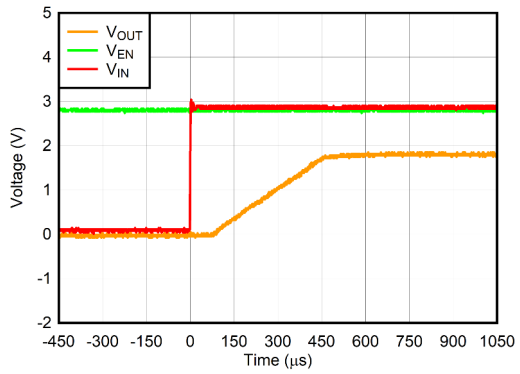

$V_{OUT}$ = 1.8V, $V_{IN}$ = 2.8V, $I_{OUT}$ = 1mA

**Figure 5-50. Output Noise vs Frequency and $C_{OUT}$**



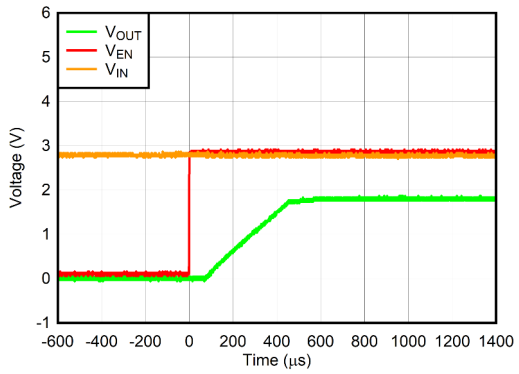

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 200mA, $C_{OUT}$ = 1µF

**Figure 5-51. Start-Up With $V_{EN}$ = $V_{IN}$**



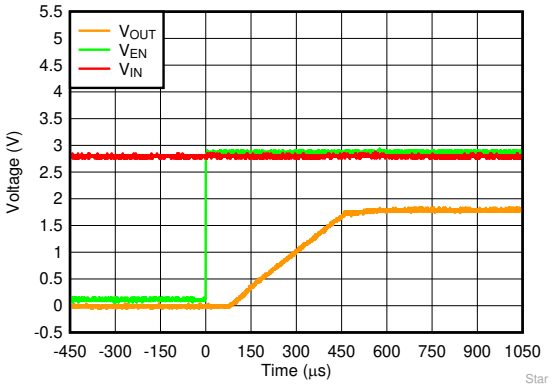

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 200mA, $C_{OUT}$ = 1µF

**Figure 5-52. Start-Up With $V_{EN}$ Before $V_{IN}$**




$V_{OUT}$ = 1.8V, $I_{OUT}$ = 200mA, $C_{OUT}$ = 1µF

**Figure 5-53. Start-Up With $V_{EN}$ After $V_{IN}$**



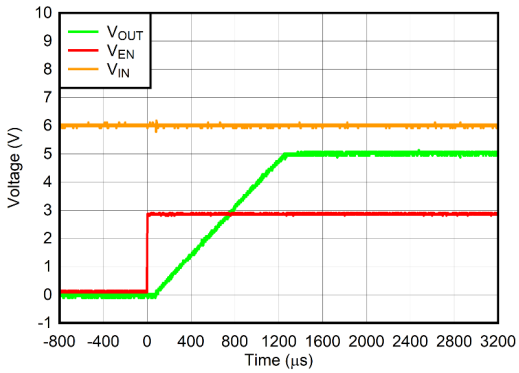

$V_{OUT}$ = 1.8V, $I_{OUT}$ = 0mA, $C_{OUT}$ = 1µF

**Figure 5-54. Start-Up With $V_{EN}$ After $V_{IN}$**


Copyright © 2026 Texas Instruments Incorporated

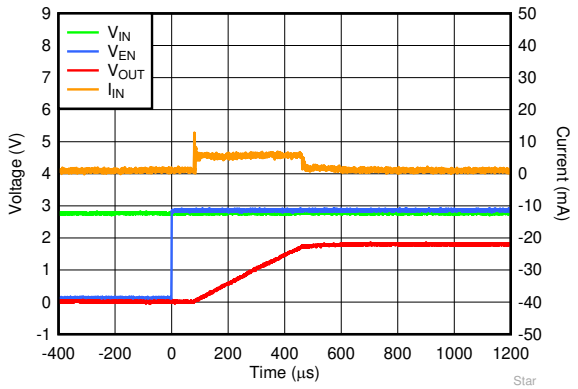
## 5.7 Typical Characteristics (continued)

at operating temperature range ($T_J$ = –40°C to +125°C), $V_{IN}$ = $V_{OUT(nom)}$ + 0.5V or 2.0V (whichever is greater), $I_{OUT}$ = 1mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1µF (unless otherwise noted)



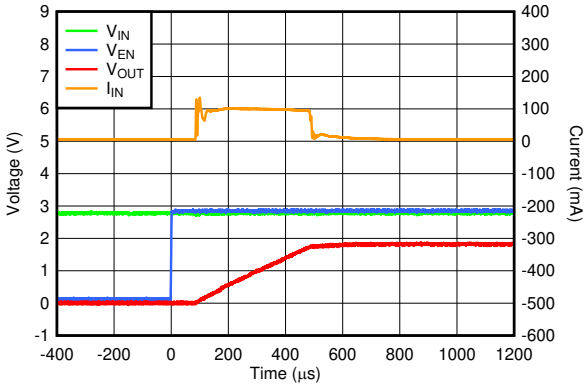

$V_{OUT}$ = 5.0V, $I_{OUT}$ = 200mA, $C_{OUT}$ = 1µF

**Figure 5-55. Start-Up With $V_{EN}$ After $V_{IN}$**




$V_{OUT}$ = 1.8V, $I_{OUT}$ = 0mA

**Figure 5-56. Start-Up Inrush Current With $C_{OUT}$ = 1µF**




$V_{OUT}$ = 1.8V, $I_{OUT}$ = 0mA

**Figure 5-57. Start-Up Inrush Current With $C_{OUT}$= 22µF**

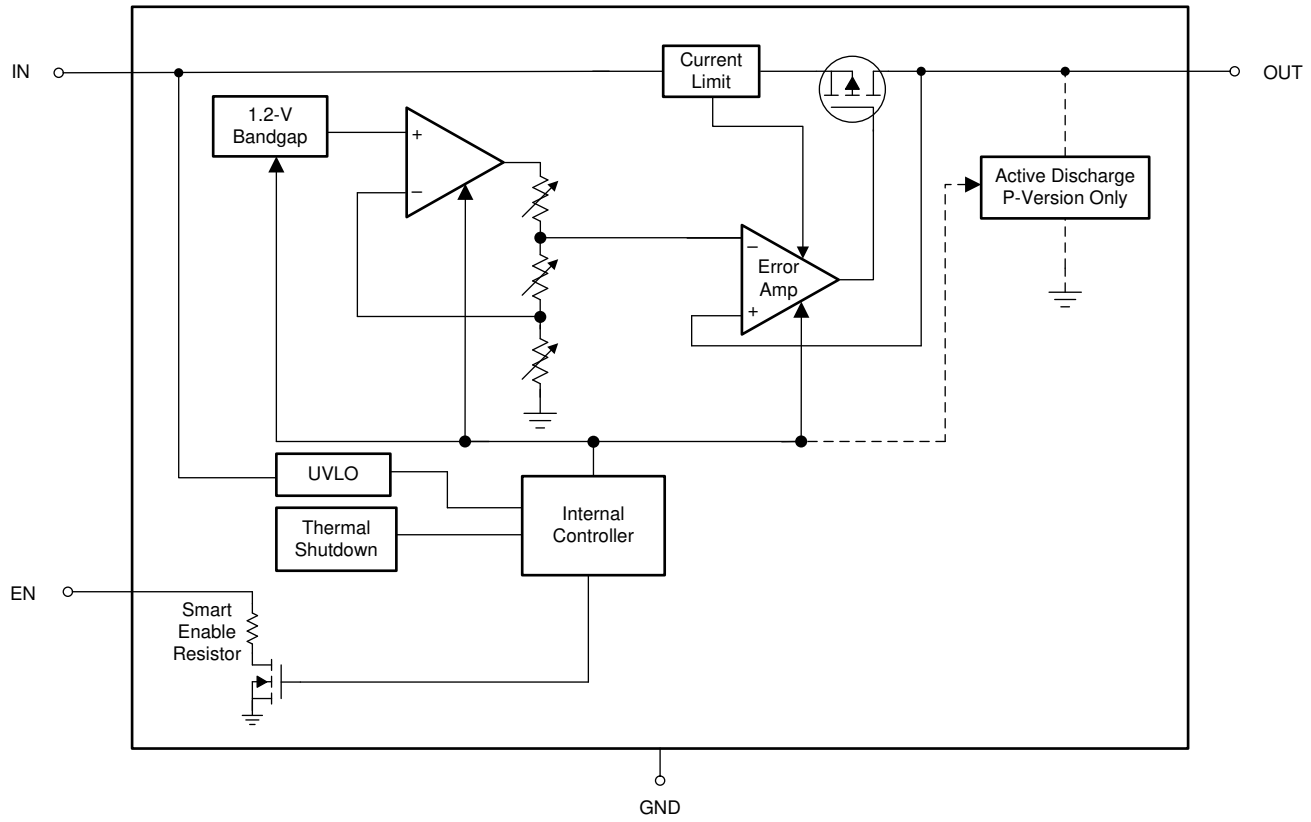
# 6 Detailed Description

## 6.1 Overview

The TPS7A03 is a ultra-low $I_Q$ linear voltage regulator optimized for excellent transient performance. These characteristics make the device designed for most battery-powered applications.

This low-dropout linear regulator (LDO) offers active discharge, foldback current limit, shutdown, and thermal protection capability.

## 6.2 Functional Block Diagram





Copyright © 2026 Texas Instruments Incorporated

## 6.3 Feature Description

### 6.3.1 Excellent Transient Response

The TPS7A03 includes several innovative circuits to ensure excellent transient response. Dynamic biasing increases the $I_Q$ for a short duration during transients to extend the closed-loop bandwidth and improve the output response time to transients.

Adaptive biasing increases the $I_Q$ as the DC load current increases, extending the bandwidth of the loop. The response time across the output voltage range is constant because a buffered reference topology is used, which keeps the control loop in unity gain at any output voltage.

These features give the device a wide loop bandwidth during transients that ensures excellent transient response while maintaining low $I_Q$ in steady-state conditions.

### 6.3.2 Active Discharge (P-Version Only)

The device has an internal pulldown MOSFET that connects a $R_{PULLDOWN}$ resistor to ground when the device is disabled to actively discharge the output voltage. The active discharge circuit is activated by the enable pin or by the undervoltage lockout (UVLO).

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed. Reverse current potentially flows from the output to the input. This reverse current flow potentially causes damage to the device. Limit reverse current to no more than 5% of the device rated current for a short period of time.

### 6.3.3 Low $I_Q$ in Dropout

In most LDOs the $I_Q$ significantly increases when the device is placed into dropout, which is especially true for low $I_Q$ LDOs. The TPS7A03 helps to reduce the battery discharge by detecting when the device is operating in dropout conditions and maintaining a low $I_Q$.

### 6.3.4 Smart Enable

The enable (EN) input polarity is active high. The output voltage is enabled when the voltage of the enable input is greater than $V_{EN(HI)}$ and disabled when the enable input voltage is less than $V_{EN(LOW)}$. If independent control of the output voltage is not needed, connect EN to IN.

This device has a smart enable circuit to reduce quiescent current. When the voltage on the enable pin is driven above $V_{EN(HI)}$, as listed in the *Electrical Characteristics* table, the device is enabled and the smart enable internal pulldown resistor ($R_{EN(PULLDOWN)}$) is disconnected. When the enable pin is floating, the $R_{EN(PULLDOWN)}$ is connected and pulls the enable pin low to disable the device. The $R_{EN(PULLDOWN)}$ value is listed in the *Electrical Characteristics* table.

This device has an internal pulldown circuit that activates when the device is disabled to actively discharge the output voltage.

### 6.3.5 Dropout Voltage

Dropout voltage ($V_{DO}$) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current ($I_{RATED}$), where the pass transistor is fully on. $I_{RATED}$ is the maximum $I_{OUT}$ listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

Copyright © 2026 Texas Instruments Incorporated

### 6.3.6 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 0.5V.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

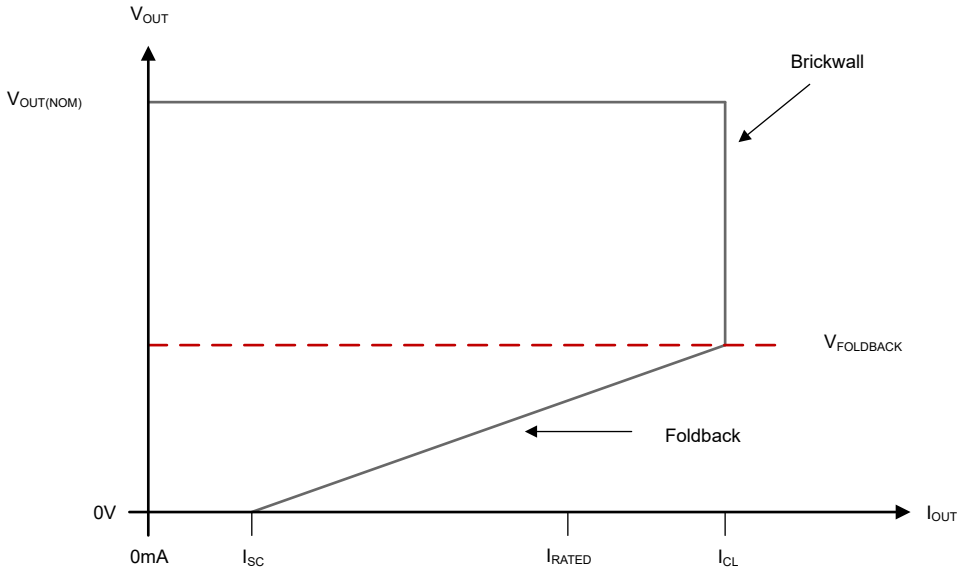



**Figure 6-1. Foldback Current Limit**

### 6.3.7 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.


Copyright © 2026 Texas Instruments Incorporated

### 6.3.8 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature ($T_J$) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short. Thus, the device cycles on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up is high from large $V_{IN} – V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

## 6.4 Device Functional Modes

### 6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 6-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 6.4.3 Dropout Operation

The device operates in dropout mode when the input voltage is lower than the nominal output voltage plus the specified dropout voltage. However, make sure all other conditions are met for normal operation. In this mode, the output voltage tracks the input voltage. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. Because of this operation, the transient performance of the device becomes significantly degraded. Line or load transients in dropout results in large output-voltage deviations.

When the device is in a steady dropout state, the pass transistor is driven into the ohmic or triode region. This state is defined as when the device is in dropout, directly after being in a normal regulation state, but *not* during start-up. During dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$. When the input voltage returns to a value ≥ $V_{OUT(NOM)} + V_{DO}$, the output voltage overshoots for a short period of time. During this time, the device pulls the pass transistor back into the linear region. $V_{OUT(NOM)}$ is the nominal output voltage and $V_{DO}$ is the dropout voltage.

Copyright © 2026 Texas Instruments Incorporated

### 6.4.4 Disabled

The device output is shutdown by forcing the enable pin voltage to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, and internal circuits are shutdown. The output voltage is also actively discharged to ground by an internal discharge circuit from the output to ground.


Copyright © 2026 Texas Instruments Incorporated

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

### *7.1.1 Recommended Capacitor Types*

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature. However, using Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

### *7.1.2 Input and Output Capacitor Requirements*

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. Use a higher value capacitor if large, fast rise-time load or line transients are anticipated. Additionally, use this capacitor if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

### *7.1.3 Load Transient Response*

The load-step transient response is the output voltage response by the LDO to a step in load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response. These transitions are from a light to a heavy load and from a heavy to a light load. The regions shown in Figure 7-1 are broken down as follows. Regions A, E, and H are where the output voltage is in steady-state.

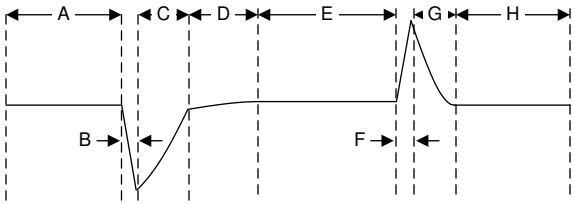



**Figure 7-1. Load Transient Waveform**

During transitions from a light load to a heavy load, the:

- Initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing the sourcing current, and leads to output voltage regulation (region C)

Copyright © 2026 Texas Instruments Incorporated

During transitions from a heavy load to a light load, the:

- Initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing the sourcing current in combination with the load discharging the output capacitor (region G)

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. Larger DC loads reduce the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

### *7.1.4 Undervoltage Lockout (UVLO) Operation*

The UVLO circuit makes sure the device stays disabled before the input supply reaches the minimum operational voltage range. This circuit also makes sure the device shuts down when the input supply collapses. Figure 7-2 shows the UVLO circuit response to various input voltage events. The diagram is separated into the following parts:

- Region A: The device does not start until the input reaches the UVLO rising threshold.
- Region B: Normal operation, regulating device.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output potentially falls out of regulation but the device remains enabled.
- Region D: Normal operation, regulating device.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start-up follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.
- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0V. The output falls because of the load and active discharge circuit.

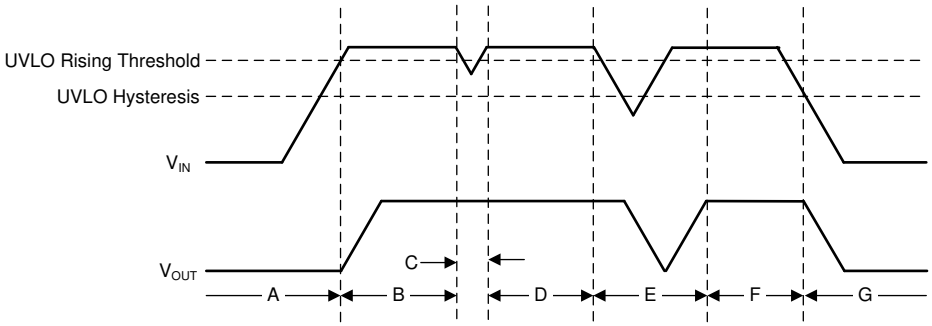



**Figure 7-2. Typical UVLO Operation**

### *7.1.5 Power Dissipation ($P_D$)*

Circuit reliability demands proper consideration be given to device power dissipation and location of the circuit on the printed circuit board (PCB). Verify correct sizing of the thermal plane. Make sure the PCB area around the regulator is as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Use Equation 2 to approximate $P_D$:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

Power dissipation is minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the TPS7A03 allows for maximum efficiency across a wide range of output voltages.


Copyright © 2026 Texas Instruments Incorporated

The main heat conduction path for the device is through the thermal pad on the package. As such, solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The maximum power dissipation determines the maximum allowable junction temperature ($T_J$) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$). The $R_{\theta JA}$ component is the combined PCB and device package and the temperature of the ambient air ($T_A$). Equation 4 rearranges Equation 3 for output current.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \quad (4)$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design. Therefore, $R_{\theta JA}$ varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area. This value is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the X2SON package $R_{\theta JC(bot)}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JC(bot)}$ is the junction-to-case (bottom) thermal resistance.

#### 7.1.5.1 Estimating Junction Temperature

The JEDEC standard now recommends using psi ($\Psi$) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics ($\Psi_{JT}$ and $\Psi_{JB}$) are used in accordance with Equation 5 and are given in the *Thermal Information* table.

$$\Psi_{JT} : T_J = T_T + \Psi_{JT} \times P_D \text{ and } \Psi_{JB} : T_J = T_B + \Psi_{JB} \times P_D \quad (5)$$

where:

- $P_D$ is the power dissipated as explained in Equation 2
- $T_T$ is the temperature at the center-top of the device package
- $T_B$ is the PCB surface temperature measured 1mm from the device package and centered on the package edge

#### 7.1.5.2 Recommended Area for Continuous Operation

The operational area of an LDO is limited by the dropout voltage, output current, junction temperature, and input voltage. The recommended area for continuous operation for a linear regulator is given in Figure 7-3 and is separated into the following parts:

- Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} - V_{OUT}$) at a given output current level. See the *Dropout Operation* section for more details.
- The rated output currents limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- The rated junction temperature limits the maximum junction temperature of the device. Exceeding this rating causes the device to fall out of specification and reduces long-term reliability.
  - The shape of the slope is given by Equation 4. The slope is nonlinear because the maximum rated junction temperature of the LDO is controlled by the power dissipation across the LDO. Thus when $V_{IN} - V_{OUT}$ increases, the output current decreases.
- The rated input voltage range governs both the minimum and maximum of $V_{IN} - V_{OUT}$.

Copyright © 2026 Texas Instruments Incorporated

Figure 7-3 shows the recommended area of operation for this device on a JEDEC-standard high-K board with a $R_{\theta JA}$ as given in the *Thermal Information* table.

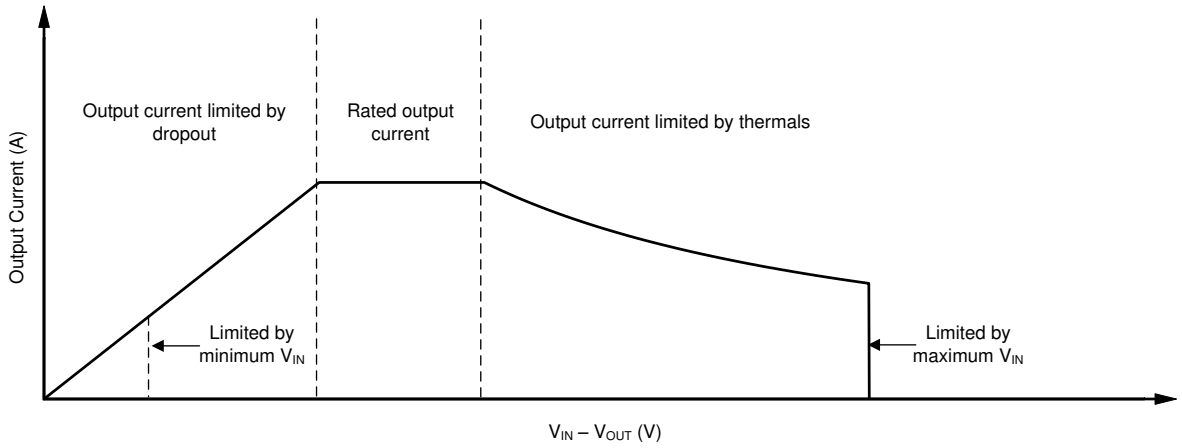



**Figure 7-3. Region Description of Continuous Operation Regime**

## 7.2 Typical Application

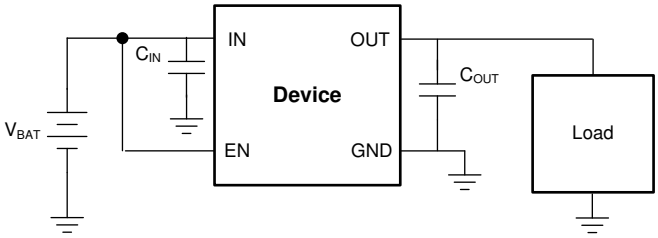



**Figure 7-4. Operation From a Battery Input Supply**

### *7.2.1 Design Requirements*

**Table 7-1. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 1.8V to 3.0V (two 1.5V batteries) |
| Output voltage | 1.0V, ±1% |
| Input current | 200mA, maximum |
| Output load | 10mA DC |
| Maximum ambient temperature | 70°C |

### *7.2.2 Detailed Design Procedure*

For this design example, the 1.0V, fixed-version TPS7A0310 is selected. A dual AA Alkaline battery was used, thus a 1.0µF input capacitor is recommended to minimize transient currents drawn from the battery. Use a 1.0µF output capacitor for excellent load transient response. Keep the dropout voltage ($V_{DO}$) within the TPS7A03 dropout voltage specification for the 1.0V output voltage option. This voltage level keeps the device in regulation under all load and temperature conditions for this design. Use the recommend 1µF input and output capacitor because the input source has a high equivalent series resistor (ESR) of 600mΩ (typ). The very small ground current consumed by the regulator maintains a high current efficiency as compared to the load current consumed by the system. This efficiency is depicted in Figure 7-5 , which allows for long battery life. Equation 6 calculates the current efficiency ($I_\eta$) of this system.

$$I_\eta(\%) = I_{OUT} / (I_{OUT} + I_Q) \times 100 \quad (6)$$


Copyright © 2026 Texas Instruments Incorporated

### 7.2.3 Application Curve

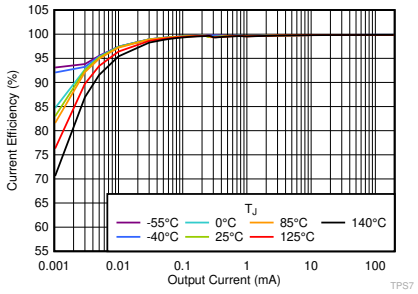



**Figure 7-5. Current Efficiency vs $I_{OUT}$ and Temperature**

## 7.3 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.5V to 6.0V. Make sure the input supply is well regulated and free of spurious noise. To verify that the output voltage is well regulated and dynamic performance is optimum, make sure the input supply is at least $V_{OUT(nom)}$ + 0.5V. Use a 1µF or greater input capacitor to reduce the impedance of the input supply, especially during transients.

## 7.4 Layout

### 7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DQN package. A via potentially wicks solder or solder paste away from the thermal pad joint during the soldering process. Therefore, leading to a compromised solder joint on the thermal pad.

### 7.4.2 Layout Examples

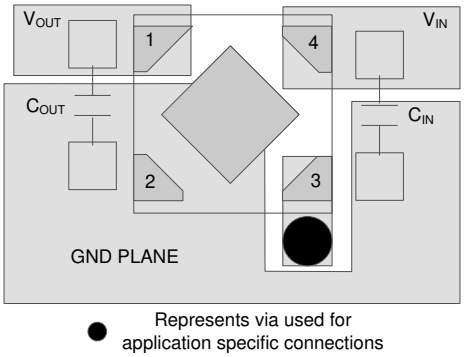



**Figure 7-6. Layout Example for the DQN Package**

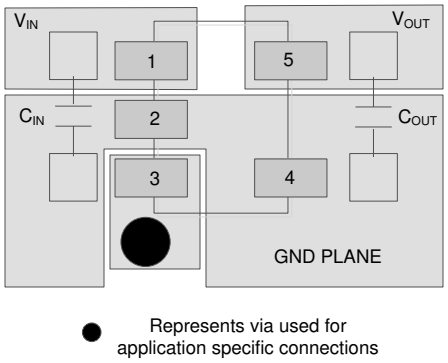



**Figure 7-7. Layout Example for the DBV Package**

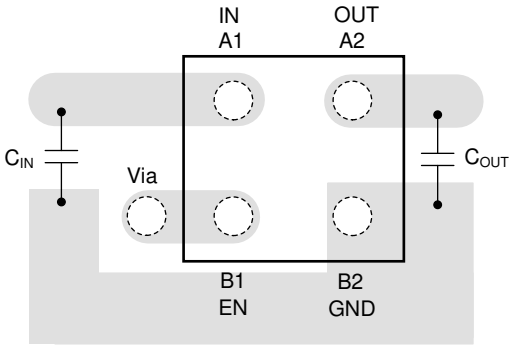



**Figure 7-8. Layout Example for the YCH Package**


Copyright © 2026 Texas Instruments Incorporated

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Device Nomenclature*

**Table 8-1. Device Nomenclature** (1) (2)

| PRODUCT | $V_{OUT}$ |
|---|---|
| TPS7A03 **xx(x)Pyyyz(M3)** | **XX(X)** is the nominal output voltage. For output voltages with a resolution of 100mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8V; 125 = 1.25V).<br>**P** indicates an active output discharge feature.<br>**YYY** is the package designator.<br>**Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). **M3** is a suffix designator for devices that only use the latest manufacturing flow. |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0V to 3.3V in 50mV increments are available. Contact the factory for details and availability.

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

Copyright © 2026 Texas Instruments Incorporated

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (September 2022) to Revision D (July 2026) | Page |
|---|---|
| • Changed X-axis time scale from "ms" to "µs" for the following typical characteristics figures, *Start-Up With $V_{EN}$ = $V_{IN}$* , *Start-Up With $V_{EN}$ Before $V_{IN}$* , *Start-Up With $V_{EN}$ After $V_{IN}$* | 8 |
| • Changed description of *P* indicator in *Device Nomenclature* table | 29 |
| • Added description of *M3* indicator in *Device Nomenclature* table | 29 |

| Changes from Revision B (April 2020) to Revision C (September 2022) | Page |
|---|---|
| • Changed YCH (DGBGA) package from preview to production data | 1 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2026 Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A0309PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | (22MT, 2FFT) |
| TPS7A0309PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (22MT, 2FFT) |
| TPS7A0309PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | P |
| TPS7A0310PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GO |
| TPS7A0310PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GO |
| TPS7A03125PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | TM |
| TPS7A0312DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OT |
| TPS7A0312DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OT |
| TPS7A0312PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21QF |
| TPS7A0312PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21QF |
| TPS7A0312PDBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21QF |
| TPS7A0312PDBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21QF |
| TPS7A0312PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OA |
| TPS7A0312PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OA |
| TPS7A0312PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | H |
| TPS7A0312PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | H |
| TPS7A0313PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 2FGT |
| TPS7A0313PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2FGT |
| TPS7A0315DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 43MU |
| TPS7A0315PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21UF |
| TPS7A0315PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21UF |
| TPS7A0315PDBVRG4 | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21UF |
| TPS7A0315PDBVRG4.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21UF |
| TPS7A0315PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GM |
| TPS7A0315PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GM |
| TPS7A0315PDQNR1 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GM |
| TPS7A0315PDQNR1.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GM |
| TPS7A0315PDQNRM3 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GM |
| TPS7A0315PDQNRM3.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GM |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A03175PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | R |
| TPS7A03175PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | R |
| TPS7A03185PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | HP |
| TPS7A03185PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HP |
| TPS7A0318DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 2CET |
| TPS7A0318DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 2CET |
| TPS7A0318DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT |
| TPS7A0318DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | PT |
| TPS7A0318PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21VF |
| TPS7A0318PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21VF |
| TPS7A0318PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | G3 |
| TPS7A0318PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G3 |
| TPS7A0318PDQNR1 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G3 |
| TPS7A0318PDQNR1.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G3 |
| TPS7A0318PDQNRM3 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G3 |
| TPS7A0318PDQNRM3.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G3 |
| TPS7A0318PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | J |
| TPS7A0318PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | J |
| TPS7A0320PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 22NT |
| TPS7A0320PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 22NT |
| TPS7A0320PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GK |
| TPS7A0320PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GK |
| TPS7A0321PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 2FHT |
| TPS7A0321PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2FHT |
| TPS7A0322DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IO |
| TPS7A0322DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IO |
| TPS7A0322PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 21RF |
| TPS7A0322PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 21RF |
| TPS7A0322PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GP |
| TPS7A0322PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GP |
| TPS7A0323DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 3BGH |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A0323DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 3BGH |
| TPS7A0323PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21SF |
| TPS7A0323PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21SF |
| TPS7A0323PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GQ |
| TPS7A0323PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GQ |
| TPS7A0325DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | K9 |
| TPS7A0325DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | K9 |
| TPS7A0325DQNR3 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | K9 |
| TPS7A0325DQNR3.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | K9 |
| TPS7A0325PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21NF |
| TPS7A0325PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21NF |
| TPS7A0325PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GN |
| TPS7A0325PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GN |
| TPS7A0325PDQNR3 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GN |
| TPS7A0325PDQNR3.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GN |
| TPS7A0325PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | K |
| TPS7A0325PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | K |
| TPS7A0328DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 29RT |
| TPS7A0328DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 29RT |
| TPS7A0328DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IG |
| TPS7A0328DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IG |
| TPS7A0328PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21OF |
| TPS7A0328PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21OF |
| TPS7A0328PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GL |
| TPS7A0328PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GL |
| TPS7A0328PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | L |
| TPS7A0328PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | L |
| TPS7A0330PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21WF |
| TPS7A0330PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21WF |
| TPS7A0330PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | G4 |
| TPS7A0330PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G4 |

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS7A0330PDQNRM3 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G4 |
| TPS7A0330PDQNRM3.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G4 |
| TPS7A0330PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | N |
| TPS7A0330PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | N |
| TPS7A0331PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21XF |
| TPS7A0331PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21XF |
| TPS7A0331PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | GR |
| TPS7A0331PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | GR |
| TPS7A0333DBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 29ST |
| TPS7A0333DBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | 29ST |
| TPS7A0333DQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IH |
| TPS7A0333DQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | IH |
| TPS7A0333PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21PF |
| TPS7A0333PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21PF |
| TPS7A0333PDQNR | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | G5 |
| TPS7A0333PDQNR.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G5 |
| TPS7A0333PDQNR3 | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G5 |
| TPS7A0333PDQNR3.A | Active | Production | X2SON (DQN) \| 4 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | G5 |
| TPS7A0333PYCHR | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | Q |
| TPS7A0333PYCHR.A | Active | Production | DSBGA (YCH) \| 4 | 12000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | Q |
| TPS7A0336PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 21TF |
| TPS7A0336PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 21TF |
| TPS7A0350PDBVR | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 2FIT |
| TPS7A0350PDBVR.A | Active | Production | SOT-23 (DBV) \| 5 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2FIT |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

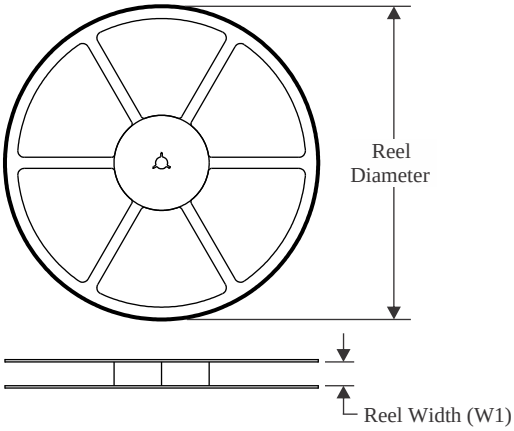
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

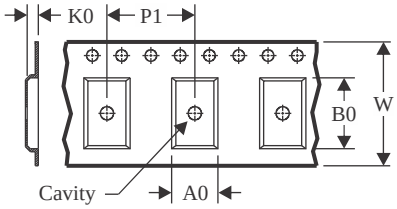
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

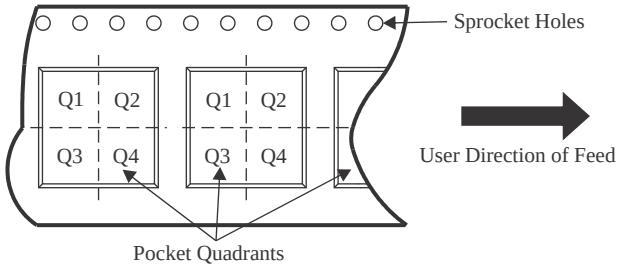



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



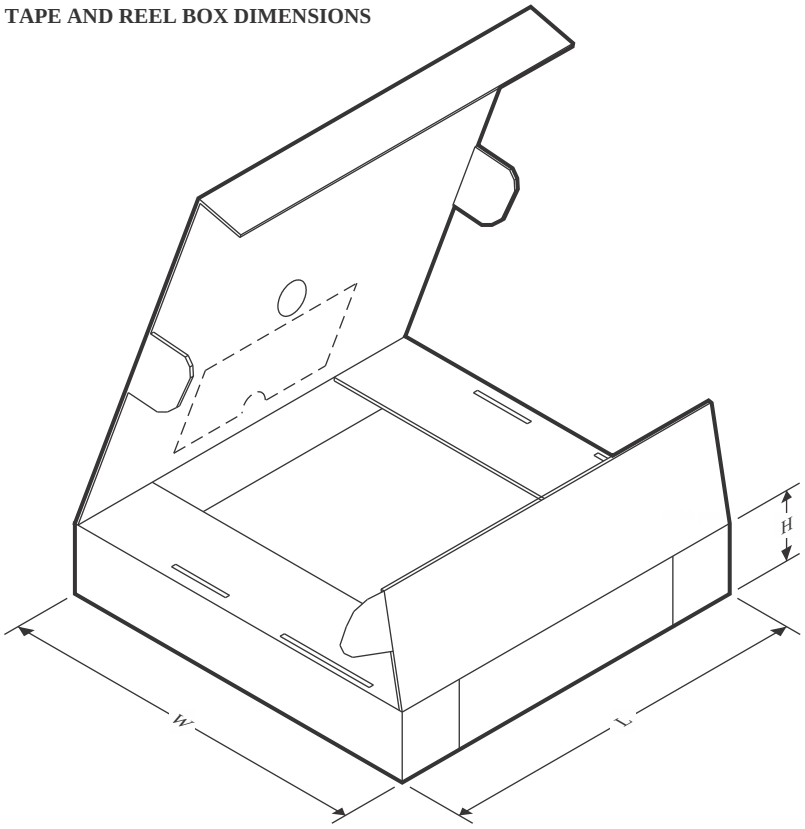

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A0309PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0309PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0310PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A03125PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0312DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0312PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0312PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0312PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0312PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0312PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0313PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0315DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0315PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0315PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0315PDQNR | X2SON | DQN | 4 | 3000 | 178.0 | 8.4 | 1.13 | 1.13 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS7A0315PDQNR1 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A0315PDQNRM3 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A03175PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A03185PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A03185PDQNR | X2SON | DQN | 4 | 3000 | 178.0 | 8.4 | 1.13 | 1.13 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS7A03185PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0318DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0318DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0318DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0318PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0318PDQNR | X2SON | DQN | 4 | 3000 | 178.0 | 8.4 | 1.13 | 1.13 | 0.53 | 4.0 | 8.0 | Q2 |
| TPS7A0318PDQNR1 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q1 |
| TPS7A0318PDQNRM3 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0318PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0320PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0320PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0320PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0321PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0322DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0322PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0322PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0322PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0323DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0323PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0323PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0325DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0325DQNR3 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| TPS7A0325PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0325PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0325PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0325PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0325PDQNR3 | X2SON | DQN | 4 | 3000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| TPS7A0325PDQNR3 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| TPS7A0325PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0328DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0328DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0328PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0328PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0328PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0330PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0330PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0330PDQNR | X2SON | DQN | 4 | 3000 | 178.0 | 8.4 | 1.13 | 1.13 | 0.53 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS7A0330PDQNRM3 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0330PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0331PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0331PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0331PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0333DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0333DQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0333PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0333PDQNR | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| TPS7A0333PDQNR3 | X2SON | DQN | 4 | 3000 | 180.0 | 8.4 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| TPS7A0333PDQNR3 | X2SON | DQN | 4 | 3000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q3 |
| TPS7A0333PYCHR | DSBGA | YCH | 4 | 12000 | 180.0 | 8.4 | 0.72 | 0.72 | 0.42 | 2.0 | 8.0 | Q1 |
| TPS7A0336PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0350PDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0350PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS7A0350PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A0309PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0309PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0310PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A03125PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0312DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0312PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0312PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0312PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0312PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0312PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0313PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0315DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0315PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0315PDBVRG4 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0315PDQNR | X2SON | DQN | 4 | 3000 | 205.0 | 200.0 | 33.0 |
| TPS7A0315PDQNR1 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0315PDQNRM3 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A03175PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A03185PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A03185PDQNR | X2SON | DQN | 4 | 3000 | 205.0 | 200.0 | 33.0 |
| TPS7A03185PDQNR | X2SON | DQN | 4 | 3000 | 184.0 | 184.0 | 19.0 |
| TPS7A0318DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS7A0318DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0318DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0318PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0318PDQNR | X2SON | DQN | 4 | 3000 | 205.0 | 200.0 | 33.0 |
| TPS7A0318PDQNR1 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0318PDQNRM3 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0318PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0320PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0320PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0320PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0321PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0322DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0322PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0322PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0322PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0323DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0323PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0323PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0325DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0325DQNR3 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0325PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0325PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0325PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS7A0325PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0325PDQNR3 | X2SON | DQN | 4 | 3000 | 184.0 | 184.0 | 19.0 |
| TPS7A0325PDQNR3 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0325PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0328DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0328DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0328PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0328PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0328PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0330PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS7A0330PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0330PDQNR | X2SON | DQN | 4 | 3000 | 205.0 | 200.0 | 33.0 |
| TPS7A0330PDQNRM3 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0330PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0331PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0331PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

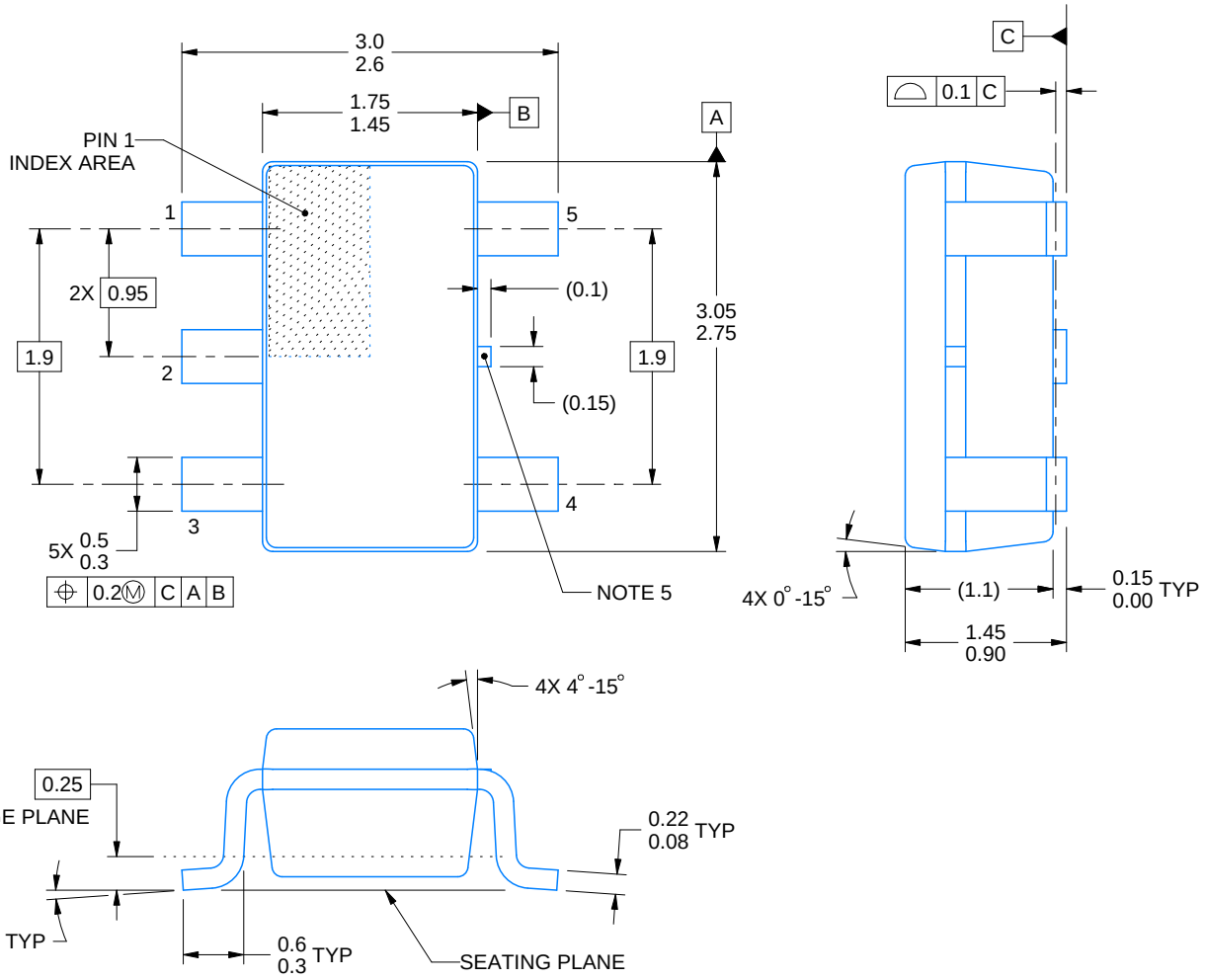
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS7A0331PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0333DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0333DQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0333PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0333PDQNR | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0333PDQNR3 | X2SON | DQN | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0333PDQNR3 | X2SON | DQN | 4 | 3000 | 184.0 | 184.0 | 19.0 |
| TPS7A0333PYCHR | DSBGA | YCH | 4 | 12000 | 182.0 | 182.0 | 20.0 |
| TPS7A0336PDBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| TPS7A0350PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| TPS7A0350PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS7A0350PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

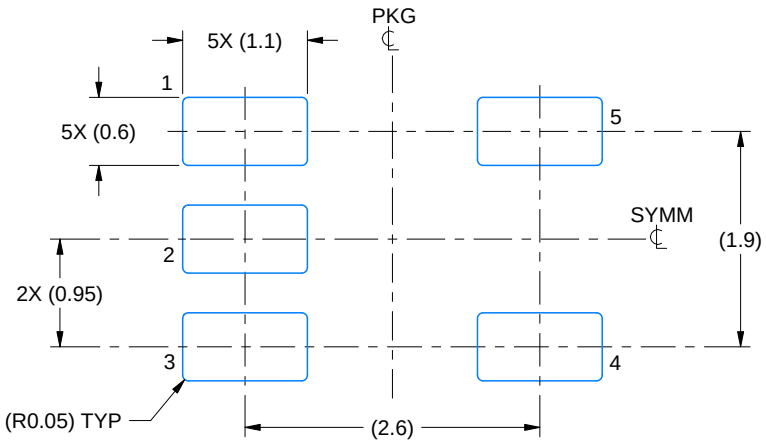
SMALL OUTLINE TRANSISTOR



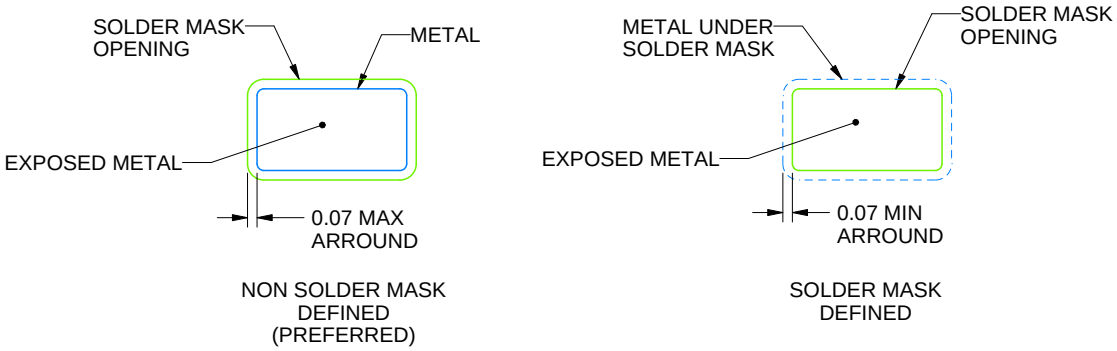

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

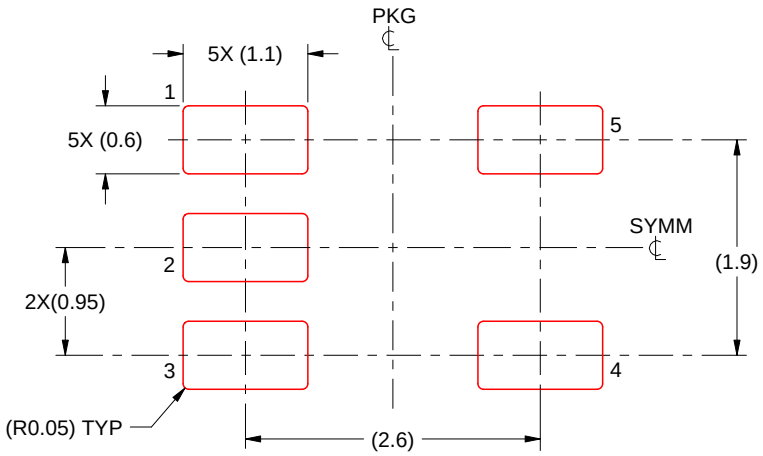



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# GENERIC PACKAGE VIEW

## DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

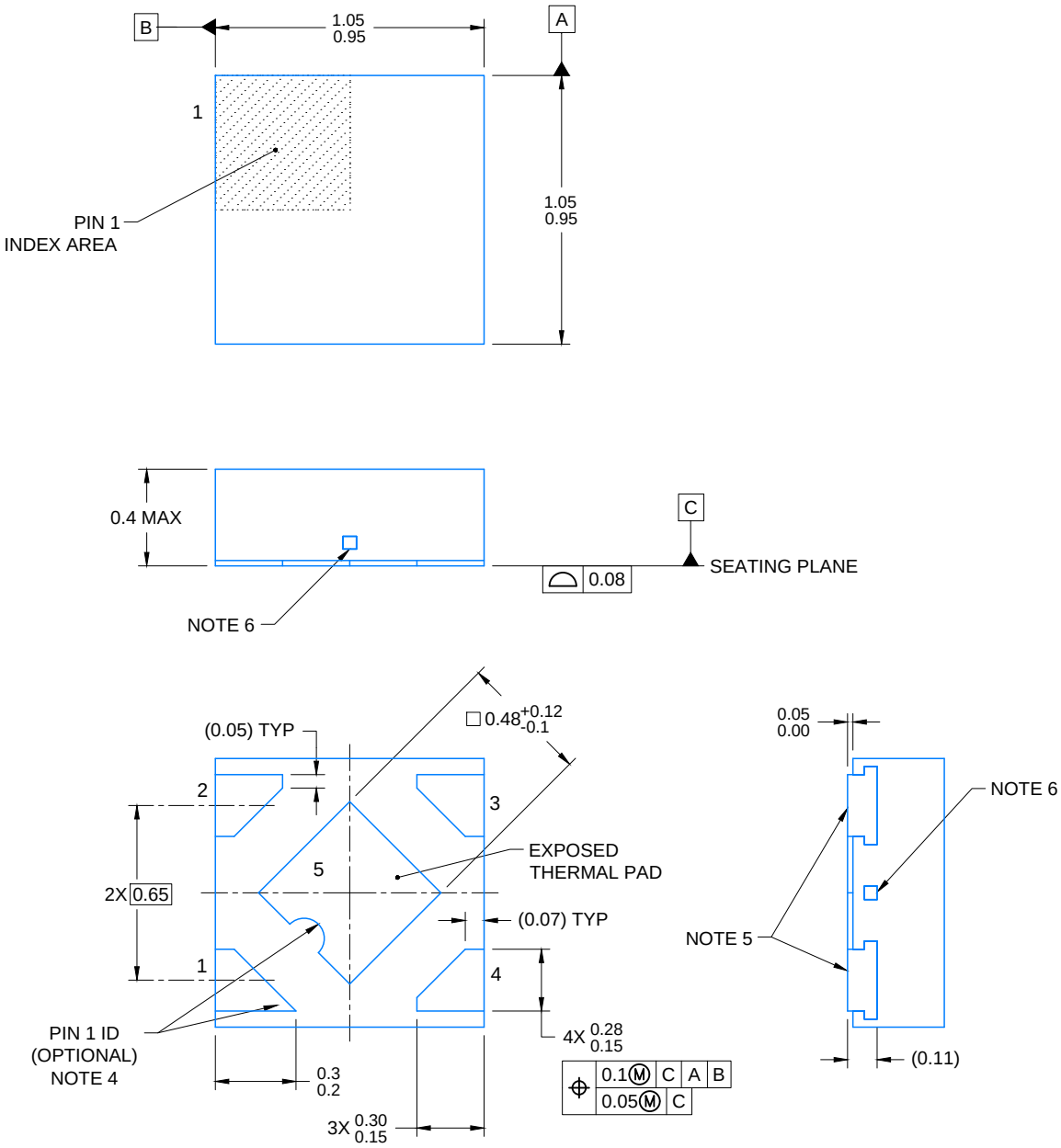
4210367/F

# PACKAGE OUTLINE

## DQN0004A

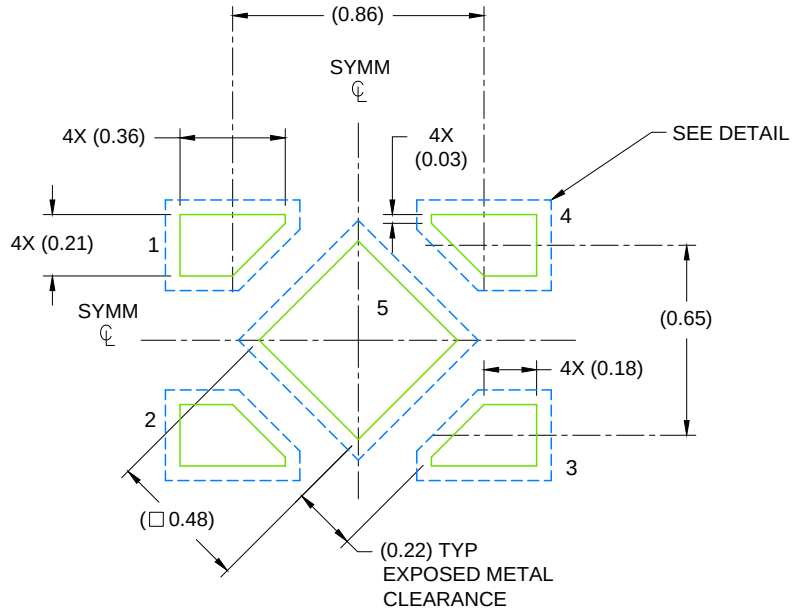
## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



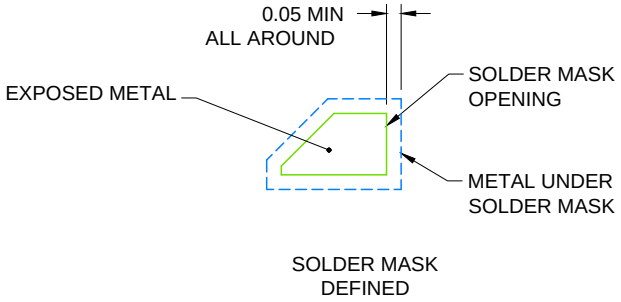

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.




LAND PATTERN EXAMPLE

SCALE: 40X

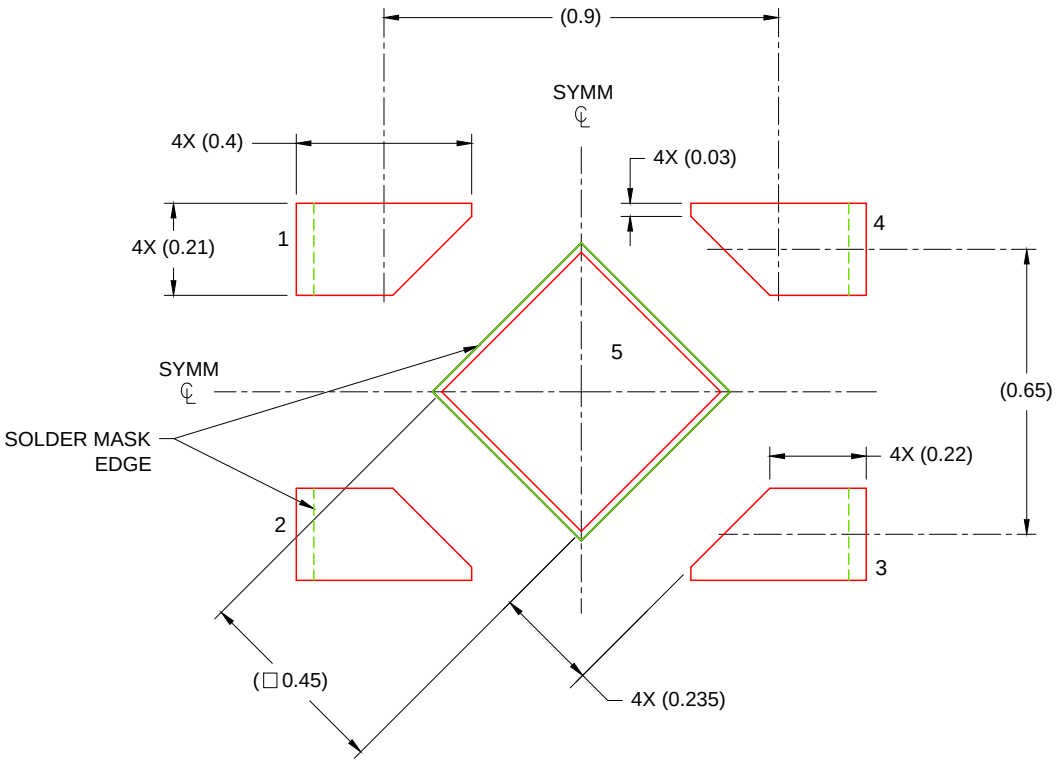



SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

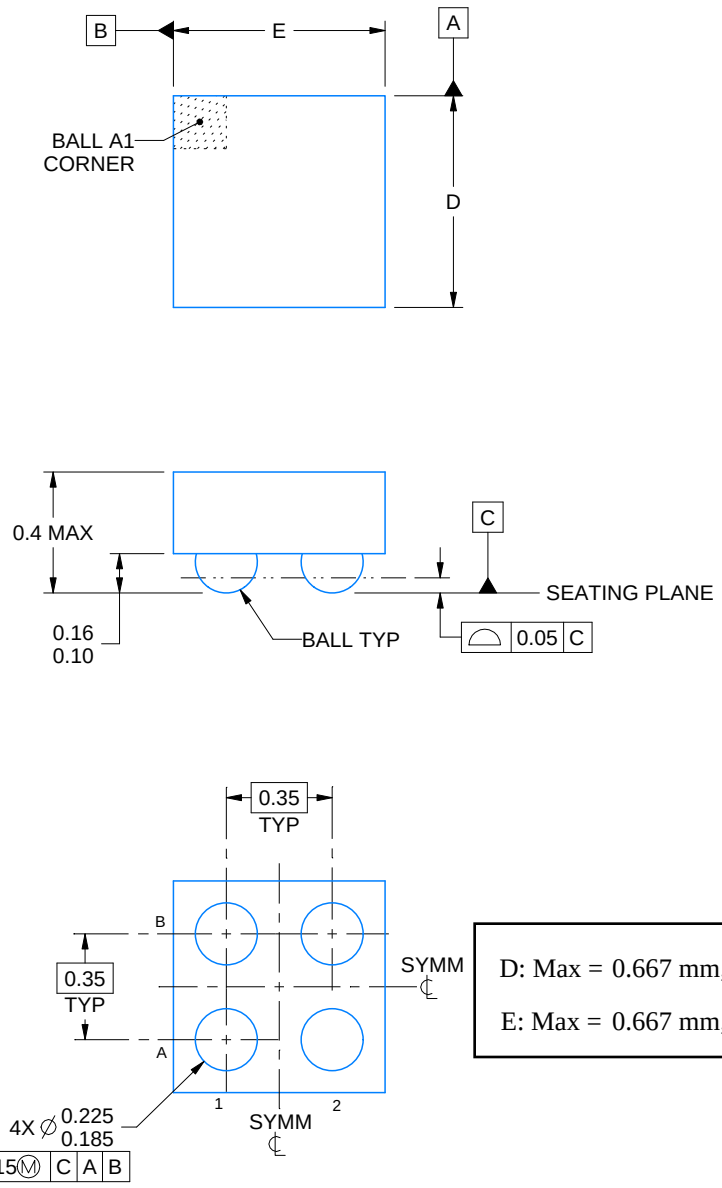
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# YCH0004

# PACKAGE OUTLINE

## DSBGA - 0.4 mm max height

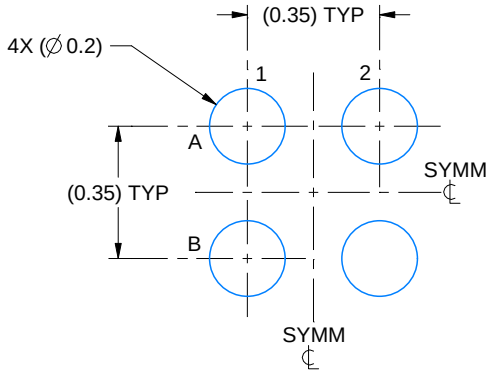
DIE SIZE BALL GRID ARRAY



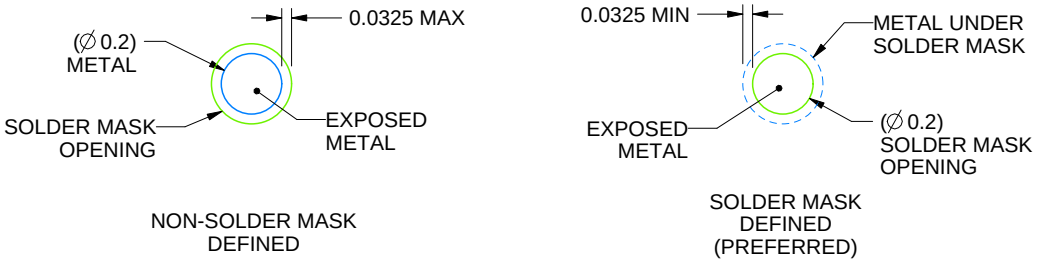

4224061/A 12/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X




SOLDER MASK DETAILS
NOT TO SCALE

4224061/A 12/2017

NOTES: (continued)

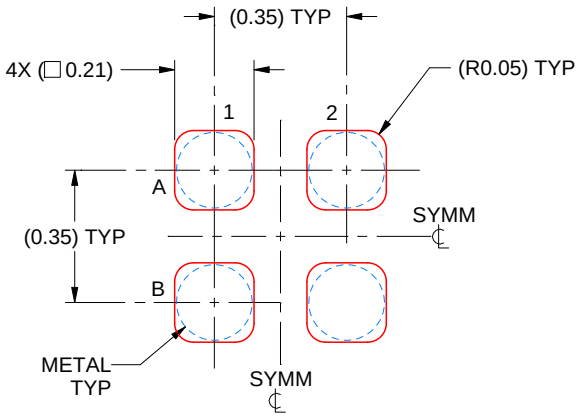
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

# EXAMPLE STENCIL DESIGN

## YCH0004

## DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY




SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4224061/A 12/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025