

## TPS7B69xx 150-mA, 40-V Ultralow-Quiescent-Current LDO

### 1 Features

- 4-V to 40-V Wide  $V_I$  Input Voltage Range With up to 45-V Transient
- Maximum Output Current: 150 mA
- Low Quiescent Current ( $I_Q$ ):
  - 15  $\mu$ A Typical at Light Loads
  - 25  $\mu$ A Maximum Under Full Temperature
- 450-mV Typical Low Dropout Voltage at 100 mA Load Current
- 10-mV Line Regulation Maximum
- 20-mV Load Regulation Maximum
- Stable With Low-ESR Ceramic Output Capacitor (2.2  $\mu$ F to 100  $\mu$ F)
- Fixed 3.3-V and 5-V Output Voltage Options
- Integrated Fault Protection:
  - Thermal Shutdown
  - Short-Circuit Protection
- Packages:
  - 5-Pin SOT-23 Package
  - 4-Pin SOT-223 Package

### 2 Applications

- E-meters, Water Meters and Gas Meters
- Appliances and White Goods
- Fire Alarm, Smoke Detector
- Medical, Health, and Fitness Applications

### 3 Description

The TPS7B69xx device is a low-dropout linear regulator that operates at up to 40-V  $V_I$ . With only 15- $\mu$ A (typical) quiescent current at light load, the device is applicable for standby microcontrol-unit systems, especially for always-on applications like e-meters, fire alarms, and smoke detectors.

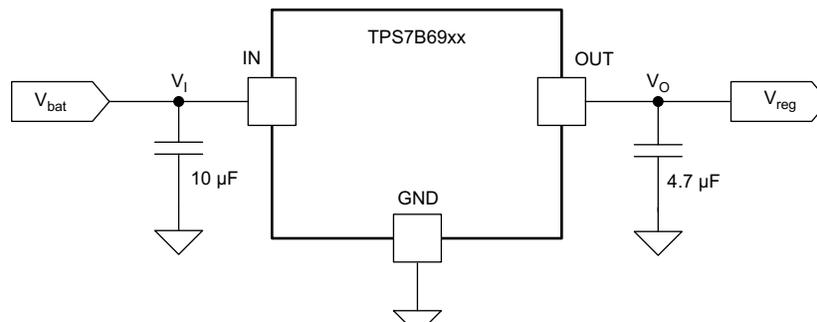
The devices have integrated short-circuit and overcurrent protection. The TPS7B69xx device operates over a  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$  temperature range.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7B6933	SOT-223 (4)	6.50 mm x 3.50 mm
TPS7B6950	SOT-23 (5)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

#### Typical Application Schematic



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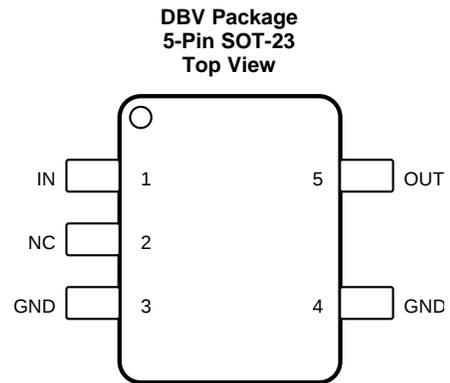
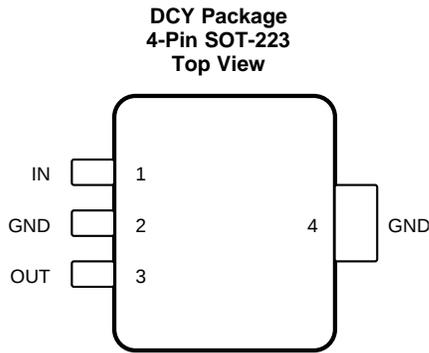
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## 4 Revision History

DATE	REVISION	NOTE
April 2016	*	Initial release

## 5 Pin Configuration and Functions



NC - No internal connection

### Pin Functions

NAME	PIN		TYPE	DESCRIPTION
	NO.			
	SOT-223	SOT-23		
GND	2, 4	3, 4	G	Ground reference
IN	1	1	P	Input power-supply voltage
NC	—	2	—	Not connected pin
OUT	3	5	P	Output voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Unregulated input voltage	IN <sup>(2)(3)</sup>	-0.3	45	V
Regulated output voltage	OUT <sup>(2)</sup>	-0.3	7	V
Operating junction temperature range, T <sub>J</sub>		-40	125	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminal.
- (3) Absolute maximum voltage, withstands 45 V for 200 ms.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>I</sub>	Unregulated input voltage	4	40	V
V <sub>O</sub>	Output voltage	0	5.5	V
C <sub>O</sub>	Output capacitor requirements <sup>(1)</sup>	2.2	100	μF
ESR <sub>CO</sub>	Output ESR requirements <sup>(2)</sup>	0.001	2	Ω
T <sub>A</sub>	Operating ambient temperature range	-40	105	°C

- (1) The output capacitance range specified in this table is the effective value.
- (2) Relevant ESR value at f = 10 kHz

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)(2)</sup>		TPS7B69xx		UNIT
		DCY (SOT-223)	DBV (SOT-23)	
		4 PINS	5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	64.2	210.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	46.8	126.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	13.3	38.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.3	16	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	13.2	37.5	°C/W

- (1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, 2s2p four layer board with 2-oz copper. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
- (2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

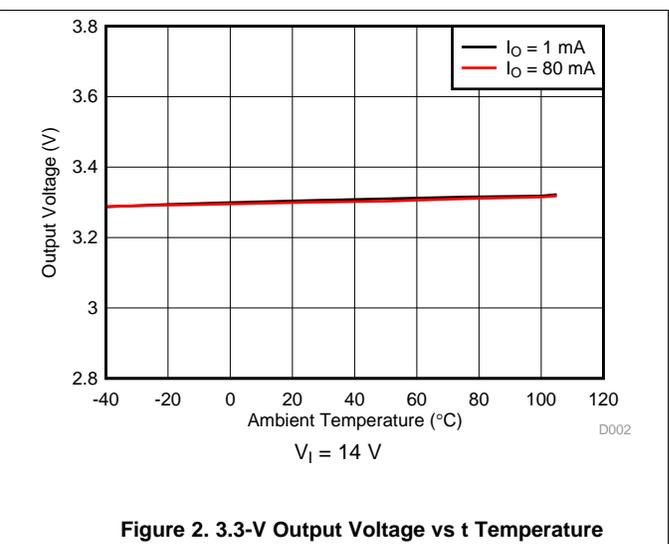
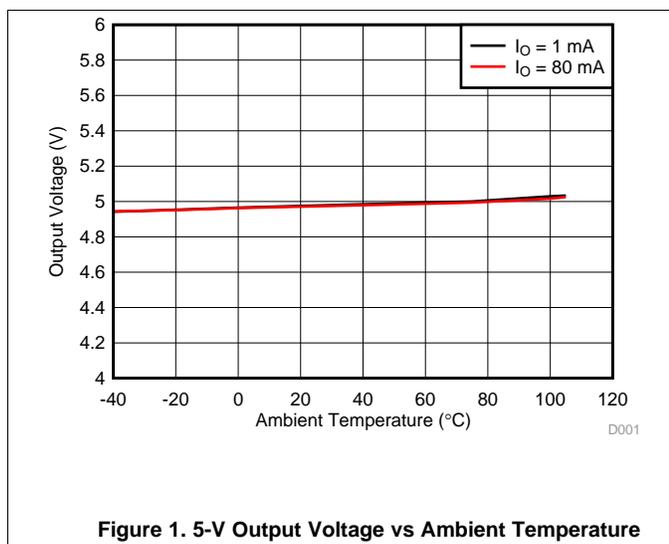
### 6.5 Electrical Characteristics

$V_{IN} = 14\text{ V}$ ,  $1\text{ m}\Omega < \text{ESR} < 2\ \Omega$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>SUPPLY VOLTAGE AND CURRENT (IN)</b>						
$V_I$	Input voltage	Fixed 3.3-V output, $I_O = 1\text{ mA}$	4		40	V
		Fixed 5-V output, $I_O = 1\text{ mA}$	5.5		40	
$I_Q$	Quiescent current	Fixed 3.3-V version, $V_I = 4$ to $40\text{ V}$ , $I_O = 0.2\text{ mA}$ Fixed 5-V version, $V_I = 5.5$ to $40\text{ V}$ , $I_O = 0.2\text{ mA}$		15	25	$\mu\text{A}$
$V_{IN(UVLO)}$	IN undervoltage detection	Ramp $V_I$ up until the output turns on	3.65			V
		Ramp $V_I$ down until the output turns OFF			3	
<b>REGULATED OUTPUT (OUT)</b>						
$V_O$	Regulated output	Fixed 3.3-V version, $V_I = 5$ to $40\text{ V}$ , $I_O = 1$ to $150\text{ mA}$	-3%		3%	
		Fixed 5-V version, $V_I = 6.5$ to $40\text{ V}$ , $I_O = 1$ to $150\text{ mA}$	-3%		3%	
$\Delta V_{O(\Delta V_I)}$	Line regulation	$V_I = 6$ to $40\text{ V}$ , $\Delta V_O$ , $I_O = 10\text{ mA}$			10	mV
$\Delta V_{O(\Delta I_L)}$	Load regulation	$I_O = 1$ to $150\text{ mA}$ , $\Delta V_O$			20	mV
$V_{DROPO}$	Dropout voltage	Fixed 3.3-V version, $V_I - V_O$ , $I_O = 50\text{ mA}$			799	mV
		Fixed 3.3-V version, $V_I - V_O$ , $I_O = 100\text{ mA}$			800	
		Fixed 5-V version, $V_I - V_O$ , $I_O = 50\text{ mA}$		220	400	
		Fixed 5-V version, $V_I - V_O$ , $I_O = 100\text{ mA}$		450	800	
$I_O$	Output current	$V_O$ in regulation	0		150	mA
$I_{OCL}$	Output current-limit	OUT short to ground	150		500	mA
PSRR	Power supply ripple rejection <sup>(1)</sup>	$V_{rip} = 0.5\text{ V}_{pp}$ , Load = $10\text{ mA}$ , $f = 100\text{ Hz}$ , $C_O = 2.2\ \mu\text{F}$		60		dB
<b>OPERATING TEMPERATURE RANGE</b>						
$T_{sd}$	Junction shutdown temperature			175		$^\circ\text{C}$
$T_{hys}$	Hysteresis of thermal shutdown			25		$^\circ\text{C}$

(1) Design Information—Not tested, ensured by characterization.

### 6.6 Typical Characteristics



Typical Characteristics (continued)

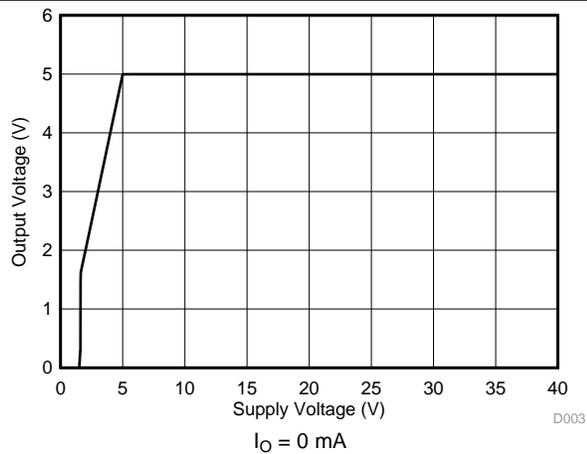


Figure 3. 5-V Output Voltage vs Supply Voltage

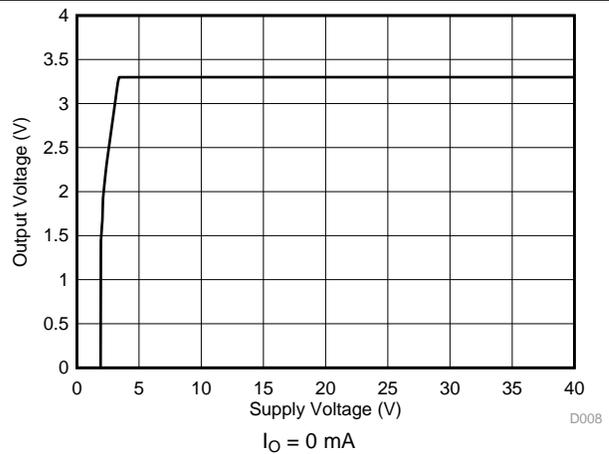


Figure 4. 3.3-V Output Voltage vs Supply Voltage

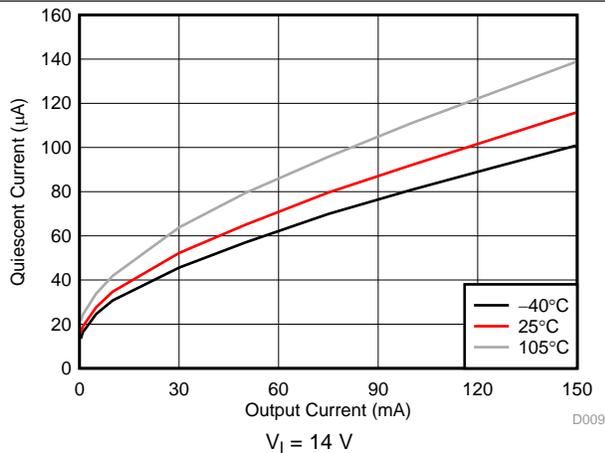


Figure 5. Quiescent Current vs Output Current

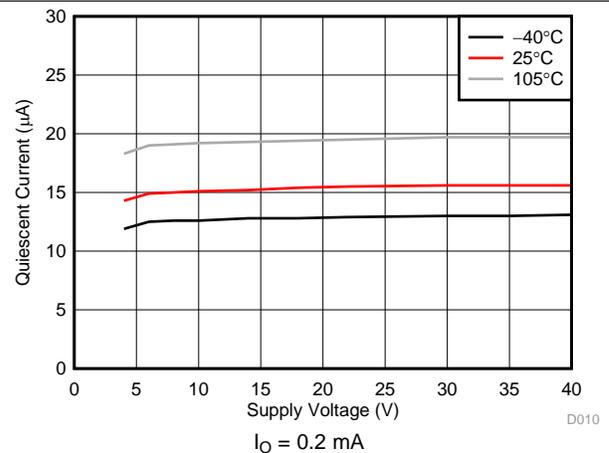


Figure 6. Quiescent Current vs Supply Voltage

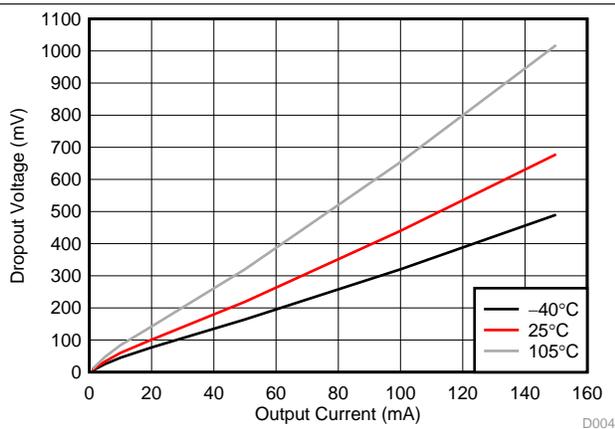


Figure 7. Dropout Voltage vs Output Current

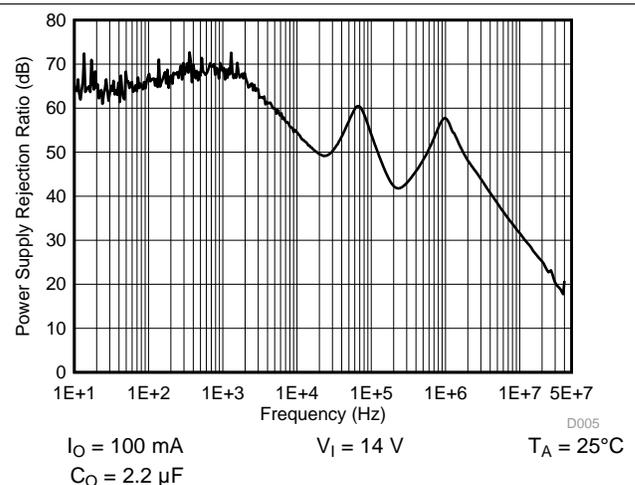


Figure 8. Power Supply Rejection Ratio

Typical Characteristics (continued)

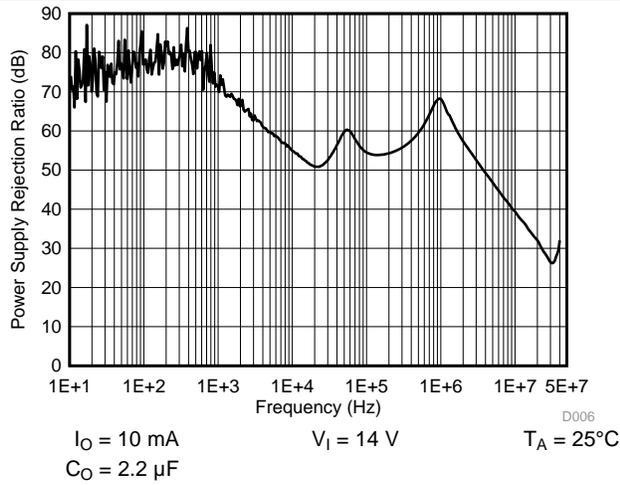


Figure 9. Power Supply Rejection Ratio

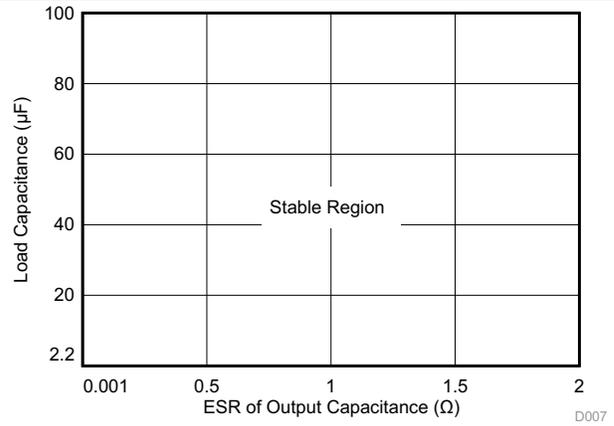


Figure 10. ESR Stability vs Output Capacitance

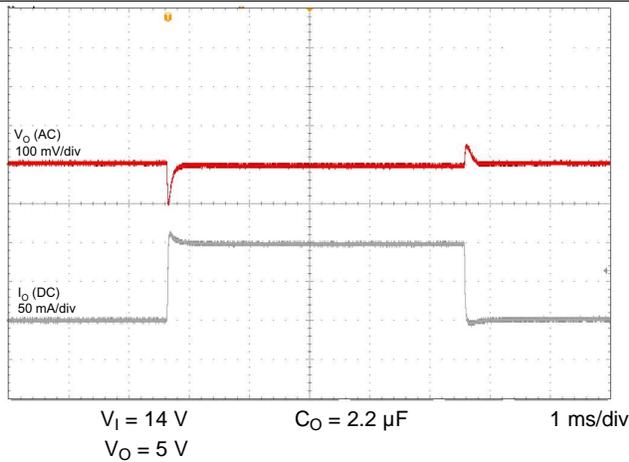


Figure 11. Load Transient (1 to 100 mA, 5 V)

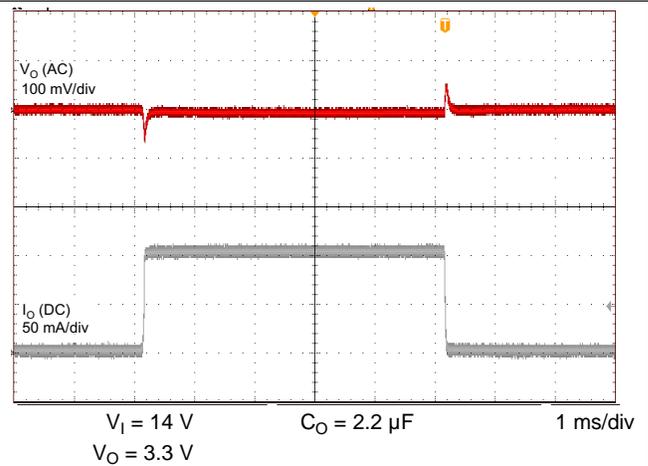


Figure 12. Load Transient (1 to 100 mA, 3.3 V)

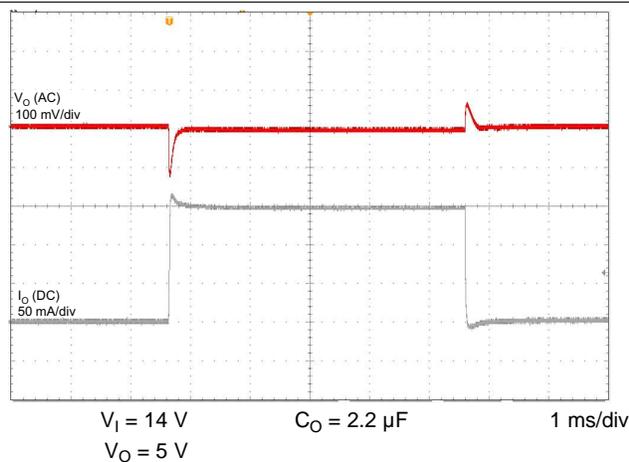


Figure 13. Load Transient (1 to 150 mA, 5 V)

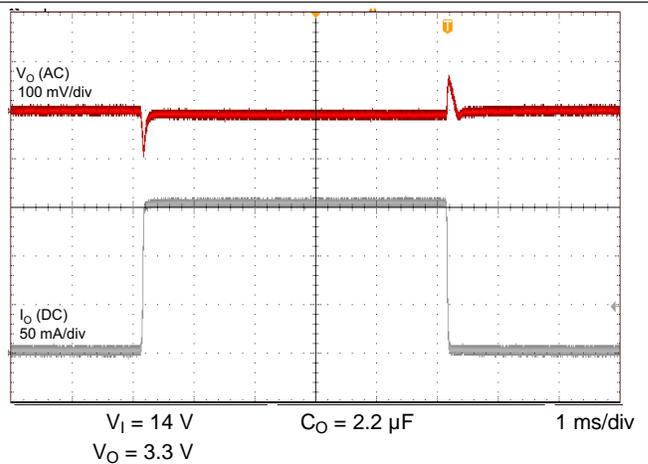
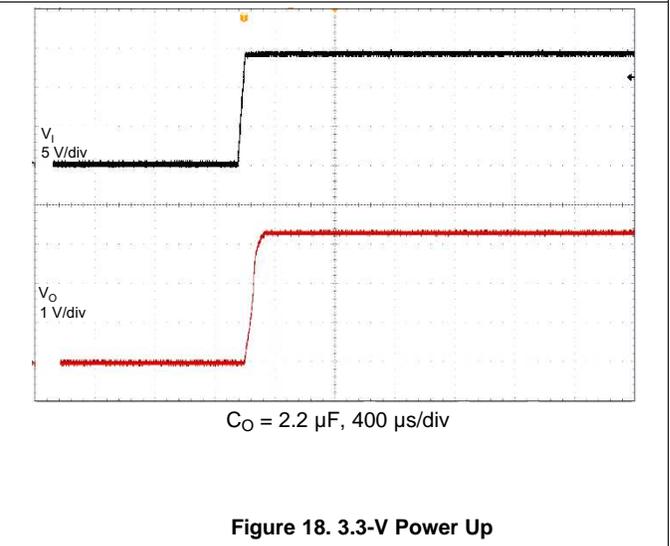
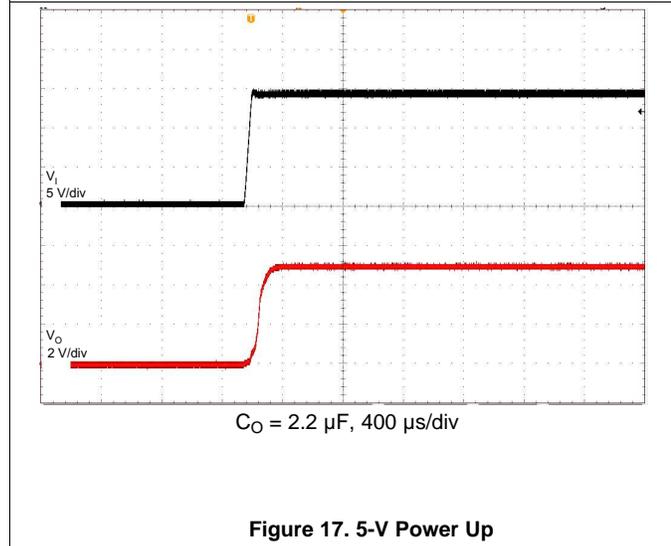
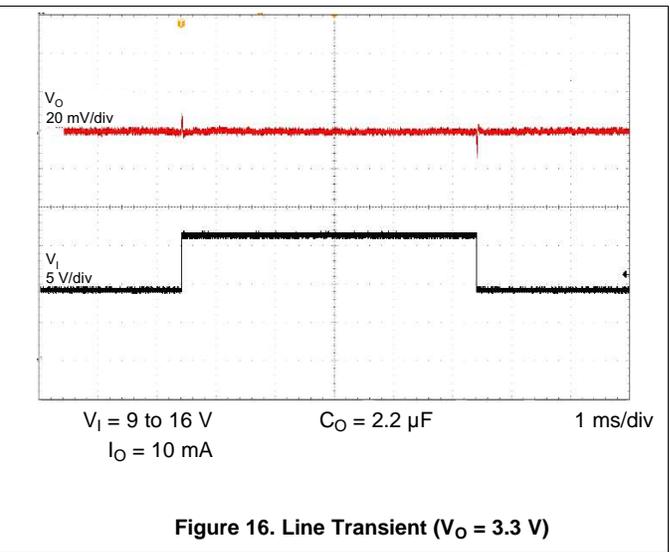
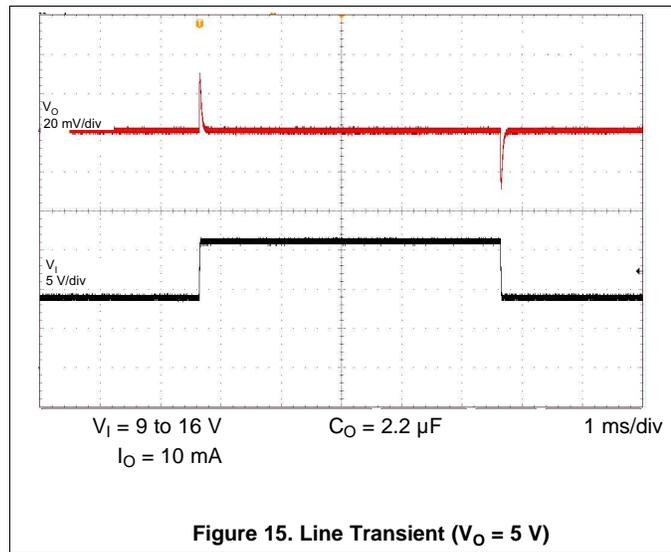


Figure 14. Load Transient (1 to 150 mA, 3.3 V)

Typical Characteristics (continued)





## Feature Description (continued)

### 7.3.4 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current ( $I_L$ ) and switch resistor. This tracking allows for a smaller input capacitor and can possibly eliminate the need for a boost converter during cold-crank conditions.

### 7.3.5 Thermal Shutdown

The TPS7B69xx family of devices incorporates a thermal-shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the hysteresis of TSD, the output turns on again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7B69xx family of devices is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7B69xx family of devices into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

### 7.4.1 Operation With $V_I$ Less Than 4 V

The TPS7B69xx family of devices operates with input voltages above 4 V. The maximum UVLO voltage is 3 V and the device operates at an input voltage above 4 V. The device can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO, the device shuts down.

### 7.4.2 Operation With $V_I$ Greater Than 4 V

When  $V_I$  is greater than 4 V, if the input voltage is higher than  $V_O$  plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to  $V_I$  minus the dropout voltage.

## 8 Application and Implementation

### NOTE

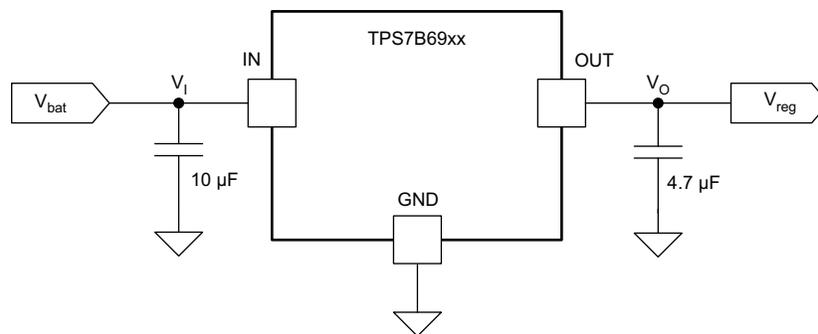
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7B69xx family of devices is a 150-mA low-dropout linear regulator designed for up to 40-V  $V_I$  operation with only 15- $\mu$ A quiescent current at light loads. Use the PSpice transient model to evaluate the base function of the device. To download the PSpice transient model, go to the device product folder on [www.TI.com](http://www.TI.com). In addition to this model, specific evaluation modules (EVM) are available for these devices. For the EVM and the EVM user guide, go to the device product folder.

### 8.2 Typical Application

Figure 19 shows the typical application circuit for the TPS7B69xx family of devices. Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to achieve better load transient response. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.



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Figure 19. Typical Application Schematic for TPS7B69xx

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	4 V to 40 V
Output voltage	3.3 V, 5 V
Output current rating	150 mA
Output capacitor range	2.2 $\mu$ F to 100 $\mu$ F
Output capacitor ESR range	1 m $\Omega$ to 2 $\Omega$

#### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating

### 8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommend value for the decoupling capacitor is higher than 0.1  $\mu\text{F}$ . The voltage rating must be greater than the maximum input voltage.

### 8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The output capacitor value should be between 2.2  $\mu\text{F}$  and 100  $\mu\text{F}$ . The ESR value range should be between 1 m $\Omega$  and 2  $\Omega$ . TI recommends a ceramic capacitor with low ESR to improve the load-transient response.

### 8.2.2.3 Power Dissipation and Thermal Considerations

Use [Equation 1](#) to calculate the power dissipated in the device.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I$$

where

- $P_D$  = continuous power dissipation
- $I_O$  = output current
- $V_I$  = input voltage
- $V_O$  = output voltage

(1)

Because  $I_Q \ll I_O$ , the term  $I_Q \times V_I$  in [Equation 1](#) can be ignored.

For a device under operation at a given ambient air temperature ( $T_A$ ), use [Equation 2](#) to calculate the junction temperature ( $T_J$ ).

$$T_J = T_A + (Z_{\theta JA} \times P_D)$$

where

$Z_{\theta JA}$  = junction-to-ambient air thermal impedance

(2)

Use [Equation 3](#) to calculate the rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (Z_{\theta JA} \times P_D)$$

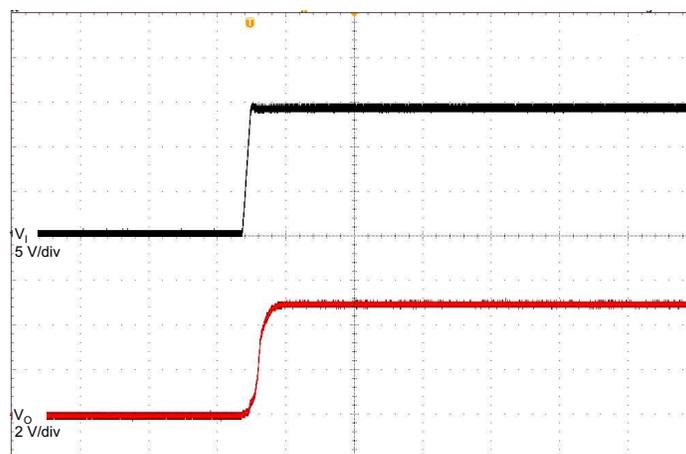
(3)

For a given maximum junction temperature ( $T_{Jmax}$ ), use [Equation 4](#) to calculate the maximum ambient air temperature ( $T_{Amax}$ ) at which the device can operate.

$$T_{Amax} = T_{Jmax} - (Z_{\theta JA} \times P_D)$$

(4)

## 8.2.3 Application Curve



$C_O = 2.2 \mu\text{F}$ , 400  $\mu\text{s/div}$

**Figure 20. Power Up (5 V)**

## 9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B69xx device, TI recommends adding an electrolytic capacitor with a value of 10  $\mu$ F and a ceramic bypass capacitor at the input.

## 10 Layout

### 10.1 Layout Guidelines

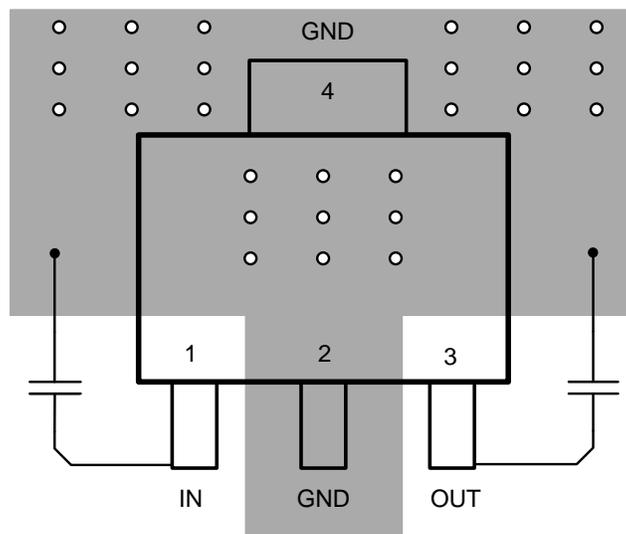
For the layout of TPS7B69xx family of devices, place the input and output capacitors near the devices as shown in [Figure 21](#) and [Figure 22](#). To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of long traces because they can impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7B69xx evaluation board.

### 10.2 Layout Example



**Figure 21. Layout Example for SOT-223 Package**

## Layout Example (continued)

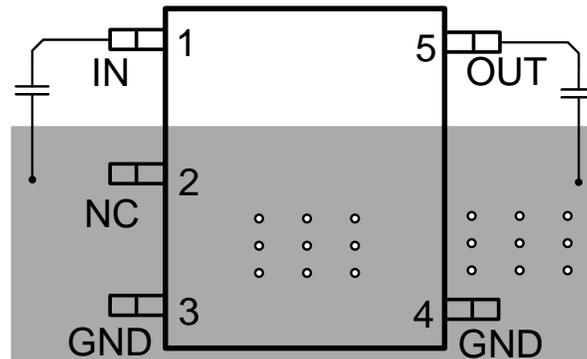


Figure 22. Layout Example for SOT-23 Package

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

*TPS7B6950EVM User's Guide*, [SLVUAC0](#).

### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS7B6933	<a href="#">Click here</a>				
TPS7B6950	<a href="#">Click here</a>				

### 11.3 Trademarks

All trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS7B6933DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 105	ZBFY
TPS7B6933DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	ZBFY
<a href="#">TPS7B6950DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 105	ZAZT
TPS7B6950DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 105	ZAZT

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPS7B69 :**

- Automotive : [TPS7B69-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B6933DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS7B6950DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B6933DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
TPS7B6950DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0

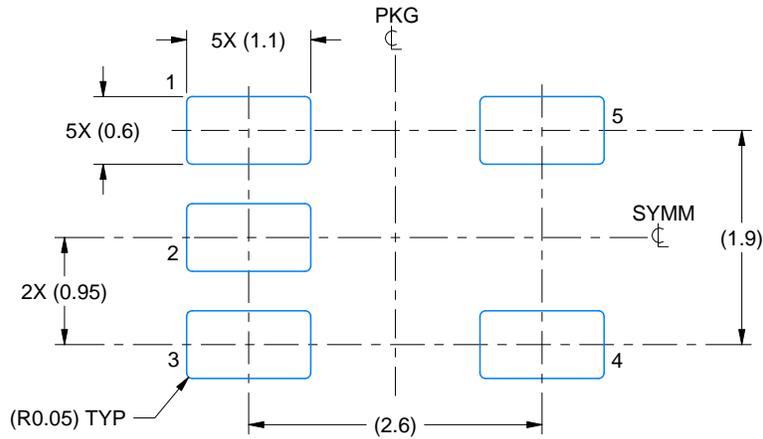


# EXAMPLE BOARD LAYOUT

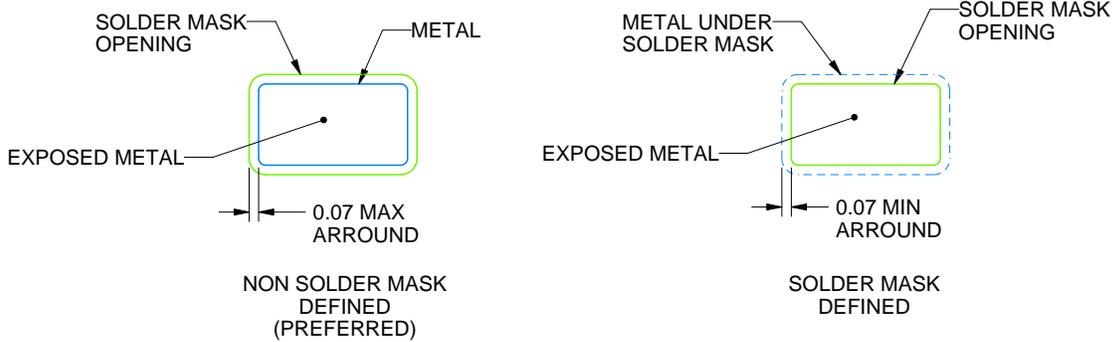
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

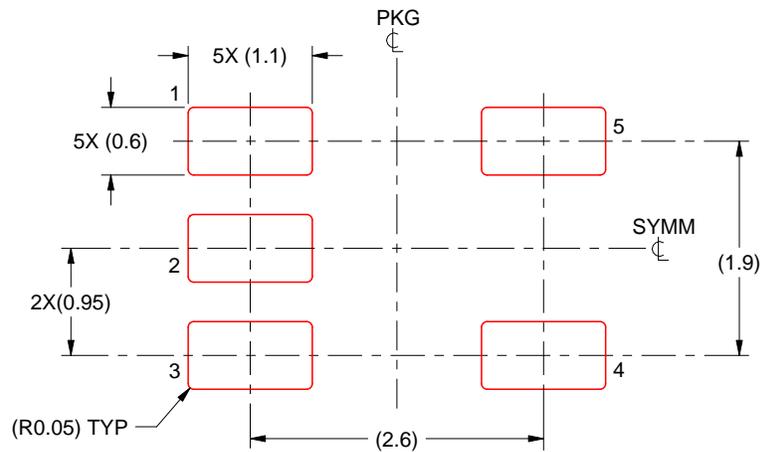
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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