TPS7H1121-SP and TPS7H1121-SEP 2.25V to 14V Input, 2A, Radiation Hardened Low Dropout (LDO) Linear Regulator

1 Features

- Total Ionizing Dose radiation characterized:
  - Radiation hardness assurance (RHA) availability of 100krad(Si) or 50krad(Si)
- Single-Event Effects (SEE) Characterized
  - Single-event latch-up (SEL), single-event burnout (SEB), and single-event gate rupture (SEGR) immune to linear energy transfer (LET) = 75MeV-cm^2/mg
  - Single-event functional interrupt (SEFI) characterized to LET = 75MeV-cm^2/mg
  - Single-event transient (SET) characterized to LET = 75MeV-cm^2/mg
- Wide V_{IN} range: 2.25V to 14V
- 2A maximum output current
- ±1.5% accuracy V_{IN} > 3V over load, and temperature
- ±1.8% accuracy V_{IN} < 3V over load, and temperature
- Soft start (SS) control through an external capacitor
- Open-drain power good (PG) output for power sequencing
- Programmable current limit through an external resistor (CL)
- Optional external control loop compensation utilizing the STAB pin
- Excellent load and line transient response
- Plastic packages out gas tested per ASTM E595
- Military (–55°C to 125°C) temperature range

2 Applications

- Satellite electrical power system (EPS)
- Clean analog supply requirements
- Command and data handling (C&DH)
- Optical imaging payload
- Radar imaging payload

3 Description

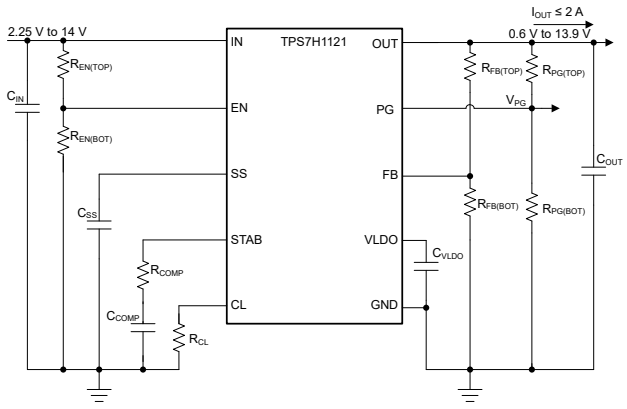
The TPS7H1121 is a radiation-hardened, low dropout linear regulator (LDO) which operates over a wide input voltage range and is optimized for powering devices in a space environment. The device is capable of sourcing up to 2A over a 2.25V to 14V input.

The device offers excellent stability and features a programmable current limit with a wide adjustment range. To support the complex power requirements of FPGAs, DSPs, and microcontrollers, the TPS7H1121 provides enable on and off functionality, programmable soft start, and a power good open-drain output.

Device Information

PART NUMBER(1)	GRADE	PACKAGE(2)
5962R2320301VXC	QMLV-RHA	22-Pin Ceramic 6.21mm × 7.69mm Mass = 415.6mg
TPS7H1121HFT/EM	Engineering sample	
5962R2320302PYE(3)	QMLP-RHA	24-Pin Plastic 4.40mm × 7.80mm Mass = 103mg
TPS7H1121MPWPTSEP	SEP	

(1) For additional information view the Section 4 table.
(2) Dimension and mass values are nominal.
(3) Product preview.



Typical Application Circuit

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

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4 Device Comparison Table

GENERIC PART NUMBER	RADIATION RATING(1)	GRADE(2)	PACKAGE	ORDERABLE PART NUMBER
TPS7H1121-SP	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm^2/mg	QMLV-RHA	22-pin CFP HFT	5962R2320301VXC
		QMLP-RHA	24 pin HTSSOP PWP	5962R2320302PYE(4)
	None	Engineering model(3)	22-pin CFP HFT	TPS7H1121HFT/EM
TPS7H1121-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV-cm^2/mg	Space Enhanced Plastic	24 pin HTSSOP PWP	TPS7H1121MPWPTSEP

(1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
(2) For additional information about part grade, view part ratings.
(3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life. For additional information about TI Engineering models, view TI Engineering Evaluation Units vs. MIL-PRF-38535 QML Class V Processing
(4) Product preview.

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5 Pin Configuration and Functions

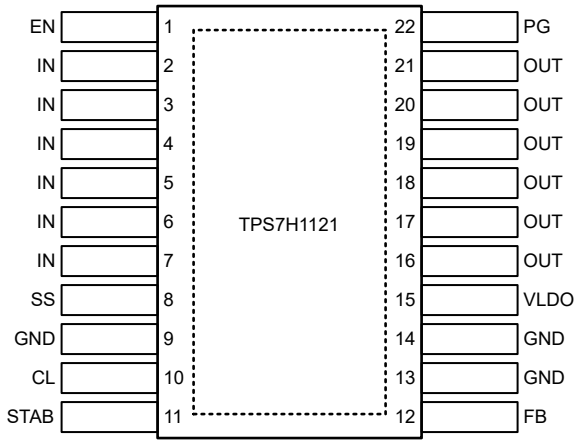


Figure 5-1. HFT Package 22-Pin CFP Top View

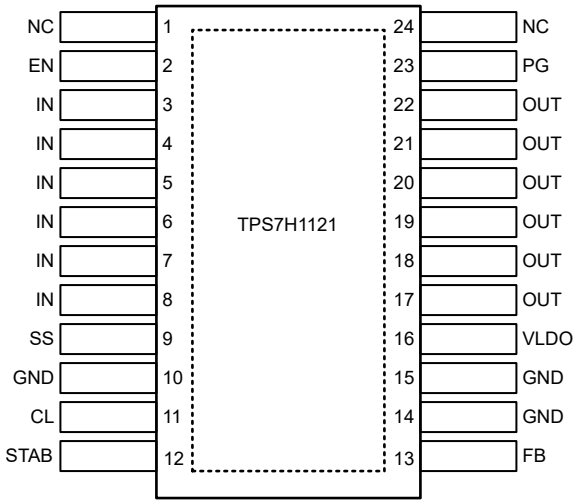


Figure 5-2. PWP Package 24-Pin HTSSOP Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	HFT (22) NO.	PWP (24) NO.		
EN	1	2	I	Enable. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device. If enable functionality is not required, connect this pin to IN using a resistor divider network, see Section 8.3.2. Do not float this pin.
IN	2, 3, 4, 5, 6, 7	3, 4, 5, 6, 7, 8	I	Input power. An input capacitor (nominally 10µF) near this pin is recommended.
SS	8	9	I/O	Soft-start. A minimum 1nF capacitor is required to prevent excessive inrush currents.
GND	9, 13, 14	10, 14, 15	—	Ground
CL	10	11	I	Programmable current limit. A resistor to GND sets the over-current limit activation point. The range of resistor that can be used on the CL terminal to GND is 41.2kΩ to 442kΩ.
STAB	11	12	I/O	Stability pin. This is an output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Standard compensation networks can be applied to the STAB (see Section 8.3.9.1); however, an output capacitance of 22µF to 220µF typically achieve high stability margins.
FB	12	13	I	The output voltage feedback input through voltage dividers. See Section 8.3.1.
NC	—	1, 24	—	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN}.
VLDO	15	16	O	Output of internal linear regulator, requires a 470nF capacitor connected to ground.
OUT	16, 17, 18, 19, 20, 21	17, 18, 19, 20, 21, 22	O	Output power pin. The regulated output voltage. A single 47µF tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22µF and 220µF are generally supported without additional compensation and wider ranges are supported with use of the STAB pin. See Section 9.2.2.8 for additional information.
PG	22	23	I/O	Power good indicator. This is an open drain pin. Use a pull-up resistor or a resistor divider (to ensure pin voltage does not exceed 7V) to achieve desired logic level when tied to VOUT. It is recommend to pull down PG to ground if left unused, the PG pin can be left floating if necessary. When the output reaches 95% (typ) of the set output voltage the PG pin is asserted.
Thermal pad	—	—	—	Internally grounded. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation.
Metal lid	Lid	N/A	—	The lid is internally connected to the thermal pad and GND through the seal ring.

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6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN, STAB	–0.3	16	V
	EN, PG	–0.3	7.5	
	FB, CL	-0.3	3.3	V
Output voltage	OUT	–0.6	16	V
	VLDO	–0.3	3.6	
	SS	-0.3	3.3	V
Input current	PG	–0.001	0.01	A
Output current	OUT	–3.9	3.9	A
Junction temperature	T_J	–55	150	°C
Storage temperature	T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	IN	2.25		14	V
	EN	0		7	
	PG	0		7	
Output voltage	OUT	0.6		$V_{IN} – V_{DO}$	V
	SS	0		1.2	
Input current	PG	0		2	mA
Output current	OUT	0		2	A
Junction temperature	T_J	–55		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS7H1121-SP	TPS7H1121-SP, -SEP	UNIT
		CFP HFT	PWP (HTSSOP)	
		22 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	18	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.5	7.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.3	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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6.5 Electrical Characteristics

Over 2.25V ≤ V_{IN} ≤ 14V, $V_{OUT\ (set)}$ ≤ V_{IN} – 0.5V, I_{OUT} = 10mA, C_{OUT} = 47µF, over operating temperature range (T_A = – 55°C to 125°C), typical values are at T_A = 25°C, unless otherwise noted; includes RLAT at TA = 25°C if sub-group number is present for QML RHA and SEP devices[2]

PARAMETER		Test Conditions		SUB-GROUP[1]	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
V_{DO}	Dropout voltage, see Figure 7-1	$V_{OUT(set)}$ = 2.25V, $V_{OUT(measured)}$ = 98% × $V_{OUT(NOM)}$	I_{OUT} = 100mA	1,2,3		28	60	mV
			I_{OUT} = 250mA	1,2,3		70	141	
			I_{OUT} = 500mA	1,2,3		150	280	
			I_{OUT} = 1A	1,2,3		300	570	
		$V_{OUT(set)}$ = 2.5V, $V_{OUT(measured)}$ = 98% × $V_{OUT(NOM)}$	I_{OUT} = 1.5A	1,2,3		525	750	
			I_{OUT} = 2A	1,2,3		570	900	
		3V ≤ $V_{OUT(set)}$ ≤ 13.3V, $V_{OUT(measured)}$ = 98% × $V_{OUT(NOM)}$	I_{OUT} = 100mA	1,2,3		20	50	
			I_{OUT} = 250mA	1,2,3		70	100	
			I_{OUT} = 500mA	1,2,3		125	180	
			I_{OUT} = 1A	1,2,3		300	340	
			I_{OUT} = 1.5A	1,2,3		325	490	
			I_{OUT} = 2A	1,2,3		500	700	
I_{PCL}	Programmed current limit (Ceramic HFT22 Package)	V_{IN} = 3.3V, $V_{OUT(short)}$ = 0.1V	RCL = 442kΩ	1,2,3	0.19	0.320	0.45	A
			RCL = 174kΩ	1,2,3	0.485	0.75	1.01	
			RCL = 82.5kΩ	1,2,3	1.16	1.55	1.94	
			RCL = 41.2kΩ	1,2,3	2.4	3	3.6	
	Programmed current limit (Plastic PWP24 Package)	V_{IN} = 3.3V, $V_{OUT(short)}$ = 0.1V	RCL = 442kΩ		0.165	0.35	0.545	A
			RCL = 174kΩ		0.51	0.835	1.1	
			RCL = 82.5kΩ		1.16	1.66	2.16	
			RCL = 41.2kΩ		2.4	3.15	3.85	
I_Q	Quiescent current	V_{EN} = 7V, I_{OUT} = 0A		1,2,3		8.75	15	mA
I_{GND} (I_{IN} - I_{OUT})	Ground current	V_{EN} = 7V	I_{OUT} = 1A	1,2,3		10	18	mA
			I_{OUT} = 2A	1,2,3		13	20	
VLDO	Internal linear regulator output voltage	V_{IN} = 2.25V		1,2,3	2.05	2.2	2.25	V
		3V ≤ V_{IN} ≤ 14V		1,2,3	2.30	2.55	2.78	
I_{SHDN}	Shutdown current	V_{EN} = 0V, I_{OUT} = 0A, V_{OUT} = 0V		1,2,3		380	775	µA
I_{FB}	Feedback leakage current	V_{FB} = 0.7V		1,2,3		1	15	nA
ACCURACY								
V_{ACC}	Output voltage accuracy	10mA ≤ I_{OUT} ≤ 2A, 0.6V ≤ V_{OUT} ≤ V_{IN} – V_{DO}, P_D ≤ 3W[3]	3V ≤ V_{IN} ≤ 14V	1,2,3	–1.5%		1.5%	
			3V ≤ V_{IN} ≤ 14V, T_A = 25°C	1	–1.1%		1.1%	
			2.25V ≤ VIN ≤ 3V	1,2,3	-1.8%		1.8%	
V_{FB}	Feedback voltage	3V ≤ V_{IN} ≤ 14V		1,2,3	0.588	0.596	0.606	V
			T_A = 25°C	1	0.591	0.596	0.603	
		2.25V ≤ V_{IN} ≤ 3V		1,2,3	0.586	0.596	0.608	
ΔV_{OUT}/ ΔV_{IN}	Line regulation, see Figure 7-2	3V ≤ V_{IN} ≤ 14V		1,2,3		100	650	µV/V
		2.25V ≤ V_{IN} ≤ 3V		1,2,3		285	1800	
ΔV_{OUT}/ ΔI_{OUT}	Load Regulation, see Figure 7-3	10mA ≤ I_{OUT} ≤ 2A, V_{IN} = 5V, V_{OUT} = 3.3V		1,2,3		4	16	mV/A
ENABLE								

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Over 2.25V ≤ V_{IN} ≤ 14V, $V_{OUT\ (set)}$ ≤ V_{IN} – 0.5V, I_{OUT} = 10mA, C_{OUT} = 47µF, over operating temperature range (T_A = – 55°C to 125°C), typical values are at T_A = 25°C, unless otherwise noted; includes RLAT at TA = 25°C if sub-group number is present for QML RHA and SEP devices(2)

PARAMETER		Test Conditions		SUB-GROUP(1)	MIN	TYP	MAX	UNIT
$V_{EN(rising)}$	Enable rising threshold (turn-on)			1,2,3	0.565	0.605	0.625	V
$V_{EN(falling)}$	Enable falling threshold (turn-off)			1,2,3	0.465	0.5	0.52	V
$t_{EN(delay)}$	EN propagation delay	EN high to V_{OUT} = 10mV		9,10,11		50	150	µs
$I_{EN(LKG)}$	Enable leakage current	V_{EN} = 7V		1,2,3		1	30	nA
T_{SD}	Thermal shutdown enter temperature					160		°C
T_{SD}	Thermal shutdown exit temperature					130		°C
POWER GOOD								
V_{PG_RISE}	Power good rising as percent of V_{OUT}			1,2,3	93%	95%	97%	
V_{PG_FALL}	Power good falling as percent of V_{OUT}			1,2,3	88.5%	91.5%	94%	
$V_{PG(OL)}$	Power good output low	$I_{PG(SINK)}$ = 2mA		1,2,3		90	190	mV
$V_{IN(MIN_PG)}$	Minimum VIN for valid PG (V_{PG} < 0.5V)	$I_{PG(SINK)}$ = 0.5mA		1,2,3		0.6	0.8	V
$I_{PG(LKG)}$	Power good leakage	V_{PG} = 7V, V_{FB} = 0.7V		1,2,3		0.05	2	µA
SOFT START								
I_{SS}	Soft-start current			1,2,3	1.4	2	2.7	µA
t_{SS}	Soft-start time	V_{IN} = 5V, V_{OUT} = 3.3V, measured from V_{OUT} = 10mV to PG assert	C_{SS} = 1nF	9,10,11	0.22	0.35	0.48	ms
			C_{SS} = 33nF	9,10,11	5.5	10	14.5	
STABILITY								
GM	Gain Margin	V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{OUT} = 47µF, T_A = 25°C, No External Compensation				24		dB
PM	Phase Margin					60°		
NOISE AND PSRR								
PSRR	Power-supply rejection ratio	V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SS} = 5.6nF	f_{ripple} = 100Hz			68		dB
			f_{ripple} = 1kHz			72		
			f_{ripple} = 10kHz			51		
			f_{ripple} = 100kHz			40		
			f_{ripple} = 1MHz			34		
V_N	Output noise voltage (bandwidth from 10Hz to 100kHz)	V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A, C_{SS} = 5.6nF				35		$µV_{RMS}$

(1) Subgroups are applicable for QML parts. For subgroup definitions see Section 6.6.
(2) See the 5962R23203 SMD for additional information on the QML RHA devices.
(3) P_D is the internal power dissipation. When P_D exceeds 3W, the current is lowered to avoid excessive local heating (due to tester limitations).

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6.6 Quality Conformance Inspections

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMPERATURE (ºC)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Dynamic tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

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6.7 Typical Characteristics

V_{IN} = 5V, V_{OUT} = 3.3V, T_A = 25ºC and C_{SS} = 5.6nF, C_{OUT}= 47µF (TBME476K025LBLC0), when used, the external compensation network is applied as depicted in Section 8.2, no R_{COMP}, no C_{Comp} unless otherwise noted.

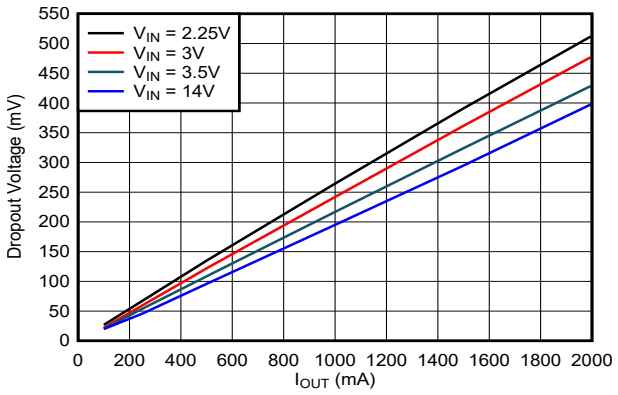
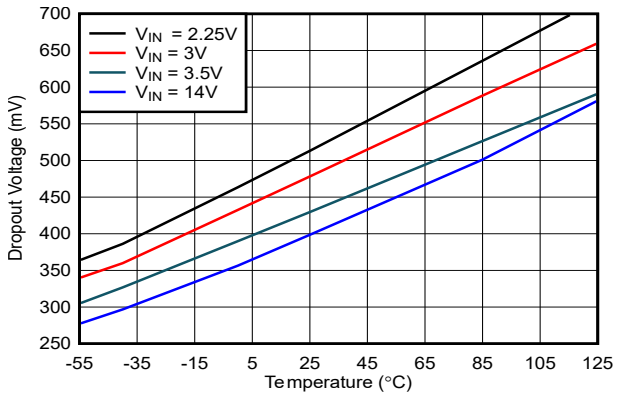
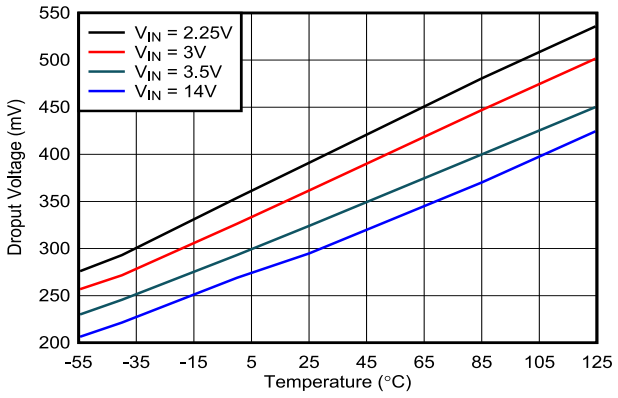


Figure 6-1. Dropout Voltage vs Current



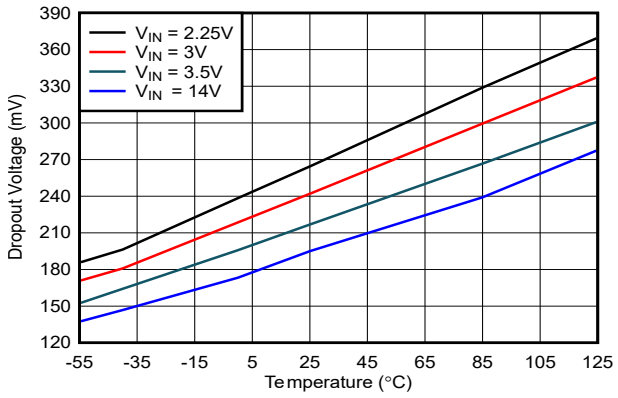
I_{Load} = 2000mA

Figure 6-2. Dropout Voltage vs Temperature



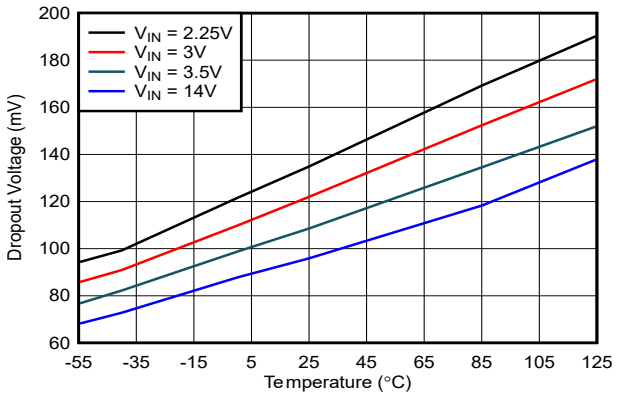
I_{Load} = 1500mA

Figure 6-3. Dropout Voltage vs Temperature



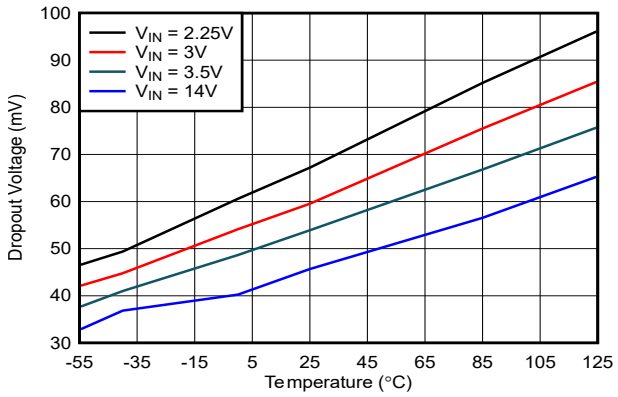
I_{Load} = 1000mA

Figure 6-4. Dropout Voltage vs Temperature



I_{Load} = 500mA

Figure 6-5. Dropout Voltage vs Temperature



I_{Load} = 250mA

Figure 6-6. Dropout Voltage vs Temperature

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6.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = 3.3V, T_A = 25ºC and C_{SS} = 5.6nF, C_{OUT}= 47µF (TBME476K025LBLC0), when used, the external compensation network is applied as depicted in Section 8.2, no R_{COMP}, no C_{Comp} unless otherwise noted.

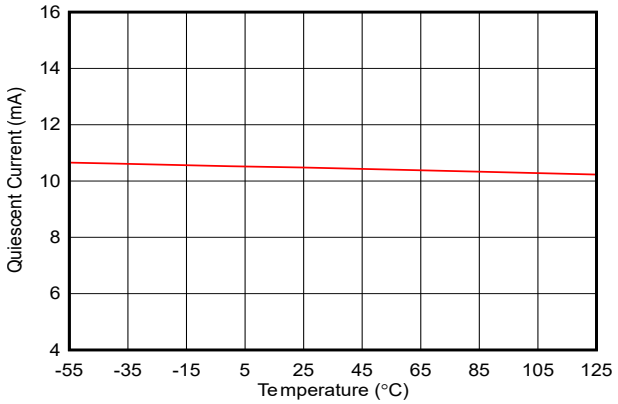


Figure 6-7. Quiescent Current vs Temperature

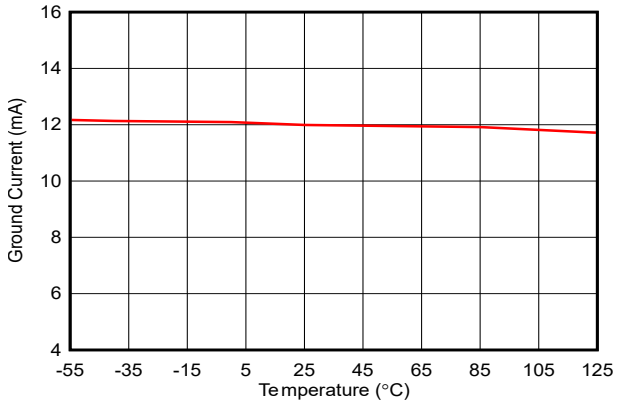


Figure 6-8. Ground Current vs Temperature

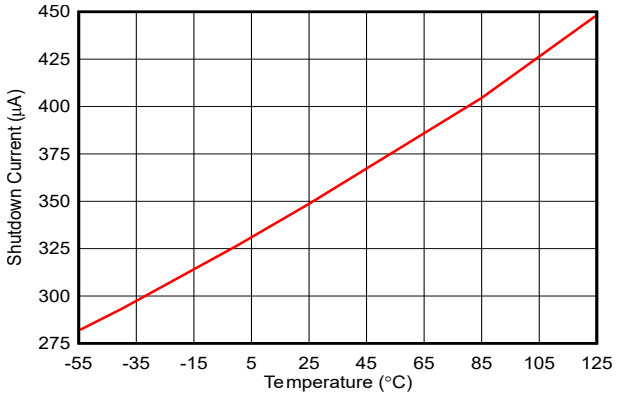


Figure 6-9. Shutdown Current vs Temperature

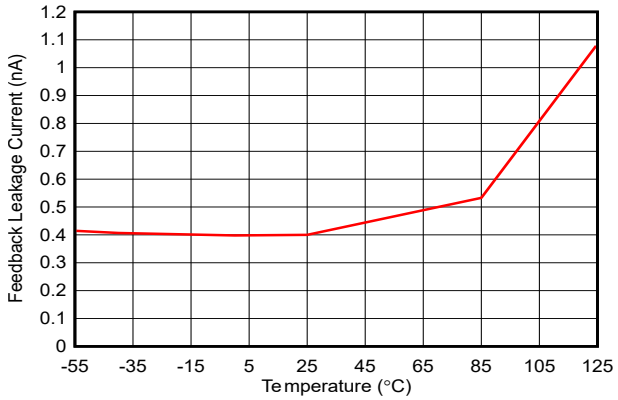


Figure 6-10. Feedback Pin Leakage Current vs Temperature

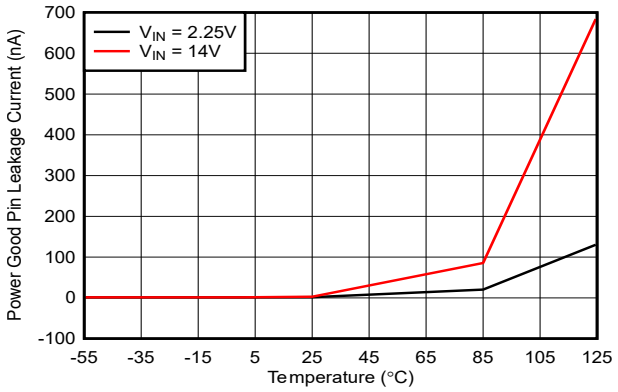


Figure 6-11. Power Good Pin Leakage Current vs Temperature

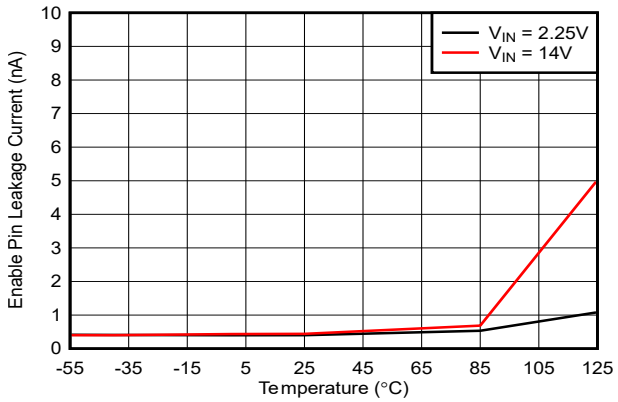


Figure 6-12. Enable Pin Leakage Current vs Temperature

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6.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = 3.3V, T_A = 25ºC and C_{SS} = 5.6nF, C_{OUT}= 47µF (TBME476K025LBLC0), when used, the external compensation network is applied as depicted in Section 8.2, no R_{COMP}, no C_{Comp} unless otherwise noted.

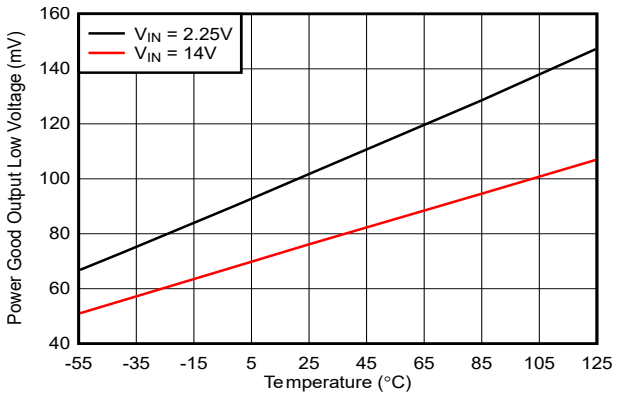


Figure 6-13. PG Pin Output Low vs Temperature

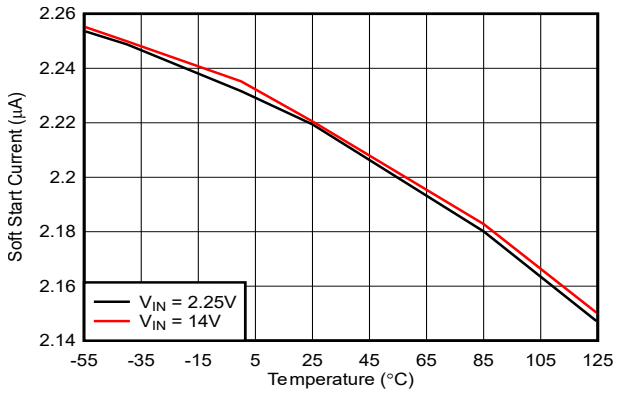
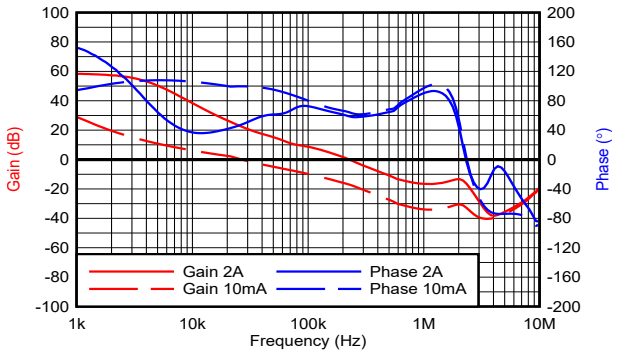
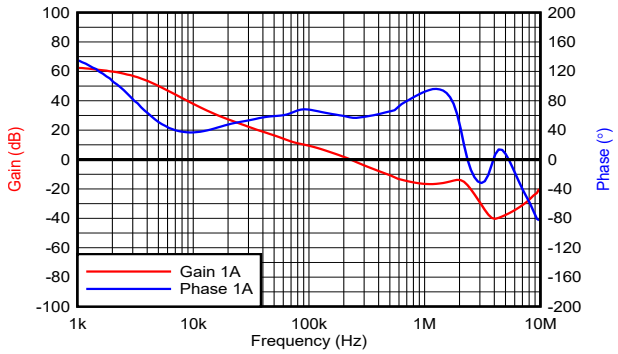


Figure 6-14. Soft Start Current vs Temperature



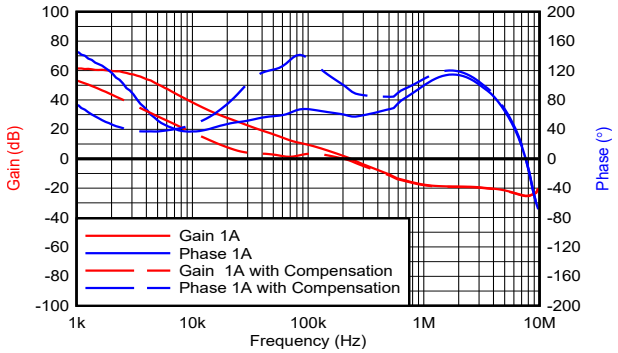
C_{OUT1} = 47µF C_{OUT2} = 1µF C_{OUT3} = 0.1µF
GM_{2A} = 17dB GM_{10mA} = 32dB
PM_{2A} = 58º PM_{10mA} = 100º

Figure 6-15. Gain and Phase Margin vs Frequency (Bode Plot)



C_{OUT1} = 47µF C_{OUT2} = 1µF C_{OUT3} = 0.1µF
GM_{2A} = 17dB
PM_{2A} = 58º

Figure 6-16. Gain and Phase Margin vs Frequency (Bode Plot)



C_{OUT} = 47µF If compensation used:
GM_{1A} = 24dB GM_{COMP} = 25dB R_{COMP} = 20kΩ
PM_{1A}= 60º PM_{COMP}= 101º C_{COMP} = 1nF

Figure 6-17. Gain and Phase Margin vs Frequency (Bode Plot)

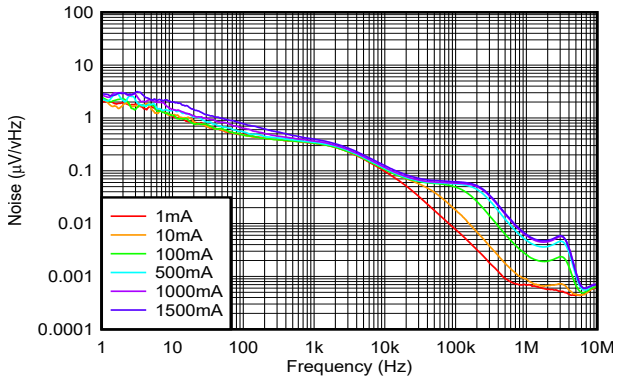
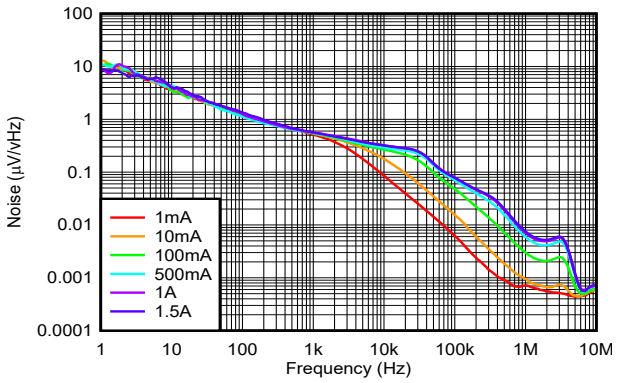


Figure 6-18. Output Noise vs Frequency Across Current (Noise Spectral Density)

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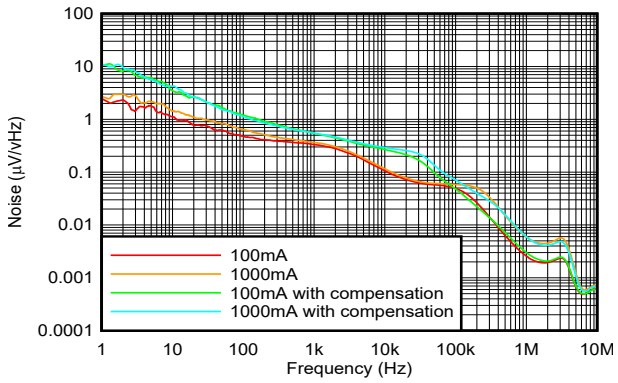
6.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = 3.3V, T_A = 25ºC and C_{SS} = 5.6nF, C_{OUT}= 47µF (TBME476K025LBLC0), when used, the external compensation network is applied as depicted in Section 8.2, no R_{COMP}, no C_{Comp} unless otherwise noted.



C_{COMP} = 1nF R_{COMP} = 20kΩ

Figure 6-19. Output Noise vs Frequency Across Current (Noise Spectral Density)



If compensation used:

C_{COMP} = 1nF R_{COMP} = 20kΩ

Figure 6-20. Output Noise vs Frequency, External Compensation Comparison (Noise Spectral Density)

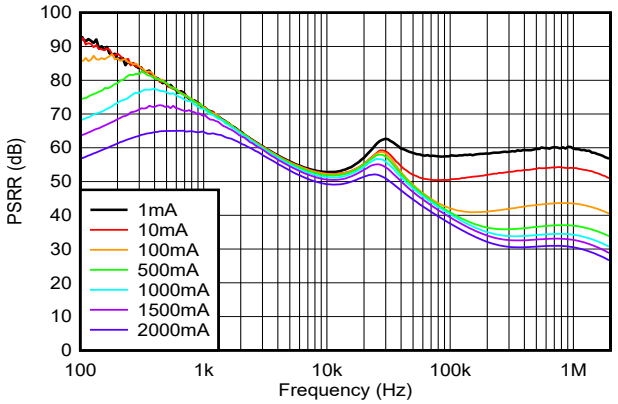
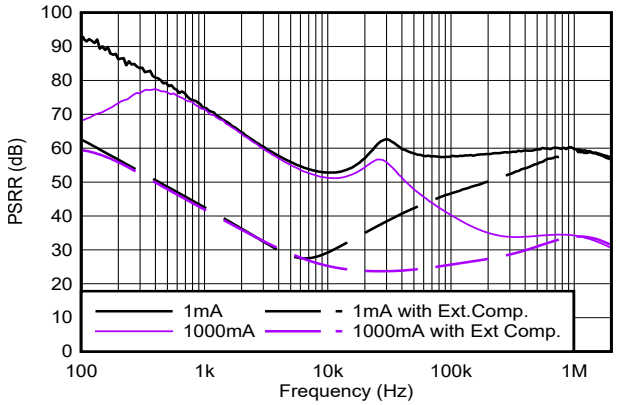


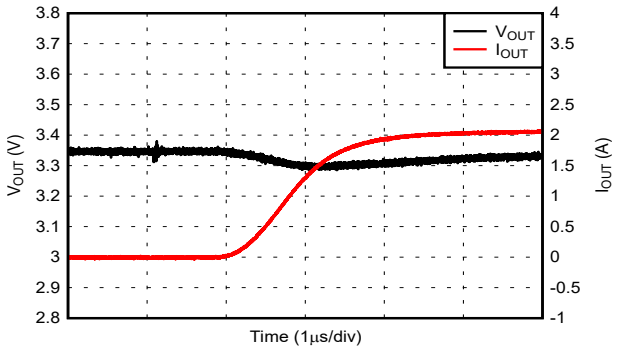
Figure 6-21. PSRR vs Frequency Across Current



If compensation used:

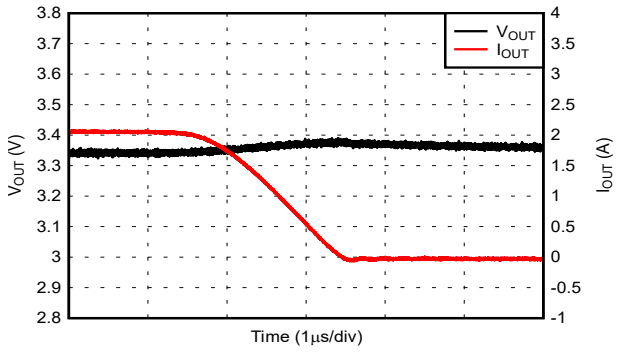
C_{COMP} = 1nF R_{COMP} = 20kΩ

Figure 6-22. PSRR vs Frequency, External Compensation Comparison



Slew Rate = 1A/µs

Figure 6-23. Load Step: 0A to 2A with VIN = 5V



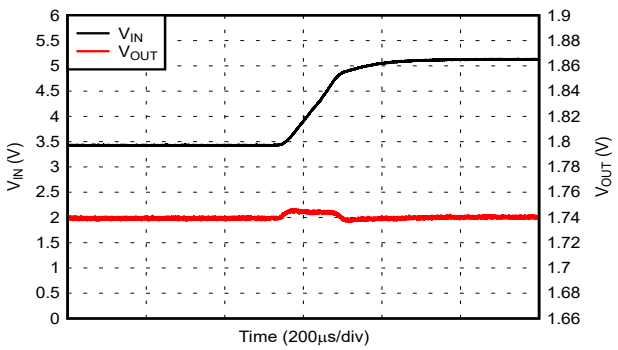
Slew Rate = 1A/µs

Figure 6-24. Load Step 2A to 0A with VOUT = 5V

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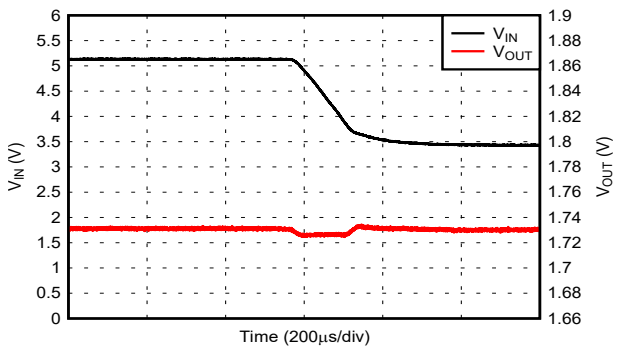
6.7 Typical Characteristics (continued)

V_{IN} = 5V, V_{OUT} = 3.3V, T_A = 25ºC and C_{SS} = 5.6nF, C_{OUT}= 47µF (TBME476K025LBLC0), when used, the external compensation network is applied as depicted in Section 8.2, no R_{COMP}, no C_{Comp} unless otherwise noted.



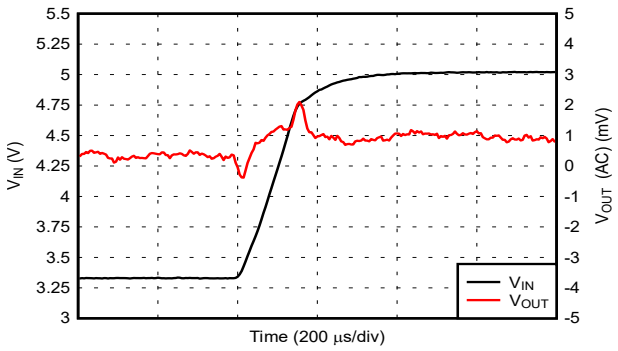
Slew Rate = 10V/ms

Figure 6-25. Line Step: 3.3V to 5V With I_{OUT} = 1.8A



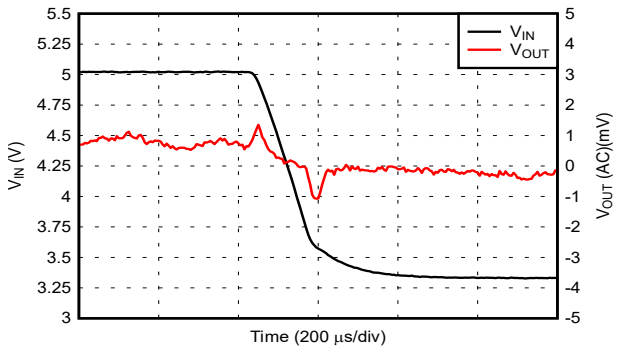
Slew Rate = 10V/ms

Figure 6-26. Line Step: 5V to 3.3V With I_{OUT} = 1.8A



Slew Rate = 10V/ms

Figure 6-27. Line Step: 3.3V to 5V AC Coupled

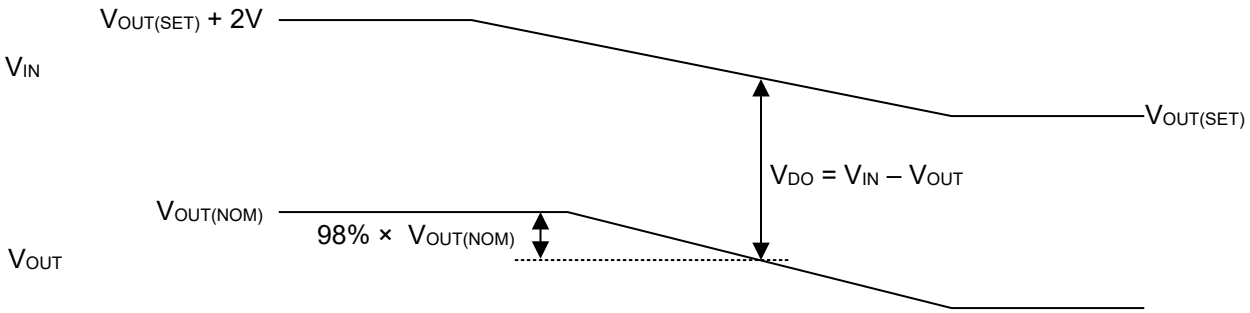


Slew Rate = 10V/ms

Figure 6-28. Line Step: 5V to 3.3V AC Coupled

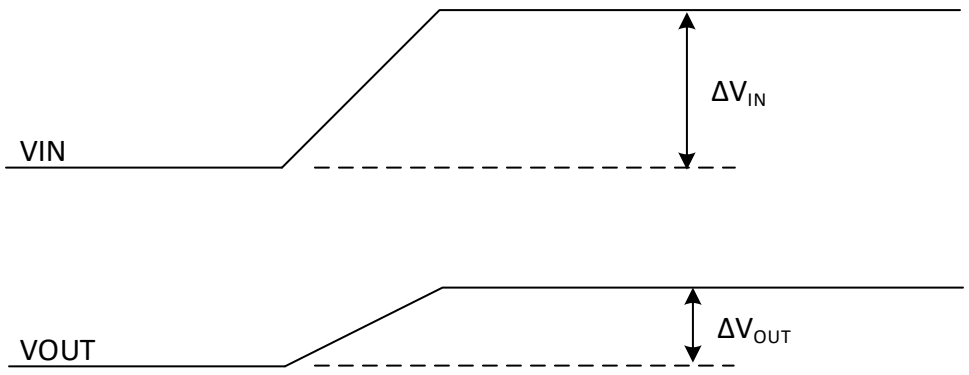
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7 Parameter Measurement Information



A. $V_{OUT(SET)}$ is the configured output voltage of the regulator using the feedback resistors, $V_{OUT(NOM)}$ is the measured output voltage. V_{IN} is set 2V above the output (limited to 14V maximum) and is decreased to the output voltage set point ($V_{OUT(SET)}$). When V_{OUT} falls to 98% of the nominal value ($V_{OUT(NOM)}$), the dropout voltage is recorded.

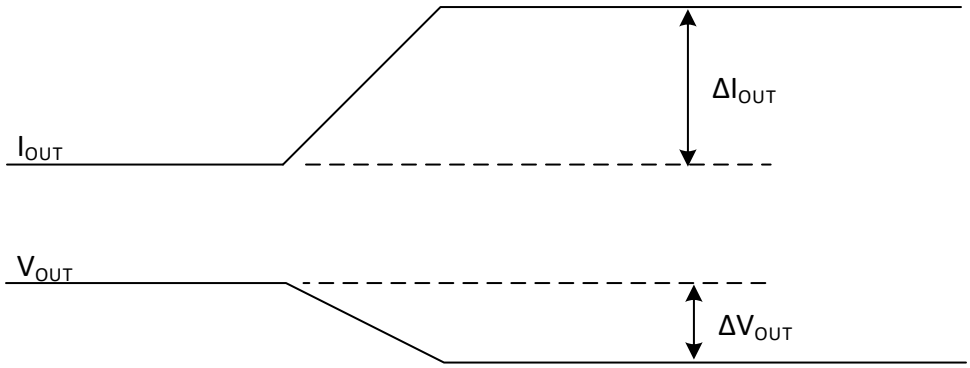
Figure 7-1. Dropout



A. ΔV_{OUT} / ΔV_{IN} = 100µV/V (typ). This means for a 1V change in V_{IN} (ΔV_{IN} = 1V), there will be a 100µV change in V_{OUT} (ΔV_{OUT} = 100µV). Line regulation is a DC parameter; therefore this waveform can only be considered valid after transients die out or for a slow V_{IN} slew rate.

Figure 7-2. Line Regulation

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A. ΔV_{OUT} / ΔI_{OUT} = 4mV/A (typ). This means for a 1A change in I_{OUT} (ΔI_{OUT} = 1A), there will be a 4mV change in V_{OUT} (ΔV_{OUT} = 4mV). Load regulation is a DC parameter; therefore this waveform can be considered valid after transients die out or for a slow I_{OUT} slew rate.

Figure 7-3. Load Regulation

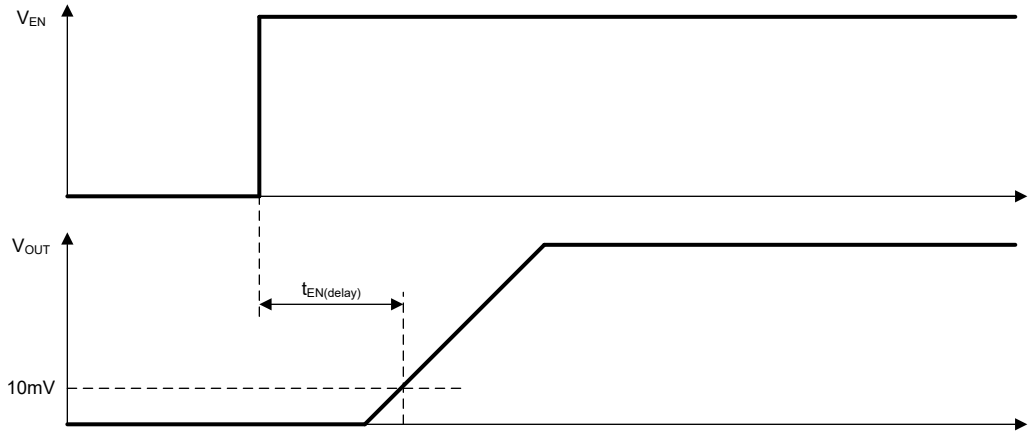


Figure 7-4. Enable Propagation Delay

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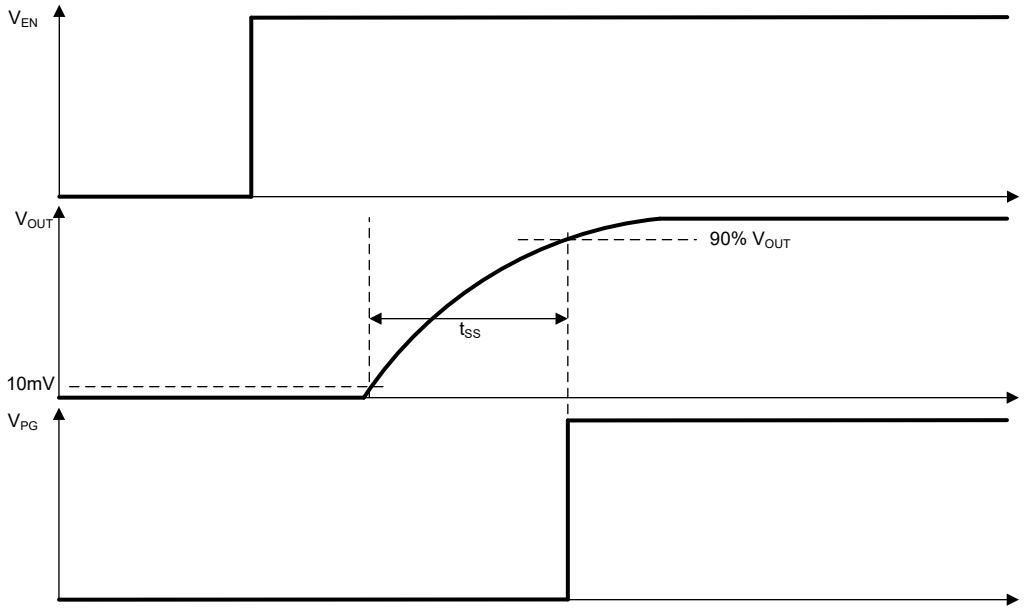


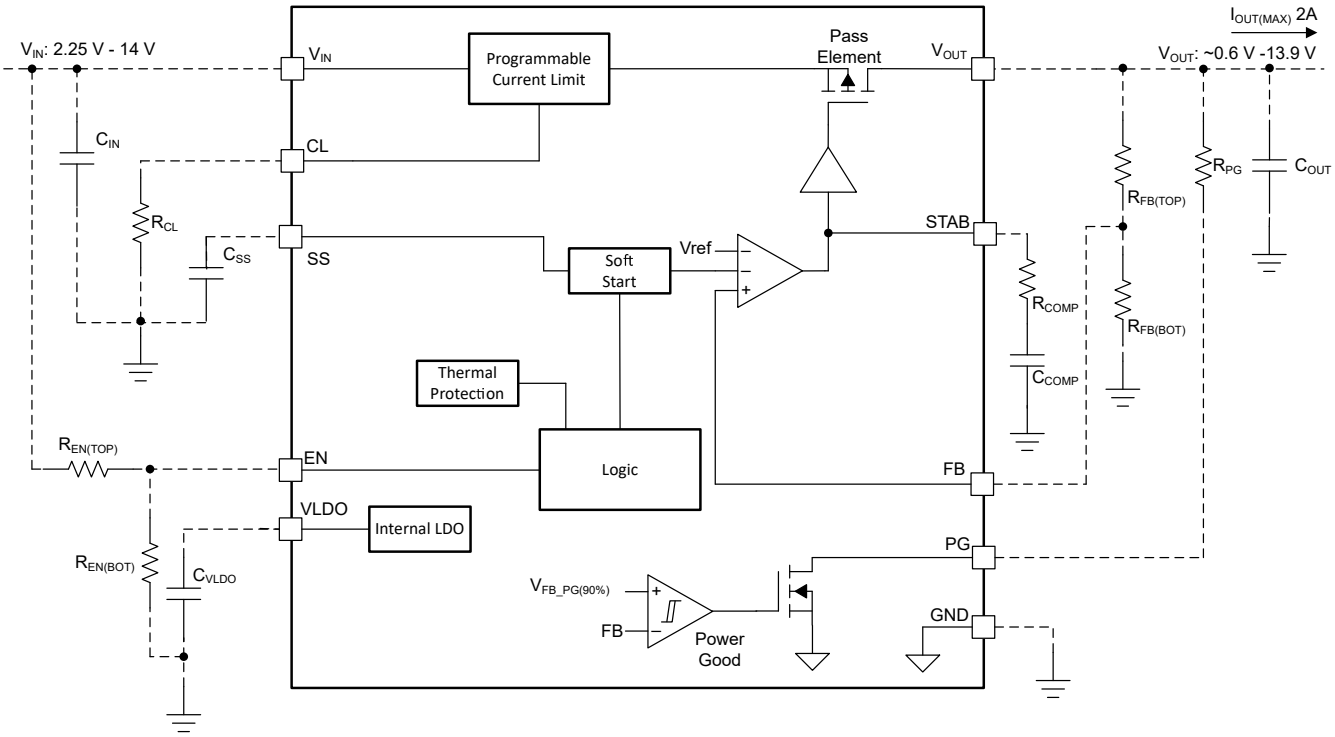
Figure 7-5. Soft Start Time

8 Detailed Description

8.1 Overview

The TPS7H1121 (TPS7H1121-SP and TPS7H1121-SEP) is a radiation-hardened low dropout linear regulator (LDO) which operates over a wide range of input voltages. The TPS7H1121 is optimized for powering devices in a space environment by using a PMOS pass element which is capable of sourcing up to 2A over a 2.25V to 14V input.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1121 can be set to a user-programmable level between 0.6V and 13.9V. Achieve this by using a resistor divider connected between V_{OUT}, FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB}, and R_{BOTTOM} connected between V_{FB} and GND.

Use Equation 5 to determine V_{OUT}.

$$V_{OUT} = \frac{\left(R_{FB(TOP)} + R_{FB(BOT)}\right) \times V_{FB}}{R_{FB(BOT)}} \quad (1)$$

where

- V_{FB} = 0.596V (typ)

8.3.2 Enable

When the enable pin is low, the device enters shutdown mode and does not regulate the output voltage. Normally, an external resistor divider from V_{IN} to GND is used to feed EN. Regulation commences when the $V_{EN(rising)}$ threshold and V_{IN} UVLO, 2V (typ) are exceeded.

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Connection of the Enable pin directly to V_{IN} is possible when V_{IN} is below the Recommended Operating level of 7V; if a higher voltage level is to be provided to the Enable pin, then a simple voltage divider can be applied, refer to Equation 2 for resistor sizing guidance at the desired turn-on voltage.

$$V_{IN(rising)} = V_{EN(rising)} \times (R_{EN_TOP} + R_{EN_BOT}) / R_{EN_BOT} \quad (2)$$

Similarly, a $V_{IN(falling)}$ voltage can also be calculated using Equation 3. The $V_{IN(rising)}$ and $V_{IN(falling)}$ can be thought of as configurable UVLO (under voltage-lockout) thresholds.

$$V_{IN(falling)} = V_{EN(falling)} \times (R_{EN_TOP} + R_{EN_BOT}) / R_{EN_BOT} \quad (3)$$

While the TPS7H1121 will turn-on at a voltage of V_{EN} of 0.6V (typ), it is recommended that the final value is above 0.8V. This is to ensure appropriate margin above the enable threshold during normal operation to prevent SEFIs during exposure to heavy ions. This recommendation is achieved by satisfying Equation 4.

$$V_{IN(final)} \times R_{EN_BOT} / (R_{EN_TOP} + R_{EN_BOT}) = V_{EN(final)} > 0.8V \quad (4)$$

Alternatively, the EN pin can be driven directly from a micro-controller or FPGA. The low voltage threshold of the enable pin aids in support of 1.1V, 1.8V, 2.5V, and 3.3V logic levels. Similarly a final V_{EN} above 0.8V for direct logic level driving is recommended (this is typically easily achieved with standard logic levels).

8.3.3 Dropout Voltage V_{DO}

Dropout voltage, V_{DO}, is defined as the input voltage minus the output voltage (V_{IN} - V_{OUT}) where the output voltage falls to 98% of the initial value at the indicated current. See Figure 7-1 for the test waveforms used to measure dropout. The dropout voltage is higher at lower values of V_{IN}; therefore, dropout voltage is specified across different conditions in Electrical Characteristics.

In dropout, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

When V_{IN} is below 3V, the error amplifier operates with less headroom versus what is present for a V_{IN} range of 3V to 14V; the reduction in headroom causes higher dropout voltage for V_{IN} voltages less than 3V(see typical dropout performance graphs Figure 6-1 through Figure 6-6).

8.3.4 Output Voltage Accuracy

The TPS7H1121 features an accurate voltage reference, which is essential in minimizing the intrinsic error of the LDO.

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage. The accuracy specification in the Electrical Characteristics table presents two operating regions, one in which the V_{IN} is above 3V and one when V_{IN} is in the "low-input" voltage region (2.25V ≤ V_{IN} ≤ 3V).

The ±1.5% specification applies across the complete temperature range of –55°C to 125°C, across the input voltage range of 3V ≤ V_{IN} ≤ 14V, when the dissipated power is ≤3W, and up to the full load (10mA ≤ I_{OUT} ≤ 2A).

When V_{IN} is below 3V (2.25V ≤ V_{IN} ≤ 3V), the output voltage accuracy is adjusted to ±1.8%.

A few additional details to the measurement are noted:

- The range of V_{IN}, I_{OUT} and temperature mean the specification applies across all load and temperature combinations. This is accomplished by testing multiple bias conditions that cover various corners.
- Footnote 3 in Section 6.5 specifies that the measurement is done with a power dissipation limit that is limited to a maximum 3W. This is due to tester thermal limitations.
- The test conditions specify a minimum of 10mA and not 0mA for more robust accuracy measurements. However, in a normal application the TPS7H1121 device does not have a minimum load current for stability

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- TI does not recommend including the following error terms into the V_{ACC} specification as the following terms are inherently covered by the V_{ACC} parameter:
  - V_{FB} accuracy
  - $\Delta V_{OUT}/\Delta V_{IN}$ (line regulation)
  - $\Delta V_{OUT}/\Delta I_{OUT}$ (load regulation)
  - V_{OUT} tempco
- The error due to the feedback resistors, such as the specified tolerances can be added to the V_{ACC} specification.
- R_{TOP} is fixed to 4.53kΩ in the accuracy testing. If using higher value resistors, the error due to I_{FB} leakage increases. While this is generally negligible, accuracy calculations can include this contribution.
- For additional information on determining accuracy see Section 9.2.2.2.

8.3.5 Output Noise

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits. The TPS7H1121 output noise is typically 35μV_{RMS}.

When an external compensation network is connected to the STAB pin, the applied network can reduce the loop bandwidth; therefore, the internal circuitry is less capable to minimize internally generated noise. Figure 6-20 shows the noise performance difference when configured with and without an external compensation network (note: R_{Comp} = 20kΩ and C_{Comp} = 1nF).

8.3.6 Power Supply Rejection Ratio (PSRR)

The PSRR (power supply rejection ratio) of the TPS7H1121, is the amount of attenuation of the input noise at V_{IN}, to the output, V_{OUT}. PSRR is mathematically defined in Equation 5.

$$\text{PSRR} = 20 \times \log_{10}\left(\frac{V_{IN(AC)}}{V_{OUT(AC)}}\right) \quad (5)$$

The input noise is generally dominated by the switching ripple of an upstream converter. This noise occurs at the switching frequency and associated harmonics.

When using an external compensation network and the loop bandwidth is reduced, then the overall PSRR diminishes as well. Figure 6-22 illustrates the trade off in a typical application in which the applied compensation network has reduced the loop band-width, but improved system stability (R_{Comp} = 20kΩ, C_{Comp} = 1nF).

8.3.7 Soft Start

Connecting a capacitor (C_{SS}) from the SS terminal to GND slows down the output voltage ramp rate. The soft-start capacitor charges up to 0.6V. Equation 6 determines the required soft start capacitor value C_{SS} with a user specified soft -start time t_{SS}.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} \quad (6)$$

where

- t_{SS} = soft-start time
- I_{SS} = 2μA (typ)
- V_{REF} = 0.6V (typ)

See Typical Graph Figure 6-14 for Soft Start Current vs Temperature Performance.

8.3.8 Power Good (PG)

Power Good terminal is an open-drain connection and can be used to sequence multiple LDOs. The PG terminal will be pulled low until the output voltage reaches 95% (typ) of its final level. At that point, the PG pin will be pulled up through the external resistor divider. Since the PG pin is open drain, it can be pulled up to any voltage as long as it does not exceed the recommended maximum of 7V listed in Electrical Characteristics.

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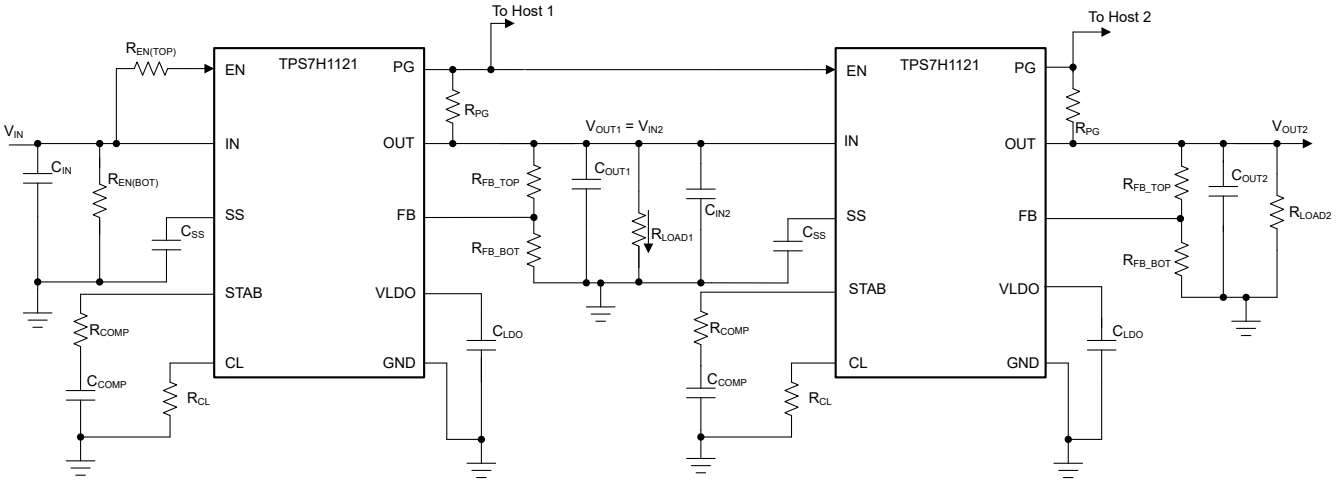


Figure 8-1. Sequenced Power Good

8.3.9 Stability

8.3.9.1 Stability

Traditional stability margins (such as gain margin ≥ 6dB and phase margin ≥ 50º) for space rated devices are often more onerous than industrial and consumer electronics. The TPS7H1121 is designed to support a wide range of space rated output capacitors (generally 22µF to 220µF) while maintaining a 6dB gain margin and 50º phase margin without utilizing the included STAB pin for external compensation.

In addition to wide intrinsic stability of the TPS7H1121, the STAB pin can be utilized to insert an external RC compensation network that ties directly to the output of the error amplifier. This architecture, as depicted in Figure 8-2, illustrates how an external compensation network is directly inserted prior to the pass element's buffer, which maximizes the efficacy of the inserted RC compensation circuit.

This level of efficacy for an external compensation network enables end-users of the TPS7H1121 to conduct in depth stability analysis and widen stability margins for the applied output load. Additionally, it enables utilization of output capacitors as low as 6.8µF while allowing flexibility in managing low-ESR capacitors.

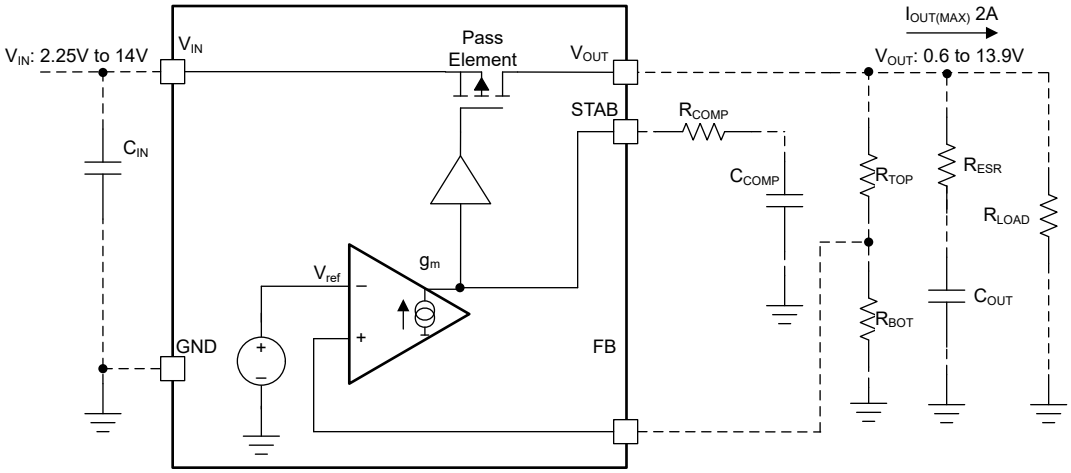


Figure 8-2. Simplified Compensation Schematic

8.3.9.2 STAB Pin

The STAB (stability) pin of the TPS7H1121 is designed to provide direct access to the error amplifier of the controller. Insertion into the control circuitry of the LDO facilitates detailed stability analysis and fine tuning of the stability performance of the LDO.

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The TPS7H1121 has a wide envelope in which typical gain and phase margin is in excess of 6dB and 50º (with output capacitance ranging from 22µF ≤ C_{OUT} ≤ 220µF). However, external compensation is provided using the STAB pin in which the R_{COMP} and C_{COMP} network can be utilized to further optimize the stability performance of the TPS7H1121 if desired. TI recommends that an external network is applied for low C_{OUT} applications or for special concerns in which maximum stability margin is necessary. For further details on how to implement Type II and III Compensation, view section Section 9.2.2.9 or Demystifying Type II and Type III Compensators Using OpAmp and OTA for DC/DC Converters.

8.3.10 Programmable Current Limit

Brick-wall current limit, also known as constant current limit, is shown in Figure 8-3. In this mode, once I_{PCL} is reached and the current limit circuitry has time to respond, the TPS7H1121 LDO enters constant current regulation mode. In other words, the output voltage reduces to whatever value is needed to keep the output current at I_{LIM}. Once the fault is removed the device resumes regulation.

Due to the high power dissipation in brick-wall current limit, there is the possibility that the TPS7H1121 enters thermal shutdown which causes the device to stop regulation until the TPS7H1121 cools enough to exit thermal shutdown.

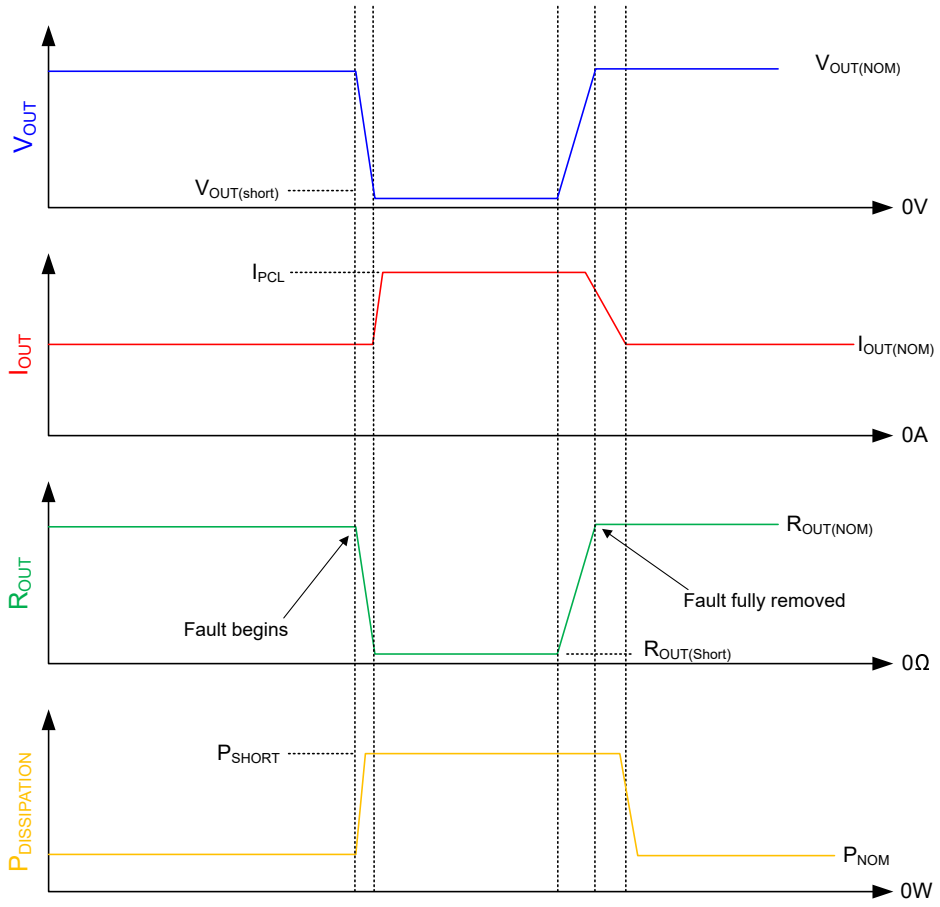


Figure 8-3. Simplified Brick-Wall Current Limit Waveforms

The programmable current limit's accuracy tightens with increased load current; Table 8-1 shows the recommended E96 value with a typical accuracy.

With the stipulated accuracy of the current limit, the programmable current limit resistor R_{CL} needs to be selected to accommodate the negative portion of the accuracy current limit circuitry. Additionally, a 20% headroom margin is recommended to prevent the current limit from intervening during nominal operation. For example an application with a nominal load of 1A can have a minimum programmable current limit setting of

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1.4A / 97.6kΩ; the setting for a 97.6kΩ programmable current limit has a negative accuracy of -25% which leads a minimum intervening current limit of 1.05A.

For example an application with a nominal load of 1A is recommended to have a minimum intervening current of 1.2A; which yields a nominal current limit of 1.6A. Therefore an R_{CL} setting of 80.6kΩ with a negative accuracy of -25% leads to a minimum intervening current limit of 1.2A; which complies with the recommended 20% headroom.

Table 8-1. Recommended Current Limit Setting Resistor

Ceramic, Package Designation: HFT22			Plastic, Package Designation: PWP24		
PROGRAMMABLE CURRENT LIMIT SETTING (A)	E96 (kΩ)	ACCURACY	PROGRAMMABLE CURRENT LIMIT SETTING (A)	E96 (kΩ)	ACCURACY
0.32	442	±35%	0.35	442	±50%
0.4	392		0.4	383	
0.5	332		0.5	301	
0.6	267	±30%	0.6	243	±40%
0.7	205		0.7	210	
0.75	174		0.8	182	
0.8	169		0.835	176	
0.9	158		0.9	158	
1	143		1	143	
1.1	133	±25%	1.1	127	±30%
1.2	121		1.2	115	
1.3	110		1.3	107	
1.4	97.6		1.4	97.6	
1.5	88.7		1.5	90.9	
1.55	82.5		1.6	84.5	
1.6	80.6		1.66	82.5	
1.7	78.6		1.8	75	
1.8	75		1.9	71.5	
1.9	71.5		2	66.5	
2	69.8		2.1	63.4	
2.1	66.5	±20%	2.2	60.4	±25%
2.2	63.4		2.3	57.6	
2.3	60.4		2.4	54.9	
2.4	57.6		2.5	52.3	
2.5	54.9		2.6	49.9	
2.6	52.3		2.7	48.7	
2.7	49.9		2.8	46.4	
2.8	46.4		2.9	45.3	
2.9	44.2		3	43.2	
3	41.2		3.15	41.2	

8.3.11 Thermal Shutdown

Upon exceeding the TPS7H1121 thermal shutdown temperature limit, the integrated thermal shutdown circuitry activates to turn-off the device when the die temperature exceeds $T_{SD(enter)}$. As the die cools below $T_{SD(exit)}$, the device resumes regulation. The typical $T_{SD(enter)}$ of 160°C and $T_{SD(exit)}$ of 130°C provides a large hysteresis (30°C typical). The large hysteresis is intended to allow the device to sufficiently cool before attempting to resume regulation.

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8.4 Device Functional Modes

8.4.1 Enable / Disable

The table below shows the device functional modes:

Table 8-2. Device Functional Modes

EN PIN	DEVICE STATUS
High	Regulation mode
Low	Shutdown mode

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H1121-SP LDO linear regulator is targeted space environment applications. This regulator has various features such as low dropout, soft start, output current limit, and error amplifier access via STAB pin.

9.2 Typical Application

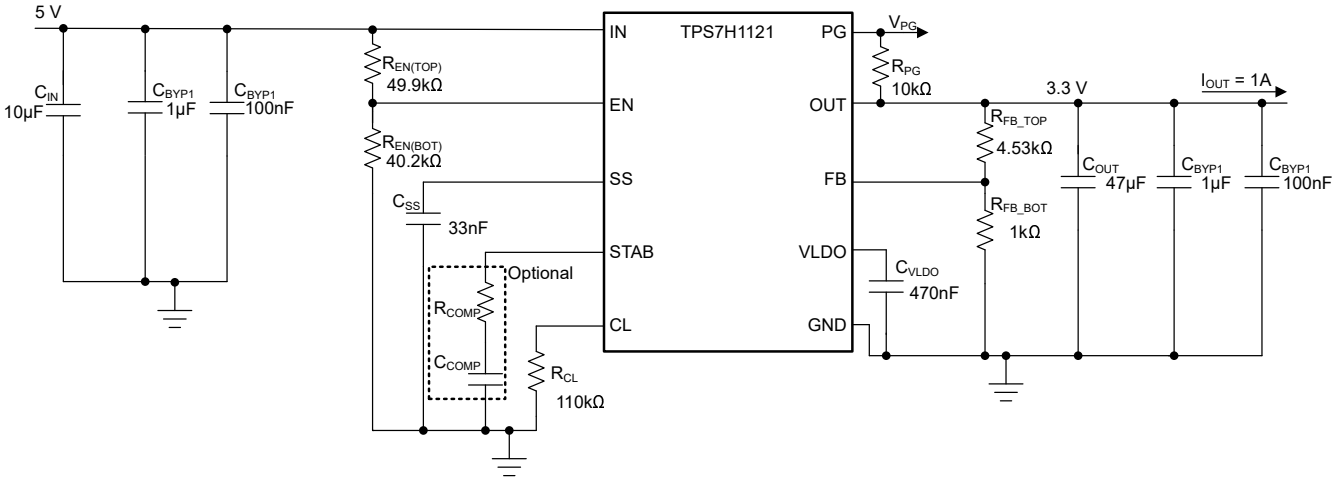


Figure 9-1. Application Schematic

9.2.1 Design Requirements

This example highlights a design using the TPS7H1121 based on the evaluation module. For more details, please refer to the EVM user's guide, *TPS7H1121EVM-CVAL Evaluation Module (EVM) User's Guide* (SLVUCX9). A few parameters must be known to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

Table 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5V ± 5%
Output voltage	3.3V ± 5%
Maximum output current	1A (typ)
$V_{IN(turn\text{-}on\ threshold)}$	1.35V (typ)
$V_{OUT(PG\ assertion\ threshold)}$	90% of $V_{OUT(final)}$ (typ), 2.97V
Soft start time, t_{SS}	10ms
Minimum phase margin	50°
Maximum gain margin	6dB

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9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Configuration

The output voltage is configured using Equation 1.

Therefore 0.1% feedback resistors are selected with $R_{FB(TOP)}$ = 1.01kΩ and $R_{FB(BOT)}$ = 4.53kΩ; using resistors with a 1% tolerance is acceptable, however this directly contributes a 1% error to the output voltage.

9.2.2.2 Output Voltage Accuracy

To determine the overall output voltage accuracy, refer to the device voltage accuracy V_{ACC} from the Electrical Characteristics, the top and bottom feedback resistors ($R_{FB(Top)}$ and $R_{FB(BOT)}$).

$$\text{System}_{(\text{error})} = V_{ACC} + R_{(\text{error})} \tag{7}$$

When the input voltage V_{IN} is below 3V, the error amp is operating with a reduced head room such that output accuracy performance is widened to ±1.8%; for this example V_{IN} is above 3V, therefore the standard ±1.5% accuracy can be applied.

For the selected 0.1% feedback resistors, the calculated error is shown in Equation 8, this assumes an uncorrelated error and the errors are added as the sum of the resistors' error squared.

$$R_{(\text{error})} = \sqrt[2]{\left(0.1^2 + 0.1^2\right)} = \pm 0.14\% \tag{8}$$

The negative and positive system error's are summed with the results for this example shown below in equations Equation 9 and Equation 10.

$$\text{System}_{(\text{neg_error})} = -1.5\% + -0.14\% \tag{9}$$

$$\text{System}_{(\text{pos_error})} = 1.5\% + 0.14\% \tag{10}$$

Adding the following errors together results in an accuracy of ±1.64%.

Figure 9-1 shows an R_{TOP} feedback resistor of 4.53kΩ and an R_{BOT} feedback resistor value of 1kΩ; when using an R_{TOP} less than 4.53kΩ, consider the influence and variation of the feedback current (I_{FB}) on the overall feedback accuracy.

9.2.2.3 Enable Threshold

The desired turn-on threshold is 2.25V. This means that as the V_{IN} rail is turned-on and begins rising, the TPS7H1121 commences turning-on as soon as V_{IN} reaches 2.25V. While this is not enough headroom from V_{IN} to V_{OUT} for final regulation, the regulator initiates start-up and V_{IN} progresses to the final voltage of 5V. If desired, a higher voltage turn-on threshold can be selected (for example, 3.5V), provided the desired voltage is below 7V.

Using Equation 1 and selecting an $R_{EN(TOP)}$ value of 49.9kΩ, the $R_{EN(BOT)}$ can be calculated as shown in Equation 11.

$$R_{EN(BOT)} = \frac{V_{EN(\text{rising})} \times R_{EN(TOP)}}{V_{IN(\text{rising})} - V_{EN(\text{rising})}} = \frac{0.605\ \text{V} \times 49.9\ \text{k}\Omega}{2.25\ \text{V} - 0.605\ \text{V}} = 18.4\ \text{k}\Omega \tag{11}$$

Using E192 resistor values, $R_{EN(BOT)}$ is chosen to be 18.4kΩ.

To comply with the maximum pin voltage for Enable use Equation 4. As shown in Equation 12, $V_{EN(final)}$ = 1.35V which is less than the recommended maximum of 7V and above the recommended minimum final value of 0.8V.

$$V_{EN(final)} = V_{IN(final)} \times \left(\frac{R_{EN(BOT)}}{R_{EN(BOT)} + R_{EN(TOP)}}\right) = \frac{5V \times 18.4k\Omega}{18.4k\Omega + 49.9k\Omega} = 1.35V \tag{12}$$

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9.2.2.4 Soft Start Capacitor

The evaluation module is specified to have a soft start time of t_{SS} of 10ms, the soft start capacitor value can be calculated with Equation 6.

$$C_{SS} = \frac{20\ ms \times 2\ \mu A}{0.6\ V} = 33.3\ nF \quad (13)$$

Therefore a 33nF ceramic capacitor is selected to configure the soft start time.

9.2.2.5 Programmable Current Limit Resistor

The evaluation module is populated with a current limit setting resistor to provide a I_{lim} = 3A; to configure a lower current limit see Table 8-1.

9.2.2.6 Characterization of Overcurrent Events That Exceed Thermal Limits

High power overcurrent events are characterized by duration, the input and output voltage occurs at, and the resulting current. In these high power overcurrent conditions, the dissipated power in the pass element becomes much greater than nominal operating conditions. Depending on the specific overcurrent conditions, the device heats up until reaching thermal shutdown. However, depending on the specific overcurrent event, the device may heat faster than the thermal shutdown circuitry can respond.

Table 8-1 specifies resistors values for a desired current limit setting and the anticipated accuracy of the programmable current limit at the specified setting.

The magnitude of the over-current condition intensifies as a function of the VIN - VOUT differential and pulse width (for faults to be evaluated as DC, a 1s pulse can be used). By combining the input and output voltage differential, fault pulse width, and programmable current limit setting, a recommended programmable current limit protection area is derived as shown in Figure 9-2 which is characterized using validation hardware for the TPS7H1121 (ceramic and plastic package) under laboratory ambient conditions (TA = 25ºC). The effective thermal resistance of the PCB thermal pad is calculated to be RTH(PCB) = 5ºC/W; this calculation takes into account the thermal via diameter, spacing, and board layers. Applied faults of pulse width of 10ms, 100ms and 1s are applied until the device is no longer functional; the applied voltage and programmed current are then adjusted lower on subsequent units until the curve is determined.

For the ceramic HFT package, 3A is a recommended maximum programmable current limit setting as the 20% accuracy has a maximum current limit of 3.6A, which is below the Absolute Maximum rating of 3.9A.

For the PWP24 (plastic) package, 3.15A is the recommended maximum programmable current limit setting. With an accuracy of 24%, the maximum current limit is 3.9A, which meets the Absolute Maximum Rating of 3.9A.

The depicted curve is very dependent on assumed ambient temperatures, package thermal resistance, PCB thermal resistances and nature of the applied short; the curve below is only applicable for the validation hardware utilized.

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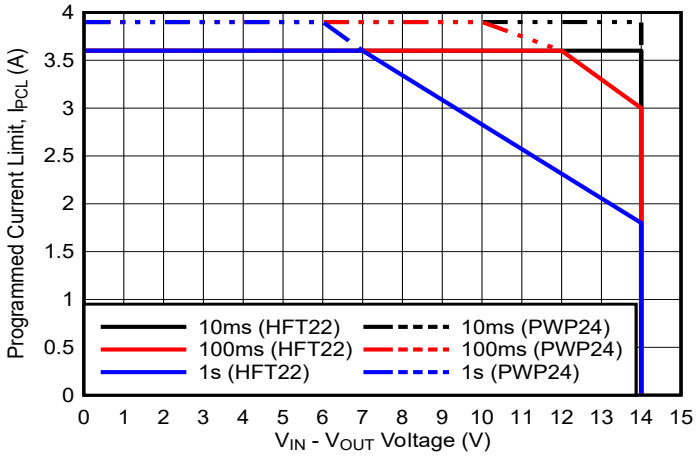


Figure 9-2. Programmable Current Limit Protection Area

9.2.2.7 Power Good Pull Up Resistor

TI recommends to use a pullup resistor between 10kΩ to 100kΩ; the evaluation module is configured with 10kΩ.

9.2.2.8 Capacitors

TPS7H1121 can use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. Table 9-2 highlights some of the supported capacitors. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

TI recommends to use a polymer or tantalum capacitor along with a 0.1µF and 1µF ceramic capacitors implemented as bypass capacitors. The device is stable for input and output tantalum, polymer or ceramic X7R capacitor values or networks with bulk capacitances ranging from 6.8µF to 880µF (some values within this range benefit from the use of external compensation). However, the dynamic performance of the device varies based on load conditions, the capacitor values used (including ESR) and utilization of the external compensation STAB pin. TI recommends for bulk output capacitance less than 22µF and capacitance exceeding 220µF, generally use an external compensation network applied to the STAB pin to achieve robust stability margins. TI recommends thorough stability analysis to verify that requisite stability margins are attained across the entirety of the mission profile.

Bulk output capacitor ESR is significantly affects system stability; the TPS7H1121 is designed to achieve wide gain and phase margins with tantalum or polymer surface mount capacitors with low ESR. Ceramic capacitors are also supported, however ceramic capacitors have lower output capacitance and ESR such that an external compensation network can be necessary to achieve stability targets.

Table 9-2. TPS7H1121 Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS (CAPACITOR, VOLTAGE, ESR at 100kHz, Case Size)	TYPE	VENDOR
TES226K035	22µF, 35V, 43mΩ, 7343	Tantalum - MnO2	AVX
TBME476K025LBLC9	47µF, 25V, 65mΩ, 7343	Tantalum - MnO2	AVX
T540D227K010AH	220µF, 10V, 24mΩ, 7343	Tantalum - Polymer	Kemet

9.2.2.8.1 Hybrid Output Capacitor Network

The recommendation for the TPS7H1121 is to utilize ceramic bypass capacitors with a tantalum bulk capacitor. The combination of a tantalum and ceramic capacitor forms a hybrid network capacitor; see application report How to Calculate the Load Pole and ESR Zero When Using Hybrid Output Capacitors (SLVAE26) for how to analytically implement and assess the applied output capacitor network.

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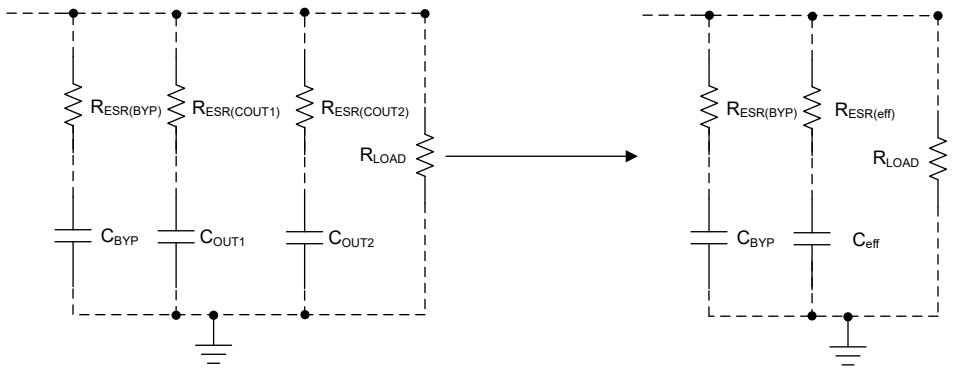


Figure 9-3. Recommended Hybrid Output Capacitor Network Simplification

TI recommends when conducting analytical analysis of the output capacitor network to only combine capacitors and the associated parasitic parameters which are identically specified (combine identical tantalums, keep bypass caps and tantalum caps distinct from each other in analysis). In the figure above, capacitors C_{OUT1} and C_{OUT2} are combined into effective capacitance and ESR of C_{eff} and R_{eff} with the bypass cap C_{BYP} being excluded.

9.2.2.9 Frequency Compensation

Applying a simple RC compensation network to the STAB pin as optionally depicted in Figure 9-1 enables the end user to optimize the phase and gain margin of the system's stability.

The addition of this RC compensation network introduces 2 poles and 1 zero to the system. Firstly, a low frequency pole is present which can be approximated in more detailed analytical analysis.

The compensation pole frequency, $f_{p(COMP)}$, is approximated using Equation 14.

$$f_{p(COMP)} = \frac{C_{COMP} + C_{OTA}}{2\pi \times R_{COMP} \times C_{COMP} \times C_{OTA}} \quad (14)$$

where

- C_{OTA} = 100pF (typical sim)

The compensation zero frequency, $f_{z(COMP)}$, is approximated by Equation 15.

$$f_{z(COMP)} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (15)$$

The open loop gain A_{OL} is approximated by Equation 16.

$$A_{OL} = g_{m(OTA)} \times R_{OTA} \quad (16)$$

where

- $g_{m(OTA)}$ = 5mS (typical sim)
- R_{OTA} = 220kΩ (typical sim)

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9.3 Power Supply Recommendations

This device is designed to operate with an input voltage supply of up to 14V. The minimum input voltage must exceed the V_{IN} UVLO, 2V (typ), and provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

9.4 Layout

9.4.1 Layout Guidelines

- For best performance, TI recommends all traces be as short as possible.
- Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
- Place the bulk output capacitors (generally tantalum or tantalum polymer) near the OUT pins of the device.
  - If a ceramic output capacitor is used, place the capacitor near the point of load.

9.4.2 Layout Example

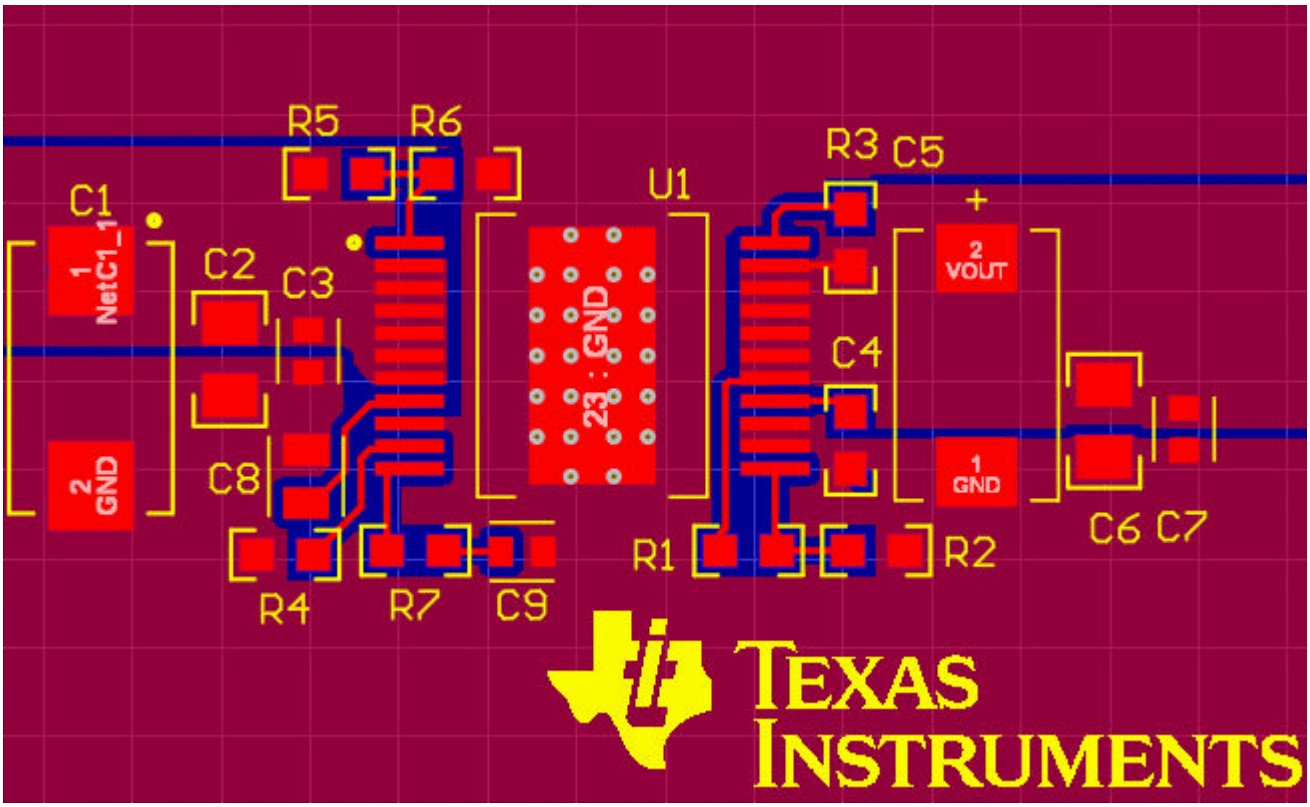


Figure 9-4. Printed Circuit Board Layout Example

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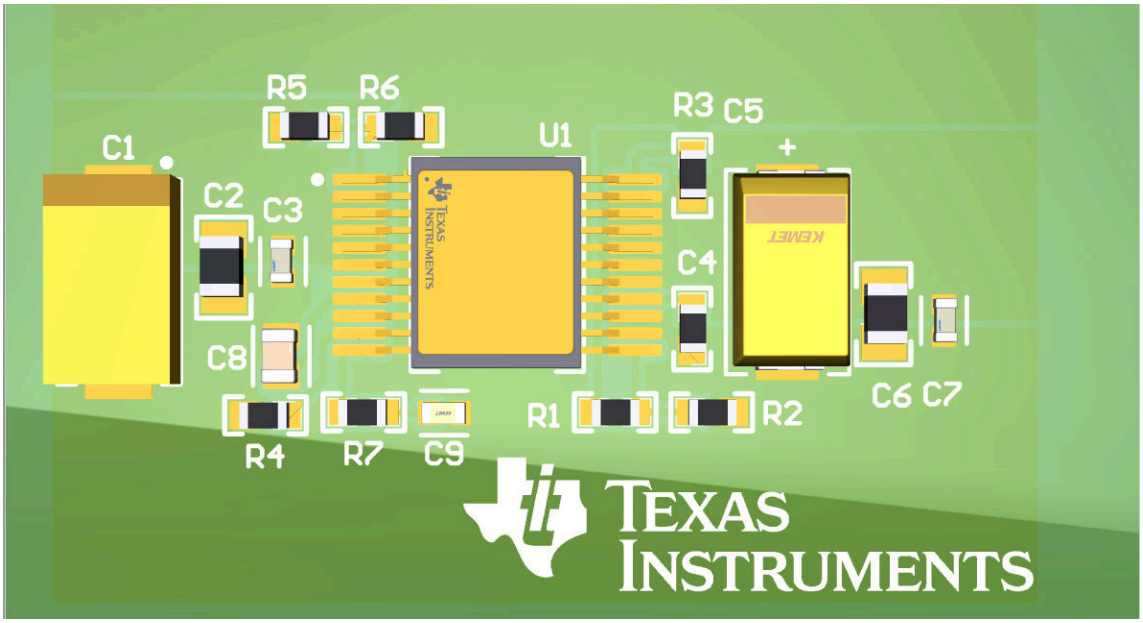


Figure 9-5. Printed Circuit Board Layout Example: 3D View

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TI Engineering Evaluation Units vs. MIL-PRF-38535 QML Class V Processing*
- Texas Instruments, *Demystifying Type II and Type III Compensators Using Op-Amp and OTA for DC/DC Converters*
- Texas Instruments, *TPS7H1121EVM-CVAL Evaluation Module (EVM)*
- Texas Instruments, *How to Calculate the Load Pole and ESR Zero When Using Hybrid Output Capacitors*
- Texas Instruments, *TPS7H1121-SEP Evaluation Module User's Guide*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2025) to Revision C (November 2025) **Page**

- Made minor grammatical and wording updates 1
- TPS7H1121-SEP status changed from Advanced Information to Production Data. 1
- Removal of "Advance Information" note for Orderable Part Number TPS7H1121-SEP in the Device Options Table. Renamed Table from "Device Options" to "Device Comparison Table". Added link to Part rating page.. 3
- Functional Block Diagram Power Good FET updated to an NMOS FET..... 18
- Added UVLO consideration to configurable turn-on..... 18
- Added additional guidance regarding the contribution of feedback resistors to output voltage accuracy calculations..... 19
- Corrected the soft-start equation V_{REF} value to 0.6V..... 20
- Changed design example soft start time to 10ms..... 25
- Changed design example turn-on threshold to 2.25V. 26
- Corrected the soft-start equation V_{REF} value to 0.6V..... 27
- Removed specific reference for ceramic hardware as the curves are valid for the validation hardware used for the ceramic and plastic packages..... 27
- Typo corrected for equation 14, added C_{OTA} to denominator..... 29
- Added additional information that the minimum input voltage includes V_{IN} UVLO..... 30
- Added link to TPS7H1121-SEP Evaluation Module User's Guide. 32

Changes from Revision A (September 2024) to Revision B (June 2025) **Page**

- TPS7H1121-SEP status changed from product preview to Advanced Information. 1
- Added separation of current limit specs based on package type..... 5
- Added the recommended current limit resistor setting values for TPS7H1121-SEP and calculation equation..... 22
- Added programmable current limit area for PWP24 package..... 27

Changes from Revision * (May 2024) to Revision A (September 2024) **Page**

- Changed TPS7H1121-SP QMLV from Advanced Information to Production Data..... 1
- Removal of "Product Preview" for part number 5962R2320301VXC in the Device Information table. 1
- Removal of "Product Preview" note for Orderable Part Number 5962R2320301VXC in the Device Options Table..... 3
- Adjusted Enable threshold values and Programmable Current Limit min and max values..... 5
- Added parameter measurement diagrams for Enable Propagation Delay ($t_{EN(delay)}$) and Soft Start Time (t_{SS})... 15
- Updated equation 12..... 26
- Added editorial changes to overcurrent events..... 27
- New frequency compensation application section in detailed design procedure..... 29

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962R2320301VXC	Active	Production	CFP (HFT) | 22	25 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	-55 to 125	5962R2320301VXC TPS7H1121MHFTV
TPS7H1121HFT/EM	Active	Production	CFP (HFT) | 22	15 | TUBE	ROHS Exempt	NIAU	N/A for Pkg Type	25 to 25	TPS7H1121HFT EVAL ONLY
TPS7H1121MPWPTSEP	Active	Production	HTSSOP (PWP) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H1121PWP
V62/23604-01XE	Active	Production	HTSSOP (PWP) | 24	250 | SMALL T&R	-	NIPDAU	Level-3-260C-168 HR	-55 to 125	7H1121PWP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS7H1121-SEP, TPS7H1121-SP :

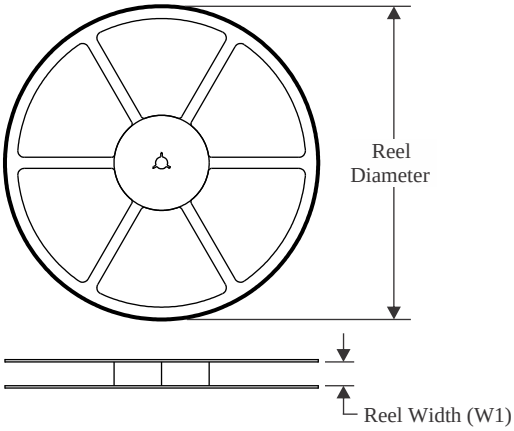
- Catalog : TPS7H1121-SEP
- Space : TPS7H1121-SP

NOTE: Qualified Version Definitions:

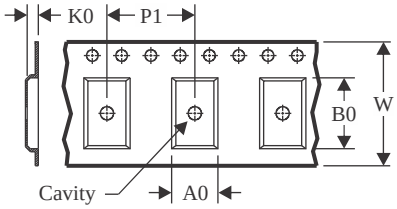
- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

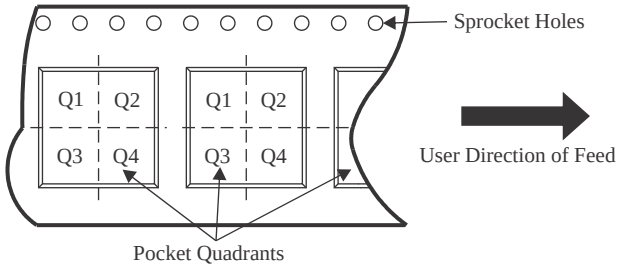


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

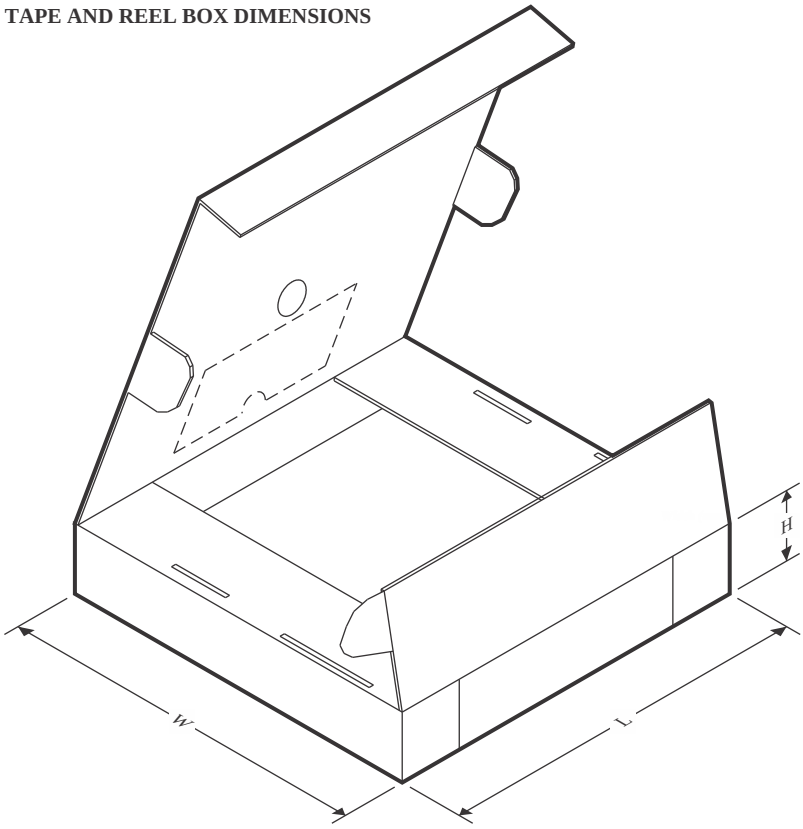
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H1121MPWPTSEP	HTSSOP	PWP	24	250	178.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

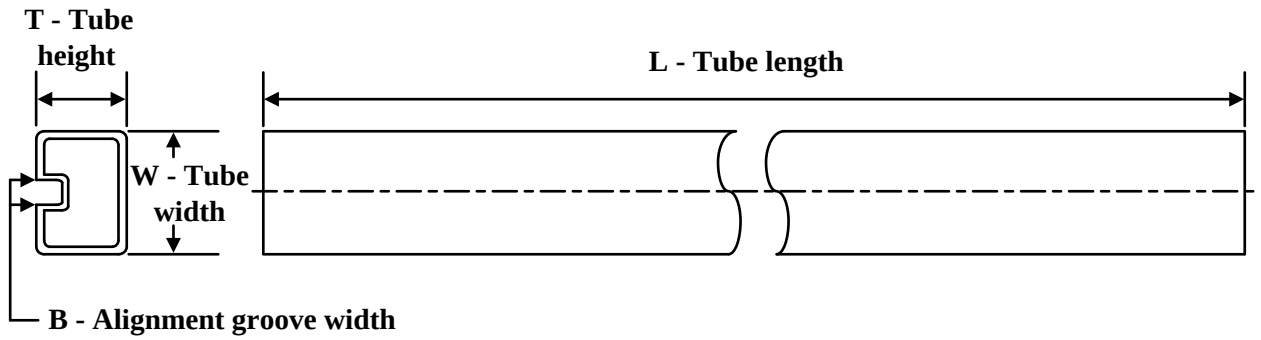
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H1121MPWPTSEP	HTSSOP	PWP	24	250	208.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R2320301VXC	HFT	CFP	22	25	506.98	32.77	9910	NA
TPS7H1121HFT/EM	HFT	CFP	22	15	506.98	32.77	9910	NA

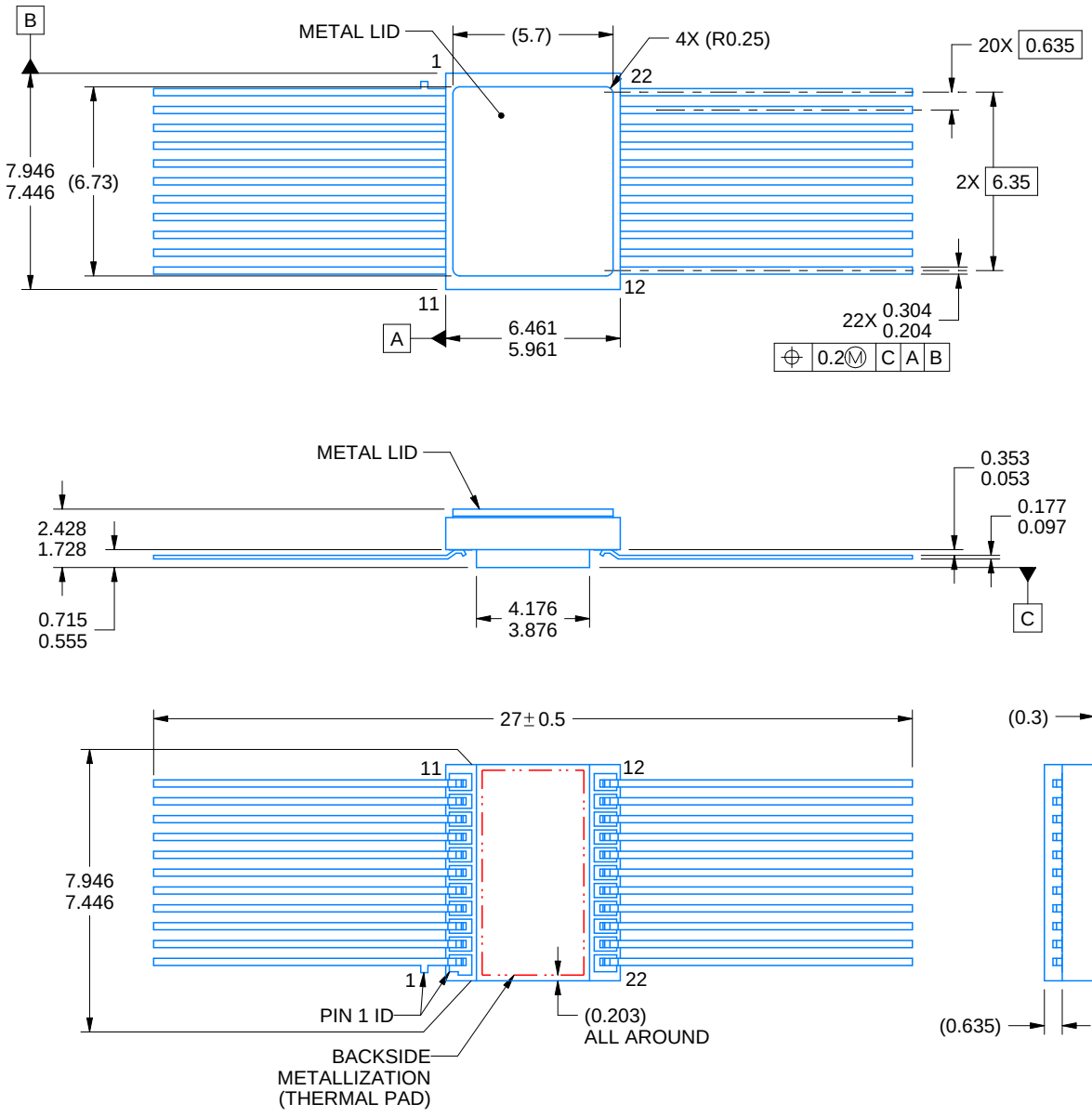


PACKAGE OUTLINE

HFT0022A

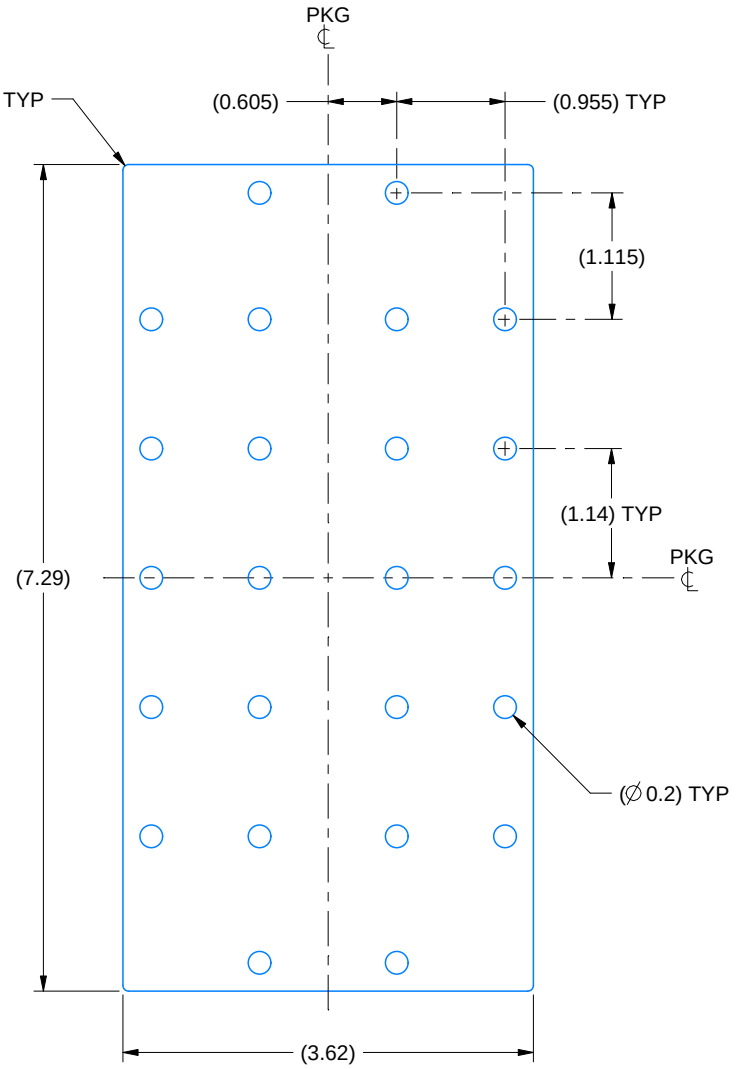
CFP - 2.428mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metalization



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

GENERIC PACKAGE VIEW

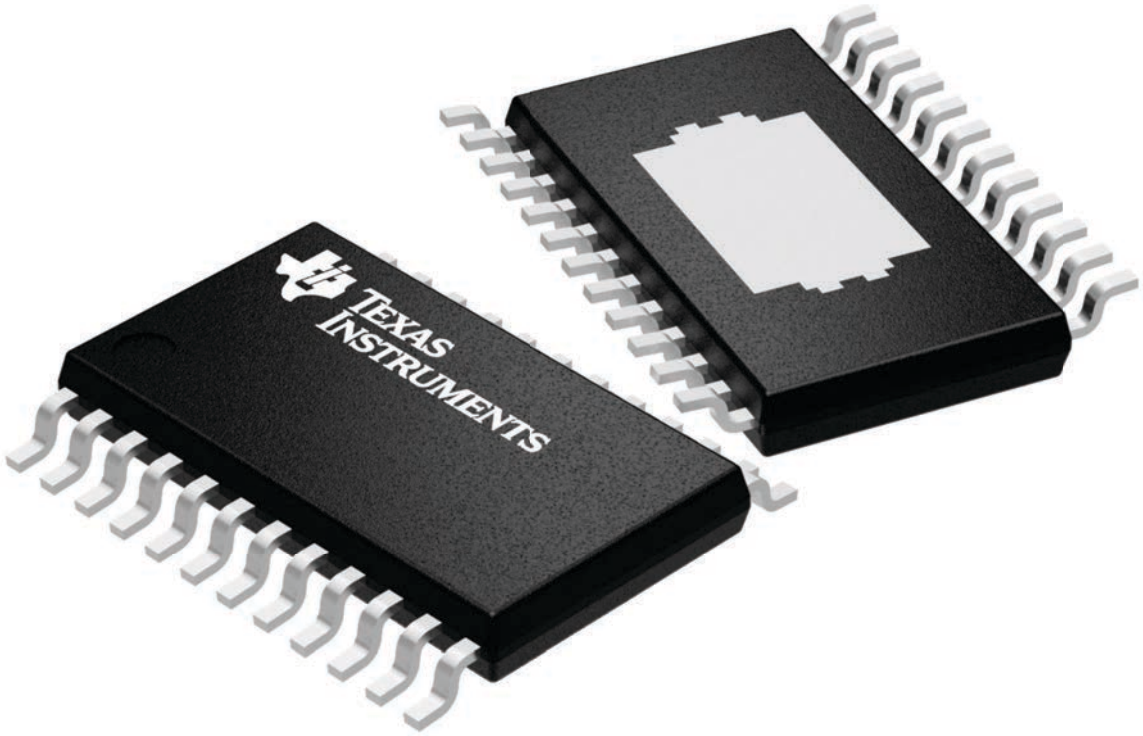
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

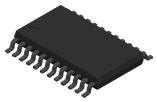
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

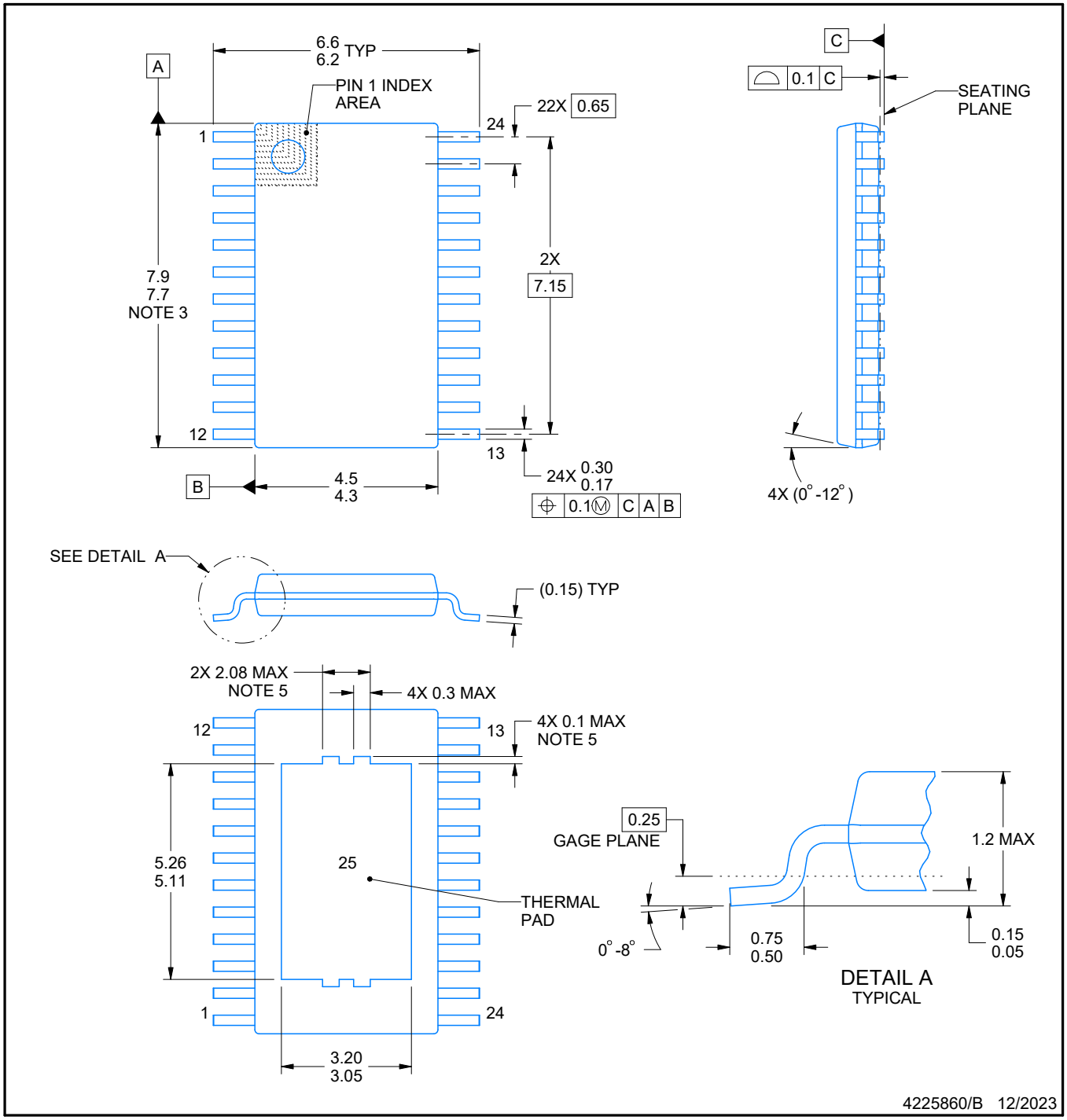
PACKAGE OUTLINE

PWP0024J



PowerPAD™ TSSOP - 1.2 mm max height

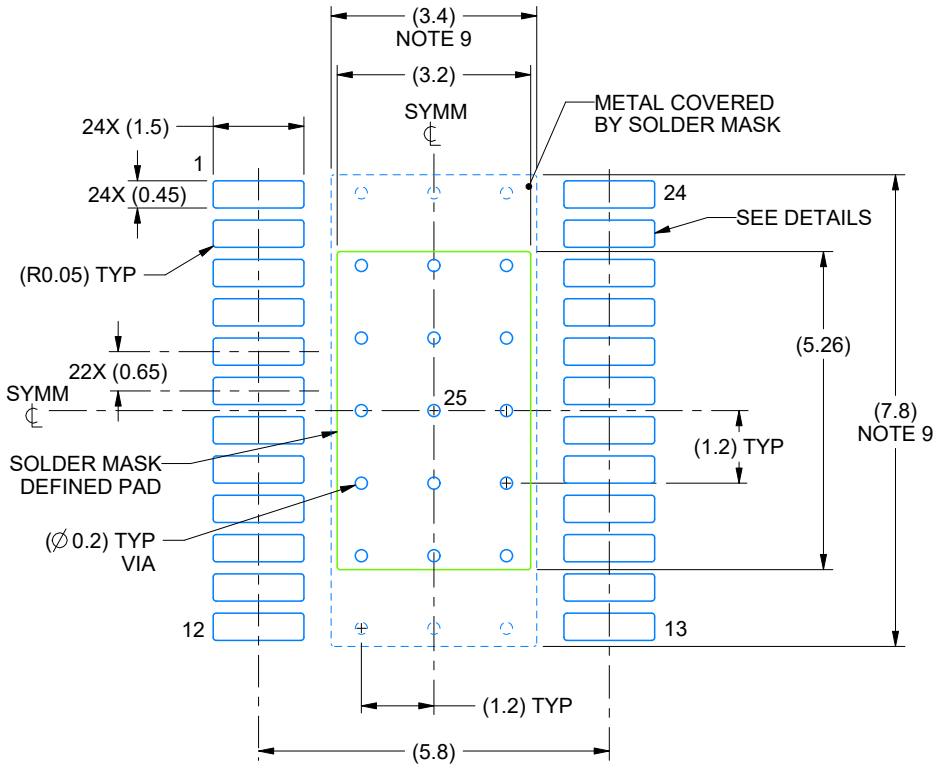
SMALL OUTLINE PACKAGE



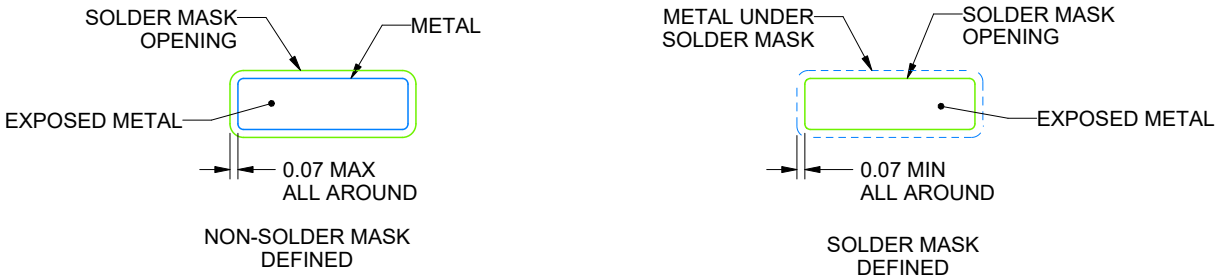
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

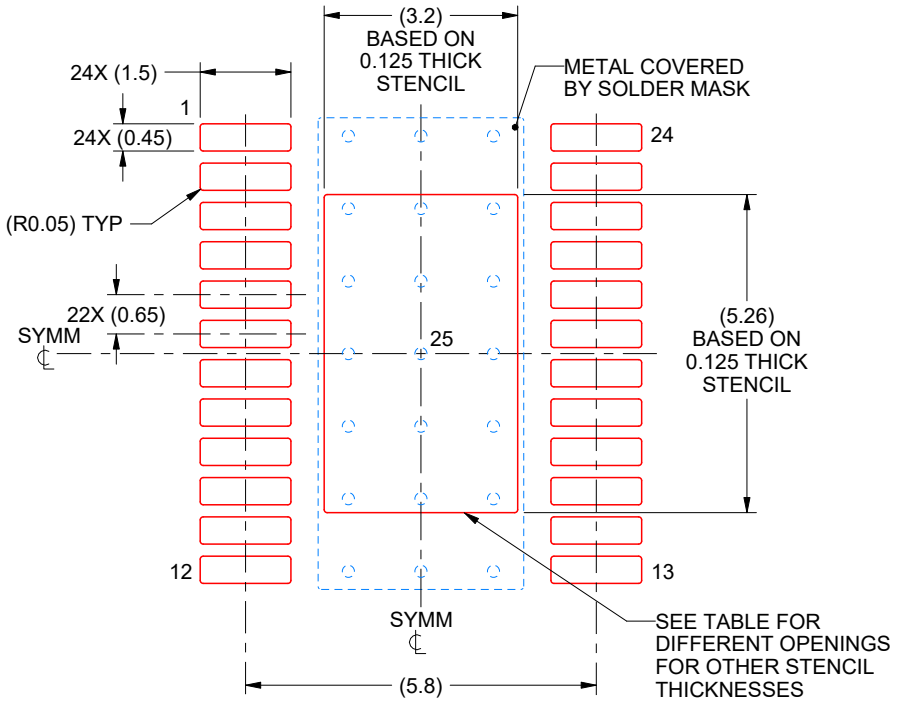


SOLDER MASK DETAILS

4225860/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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